SLG7RN45356

GreenPAK ™

RZ/G2L SMARC POWER_RESET

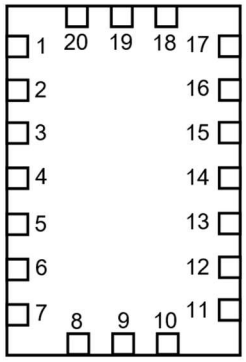
General Description

Renesas SLG7RN45356 is a low power and small form device. The SoC is housed in a 2mm x 3mm STQFN package which is optimal for using with small devices.

Features

- Low Power Consumption
- Pb - Free / RoHS Compliant
- Halogen - Free
- STQFN - 20 Package

Pin Configuration



STQFN-20
(Top View)

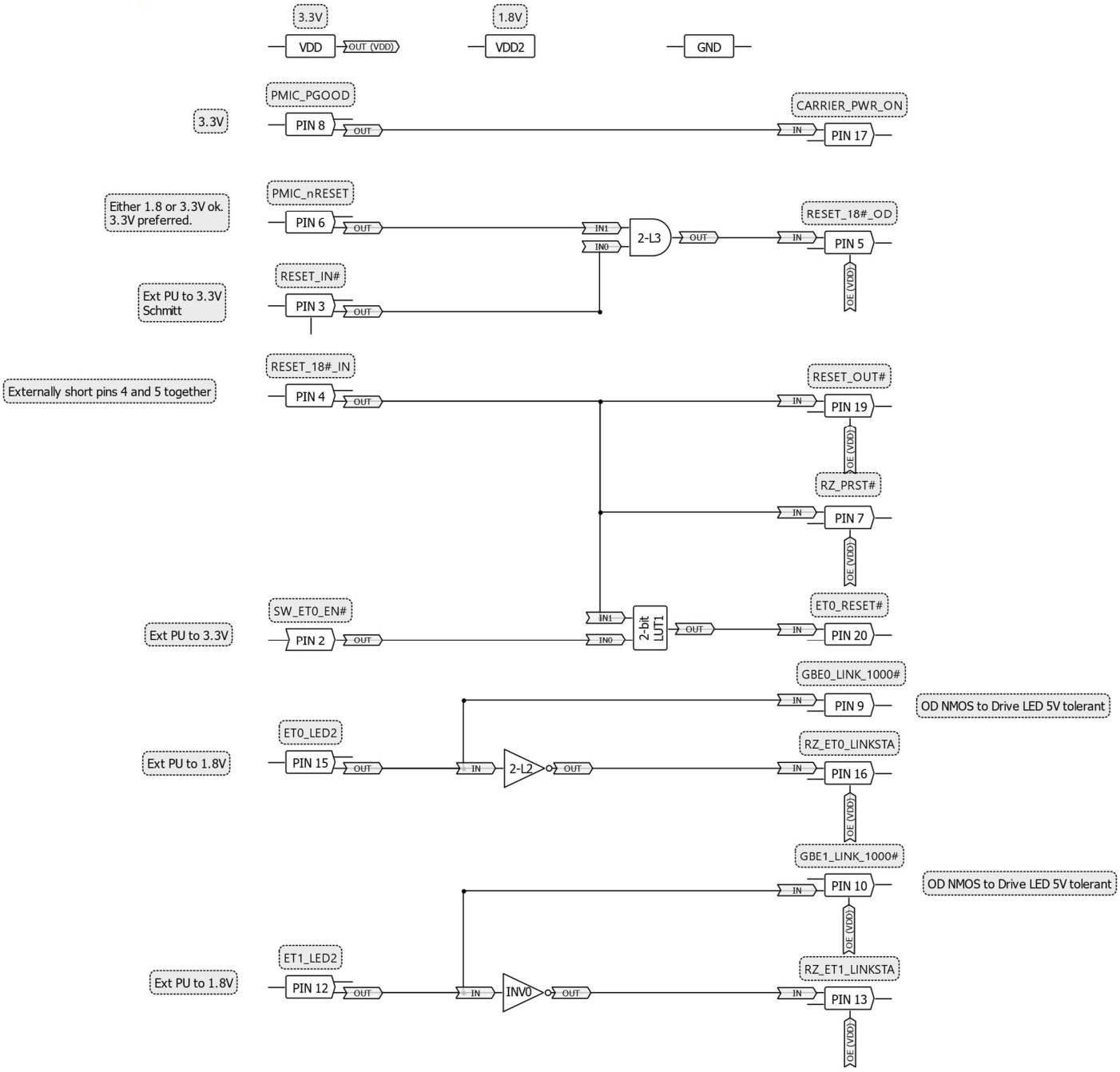
Output Summary

3 Outputs - Open Drain NMOS 2X
4 Outputs - Push Pull 1X
2 Outputs - Push Pull 2X

Pin name

Pin #	Pin name	Pin #	Pin name
1	VDD	11	GND
2	SW_ET0_EN#	12	ET1_LED2
3	RESET_IN#	13	RZ_ET1_LINKSTA
4	RESET_18#_IN	14	VDD2
5	RESET_18#_OD	15	ET0_LED2
6	PMIC_nRESET	16	RZ_ET0_LINKSTA
7	RZ_PRST#	17	CARRIER_PWR_ON
8	PMIC_PGOOD	18	NC
9	GBE0_LINK_1000#	19	RESET_OUT#
10	GBE1_LINK_1000#	20	ET0_RESET#

Block Diagram



Pin Configuration

Pin #	Pin Name	Type	Pin Description	Internal Resistor
1	VDD	PWR	Supply Voltage	--
2	SW_ET0_EN#	Digital Input	Digital Input with Schmitt trigger	floating
3	RESET_IN#	Digital Input	Digital Input with Schmitt trigger	floating
4	RESET_18#_IN	Digital Input	Digital Input without Schmitt trigger	1MΩ pulldown
5	RESET_18#_OD	Digital Output	Open Drain NMOS 2X	floating
6	PMIC_nRESET	Digital Input	Low Voltage Digital Input	floating
7	RZ_PRST#	Digital Output	Push Pull 1X	floating
8	PMIC_PGOOD	Digital Input	Digital Input without Schmitt trigger	floating
9	GBE0_LINK_1000#	Digital Output	Open Drain NMOS 2X	floating
10	GBE1_LINK_1000#	Digital Output	Open Drain NMOS 2X	floating
11	GND	GND	Ground	--
12	ET1_LED2	Digital Input	Low Voltage Digital Input	floating
13	RZ_ET1_LINKSTA	Digital Output	Push Pull 2X	floating
14	VDD2	PWR	Supply Voltage	--
15	ET0_LED2	Digital Input	Low Voltage Digital Input	floating
16	RZ_ET0_LINKSTA	Digital Output	Push Pull 2X	floating
17	CARRIER_PWR_ON	Digital Output	Push Pull 1X	floating
18	NC	--	Keep Floating or Connect to GND	--
19	RESET_OUT#	Digital Output	Push Pull 1X	floating
20	ET0_RESET#	Digital Output	Push Pull 1X	floating

Ordering Information

Part Number	Package Type
SLG7RN45356V	20-pin STQFN - Tape and Reel (3k units)

Absolute Maximum Conditions

Parameter		Min.	Max.	Unit
Supply Voltage on VDD relative to GND		-0.5	7	V
Supply voltage on VDD2 relative to GND		-0.5	VDD + 0.5	V
DC Input voltage	PINs 2, 3, 4, 5, 6, 7, 8, 9, 10	GND - 0.5	VDD + 0.5	V
	PINs 12, 13, 15, 16, 17, 18, 19, 20		VDD2 + 0.5	
Maximum Average or DC Current (Through pin)	Push-Pull 1x	--	11	mA
	Push-Pull 2x	--	16	
	OD 2x	--	21	
Current at Input Pin		-1.0	1.0	mA
Input leakage (Absolute Value)		--	1000	nA
Storage Temperature Range		-65	150	°C
Junction Temperature		--	150	°C
ESD Protection (Human Body Model)		2000	--	V
ESD Protection (Charged Device Model)		500	--	V
Moisture Sensitivity Level		1		

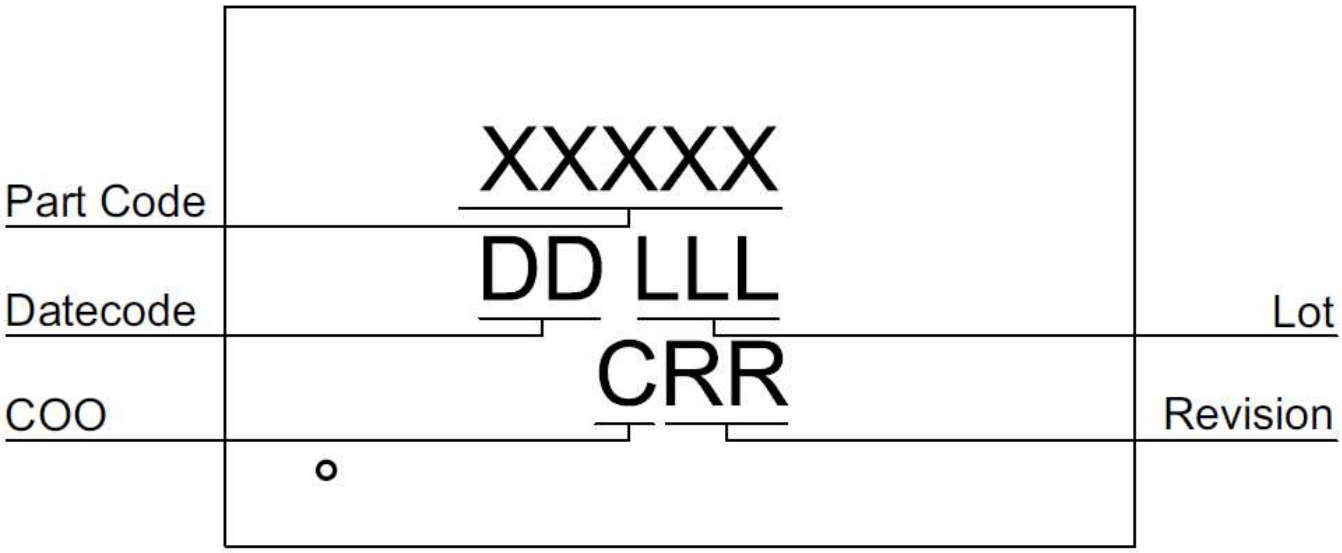
Electrical Characteristics

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		3	3.3	3.6	V
V_{DD2}	Supply Voltage		1.71	1.8	2	V
T_A	Operating Temperature		-40	25	85	°C
C_{VDD}	Capacitor Value at VDD		--	0.1	--	µF
C_{IN}	Input Capacitance		--	4	--	pF
I_Q	Quiescent Current	Static inputs and floating outputs	--	1	--	µA
V_O	Maximal Voltage Applied to any PIN in High-Impedance State		--	--	VDD	V
I_{VDD}	Maximum Average or DC Current Through VDD Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	45	mA
		T_J = 110°C	--	--	22	mA
I_{GND}	Maximum Average or DC Current Through GND Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	86	mA
		T_J = 110°C	--	--	41	mA
V_{IH}	HIGH-Level Input Voltage PINs 2, 3, 4, 5, 6, 7, 8, 9 and 10	Logic Input at VDD=3.3V	1.81	--	VDD	V
		Logic Input with Schmitt Trigger at VDD=3.3V	2.14	--	VDD	V
		Low-Level Logic Input at VDD=3.3V	1.06	--	VDD	V
V_{IH2}	HIGH-Level Input Voltage PINs 12, 13, 15, 16, 17, 18, 19, 20	Low-Level Logic Input at VDD2=1.8V	0.94	--	VDD	V
		Low-Level Logic Input at VDD2=3.3V	1.06	--	VDD	V
V_{IL}	LOW-Level Input Voltage PINs 2, 3, 4, 5, 6, 7, 8, 9 and 10	Logic Input at VDD=3.3V	0	--	1.31	V
		Logic Input with Schmitt Trigger at VDD=3.3V	0	--	0.97	V
		Low-Level Logic Input at VDD=3.3V	0	--	0.67	V
V_{IL2}	LOW-Level Input Voltage PINs 12, 13, 15, 16, 17, 18, 19, 20	Low-Level Logic Input at VDD2=1.8V	0	--	0.52	V
		Low-Level Logic Input at VDD2=3.3V	0	--	0.67	V

V_{OH}	HIGH-Level Output Voltage PINs 2, 3, 4, 5, 6, 7, 8, 9 and 10	Push-Pull 1X, I_{OH}=3mA at VDD=3.3V	2.74	3.12	--	V
V_{OH2}	HIGH-Level Output Voltage PINs 12, 13, 15, 16, 17, 18, 19, 20	Push-Pull 1X, I_{OH}=100µA at VDD2=1.8V	1.69	1.79	--	V
		Push-Pull 1X, I_{OH}=3mA at VDD2=3.3V	2.74	3.12	--	V
		Push-Pull 2X, I_{OH}=100µA at VDD2=1.8V	1.70	1.79	--	V
		Push-Pull 2X, I_{OH}=3mA at VDD2=3.3V	2.87	3.21	--	V
V_{OL}	LOW-Level Output Voltage PINs 2, 3, 4, 5, 6, 7, 8, 9 and 10	Push-Pull 1X, I_{OL}=3mA at VDD=3.3V	--	0.13	0.23	V
		Open Drain NMOS 2X, I_{OL}=3mA at VDD=3.3V	--	0.04	0.08	V
V_{OL2}	LOW-Level Output Voltage PINs 12, 13, 15, 16, 17, 18, 19, 20	Push-Pull 1X, I_{OL}=100µA at VDD2=1.8V	--	0.01	0.03	V
		Push-Pull 1X, I_{OL}=3mA at VDD2=3.3V	--	0.13	0.23	V
		Push-Pull 2X, I_{OL}=100µA at VDD2=1.8V	--	0.01	0.01	V
		Push-Pull 2X, I_{OL}=3mA at VDD2=3.3V	--	0.06	0.11	V
I_{OH}	HIGH-Level Output Current (see Note 1) PINs 2, 3, 4, 5, 6, 7, 8, 9 and 10	Push-Pull 1X, V_{OH}=2.4V at VDD=3.3V	6.05	12.08	--	mA
I_{OH2}	HIGH-Level Output Current (see Note 1) PINs 12, 13, 15, 16, 17, 18, 19, 20	Push-Pull 1X, V_{OH}=VDD-0.2V at VDD2=1.8V	1.07	1.70	--	mA
		Push-Pull 1X, V_{OH}=2.4V at VDD2=3.3V	6.05	12.08	--	mA
		Push-Pull 2X, V_{OH}=VDD-0.2V at VDD2=1.8V	2.22	3.41	--	mA
		Push-Pull 2X, V_{OH}=2.4V at VDD2=3.3V	11.54	24.16	--	mA
I_{OL}	LOW-Level Output Current (see Note 1) PINs 2, 3, 4, 5, 6, 7, 8, 9 and 10	Push-Pull 1X, V_{OL}=0.4V at VDD=3.3V	4.88	8.24	--	mA
		Open Drain NMOS 2X, V_{OL}=0.4V at VDD=3.3V	14.54	24.74	--	mA
I_{OL2}	LOW-Level Output Current (see Note 1) PINs 12, 13, 15, 16, 17, 18, 19, 20	Push-Pull 1X, V_{OL}=0.15V at VDD2=1.8V	0.92	1.69	--	mA
		Push-Pull 1X, V_{OL}=0.4V at VDD2=3.3V	4.88	8.24	--	mA
		Push-Pull 2X, V_{OL}=0.15V at VDD2=1.8V	1.83	3.38	--	mA
		Push-Pull 2X, V_{OL}=0.4V at VDD2=3.3V	9.75	16.49	--	mA
R_{PULL_DOWN}	Internal Pull Down Resistance	Pull down on PIN 4	--	1	--	MΩ
T_{SU}	Startup Time	From VDD rising past PON_{THR}	0.63	1.36	1.87	ms
PON_{THR}	Power On Threshold	V_{DD} Level Required to Start Up the Chip	1.41	1.54	1.66	V
$POFF_{THR}$	Power Off Threshold	V_{DD} Level Required to Switch Off the Chip	1.00	1.15	1.31	V

Note:
1. DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
2. The GreenPAK's power rails are divided in two sides. PINs 2, 3, 4, 5, 6, 7, 8, 9 and 10 are connected to one side, PINs 12, 13, 15, 16, 17, 18, 19, and 20 to another.
3. Guaranteed by Design.

Package Top Marking



XXXXX – Part ID Field: identifies the specific device configuration
DD – Date Code Field: Coded date of manufacture
LLL – Lot Code: Designates Lot #
C – Assembly Site/COO: Specifies Assembly Site/Country of Origin
RR – Revision Code: Device Revision

Datasheet Revision	Programming Code Number	Lock Status	Checksum	Part Code	Revision	Date
0.12	001	U	0xF6DC880D	45356	AA	07/12/2023

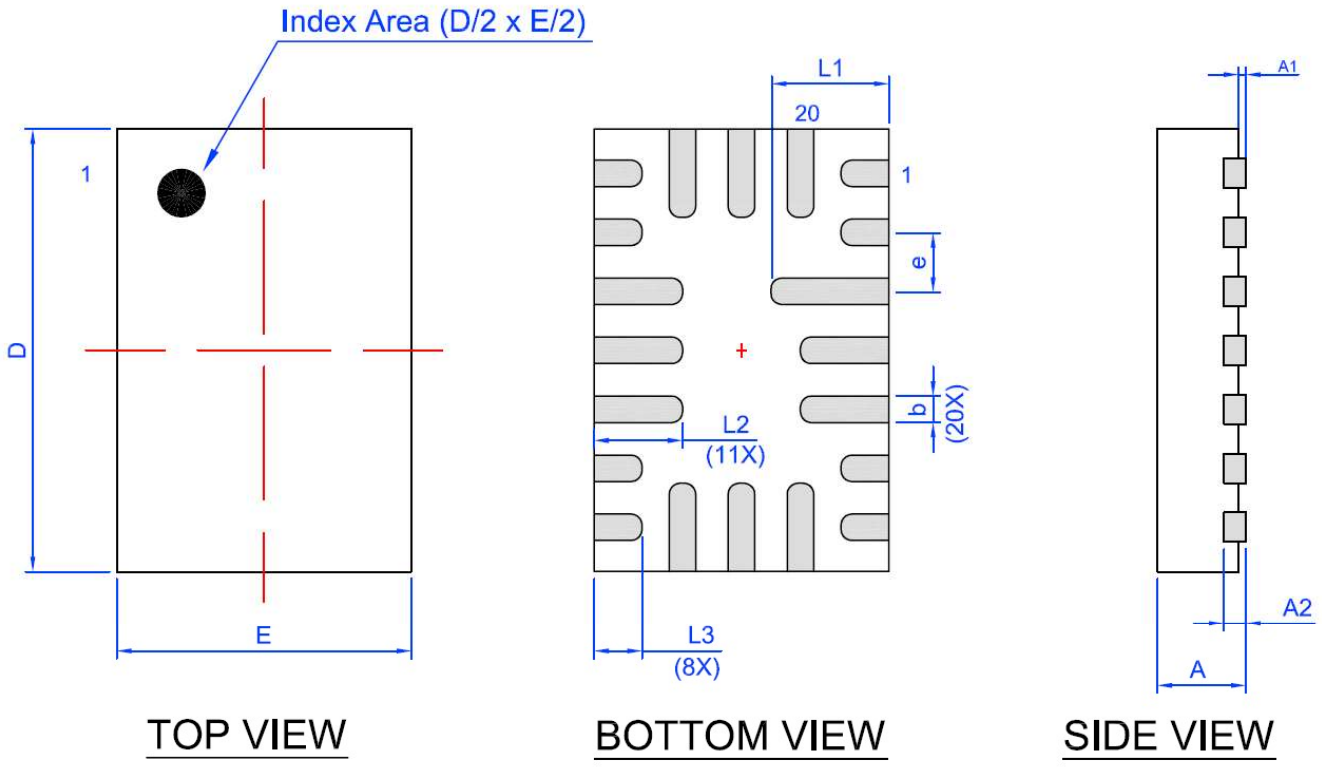
Lock coverage for this part is indicated by √, from one of the following options:

√	Unlocked
	Locked for read, bits <1535:0>
	Locked for write, bits <1535:0>
	Locked for write all bits
	Locked for read and write bits <1535:0>
	Locked for read bits <1535:0> and write of all bits

The IC security bit is locked/set for code security for production unless otherwise specified. The Programming Code Number is not changed based on the choice of locked vs. unlocked status.

Package Drawing and Dimensions

STQFN 20L 2x3mm 0.4P COL Package
JEDEC MO-220



TOP VIEW BOTTOM VIEW SIDE VIEW

Unit: mm

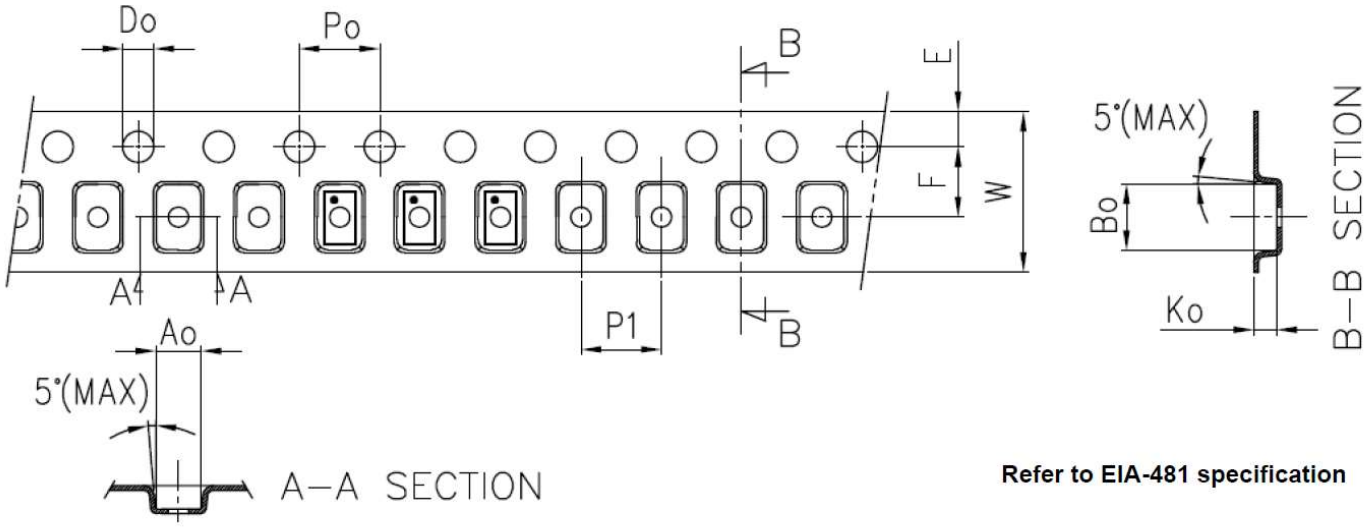
Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.50	0.55	0.60	D	2.95	3.00	3.05
A1	0.005	-	0.050	E	1.95	2.00	2.05
A2	0.10	0.15	0.20	L1	0.75	0.80	0.85
b	0.13	0.18	0.23	L2	0.55	0.60	0.65
e	0.40 BSC			L3	0.275	0.325	0.375

Tape and Reel Specification

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
STQFN 20L 2x3mm 0.4P COL	20	2x3x0.55	3000	3000	178/60	100	400	100	400	8	4

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width
	A0	B0	K0	P0	P1	D0	E	F	W
STQFN 20L 2x3 mm 0.4P COL	2.2	3.15	0.76	4	4	1.5	1.75	3.5	8



Refer to EIA-481 specification

Recommended Reflow Soldering Profile

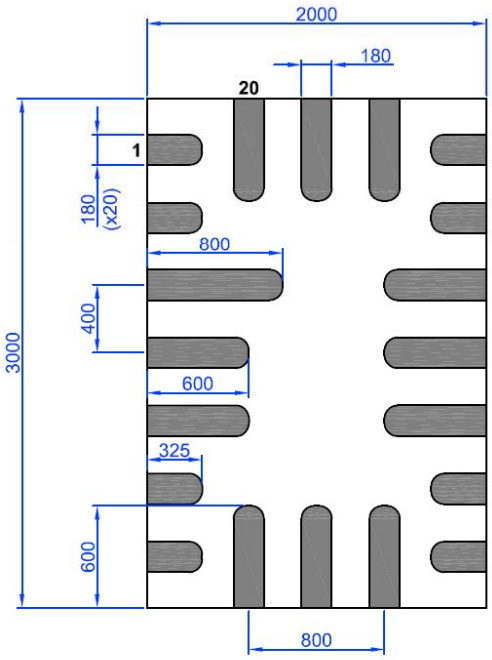
Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 3.30 mm^3 (nominal). More information can be found at www.jedec.org.

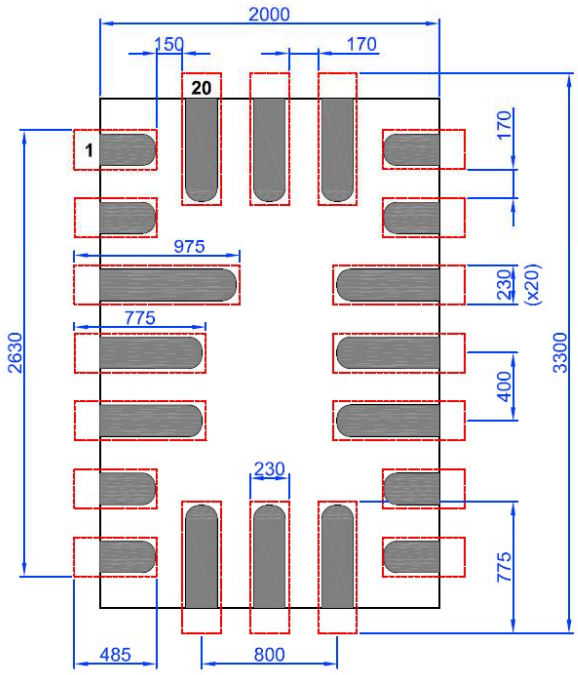
Recommended Land Pattern

Exposed Pad
(Top View)

Recommended Land Pattern
(Top View)

Units: µm





Datasheet Revision History

Date	Version	Change
11/01/2021	0.10	New design for SLG46538V chip
11/02/2021	0.11	Updated Device Revision Table
07/12/2023	0.12	Moved to Renesas template

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