SLG7RN45688

GreenPAK ™

GPIO Expander

General Description

Renesas SLG7RN45688 is a low power and small form device. The SoC is housed in a 2mm x 3mm STQFN package which is optimal for using with small devices.

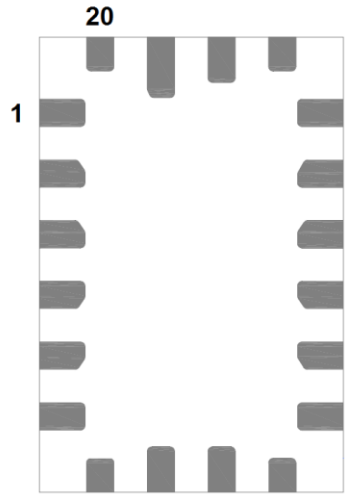
Features

- Low Power Consumption
- Pb - Free / RoHS Compliant
- Halogen - Free
- STQFN - 20 Package

Output Summary

12 Outputs - Push Pull 1X

Pin Configuration

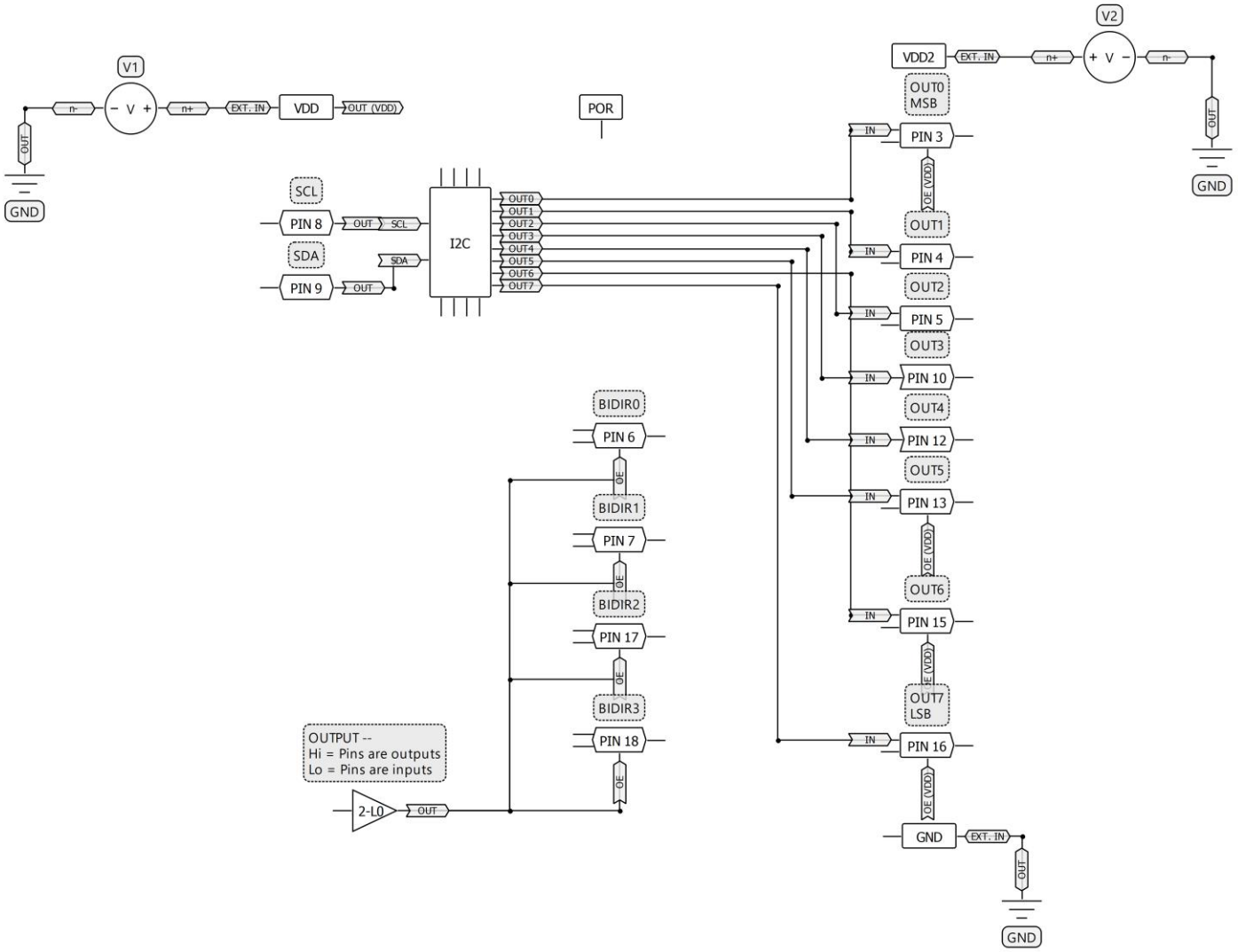


20-pin STQFN
(Top View)

Pin name

Pin #	Pin name	Pin #	Pin name
1	VDD	11	GND
2	NC	12	OUT4
3	OUT0 MSB	13	OUT5
4	OUT1	14	VDD2
5	OUT2	15	OUT6
6	BIDIR0	16	OUT7 LSB
7	BIDIR1	17	BIDIR2
8	SCL	18	BIDIR3
9	SDA	19	NC
10	OUT3	20	NC

Block Diagram



Pin Configuration

Pin #	Pin Name	Type	Pin Description	Internal Resistor
1	VDD	PWR	Supply Voltage	--
2	NC	--	Keep Floating or Connect to GND	--
3	OUT0 MSB	Digital Output	Push Pull 1X	floating
4	OUT1	Digital Output	Push Pull 1X	floating
5	OUT2	Digital Output	Push Pull 1X	floating
6	BIDIR0	Bi-directional	Digital Input without Schmitt trigger / Push Pull 1X	floating
7	BIDIR1	Bi-directional	Digital Input without Schmitt trigger / Push Pull 1X	floating
8	SCL	Digital Input	Digital Input without Schmitt trigger	floating
9	SDA	Digital Input	Digital Input without Schmitt trigger	floating
10	OUT3	Digital Output	Push Pull 1X	floating
11	GND	GND	Ground	--
12	OUT4	Digital Output	Push Pull 1X	floating
13	OUT5	Digital Output	Push Pull 1X	floating
14	VDD2	PWR	Supply Voltage	--
15	OUT6	Digital Output	Push Pull 1X	floating
16	OUT7 LSB	Digital Output	Push Pull 1X	floating
17	BIDIR2	Bi-directional	Digital Input without Schmitt trigger / Push Pull 1X	floating
18	BIDIR3	Bi-directional	Digital Input without Schmitt trigger / Push Pull 1X	floating
19	NC	--	Keep Floating or Connect to GND	--
20	NC	--	Keep Floating or Connect to GND	--

Ordering Information

Part Number	Package Type
SLG7RN45688V	20-pin STQFN
SLG7RN45688VTR	20-pin STQFN - Tape and Reel (3k units)

Absolute Maximum Conditions

Parameter		Min.	Max.	Unit
V_{HIGH} to GND		-0.3	7	V
Voltage at Input Pin		GND-0.5V	VDD+0.5V	V
Maximum Average or DC Current Through V_{DD} Pin		--	90	mA
Maximum Average or DC Current Through V_{DD2} Pin		--	90	mA
Maximum Average or DC Current Through GND Pin (Per chip side, (Note 1))		--	100	mA
Maximum Average or DC Current (Through pin)	Push-Pull 1x	--	15.3	mA
Current at Input Pin		-1.0	1.0	mA
Input leakage (Absolute Value)		--	1000	nA
Storage Temperature Range		-65	150	°C
Junction Temperature		--	150	°C
ESD Protection (Human Body Model)		2000	--	V
ESD Protection (Charged Device Model)		1300	--	V
Moisture Sensitivity Level		1		
Note 1 The GreenPAK's GND rail is divided in two sides. IOs 0 to 6, SCL, SDA are connected to one side and IOs 7 to 14 are connected to another side.				

Electrical Characteristics

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		2.3	3.3	5.5	V
V_{DD2}	Supply Voltage		1.71	3.3	5.5	V
T_A	Operating Temperature		-40	25	85	°C
C_{VDD}	Capacitor Value at VDD		--	0.1	--	µF
C_{IN}	Input Capacitance		--	4	--	pF
I_Q	Quiescent Current	Static inputs and floating outputs	--	1	--	µA
V_O	Maximal Voltage Applied to any PIN in High-Impedance State		--	--	VDD+0.3	V
V_{IH}	HIGH-Level Input Voltage (Note 1)	Logic Input at VDD=2.5V	0.7xVDD	--	VDD+0.3	V
		Logic Input at VDD=3.3V	0.7xVDD	--	VDD+0.3	V
		Logic Input at VDD=5.0V	0.7xVDD	--	VDD+0.3	V
V_{IL}	LOW-Level Input Voltage (Note 1)	Logic Input at VDD=2.5V	GND-0.3	--	0.3xVDD	V
		Logic Input at VDD=3.3V	GND-0.3	--	0.3xVDD	V
		Logic Input at VDD=5.0V	GND-0.3	--	0.3xVDD	V
V_{OH}	HIGH-Level Output Voltage (Note 1)	Push-Pull 1X, I_{OH}=100µA at VDD=2.5V	2.389	--	--	V
		Push-Pull 1X, I_{OH}=3mA at VDD=3.3V	3.039	--	--	V
		Push-Pull 1X, I_{OH}=5mA at VDD=5.0V	4.678	--	--	V
V_{OL}	LOW-Level Output Voltage (Note 1)	Push-Pull 1X, I_{OL}=100µA, at VDD=2.5V	--	--	0.079	V
		Push-Pull 1X, I_{OL}=3mA, at VDD=3.3V	--	--	0.195	V
		Push-Pull 1X, I_{OL}=5mA, at VDD=5.0V	--	--	0.256	V

I_{OH}	HIGH-Level Output Current (Note 1)	Push-Pull 1X, VOH=VDD-0.2V at VDD=2.5V	1.76	--	--	mA
		Push-Pull 1X, VOH=2.4V at VDD=3.3V	8.56	--	--	mA
		Push-Pull 1X, VOH=2.4V at VDD=5.0V	25.12	--	--	mA
I_{OL}	LOW-Level Output Current (Note 1)	Push-Pull 1X, V_{OL}=0.15V, at VDD=2.5V	1.87	--	--	mA
		Push-Pull 1X, V_{OL}=0.4V, at VDD=3.3V	5.90	--	--	mA
		Push-Pull 1X, V_{OL}=0.4V, at VDD=5.0V	7.67	--	--	mA
T_{SU}	Startup Time	From VDD rising past PON_{THR}	--	1.66	2.59	ms
PON_{THR}	Power On Threshold	V_{DD} Level Required to Start Up the Chip	1.60	1.85	2.07	V
$POFF_{THR}$	Power Off Threshold	V_{DD} Level Required to Switch Off the Chip	0.97	1.23	1.46	V

Note:
1. PINs 1 to 10 are powered from VDD and PINs 12 to 20 are powered from VDD2.
2. Guaranteed by Design.

I²C Specifications

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
F_{SCL}	Clock Frequency, SCL	V_{DD} = (2.3...5.5) V	--	--	400	kHz
t_{LOW}	Clock Pulse Width Low	V_{DD} = (2.3...5.5) V	1300	--	--	ns
t_{HIGH}	Clock Pulse Width High	V_{DD} = (2.3...5.5) V	600	--	--	ns
t_I	Input Filter Spike Suppression (SCL, SDA)	V_{DD} = (2.3...5.5) V	--	--	95	ns
t_{AA}	Clock Low to Data Out Valid	V_{DD} = (2.3...5.5) V	--	--	900	ns
t_{BUF}	Bus Free Time between Stop and Start	V_{DD} = (2.3...5.5) V	1300	--	--	ns
t_{HD_STA}	Start Hold Time	V_{DD} = (2.3...5.5) V	600	--	--	ns
t_{SU_STA}	Start Set-up Time	V_{DD} = (2.3...5.5) V	600	--	--	ns
t_{HD_DAT}	Data Hold Time	V_{DD} = (2.3...5.5) V	0	--	--	ns
t_{SU_DAT}	Data Set-up Time	V_{DD} = (2.3...5.5) V	100	--	--	ns
t_R	Inputs Rise Time	V_{DD} = (2.3...5.5) V	--	--	300	ns
t_F	Inputs Fall Time	V_{DD} = (2.3...5.5) V	--	--	300	ns
t_{SU_STO}	Stop Set-up Time	V_{DD} = (2.3...5.5) V	600	--	--	ns
t_{DH}	Data Out Hold Time	V_{DD} = (2.3...5.5) V	50	--	--	ns

Chip address

HEX	BIN	DEC
0x08	0001000	8

I2C Description

1. I2C Basic Command Structure

Each command to the I2C Serial Communications block begins with a Control Byte. The bits inside this Control Byte are shown in Figure 1. After the Start bit, the first four bits are a control code, which can be set by the user in reg<1623:1620>. The Block Address is the next three bits (A10, A9, A8), which will define the most significant bits in the addressing of the data to be read (“1”) or written (“0”) by the command. This Control Byte will be followed by an Acknowledge bit (ACK).

With the exception of the Current Address Read command, all commands will have the Control Byte followed by the Word Address. The Word Address, in conjunction with the three address bits in the Control Byte, will define the specific data byte to be read or written in the command. Figure 1 shows this basic command structure.

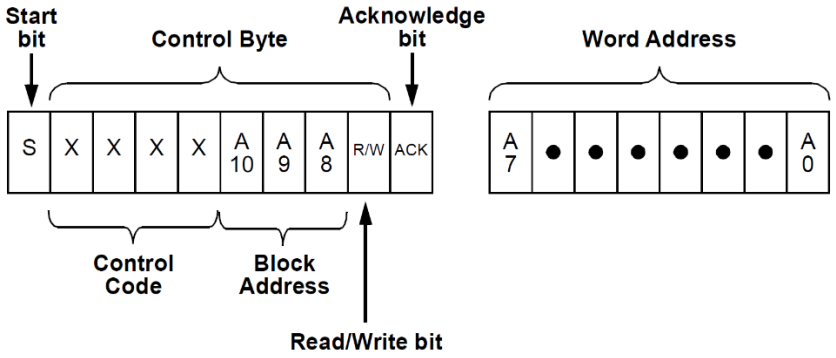


Figure1. I2C Basic Command Structure

2. I2C Serial General Timing

Shown in Figure 2 is the general timing characteristics for the I2C Serial Communications block.

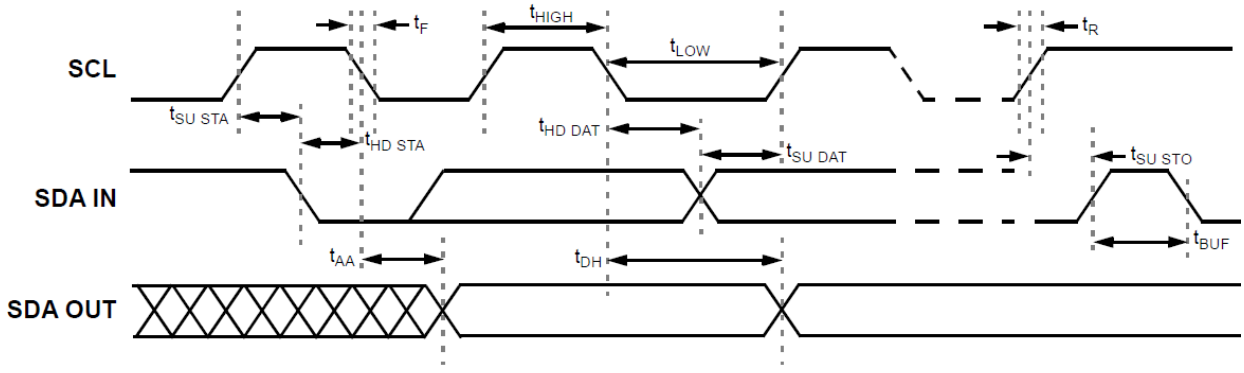


Figure2. I2C Serial General Timing

3. I2C Serial Communications: Read and Write Commands

Following the Start condition from the master, the Control Code [4 bits], the block address [3 bits] and the R/W bit (set to “0”), is placed onto the bus by the Bus Master. After the I2C Serial Communications block has provided an Acknowledge bit (ACK) the next byte transmitted by the master is the Word Address. The Block Address is the next three bits, and is the higher order addressing bits (A10, A9, A8), which when added to the Word Address will together set the internal address pointer in the SLG7RN45688 to the correct data byte to be written. After the SLG7RN45688 sends another Acknowledge bit, the Bus Master will transmit the data byte to be written into the addressed memory location. The SLG7RN45688 again provides an Acknowledge bit and then the Bus Master generates a Stop condition. The internal write cycle for the data will take place at the time that the SLG7RN45688 generates the Acknowledge bit.

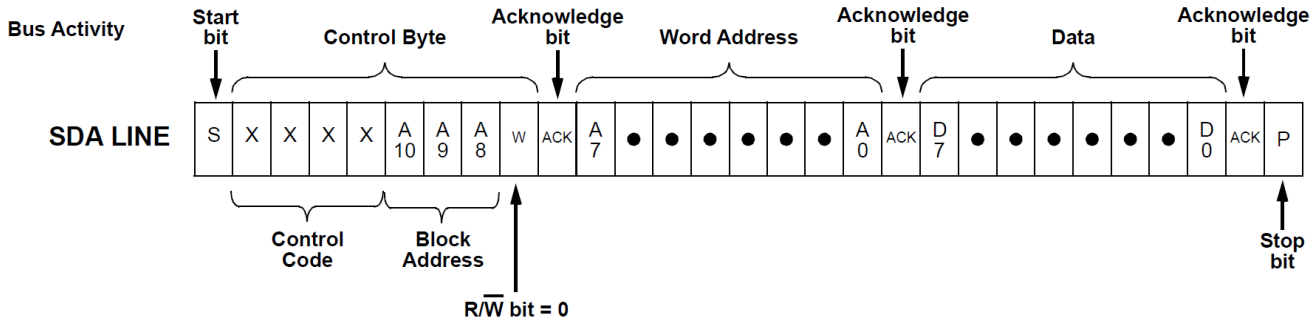


Figure3. I2C Write Command

The Random Read command starts with a Control Byte (with R/$\overline{W}$ bit set to “0”, indicating a write command) and Word Address to set the internal byte address, followed by a Start bit, and then the Control Byte for the read (exactly the same as the Byte Write command). The Start bit in the middle of the command will halt the decoding of a Write command, but will set the internal address counter in preparation for the second half of the command. After the Start bit, the Bus Master issues a second control byte with the R/$\overline{W}$ bit set to “1”, after which the SLG7RN45688 issues an Acknowledge bit, followed by the requested eight data bits.

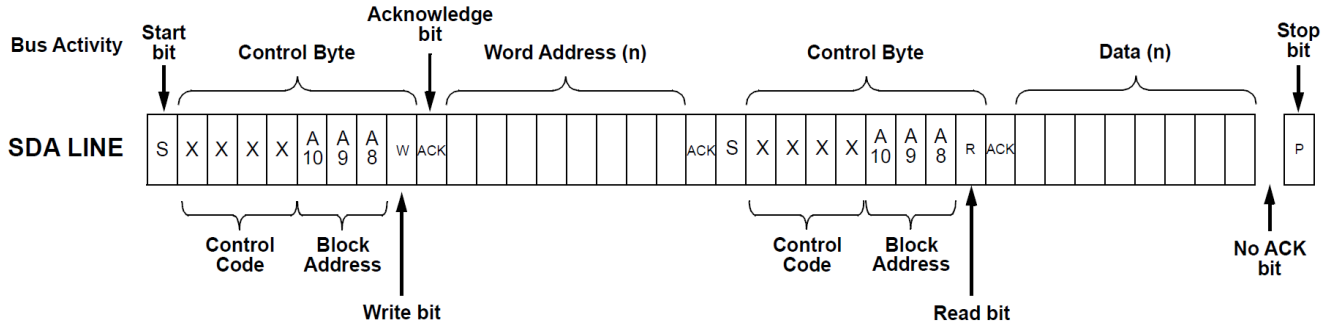


Figure4. I2C Random Read Command

4. Chip reconfiguration

SLG7RN45688 has an ISP capability. This means that the chip internal blocks configuration may be changed on the fly or even re-programmed via I2C. If there is a need for temporary change of the chip configuration (it will be reset to the programmed configuration after the chip is reset or powered ON again) one should use Registers (A10, A9, A8 = “000”). To reprogram a configuration via I2C NVM should be accessed with A10, A9, A8 = “010”. Please keep in mind that random byte write procedure is not supported, this may lead to incorrect chip configuration. Only page write procedure is supported.

5. I2C register control data

Address Byte	Register Bit	Block	Function
0x7A	reg<983>	Virtual Input <0>	Enable (0) and disable (1) switch Pin3 Default is 0.
	reg<982>	Virtual Input <1>	Enable (0) and disable (1) switch Pin4 Default is 0.
	reg<981>	Virtual Input <2>	Enable (0) and disable (1) switch Pin5 Default is 0.
	reg<980>	Virtual Input <3>	Enable (0) and disable (1) switch Pin10 Default is 0.
	reg<979>	Virtual Input <4>	Enable (0) and disable (1) switch Pin12 Default is 0.
	reg<978>	Virtual Input <5>	Enable (0) and disable (1) switch Pin13 Default is 0.
	reg<977>	Virtual Input <6>	Enable (0) and disable (1) switch Pin15 Default is 0.
	reg<976>	Virtual Input <7>	Enable (0) and disable (1) switch Pin16 Default is 0.
0x00	reg<5:0>	IN0 of LUT2_0	Matrix OUT0, control Pin6, 7, 17, 18 Input or Output mode.
0x36	reg<437:432>	IO4 Digital Output	Matrix OUT72, control Pin6 to H or L
0x37	reg<449:444>	IO5 Digital Output	Matrix OUT74, control Pin7 to H or L
0x38			
0x3F	reg<509:504>	IO11 Digital Output	Matrix OUT84, control Pin17 to H or L
0x40	reg<521:516>	IO12 Digital Output	Matrix OUT86, control Pin18 to H or L
0x41			
0xC8	reg<1601>	I2C reset bit with reloading NVM into Data register (soft reset)	0: Keep existing condition 1: Reset execution
0x74	reg<933>	IO4 Digital Input	Pin6 input status
	reg<934>	IO5 Digital Input	Pin7 input status
0x75	reg<938>	IO11 Digital Input	Pin17 input status
	reg<939>	IO12 Digital Input	Pin18 input status
0x71	reg<905:904>	IO12 input mode configuration	00: digital in without Schmitt Trigger 10: low voltage digital in mode
0xE3	reg<1820:1816>	Page Selection for Erase ERSEB[4:0]	Define the page address which will be erased. ERSEB[4] = 0 corresponds to the upper 2k NVM used for chip configuration;
	reg<1823>	Erase Enable ERSE	0: erase disable 1: cause the NVM erase: full NVM (4k bits) erase for ERSCHIP = 1 (reg[1973]) if DIS_ERSCHIP = 0 (reg[1972]) or page erase for ERSCHIP = 0 (reg[1973]).

6. I2C control code and device address relationship

Control code bin	Control byte, read/write	Device address, dec/hex
0000	0x01/0x00	0/0x00
0001(default)	0x11/0x10	8/0x08
0010	0x21/0x20	16/0x10
0011	0x31/0x30	24/0x18
0100	0x41/0x40	32/0x20
0101	0x51/0x50	40/0x28

Control code can from 0000 to 1111. Please check GreenPAK designer I2C marcocell for more information.

7. I2C Commands:

1. [start] [0x08] [w] [0x7A] [(OUT0)xxxxxxx] [stop] // write 1 to switch PIN3(OUT0 MSB) to High
2. [start] [0x08] [w] [0x7A] [x(OUT1)xxxxxx] [stop] // write 1 to switch PIN4(OUT1) to High
3. [start] [0x08] [w] [0x7A] [xx(OUT2)xxxxx] [stop] // write 1 to switch PIN5(OUT2) to High
4. [start] [0x08] [w] [0x7A] [xxx(OUT3)xxxx] [stop] // write 1 to switch PIN10(OUT3) to High
5. [start] [0x08] [w] [0x7A] [xxxx(OUT4)xxx] [stop] // write 1 to switch PIN12(OUT4) to High
6. [start] [0x08] [w] [0x7A] [xxxxx(OUT5)xx] [stop] // write 1 to switch PIN13(OUT5) to High
7. [start] [0x08] [w] [0x7A] [xxxxxx(OUT6)x] [stop] // write 1 to switch PIN15(OUT6) to High
8. [start] [0x08] [w] [0x7A] [0xFF] [stop] // set all 8 pins outputs high
9. [start] [0x08] [w] [0x7A] [0xB2] [stop] // set the pins as (MSB) 10110010 (LSB)
10. [start] [0x08] [w] [0x7A] [xxxxxxx(OUT7)] [stop] // write 1 to switch PIN16(OUT7 LSB) to High
11. [start] [0x08] [w] [0x00] [0xE3] [stop] // switch PIN6, 7, 17, 18 to output mode
12. [start] [0x08] [w] [0x00] [0x00] [stop] // switch PIN6, 7, 17, 18 to Input mode(default)
13. [start] [0x08] [w] [0x36] [0xBE] [stop] // switch PIN6 to High(When Pin set to Output mode)
14. [start] [0x08] [w] [0x36] [0x80] [stop] // switch PIN6 to LOW(When Pin set to Output mode)
15. [start] [0x08] [w] [0x37] [0xE3][0x3B] [stop] // switch PIN7 to High(When Pin set to Output mode)
16. [start] [0x08] [w] [0x37] [0x03][0x38] [stop] // switch PIN7 to LOW(When Pin set to Output mode)
17. [start] [0x08] [w] [0x3F] [0xBE] [stop] // switch PIN17 to High(When Pin set to Output mode)
18. [start] [0x08] [w] [0x3F] [0x80] [stop] // switch PIN17 to LOW(When Pin set to Output mode)
19. [start] [0x08] [w] [0x40] [0xE3][0x3B] [stop] // switch PIN18 to High(When Pin set to Output mode)
20. [start] [0x08] [w] [0x40] [0x03][0x38] [stop] // switch PIN18 to LOW(When Pin set to Output mode)
21. [start] [0x08] [w] [0x74] [stop] [start] [0x08] [R] [x(PIN7)(PIN6)xxxxx] [stop] // read Pin6 and Pin7 input status
22. [start] [0x08] [w] [0x75] [stop] [start] [0x08] [R] [xxxx(PIN18)(PIN17)xx] [stop] // read Pin18 and Pin17 input status
23. [start] [0x08] [w] [0xC8] [0x02] [stop] // I2C reset bit with reloading NVM into Data register (soft reset)
24. [start] [0x08] [w] [0x71] [0x02] [stop] // Change Pin18 Input mode as Low voltage digital Input, default is 0x00
25. [start] [0x08] [w] [0xE3] [0x90] [stop] // erase the EEPROM

8. SERIAL NVM WRITE OPERATIONS:

Write access to the NVM is possible by setting A3 A2 A1 A0 to “0000”, which allows serial write data for a single page only. Upon receipt of the proper Control Byte and Word Address bytes, the SLG46826 will send an ACK. The device will then be ready to receive page data, which is 16 sequential writes of 8-bit data words. The SLG46826 will respond with an ACK after each data word is received. The addressing device, such as a bus Master, must then terminate the write operation with a Stop condition after all page data is written. At that time the device will enter an internally self-timed write cycle, which will be completed within tWR. While the data is being written into the NVM Memory Array, all inputs, outputs, internal logic, and I2C access to the Registerdata will be operational/valid. Please refer to Figure 3 for the SLG46826 Memory Map.

A10 will be ignored during communication to SLG46826.

A9 = 1 will enable access to the NVM.

A9 = 1 and A8 = 0 corresponds to the 2K bits chip configuration NVM data.

A9 = 1 and A8 = 1 corresponds to the 2K bits of emulated EEPROM data.

A3, A2, A1, and A0 should be 0000 for the page write operation.

	I^2C Block Address			Memory Space
Lowest I^2C Address = 000h	A10 = 0	A9 = 0	A8 = X	2 Kbits Register Data Configuration
	A10 = 0	A9 = 1	A8 = 0	2 Kbits NVM Data Configuration
	A10 = 0	A9 = 1	A8 = 1	2 Kbits EEPROM
Highest I^2C Address = 7FFh	A10 = 1	A9 = X	A8 = X	Not Used

Figure5. I2C Block Addressing

9. SERIAL NVM ERASE OPERATIONS:

The erase scheme allows a 16 byte page in the emulated EEPROM space or in the NVM chip configuration space to be erased by modifying the contents of the Erase Register (ERSR). When the ERSE bit is set in the ERSR register, the device will start a self-timed erase cycle which will complete in a maximum of tER ms.

The VDD pin requires a voltage ranging from 2.5 V to 5.5 V for Programming and Erase operations.

Changing the state of the ERSR is accomplished with a Byte Write sequence with the requirements outlined in this section.

The ERSR register is located on I2C Block Address = 000b, I2C Word Address = E3H

The ERSR format is shown in Table 55, and the ERSR bit functions are included in Table 56.

Table 55: Erase Register Bit format

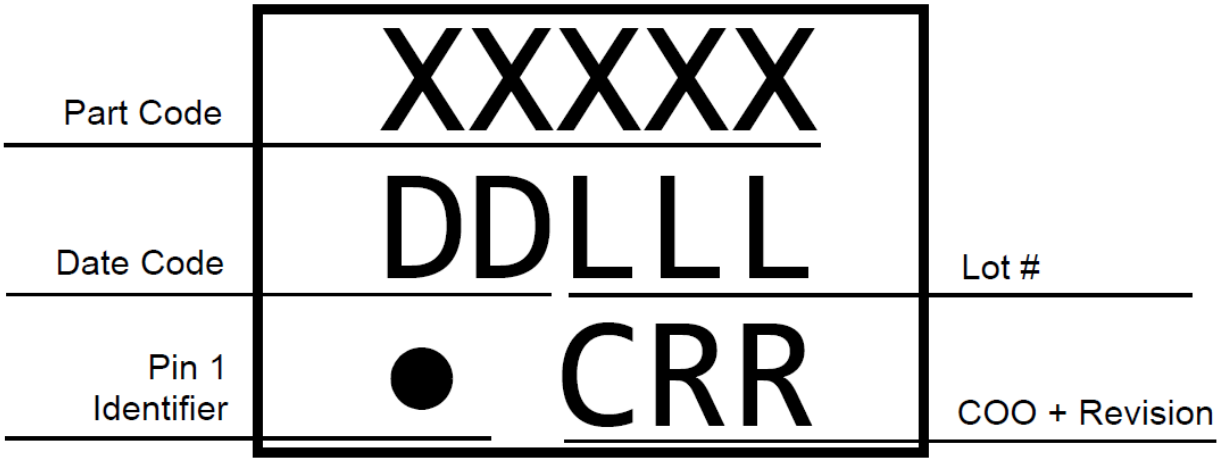
	b7	b6	b5	b4	b3	b2	b1	b0
Page Erase Register	ERSE	--	--	ERSEB4	ERSEB3	ERSEB2	ERSEB1	ERSEB0

Table 56: Erase Register Bit Function Description

Bit	Name		Type	Description
7	ERSE	Erase Enable	W	Setting b7 bit to "1" will start an internal erase cycle on the page defined by ERSEB4-0
6	--	--	--	--
5	--	--	--	--
4	ERSEB4	Page Selection for Erase	W	Define the page address, which will be erased. ERSB4 = 0 corresponds to the Upper 2K NVM used for chip configuration; ERSB4 = 1 corresponds to the 2-k emulated EEPROM.
3	ERSEB3		W	
2	ERSEB2		W	
1	ERSEB1		W	
0	ERSEB0		W	

Upon receipt of the proper Device Address and Erase Register Address, the SLG46826 will send an ACK. The device will then be ready to receive Erase Register data. The SLG46826 will respond with an ACK after Erase Register data word is received. The addressing device, such as a bus Master, must then terminate the write operation with a Stop condition. At that time the device will enter an internally self-timed erase cycle, which will be completed within tER ms. While the data is being written into the Memory Array, all inputs, outputs, internal logic, and I2C access to the Register data will be operational/valid. After the erase has taken place, the contents of ERSE bits will be set to “0” automatically. The internal erase cycle will be triggered at the time the Stop Bit in the I2C command is received.

Package Top Marking



XXXXX - Part ID FieldL identifies the specific device configuration
DD - Date Code Field: Coded date of manufacture
LLL - Lot Code: Designates Lot #
C - Assembly Site/COO: Specifies Assembly Site/Country of Origin
RR - Revision Code: Device Revision

Datasheet Revision	Programming Code Number	Lock Status	Checksum	Part Code	Revision	Date
0.10	001	U	0xC119FFAF			04/07/2022

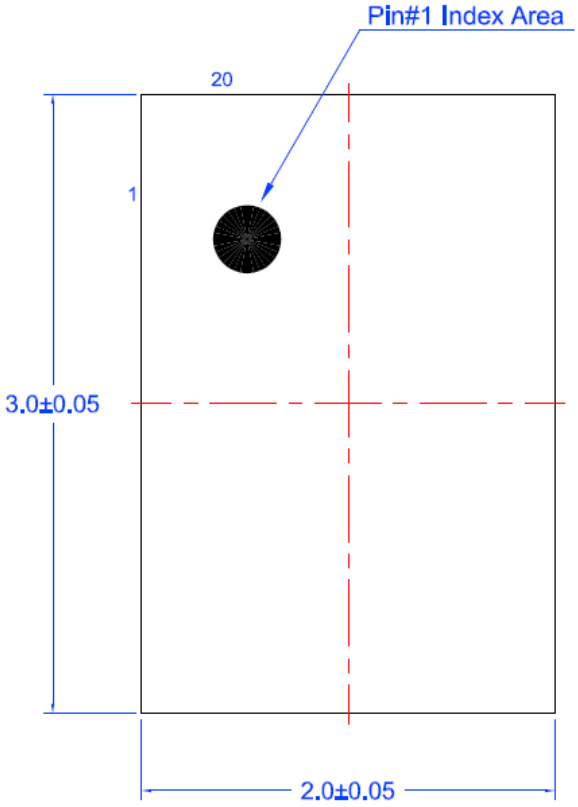
Lock coverage for this part is indicated by √, from one of the following options:

√	Unlocked
	Partly lock read
	Partly lock write
	Partly lock read and write
	Partly lock read and lock write
	Lock read and partly lock write
	Read lock
	Write lock
	Lock read and write

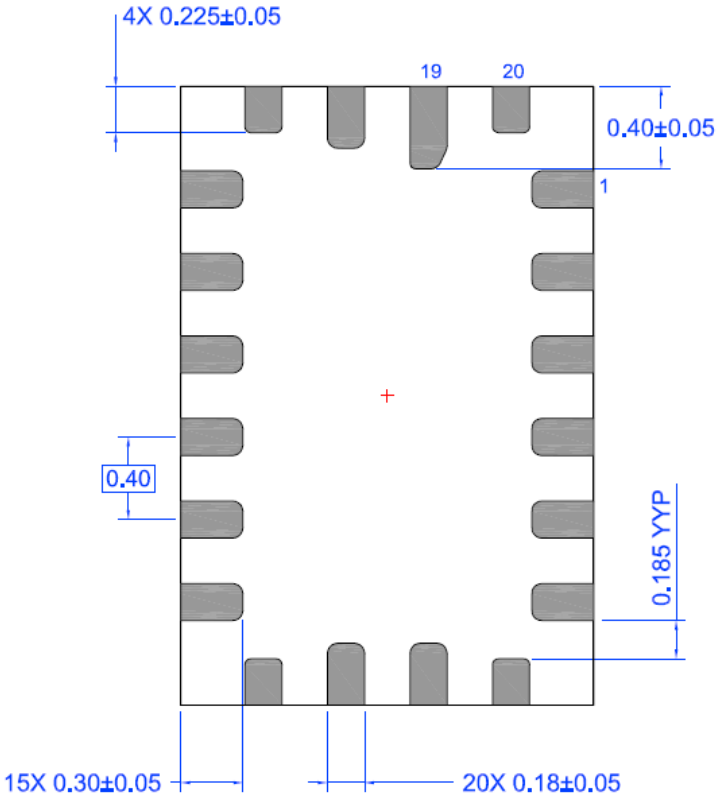
The IC security bit is locked/set for code security for production unless otherwise specified. The Programming Code Number is not changed based on the choice of locked vs. unlocked status.

Package Outlines

STQFN 20L 2x3mm 0.4P FCD Package
IC Net Weight: 0.008 g



Marking View



BTM View

Side View

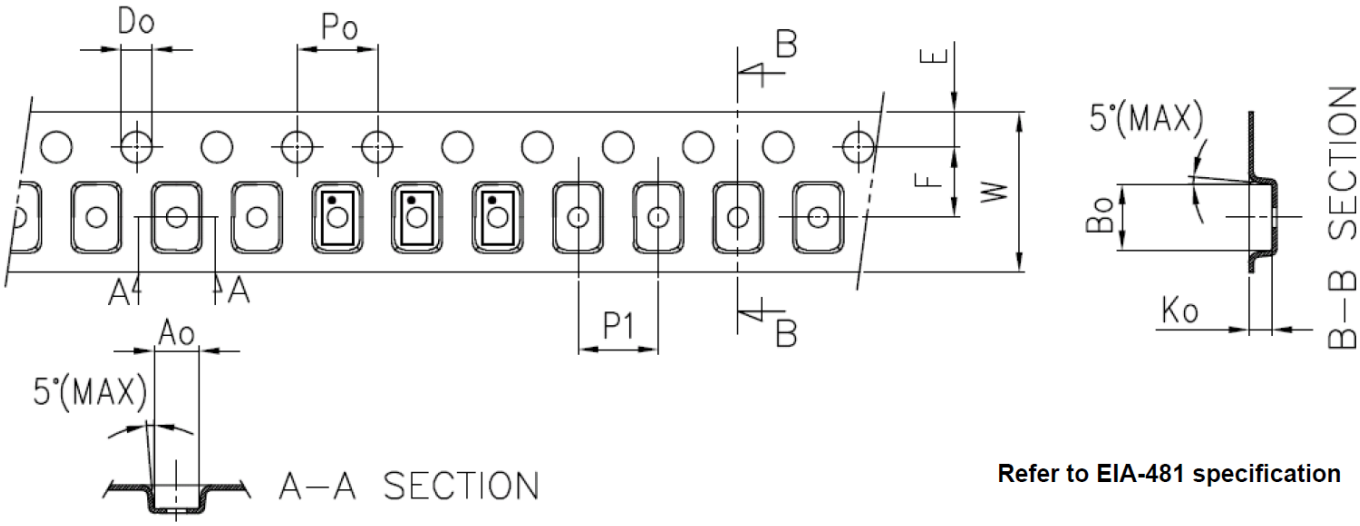
Unit: mm

Tape and Reel Specification

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
STQFN 20L 2x3mm 0.4P FCD	20	2 x 3 x 0.55	3000	3000	178 / 60	100	400	100	400	8	4

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width
	A0	B0	K0	P0	P1	D0	E	F	W
STQFN 20L 2x3mm 0.4P FCD	2.2	3.15	0.76	4	4	1.5	1.75	3.5	8

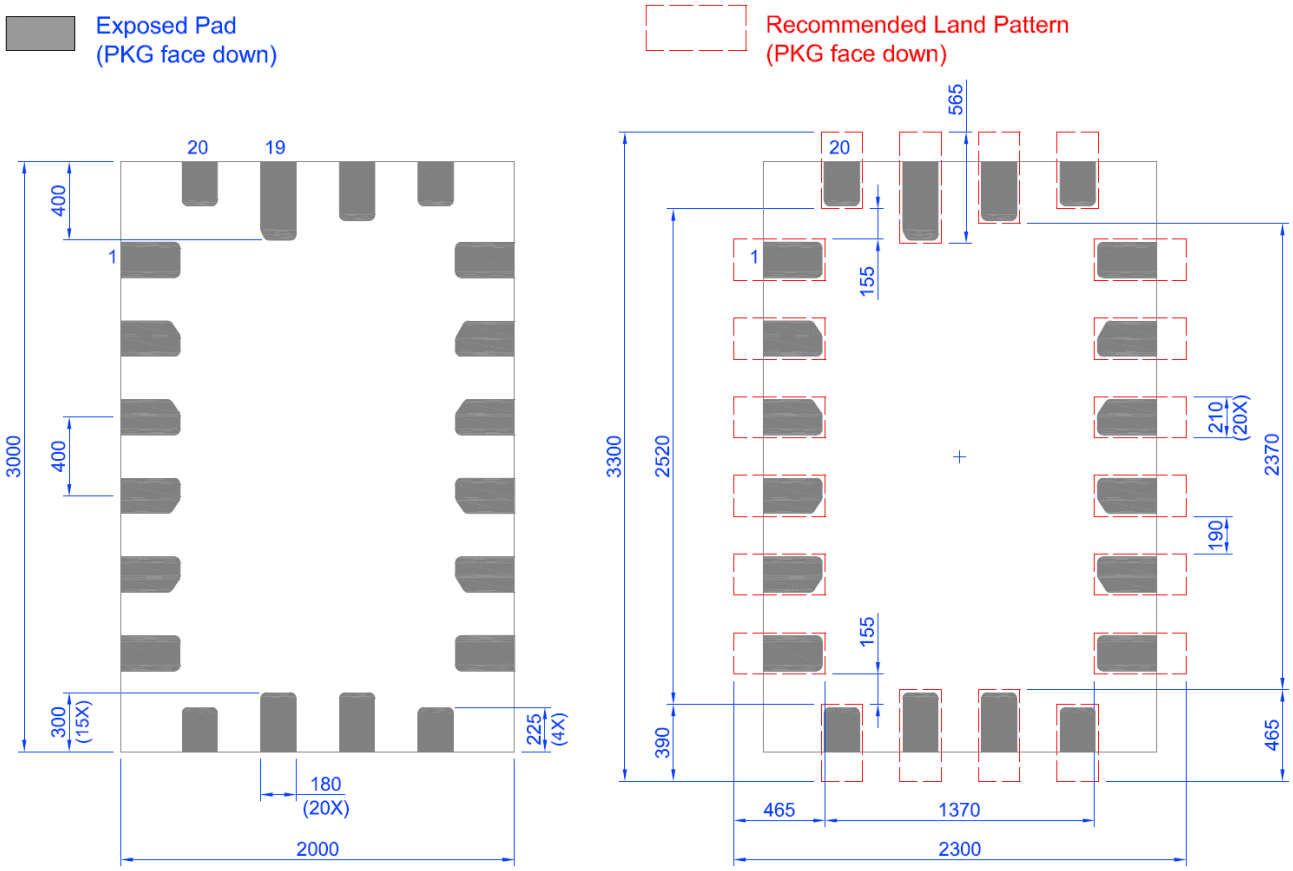


Refer to EIA-481 specification

Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 3.30 mm^3 (nominal). More information can be found at www.jedec.org.

Layout Guidelines



Unit: µm

Datasheet Revision History

Date	Version	Change
04/07/2022	0.10	New design for SLG46826 chip

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