

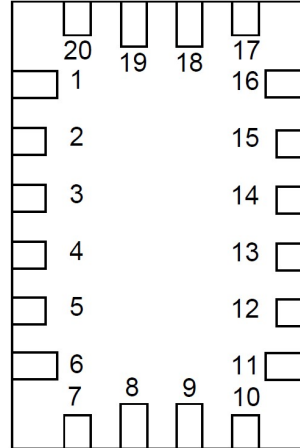
General Description

Dialog SLG7RN45803 is a low power and small form device. The SoC is housed in a 2mm x 3mm STQFN package which is optimal for using with small devices.

Features

- Low Power Consumption
- Pb - Free / RoHS Compliant
- Halogen - Free
- STQFN - 20 Package

Pin Configuration



STQFN-20
(Top view)

Pin name

| Pin # | Pin name | Pin # | Pin name |
|-------|----------|-------|----------|
| 1 | NC | 11 | |
| 2 | NC | 12 | |
| 3 | NC | 13 | |
| 4 | NC | 14 | |
| 5 | NC | 15 | |
| 6 | NC | 16 | |
| 7 | VDD | 17 | AGND |
| 8 | | 18 | NC |
| 9 | | 19 | NC |
| 10 | NC | 20 | GND |

Pin Configuration

| Pin # | Pin Name | Type | Pin Description | Internal Resistor |
|-------|----------|---------------|---------------------------------------|-------------------|
| 1 | NC | -- | Keep Floating or Connect to GND | -- |
| 2 | NC | -- | Keep Floating or Connect to GND | -- |
| 3 | NC | -- | Keep Floating or Connect to GND | -- |
| 4 | NC | -- | Keep Floating or Connect to GND | -- |
| 5 | NC | -- | Keep Floating or Connect to GND | -- |
| 6 | NC | -- | Keep Floating or Connect to GND | -- |
| 7 | VDD | PWR | Supply Voltage | -- |
| 8 | | Digital Input | Digital Input without Schmitt trigger | floating |
| 9 | | Digital Input | Digital Input without Schmitt trigger | floating |
| 10 | NC | -- | Keep Floating or Connect to GND | -- |
| 11 | | Analog Output | LDO0 VOUT Analog Output | floating |
| 12 | | Analog Input | LDO0/1 VIN Analog Input | floating |
| 13 | | Analog Output | LDO1 VOUT Analog Output | floating |
| 14 | | Analog Output | LDO2 VOUT Analog Output | floating |
| 15 | | Analog Input | LDO2/3 VIN Analog Input | floating |
| 16 | | Analog Output | LDO3 VOUT Analog Output | floating |
| 17 | AGND | AGND | Ground | -- |
| 18 | NC | -- | Keep Floating or Connect to GND | -- |
| 19 | NC | -- | Keep Floating or Connect to GND | -- |
| 20 | GND | GND | Ground | -- |

Ordering Information

| Part Number | Package Type |
|----------------|---|
| SLG7RN45803V | 20-pin STQFN |
| SLG7RN45803VTR | 20-pin STQFN - Tape and Reel (3k units) |

Absolute Maximum Conditions

| Parameter | Min. | Max. | Unit |
|---------------------------------------|------------|------------|------|
| Supply Voltage on VDD relative to GND | -0.3 | 7 | V |
| DC Input Voltage | GND - 0.5V | VDD + 0.5V | V |
| Current at Input Pin | -1.0 | 1.0 | mA |
| Input leakage (Absolute Value) | -- | 1000 | nA |
| Storage Temperature Range | -65 | 150 | °C |
| Junction Temperature | -- | 150 | °C |
| ESD Protection (Human Body Model) | 2000 | -- | V |
| ESD Protection (Charged Device Model) | 1300 | -- | V |
| Moisture Sensitivity Level | 1 | | |

Electrical Characteristics

| Symbol | Parameter | Condition/Note | Min. | Typ. | Max. | Unit |
|----------------------|---|---|---------|------|---------|------|
| V _{DD} | Supply Voltage | | 2.3 | 3.3 | 5.5 | V |
| T _A | Operating Temperature | | -40 | 25 | 85 | °C |
| C _{VDD} | Capacitor Value at VDD | | -- | 0.1 | -- | µF |
| C _{IN} | Input Capacitance | | -- | 4 | -- | pF |
| I _Q | Quiescent Current | Static inputs and floating outputs | -- | 1 | -- | µA |
| V _O | Maximal Voltage Applied to any PIN in High-Impedance State | | -- | -- | VDD+0.3 | V |
| I _{VDD} | Maximum Average or DC Current Through VDD Pin (Per chip side, see Note 2) | T _J = 85°C | -- | -- | 73 | mA |
| | | T _J = 110°C | -- | -- | 35 | mA |
| I _{GND} | Maximum Average or DC Current Through GND Pin (Per chip side, see Note 2) | T _J = 85°C | -- | -- | 152 | mA |
| | | T _J = 110°C | -- | -- | 72 | mA |
| V _{IH} | HIGH-Level Input Voltage | Logic Input at VDD=2.5V | 0.7xVDD | -- | VDD+0.3 | V |
| | | Logic Input at VDD=3.3V | 0.7xVDD | -- | VDD+0.3 | V |
| | | Logic Input at VDD=5.0V | 0.7xVDD | -- | VDD+0.3 | V |
| V _{IL} | LOW-Level Input Voltage | Logic Input at VDD=2.5V | GND-0.3 | -- | 0.3xVDD | V |
| | | Logic Input at VDD=3.3V | GND-0.3 | -- | 0.3xVDD | V |
| | | Logic Input at VDD=5.0V | GND-0.3 | -- | 0.3xVDD | V |
| LDO0 | LDO0 output voltage | Vout0 voltage | -- | 2.00 | -- | V |
| | | Vout1 voltage | -- | 2.00 | -- | V |
| LDO1 | LDO1 output voltage | Vout0 voltage | -- | 0.90 | -- | V |
| | | Vout1 voltage | -- | 0.90 | -- | V |
| LDO2 | LDO2 output voltage | Vout0 voltage | -- | 0.90 | -- | V |
| | | Vout1 voltage | -- | 0.90 | -- | V |
| LDO3 | LDO3 output voltage | Vout0 voltage | -- | 0.90 | -- | V |
| | | Vout1 voltage | -- | 0.90 | -- | V |
| T _{SU} | Startup Time | From VDD rising past P _{ON} THR | -- | 1.3 | -- | ms |
| P _{ON} THR | Power On Threshold | V _{DD} Level Required to Start Up the Chip | 1.34 | 1.55 | 1.74 | V |
| P _{OFF} THR | Power Off Threshold | V _{DD} Level Required to Switch Off the Chip | 1.05 | 1.25 | 1.45 | V |

Note:

1. DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
2. The GreenPAK's power rails are divided in two sides. PINs 1, 2, 3, 4, 5 and 6 are connected to one side, PINs 8, 9, 10, 18 and 19 to another.
3. Guaranteed by Design.

I²C Specifications

| Symbol | Parameter | Condition/Note | Min. | Typ. | Max. | Unit |
|---------------------|---|---------------------------------|------|------|------|------|
| F _{SCL} | Clock Frequency, SCL | V _{DD} = (2.3...5.5) V | -- | -- | 400 | kHz |
| t _{LOW} | Clock Pulse Width Low | V _{DD} = (2.3...5.5) V | 1300 | -- | -- | ns |
| t _{HIGH} | Clock Pulse Width High | V _{DD} = (2.3...5.5) V | 600 | -- | -- | ns |
| t _i | Input Filter Spike Suppression (SCL, SDA) | V _{DD} = 2.5V ± 8% | -- | -- | 168 | ns |
| | | V _{DD} = 3.3V ± 10% | -- | -- | 157 | ns |
| | | V _{DD} = 5.0V ± 10% | -- | -- | 156 | ns |
| t _{AA} | Clock Low to Data Out Valid | V _{DD} = (2.3...5.5) V | -- | -- | 900 | ns |
| t _{BUF} | Bus Free Time between Stop and Start | V _{DD} = (2.3...5.5) V | 1300 | -- | -- | ns |
| t _{HD_STA} | Start Hold Time | V _{DD} = (2.3...5.5) V | 600 | -- | -- | ns |
| t _{SU_STA} | Start Set-up Time | V _{DD} = (2.3...5.5) V | 600 | -- | -- | ns |
| t _{HD_DAT} | Data Hold Time | V _{DD} = (2.3...5.5) V | 0 | -- | -- | ns |
| t _{SU_DAT} | Data Set-up Time | V _{DD} = (2.3...5.5) V | 100 | -- | -- | ns |
| t _R | Inputs Rise Time | V _{DD} = (2.3...5.5) V | -- | -- | 300 | ns |
| t _F | Inputs Fall Time | V _{DD} = (2.3...5.5) V | -- | -- | 300 | ns |
| t _{SU_STO} | Stop Set-up Time | V _{DD} = (2.3...5.5) V | 600 | -- | -- | ns |
| t _{DH} | Data Out Hold Time | V _{DD} = (2.3...5.5) V | 50 | -- | -- | ns |

LDO Regulator Thermal Limitations

| Symbol | Parameter | Condition/Note | Min. | Typ. | Max. | Unit |
|------------------|-------------------------------|---------------------------------|------|------|------|------|
| IC _{TL} | Thermal Limitation | 85 °C ambient, Total IC package | -- | -- | 0.6 | W |
| | | 70 °C ambient, Total IC package | -- | -- | 0.8 | W |
| | | Max Watt per LDO ¹ | -- | -- | 0.5 | W |
| Shutdown | Thermal Shutdown ² | | 115 | 125 | 135 | °C |
| | Thermal Shutdown Recovery | | 90 | 100 | 110 | °C |

Note:

1. Please note that Max Watt LDO multiplied by number of LDOs can easily exceed the Max Watt for the total IC package. In this case an external resistor should be used on LDO Vin to lower the voltage drop across the LDO Regulator.
2. Lower Thermal shutdown levels may be achieved by using the temperature sensor and comparator.

LDO HP MODE Electrical Specifications

| Symbol | Parameter | Condition/Note | Min. | Typ. | Max. | Unit |
|-------------------|--------------------------------------|--------------------------------------|------|------|-----------------|------|
| I _{OUT} | Output Current Rating | | -- | -- | 150 | mA |
| V _{IN} | Voltage Input | | 2.3 | -- | V _{DD} | V |
| V _{DO} | Voltage Dropout | | -- | 250 | 300 | mV |
| ΔV _{OUT} | Output Voltage Accuracy (see Note 1) | over PVT of V _{OUT} > 1.5 V | -3 | -- | +3 | % |
| | | over PVT of V _{OUT} ≤ 1.5 V | -60 | -- | +60 | mV |
| e _N | Noise Voltage (rms) | 10 Hz to 100 kHz | -- | 75 | -- | μV |

| | | | | | | |
|-------------------|---|---|------|------|------|-----------|
| PSRR | Power Supply Rejection Ratio (see Note 2) | 100 Hz to 100 kHz | TBD | 50 | -- | dB |
| CTRR | Crosstalk Rejection Ratio | LDO0 to LDO1 regulation perturbation, and LDO2 to LDO3 perturbation at 0 to 150 mA at 1 kHz at 1.8 V V_{OUT} | TBD | 50 | -- | dB |
| ΔV_{LINE} | Line Regulation | $V_{OUT} + 0.5 V < V_{IN} \leq 5.5 V$ | -1% | -- | +1% | %/V |
| ΔV_{LOAD} | Load Regulation | $1 mA < I_{OUT} < 150 mA$ | -- | -- | 0.3 | mV/ mA |
| ΔV_{TC} | V_{OUT} Temp Coefficient | | -- | 100 | -- | ppm/ C |
| C_{IN} | External Input Capacitor (see Note 2) | | 2 | -- | -- | μF |
| C_{OUT} | External Output Capacitor | | 2 | -- | -- | μF |
| t_{SS_0} | Soft Start Option 0 Time | V_{OUT} 5% to 95% | -20% | 10 | +20% | V/ms |
| t_{SS_1} | Soft Start Option 1 Time | V_{OUT} 5% to 95% | -20% | 20 | +20% | V/ms |
| t_{SS_2} | Soft Start Option 2 Time | V_{OUT} 5% to 95% | -30% | 1.25 | +30% | V/ms |
| t_{SS_3} | Soft Start Option 3 Time | V_{OUT} 5% to 95% | -30% | 2.50 | +30% | V/ms |
| SC | Short Circuit Protection | | TBD | TBD | TBD | mA |
| t_{WAIT} | Wait Time | Time from EN=1 to V_{OUT} start rise | -- | 500 | -- | μs |
| R_D | Output Discharge Pull-down Resistance | EN=0, Dis_EN = 1 | -- | 300 | -- | Ω |

Note:

1. Accuracy specifies all the effects of line regulation (ΔV_{LINE}), load regulation (ΔV_{LOAD}), and temperature coefficient (ΔV_{TC}),
2. X7R-type and X5R-type capacitors are recommended

LDO LP MODE Electrical Specifications

| Symbol | Parameter | Condition/Note | Min. | Typ. | Max. | Unit |
|------------------|--|------------------|------|------|------|----------|
| I_{OUT} | Output Current Rating | | -- | -- | 100 | μA |
| V_{IN} | Voltage Input | | 2.3 | -- | VDD | V |
| V_{DO} | Voltage Dropout | | -- | 500 | 750 | mV |
| ΔV_{OUT} | Output Voltage Accuracy | over PVT | -10 | -- | +10 | % |
| C_{IN} | External Input Capacitor (see Note 1) | | 2 | -- | -- | μF |
| C_{OUT} | External Output Capacitor (see Note 1) | | 2 | -- | -- | μF |
| R_D | Output Discharge Pull-down Resistance | EN=0, Dis_EN = 1 | -- | 300 | -- | Ω |

Note:

1. X7R-type and X5R-type capacitors are recommended

Chip address

| HEX | BIN | DEC |
|------|---------|-----|
| 0x28 | 0101000 | 40 |

I2C Description

1. I2C Basic Command Structure

Each command to the I2C Serial Communications block begins with a Control Byte. The bits inside this Control Byte are shown in Figure 1. After the Start bit, the first four bits are a control code, which can be set by the user in reg<1867:1864>. The Block Address is the next three bits (A10, A9, A8), which will define the most significant bits in the addressing of the data to be read ("1") or written ("0") by the command. This Control Byte will be followed by an Acknowledge bit (ACK).

With the exception of the Current Address Read command, all commands will have the Control Byte followed by the Word Address. The Word Address, in conjunction with the three address bits in the Control Byte, will define the specific data byte to be read or written in the command. Figure 1 shows this basic command structure.

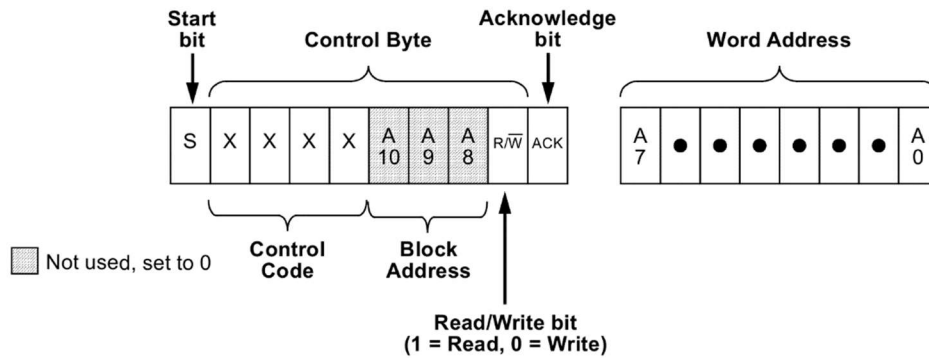


Figure1. I2C Basic Command Structure

2. I2C Serial General Timing

Shown in Figure 2 is the general timing characteristics for the I2C Serial Communications block.

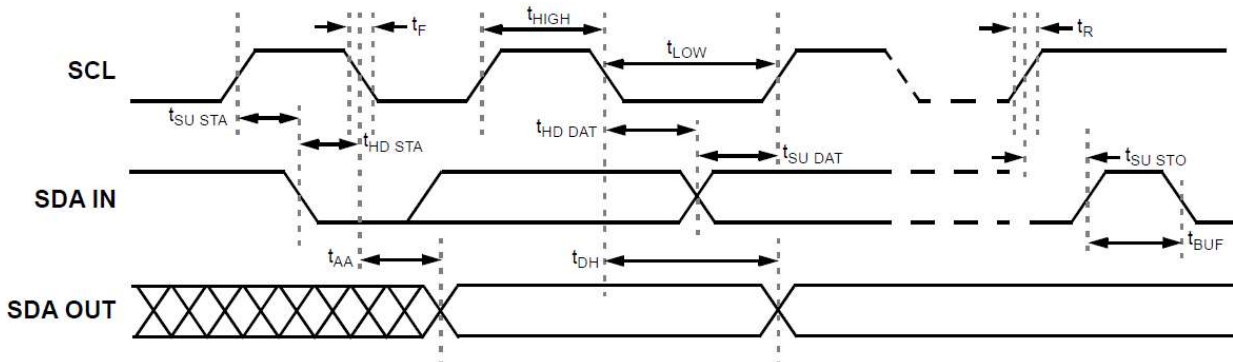


Figure2. I2C Serial General Timing

3. I2C Serial Communications: Read and Write Commands

Following the Start condition from the master, the Control Code [4 bits], the block address [3 bits] and the R/W bit (set to “0”), is placed onto the bus by the Bus Master. After the I2C Serial Communications block has provided an Acknowledge bit (ACK) the next byte transmitted by the master is the Word Address. The Block Address is the next three bits, and is the higher order addressing bits (A10, A9, A8), which when added to the Word Address will together set the internal address pointer in the SLG7RN45803 to the correct data byte to be written. After the SLG7RN45803 sends another Acknowledge bit, the Bus Master will transmit the data byte to be written into the addressed memory location. The SLG7RN45803 again provides an Acknowledge bit and then the Bus Master generates a Stop condition. The internal write cycle for the data will take place at the time that the SLG7RN45803 generates the Acknowledge bit.

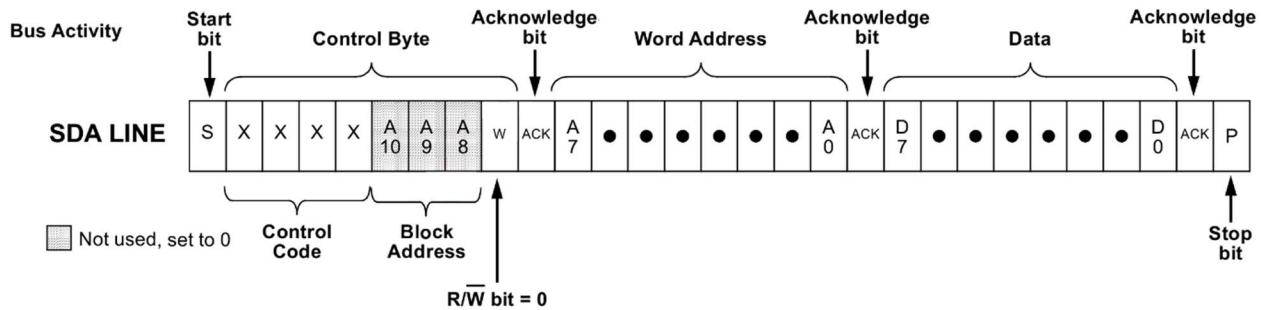


Figure3. I2C Write Command

The Random Read command starts with a Control Byte (with $\overline{R/W}$ bit set to “0”, indicating a write command) and Word Address to set the internal byte address, followed by a Start bit, and then the Control Byte for the read (exactly the same as the Byte Write command). The Start bit in the middle of the command will halt the decoding of a Write command, but will set the internal address counter in preparation for the second half of the command. After the Start bit, the Bus Master issues a second control byte with the $\overline{R/W}$ bit set to “1”, after which the SLG7RN45803 issues an Acknowledge bit, followed by the requested eight data bits.

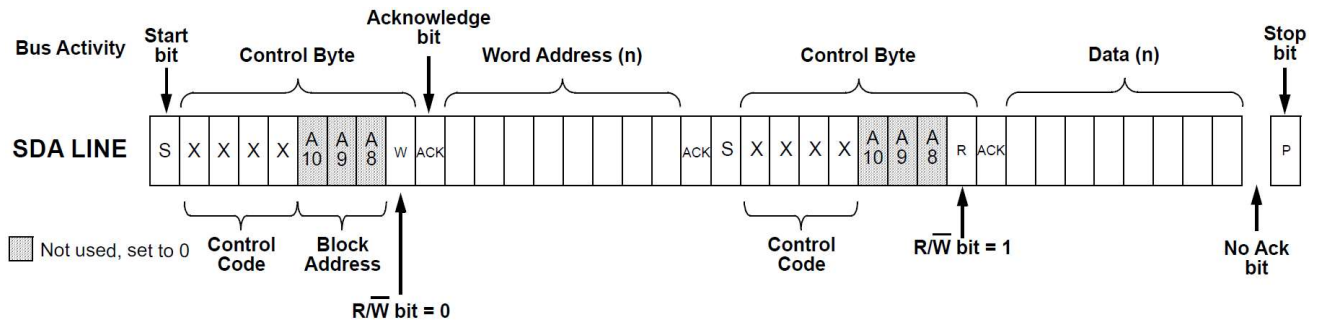
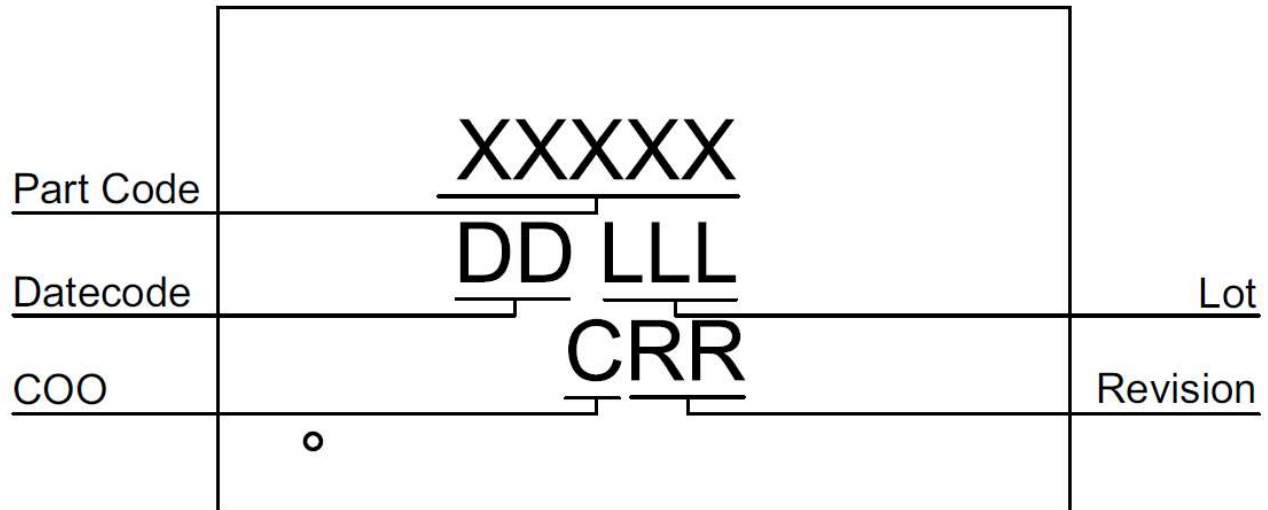


Figure4. I2C Random Read Command

4. I2C register control data

| Address Byte | Register Bit | Block | Function |
|--------------|----------------|-------------------|--|
| 0xF4 | reg<1952> | Virtual Input <0> | Enable (0) and disable (1) switch0 (VOUT0) Default is 0. |
| | reg<1953> | Virtual Input <1> | Enable (0) and disable (1) switch1 (VOUT1) Default is 0. |
| 0xC0 | reg<1543:1536> | CNT0 Control Data | PWM control data for LED1 Default is 0x65. Duty cycle is 0%. |
| 0xC1 | reg<1551:1544> | CNT1 Control Data | PWM control data for LED2 Default is 0x65. Duty cycle is 0%. |
| 0xC2 | reg<1559:1552> | CNT2 Control Data | PWM control data for LED3 Default is 0x65. Duty cycle is 0%. |

Package Top Marking



- XXXXX – Part ID Field: identifies the specific device configuration
- DD – Date Code Field: Coded date of manufacture
- LLL – Lot Code: Designates Lot #
- C – Assembly Site/COO: Specifies Assembly Site/Country of Origin
- RR – Revision Code: Device Revision

| Datasheet Revision | Programming Code Number | Lock Status | Checksum | Part Code | Revision | Date |
|--------------------|-------------------------|-------------|------------|-----------|----------|------------|
| 0.10 | 001 | U | 0x5B58769C | | | 06/01/2022 |

Lock coverage for this part is indicated by \checkmark , from one of the following options:

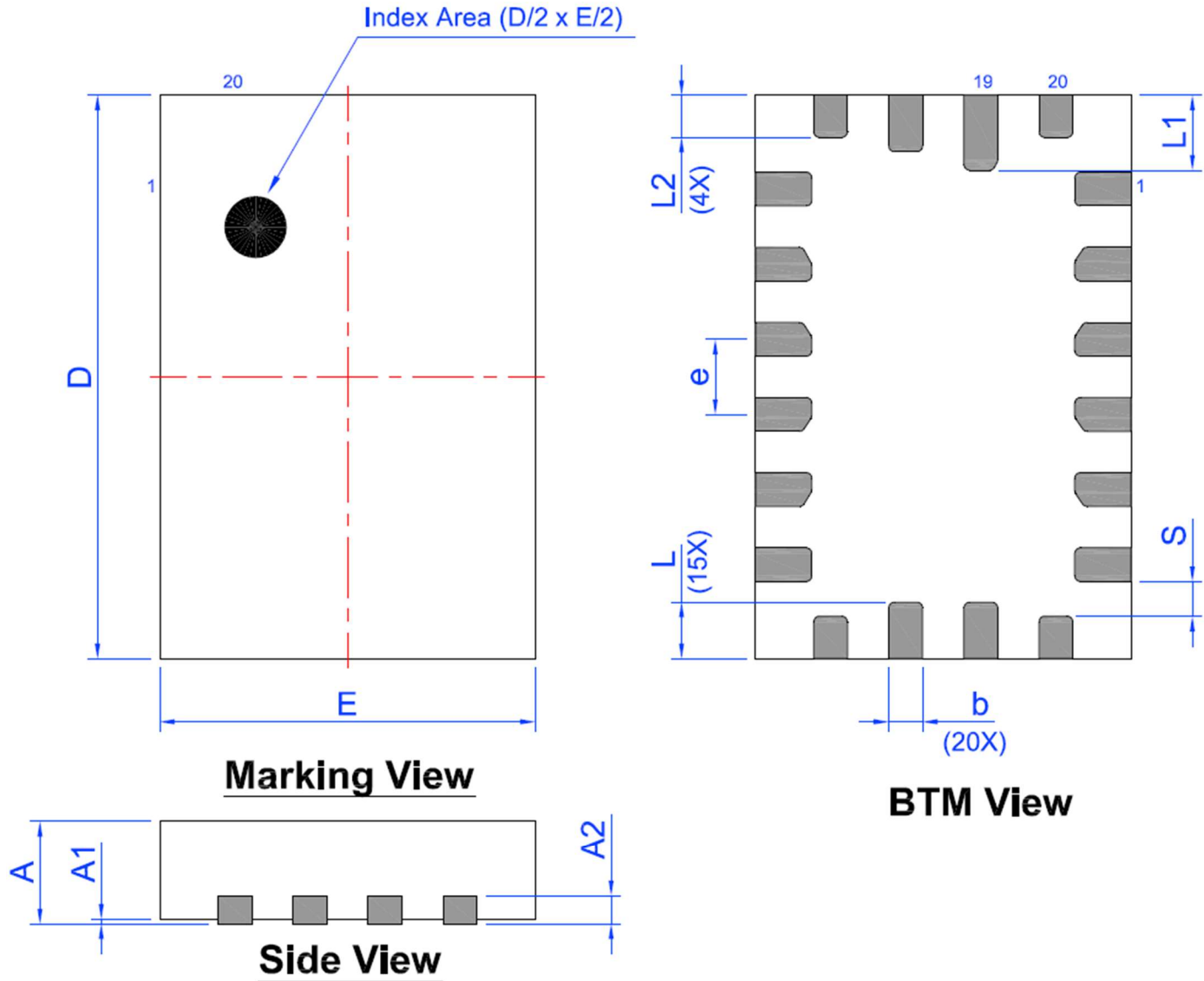
| | |
|--------------|---|
| \checkmark | Unlocked |
| | Locked for read, bits <1535:0> |
| | Locked for write, bits <1535:0> |
| | Locked for write all bits |
| | Locked for read and write bits <1535:0> |
| | Locked for read bits <1535:0> and write of all bits |

The IC security bit is locked/set for code security for production unless otherwise specified. The Programming Code Number is not changed based on the choice of locked vs. unlocked status.

Package Drawing and Dimensions

STQFN 20L 2x3mm 0.4P FCD Package

JEDEC MO-220, Variation WECE



Unit: mm

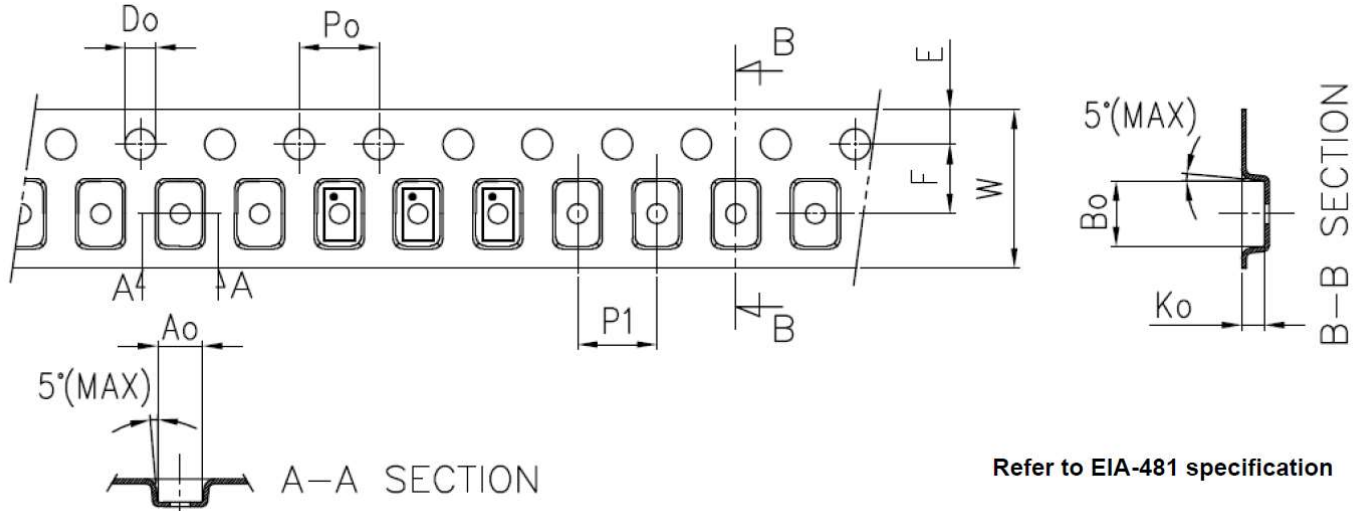
| Symbol | Min | Nom. | Max | Symbol | Min | Nom. | Max |
|--------|-----------|------|-------|--------|-------|-------|-------|
| A | 0.50 | 0.55 | 0.60 | D | 2.95 | 3.00 | 3.05 |
| A1 | 0.005 | - | 0.050 | E | 1.95 | 2.00 | 2.05 |
| A2 | 0.10 | 0.15 | 0.20 | L | 0.25 | 0.30 | 0.35 |
| b | 0.13 | 0.18 | 0.23 | L1 | 0.35 | 0.40 | 0.45 |
| e | 0.40 BSC | | | L2 | 0.175 | 0.225 | 0.275 |
| S | 0.185 TYP | | | | | | |

Tape and Reel Specification

| Package Type | # of Pins | Nominal Package Size [mm] | Max Units | | Reel & Hub Size [mm] | Leader (min) | | Trailer (min) | | Tape Width [mm] | Part Pitch [mm] |
|--------------------------------------|-----------|---------------------------|-----------|---------|----------------------|--------------|-------------|---------------|-------------|-----------------|-----------------|
| | | | per Reel | per Box | | Pockets | Length [mm] | Pockets | Length [mm] | | |
| STQFN 20L 2x3mm 0.4P FCD | 20 | 2 x 3 x 0.55 | 3000 | 3000 | 178/60 | 100 | 400 | 100 | 400 | 8 | 4 |

Carrier Tape Drawing and Dimensions

| Package Type | Pocket BTM Length | Pocket BTM Width | Pocket Depth | Index Hole Pitch | Pocket Pitch | Index Hole Diameter | Index Hole to Tape Edge | Index Hole to Pocket Center | Tape Width |
|--------------------------------|-------------------|------------------|--------------|------------------|--------------|---------------------|-------------------------|-----------------------------|------------|
| | A0 | B0 | K0 | P0 | P1 | D0 | E | F | W |
| STQFN 20L 2x3mm 0.4P FCD | 2.2 | 3.15 | 0.76 | 4 | 4 | 1.5 | 1.75 | 3.5 | 8 |



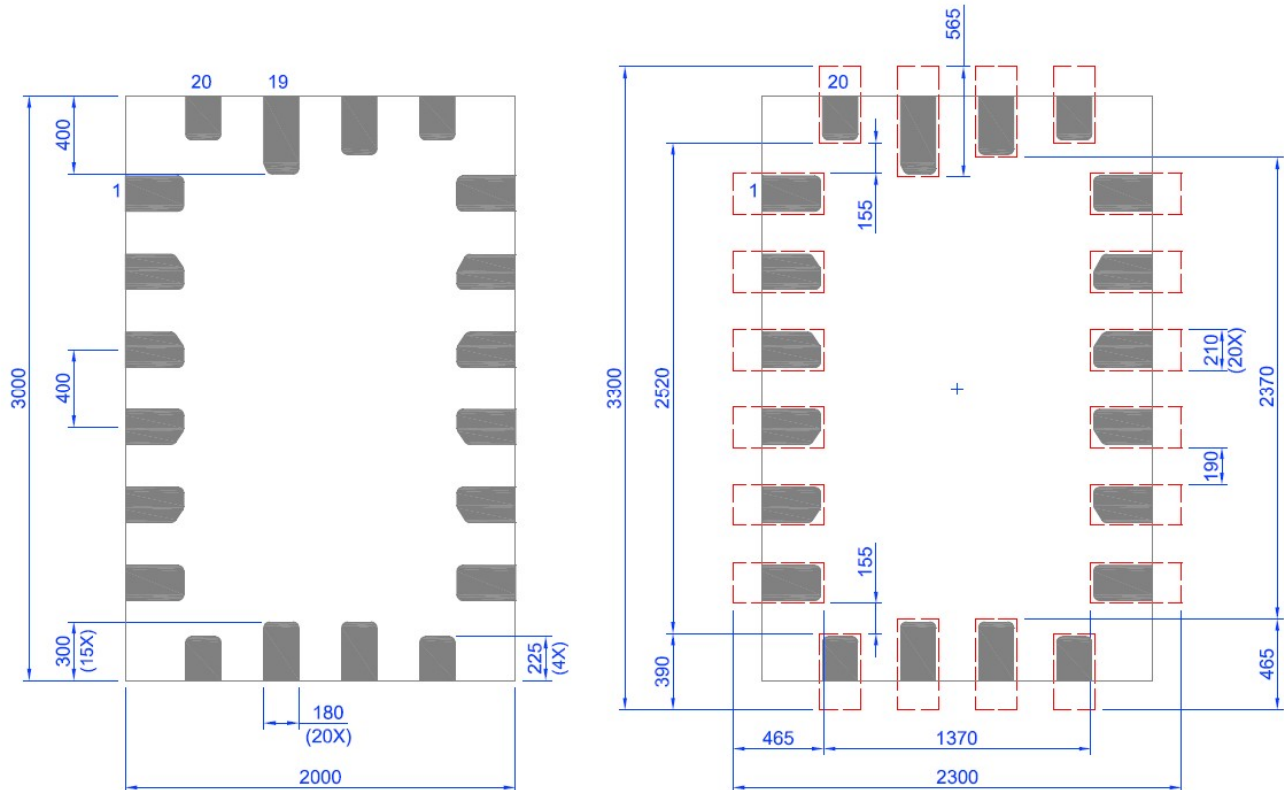
Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 3.30 mm³ (nominal). More information can be found at www.jedec.org.

Recommended Land Pattern

 Exposed Pad
(PKG face down)

 Recommended Land Pattern
(PKG face down)



Unit:um

Datasheet Revision History

| Date | Version | Change |
|------------|---------|------------------------------|
| 06/01/2022 | 0.10 | New design for SLG46580 chip |

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Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

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