NOT RECOMMENDED FOR NEW DESIGNS
RECOMMENDED REPLACEMENT PART
TW2837

TW2834

4-Channel Video QUAD/MUX Controller for Security Applications

FN7739
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The TW2834 has four high quality NTSC/PAL video decoders, dual color display controllers and dual video encoders. The TW2834 contains four built-in analog anti-aliasing filters, four 10-bit analog-to-digital converters, proprietary digital gain/clamp controller, high quality Y/C separator to reduce cross-noise and high performance free scaler. Four built-in motion and blind detectors can increase the feature of the security system. The TW2834 has a flexible video display controller including basic QUAD and MUX functions. The TW2834 also has an excellent graphic overlay function that displays character/bitmap for OSD, single box, 2D array box and mouse pointer. The built-in channel ID CODEC allows auto decoding and displaying during playback and the additional scaler on the playback supports multicropping function of the same field or frame image. The TW2834 contains two video encoders with four 10-bit digital-to-analog converters for providing 2 composite or S-video. The TW2834 also can be extended up to 8-/16-channel video controller using chip-to-chip cascade connection.

Applications

- Analog QUAD/MUX system
- 4-/8-/16-channel DVR system
- Car rear vision system
- Hair shop system
- Dental care system

Features

Four Video Decoders

- Accepts all NTSC/PAL standard formats with auto detection
- Integrated four analog anti-aliasing filters and four 10-bit CMOS ADCs
- High performance adaptive comb filters for all NTSC/PAL standards
- IF compensation filter for improvement of color demodulation
- PAL delay lines for correcting PAL phase errors
- Programmable hue, saturation, contrast, brightness and sharpness
- High performance horizontal and vertical scaler for each path including playback input
- Fast video locking system for non-realtime applications
- Four built-in motion detectors with 16x12 cells and blind detectors
- Additional digital input for playback with ITU-R BT.656 standard
- Auto cropping/strobe for playback input with Channel ID decoder
- Supports 4-channel full D1 record and playback mode

Dual Video Controllers

- Full live/strobe/switch function
- Various channel attribute control
- Supports pseudo 8-channel or dual page mode
- Horizontal/vertical mirroring for each channel
- Last image capture when video-loss detected
- Auto sequence switch with 128 queues and/or manual switch by interrupt for record path
- Channel skip in auto sequence switch for record path when video-loss detected
- Image enhancement for zoomed or still image in display path

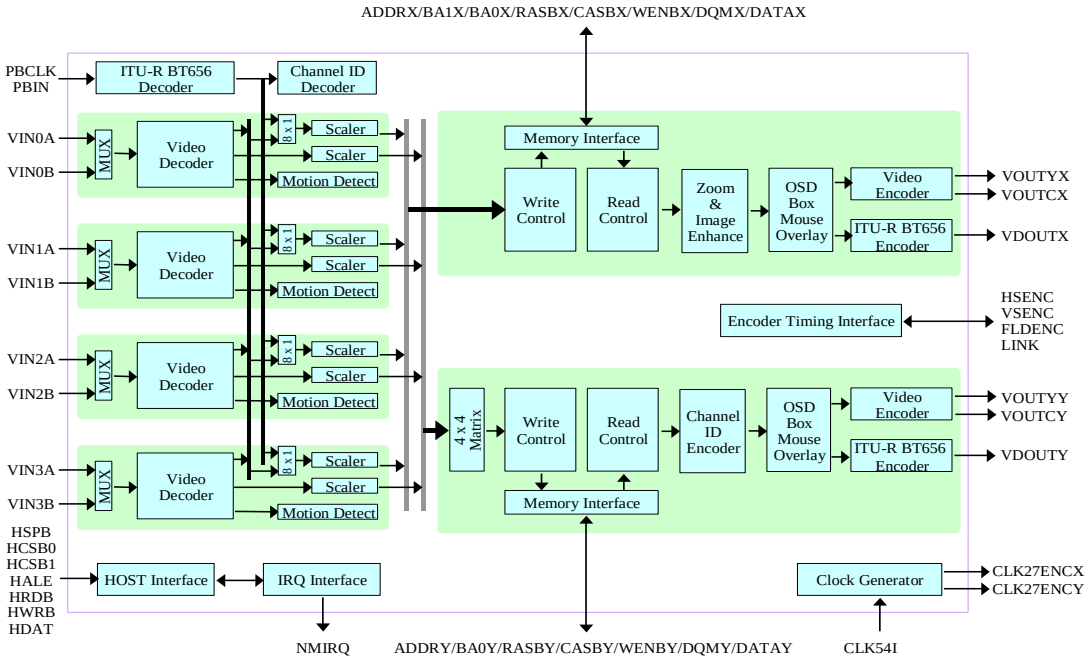
Features *(Continued)*

- High performance 2x zoom to horizontal and vertical direction for display path
- Supports save and recall function for display path
- Extendable up to 8-/16-channel video controller using cascade connection
- Quad MUX switch with 32 queues and/or manual control by interrupt for record path
- Character/bitmap overlay for OSD with 720x480 resolution in NTSC/720x588 in PAL
- Sixteen programmable single boxes overlay
- Four 2D arrayed boxes overlay with dual color for motion result or table display
- Mouse pointer overlay
- Analog/digital channel ID encoder

Dual Video Encoders

- Dual path digital outputs with ITU-R BT.656 standard
- Dual path analog outputs with all analog NTSC/PAL standards
- Programmable bandwidth of luminance and chrominance signal for each path
- Four 10-bit video CMOS DACs

Block Diagram



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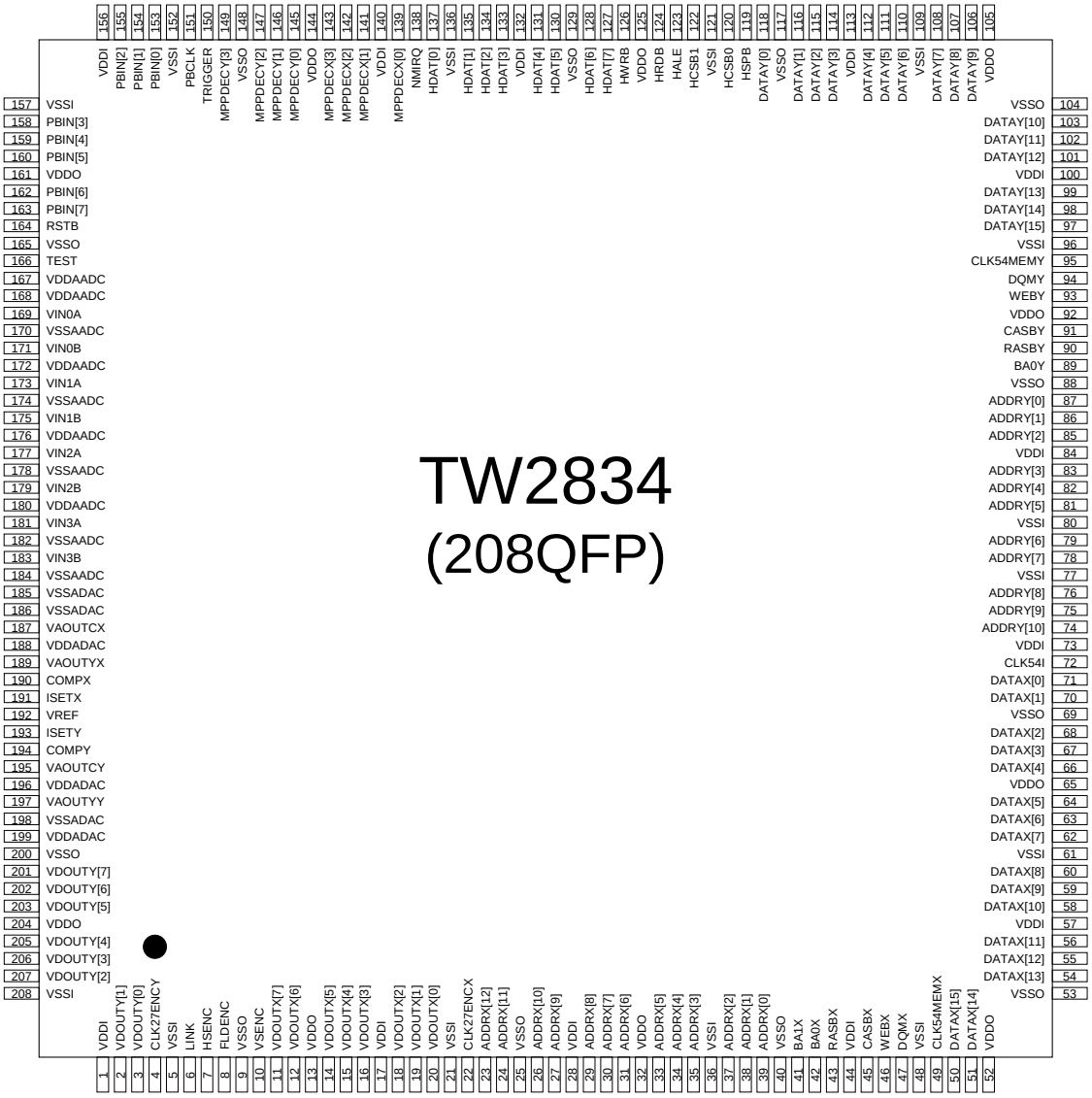
Pin Diagram


TW2834
(208QFP)
1 VDDI
2 VDOUTY[1]
3 VDOUTY[0]
4 CLK27ENCY
5 VSSI
6 LINK
7 HSENC
8 FLDENC
9 VSSO
10 VSENC
11 VDOUTX[7]
12 VDOUTX[6]
13 VDDO
14 VDOUTX[5]
15 VDOUTX[4]
16 VDOUTX[3]
17 VDDI
18 VDOUTX[2]
19 VDOUTX[1]
20 VDOUTX[0]
21 VSSI
22 CLK27ENCX
23 ADDRX[12]
24 ADDRX[11]
25 VSSO
26 ADDRX[10]
27 ADDRX[9]
28 VDDI
29 ADDRX[8]
30 ADDRX[7]
31 ADDRX[6]
32 VDDO
33 ADDRX[5]
34 ADDRX[4]
35 ADDRX[3]
36 VSSI
37 ADDRX[2]
38 ADDRX[1]
39 ADDRX[0]
40 VSSO
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42 BA0X
43 RASBX
44 VDDI
45 CASBX
46 WEBX
47 DQMX
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51 DATAX[14]
52 VDDO
53 VSSO
54 DATAX[13]
55 DATAX[12]
56 DATAX[11]
57 VDDI
58 DATAX[10]
59 DATAX[9]
60 DATAX[8]
61 VSSI
62 DATAX[7]
63 DATAX[6]
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91 CASBY
92 VDDO
93 WEBY
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108 DATAY[7]
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134 HDAT[2]
135 HDAT[1]
136 VSSI
137 HDAT[0]
138 NMIRQ
139 MPPDECX[0]
140 VDDI
141 MPPDECX[1]
142 MPPDECX[2]
143 MPPDECX[3]
144 VDDO
145 MPPDECY[0]
146 MPPDECY[1]
147 MPPDECY[2]
148 VSSO
149 MPPDECY[3]
150 TRIGGER
151 PBCLK
152 VSSI
153 PBIN[0]
154 PBIN[1]
155 PBIN[2]
156 VDDI
157 VSSI
158 PBIN[3]
159 PBIN[4]
160 PBIN[5]
161 VDDO
162 PBIN[6]
163 PBIN[7]
164 RSTB
165 VSSO
166 TEST
167 VDDAADC
168 VDDAADC
169 VIN0A
170 VSSAADC
171 VIN0B
172 VDDAADC
173 VIN1A
174 VSSAADC
175 VIN1B
176 VDDAADC
177 VIN2A
178 VSSAADC
179 VIN2B
180 VDDAADC
181 VIN3A
182 VSSAADC
183 VIN3B
184 VSSAADC
185 VSSADAC
186 VSSADAC
187 VAOUTCX
188 VDDADAC
189 VAOUTYX
190 COMPX
191 ISETX
192 VREF
193 ISETY
194 COMPY
195 VAOUTCY
196 VDDADAC
197 VAOUTYY
198 VSSADAC
199 VDDADAC
200 VSSO
201 VDOUTY[7]
202 VDOUTY[6]
203 VDOUTY[5]
204 VDDO
205 VDOUTY[4]
206 VDOUTY[3]
207 VDOUTY[2]
208 VSSI

Pin Description

Analog Interface Pins

Name	Number	Type	Description
VIN0A	169	A	Composite video input 0A. Must be connected through 2.2uF to input.
VIN0B	171	A	Composite video input 0B. Must be connected through 2.2uF to input.
VIN1A	173	A	Composite video input 1A. Must be connected through 2.2uF to input.
VIN1B	175	A	Composite video input 1B. Must be connected through 2.2uF to input.
VIN2A	177	A	Composite video input 2A. Must be connected through 2.2uF to input.
VIN2B	179	A	Composite video input 2B. Must be connected through 2.2uF to input.
VIN3A	181	A	Composite video input 3A. Must be connected through 2.2uF to input.
VIN3B	183	A	Composite video input 3B. Must be connected through 2.2uF to input.
VOUTYX	189	A	Analog video output
VOUTCX	187	A	Analog video output
VOUTYY	197	A	Analog video output
VOUTCY	195	A	Analog video output
COMPX	190	A	Compensation capacitance.
COMPY	194	A	Compensation capacitance.
ISETX	191	A	Current setting resistor for display path.
ISETY	193	A	Current setting resistor for record path.
VREF	192	A	Voltage reference. Must be connected though 0.1uF to VSSDAC.

Digital Video Interface Pins

Name	Number	Type	Description
VDOUTX [7:0]	11,12,14, 15,16,18, 19,20,	O	Digital video data output for display path or Chip-to-chip cascade connection pin.
VDOUTY [7:0]	201,202,203, 205,206,207, 2,3	I/O	Digital video data output for record path or Playback input 1
CLK27ENCX	22	O	Clock of VDOUTX. Clock phase/frequency is controlled via register.
CLK27ENCY	4	O	Clock of VDOUTY. Clock phase/frequency is controlled via register.
HSENC	7	I/O	Encoder horizontal sync or Chip-to-chip cascade connection pin.
VSENC	10	I/O	Encoder vertical sync or Chip-to-chip cascade connection pin.
FLDENC	8	I/O	Encoder field flag.
LINK	6	I/O	Chip-to-chip cascade connection pin.
PBIN[7:0]	163,162,160, 159,158,155, 154,153	I	Video data of playback input 0
PBCLK	151	I	Clock of playback input 0.
TRIGGER	150	I	Pin trigger Input for switch operation or Chip-to-chip cascade connection pin.
MPPDECY[3:0] MPPDECX[3:0]	149,147,146, 145,143,142, 141,139	I/O	Multi-purpose output or Chip-to-chip cascade connection pin.

Memory Interface Pins

Name	Number	Type	Description
DATAX[15:0]	50,51,54, 55,56,58, 59,60,62, 63,64,66, 67,68,70, 71	I/O	SDRAM data bus of display path.
ADDRX[12:0]	23,24,26, 27,29,30, 31,33,34, 35,37,38, 39	O	SDRAM address bus of display path. ADDRX[10] is AP. ADDRX[12] can be used for PBIN 2 clock. ADDRX[11] can be used for PBIN 1 clock.
BA1X	41	O	SDRAM bank1 selection of display path or Can be used for PBIN 3 clock.
BA0X	42	O	SDRAM bank0 selection of display path.
RASBX	43	O	SDRAM row address selection of display path.
CASBX	45	O	SDRAM column address selection of display path
WEBX	46	O	SDRAM write enable of display path.
DQMX	47	O	SDRAM write mask of display path.
CLK54MEMX	49	O	SDRAM clock of display path. Clock phase/frequency is controlled via register.
DATAY[15:0]	97,98,99, 101,102,103, 106,107,108, 110,111,112, 114,115,116, 118	I/O	SDRAM data bus of record path or PBIN 2 and PBIN 3 input.
ADDRY[10:0]	74,75,76, 78,79,81, 82,83,85, 86,87	O	SDRAM address bus of record path. ADDRY[10] is AP. or ADDRY[10:3] is Decoder Bypass output 1/3. ADDRY[2:0] is Decoder Bypass output 0/2 [7:5].
BA0Y	89	O	SDRAM Bank0 Selection of record path or Decoder Bypass output 0/2 [4].
RASBY	90	O	SDRAM row address selection of record path or Decoder Bypass output 0/2 [3].
CASBY	91	O	SDRAM column address selection of record path or Decoder Bypass output 0/2 [2].
WEBY	93	O	SDRAM write enable of record path or Decoder Bypass output 0/2 [1].
DQMY	94	O	SDRAM write mask of record path or Decoder Bypass output 0/2 [0]
CLK54MEMY	95	O	SDRAM clock of record path. Clock phase/frequency is controlled via register.

System Control Pins

Name	Number	Type	Description
TEST	166	I	Only for the test purpose. Must be connected to VSSO.
RSTB	164	I	System reset.
NMIRQ	138	O	Interrupt request signal.
HDAT[7:0]	127,128,130, 131,133,134, 135,137	I/O	Data bus for parallel interface. HDAT[7] is serial data for serial interface. HDAT[6:1] is slave address[6:1] for serial interface.
HWRB	126	I	Write enable for parallel interface. VSSO for serial interface.
HRDB	124	I	Read enable for parallel interface. VSSO for serial interface.
HALE	123	I	Address line enable for parallel interface. Serial clock for serial interface.
HCSB1	122	I	Chip select 1 for parallel interface. VSSO for serial interface.
HCSB0	120	I	Chip select 0 for parallel interface. Slave address[0] for serial interface.
HSPB	119	I	Select serial/parallel host interface.
CLK54I	72	I	54MHz system clock.

Power / Ground Pins

Name	Number	Type	Description
VDDO	204,161,144, 125,105,92, 65,52,32, 13	P	Digital power for output driver. 3.3V.
VSSO	200,165,148, 129,117,104, 88,69,53, 40,25,9	G	Digital ground for output driver.
VDDI	156,140,132, 113,100,84, 73,57,44, 28,17,1	P	Digital power for internal logic. 2.5V.
VSSI	208,157,152, 136,121,109, 96,80,77, 61,48,36, 21,5	G	Digital ground for internal logic.
VDDADAC	199,196,188	P	Analog power for DAC. 2.5V.
VSSADAC	198,186,185	G	Analog ground for DAC.
VDDAADC	180,176,172, 168, 167	P	Analog power for ADC. 2.5V.
VSSAADC	184,182,178, 174, 170	G	Analog ground for ADC.

Functional Description

Video Input

The TW2834 has 8 input interfaces that consist of 4 digital video inputs and 4 analog composite video inputs. 4 analog video inputs are converted to digital video stream through 10 bits ADC and luminance/chrominance processor in built-in four video decoders. 4 digital video inputs are decoded by internal ITU-R BT656 decoder and then fed to video control part and channel ID decoder. Each built-in video decoder has own motion detector and dual scaler. For playback application, each scaler in display path can receive the digital video data from internal ITU-R BT656 decoder. The structure of video input is shown in the following Fig 1.

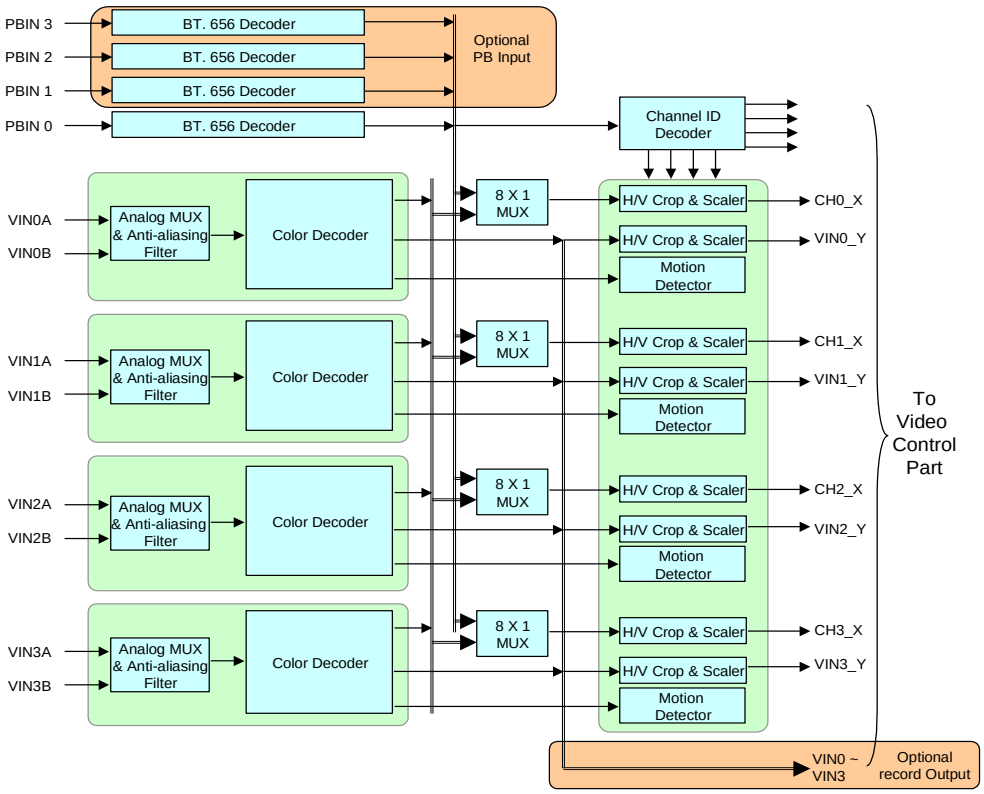


Fig 1 The structure of video input

For the special 4ch real-time record and playback application, the TW2834 supports 4 video decoder output and additional 3 digital video input interfaces via the SDRAM interface in record path.

Analog Video Input

The TW2834 supports all NTSC/PAL video standards for analog input and contains automatic standard detection circuit. Automatic standard detection can be overridden by writing the value into the IFMTMAN and IFORMAT (0x01, 0x41, 0x81, 0xC1) registers. Even if video loss is detected, the TW2834 can be forced to free-running in a particular video standard mode by IFORMAT register. The Table 1 shows the video input standards supported by TW2834.

Table 1 Video input standards

Format	Line/Fv (Hz)	Fh (KHz)	Fsc (MHz)
NTSC-M* NTSC-J	525/59.94	15.734	3.579545
NTSC-4.43*	525/59.94	15.734	4.43361875
NTSC-N	625/50	15.625	3.579545
PAL-BDGHI PAL-N*	625/50	15.625	4.43361875
PAL-M*	525/59.94	15.734	3.57561149
PAL-NC	625/50	15.625	3.58205625
PAL-60	525/59.94	15.734	4.43361875

Notes: * 7.5 IRE Setup

Anti-aliasing Filter

The TW2834 contains an anti-aliasing filter to prevent out-of-band frequency in analog video input signal. So there is no need of external components in analog input pin except ac coupling capacitor and termination resistor. The anti-aliasing filer can be bypassed via the AFIL_BYP (0xFC) register. The following Fig 2 shows the frequency response of the anti-aliasing filter.

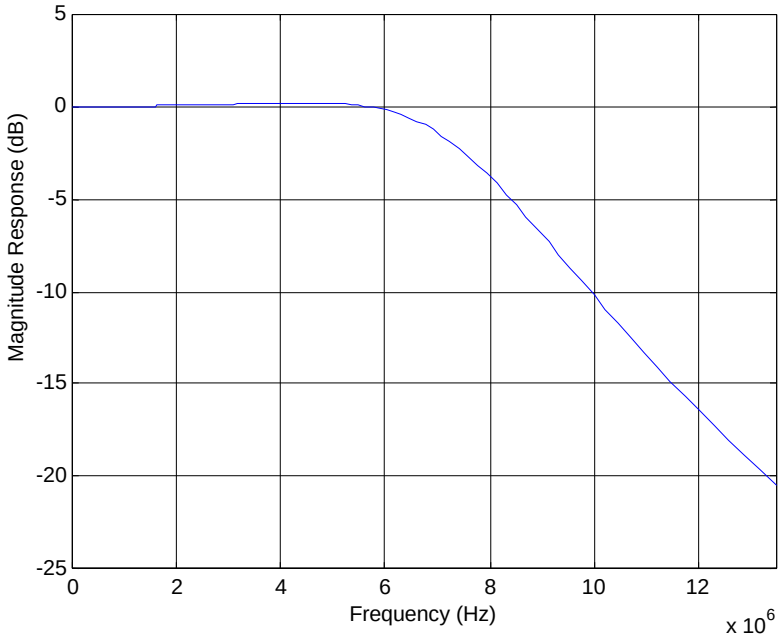


Fig 2. The frequency response of anti-aliasing filter

Analog-to-Digital Converter

The TW2834 contains four 10-bit ADC (Analog to Digital Converters) to digitize the analog video inputs. Each ADC has two analog switches that are controlled by the ANA_SW (0x22, 0x62, 0xA2, and 0xE2) register. The ADC can also be put into power-down mode by the ADC_PWDN (0x78) register.

Sync Processing

The sync processor of the TW2834 detects horizontal and vertical synchronization signals in the composite video signal. The TW2834 utilizes proprietary technology for locking to weak, noisy, or unstable signals such as those from on air signal or fast forward/backward play of VCR system.

A digital gain and clamp control circuit restores the ac coupled video signal to a fixed dc level. The clamping circuit provides line-by-line restoration of the video pedestal level to a fixed dc reference voltage. In no AGC mode, the gain control circuit adjusts only the video sync gain to achieve desired sync amplitude so that the active video is bypassed regardless of the gain control. But when AGC mode is enabled, both active video and sync are adjusted by the gain control.

The horizontal synchronization processor contains a sync separator, a PLL and the related decision logic. The horizontal sync separator detects the horizontal sync by examining low-pass filtered video input whose level is lower than a threshold. Additional logic is also used to avoid false detection on glitches. The horizontal PLL locks onto the extracted horizontal sync in all conditions to provide jitter free image output. In case of missing horizontal sync, the PLL is on free running status that matches the standard raster frequency.

The vertical sync separator detects the vertical synchronization pattern in the input video signals. The field status is determined at vertical synchronization time. When the location of the detected vertical sync is inline with a horizontal sync, it indicates a frame start or the odd field start. Otherwise, it indicates an even field.

Color Decoding

The digitized composite video data at 2X pixel clock rate first passes through decimation filter. The decimation filter is required to achieve optimum performance and prevent high frequency components from being aliased back into the video image. Fig 3 shows the frequency characteristic of the decimation filter.

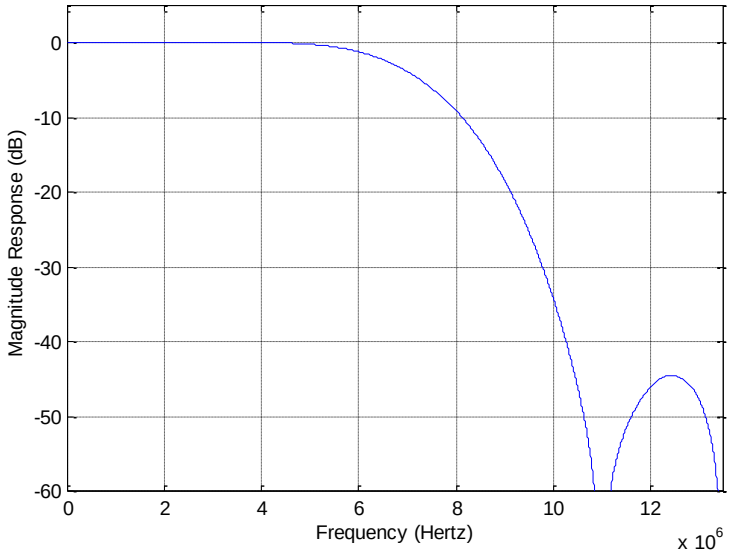


Fig 3 The frequency characteristic of the decimation Filter

The adaptive comb filter is used for high performance luminance/chrominance separation from NTSC/PAL composite video signals. The comb filter improves the luminance resolution and reduces noise such as cross-luminance and cross-color. The adaptive algorithm eliminates most of errors without introducing new artifacts or noise. To accommodate some viewing preferences, additional chrominance trap filters are also available in the luminance path.

Fig 4 and Fig 5 show the frequency response of notch filter for each system NTSC and PAL.

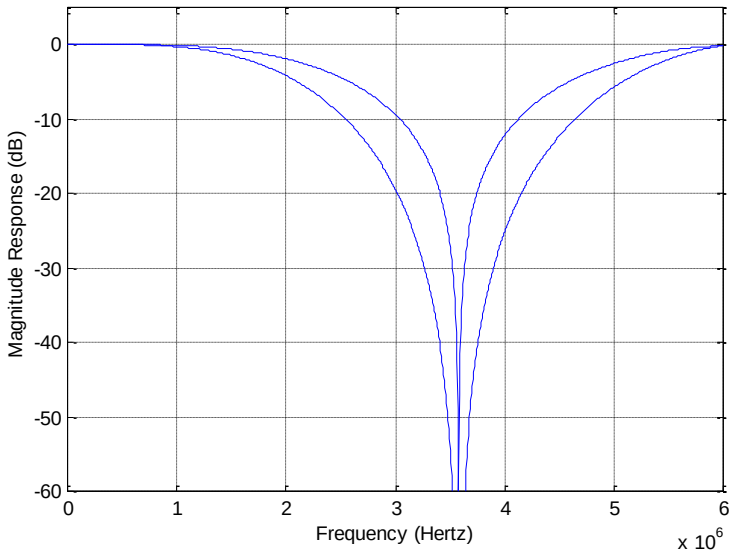


Fig 4 The frequency response of luminance notch filter for NTSC

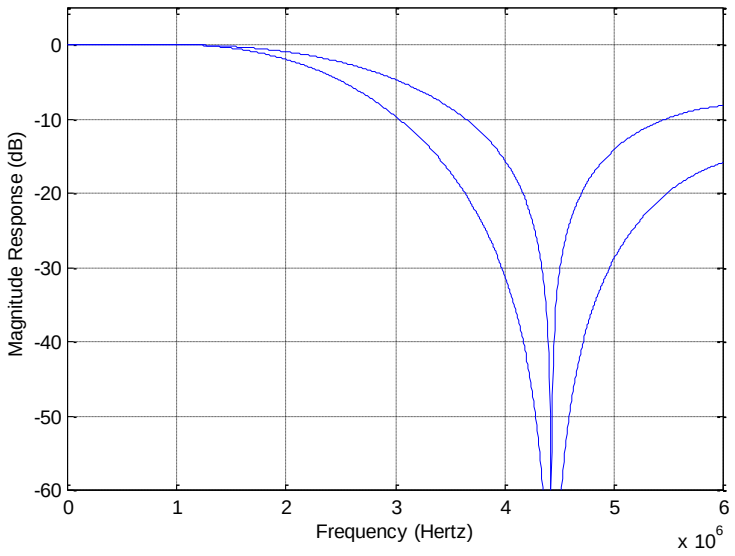


Fig 5 The frequency response of luminance notch filter for PAL

Luminance Processing

The luminance signal separated by adaptive comb or trap filter is then fed to a peaking circuit. The peaking filter enhances the high frequency components of the luminance signal via the Y_PEAK (0x14, 0x54, 0x94, 0xD4) register. The following Fig 6 shows the characteristics of the peaking filter for four different gain modes.

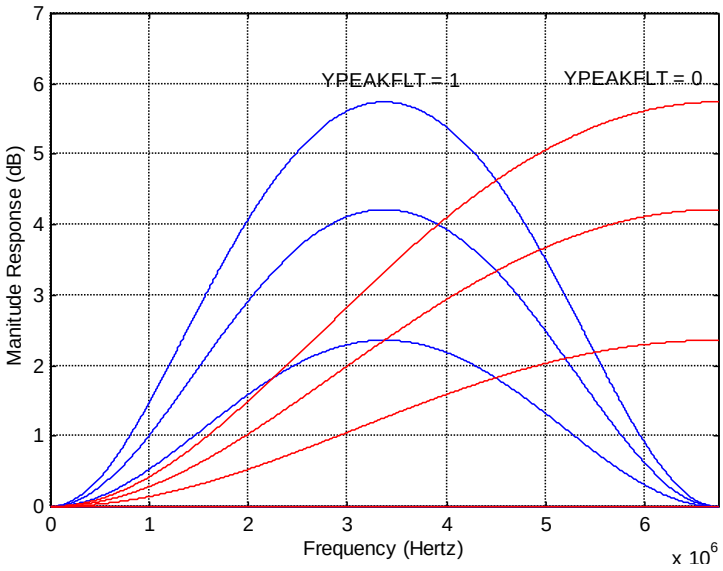


Fig 6 The frequency characteristic of luminance peaking filter

The picture contrast and brightness adjustment is provided through the CONT (0x11, 0x51, 0x91, 0xD1) and BRT (0x12, 0x52, 0x92, 0xD2) registers. The contrast adjustment range is from approximately 0 to 200 percent and the brightness adjustment is in the range of ±25 IRE. Moreover, a high frequency coring function is also embedded in TW2834 to minimize a high frequency noise. The coring level is adjustable through the Y_H_CORE (0xF8) register.

Chrominance Processing

The chrominance demodulation is done by first quadrature mixing for NTSC and PAL. The mixing frequency is equal to the sub-carrier frequency of NTSC and PAL. After the mixing, a LPF is used to remove 2X carrier signal and yield chrominance components. The characteristic of LPF can be selected for optimized transient color performance. The Fig 7 is showing the frequency response of chrominance LPF.

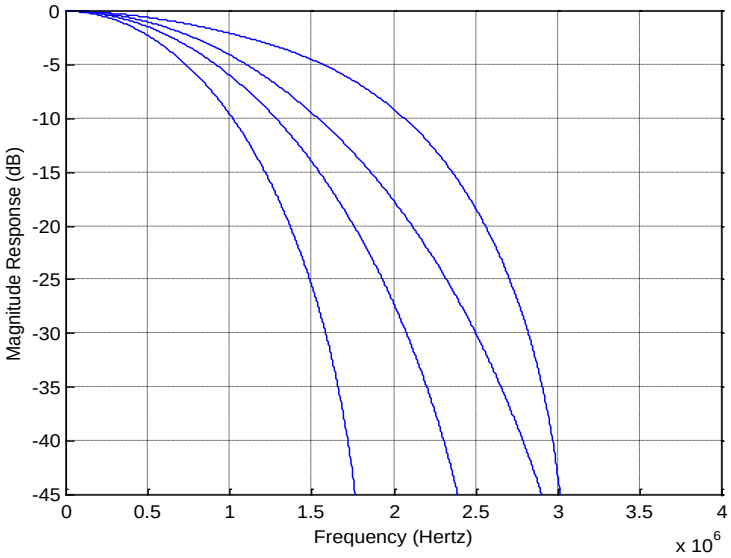


Fig 7 The frequency response of chrominance LPF

In case of a mistuned IF source, IF compensation filter makes up for any attenuation at higher frequencies or asymmetry around the color sub-carrier. The gain for the upper chrominance side band is controlled by the IFCOMP (0x13, 0x53, 0x93, 0xD3) register. The Fig 8 shows the frequency response of IF-compensation filter.

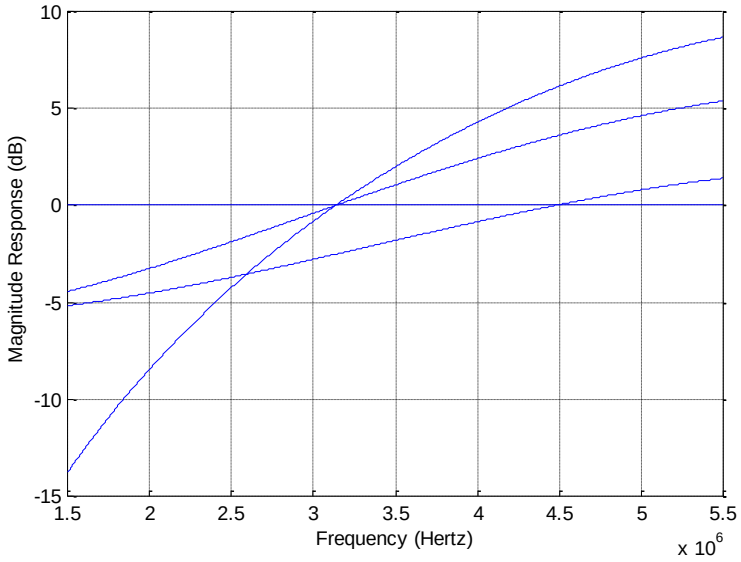


Fig 8 The frequency characteristics of IF-compensation filter

The ACC (Automatic Color gain Control) compensates for reduced chrominance amplitudes caused by high frequency suppression in video signal. The range of ACC is from –6dB to 30dB approximately. For black & white video or very weak & noisy signals, the internal color killer circuit will turn off the color. The color killing function can also be always enabled or disabled by programming CKIL (0x14, 0x54, 0x94, 0xD4) register.

The color saturation can be adjusted by changing SAT (0x10, 0x50, 0x90, 0xD0) register. The Cb and Cr gain can be also adjusted independently by programming UGAIN (0x3C) and VGAIN (0x3D) registers. Likewise, the Cb and Cr offset can be programmed through the U_OFF (0x3E) and V_OFF (0x3F) registers. Hue control is achieved with phase shift of the digitally controlled oscillator. The phase shift can be programmed through the HUE (0x0F, 0x4F, 0x8F, 0xCF) register.

Digital Video Input

The TW2834 supports digital video input with 8bit ITU-R BT.656 standard for playback. This digital input is decoded in built-in ITU-R BT 656 decoder and fed to the scaler block to display scaled video data. The TW2834 supports error correction code for decoding ITU-R BT.656. The decoded video data are also transferred to channel ID decoder part for auto cropping and strobe function.

Digital Video Input Format

The timing of digital video input is illustrated in Fig 9.

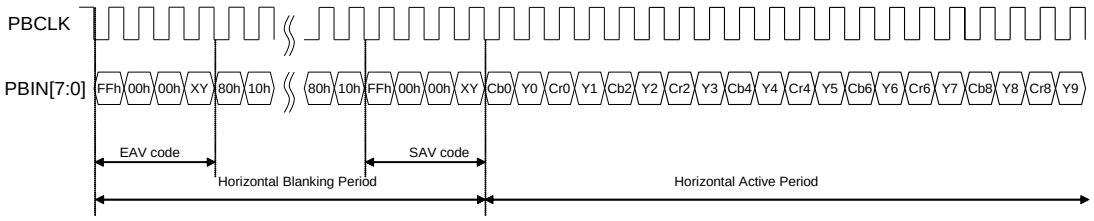


Fig 9 Timing diagram of ITU-R BT.656 format for digital video input

The SAV and EAV sequences are shown in Table 2.

Table 2 ITU-R BT.656 SAV and EAV code sequence

Condition			656 FVH Value			SAV/EAV Code Sequence			
Field	Vertical	Horizontal	F	V	H	First	Second	Third	Fourth
EVEN	Blank	EAV	1	1	1	0xFF	0x00	0x00	0xF1
		SAV			0				0xEC
EVEN	Active	EAV	1	0	1				0xDA
		SAV			0				0xC7
ODD	Blank	EAV	0	1	1				0xB6
		SAV			0				0xAB
ODD	Active	EAV	0	0	1				0x9D
		SAV			0				0x80

To display the playback input in display path, PB_CH_EN (0x38) register should be set to “1” and PB_PATH_CH (0x39) register should set properly to select playback input for each input path.

Channel ID Decoder

The TW2834 provides channel ID CODEC for auto cropping and strobe function. The channel ID includes the channel number, analog switch, event, region enable and field/frame mode information. The TW2834 supports two kinds of channel ID such as User channel ID and Auto channel ID. The User channel ID is used for customized information like system information and date. The auto channel ID is employed for automatic identification of picture configuration. The TW2834 also supports both analog and digital type channel ID during VBI period.

The TW2834 can receive 4 playback inputs, but channel ID detection can be supported only in PBIN0 input from PBIN pin. The TW2834 can detect the channel ID automatically, which can be enabled via AUTO_VBI_DET (1xC9) register. For automatic channel ID detection mode, the playback input should be included with run-in clock. For manual channel ID detection mode, the playback input can be included with or without run-in clock via VBI_RIC_ON (1xC9) register. In manual detection mode, the TW2834 has several related register such as VBI_PIXEL_H_OS (1xCA) to define horizontal start offset, VBI_FLD_OS (1xCB) to define line offset between odd and even field, VBI_PIXEL_HW to define pulse width for 1 bit data, VBI_LINE_SIZE (1xCC) to define channel ID line size and VBI_LINE_OS (1xCC) to define line offset for channel ID. The VBI_MID_VAL (1xCD) register is used to define the threshold level between high and low. Even in automatic channel ID detection mode, the line size and bit width can be discriminated by reading of VBI_LINE_SIZE, VBI_PIXEL_HW (1xCB) register. The following Fig 10 shows the relationship between channel ID and register setting.

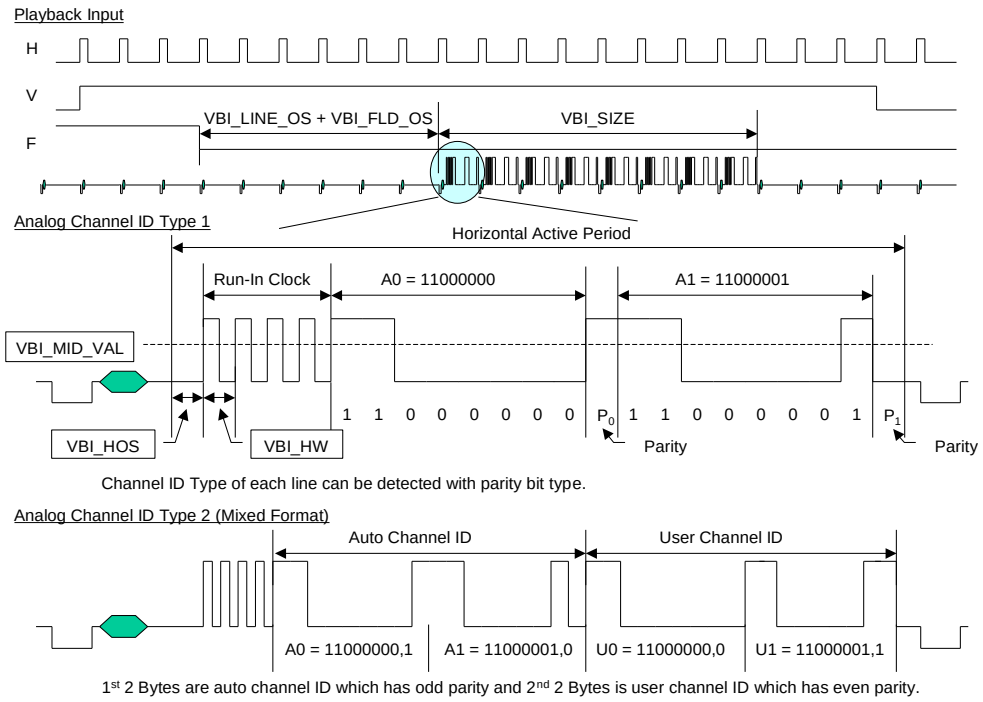


Fig 10 The related register for manual channel ID detection

The channel ID type can be discriminated by reading the CHID_TYPE (1xCF) register, which indicates the Auto channel ID type with “1” value and User channel ID type with “0” value. The CHID_VALID (1xCE) register indicates whether the detected channel ID type is valid or not. When both Auto and User channel ID are mixed in the same line, the VBI_MIX_ON (1xC9) register should be set into “1”. The channel ID data can be read through the AUTO_CHID (1xE0 ~ 1xE3) register for Auto channel ID and the VIS_MAN0~7 (1xD0 ~ 1xDF) register for User channel ID. Originally the VIS_MAN0~7 registers are used to insert the user information in the channel ID encoding, but in read mode it indicates the decoded User channel ID information when VBI_RD_CTL (1xC9) = “1”. This channel ID information is updated as soon as it is detected and decoded during VBI period. For a robust error detection mode, the Auto channel ID can be repeated two times by setting “1” into the VBI_EC_ON (1xC9) register.

The TW2834 also supports the digital channel ID decoding via the VBI_CODE_EN (1xC9) register. The digital channel ID has priority over analog channel ID. The digital channel ID can also be detected automatically in automatic channel ID detection. The digital channel ID also supports the robust error detection for the Auto channel ID type via VBI_EC_ON (1xC9) register.

Additionally to detect properly the channel ID against noise such as VCR source, the channel ID LPF can be enabled via the VBI_FLT_EN (1xC9) register.

The detailed auto strobe and cropping function will be described at “Cropping Function” section (page 26) and “Playback Path Control” section (page 59).

Normally the channel ID is located in VBI period and auto strobe and cropping is executed after channel ID decoding. But for some case, the channel ID can be placed in vertical active period instead of VBI period. For this mode, the TW2834 also supports the channel ID decoding function within vertical active period via the VAV_CHK (1xCB) register and manual cropping function via the MAN_PB_CROP (0x38) register with proper VDELAY value.

Cropping and Scaling Function

The TW2834 provides two methods to reduce the amount of video pixel data, scaling and cropping. The scaling function provides video image at lower resolution while the cropping function supplies only a portion of the video image. The TW2834 also supports an auto cropping function for playback input with channel ID decoding. The TW2834 has a free scaler for a variable image size in display path, but has a limitation of image size in record path like as Full / QUAD / CIF size and has a limitation of image cropping in record path as recommended value on page 115.

Cropping Function

The cropping function allows only subsection of a video image to be output. The active video region is determined by the HDELAY, HACTIVE (0x04 ~ 0x07, 0x44 ~ 0x47, 0x84 ~ 0x87, 0xC4 ~ 0xC7), VDELAY and VACTIVE (0x09 ~ 0x0D, 0x49 ~ 0x4D, 0x89 ~ 0x8D, 0xC9 ~ 0xCD) register. The first active line is defined by the VDELAY register and the first active pixel is defined by the HDELAY register. The VACTIVE register can be programmed to define the number of active lines in a video field, and the HACTIVE register can be programmed to define the number of active pixels in a video line. This function is used to implement for panning and tilt.

The horizontal delay register HDELAY determines the number of pixel delays between the horizontal reference and the leading edge of the active region. The horizontal active register HACTIVE determines the number of active pixels to be processed. Note that these values are referenced to the pixel number before scaling. Therefore, even if the scaling ratio is changed, the active video region used for scaling remains unchanged as set by the HDEALY and HACTIVE register. In order for the cropping to work properly, the following equation should be satisfied.

HDELAY + HACTIVE < Total number of pixels per line

Where the total number of pixels per line is 858 for NTSC and 864 for PAL

To process full size region, the HDELAY should be set to 32 and HACTIVE set to 720 for both NTSC and PAL system.

The vertical delay register (VDELAY) determines the number of line delays from the vertical reference to the start of the active video lines. The vertical active register (VACTIVE) determines the number of lines to be processed. These values are referenced to the incoming scan lines before the vertical scaling. In order for the vertical cropping to work properly, the following equation should be satisfied.

VDELAY + VACTIVE < Total number of lines per field

Where the total number of lines per field is 262 for NTSC and 312 for PAL

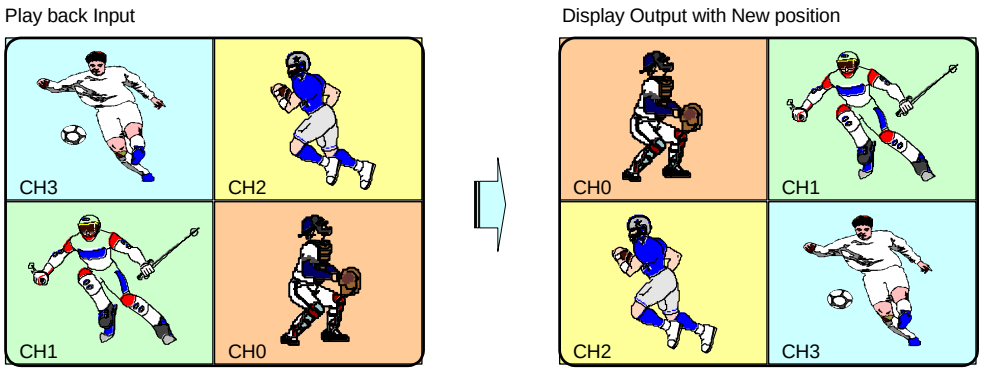
To process full size region, the VDELAY should be set to 6 and VACTIVE set to 240 for NTSC and the VDELAY should be also set to 5 and VACTIVE set to 288 for PAL.

The TW2834 supports an auto cropping function with channel ID decoding for playback input. Each channel with the multiplexed playback input can be mapped into the desired position with the auto cropping function.

If the PB_AUTO_EN (1x16) = “0”, it is manual cropping mode so that user can control cropping with VDELAY and HDELAY register. If PB_AUTO_EN = “1”, it is auto cropping mode and the TW2834 has several related registers for this mode such as PB_CH_NUM (1x16, 1x1E, 1x26, 1x2E), PB_CROP_MD, and PB_ACT_MD (0x38) registers.

To operate auto cropping function, the playback input should be selected for each path with PB_CH_EN (0x38) register and the PB_AUTO_EN register should also be set into “1”. In this case, the desired channel can be chosen by PB_CH_NUM register and it will be cropped automatically to horizontal and vertical direction in playback input.

The PB_CROP_MD defines the record mode of the playback input such as normal record mode or DVR record mode (refer to Record Path Control section, page 49). The PB_ACT_MD defines an active pixel size of horizontal direction such as 720 / 704 / 640 pixels. The following Fig 11 shows the effect of auto cropping function.



CH0 : PB_CH_NUM0 = 0, (cropping H/V) CH1 : PB_CH_NUM1 = 1, (cropping V)
CH2 : PB_CH_NUM2 = 2, (cropping H) CH3 : PB_CH_NUM3 = 3, (No cropping)

Fig 11 The effect of auto cropping function

Scaling Function

The TW2834 includes a high quality free horizontal and vertical down scaler for display path. But the TW2834 cannot use a free scaler function in record path because channel size definition for record path has a limitation such as Full / QUAD / CIF. (Please refer to “Record Path Control” section, page 49)

The video images can be downscaled in both horizontal and vertical direction to an arbitrary size. The luminance horizontal scaler includes an anti-aliasing filter to reduce image artifacts in the resized image and a 32 poly-phase filter to accurately interpolate the value of a pixel. This results in more aesthetically pleasing video as well as higher compression ratio in bandwidth-limited application. Fig 12 shows the frequency response of anti-aliasing filter for horizontal scaling.

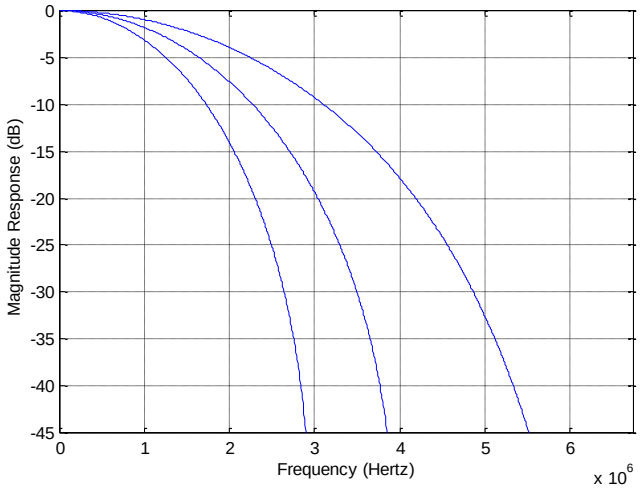


Fig 12 The frequency response of anti-aliasing filter for horizontal scaling

Similarly, the vertical scaler also contains an anti-aliasing filter and 16 poly-phase filters for down scaling. The filter characteristics are shown in Fig 13.

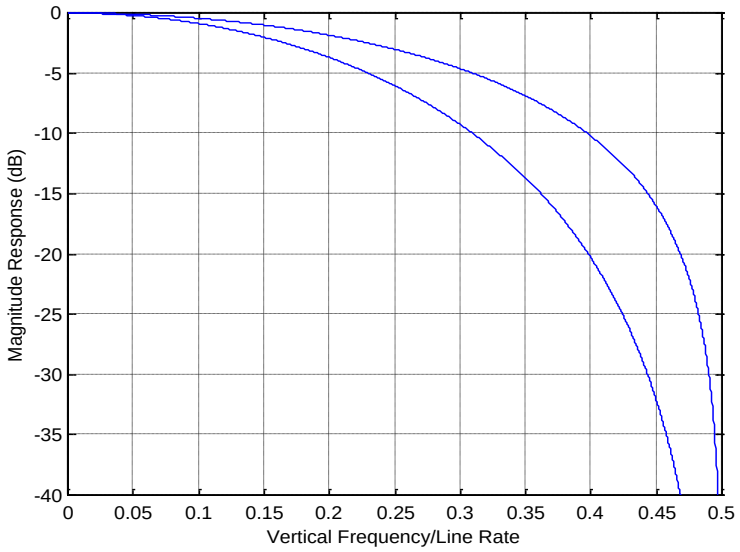


Fig 13 The characteristics of anti-aliasing filter for vertical scaling

Down scaling is achieved by programming the horizontal scaling register HSCALE (0x1C ~ 0x1F, 0x5C ~ 0x5F, 0x9C ~ 0x9F, 0xDC ~ 0xDF) and vertical scaling register VSCALE (0x18 ~ 0x1B, 0x58 ~ 0x5B, 0x98 ~ 0x9B, 0xD8 ~ 0xDB). When no scaled video image, the TW2834 will output the number of pixels per line as specified by the HACTIVE (0x04 ~ 0x07, 0x44 ~ 0x47, 0x84 ~ 0x87, 0xC4 ~ 0xC7) register. If the number of output pixels required is smaller than the number specified by the HACTIVE register, the 16bit HSCALE register is used to reduce the output pixels to the desired number.

The following equation is used to determine the horizontal scaling ratio to be written into the 16bit HSCALE register.

$$HSCALE = [N_{pixel\_desired} / HACTIVE] * (2^{16} - 1)$$

Where $N_{pixel\_desired}$ is the desired number of active pixels per line

For example, to scale picture from full size (HACTIVE = 720) to CIF (360 pixels), the HSCALE value can be found as:

$$HSCALE = [360/720] * (2^{16} - 1) = 0x7FFF$$

The following equation is used to determine the vertical scaling ratio to be written into the 16bit VSCALE register.

$$VSCALE = [N_{line\_desired} / VACTIVE] * (2^{16} - 1)$$

Where $N_{line\_desired}$ is the desired number of active lines per field

For example, to scale picture from full size (VACTIVE = 240 lines for NTSC and 288 lines for PAL) to CIF (120 lines for NTSC and 144 lines for PAL), the VSCALE value can be found as:

$$VSCALE = [120 / 240] * (2^{16} - 1) = 0x7FFF \text{ for NTSC}$$

$$VSCALE = [144 / 288] * (2^{16} - 1) = 0x7FFF \text{ for PAL}$$

The scaling ratios of popular case are listed in Table 3.

Table 3 HSCALE and VSCALE value for popular video formats

Scaling Ratio	Format	Output Resolution	HSCALE	VSCALE
1	NTSC PAL	720x480 720x576	0xFFFF 0xFFFF	0xFFFF 0xFFFF
1/2 (CIF)	NTSC PAL	360x240 360x288	0x7FFF 0x7FFF	0x7FFF 0x7FFF
1/4 (QCIF)	NTSC PAL	180x120 180x144	0x3FFF 0x3FFF	0x3FFF 0x3FFF

The effect of scaling and cropping is shown in Fig 14.

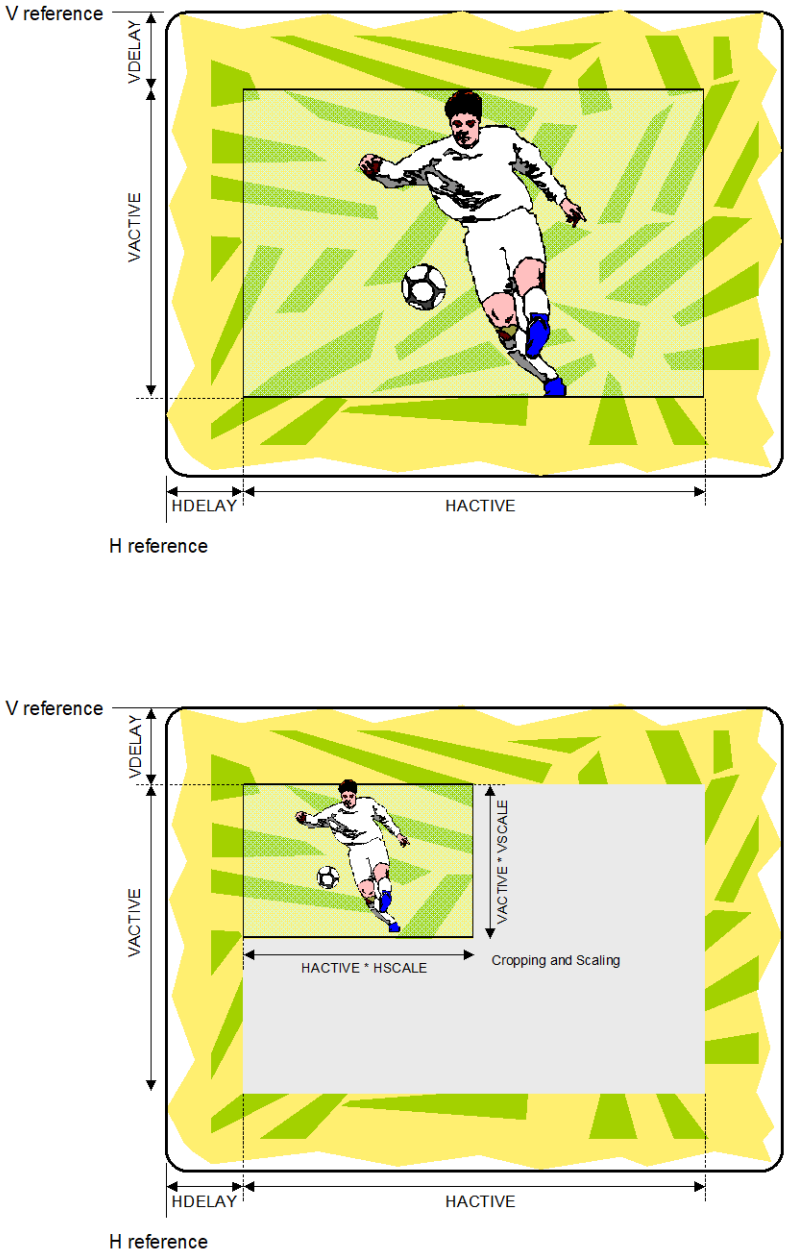


Fig 14 The effect of cropping and scaling

Motion Detection

The TW2834 supports motion detector individually for 4 analog video inputs. The built-in motion detection algorithm uses the difference of luminance level between current and reference field. The TW2834 also supports blind input detection for 4 analog video inputs.

To detect motion properly according to situation, the TW2834 provides several sensitivity and velocity control parameters for each motion detector. The TW2834 supports manual strobe function to update motion detection so that it is more appropriate for non-realtime application or user-defined motion sensitivity control.

When motion or blind is detected in any video inputs, the TW2834 provides the interrupt request to host via NMIRQ pin. The host processor (i.e. Micom or CPU) can take the information of motion or blind by accessing the DET_MOTION (1x7B), DET_BLIND (1x7C), MD_MASK (2x86 ~ 2x9D, 2xA6 ~ 2xBD, 2xC6 ~ 2xDD, 2xE6 ~ 2xFD) register. This status information is updated in the vertical blank period of each input.

The TW2834 also provides the motion detection result through MPPDEC pin with the control of MPPSET (1x50) register. The TW2834 supports an overlay function to display the motion detection result in the picture with 2D arrayed box.

The MD_PATH (2x9E) register is used to determine which path is selected to store the motion detection information between display and record path. In case that 64M/128M/256M/512M SDRAM is used for display path and 16M SDRAM for record path, the MD_PATH should be set into “0” to select the SDRAM of display path. If 16M SDRAM is used for both display and record path, the MD_PATH should be set into “1” to use the SDRAM of record path for motion information because of OSD page expansion of display path. When 16M SDRAM is used for display path and no SDRAM is for record path to support the special 4ch real-time record and playback application, the MD_PATH should be set into “0” so that no OSD page expansion for display path can be achieved.

Mask and Detection Region Selection

The motion detection algorithm utilizes the full screen video data and detects individual motion of 16x12 cells. This full screen for motion detection consists of 704 pixels and 240 lines for NTSC and 288 lines for PAL. Starting pixel in horizontal direction can be shifted from 0 to 15 pixels using the MD_ALIGN (2x81, 2xA1, 2xC1, 2xE1) register.

Each cell can be masked via the MD_MASK (2x86 ~ 2x9D, 2xA6 ~ 2xBD, 2xC6 ~ 2xDD, 2xE6 ~ 2xFD) register as illustrated in Fig 15. If the mask bit in specific cell is programmed to high, the related cell is ignored for motion detection.

The MD_MASK register has different function for reading and writing mode. For writing mode, setting “1” to MD_MASK register inhibits the specific cell from detecting motion. For reading mode, the state of MD_MASK register has two kinds of information depending on MASK_MODE (2x82, 2xA2, 2xC2, 2xE2) register. For MASK_MODE = “1”, the state of MD_MASK register means masking information of cell. For MASK_MODE = “0”, the state of MD_MASK register means the result of motion detection that “1” indicates detecting motion and “0” denotes no motion detection in the cell.

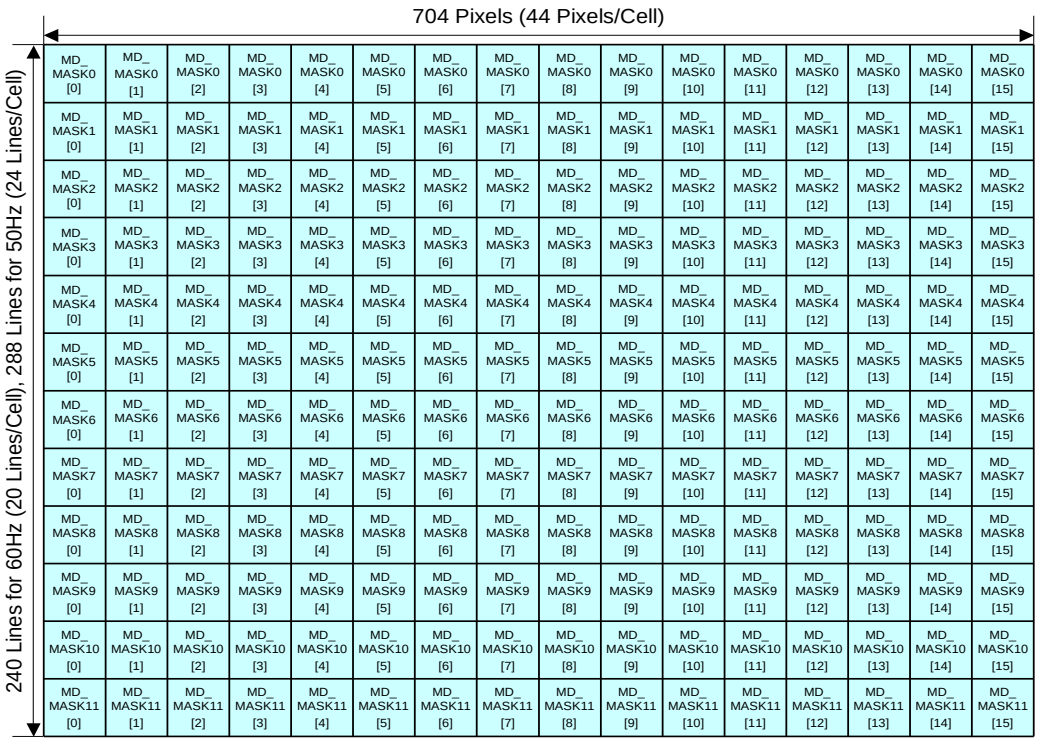


Fig 15 Motion mask and detection cell

Sensitivity Control

The motion detector has 4 sensitivity parameters to control threshold of motion detection such as level sensitivity via the MD_LVSENS (2x82, 2xA2, 2xC2, 2xE2) register, spatial sensitivity via the MD_SPSENS (2x85, 2xA5, 2xC5, 2xE5) and MD_CELSENS (2x82, 2xA2, 2xC2, 2xE2) register, and temporal sensitivity parameter via the MD_TMPSENS (2x85, 2xA5, 2xC5, 2xE5) register.

Level Sensitivity

In built-in motion detection algorithm, motion is detected when luminance level difference between current and reference field is greater than MD_LVSENS value. Motion detector is more sensitive for the smaller MD_LVSENS value and less sensitive for the larger. When the MD_LVSENS is too small, the motion detector may be weak in noise.

Spatial Sensitivity

The TW2834 uses 192 (16x12) detection cells in full screen for motion detection. Each detection cell is composed of 44 pixels and 20 lines for NTSC and 24 lines for PAL. Motion detection from only luminance level difference between two fields is very weak in spatial random noise. To remove the fake motion detection from the random noise, a spatial filter is used. The MD_SPSENS defines the number of detected cell to decide motion detection in full size image. The large MD_SPSENS value increases the immunity of spatial random noise.

Each detection cell has 4 sub-cells also. Actually motion detection of each cell comes from comparison of sub-cells in it. The MD_CELSENS defines the number of detected sub-cell to decide motion detection in cell. Likewise, the large MD_CELSENS value increases the immunity of spatial random noise in small area.

Temporal Sensitivity

Similarly, temporal filter is used to remove the fake motion detection from the temporal random noise. The MD_TMPSENS regulates the number of taps in the temporal filter to control the temporal sensitivity so that the large MD_TMPSENS value increases the immunity of temporal random noise.

Velocity Control

Motion has various velocities. That is, in a fast motion an object appears and disappears rapidly between the adjacent fields while in a slow motion it is to the contrary. As the built-in motion detection algorithm uses the only luminance level difference between two adjacent fields, a slow motion is inferior in detection rate to a fast motion. To compensate this weakness, MD_SPEED (2x83, 2xA3, 2xC3, 2xE3) parameter is used which is controllable up to 64 fields. MD_SPEED parameter adjusts the field interval in which the luminance level is compared. Thus, for detection of a fast motion a small value is needed and for a slow motion a large value is required. The parameter MD_SPEED value should be greater than MD_TMPSENS value.

Additionally, the TW2834 has 2 more parameters to control the selection of reference field. The MD_FLD (2x81, 2xA1, 2xC1, 2xE1) register is a field selection parameter such as odd, even, any field or frame.

The MD_REFFLD (2x80, 2xA0, 2xC0, 2xE0) register is provided to control the updating period of reference field. For MD_REFFLD = “0”, the interval from current field to reference field is always same as the MD_SPEED. It means that the reference filed is always updated every field. The Fig 16 shows the relationship between current and reference field for motion detection when MD_REFFLD is “0”.

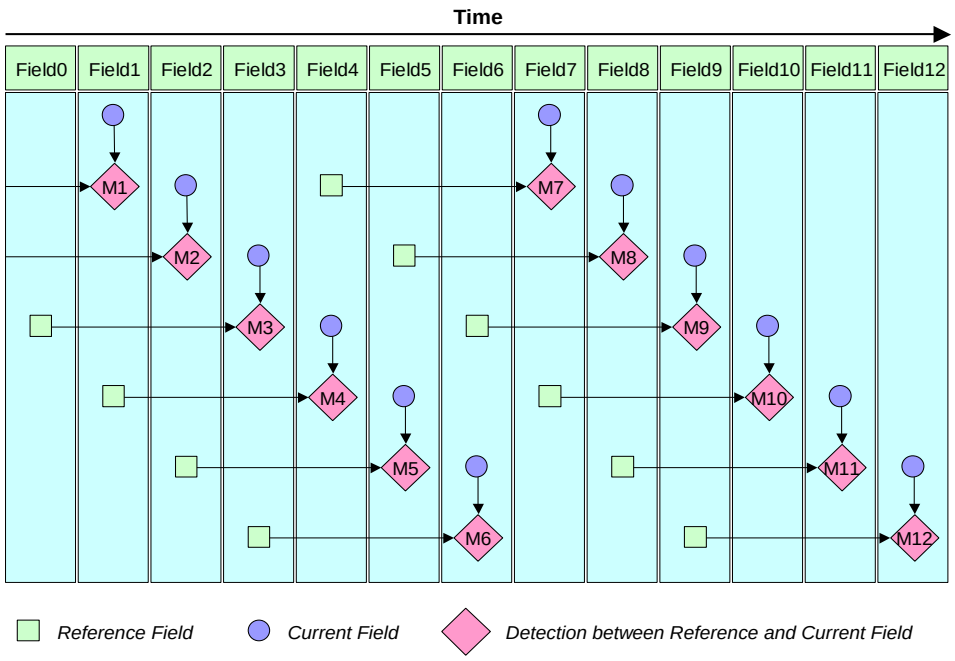


Fig 16 The relationship between current and reference field when MD_REFFLD = “0”

The TW2834 can update the reference field only at the period of MD_SPEED when MD_REFFLD is high. For this case, the TW2834 can detect a motion with sense of a various velocity. The Fig 17 shows the relationship between current and reference field for motion detection when MD_REFFLD = ”1”.

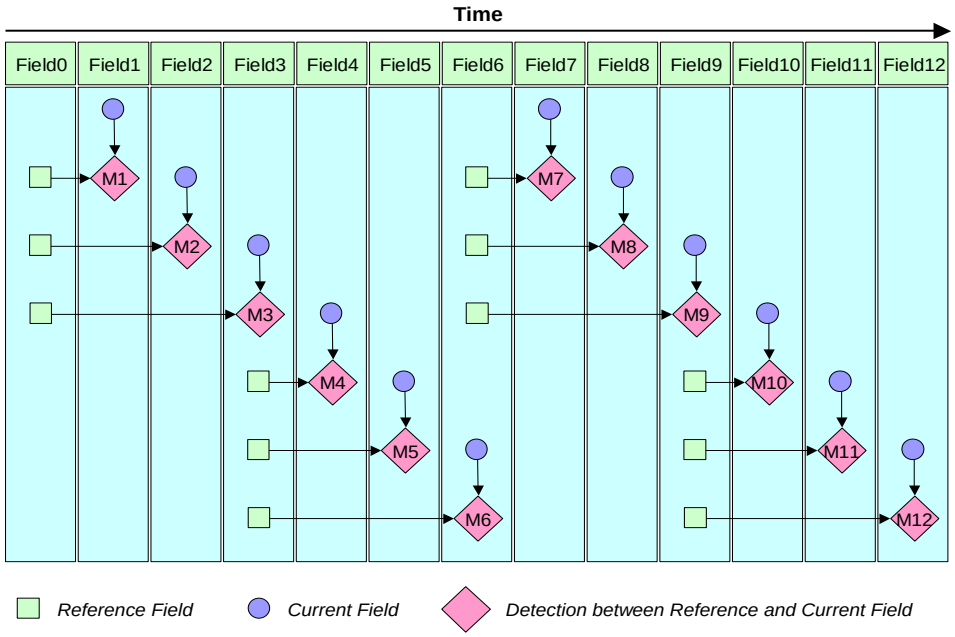


Fig 17 The relationship between current and reference field when MD_REFFLD = “1”

The TW2834 also supports the update timing control of the reference field/frame via the MD_STRB_EN and MD_STRB (2x83, 2xA3, 2xC3, 2xE3) register. For MD_STRB_EN = “0”, the reference field/frame is automatically updated and reserved on every reference field/frame. For MD_STRB_EN = “1”, the reference field/frame is updated and reserved only when MD_STRB = “1”. In this mode, the interval between current and reference field/frame depends on user’s strobe timing. This mode is very useful for non-realtime application such as pseudo-8ch application or for a specific purpose like non-periodical velocity control and very slow motion detection.

The TW2834 also provides the interrupt period control from the motion detection via the MD_DET_PERIOD (2x84, 2xA4, 2xC4, 2xE4) register. Normally, the motion detection information is sent to host by interrupt pin whenever motion is detected. However, if motion is detected very frequently, the host will be burden by too many interrupt requests. In this case, the TW2834 can send one interrupt request during the defined motion interrupt period.

Blind Detection

The TW2834 supports a blind input detection individually for 4 analog video inputs and makes an interrupt of blind detection to host. If video level in wide area of field is almost equal to average video level of field due to camera shaded by something, this input is defined as blind input.

The TW2834 has two sensitivity parameters to detect blind input such as level sensitivity via the BD_LVSENS (2x80, 2xA0, 2xC0, 2xE0) register and spatial sensitivity via the BD_CELSENS (2x80, 2xA0, 2xC0, 2xE0) register. The BD_LVSENS parameter controls threshold of level between cell and field average. The BD_CELSENS parameter defines the number of cells to detect blind. The TW2834 uses total 768 (32x24) cells of full screen. For BD_CELSENS = “0”, the number of cell whose level is same as average of field should be over than 60% to detect blind. The large value of BD_LVSENS and BD_CELSENS makes blind detector less sensitive.

Video Control

The TW2834 has dual video controllers for display and record path. Basically, each path requires only external 16M SDRAM for normal operation. However for display path, external SDRAM can be extended from 16M to 512M bits. This capability is related to save and recall function. The block diagram of video controller is shown in following Fig 18.

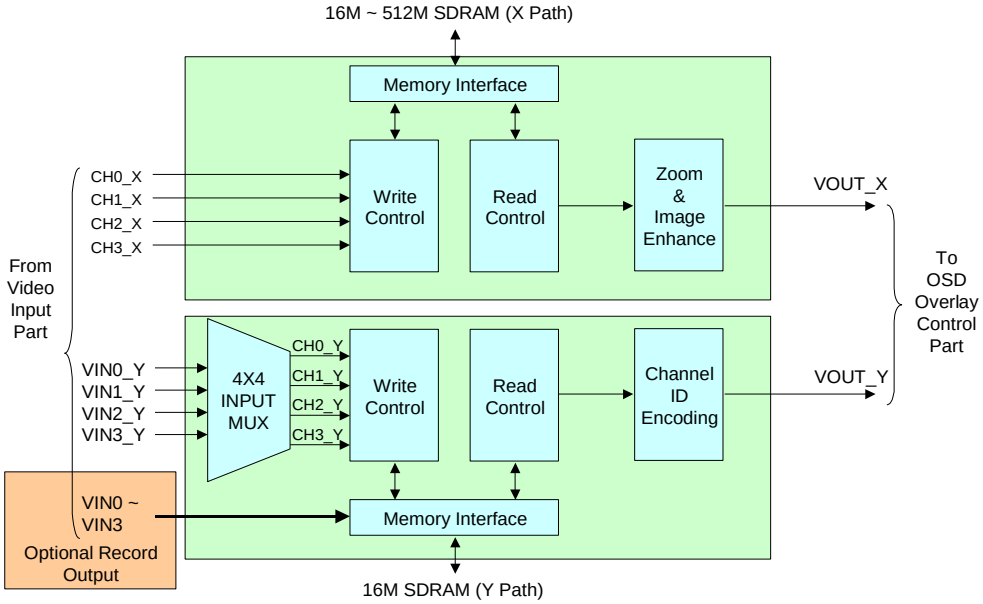


Fig 18 Block diagram of video controller

The TW2834 supports channel blanking, boundary on/off, blink, horizontal/vertical mirroring, and freeze function for each channel. The TW2834 can capture last 4 images automatically for each channel when video loss is detected.

The TW2834 has three operating modes such as live, strobe and switch mode. Each channel can be operated in its individual operating mode. That is, the TW2834 can be operated as multi-operating mode if each channel has different operating mode. Live mode is used to display real time video as QUAD or full live display, strobe mode is used to display non-realtime video with strobe signal from host and switch mode is used to display time-multiplexed video from several channels. For switch mode, the TW2834 supports two different types such as switch live and switch still mode.

The TW2834 also provides four record picture modes such as normal record mode and frame record mode and DVR normal record mode and DVR frame record mode. For record path, channel size and position have a limitation to half or full size in the horizontal and vertical direction.

For display path, the TW2834 can save and recall video through external extended SDRAM and support image enhancement function for non-realtime video such as freezing or playback video and provide high performance 2X zoom function. The TW2834 also supports dummy channel operation for display path. So it is very useful to implement pseudo-8ch display.

The TW2834 provides the channel ID encoding in both display and record path. The channel ID of record path contains all current picture configurations while the channel ID of display path has only channel switching information.

The TW2834 supports 4ch full D1 record output using SDRAM interface in record path. It’s useful for 4ch realtime recording and playback application. In this case, external SDRAM in record path cannot be used.

The TW2834 also provides chip-to-chip cascade connection for 8 or 16 channel application.

Channel Input Selection

The channel for display path can select 8 video inputs including 4 analog video inputs and 4 playback inputs, but the channel for record path can choose 4 analog video inputs. The analog video inputs can be selected via the DEC_PATH (0x22, 0x62, 0xA2, 0xE2 for display path, 1x60, 1x63, 1x66, 1x69 for record path) register and the playback inputs can be chosen via the PB_PATH (0x39) register. For display path, the PB_CH_EN (0x38) register can control the following video input path. The Fig 19 shows the internal channel input selection.

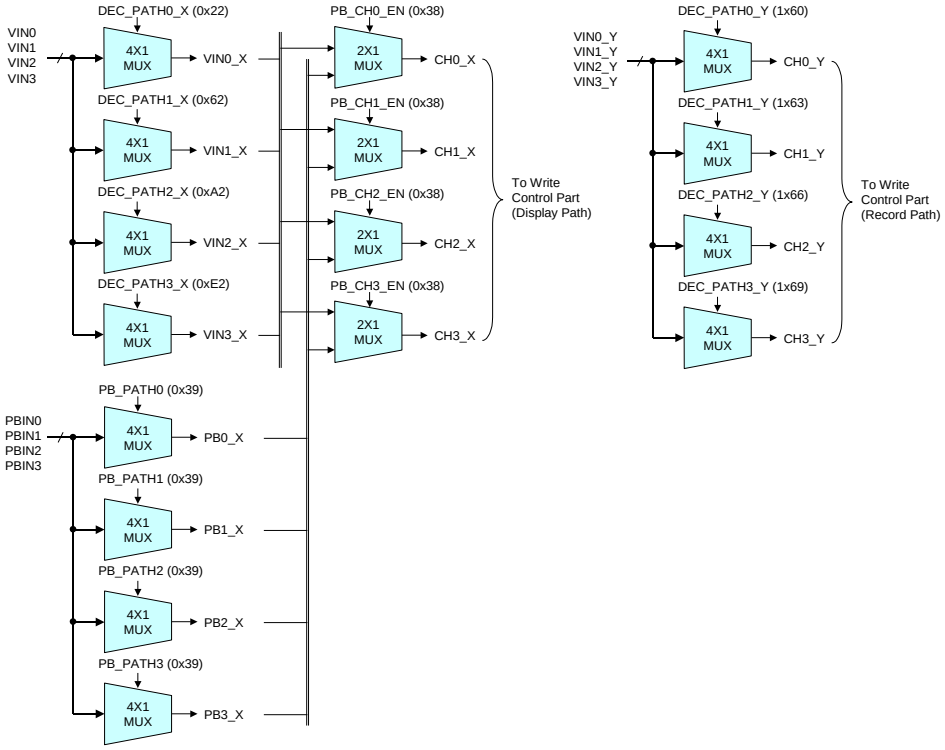


Fig 19 Channel input selection

Channel Operation Mode

Each channel can be working with three kinds of operating mode such as live, strobe and switch mode via the FUNC_MODE (1x10, 1x18, 1x20, 1x28 for display path, 1x60, 1x63, 1x66, 1x69 for record path) register. The operation mode can be selected individually for each channel so that multi-operating mode can be implemented.

Live Mode

If FUNC_MODE is “0”, channel is operated in live mode. For the live mode, the video display is updated with real time. This mode is used to display a live video such as QUAD, PIP, and POP.

When changing the picture configuration such as input path, popup priority, PIP, POP, and etc, the TW2834 supports anti-rolling sequence by monitoring channel update via the STRB_REQ register (1x04 for display path, 1x54 for record path) after changing to strobe operation mode (FUNC_MODE = “1”). The following Fig 20 shows the sequence to change picture configuration.

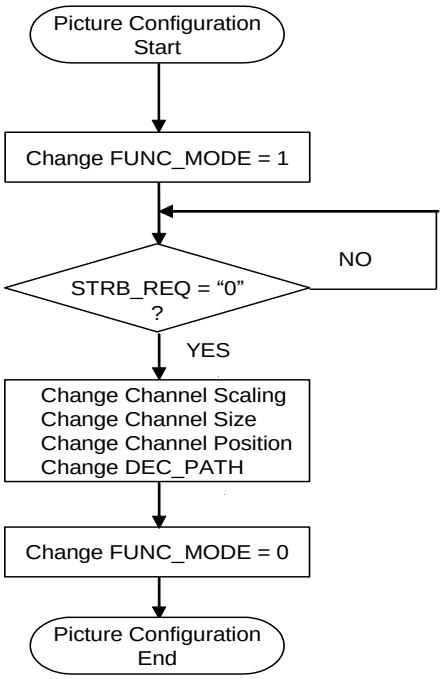


Fig 20 The sequence to change picture configuration

The status of STRB_REQ register can also be read through MPPDEC pin with control of the MPPSET (1x50) register.

Strobe Mode

If FUNC_MODE is “1”, channel is operated in strobe mode. For strobe mode, video display is updated whenever the TW2834 receives strobe command from host like CPU or Micom. If host doesn’t send a strobe command to the TW2834 anymore, the channel maintains the last strobe image until getting a new strobe command. This mode is useful to display non-realtime video input such as playback video with multiplexed signal input and to implement pseudo 8 channel application or dual page mode or panorama channel display. Specially, the TW2834 supports easy interface for pseudo 8channel application that will be covered in dummy channel function section. The TW2834 also supports auto strobe function for auto playback display that will be covered later in auto strobe function section.

Strobe operation is performed independently for each channel via the STRB_REQ (1x04, 1x54) register. But the STRB_REQ register has a different mode for reading and writing. Writing “1” into STRB_REQ in each channel makes the TW2834 updated by each incoming video. The updating status after strobe command can be known by reading the STRB_REQ register. If reading value is “1”, updating is not completed after getting the strobe command. In that case, this channel cannot accept a new strobe command or a disabling strobe command from host. To send a new strobe command, host should wait until STRB_REQ state is “0”. For freeze or non-strobe channel, the TW2834 can ignore the strobe command even though host sends it. In this case, the STRB_REQ register is cleared to “0” automatically without any updating video. The status of STRB_REQ register can also be read through MPPDEC pin with control of the MPPSET (1x50) register.

When updating video with a strobe command, the TW2834 supports field or frame updating mode via the STRB_FLD (1x04, 1x54) register. Odd field of input video can be updated and displayed for STRB_FLD = “0”, even field for “1”. For “2” of STRB_FLD register, the TW2834 doesn’t care for even or odd field, and updates video by next any field. If the STRB_FLD register is “3”, the strobe command updates video by frame. The following Fig 21 shows the example of strobe sequence for various STRB_FLD value.

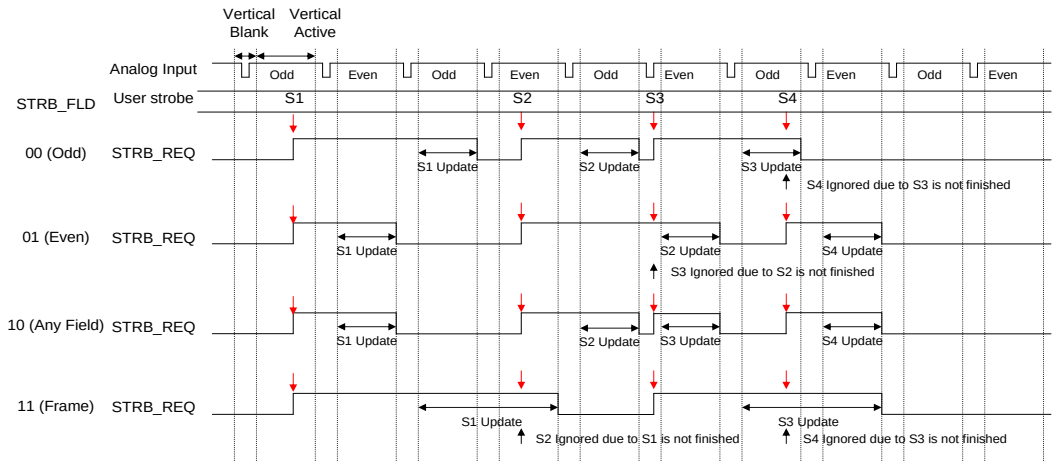


Fig 21 The example of strobe sequence for various STRB_FLD setting

The timing of strobe operation is related only with input video timing and strobe operation can be performed independently for each channel. So each channel is updated with different timing. The TW2834 provides a special feature as dual page mode using the DUAL_PAGE (1x04, 1x54) register. Although each channel is updated with different time, all channels can be displayed simultaneously in dual page mode. This means that the TW2834 waits until all channels are updated and then displays all channels with updated video at the same time. When dual page mode is enabled, host should send a strobe command for all channels and host should wait until all channels complete their strobe operations to send a new strobe command. The Fig 22 shows the example of 4 channel strobe sequences for dual page.

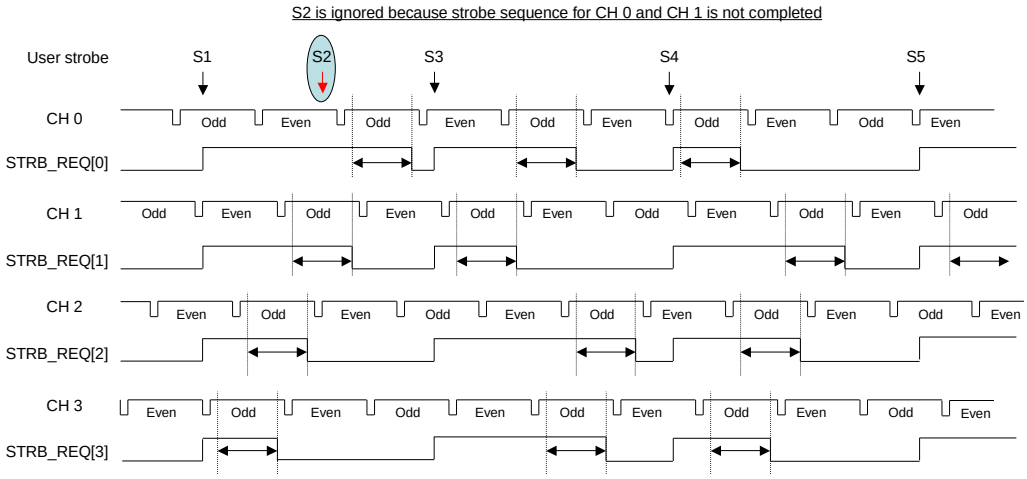


Fig 22 The example of 4 channel strobe sequences for dual page mode

Switch Mode

If FUNC_MODE is “2”, channel is operated in switch mode. The TW2834 supports 2 different types of switching mode such as still switching and live switching mode via the MUX_MODE (1x06, 1x56) register. For still switching mode, the TW2834 maintains the switched channel video as still image until next switching request, but for live switching mode the TW2834 updates every field of switched channel until next switching request. The live switching mode is used for channel sequencer without any timing loss or disturbing. In switch mode, there is a constraint that the picture size of all switched channel should be same even though their size can be varied. The TW2834 can switch the channel by fields or frames that can be programmed up to 1 field or 1 frame rate. But if the channel is on freeze state or disabled, the TW2834 ignores the request for switch mode.

The TW2834 contains 128 depth internal queues that have channel sequence information with internal or external triggering. Actual queue size can be defined by the QUE_SIZE (1x57) register. The channel switching sequence in the internal queue is changed by setting “1” to QUE_WR (1x5A) register after defining the queue address with the QUE_ADDR (1x5A) register and the channel switching information with the MUX_WR_CH (1x59) register. The QUE_WR register will be cleared automatically after updating queue. The channel sequence information can be read via the CHID_MUX_OUT (1x0A for display path, 1x5E for record path) register.

To operate the switching function properly, the channel switching should be requested with triggering that has three kinds of mode such as internal triggering from internal field counter, external triggering from external host or pin and interrupted triggering like alarm. The triggering mode can be selected by the TRIG_MODE (1x56) register. The TW2834 supports all triggering mode in record path, but provides only interrupt triggering mode in display path. The Fig 23 shows the structure of switching operation.

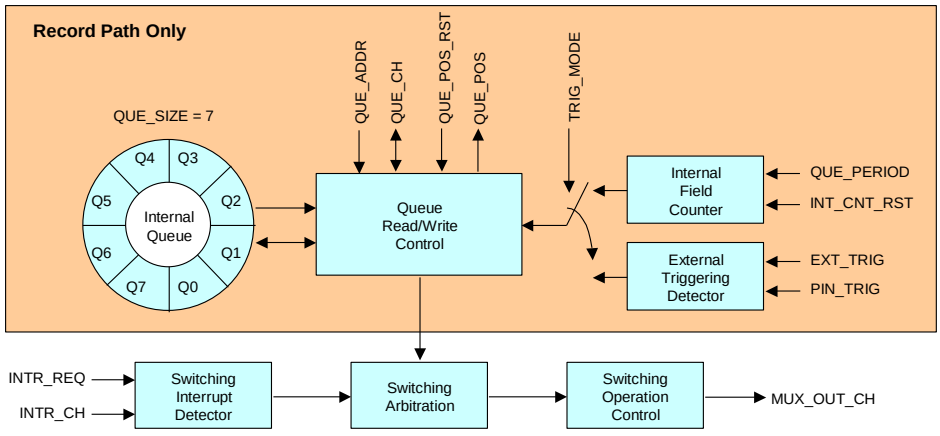


Fig 23 The structure of switching operation when QUE_SIZE = 7

For internal triggering mode, the switching period can be specified in the QUE_PERIOD (1x58) register that has 1 ~ 1024 field range. The internal field counter can be reset at anytime using the QUE_CNT_RST (1x5B) register and restarted automatically after reset. To reset an internal queue position, set “1” to QUE_POS_RST (1x5B) register and then the queue position will be restarted after reset. Both QUE_CNT_RST and QUE_POS_RST register can be cleared automatically after set to “1”. The following Fig 24 shows an illustration of QUE_POS_RST and QUE_CNT_RST. The next queue position can be read via the QUE_ADDR (1x5A) register.

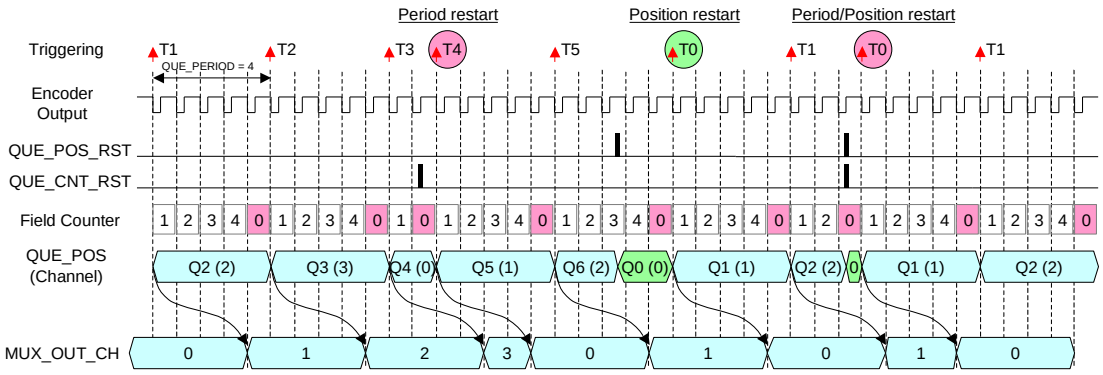


Fig 24 The illustration of QUE_POS_RST and QUE_CNT_RST

For external triggering mode, the request of channel switching comes from the EXT_TRIG (1x59) register or TRIGGER pin that is controlled by the PIN_TRIG_MD (1x56) register. Like internal triggering mode, writing “1” to the QUE_POS_RST register can reset the queue position in external triggering mode.

For interrupt triggering, host can request the channel switching at anytime via the INTR_REQ (1x07, 1x59) register. The switching channel is defined by the INTR_CH (1x07 for display path) or MUX_WR_CH (1x59 for record path) registers. Because the interrupted trigger has a priority over internal or external triggering in record path, the channel defined by the MUX_WR_CH can be inserted into the programmed channel sequence immediately.

The TW2834 also provides various switching types as odd field, even field or frame switching via the MUX_FLD (1x06, 1x56) register. For MUX_FLD = “0”, it is working as field switching mode with only odd field, but with only even field for MUX_FLD = “1”. For MUX_FLD = “2” or “3”, it is working as frame switching with both odd and even field. But in the frame record mode (it will be covered in “Frame Record Mode” section, page 55), the switching type is defined by the FRAME_FLD (1x01, 1x51) register.

Actually the channel switching is executed just before vertical sync of video output in field switching mode or before vertical sync of only odd field in frame switching mode. So all registers for switching should be set before that timing. Otherwise, the control values will be applied to the next field or frame.

For the reference timing of switching, the TW2834 provides the LINK pin whose represents the field transition with “1” for even field.

Likewise, the switching channel information is updated just before vertical sync of video output in field switching or before vertical sync of only odd field in frame switching mode. Basically it takes 4 field duration to display the switching channel from any triggering (field or frame). The host can read the current switching channel information through the MUX_OUT_CH (1x08, 1x6E) register. The TW2834 also support external pin output for this channel information with MPPDEC pin via the MPPSET (1x50) register. The switching channel information can also be discriminated by the channel ID in the video stream.

The illustration of channel switching is shown in the Fig 25 and Fig 26.

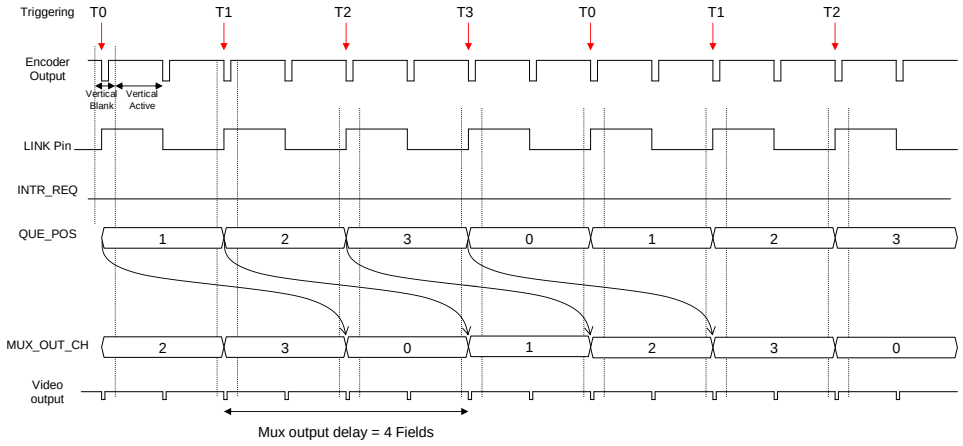


Fig 25 The illustration of switching sequence when QUE_SIZE = 3, QUE_PERIOD = 1

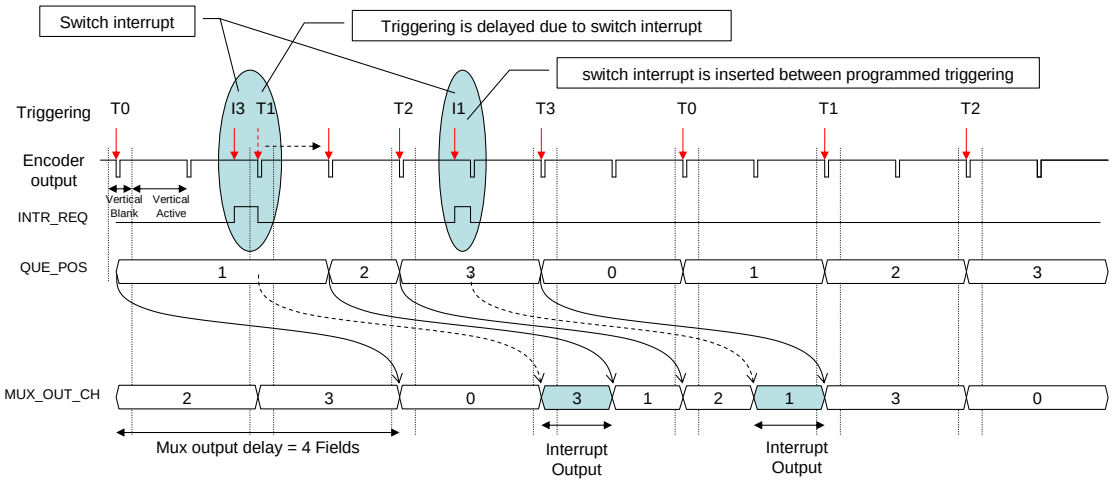


Fig 26 The interrupted switching sequence when QUE_SIZE = 3, QUE_PERIOD = 1

The TW2834 supports the skip function of the switching queue for switch mode in record path. In single chip application, the auto skip function of the switching queue can be supported if the MUX_SKIP_EN (1x5B) register is “1” and the NOVID_MODE is “1” or “3”. But in the chip-to-chip cascaded application, the skip function should be forced with the MUX_SKIP_CH (1x5C, 1x5D) register because the switching queue for whole channels is located in the lowest slaver device but cannot get the no-video information from the other chips.

The QUAD MUX function in chip-to-chip cascade application will be covered in the “Chip-to-Chip Cascade Operation (page 72)”.

Channel Attribute

The TW2834 provides various channel attributes such as channel enable, boundary selection, blank enable, freeze, horizontal/vertical mirroring for both display and record path. As special feature, the TW2834 supports the last image capture function, save/recall function, image enhancement and dummy channel display function for display path. For last image capture mode, channel can be blanked or boundary can be blinked automatically on no-video state.

Background Control

Summation of all active channel regions can be called as active region and the rest region except active region is defined as background region. The TW2834 supports background overlay and the overlay color is controlled via the BGDCOL (1x0F, 1x5F) register.

Boundary Control

The TW2834 can overlay channel boundary on each channel region using the BOUND (1x11, 1x13, 1x19, 1x1B, 1x21, 1x23, 1x29, 1x2B for display path, 1x61, 1x64, 1x67, 1x6A for record path) register and it can be blinked via the BLINK (1x11, 1x13, 1x19, 1x1B, 1x21, 1x23, 1x29, 1x2B for display path, 1x61, 1x64, 1x67, 1x6A for record path) register when BOUND is high. The boundary color can be selected through the BNDCOL (1x0F, 1x5F) register. The blink period can be also controlled through the TBLINK (1x02, 1x52) register.

Blank Control

Each channel can be blanked with specified color using the BLANK (1x11, 1x13, 1x19, 1x1B, 1x21, 1x23, 1x29, 1x2B for display path, 1x61, 1x64, 1x67, 1x6A for record path) register and the blank color can be specified via the BLKCOL (1x0F, 1x3F) register.

Freeze Control

Each channel can capture last 4 field images whenever freeze function is enabled and display 1 field image out of the captured 4 field images using the FRZ_FLD (1x0F, 1x3F) register. The freeze function can be enabled or disabled independently for each channel via the FREEZE (1x11, 1x13, 1x19, 1x1B, 1x21, 1x23, 1x29, 1x2B for display path, 1x61, 1x64, 1x67, 1x6A for record path) register.

Last Image Capture

When video loss has occurred or gone, the TW2834 provides 4 kinds of indication such as bypass of incoming video, channel blank, capture of last image, and capture of last image with blinking channel boundary depending on the NOVID_MODE (1x05, 1x55) register. This function is working automatically on video loss. The capturing last image is same as freeze function described above. User can select 1 field image out of captured 4 filed images via the FRZ_FLD (1x0F, 1x5F) register which is shared with freeze function.

Horizontal / Vertical Mirroring

The TW2834 supports image-mirroring function for horizontal and/or vertical direction. The horizontal mirroring is achieved via the H_MIRROR (1x11, 1x13, 1x19, 1x1B, 1x21, 1x23, 1x29, 1x2B for display path, 1x61, 1x64, 1x67, 1x6A for record path) register and the vertical mirroring is attained via the V_MIRROR (1x11, 1x13, 1x19, 1x1B, 1x21, 1x23, 1x29, 1x2B for display path, 1x61, 1x64, 1x67, 1x6A for record path) register. It is useful for a reflection image in the horizontal and vertical direction.

Display Path Control

The TW2834 can save images in external memory and recall them to display. This function can be working in display path only because the external memory can be extended from 16M to 512M bits only in display path. The TW2834 also supports the special filter to enhance image quality in display path for non-realtime video display such as recalled image from saving images and playback with multiplexed video source. The TW2834 provides high performance 2X zoom function in the vertical and horizontal direction. The TW2834 supports any kind of picture configuration for display path with variable picture size, position and pop-up control. The TW2834 also provides a dummy channel function for pseudo 8ch application.

Save and Recall Function

The save/recall function can be working independently for each channel and the number of the saved images depends on the extended memory capability, picture size and field type. The TW2834 can save image only in live channel so that it cannot be saved in freezing channel. If channel is working on strobe operating mode, this channel can be saved with new strobe command. For switch operating mode, the channel can be saved only on switching time because this channel can be updated at this moment.

To save image, several parameters should be controlled that are the SAVE_FLD, SAVE_HID, SAVE_REQ (1x03) and SAVE_ADDR (1x02) registers. The SAVE_FLD determines field or frame type for image to be saved. Even though the channel to be saved is hidden by upper layer picture, it can be saved using the SAVE_HID register that makes no effect on current display. The saving function is requested by writing “1” to the SAVE_REQ register and this register will be cleared when saving is done. Before it is cleared, the TW2834 cannot accept new saving request. The SAVE_ADDR register defines address where an image will be saved. Because 4M bits is allocated for each 1 field image, SAVE_ADDR unit is 4M bits and can have range 0 ~ 127 for 512M bits. The first 0~ 3 addresses are reserved for normal operation so that it cannot be used for saving function.

To recall the saved video image, several parameters are required such as RECALL_FLD (1x03), RECALL_EN (1x11, 1x13, 1x19, 1x1B, 1x21, 1x23, 1x29, 1x2B) and RECALL_ADDR (1x12, 1x14,

1x1A, 1x1C 1x22, 1x24, 1x2A, 1x2C) registers. If the RECALL_EN is “1”, the TW2834 recalls the saved image that is located at RECALL_ADDR in external memory and displays it just like incoming video. The RECALL_FLD register determines 1 field or 1 frame mode to display. The following Fig 27 illustrates the relationship between external SDRAM size and SAVE_ADDR / RECALL_ADDR.

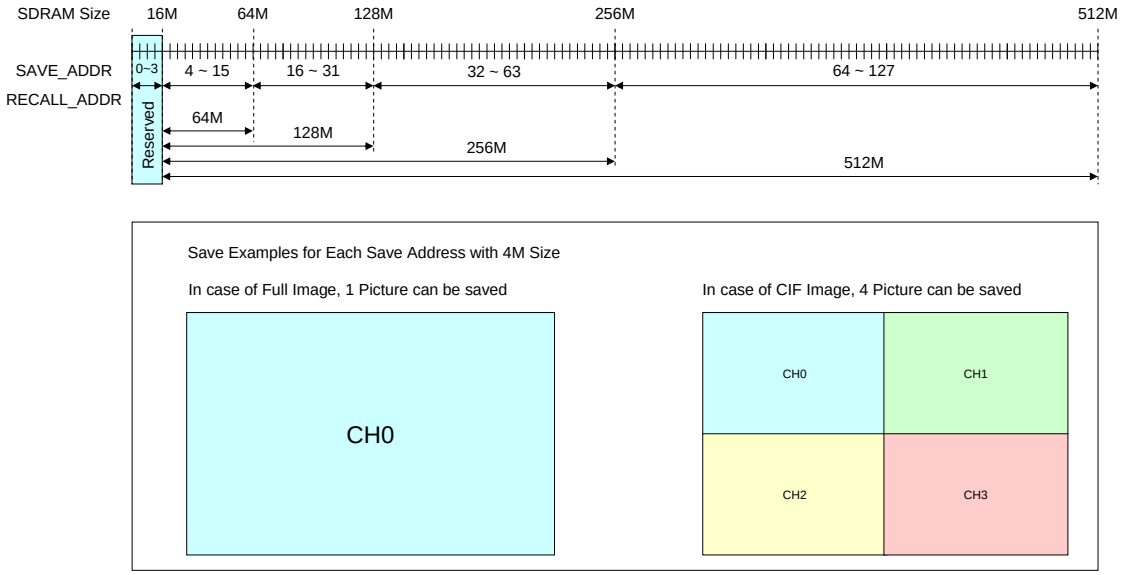


Fig 27 The relationship between SDRAM size and SAVE_ADDR / RECALL_ADDR

Image Enhancement

In non-realtime video such as freeze image, recalled image from saving images and playback video which records multi-channel video using field switching, so many line flicker noise can be found in image because it displays same field image for both odd and even field. The embedded filter in the TW2834 can remove effectively this line flicker noise and be enabled via the ENHANCE (1x11, 1x13, 1x19, 1x1B, 1x21, 1x23, 1x29, 1x2B) register for each channel. This filter coefficient can be controlled via the FR_EVEN_OS and FR_ODD_OS (1x0B) register.

Zoom Function

The TW2834 supports high performance 2X zoom function in the vertical and horizontal direction for display path. The zoom function can be working in any operation mode such as live, strobe and switch mode. Conventional system also has zoom function, but it has a very poor quality due to line flicker noise even though interpolation filter is adapted. The TW2834 provides high quality zoom characteristics using high performance interpolation filter and image enhancement technique. When zoom is executed, the image enhancement is operated automatically and the filter coefficient can be controlled via the ZM_EVEN_OS and ZM_ODD_OS (1x0B) register.

The zoomed region will be defined with the ZOOMH (1x0D) and ZOOMV (1x0E) registers and can be displayed depending on the ZMBNDCOL, ZMBNDEN, ZMAREAEN, ZMAREA (1x0C) register. The zoom operation is enabled via the ZMENA (1x0C) register.

Picture Size and Popup Control

Each channel region can be defined using its own PICHL (1x30, 1x34, 1x38, 1x3C), PICHR (1x31, 1x35, 1x39, 1x3D), PICVT (1x32, 1x36, 1x3A, 1x3E), and PICVB (1x33, 1x37, 1x3B, 1x3F) register. If more than 2 channels have same region, there will be a conflict of what to display for that area. Generally the TW2834 defines that the channel 0 has priority over channel 3. So if a conflict happens between more than 2 channels, the channel 0 will be displayed first as top layer and then channel 1 and 2 and 3 are hidden beneath.

The TW2834 also provides a channel pop-up attribute via the POP_UP (1x10, 1x18, 1x20, 1x28) register to give priority for another display. If a channel has pop-up attribute, it will be displayed as top layer. This feature is used to configure PIP (Picture-In-Picture) or POP (Picture-Out-Picture). The following Fig 28 shows the channel definition and priority for display path.

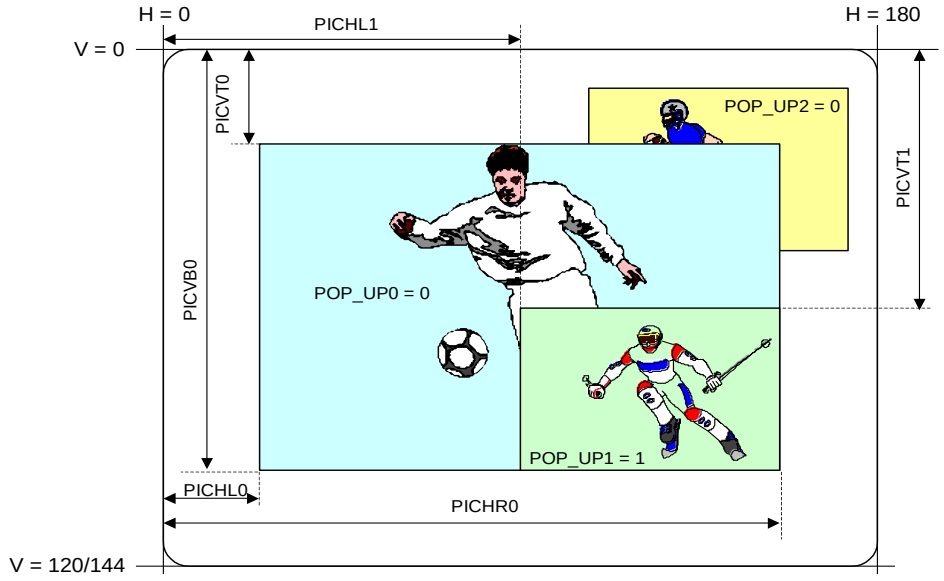


Fig 28 The channel position and priority in display path

Dummy Channel Function

The TW2834 supports additional 4 dummy channel controllers to display up to 8 channel videos in display path for non-realtime application. That is, this dummy channel is useful to implement low cost and high feature application system such as pseudo 8-channel QUAD system.

The TW2834 has 4 main channel controllers as described before and each main channel has its own corresponding dummy channel. The dummy channel has input source selection and pop-up attribute in common with the main channel, but has its own attributes such as boundary, blank, enhancement, recall and so on.

To use dummy channel function, dummy channel region should be defined in the DMPICHL (1x40, 1x44, 1x48 and 1x4C), DMPICHR (1x41, 1x45, 1x49 and 1x4D), DMPICVT (1x42, 1x46, 1x4A and 1x4E), and DMPICVB (1x43, 1x47, 1x4B and 1x4F) registers and dummy channel should be enabled using the DMCH_EN (1x10, 1x18, 1x20 and 1x28) register. The updated input selection can be controlled via the DMCH_PATH (1x10, 1x18, 1x20 and 1x28) register. If the DMCH_PATH is “1”, the dummy channel will be updated, but if DMCH_PATH is “0”, the main channel will be updated. So the updated input selection should be defined before update such as during vertical blanking time or between completed strobe and new strobe.

This dummy channel can also be used to display 8 split channel for playback input with multiplexed or dual page video format. For playback application using auto cropping and auto strobe mode, the updated input selection is controlled automatically from channel ID decoder when dummy channel is enabled.

The following Fig 29 shows pseudo 8-channel operation using dummy channel function, strobe operating mode and internal analog switch.

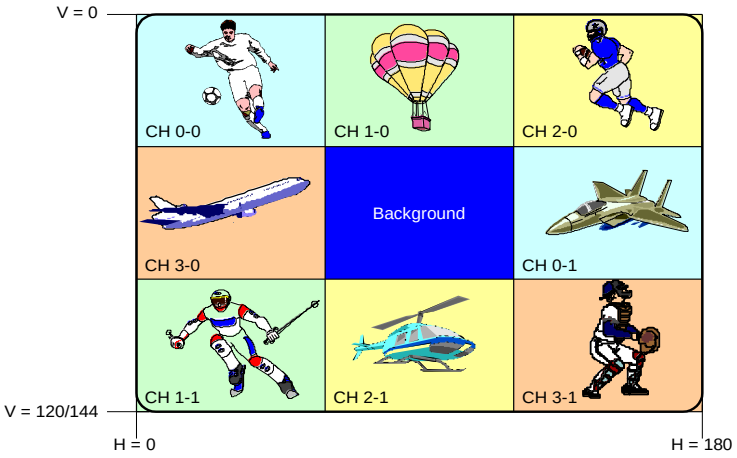


Fig 29 Pseudo 8 channel operation

Record Path Control

The TW2834 supports 4 record modes such as normal record mode, frame record mode, DVR record mode and DVR frame record mode. The DVR record mode and DVR frame record mode generate continuous video stream for each channel and transfer it to compression part (M-JPEG or MPEG) so that they are very useful for DVR application. The frame record mode can be used to record each channel with full vertical resolution. The record mode is selected via the DIS_MODE and FRAME_OP (1x51) register. If the FRAME_OP is “0”, the DIS_MODE = “0” stands for normal record mode and the DIS_MODE = “1” represents DVR record mode. If the FRAME_OP is “1”, the DIS_MODE = “0” stands for frame record mode and the DIS_MODE = “1” represents DVR frame record mode.

The TW2834 support high performance free scaler for vertically and horizontally in display path, but has the size and position limitation such as Full / Quad / CIF in record path.

The TW2834 can provide various record formats with various record modes (normal/frame/DVR /DVR frame), operation modes (live/strobe/switch) and respective size/position definition. Many illustration and detail description is covered in the application note.

The TW2834 also supports four channel real-time record mode with full D1 format. In this case, the external SDRAM in record path should not be used so that four channel full D1 data can be output though the SDRAM interface pin.

Normal Record Mode

Each channel position and size can be defined using its own PIC_SIZE (1x6C), and PIC_POS (1x6D) register. The channel size is defined via the PIC_SIZE register such as “0” for Horizontal/Vertical half size (QUAD), “1” for Horizontal full size and Vertical half size, “2” for Horizontal half size and Vertical full size, and “3” for Horizontal/Vertical full size. The channel position is defined via the PIC_POS register such as “0” for no Horizontal/Vertical offset, “1” for Horizontal half picture offset, “2” for Vertical half picture offset and “3” for Horizontal/Vertical half picture offset. The channel size and location should be defined within the full picture size (i.e. PIC_SIZE = “3” & PIC_POS = “2” is not allowed).

The horizontal full size of picture is controlled via the SIZE_MODE (1x51) register such as “0” for 720 pixels, “1” for 702 pixels, and “2” for 640 pixels. Likewise, the vertical full size is selected by the SYS5060 (1x00) register such as “0” for 240 lines and “1” for 288 lines.

If more than 2 channels have same region, there will be a conflict of what to display for that area. Generally the TW2834 defines that the channel 0 has priority over channel 3. So if a conflict happens between more than 2 channels, the channel 0 will be displayed first as top layer and then the channel 1 and 2 and 3 are hidden beneath. The TW2834 also provides a channel pop-up attribute via the POP_UP (1x60, 1x63, 1x66, and 1x69) register to give priority for another display. If a channel has pop-up attribute, it will be displayed as top layer. The following Fig 30 shows the example of the channel position and size control in normal record mode.

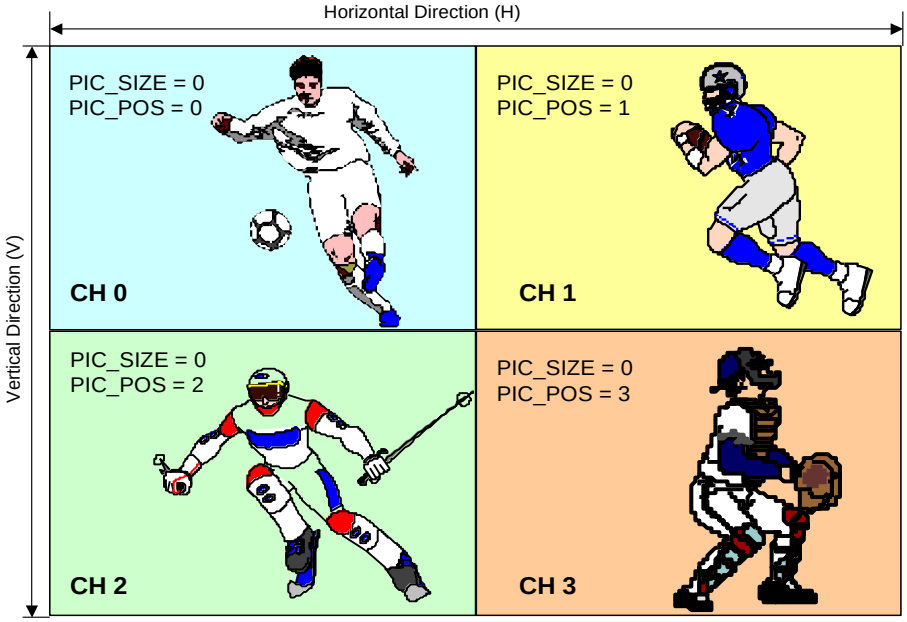


Fig 30 The channel position and size control in normal record mode

Frame Record Mode

The frame record mode is similar to normal record mode except that the definition of picture size is extended to frame area and only one field data can be output in 1 frame. The odd or even field selection is controlled via the FRAME_FLD (1x51) register. Like normal record mode, each channel position and size can be defined using its own PIC_SIZE (1x6C), and PIC_POS (1x6D) register. The channel size is defined via the PIC_SIZE register such as “0” for Horizontal half size and Vertical full size, “1” for Horizontal/Vertical full size, but “2” or “3” is not allowed. That is, the channel size for vertical direction supports only one field size. The channel position is defined via the PIC_POS register such as “0” for no Horizontal/Vertical offset, “1” for Horizontal half picture offset, “2” for Vertical 1 field offset, and “3” for Horizontal half picture offset and Vertical 1 field offset. The channel size and location should be defined within the full picture size. In frame record mode, the TW2834 also supports the full operation mode such as live, strobe or switch operation and provides a pop-up attribute via the POP_UP register. The Fig 31 shows the example of the channel position and size control in frame record mode.

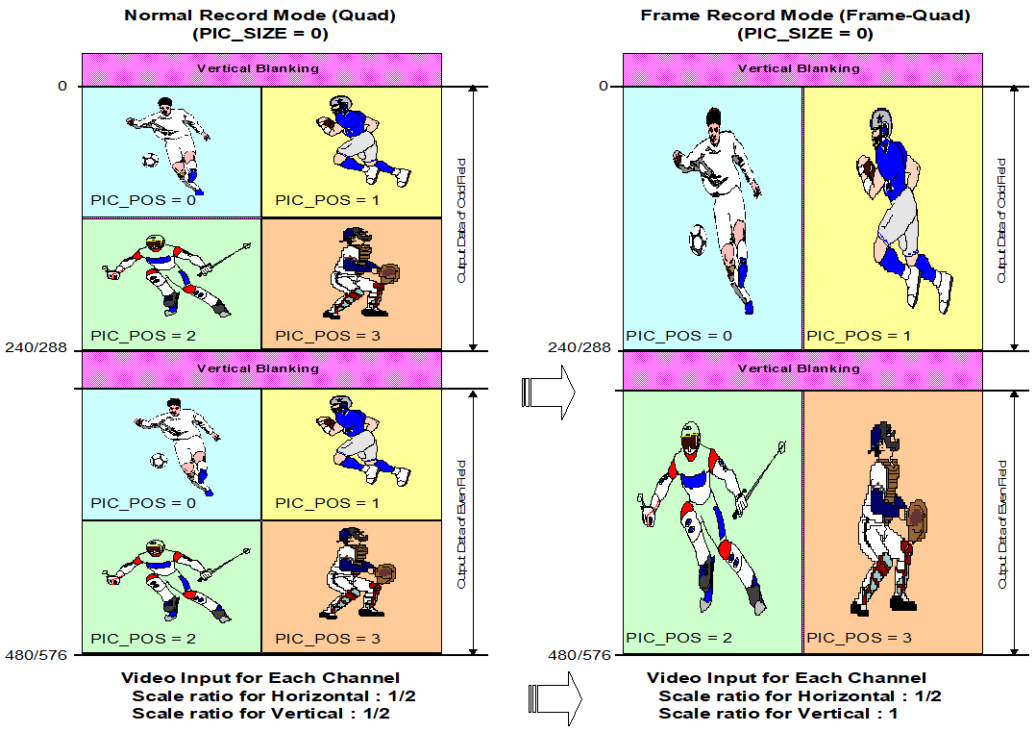


Fig 31 The channel position and size control in frame record mode

DVR Normal Record Mode

The DVR normal record mode outputs the continuous video stream for compression part (M-JPEG or MPEG) in DVR application. Like normal record mode, each channel position and size can be defined using its own PIC_SIZE (1x6C), and PIC_POS (1x6D) register.

The channel size is defined via the PIC_SIZE register such as “0” for Horizontal/Vertical half size (QUAD), “1” for Horizontal full size and Vertical half size, “2” for Horizontal half size and Vertical full size, and “3” for Horizontal/Vertical full size. The channel position is defined via the PIC_POS register such as “0” for no Vertical offset, “1” for Vertical 1/4 picture offset, “2” for Vertical 1/2 picture offset and “3” for Vertical 3/4 picture offset. The channel size and location should be defined within the full picture size. In DVR normal record mode, the TW2834 also supports the full operation mode such as live, strobe or switch operation and provides a pop-up attribute via the POP_UP register. But the channel boundary is not supported in DVR normal record mode. The following Fig 32 shows the example of the channel position and size control in DVR normal record mode.

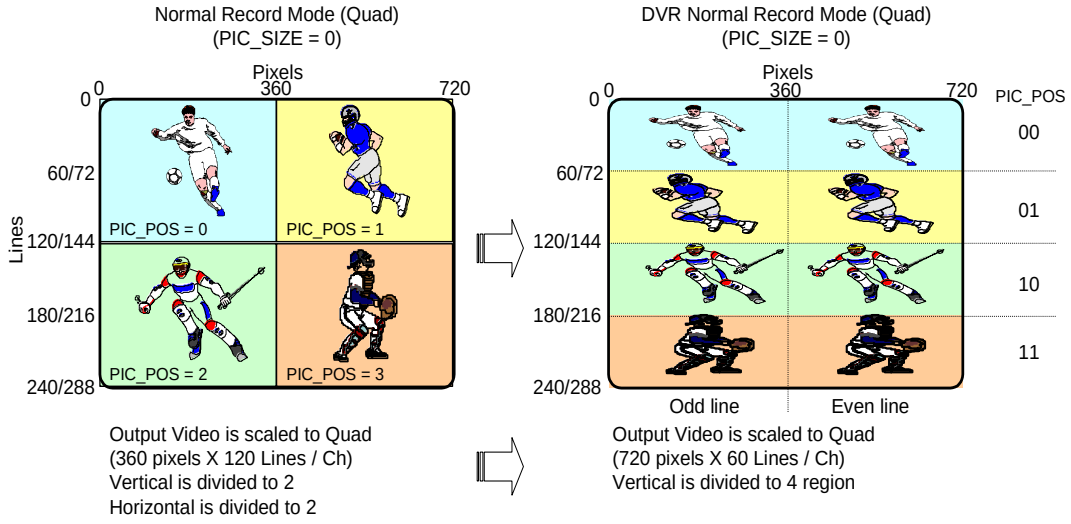


Fig 32 The channel position and size control for DVR normal record mode

DVR Frame Record Mode

The DVR frame record mode is the combination of frame record mode and DVR normal record mode. The odd or even field selection is controlled via the FRAME_FLD (1x51) register like frame record mode. The TW2834 also supports the full operation mode such as live, strobe or switch operation, but the channel boundary is not supported in DVR frame record mode. The following Fig 33 shows the example of DVR frame record mode.

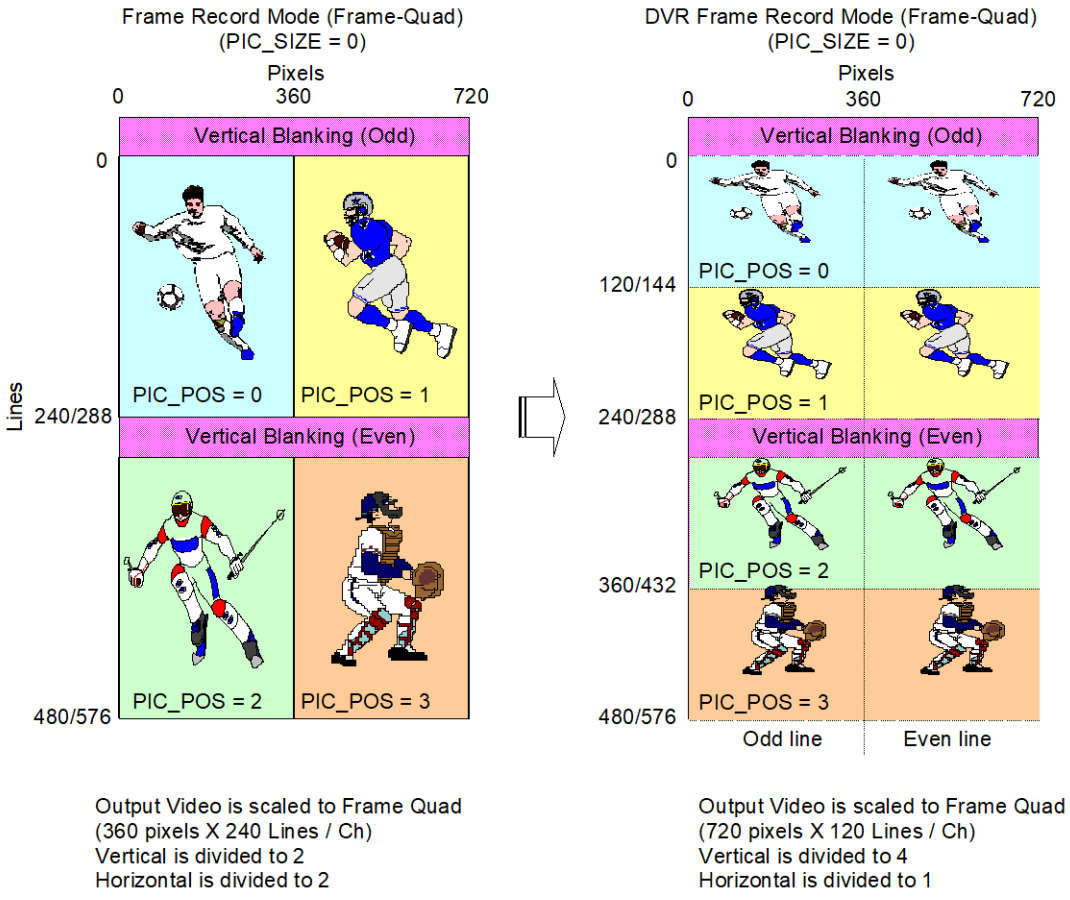


Fig 33 The channel position and overlay for DVR frame record mode

Realtime Record/Playback Mode

The TW2834 supports 4 channel real-time record output with full D1 or scaled format. In this case, the external SDRAM in record path should not be used so that four channel full D1 data can be output with 54MHz ITU-R BT 656 format though the SDRAM interface pins such as DATAY[15:0], ADDRY [10:0], BA0Y, WEBY, RASBY, CASBY, and DQMY pin. The I/O of SDRAM Interface pins are controlled via the MEM_OP_EN (1x55) register such as “0” for 4 channel digital output mode and “1” for normal operation mode. The real-time record output format can be selected via the DEC_BYP_EN (1xBB) register such as “1” for scaled display output mode, “2” for scaled record output mode, and “3” for full D1 output mode. Four channel real-time record output is synchronous with each video decoder timing. Each channel H/V/F signal can be monitored through the MPPDEC pins via the control of the MPPSET (1x50) register. The following Fig 34 shows the example of 4 channel real-time record / playback application.

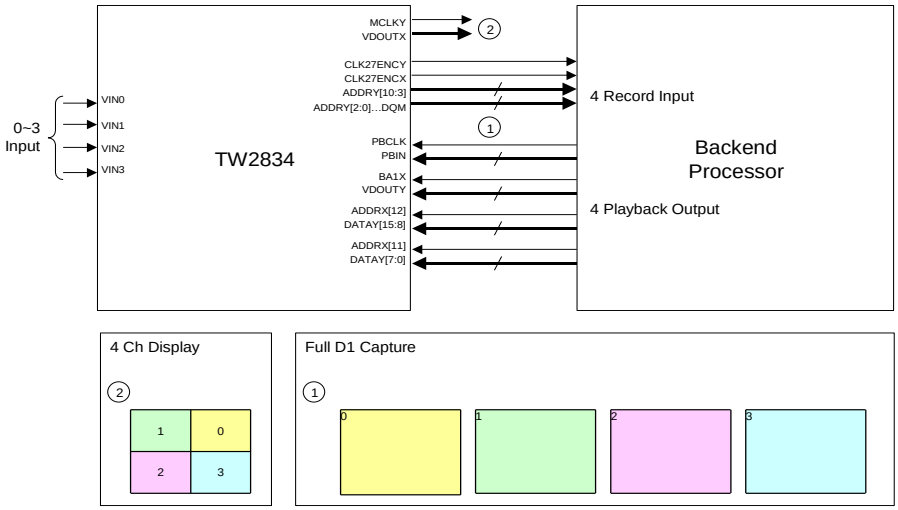


Fig 34 The example of 4 channel record connection with 54MHz time multiplexing

Playback Path Control

The TW2834 supports the playback function for variable record mode input such as normal record mode, frame record mode, DVR normal record mode, and DVR frame record mode. The TW2834 also supports auto cropping and auto strobe function for playback input with auto channel ID decoding.

The TW2834 provides various playback functions for normal record mode input. If the channel operation mode is live mode (FUNC_MODE = “0”), the playback input can be bypassed in display path, but the auto cropping function from the channel ID decoder is available to separate each channel from the multi-channel format such as QUAD (Auto cropping function is described in “Cropping Function” section, page 26).

The TW2834 supports not only auto cropping function but also auto strobe function for playback input through auto channel ID decoder. The auto strobe function implies that the selected channel by the PB_CH_NUM (1x16, 1x1E, 1x26, 1x2E) register is updated automatically from the playback input of the time-multiplexed full D1 or quad format via auto channel ID decoder.

If the channel operation mode is strobe mode (FUNC_MODE = “1”), the auto strobe function is used to update the channel automatically. The TW2834 also supports event strobe mode using event information in auto channel ID. It makes the channel updated whenever event information in auto channel ID is detected. The event strobe mode can be enabled via the EVENT_PB (1x16, 1x1E, 1x26, 1x2E) register. The auto strobe function can also be used to display pseudo 8-channel with dummy channel for playback input of the dual page or pseudo 8-channel MUX using analog switch.

The TW2834 also provides an anti-rolling function for picture configuration change in playback application via the PB_STOP (1x16, 1x1E, 1x26, 1x2E) register. If the PB_STOP is set to high in strobe operation mode (FUNC_MODE = “1”), the channel is not updated until the PB_STOP is set to low after picture configuration change.

Normal Record Mode

The following Fig 35 shows the examples of playback function for normal record mode using cropping, scaling and repositioning.

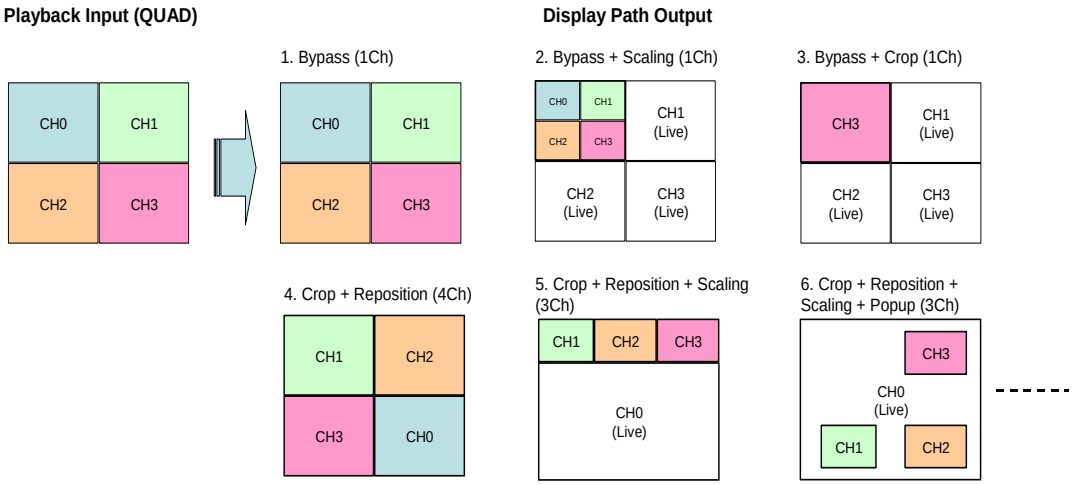


Fig 35 The examples of the playback function for normal record mode

The following Fig 36 shows the various examples for auto cropping and strobe function.

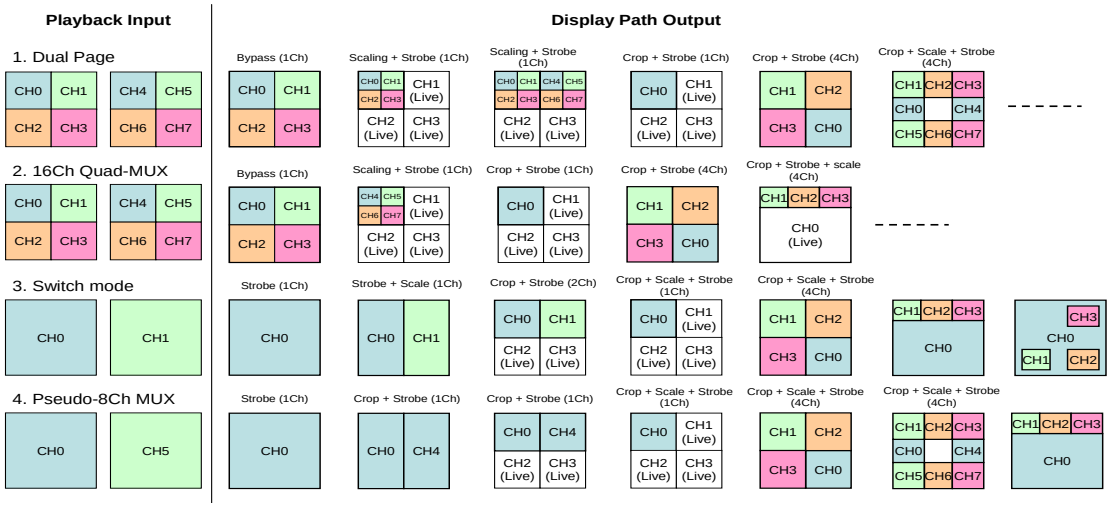


Fig 36 The example of auto strobe function for normal record mode

Frame Record Mode

The TW2834 supports the playback function for playback input of frame record mode. The playback input of frame record mode is formed with 1 frame so that the vertical lines of each playback channel have twice as many as the normal record mode. So if the displayed channel size is half size of the playback input in vertical direction, the playback input can be separated into two (odd/even) fields according to the line numbers such as odd line for odd field and even line for even field. With this conversion, the vertical resolution of the playback input can be enhanced compared with simple half vertical scaling of the playback input. This mode can be enabled via the FIELD_OP (1x76) register. The following Fig 37 shows the illustration of this conversion from frame record mode to normal display mode in playback application.

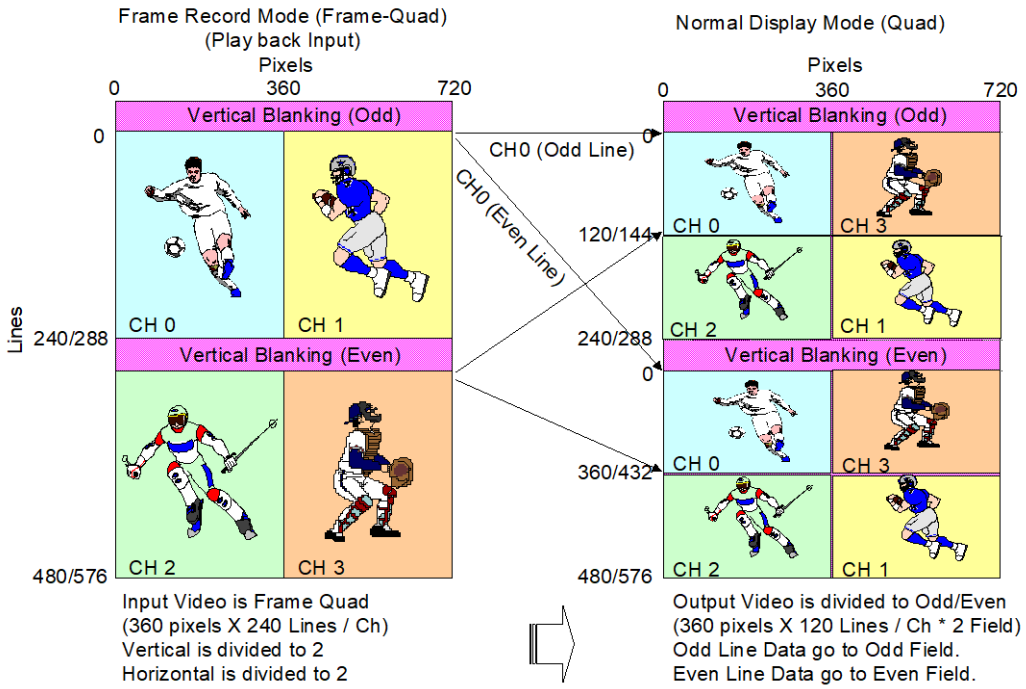


Fig 37 The conversion from frame record mode to normal display mode

The following Fig 38 shows the various examples of auto cropping and strobe function for playback input of frame record mode.

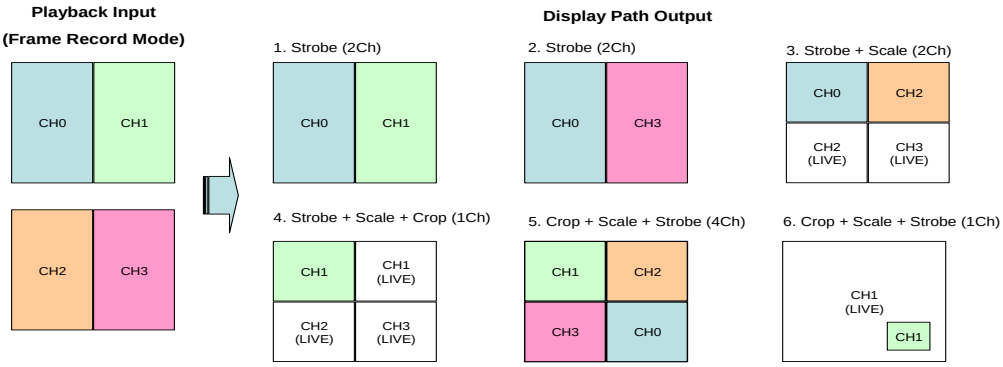


Fig 38 The examples of the playback function for frame record mode

DVR Normal Record Mode

If the playback input is the DVR normal record mode, it cannot be displayed directly because it is special mode not for display but for record to compression part. The TW2834 supports the conversion from this DVR normal record mode to normal display mode via the DVR_IN (1x76) register. For auto cropping function of the playback with this mode, the PB_CROP_MD (0x38) register should be set into “1” to crop the 1/4 vertical picture size (Please refer to “Cropping Function” section in Page 26). The auto strobe function and all channel attributes can also be supported, but the scaling function cannot be supported in this mode. The following Fig 39 shows the illustration of conversion from DVR normal record mode to normal display mode in playback application.

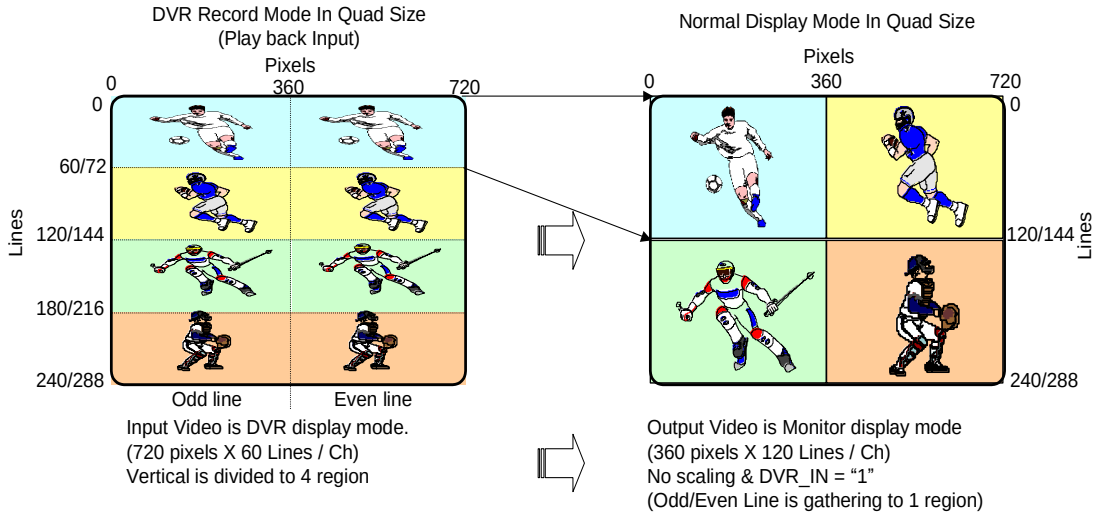


Fig 39 The conversion from DVR normal record mode to normal display mode

DVR Frame Record Mode

The TW2834 also provides the conversion from DVR frame record mode to normal display mode using combination of frame record mode and DVR normal record mode via the DVR_IN and FIELD_OP (1x76) register. Likewise, the auto strobe function and all channel attributes can also be supported, but the scaling function cannot be supported in this mode. The following Fig 40 shows the illustration of conversion from DVR frame record mode to normal display mode in playback application.

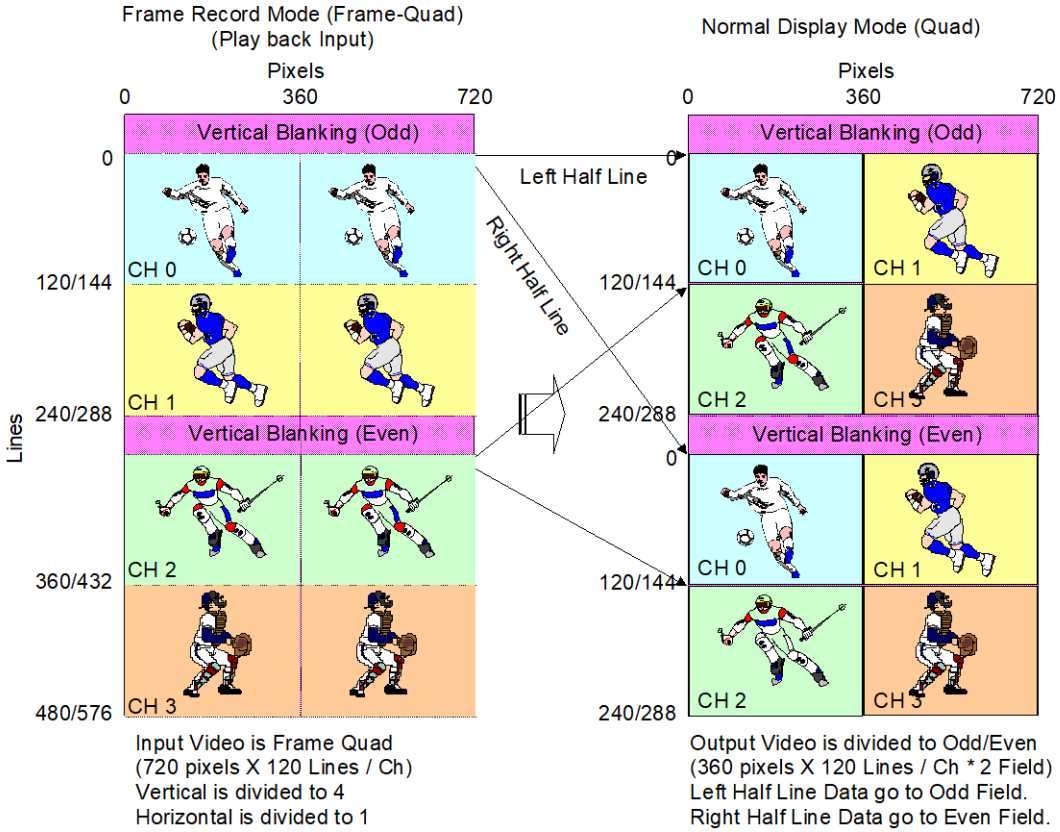


Fig 40 The conversion from DVR frame record mode to normal display mode

Real-time Record/playback Mode

The TW2834 provides 4 channel playback input in real-time 4 channel full D1 record application. This mode supports ITU-R BT. 656 interface with 27MHz through the PBIN, DATAY, VDOUTY pins for 4 playback inputs. The DATAY[15:0] pins are used for playback input 2 and 3 via the DEC_BYP_EN (1xBB) register such as “0” for normal operation mode, and “1/2/3” for playback input mode. The VDOUTY pins are used for playback input 1 via the VDOUTY_MODE (1x8C) register. The ADDRX [12:11] and BA1X pin can be used for 4ch playback clock input via the ADDR_OUT_EN (1x05) register.. In this case, the Save/Recall function of display path cannot be supported because the extended SDRAM pin interface is shared for it. The following Fig 41 shows the example of 4 channel real-time record/playback application.

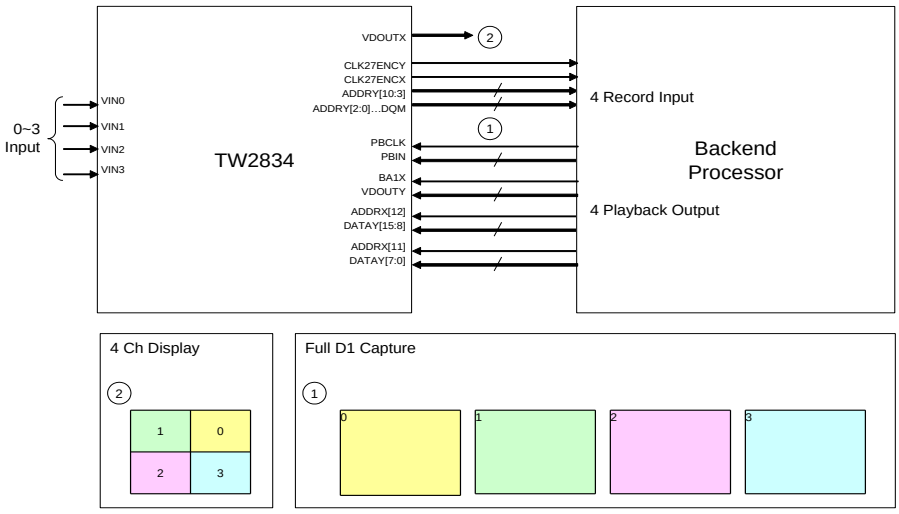


Fig 41 The example of 4 channel real-time record/playback application

Real-time Record/Spot Mode

The TW2834 provides 4 channel realtime record output, 1 channel spot output, 1 channel display output and 1 channel playback input simultaneously. In this mode the SDRAM interface for Y path are used for spot output with normal operation and the VDOUTX pins are used for output interface of display and spot data with 54MHz ITU-R BT 656 format. The VDOUTY pins are used for real-time record output interface of channel 2/3 via the BYPASS_Y (1x83) register of “11b” value and CCIR_IN_SEL (1x80) register of “2, 3” value. The MPPDEC pins are used for real-time record output interface of channel 0/1 via the BYP_MPP (1xBB) register of “1” value, MPPSET_X register of “8” value and MPPSET_Y (1x 50) register of “9” value.

In this mode, the TW2834 support independent 2 analog output for display and spot, but provides only 1 playback input interface through the PBIN pins and cannot be extended to 8/16 application because MPPDEC pins are used for real-time record output interface.

The following Fig 42 shows the example of 4 channel real-time record/spot application.

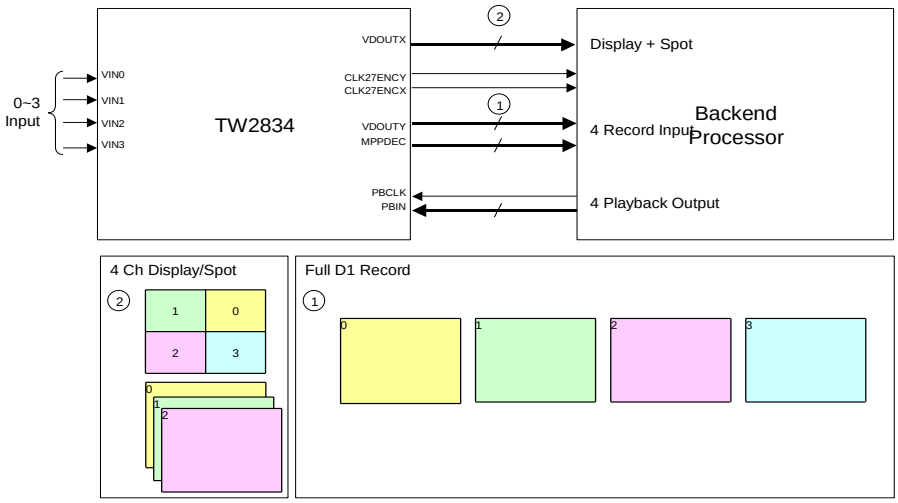


Fig 42 The example of 4 channel real-time record/spot application

Channel ID Encoder

The TW2834 supports the channel ID encoding to detect the picture information in video stream for Y path. The TW2834 has two kinds of channel ID such as User channel ID and Auto channel ID. The User channel ID is used for customized information such as system information and date. The Auto channel ID is employed for automatic identification of picture configuration. The Auto channel ID includes the channel number with cascade stage, analog switch, event, region enable and field/frame mode information. The TW2834 also supports both analog and digital type channel ID during VBI period.

Channel ID Information

The channel ID can be composed of 16 byte User channel ID and 4 byte Auto channel ID. The User channel ID is defined by user and may be used for system information, date and so on. The Auto channel ID is used to identify the current picture configuration. Basically the Auto channel ID has 4 byte data that contains 4 region channel information in one picture such as QUAD split image. That is, each region has 1 byte channel information. The Auto channel ID format is described in the following Table 4.

Table 4 The Auto channel ID information

Bit	Name	Function
7	REG_EN	Region Enable Information
6	EVENT	New Event Information
5	FLDMODE	Sequence Unit (0 : Frame, 1 : Field)
4	ANAPATH	Analog switch information
[3:2]	CASCADE	Cascade Stage Information
[1:0]	VIN_PATH	Video Input Path Number (depending on DEC_PATH_Y)

The REG_EN is used to indicate whether the corresponding 1/4 region is active or blank region. The EVENT is used to denote the update information of each channel in live, strobe or switch operation. Especially the EVENT information is very useful for switch operation or non-realtime application such as pseudo 8ch or dual page mode because each channel can be updated whenever EVENT is detected. The FLDMODE is used to denote the sequence unit such as frame or field. The ANAPATH is used to identify the analog switch information in the channel input path. The ANAPATH information is required for non-realtime application such as pseudo 8ch, dual page or pseudo 8channel MUX application using analog switch. The CASCADE is used to indicate the cascade stage of channel in chip-to-chip cascade application. The VIN_PATH information is used to indicate the video input path of channel.

Four bytes of Auto channel ID can be distinguished by its order. The first byte of Auto channel ID defines the left top region configuration. Likewise the second byte defines the right top, the third byte defines the left bottom and the fourth byte defines the right bottom region configuration in one picture.

The following Fig 43 shows the example of Auto channel ID.

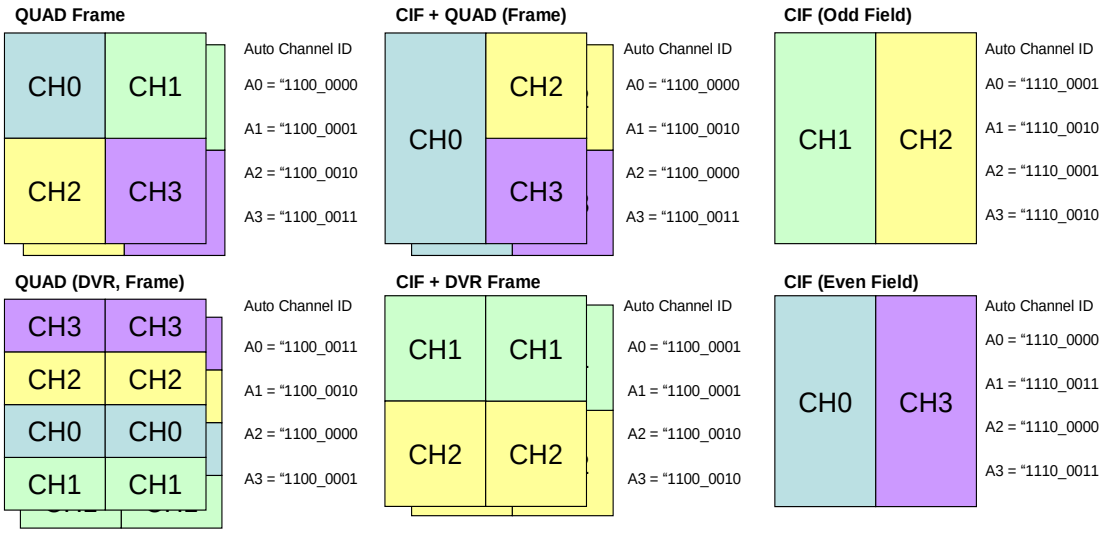


Fig 43 The example of Auto channel ID

These information of encoded channel ID can be readied via AUTO_CHID0 ~ AUTO_CHID3 (1xE0 ~ 1xE3) register and updated at the beginning of each field.

Analog Type Channel ID in VBI

The TW2834 supports the analog type channel ID during VBI period. The analog channel ID has max 8 lines whose line width can be controlled by the VIS_LINE_WIDTH (1xC4) register and each line has 2 bytes channel information. The H/V start position of analog channel ID is controlled by the VIS_LINE_OS (1xC4) register for vertical direction with 1 line unit and VIS_H_OS (1xC2) register for horizontal direction with 2 pixels unit. The pixel width of each bit is controlled by the VIS_PIXEL_WIDTH (1xC3) register with 1 pixel unit. The magnitude of each bit is defined by the VIS_HIGH_VAL (1xC5) and the VIS_LOW_VAL (1xC6) register. The analog channel ID can be enabled independently for each path via the VIS_ENA (1xC1) register. The following Fig 44 shows the illustration of analog channel ID.

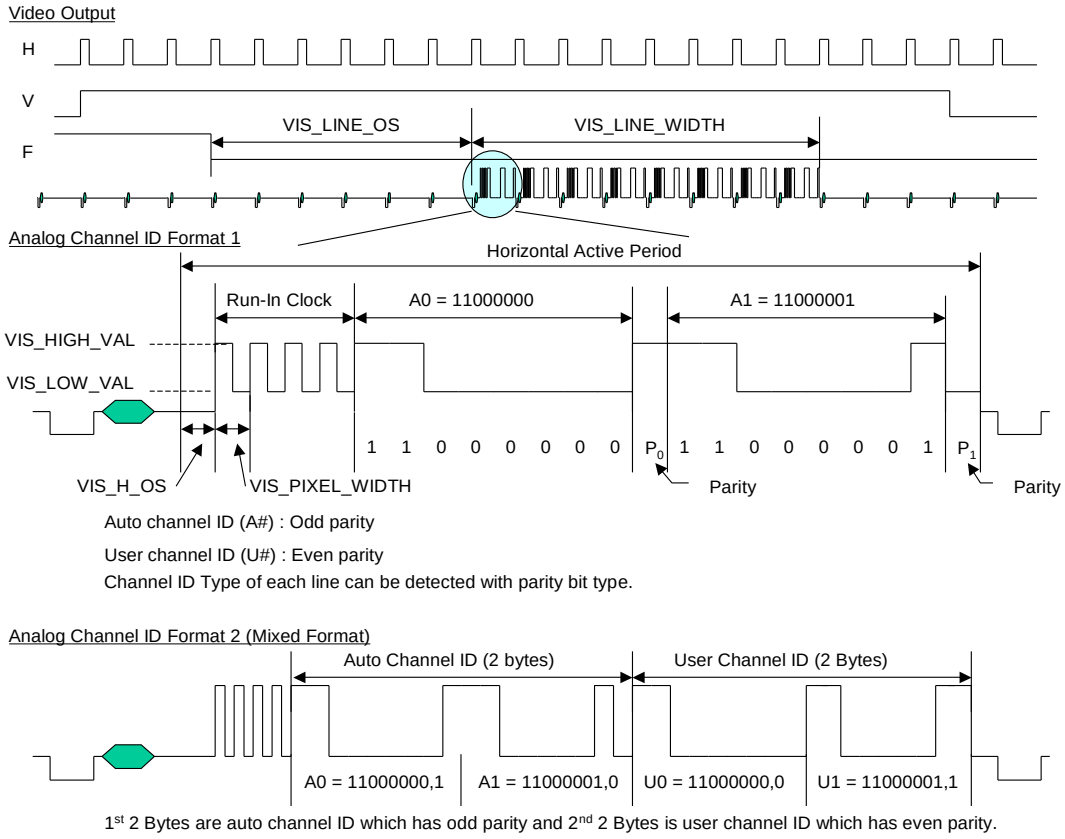


Fig 44 The illustration of analog channel ID

The analog channel ID consists of run-in clock, data and parity bit. The run-in clock insertion is enabled via the VIS_RIC_EN (1xC0) register. The format of analog channel ID is selected via the VIS_MIX_EN (1xC1) register which indicates the analog channel ID format 1 with “0” value and analog channel ID format 2 with “1” value. For analog channel ID format 1, the channel ID has 2 bytes per line and the Auto/User channel ID can be selected via the VIS_SEL (1xC1) register with 2 line unit. For analog channel ID format 2, the channel ID has 4 bytes per line and each line has both 2 byte Auto channel ID and 2 byte User channel ID. Each byte of channel ID has a parity bit and the

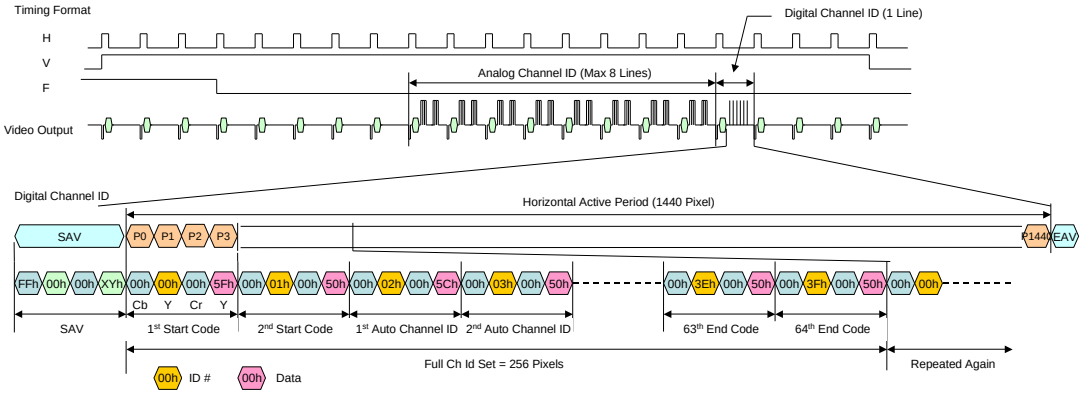
kind of channel ID can be detected with this parity type. That is, the odd parity type is used for Auto channel ID and even parity for User channel ID. Therefore, the parity type should be same for 2 bytes of channel ID.

The TW2834 supports a robust error detection mode via the VIS_EC_EN (1xC1) register. In this case, the Auto channel ID occupies 4 lines that consist of first 2 lines for normal channel ID and next 2 lines for inverted channel ID.

Digital Type Channel ID in VBI

The TW2834 also provides the digital type channel ID during VBI period. It's useful for DSP application because the channel ID can be inserted in just 1 line with special format. The digital channel ID is located after analog channel ID line. The digital channel ID can be enabled via the VIS_CODE_EN (1xC1) register.

The digital channel ID is inserted in Y data in ITU-R BT.656 stream and composed of ID # and channel information. The ID # indicates the index of digital type channel ID including the Start code, Auto/User channel ID and End code. The ID # has 0 ~ 63 index and each 1 byte channel information is divided into 2 bytes with 4 LSB to take "50h" offset against ID # for discrimination. The Start code is located in ID# 0 ~ 1 and the Auto channel ID is situated in ID# 2 ~ 9. The User channel ID is located in ID # 10 ~ 41 and the inverted Auto channel ID is situated in ID # 42 ~ 49 only when VIS_EC_EN = "1". The End code occupies the others. The digital channel ID is repeated more than 5 times during horizontal active period. The following Fig 45 shows the illustration of the digital channel ID.



Digital Channel ID Format

Id #	0	1	2	~	9	10	~	41	42	~	49	50	--	63
Data	5Fh	50h	{0101, A0_MSB}	~	{0101, A3_LSB}	{0101, U0_MSB}	~	{ 0101, U15_LSB}	{0101, !A0_MSB}	~	{0101, !A3_LSB}	{0101, 0000}		
description	Start Code		Auto Channel ID (4 Bytes)			User Channel ID (16 Bytes)			Inverted Auto Channel ID (Option) Or End Code {0101, 0000}			End Code		

Fig 45 The illustration of the digital channel ID in VBI period

Digital Type Channel ID in Channel Boundary

The TW2834 also support the extra type of the digital channel ID in horizontal boundary for each channel. This information can be used for very easy memory management of each channel because this digital channel ID information includes not only the channel information but also line number of picture. The Auto channel ID format is described in the following Table 5.

Table 5 The digital channel ID information in active area

Bit	Name	Function
[15:7]	LINENUM	Active Line number
6	FIELD	Field Polarity Information
5	REG_EN	Region Enable Information
4	ANAPATH	Analog switch information
[3:2]	CASCADE	Cascade Stage Information
[1:0]	VIN_PATH	Video Input Path Number (depending on DEC_PATH_Y)

This digital channel ID is enabled in the horizontal active area by setting “1” to the CH_START (1x55) register. The following Fig 46 shows the digital channel ID in the horizontal active area.

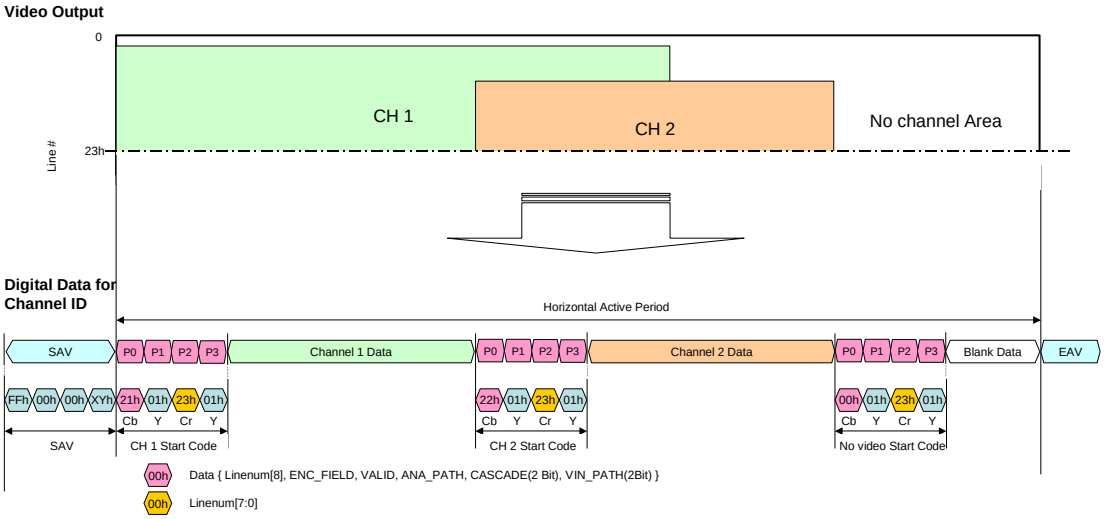


Fig 46 The digital channel ID format in the horizontal active area

Chip-to-Chip Cascade Operation

The TW2834 supports chip-to-chip cascade connection up to 4 chips for 16-channel application and also provides the independent operation for display and record path. That is, the display path can be operated with cascaded connection even though the record path is working in normal operation. Likewise, the cascade connection of record path is limited within 4 chips while the infinite cascade connection of display path can be supported for more than 16-channel application. For the record path in cascade connection, the TW2834 supports the switch operation mode with switching queue for full D1 multiplexing output or the auto strobe operation mode with QUAD_MUX queue for QUAD multiplexing output.

Channel Priority Control

When 2 channels are overlapped in chip-to-chip cascade operation for display path, there is a priority with the following order such as popup attributed channel of master device, popup attributed channel of slaver device, non-popup attributed channel of master device and non-popup attributed channel of slaver device. Using this popup attribute, the TW2834 can implement the channel overlay such as PIP, POP, and full D1 format channel switching in chip-to-chip cascade connection.

For QUAD multiplexing record output in chip-to-chip application, the popup priority of the channel is controlled via the QUAD_MUX queue. The QUAD_MUX operation is enabled via the POS_CTL_EN (1x70) register and the operation mode should be set into strobe operation (FUNC_MODE = “1”). If the POS_CTL_EN is “0”, the channel position is defined via the PIC_POS (1x6D) register and the priority from top to bottom layer is controlled by the popup attribute like the display path. If the POS_CTL_EN is “1”, the channel position and priority is controlled by the pre-defined queue or interrupt.

The TW2834 supports the interrupt triggering via the POS_INTR (1x70), POS_CH (1x73, 1x74) register and also provides the internal or external triggering mode for the QUAD_MUX operation. The triggering mode is selected via the POS_TRIG_MODE (1x70) register such as “0” for external trigger mode and “1” for internal trigger mode.

The QUAD_MUX queue size can be defined by the POS_QUE_SIZE (1x71) register. To change the channel popup sequence in internal queue, the POS_QUE_WR (1x75) register should be set to “1” after defining the queue address with the POS_QUE_ADDR (1x75) register and the channel number with the POS_CH (1x73, 1x74) register. The POS_QUE_WR register will be cleared automatically after updating queue. The QUAD_MUX queue is shared with the normal switching queue so that the maximum queue size for QUAD_MUX is 32 (=128/4) depth.

The QUAD_MUX switching period can be defined via the POS_QUE_PERIOD (1x72) register that has 1 ~ 1024 period range in the internal triggering mode. The switching period unit is controlled via the POS_FLD_MD (1x71) register as field or frame. If switching period unit is frame, switching will occur at the beginning of odd field. The internal field counter can be reset at anytime using the POS_CNT_RST (1x75) register that will be cleared automatically after reset. To reset an internal queue position, the POS_CNT_RST (1x75) register should be set to “1” and will be cleared automatically after set to “1”. The structure of QUAD_MUX switching operation is shown in the following Fig 47.

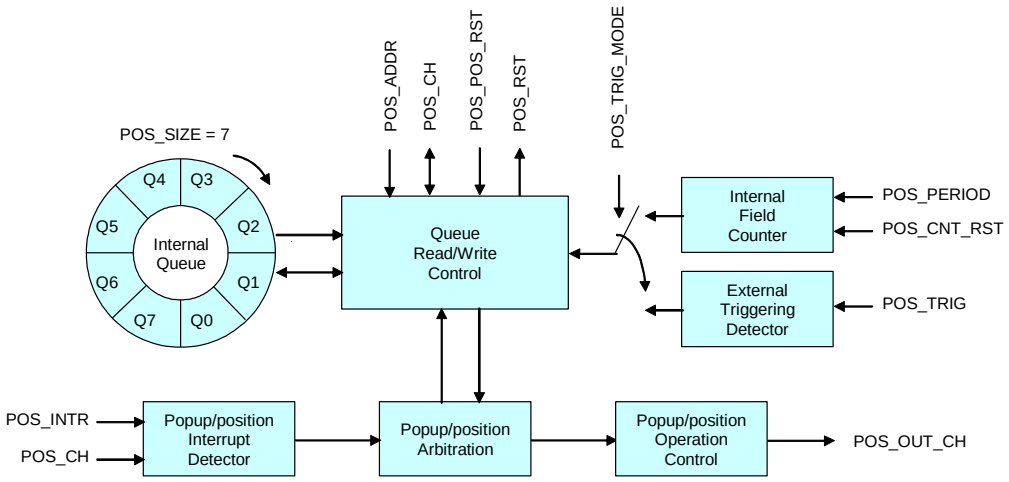


Fig 47 The structure of QUAD_MUX switching operation when POS_SIZE = 7

For QUAD_MUX switching operation by field unit, the TW2834 supports an auto strobe mode for channel to be updated automatically with specific field data. The STRB_FLD (1x04, 1x54) register is used to select specific field data in strobe mode and the STRB_AUTO (1x07, 1x57) register is used to update it automatically.

The QUAD_MUX operation has several limitations. The first is that the channel region should not be overlapped with other channel region via the PIC_SIZE and PIC_POS register. The second is that the channel position and popup property in live or strobe operation mode can be controlled by the popup/position control. But the channel position and priority in switch operation mode is determined by the QUAD_MUX queue. The third is that the POS_CH register in QUAD_MUX queue should be set as the following sequence that is the left top, right top, left bottom and right bottom position in the picture. The POS_CH register includes the cascade stage and channel number information.

120 CIF/Sec Record Mode

For chip-to-chip cascade connection, the MPPDEC and TRIGGER and LINK pin in master chip should be connected to VDOUTX and VSENC and HSENC pin in slaver chips. So the VDOUTX and VSENC and HSENC output pin is only available in master device when cascaded.

The TW2834 has several registers for cascade operation such as the LINK_EN, LINK_NUM and LINK_LAST (1x00) register. For lowest slaver chip, both LINK_LAST_X and LINK_LAST_Y should be set to “1”. To receive the cascade data from slaver chip, either LINK_EN_X or LINK_EN_Y should be set to “1”. To transfer the cascade data properly among the chips, the LINK_NUM should be set properly in accordance with its order. In 120 CIF/Sec record mode, the TW2834 transfers all information of slaver chips to master chip including video data, zoom factors, switching information and 2D box except overlay information such as single box, mouse pointer and OSD information. Therefore, the master chip should be controlled for overlay and the lowest slaver chip should be controlled for the others such as video data, zoom and switching. The information of switching channel can be taken from master chip via the channel ID in video stream or by reading the MUX_OUT_CH (1x08, 1x6E) register. The information of switching channel can also be taken from the lowest slaver chip via the MPPDEC pins. The following Fig 48 illustrates the cascade connection for 120 CIF/Sec record mode.

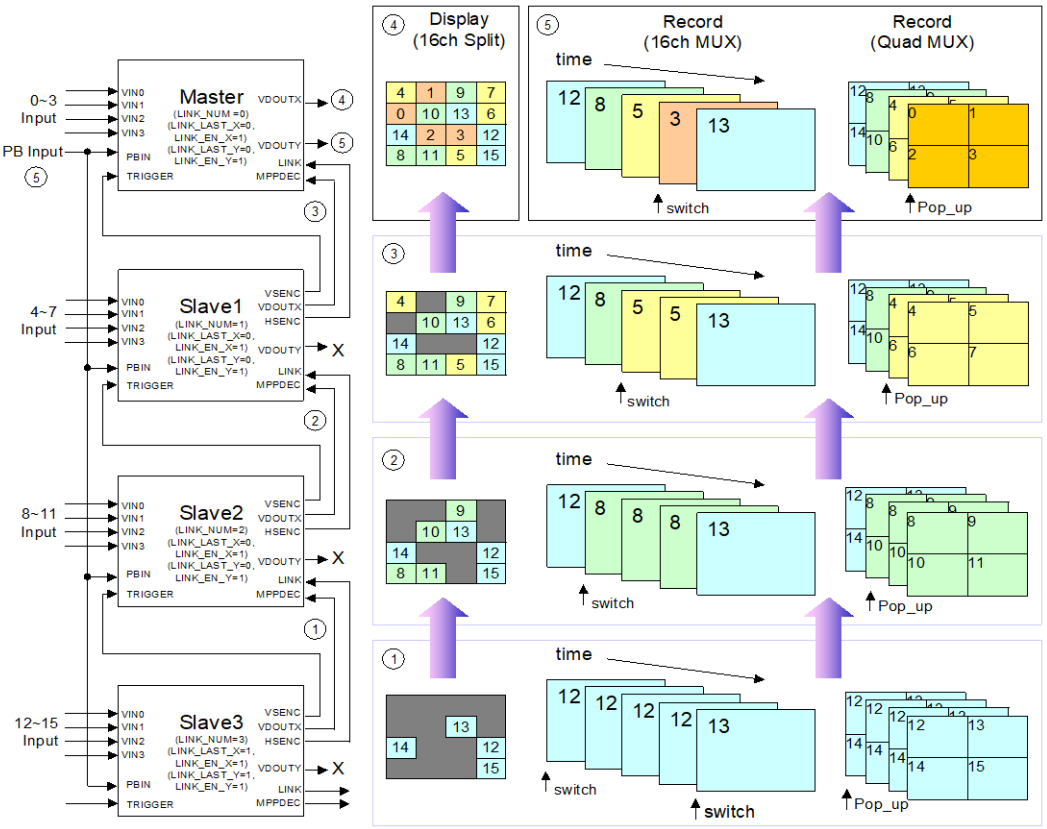


Fig 48 The cascade connection for 120 CIF /sec record mode

240 CIF/Sec Record Mode

The TW2834 supports 240 CIF/Sec record mode in the chip-to-chip cascade connection. In this case, the display path is composed of 4 chip cascade stage, but the record path consists of 2 chip cascade stage. That is, two lowest slaver chips for record path should be set with the LINK_LAST_Y = “1” and the information of switching channel can be taken from two master chips for record path by reading the MUX_OUT_CH (1x6E) register. The following Fig 49 illustrates the cascade connection for 240 CIF/Sec record mode.

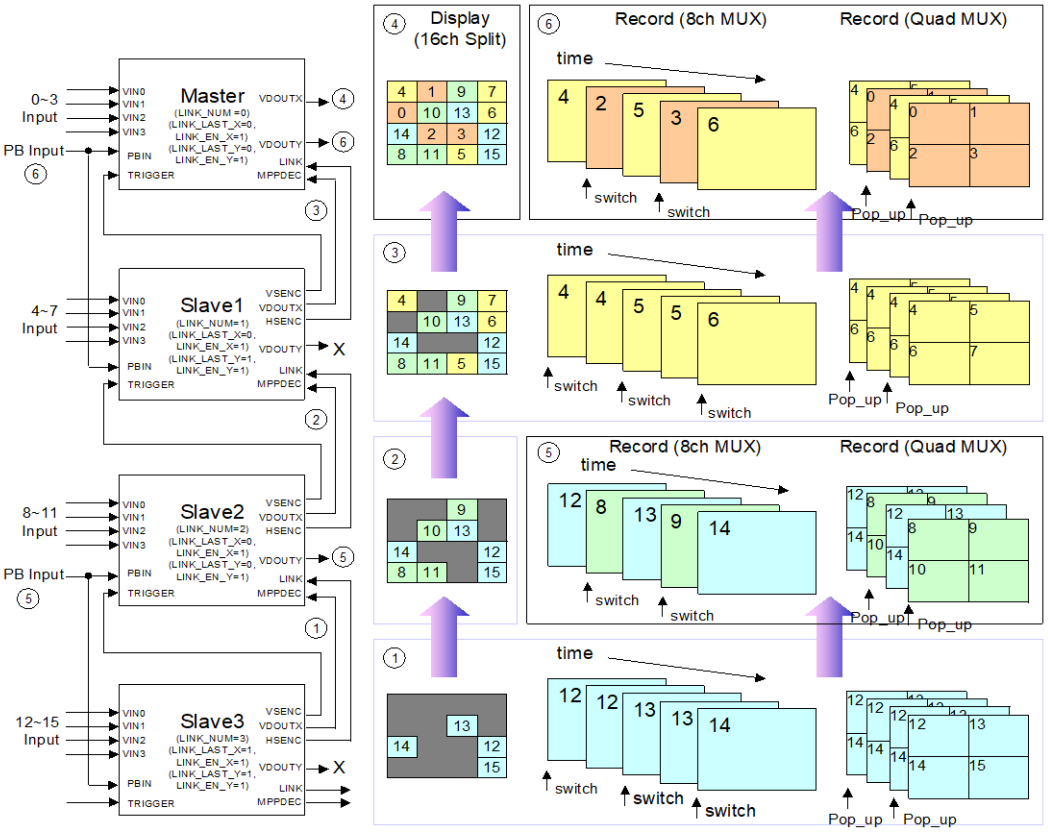


Fig 49 The cascade connection for 240 CIF/sec record mode

480 CIF/Sec Record Mode

The TW2834 also supports 480 CIF/Sec record mode in the chip-to-chip cascade connection. In this case, the display path is composed of 4 chip cascade stage, but the record path has no cascade connection. Even though the record path has no cascade connection, the LINK_NUM should be set properly in accordance with its cascade order for correct channel number in channel ID and the LINK_EN_Y should be set to “0” or the LINK_LAST_Y should be set to “1”. The TW2834 transfers the slaver chip information to master chip such as zoom control and 2D box only for display path and the information of the switching channel for record path can be taken from each chip by reading for the MUX_OUT_CH (1x6E) register. The TW2834 also provides the channel ID encoding for each chip. The following Fig 50 illustrates cascade connection for 480 CIF/Sec record mode.

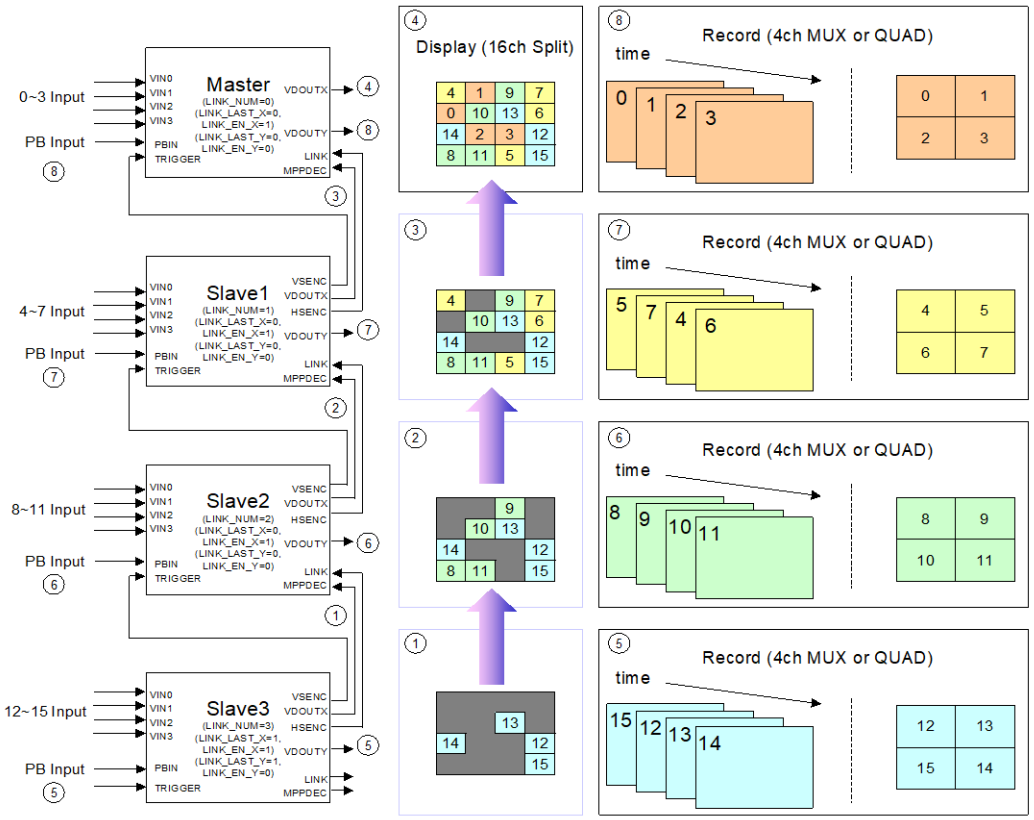


Fig 50 The cascade connection for 480 CIF/Sec record mode

Realtime Record Mode

The TW2834 also supports the real-time record mode in chip-to-chip cascade connection. In this case, the TW2834 use the SDRAM interface pin of record path for real-time record and playback interface. Like 480 CIF/Sec record mode, the record path has no cascade connection but the display path can be extended with more than 4 chip cascade stage (It will be described in the next “Infinite Cascade Mode for Display Path” section, page78). In real-time record mode, the TW2834 does not support the channel ID encoding because there is no need of channel ID insertion for independent full channel recording. The Fig 51 shows the example of real-time record mode.

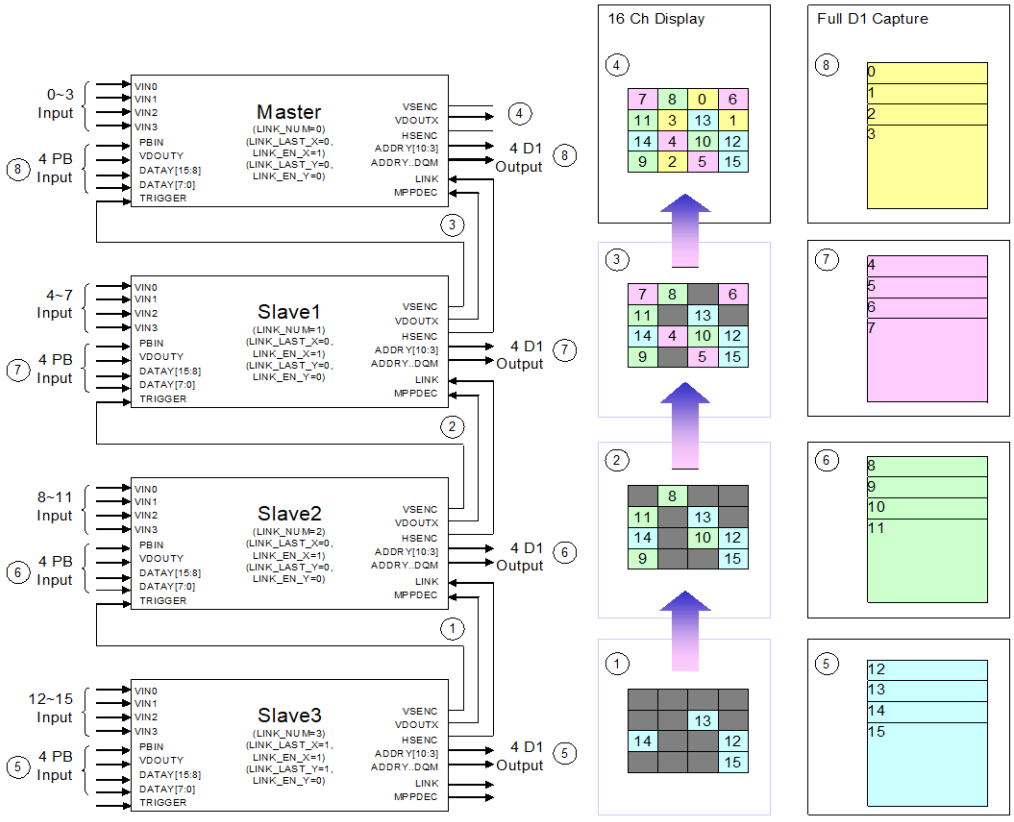


Fig 51 The cascade connection for real-time record mode

Infinite Cascade Mode for Display Path

In normal cascade connection, the master chip has LINK_NUM = “0” and the lowest slaver chip has LINK_NUM = “3”. The master chip can output both display and record path, but the slaver device can output only record path. To implement more than 16 channel application, the TW2834 also provides the infinity cascade connection for display path. That is, the video data and popup information can be transferred to next cascade chip even though the master chip is set with LINK_NUM = “0” and the slaver chip with LINK_NUM = “3” for display path. This mode can be enabled via the T_CASCADE_EN (1xBA) register.

The following Fig 52 illustrates the multiple cascade connection for display path. In this example, the display path in the last master chip can output 32 channel video and the record path can implement “480 CIF/sec” with lower 4 chips and “120 CIF/sec” with upper 4 chips

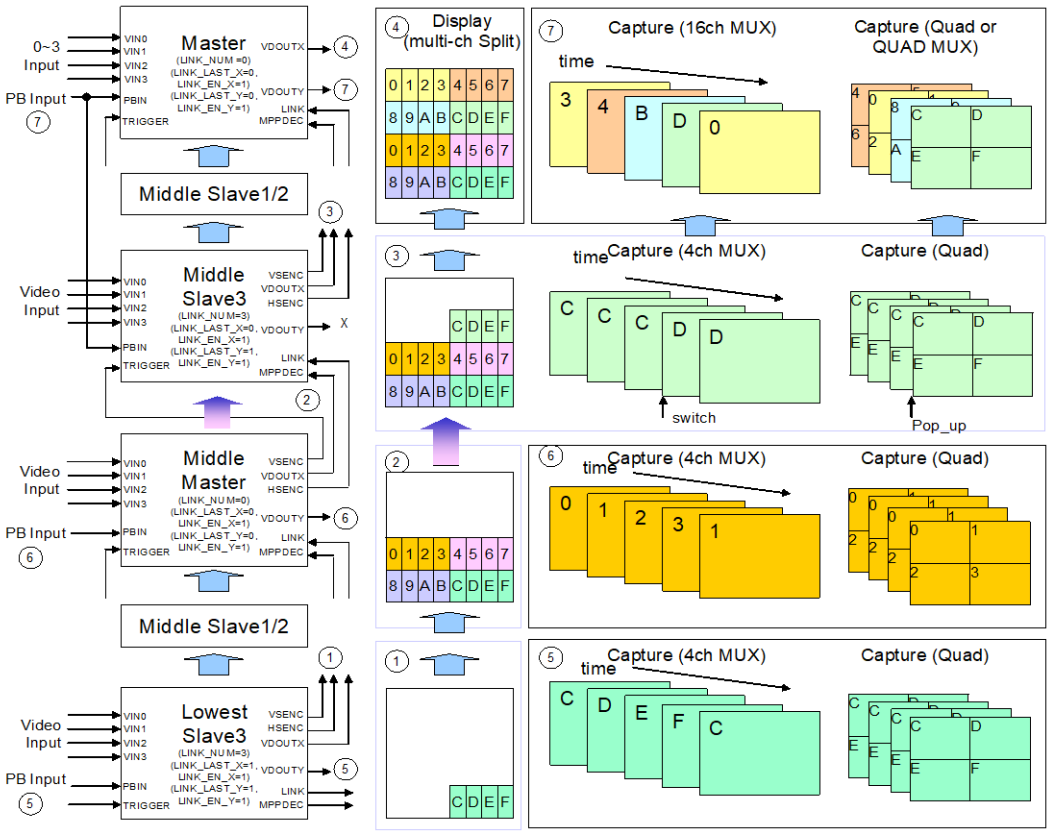


Fig 52 Infinite cascade mode for display path

OSD (On Screen Display) Control

The TW2834 provides various overlay layers such as character/bitmap overlay, box overlay and mouse pointer that can be overlaid on display and record path independently. The following Fig 53 shows the overlay block diagram.

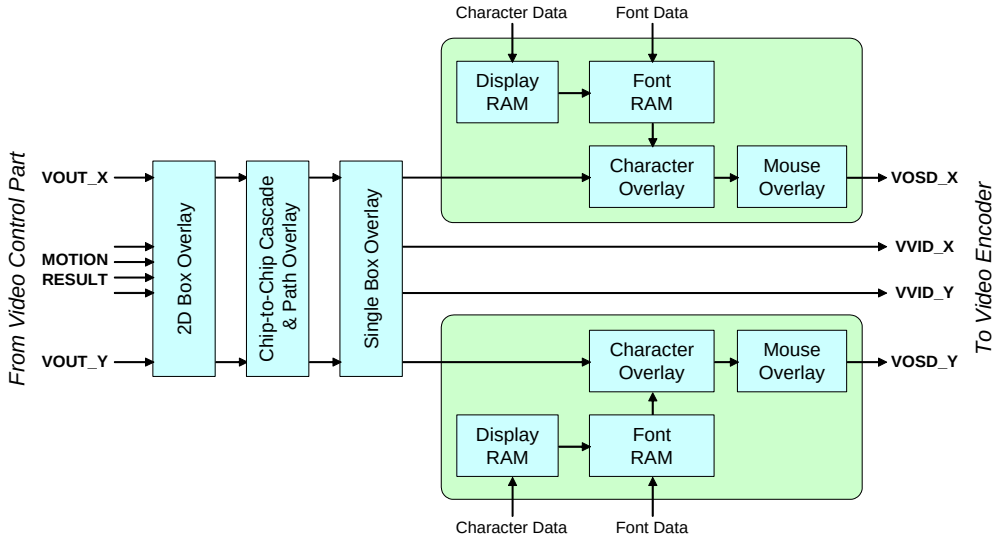


Fig 53 Overlay block diagram

The font data can be downloaded from host and supported up to 128 fonts * 2 fields * 16 pages. The TW2834 supports 16 programmable single boxes and four 2D arrayed boxes that are programmable for size, position and color.

Dual analog video outputs and dual digital video outputs can enable or disable a character and mouse pointer respectively. The overlay priority of OSD layer is shown in Fig 54. The various OSD overlay function is very useful to build GUI interface.

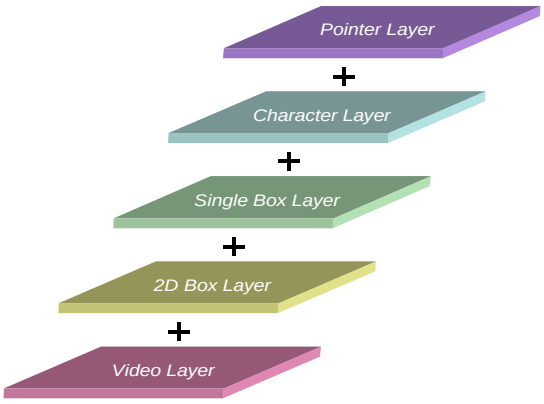


Fig 54 The overlay priority of OSD layer

Character/Bitmap Overlay

The TW2834 has character overlay function for display and record path independently. Each character overlay function block consists of a font RAM, a display RAM and an overlay control block. A font RAM stores font data that can be downloaded from host at anytime. A display RAM stores index, position and attributes of character to be displayed. Character size can be defined as 8~16 dots for 360 pixel rate and 16 ~ 32 dots for 720 pixel rate in the horizontal and 10 ~ 16 lines in the vertical direction.

Bitmap data can also be downloaded from host like character. That is, Bitmap is almost same as character except the control of class 0 color. A character type has a blank for class 0 color in default mode, but a bitmap color has a selectable color for it. However, if CLASS0ENA (1xA0) is set to “1”, even a character type can have a selectable color like bitmap type. In that case, a character type is completely same as a bitmap type. The character and bitmap types can be selected via the FONT_TYPE bit of character attributes in display RAM.

Download Font Group

The TW2834 supports 16 pages * 2 different font groups and each font group can have 128 fonts. A font consists of several dots such as 8 (10, 12, 14, 16 in 360 dot rate and 16, 20, 24, 28, 32 in 720 dot rate) x 10 (12, 14, 16) dots. 1 dot is composed of 2 pixels x 1 video line in 360 dot rate and 1 pixel x 1 video line in 720 dot rate. Each dot has 2 bits to define colors (class 0, class1, class2 and class3). The TW2834 has individual font RAM for display and record path so that the different font data can be stored. The following Fig 55 shows a font RAM structure.

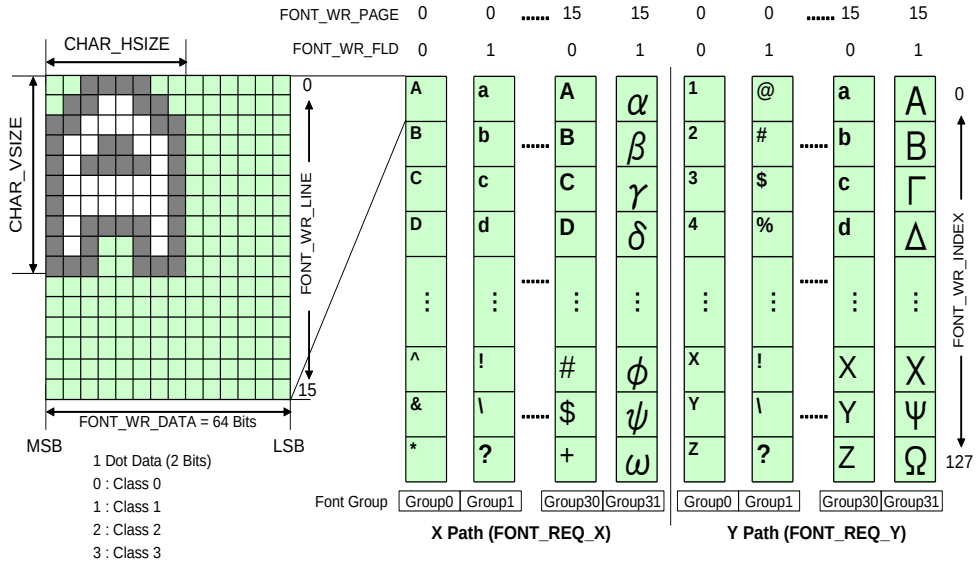


Fig 55 Font RAM structure

The font data can be written to font RAM via FONT_WR_FLD, FONT_WR_TYPE, and FONT_REQ (1x9A), FONT_WR_LINE, FONT_WR_PAGE (1x99), FONT_WR_DATA (1x90 ~ 1x97), FONT_WR_INDEX (1x98) register. By setting “1” to FONT_REQ, font data in the FONT_WR_DATA is transferred to font RAM addressed by FONT_WR_PAGE, FONT_WR _FLD, FONT_WR_LINE, and FONT_WR_INDEX. The FONT_REQ register has status information of transferring in read mode. If the FONT_REQ = “1” in read mode, it means that the TW2834 is busy in transferring font data. In this case, additional request cannot be accepted. The following Fig 56 shows the flow chart of transferring font data to font RAM.

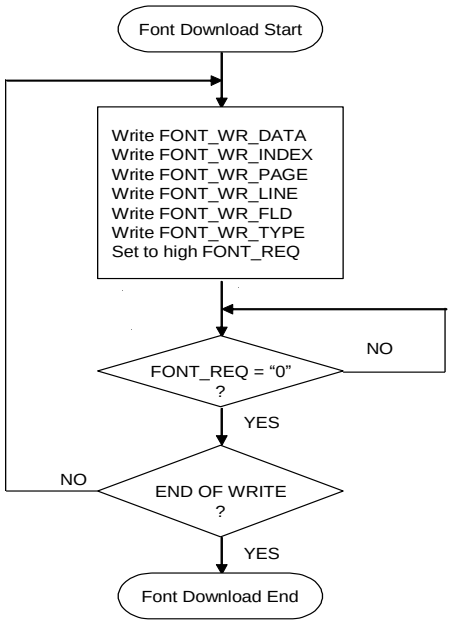


Fig 56 Flow chart of downloading font data

The horizontal resolution of font is defined via the FONT_WR_TYPE such as “0” for 360 dot rate with 8~16 dot size or for 720 dot rate with 16 dot size, “1” for 720 dot rate with 20~24 dot size, and “2” or “3” for 720 dot rate with 28~32 dot size. The FONT_WR_TYPE also determines the available index number of font as 128 font index for “0”, 86 index for “1” and 64 index for “2” or “3”. The TW2834 requires special font data for index 0 to define blank character that will be discussed in following “Write Character and Select Font Group” section (page 82). The max font page size depends on the external SDRAM size in display path and the motion data path via the MD_PATH (2x9E) register (Please refer to “Motion Detection” section, page 32).

Write Character and Select Font Group

The TW2834 has independent 2 display RAM for display and record path. Each character in the display RAM has its own attributes that include mix, blink, class 3 color, type and font index. Additionally, each character line in the display RAM has its own attributes that contain font page, font field, horizontal and vertical size with 12 bit width. That is, the display RAM consists of 45x29 character attributes and 29x12bit character line attributes. Actually the number of displayed characters depends on character size. The horizontal and vertical address of the display RAM represents character position to be displayed. The following Fig 57 shows the structure of the display RAM.

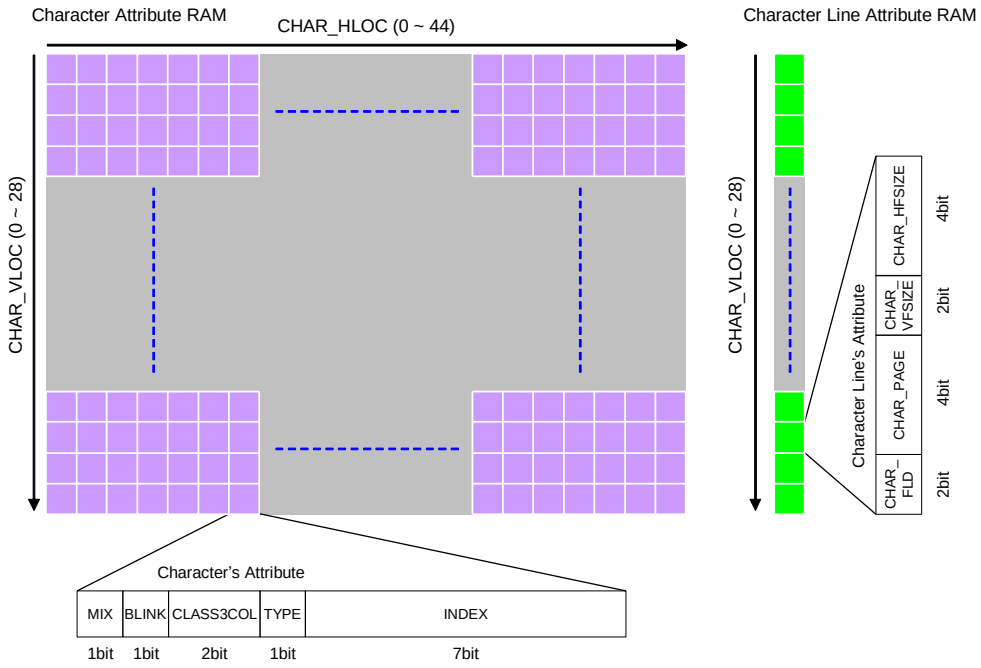


Fig 57 The structure of the display RAM

To define the location of the displayed characters, the CHAR_PATH, CHAR_WR_MODE, CHAR_VLOC (1x9B), and CHAR_HLOC register should be set before writing the character attribute and character line attribute. The CHAR_PATH defines the path (display or record path) and CHAR_VLOC defines the vertical location of the displayed character. The CHAR_WR_MODE defines the write mode of the display RAM such as “0” for writing character attribute, “1” for writing one character line attribute and “2” for writing all character line attributes to reset. In case of CHAR_WR_MODE = “1” or “2”, the character attribute can be written continuously after the character line attributes are written.

The character line attribute consists of 12bit so that 2 bytes are required to write in display RAM. The CHAR_RD_PAGE (1x9C) register selects one of 16 font pages and CHAR_RD_FLD (1x9C) register defines the font field mode. Setting “0” to the CHAR_RD_FLD makes a character overlay function disabled. If the CHAR_FLD is set to “1” or “2”, only one font group is displayed for both odd and even field. But by setting “3” to the CHAR_FLD, the different font groups are displayed on odd and even field respectively so that the character resolution can be enhanced 2 times in vertical direction. The CHAR_VF_SIZE and CHAR_HF_SIZE (1x9C) register defines the vertical and horizontal size of font.

Likewise, the character’s attribute consists of 12bit so that 2 bytes are required to write in display RAM. The TW2834 supports the special procedure for writing to and reading from display RAM as shown in the Fig 58. If the character’s attributes are written continuously in the same path and vertical location, the CHAR_HLOC value increases by 1 automatically.

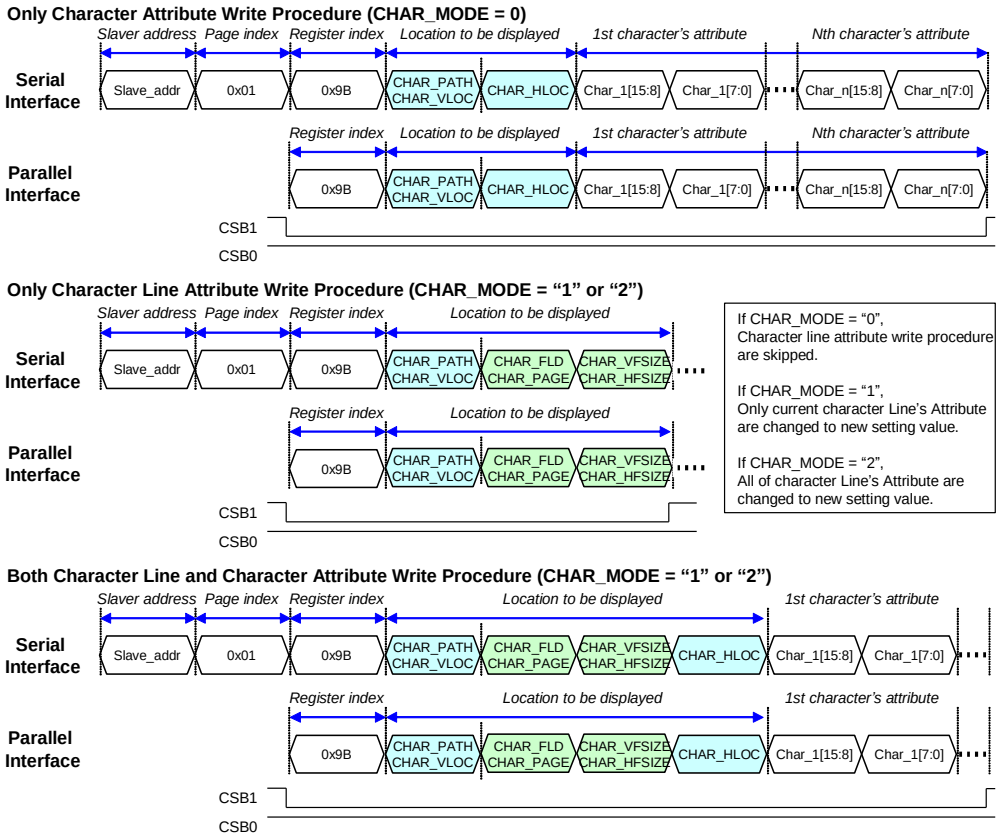


Fig 58 Writing procedure to display RAM

The TW2834 also supports the display RAM clear function that resets all character attributes in display RAM automatically by setting “1” to RAMCLR (1xA0). This function requires that font data in index 0 should be blank character and the CLASS0ENA (1xA0) register should be set to “0”. This RAM clear function takes about 100usec and the RAMCLR register will be cleared by itself after finished.

Character Attribute

Each character has its own attributes in display RAM that includes mix, blink, class 3 color of character, type and font index. The mix attribute makes character mixed with video data and blink attribute makes character blinked with the period defined in the BLK_TIME (1xA0) register. The class 3 color of character takes one of 4 colors defined in the CLASS3COL (1xA7 ~ 1xAA) register. The type attribute defines one of 2 types, character or bitmap type for each character and the font index attribute defines address of font. The mix and blink attributes can be enabled for each class via the CHAR_MIX (1xA5), CHAR_BLK (1xA6) register for each character or bitmap. The alpha blending for OSD is also supported with 25%, 50%, and 75% level via the ALPHA_OSD (1xBA) register.

The TW2834 provides 16 different colors that consist of fixed 12 colors (8 colors from color bar of 75% amplitude 100% saturation, 100% white, 50% gray, 25% gray and 75% blue) and user’s defined 4 colors using the CLUT (1xAE ~ 1xB9) register. The class 0, 1 and 2 color of character will be one of 16 colors via the CLASS0COL, CLASS1COL and CLASS2COL (1xAB ~ 1xAD) registers and are applied to all of characters to be displayed. For class 3 color, 4 colors are predefined via the CLASS3COL (1xA7 ~ 1xAA) register and each character can take one of these 4 colors using character’s attribute as described previously. The different color selection for each character and bitmap can be supported also.

A character type has a blank for class 0 color in default mode, but a bitmap color has a selectable color for it. However, if the CLASS0ENA (1xA0) is set to “1”, a character type can have a selectable color like bitmap type. Likewise, if the B_CLASS0DIS (1xA0) is set to “1”, a bit map type can be changed to character type. However for the display RAM clear function, the CLASS0ENA should be set into “0” because the font data of index 0 should have class 0 with blank character.

The space between characters can be varied horizontally and vertically. The CHAR_HSPC (1xA1, 1xA3) register defines horizontal character space that can be increased by 2 pixel and the CHAR_VSPC (1xA1, 1xA3) register defines vertical character space that can be increased by 1 line unit. Likewise, The TW2834 can define the horizontal and vertical delay for first starting character. The CHAR_HDEL (1xA2, 1xA4) register defines the horizontal delay from left boundary and the CHAR_VDEL (1xA2, 1xA4) register defines the vertical delay from top boundary. Each unit is same as CHAR_HSPC and CHAR_VSPC unit.

Box Overlay

The TW2834 supports two kinds of box overlay such as 16 single boxes and 4 2-dimensional arrayed boxes. The 2-dimensional arrayed box has two modes as table mode and motion display mode.

Single Box

The TW2834 provides 16 single boxes that can be a flat type or 3D type using the BOX_TYPE (2x03) register. The flat type is just simple rectangular box and 3D type looks like 3 dimension view. Each single box has programmable location and size parameters with the BOX_HL (2x11 + 5N, N = 0 ~ 15), BOX_HW (2x12 + 5N, N = 0 ~ 15), BOX_VT (2x13 + 5N, N = 0 ~ 15) and BOX_VW (2x14 + 5N, N = 0 ~ 15) registers. The BOX_HL is the horizontal location of box with 2 pixel unit and the BOX_HW is the horizontal size of box with 4 pixel unit. The BOX_VT is the vertical location of box with 1 line unit and the BOX_VW is the vertical size of box with 2 line unit. There are some definitions about single box as shown in the Fig 59.

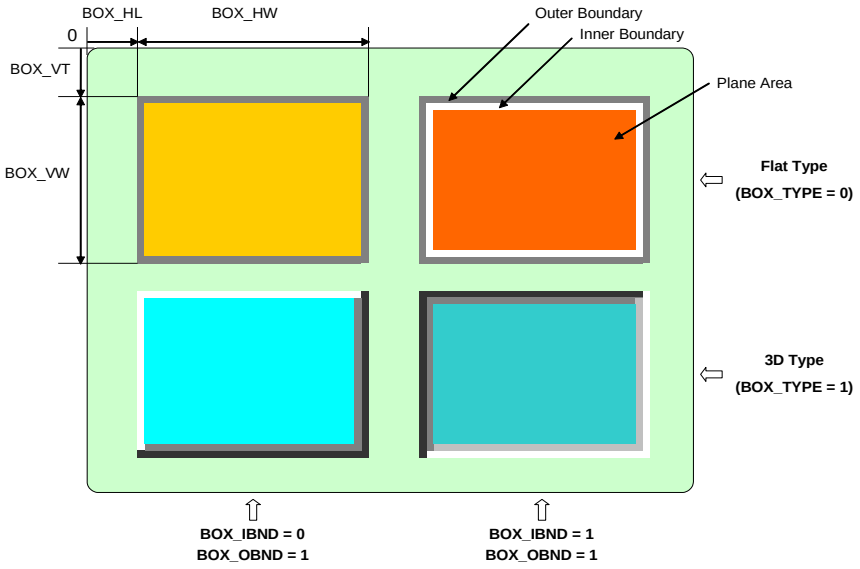


Fig 59 The structure of Single box

The BOX_PLNEN (2x10 + 5N, N = 0 ~ 15) register enables each plane color and its color is defined by the BOX_PLNCOL (2x05 ~ 2x0C) register as described in character color section. Actually the TW2834 provides total 16 different colors that consist of fixed 12 colors (8 colors from color bar and 100%, 50%, 25% gray and 75% blue) and user's defined 4 colors using CLUT (1xAE ~ 1xB9) register. This color table is used in common with plane color for single box and character color. For the box plane, luminance level can be controlled through the BOX_IBND (2x10 + 5N, N = 0 ~ 15) register when the BOX_EMP (2x03) register = '1". The BOX_IBND = "1" makes luminance level of plane down by 20IRE and "0" makes up by 20IRE. The each box plane can be mixed with video data via the BOX_PLNMIX (2x10 + 5N, N = 0~15) register. The alpha blending level is controlled as 25%, 50%, and 75% via the ALPHA_BOX (2x03) register. The BOX_EN (2x10 + 5N, N = 0~15) register determines the boxes to be displayed for each path.

The color of box boundary is defined by the BOX_TYPE (2x03), BOX_OBND (2x10 + 5N, N = 0~15), BOX_IBND (2x10 + 5N, N = 0~15) and BOX_BNDCOL (2x04) registers as described in the Table 6.

Table 6 The Color of Single Box Boundary

Boundary		Control Register			Color Description	
		BOX_TYPE	BOX_OBND	BOX_IBND	Register	Color
Outer		0 (Flat Type)	0	X	BOX_ BNDCOL [7:4]	Outer Boundary off
			1	X		0~10 : 0, 10, 20, 30, 40, 50, 60, 70, 80, 90, 100 IRE Gray 11~14 : User defined Color (1xAE ~ 1xB9). 15 : Same as plane color with 20IRE down of luminance
Inner			X	0	BOX_ BNDCOL [3:0]	Inner Boundary off
			X	1		0~10 : 0, 10, 20, 30, 40, 50, 60, 70, 80, 90, 100 IRE Gray 11~14 : User defined Color (1xAE ~ 1xB9). 15 : Same as plane color with 20IRE up of luminance
Outer	Left & Top	1 (3D Type)	0	X	BOX_ BNDCOL [7:6]	Boundary off
			1	0		0~3 : 90, 80, 70, 60 IRE Gray
			1	1		0~3 : 0, 10, 20, 30 IRE Gray
	Right & Bottom		0	X	BOX_ BNDCOL [5:4]	Boundary off
			1	0		0~3 : 0, 10, 20, 30 IRE Gray
			1	1		0~3 : 90, 80, 70, 60 IRE Gray
Inner	Left & Top		0	X	BOX_ BNDCOL [3:2]	Boundary off
			1	0		Same as inner area
			1	1		0~3 : 30, 40, 50, 60 IRE Gray
	Right & Bottom		0	X	BOX_ BNDCOL [1:0]	Boundary off
			1	0		0~3 : 30, 40, 50, 60 IRE Gray
			1	1		0~3 : 70, 60, 50, 40 IRE Gray

In case that several boxes have same region, there will be a conflict of what to display for that region. Generally the TW2834 defines that the box 0 has priority over box 15. So if a conflict happens between more than 2 boxes, the box 0 will be displayed first as top layer and box 1 to box 15 are hidden beneath that are not supported for pop-up attribute unlike channel display.

2Dimensional Arrayed Box

The TW2834 supports 4 2D arrayed boxes that have programmable cell size up to 16x16. The 2D arrayed box is useful to make a table menu or display motion detection result for analog input. The 2D arrayed box mode is selected via the 2DBOX_MODE (2x60, 2x68, 2x70, 2x78) register. Each 2D arrayed box can be displayed on each path by the 2DBOX_EN (2x60, 2x68, 2x70, 2x78) register.

The 2DBOX_HNUM and 2DBOX_VNUM (2x66, 2x6E, 2x76, 2x7E) registers define the number of row and column cells. For each 2D arrayed box, the horizontal location of left top for 2D box is defined by the 2DBOX_HL (2x62, 2x6A, 2x72, 2x7A) register with 2 pixel step and the vertical location of left-top is defined by the 2DBOX_VT (2x64, 2x6C, 2x74, 2x7C) register with 1 line step. The vertical size of each cell is defined by the 2DBOX_VW (2x65, 2x6D, 2x75, 2x7D) registers with 1 line step and the horizontal size is defined by the 2DBOX_HW (2x63, 2x6B, 2x73, 2x7B) registers with 2 pixel step. So the whole size of 2D arrayed box is same as the sum of cells in row and column. The following Fig 60 shows the 2D arrayed box of table mode.

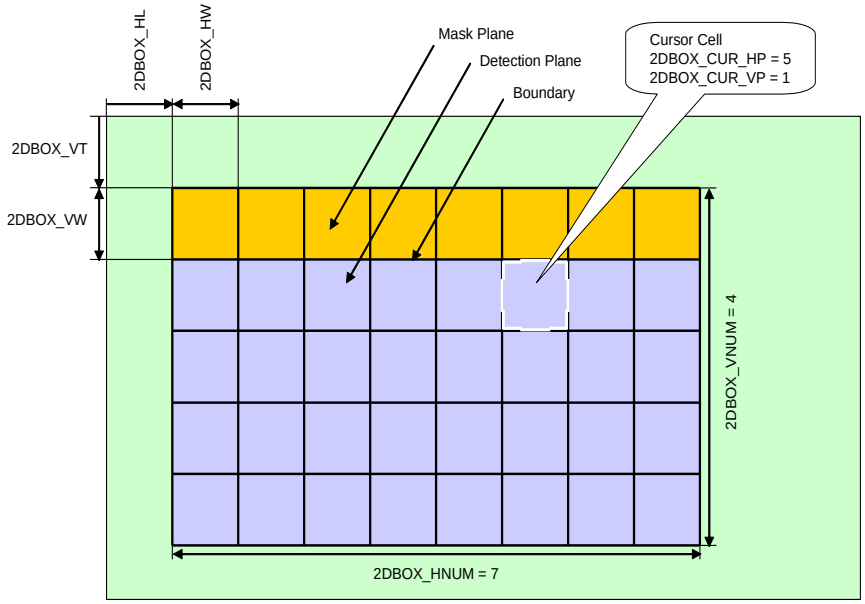


Fig 60 2D arrayed box in table mode

The boundary of 2D arrayed box can be enabled by the 2DBOX_BNDEN (2x60, 2x68, 2x70, 2x78) register and its color is controlled via the 2DBOX_BNDCOL (2x61, 2x69, 2x71, 2x79) register which selects one of 4 colors such as 0% black, 25% gray, 50% gray and 75% white.

The plane of 2D arrayed box is separated into mask plane and detection plane. The mask plane represents the cell defined by MD_MASK (2x86 ~ 2x9D, 2xA6 ~ 2xBD, 2xC6 ~ 2xDD, 2xE6 ~ 2xFD) register. The detection plane represents the cell excluding the mask cells among whole cells.

The mask plane of 2D arrayed box is enabled by the 2DBOX_MSKEN (2x60, 2x68, 2x70, 2x78) register and the detection plane is enabled by the 2DBOX_DETEN (2x60, 2x68, 2x70, 2x78) register.

The color of mask plane can be controlled by the 2DBOX_PLNCOL (2x61, 2x69, 2x71, 2x79) register, which selects one of 16 colors as described in character color and plane color of single box. For DETCOL_EN (2x9E) = “0”, the color of detection plane is same as the mask plane color, but for DETCOL_EN = “1”, its color is controlled by the DETCOL_SEL (2x9E) register. The plane can be mixed with video data by the 2DBOX_MIX (2x60, 2x68, 2x70, 2x78) register. The alpha blending level is controlled as 25%, 50%, and 75% via the ALPHA_2DBOX (2x03) register.

Specially, the TW2834 provides the function to indicate cursor cell inside 2D arrayed box. The cursor cell is enabled by the 2DBOX_CUREN (2x60, 2x68, 2x70, 2x78) register and the displayed location is defined by the 2DBOX_CURHP and 2DBOX_CURVP (2x67, 2x6F, 2x77, 2x7F) registers. Its color is a reverse color of cell boundary. It is useful function to control motion mask region.

The 2D arrayed box can be also used to display motion information. When the 2D arrayed box is working in motion display mode, the mask plane of 2D arrayed box shows the mask information according to the MD_MASK registers automatically. For the motion display mode, an additional narrow boundary of each cell is provided to display motion detection via the 2DBOX_DETEN register and its color is a reverse cell boundary color. Even in the horizontal / vertical mirroring mode, the video data and motion detection result can be matched via the 2DBOX_HINV and 2DBOX_VINV (2x81, 2xA1, 2xC1, 2xE1) registers.

The TW2834 has 4 2D arrayed boxes so that 4 video channels can have its own 2D arrayed box for motion display mode. To overlay mask information and motion result on video data properly, the scaling ratio of video should be matched with 2D arrayed box size.

The following Fig 61 shows 2D arrayed box of motion display mode.

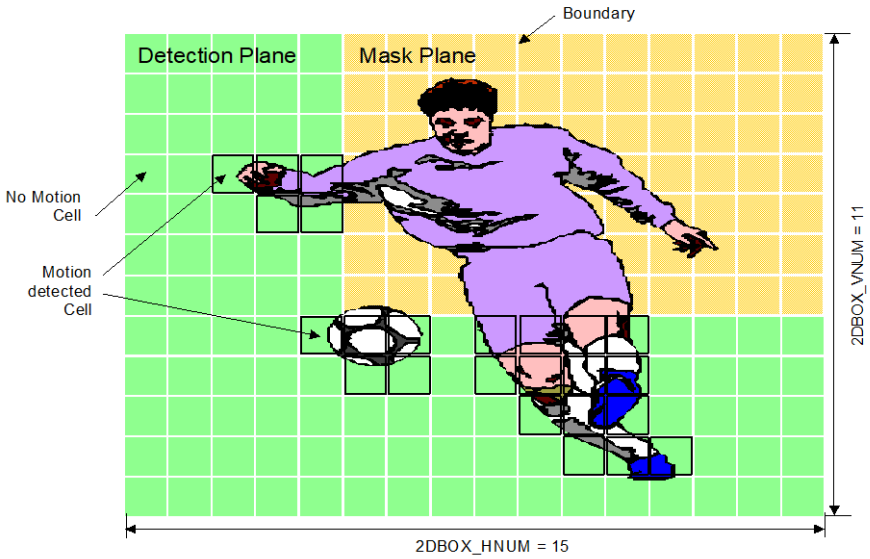


Fig 61 2D arrayed box in motion display mode

In case those several 2D arrayed boxes have same region, there will be a conflict of what to display for that region. Generally the TW2834 defines that 2D arrayed box 0 has priority over other 2D arrayed box. So if a conflict happens between more than 2 2D arrayed boxes, 2D arrayed box 0 will be displayed first as top layer and 2D arrayed box 1, box 2, and box 3 are hidden beneath that are not supported for pop-up attribute like channel attribute.

Mouse Pointer

The TW2834 supports the mouse pointer that has attributes such as pointer enable, pointer location, blink and sub-layer enable. The mouse pointer can be overlaid on both display and record path independently.

The mouse pointer is located in the full screen according to the CUR_HP (2x01) register with 2 pixel step and CUR_VP (2x02) register with 1 line step. Two kinds of mouse pointer are provided through the CUR_TYPE (2x00) register. The CUR_SUB (2x00) register determines a pointer inside area to be filled with 100% white or to be transparent and CUR_BLINK (2x00) register controls a blink function of mouse. Actually the CUR_ON (2x00) register enables or disables mouse pointer for display and record path independently. The following Fig 62 describes the parameters of mouse pointer.

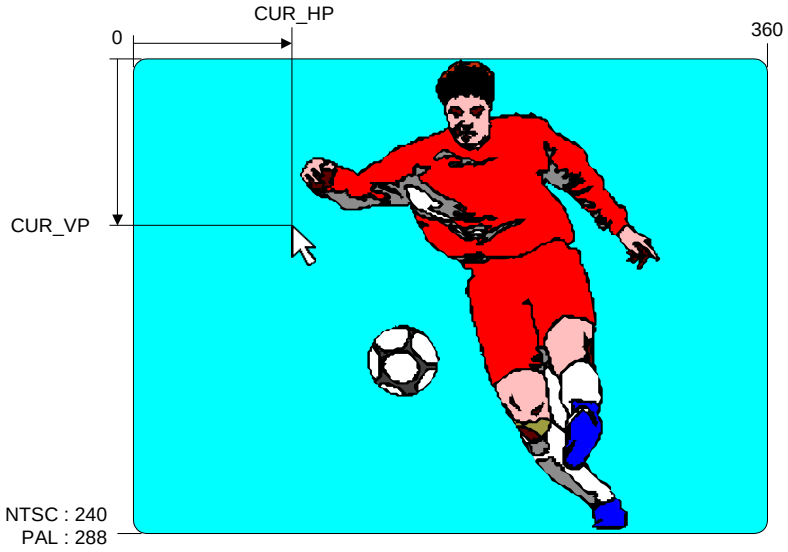


Fig 62 The parameters of mouse pointer

Video Output

The TW2834 supports dual digital video outputs with ITU-R BT.656 format and 2 analog video outputs with built-in video encoder at the same time. Dual video controllers described above generate 4 kinds of video data, the display path video data with or without OSD and the record path video data with or without the OSD. The CCIR_IN (1x80) register selects one of 4 video data for the digital video output and ENC_IN (1x80) register selects one of 4 video data for the analog video output as shown in Fig 63.

The TW2834 supports all NTSC and PAL standards for analog output, which can be composite, or S-video video for both display and record path. All outputs can be operated as master mode to generate timing signal internally or slave mode to be synchronized with external timing.

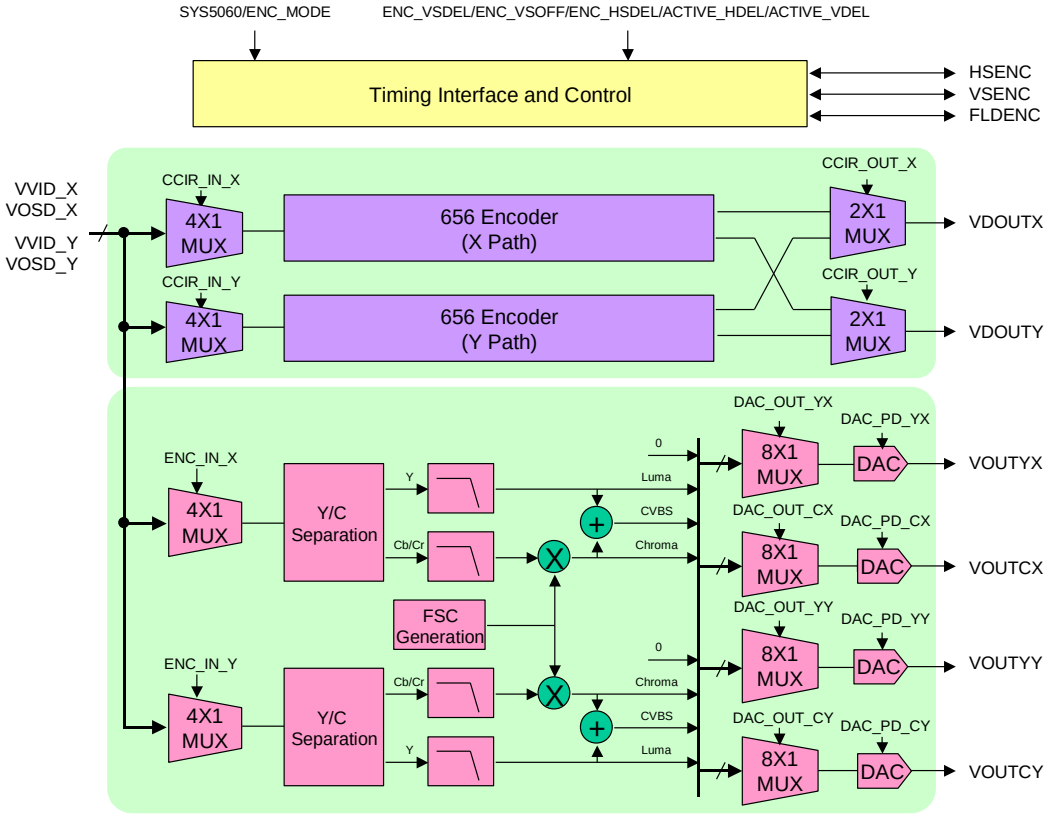


Fig 63 Video output selection

Analog Video Output

The TW2834 supports analog video output using built-in video encoder, which generates composite or S-video with 10 bit dual DAC for both display and record path. The incoming digital video are adjusted for gain and offset according to NTSC or PAL standard. Both the luminance and chrominance are band-limited and interpolated to 27MHz sampling rate for digital to analog conversion. The NTSC output can be selected to include a 7.5 IRE pedestal. The TW2834 also provides internal test color bar generation.

Output Standard Selection

The TW2834 supports various video standard outputs via the SYS5060 (1x00) and ENC_FSC, ENC_PHALT, ENC_PED (1x89) registers as described in the following Table 7.

Table 7 Analog output video standards

Format	Specification			Register			
	Line/Fv (Hz)	Fh (KHz)	Fsc (MHz)	SYS5060	ENC_ FSC	ENC_PHALT	ENC_PED
NTSC-M	525/59.94	15.734	3.579545	0	0	0	1
NTSC-J							0
NTSC-4.43	525/59.94	15.734	4.43361875	0	1	0	1
NTSC-N	625/50	15.625	3.579545	1	0	0	0
PAL-BDGHI	625/50	15.625	4.43361875	1	1	1	0
PAL-N							1
PAL-M	525/59.94	15.734	3.57561149	0	2	1	0
PAL-NC	625/50	15.625	3.58205625	1	3	1	0
PAL-60	525/59.94	15.734	4.43361875	0	1	1	0

If the ENC_ALTRST (1x89) register is set to “1”, phase alternation can be reset every 8 field so that phase alternation keeps same phase every 8 field.

Luminance Filter

The band of luminance signal can be selected as shown in the following Fig 64.

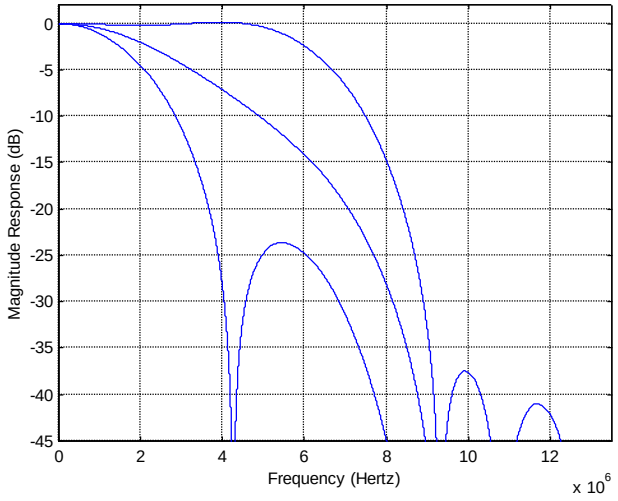


Fig 64 Characteristics of luminance filter

Chrominance Filter

The band of chrominance signal can be selected as shown in the following Fig 65.

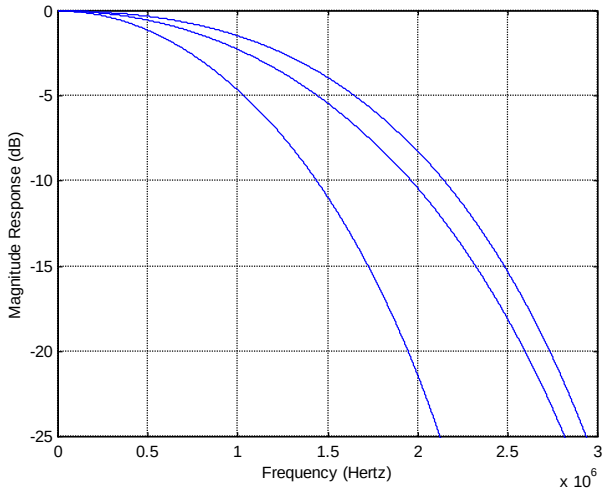


Fig 65 Characteristics of chrominance Filter

Digital-to-Analog Converter

Digital video data from video encoder is converted to analog video signal by DAC (Digital to Analog Converter). The analog video signal format can be selected for each DAC independently via the DAC_OUT (1x81, 1x82) register. For DAC_OUT = “0”, no output is selected and for DAC_OUT = “1”,

CVBS output is selected. If the DAC_OUT is “2”, luminance output is chosen and if the DAC_OUT is “3”, chrominance output is chosen. Each DAC can be disabled independently to save power by the DAC_PD (1x81, 1x82) register.

A simple reconstruction filter is required externally to reject noise as shown in the Fig 66.

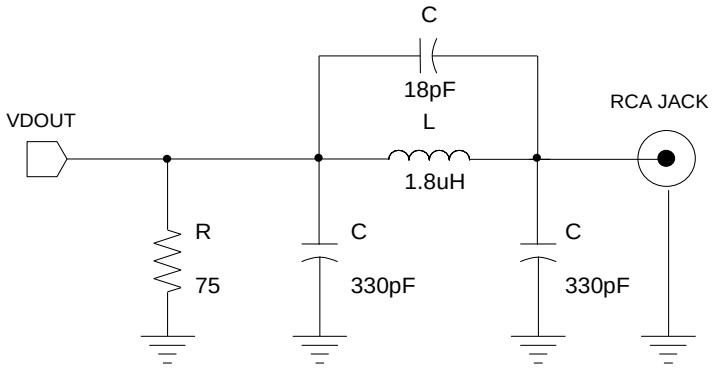


Fig 66 Example of reconstruction filter

Digital Video Output

The digital output data of ITU-R BT.656 format is synchronized with CLK27ENC pin, which is 27MHz for single output or 54MHz for dual output. Each digital data of display and record path can be output through VDOUTX and VDOUTY pin respectively on single output mode. For the dual output mode, both display and record path output can come out through only one VDOUTX or VDOUTY. The level of active video of ITU-R BT.656 can be limited to 1 ~ 254 level by the CCIR_LMT (1x84) register. For digital channel ID mode, the CCIR_LMT should be set to low.

Table 8 ITU-R BT.656 SAV and EAV code sequence

	Line		Condition			FVH			SAV/EAV Code Sequence			
	From	To	Field	Vertical	Horizontal	F	V	H	First	Second	Third	Fourth
60Hz (525Lines)	523 (1[*1])	3	EVEN	Blank	EAV	1	1	1	0xFF	0x00	0x00	0xF1
					SAV			0				0xEC
	4	19	ODD	Blank	EAV	0	1	1				0xB6
					SAV			0				0xAB
	20	259 (263[*1])	ODD	Active	EAV	0	0	1				0x9D
					SAV			0				0x80
	260 (264[*1])	265	ODD	Blank	EAV	0	1	1				0xB6
					SAV			0				0xAB
	266	282	EVEN	Blank	EAV	1	1	1				0xF1
					SAV			0				0xEC
	283	522 (525[*1])	EVEN	Active	EAV	1	0	1				0xDA
					SAV			0				0xC7
50Hz (625Lines)	1	22	ODD	Blank	EAV	0	1	1	0xFF	0x00	0x00	0xB6
					SAV			0				0xAB
	23	310	ODD	Active	EAV	0	0	1				0x9D
					SAV			0				0x80
	311	312	ODD	Blank	EAV	0	1	1				0xB6
					SAV			0				0xAB
	313	335	EVEN	Blank	EAV	1	1	1				0xF1
					SAV			0				0xEC
	336	623	EVEN	Active	EAV	1	0	1				0xDA
					SAV			0				0xC7
	624	625	EVEN	Blank	EAV	1	1	1				0xF1
					SAV			0				0xEC

Note 1. The number of ( ) is ITU-R BT. 656 standard. The TW2834 also supports this standard by CCIR_STD register (1x88 Bit[6]).

The TW2834 also supports ITU-R BT.601 interface through the VDOUTX pin for Y data and VDOUTY pin for C data.

Single Output Mode

For the single output mode, each digital output data in display and record path can be output at 27MHz ITU-R BT 656 interface through VDOUTX and VDOUTY pin that are synchronized with CLK27ENCX and CLK27ENCY. The output data is selected by the CCIR_OUT (1x83) register which selects the display path data for “0” and record path data for “1”. The timing diagram of single output mode for ITU-R BT.656 interface is shown in the following Fig 67.

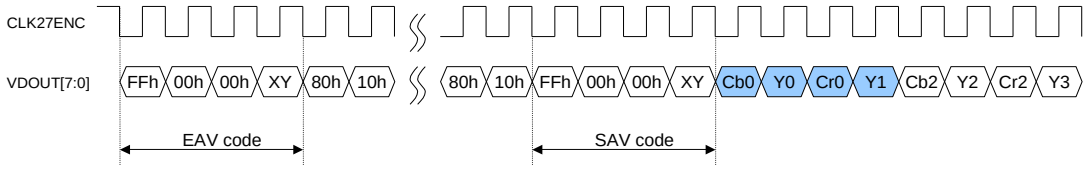


Fig 67 Timing diagram of single output mode for 656 Interface

The TW2834 also supports 13.5MHz ITU-R BT 601 interface through VDOUTX and VDOUTY pin via the CCIR_601 (1x83) register. The output data is selected via the CCIR_OUT register which selects the display path data for “0” and record path data for “1”. The timing diagram of single output mode for ITU-R BT 601 interface is shown in the following Fig 68.

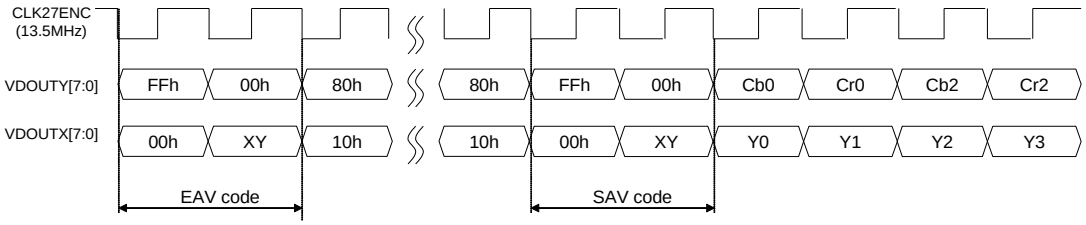


Fig 68 Timing diagram of single output mode for 601 Interface

The output is synchronized with CLK27ENCX and CLK27ENCY pins whose phase and frequency can be controlled by the ECLK_FR_X, ECLK_FR_Y, ECLK_PH_X and ECLK_PH_Y (1x8D) registers.

Dual Output Mode

The TW2834 also supports dual output mode that is time-multiplexed with display and record path data at 54MHz clock rate. The sequence is related with the CCIR_OUT (1x83) register that the display path data precedes the record path for CCIR_OUT = “2” and the record path data precedes the display path for CCIR_OUT = “3”.

The timing diagram of dual output mode for ITU-R BT 656 interface is illustrated in the Fig 69. The dual output mode is useful to reduce number of pins for interface with other devices.

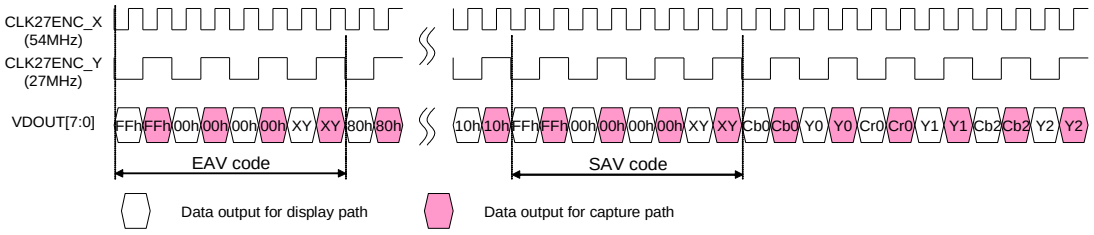


Fig 69 Timing diagram of dual output mode for 656 Interface

The TW2834 also supports dual output mode with 13.5MHz ITU-R BT 601 interface that is timing multiplexed to 27MHz through VDOUTX and VDOUTY pin via the CCIR_601 (1x83) register. The sequence is determined by the CCIR_OUT register like 54MHz ITU-R BT.656 interface. The timing diagram of single output mode for ITU-R BT 601 interface is shown in the following Fig 70.

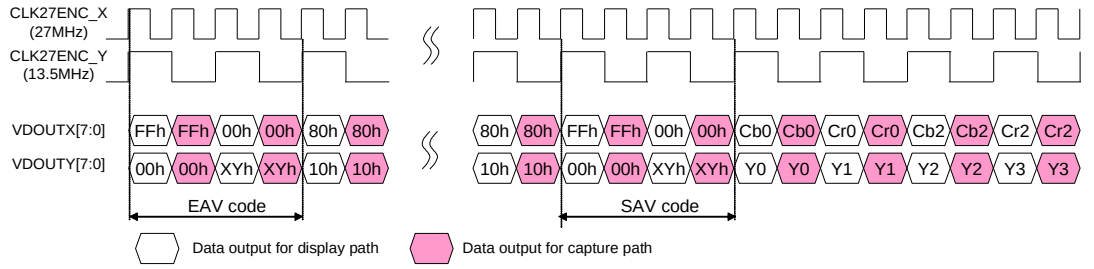


Fig 70 Timing diagram of dual output mode for 601 Interface

The output is synchronized with CLK27ENCX and CLK27ENCY pins whose polarity and frequency can be controlled by the ECLK_FR_X, ECLK_FR_Y, ECLK_PH_X and ECLK_PH_Y registers.

Timing Interface and Control

The TW2834 can be operated in master or slave mode via the ENC_MODE (1x84) register. In master mode, the TW2834 can generate all of timing signals internally while the TW2834 receives all of timing signals from external device in slaver mode. The polarity of horizontal, vertical sync and field flag can be controlled by the ENC_HSPOL, ENC_VSPOL and ENC_FLDPOL (1x84) registers respectively for both master and slave mode. In slave mode, the TW2834 can detect field polarity from vertical sync and horizontal sync via the ENC_FLD (1x84) register or can detect vertical sync from the field flag via the ENC_VS (1x84) register.

The TW2834 provides or receives the timing signal through the HSENC, VSENC and FLDENC pins. To adjust the timing of those pins, the TW2834 has the ENC_HSDEL (1x86), ENC_VSDEL and ENC_VSOFF (1x85) registers which control only the related signal timing regardless of analog and digital video output. Likewise, by controlling the ACTIVE_VDEL (1x87) and ACTIVE_HDEL (1x88) registers, only active video period can be shifted on horizontal and vertical direction independently. The shift of active video period produces the cropped video image because the timing signal is not changed even though active period is moved. So this feature is restricted to adjust video location in monitor for example. The active video data period of analog video output is same as digital video output so that the video timing of both outputs can be controlled in common. The detailed timing diagram is illustrated in the following Fig 71.

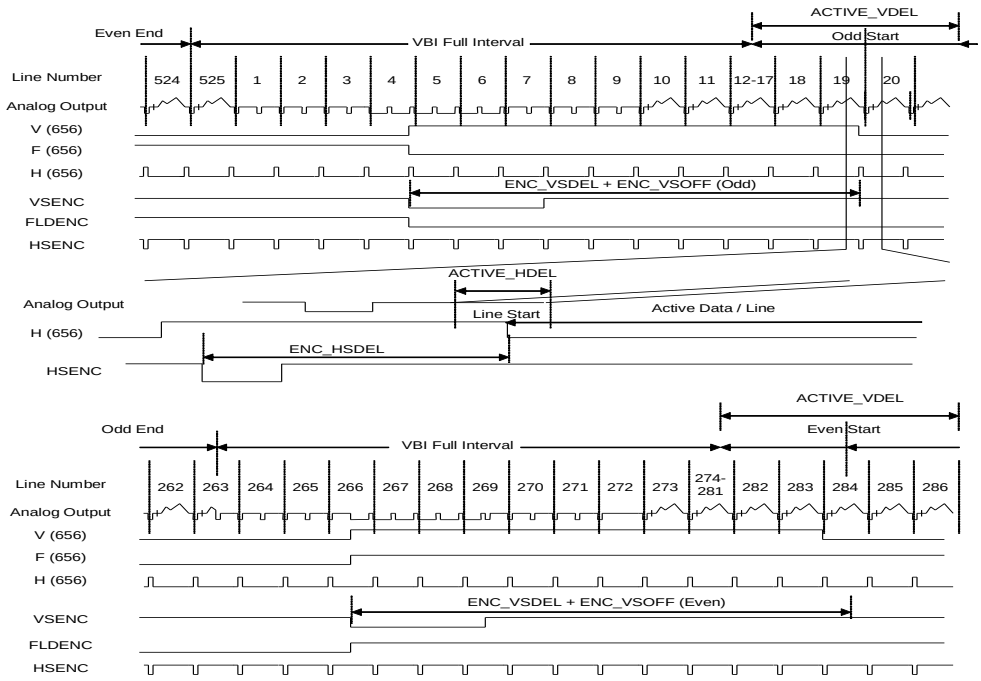


Fig 71 Horizontal and vertical timing control

Host Interface

The TW2834 provides serial and parallel interfaces that can be selected by HSPB pin. When HSPB is low, the parallel interface is selected, the serial interface for high. Some of the interface pins serve a dual purpose depending on the working mode. The pins HALE and HDAT [7] in parallel mode become SCLK and SDAT pins in serial mode and the pins HDAT [6:1] and HCSB0 in parallel mode become slave address in serial mode respectively. Each interface protocol is shown in the following figures.

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Table 9 Pin assignments for serial and parallel interface

Pin Name	Serial Mode	Parallel Mode
HSPB	HIGH	LOW
HALE	SCLK	AEN
HRDB	Not Used (VSSO)	RENB
HWRB	Not Used (VSSO)	WENB
HCSB0	Slave Address[0]	CSB0
HCSB1	Not Used (VSSO)	CSB1
HDAT[0]	Not Used (VSSO)	PDATA[0]
HDAT[1]	Slave Address[1]	PDATA[1]
HDAT[2]	Slave Address[2]	PDATA[2]
HDAT[3]	Slave Address[3]	PDATA[3]
HDAT[4]	Slave Address[4]	PDATA[4]
HDAT[5]	Slave Address[5]	PDATA[5]
HDAT[6]	Slave Address[6]	PDATA[6]
HDAT[7]	SDAT	PDATA[7]

Serial Interface

HDAT [6:1] and HCSB0 pins define slave address in serial mode. Therefore, any slave address can be assigned for full flexibility. The Fig 72 shows an illustration of serial interface for the case of slave address (Read : “0x85”, Write : 0x84”).

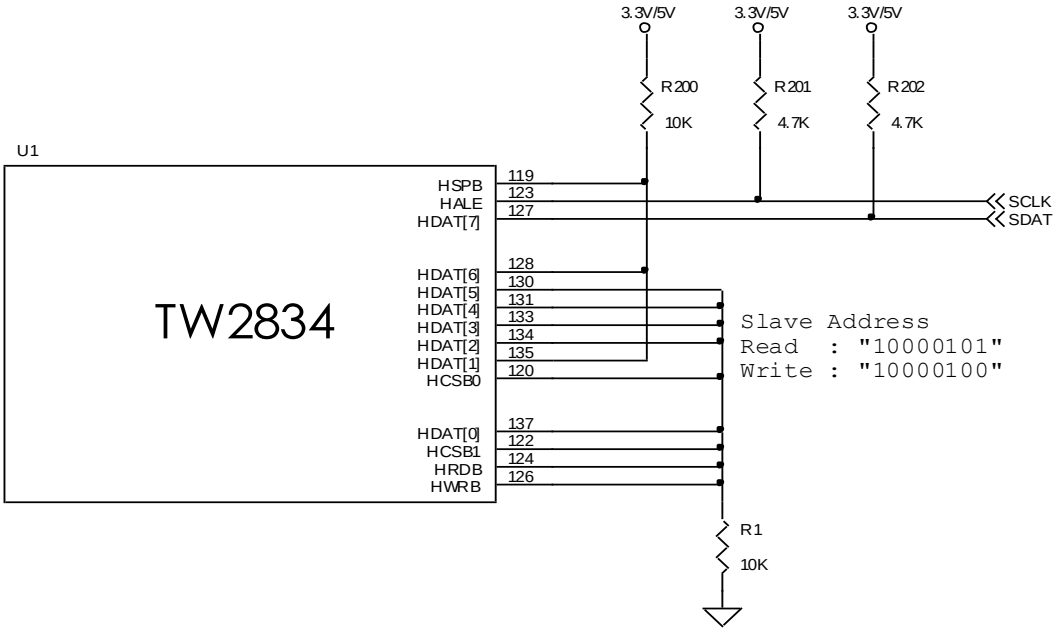


Fig 72 The serial interface for the case of slave address. (Read : “0x85”, Write : “0x84”)

The TW2834 has total 3 pages for registers (1 page can contain 256 registers) so that the page index [1:0] is used for selecting page of registers. Page 0 is assigned for video decoder, Page 1 is for video controller / OSD / encoder and Page 2 is for motion detector / Box / Mouse pointer. The detailed timing diagram is illustrated in the Fig 73 and Fig 74.

The TW2834 also supports automatic index increment so that it can read or write continuous multi-bytes without restart. Therefore, the host can read or write multiple bytes in sequential order without writing additional slave address, page index and index address. The data transfer rate on the bus is up to 400K bits/s.

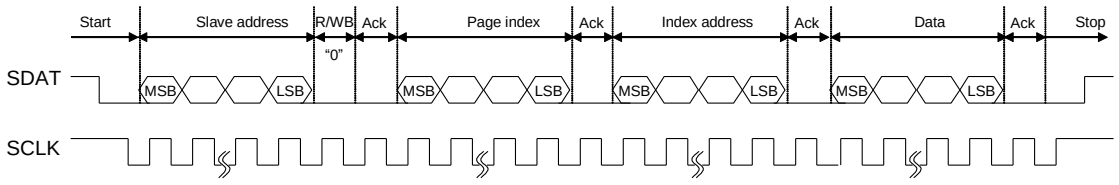


Fig 73 Write timing of serial interface

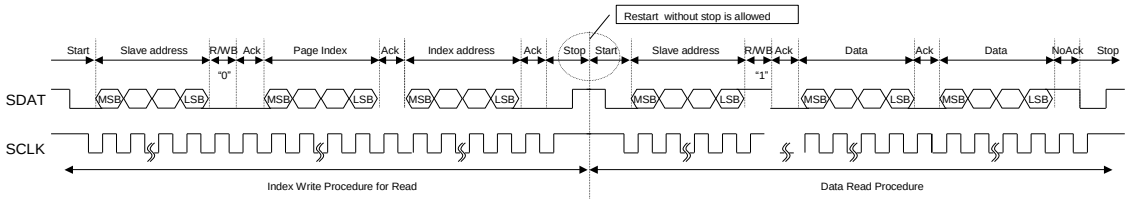


Fig 74 Read timing of serial interface

Parallel Interface

In parallel interface, page of registers can be selected by CSB0 and CSB1 pins, which are working as page index [1:0] in serial interface. Page number 0 is selected by CSB1 = “0” and CSB0 = “0”, page number 1 is by CSB1 = “0” and CSB0 = “1”, and page number 2 is by CSB1 = “1” and CSB0 = “0”. The TW2834 also supports automatic index increment for parallel interface. The writing and reading timing is shown in the Fig 75 and Fig 76 respectively. The detail timing parameters are in Table 10.

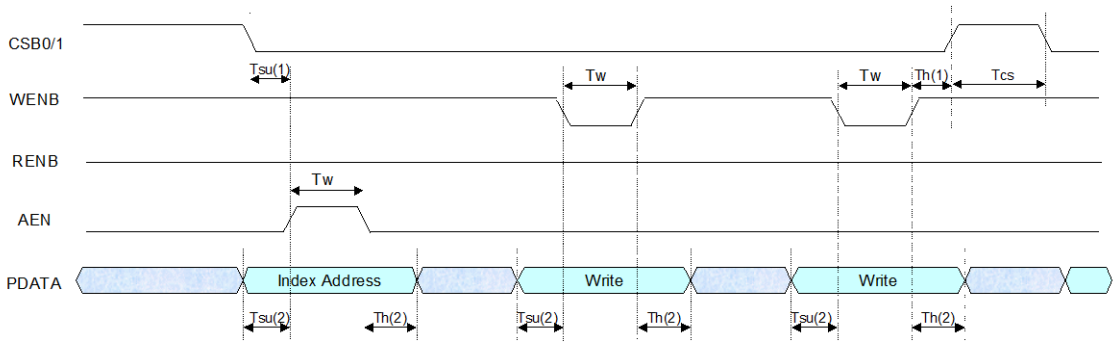


Fig 75 Write timing of parallel interface with auto index increment mode

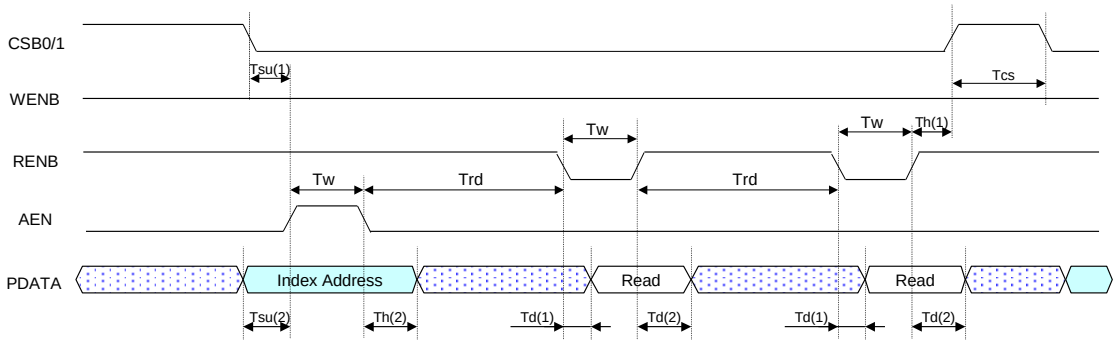


Fig 76 Read timing of parallel interface with auto index increment mode

Table 10 Timing parameters of parallel interface

Parameter	Symbol	Min	Typ	Max	Units
CSB setup until AEN active	Tsu(1)	10			ns
PDATA setup until AEN,WENB active	Tsu(2)	10			ns
AEN, WENB, RENB active pulse width	Tw	40			ns
CSB hold after WENB, RENB inactive	Th(1)	60			ns
PDATA hold after AEN,WENB inactive	Th(2)	20			ns
PDATA delay after RENB active	Td(1)			12	ns
PDATA delay after RENB inactive	Td(2)	60			ns
CSB inactive pulse width	Tcs	60			ns
RENB active delay after AEN inactive RENB active delay after RENB inactive	Trd	60			ns

Interrupt Interface

The TW2834 provides the interrupt request function via an NMIRQ pin. Any video loss, motion or blind detection will make the NMIRQ pin low until cleared via the register. Writing high to the corresponding bit of the interrupt clear register IRQCLR_NOVID, IRQCLR_MDBD (1x7A) will clear the interrupt request. The host can distinguish what event makes interrupt request to IRQ pin by reading the status of IRQCLR_NOVID, IRQCLR_MDBD (1x7A) registers before clearing. Then, the host has to read another status of DET_NOVID, DET_MOTION, DET_BLIND (1x7B, 1x7C) registers to find out whether the event is generated by video loss or video detection, or whether it is made by motion or blind detection. To disable each interrupt, the interrupt status also has its own mask register such as IRQENA_NOVID, IRQENA_MOTION (1x79), and IRQENA_BLIND (1x7C) register. An illustration of the interrupt sequence is shown in the following Fig 77.

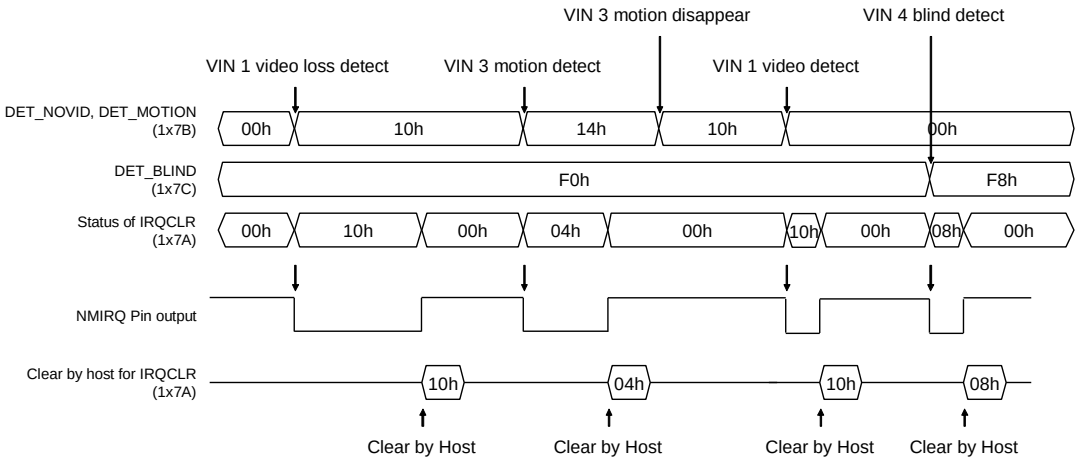


Fig 77 Timing Diagram of Interrupt Interface

The TW2834 also provides the status of video loss, motion detection or the strobe acknowledge for individual channel through the MPPDEC pins with the control of the MPPSET (1x50) register.

Control Register

Register Map

For Video Decoder

Address				BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
VIN0	VIN1	VIN2	VIN3								
0x00	0x40	0x80	0xC0	DET_FORMAT *			DET_COLOR *	LOCK_COLOR *	LOCK_GAIN *	LOCK_OFST *	LOCK_PLL *
0x01	0x41	0x81	0xC1	IFMTMAN	IFORMAT			0	1	DET_NONSTD *	DET_FLD60 *
0x02	0x42	0x82	0xC2	AGC	PEDEST	1	0	GNTIME		OSTIME	
0x03	0x43	0x83	0xC3	HDELAY_X [7:0]							
0x04	0x44	0x84	0xC4	HACTIVE_X [7:0]							
0x05	0x45	0x85	0xC5	HDELAY_Y [7:0]							
0x06	0x46	0x86	0xC6	HACTIVE_Y [7:0]							
0x07	0x47	0x87	0xC7	HACTIVE_Y [9:8]		HDELAY_Y [9:8]		HACTIVE_X [9:8]		HDELAY_X [9:8]	
0x08	0x48	0x88	0xC8	0	0	HSWIDTH					
0x09	0x49	0x89	0xC9	VDELAY_X [7:0]							
0x0A	0x4A	0x8A	0xCA	VACTIVE_X [7:0]							
0x0B	0x4B	0x8B	0xCB	VDELAY_Y [7:0]							
0x0C	0x4C	0x8C	0xCC	VACTIVE_Y [7:0]							
0x0D	0x4D	0x8D	0xCD	HPLLMAN	HPLLTIME			VACTVE_Y [8]	VDELAY_Y [8]	VACTVE_X [8]	VDELAY_X [8]
0x0E	0x4E	0x8E	0xCE	FLDMODE		VSMODE	FLDPOL	HSPOL	VSPOL	1	0
0x0F	0x4F	0x8F	0xCF	HUE							
0x10	0x50	0x90	0xD0	SAT							
0x11	0x51	0x91	0xD1	CONT							
0x12	0x52	0x92	0xD2	BRT							
0x13	0x53	0x93	0xD3	IFCOMP		CLPF		ACCTIME		APCTIME	
0x14	0x54	0x94	0xD4	YPEAK_Y		YPEAK_X		YPEAK_FLT_Y	YPEAK_FLT_X	CKIL	
0x15	0x55	0x95	0xD5	VSFLT_Y		VSFLT_X		HSFLT_Y		HSFLT_X	
0x16	0x56	0x96	0xD6	YBWI_X	COMBMD_X		0	0	0	0	0
0x17	0x57	0x97	0xD7	YBWI_Y	COMBMD_Y		0	0	0	0	0
0x18	0x58	0x98	0xD8	VSCALE_X [15:8]							
0x19	0x59	0x99	0xD9	VSCALE_X [7:0]							
0x1A	0x5A	0x9A	0xDA	VSCALE_Y [15:8]							
0x1B	0x5B	0x9B	0xDB	VSCALE_Y [7:0]							
0x1C	0x5C	0x9C	0xDC	HSCALE_X [15:8]							
0x1D	0x5D	0x9D	0xDD	HSCALE_X [7:0]							
0x1E	0x5E	0x9E	0xDE	HSCALE_Y [15:8]							
0x1F	0x5F	0x9F	0xDF	HSCALE_Y [7:0]							
0x20	0x60	0xA0	0xE0	0	VFLT_MD_X	VBW_X		PAL_DLY_X	ODD_EN_X	EVEN_EN_X	1
0x21	0x61	0xA1	0xE1	0	VFLT_MD_Y	VBW_Y		PAL_DLY_Y	ODD_EN_Y	EVEN_EN_Y	1
0x22	0x62	0xA2	0xE2	BLKEN	BLKCOL	0	LMTOUT	SW_RESET	ANA_SW	DEC_PATH_X	
0x23	0x63	0xA3	0xE3	0	0	0	1	0	0	0	1
0x24	0x64	0xA4	0xE4	HDELAY_PB [7:0] **							
0x25	0x65	0xA5	0xE5	HACTIVE_PB [7:0] **							

For Video Decoder

Address				BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
VIN0	VIN1	VIN2	VIN3								
0x26	0x66	0xA6	0xE6	PB_SCLFLT_EN **	PB_SYNC_EN **	VACTIVE_PB [8] **	VDELAY_PB [8] **	HACTIVE_PB [9:8] **		HDELAY_PB [9:8]	
0x27	0x67	0xA7	0xE7	VDELAY_PB [7:0] **							
0x28	0x68	0xA8	0xE8	VACTIVE_PB [7:0] **							
0x36				VSFLT_PB1 **		HSFLT_PB1 **		VSFLT_PB0 **		HSFLT_PB0 **	
0x37				VSFLT_PB3 **		HSFLT_PB3 **		VSFLT_PB2 **		HSFLT_PB2 **	
0x38				MAN_PB_CROP	PB_CROP_MD	PB_ACT_MD		PB_CH_EN			
0x39				PB_PATH_CH3		PB_PATH_CH2		PB_PATH_CH1		PB_PATH_CH0	
0x3A				PB_FLDPOL				PB_NOVID			
0x3B				0	0	0	0	PB_EC_656	0	0	PB_4CH_MD
0x3C				U_GAIN							
0x3D				V_GAIN							
0x3E				U_OFF							
0x3F				V_OFF							
0x77 **				0	0	0	0	0	0	0	0
0x78				1	0	1	ANA_CH_EN	ADC_PWDN			
0x79				1	0	0	0	0	0	0	0
0x7A				0	0	0	0	0	0	0	0
0x7B				FLDOS_3Y	FLDOS_2Y	FLDOS_1Y	FLDOS_0Y	FLDOS_3X	FLDOS_2X	FLDOS_1X	FLDOS_0X
0x7C				0	0	0	0	1	1	1	1
0x7D				0	0	0	0	0	PB_SDEL_EN **	PB_SDEL **	
0xB8				0	0	0	0	0	0	NOVID_MODE	
0xB9				FLD3*	FLD2*	FLD1*	FLD0*	VAV3*	VAV2*	VAV1*	VAV0*
0xBA				ANA_CH3		ANA_CH2		ANA_CH1		ANA_CH0	
0xF8				HAV_VALID	0	AUTO_BGND	0	C_CORE		Y_H_CORE	
0xF9				0	CDEL			0	0	0	0
0xFA				0	0	1	1	1	1	0	0
0xFB				0	0	0	1	0	0	0	0
0xFC				AFIL_BYP				0	0	0	0
0xFD				0	0	0	0	0	0	0	0
0xFE				0x10*							

Notes 1. "*" stand for read only register
2. VIN0 ~ VIN3 stand for video input 0 ~ video input 3.
3. "**" Modified in TW2834 RevC

For Video Controller (Display path)

Address				BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
CH0	CH1	CH2	CH3								
1x00				SYS_5060	OVERLAY	LINK_LAST_X	LINK_LAST_Y	LINK_EN_X	LINK_EN_Y	LINK_NUM	
1x01				0	0	0	0	0	0	0	0
1x02				TBLINK	SAVE_ADDR						
1x03				RECALL_FLD	SAVE_FLD		SAVE_HID	SAVE_REQ			
1x04				0	STRB_FLD		DUAL_PAGE	STRB_REQ			
1x05				NOVID_MODE		0	0	0	ADDR_OUT_EN	INVALID_MODE	
1x06				MUX_MODE	0	MUX_FLD		0	0	0	0
1x07				STRB_AUTO **	0	0	INTR_REQX	INTR_CH			
1x08				MUX_OUT_CH0				MUX_OUT_CH1			
1x09				MUX_OUT_CH2				MUX_OUT_CH3			
1x0A				CHID_MUX_OUT							
1x0B				ZM_EVEN_OS		ZM_ODD_OS		FR_EVEN_OS		FR_ODD_OS	
1x0C				ZMENA	0	ZMBNDCOL		ZMBNDEN	ZMAREAEN	ZMAREA	
1x0D				ZOOMH							
1x0E				ZOOMV							
1x0F				FRZ_FLD		BNDCOL		BGDCOL		BLKCOL	
1x10	1x18	1x20	1x28	CH_EN	POP_UP	FUNC_MODE		DMCH_EN	DMCH_PATH	Reserved	
1x11	1x19	1x21	1x29	RECALL_CH	FRZ_CH	H_MIRROR	V_MIRROR	ENHANCE	BLANK	BOUND	BLINK
1x12	1x1A	1x22	1x2A	0	RECALL_ADDR						
1x13	1x1B	1x23	1x2B	RECALL_DM	FRZ_DM	H_MIRROR_DM	V_MIRROR_DM	ENHANCE_DM	BLANK_DM	BOUND_DM	BLINK_DM
1x14	1x1C	1x24	1x2C	0	RECALL_ADDR_DM						
1x15	1x1D	1x25	1x2D	0	0	0	0	0	0	0	0
1x16	1x1E	1x26	1x2E	PB_AUTO_EN	0	PB_STOP **	EVENT_PB	PB_CH_NUM			
1x2F				0	0	0	0	0	0	0	0
1x30	1x34	1x38	1x3C	PICHL							
1x31	1x35	1x39	1x3D	PICHR							
1x32	1x36	1x3A	1x3E	PICVT							
1x33	1x37	1x3B	1x3F	PICVB							
1x40	1x44	1x48	1x4C	PICHL_DM							
1x41	1x45	1x49	1x4D	PICHR_DM							
1x42	1x46	1x4A	1x4E	PICVT_DM							
1x43	1x47	1x4B	1x4F	PICVB_DM							

Notes 1. "*" stand for read only register
2. CH0 ~ CH3 stand for channel 0 ~ channel 3.
3. "**" Modified in TW2834 RevC

For Video Controller (Record path)

Address				BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
CH0	CH1	CH2	CH3								
1x50				MPPSET_X				MPPSET_Y			
1x51				0	FRAME_OP	FRAME_FLD	DIS_MODE	0	0	SIZE_MODE	
1x52				TBLINK	0	0	0	0	0	0	0
1x53				0	0	0	0	0	0	0	0
1x54				0	STRB_FLD		DUAL_PAGE	STRB_REQ			
1x55				NOVID_MODE		0	CH_START	0	MEM_OP_EN	INVALID_MODE	
1x56				MUX_MODE	TRIG_MODE	MUX_FLD		PIN_TRIG_MD		0	0
1x57				STRB_AUTO	QUE_SIZE						
1x58				QUE_PERIOD[7:0]							
1x59				QUE_PERIOD[9:8]		EXT_TRIG	INTR_REQY	MUX_WR_CH			
1x5A				QUE_WR	QUE_ADDR						
1x5B				0	Q_POS_RD_CTL	Q_DATA_RD_CTL		MUX_SKIP_EN	ACCU_TRIG	QUE_CNT_RST	QUE_POS_RST
1x5C				MUX_SKIP_CH[15:8]							
1x5D				MUX_SKIP_CH[7:0]							
1x5E				CHID_MUX_OUT							
1x5F				FRZ_FLD		BNDCOL		BGDCOL		BLKCOL	
1x60	1x63	1x66	1x69	CH_EN	POP_UP	FUNC_MODE		0	0	DEC_PATH_Y	
1x61	1x64	1x67	1x6A	0	FRZ_CH	H_MIRROR	V_MIRROR	ENHANCE	BLANK	BOUND	BLINK
1x62	1x65	1x68	1x6B	0	0	0	0	0	0	0	0
1x6C				PIC_SIZE3		PIC_SIZE2		PIC_SIZE1		PIC_SIZE0	
1x6D				PIC_POS3		PIC_POS2		PIC_POS1		PIC_POS0	
1x6E				MUX_OUT_CH0				MUX_OUT_CH1			
1x6F				MUX_OUT_CH2				MUX_OUT_CH3			
1x70				POS_CTL_EN	POS_TRIG_MODE	POS_TRIG	POS_INTR	0	POS_RD_CTL	POS_DATA_RD_CTL	
1x71				POS_PERIOD[9:8]		POS_FLD_MD **	POS_SIZE				
1x72				POS_QUE_PER[7:0]							
1x73				POS_CH0				POS_CH1			
1x74				POS_CH2				POS_CH3			
1x75				POS_QUE_WR	POS_CNT_RST	POS_QUE_RST	POS_QUE_ADDR				
1x76				FLD_OP				DVR_IN			
1x77				0	0	0	0	0	0	0	0
1x78				0	0	0	0	0	IRQPOL	IRQRPT	0
1x79				IRQENA_NVMD				IRQENA_MOTION			
1x7A				IRQ_CLEAR				IRQCLR_MDBD			
1x7B				DET_NOVID				DET_MOTION			
1x7C				IRQENA_BLIND				DET_BLIND			
1x7D				MCLK_FR_Y **		MCLK_PH_Y		MCLK_FR_X **		MCLK_PH_X	
1x7E				MCLK_CTL_Y				MCLK_CTL_X			
1x7F				MEM_INIT	0	0	0	0	0	0	1

Notes 1. "*" stand for read only register

2. CH0 ~ CH3 stand for channel 0 ~ channel 3.

3. "**" Modified in TW2834 RevC

For Video Output

Address	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
1x80	ENC_IN_X		ENC_IN_Y		CCIR_IN_X		CCIR_IN_Y	
1x81	DAC_PD_YX	DAC_OUT_YX			DAC_PD_CX	DAC_OUT_CX		
1x82	DAC_PD_YY	DAC_OUT_YY			DAC_PD_CY	DAC_OUT_CY		
1x83	0	CCIR_601	CCIR_OUT_X		BYPASS_Y		CCIR_OUT_Y	
1x84	ENC_MODE	CCIR_LMT	ENC_VS	ENC_FLD	CCIR_FLDPOL	ENC_HSPOL	ENC_VSPOL	ENC_FLDPOL
1x85	ENC_VSOFF		ENC_VSDEL					
1x86	ENC_HSDEL[7:0]							
1x87	ENC_HSDEL[9:8]		0	ACTIVE_VDEL				
1x88	0	CCIR_STD **	ACTIVE_HDEL					
1x89	ENC_FSC		0	0	1	ENC_PHALT	ENC_ALTRST	ENC_PED
1x8A	ENC_CBW_X		ENC_YBW_X		ENC_CBW_Y		ENC_YBW_Y	
1x8B	0	0	ENC_BAR_X	ENC_CKILL_X	0	0	ENC_BAR_Y	ENC_CKILL_Y
1x8C	ENC_HS_LINK	0	0	0	VDOUTY_MODE	HOUT	VOUT	FOUT
1x8D	ECLK_FR_Y		ECLK_PH_Y		ECLK_FR_X		ECLK_PH_X	
1x8E	ECLK_CTL_Y				ECLK_CTL_X			

Notes 1. "*" stand for read only register

2. "**" Modified in TW2834 RevC

For Character Overlay

Address	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
1x90	FONT_WR_DATA[63:56]							
1x91	FONT_WR_DATA[55:48]							
1x92	FONT_WR_DATA[47:40]							
1x93	FONT_WR_DATA[39:32]							
1x94	FONT_WR_DATA[31:24]							
1x95	FONT_WR_DATA[23:16]							
1x96	FONT_WR_DATA[15:8]							
1x97	FONT_WR_DATA[7:0]							
1x98	0	FONT_WR_INDEX						
1x99	FONT_WR_PAGE				FONT_WR_LINE			
1x9A	FONT_REQ_X	FONT_REQ_Y	0	0	0	FONT_WR_TYPE		FONT_WR_FLD
1x9B	CHAR_PATH	CHAR_WR_MODE		CHAR_VLOC				
1x9C	0		CHAR_RD_FLD		CHAR_RD_PAGE			
	0		CHAR_VF_SIZE		CHAR_HF_SIZE			
	0		CHAR_HLOC					
1x9D	0	0	0	0	MIX	BLINK	CLASS3_COL	
	CHAR_TYPE	CHAR_INDEX						

For Character Overlay

Address	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
1xA0	RAMCLR_X	RAMCLR_Y	BLK_TIME		CLASS0ENA_X	CLASS0ENA_Y	B_CLASS0DIS_X	B_CLASS0DIS_Y
1xA1	CHAR_VSPC_X				CHAR_HSPC_X			
1xA2	CHAR_VDEL_X				CHAR_HDEL_X			
1xA3	CHAR_VSPC_Y				CHAR_HSPC_Y			
1xA4	CHAR_VDEL_Y				CHAR_HDEL_Y			
1xA5	CHAR_MIX_C				CHAR_MIX_B			
1xA6	CHAR_BLK_C				CHAR_BLK_B			
1xA7	CLASS3COL1_C				CLASS3COL0_C			
1xA8	CLASS3COL3_C				CLASS3COL2_C			
1xA9	CLASS3COL1_B				CLASS3COL0_B			
1xAA	CLASS3COL3_B				CLASS3COL2_B			
1xAB	CLASS2COL_C				CLASS2COL_B			
1xAC	CLASS1COL_C				CLASS1COL_B			
1xAD	CLASS0COL_C				CLASS0COL_B			
1xAE	CLUT0_Y							
1xAF	CLUT0_CB							
1xB0	CLUT0_CR							
1xB1	CLUT1_Y							
1xB2	CLUT1_CB							
1xB3	CLUT1_CR							
1xB4	CLUT2_Y							
1xB5	CLUT2_CB							
1xB6	CLUT2_CR							
1xB7	CLUT3_Y							
1xB8	CLUT3_CB							
1xB9	CLUT3_CR							
1xBA	0	0	0	0	T_CASCADE_EN	0	ALPHA_OSD **	
1xBB	0	0	BYP_MPP	0	1	0	DEC_BYP_EN	
1xBC	0	0	0	0	0	0	0	0

Notes 1. "**" Modified in TW2834 RevC

For Channel ID CODEC

Address	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
1xC0	0	0	0	VIS_RIC_EN	0	0	0	0
1xC1	VIS_ENA	VIS_EC_EN	VIS_CODE_EN	VIS_MIX_EN	VIS_SEL			
1xC2	VIS_H_OS							
1xC3	0	0	0	VIS_PIXEL_WIDTH				
1xC4	VIS_LINE_WIDTH			VIS_LINE_OS				
1xC5	VIS_HIGH_VAL							
1xC6	VIS_LOW_VAL							
1xC9	AUTO_VBI_DET	VBI_EC_ON	VBI_CODE_EN	VBI_RIC_ON	VBI_MIX_ON	VBI_FLT_EN	0	VBI_RD_CTL
1xCA	VBI_PIXEL_H_OS							
1xCB	VBI_FLD_OS		VAV_CHK **	VBI_PIXEL_HW				
1xCC	VBI_LINE_SIZE			VBI_LINE_OS				
1xCD	MID_VAL							
1xCE	CHID_VALID *							
1xCF	CHID_TYPE *							
1xD0	VIS_MAN0 [15:8]							
1xD1	VIS_MAN0 [7:0]							
1xD2	VIS_MAN1 [15:8]							
1xD3	VIS_MAN1 [7:0]							
1xD4	VIS_MAN2 [15:8]							
1xD5	VIS_MAN2 [7:0]							
1xD6	VIS_MAN3 [15:8]							
1xD7	VIS_MAN3 [7:0]							
1xD8	VIS_MAN4 [15:8]							
1xD9	VIS_MAN4 [7:0]							
1xDA	VIS_MAN5 [15:8]							
1xDB	VIS_MAN5 [7:0]							
1xDC	VIS_MAN6 [15:8]							
1xDD	VIS_MAN6 [7:0]							
1xDE	VIS_MAN7 [15:8]							
1xDF	VIS_MAN7 [7:0]							
1xE0	AUTO_CHID0							
1xE1	AUTO_CHID1							
1xE2	AUTO_CHID2							
1xE3	AUTO_CHID3							

Notes 1. "*" stand for read only register

2. "**" Modified in TW2834 RevC

For Mouse Pointer

Address	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
2x00	CUR_ON_X	CUR_ON_Y	CUR_TYPE	CUR_SUB	CUR_BLINK	0	CUR_HP [0]	CUR_VP [0]
2x01	CUR_HP [8:1]							
2x02	CUR_VP [8:1]							

For Single Box

Address	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
2x03	BOX_TYPE	BOX_EMP	0	0	ALPHA_2DBOX **		ALPHA_BOX **	
2x04	BOX_BNDCOL							
2x05	BOX_PLNCOL1				BOX_PLNCOL0			
2x06	BOX_PLNCOL3				BOX_PLNCOL2			
2x07	BOX_PLNCOL5				BOX_PLNCOL4			
2x08	BOX_PLNCOL7				BOX_PLNCOL6			
2x09	BOX_PLNCOL9				BOX_PLNCOL8			
2x0A	BOX_PLNCOLB				BOX_PLNCOLA			
2x0B	BOX_PLNCOLD				BOX_PLNCOLC			
2x0C	BOX_PLNCOLF				BOX_PLNCOLE			

Address								BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
B0	B1	B2	B3	B4	B5	B6	B7								
2x10	2x15	2x1A	2x1F	2x24	2x29	2x2E	2x33	BOX_EN_X	BOX_EN_Y	BOX_OBND	BOX_IBND	BOX_PLNMIX	BOX_PLNEN	BOX_HL[0]	BOX_VT[0]
2x11	2x16	2x1B	2x20	2x25	2x2A	2x2F	2x34	BOX_HL[8:1]							
2x12	2x17	2x1C	2x21	2x26	2x2B	2x30	2x35	BOX_HW							
2x13	2x18	2x1D	2x22	2x27	2x2C	2x31	2x36	BOX_VT[8:1]							
2x14	2x19	2x1E	2x23	2x28	2x2D	2x32	2x37	BOX_VW							

Address								BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
B8	B9	B10	B11	B12	B13	B14	B15								
2x38	2x3D	2x42	2x47	2x4C	2x51	2x56	2x5B	BOX_EN_X	BOX_EN_Y	BOX_OBND	BOX_IBND	BOX_PLNMIX	BOX_PLNEN	BOX_HL[0]	BOX_VT[0]
2x39	2x3E	2x43	2x48	2x4D	2x52	2x57	2x5C	BOX_HL[8:1]							
2x3A	2x3F	2x44	2x49	2x4E	2x53	2x58	2x5D	BOX_HW							
2x3B	2x40	2x45	2x4A	2x4F	2x54	2x59	2x5E	BOX_VT[8:1]							
2x3C	2x41	2x46	2x4B	2x50	2x55	2x5A	2x5F	BOX_VW							

Notes 1. B0 ~ B15 stand for single box 0 to 15.

2. "**" Modified in TW2834 RevC

For 2D Arrayed Box & Motion Detector

Address				BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
2DB0	2DB1	2DB2	2DB3								
2x60	2x68	2x70	2x78	2DBOX_EN_X	2DBOX_EN_Y	2DBOX_MODE	2DBOX_DETEN	2DBOX_MSKEN	2DBOX_MIX	2DBOX_CUREN	2DBOX_BNDEN
2x61	2x69	2x71	2x79	2DBOX_PLNCOL				2DBOX_BNDCOL		2DBOX_HL[0]	2DBOX_VT[0]
2x62	2x6A	2x72	2x7A	2DBOX_HL[8:1]							
2x63	2x6B	2x73	2x7B	2DBOX_HW							
2x64	2x6C	2x74	2x7C	2DBOX_VT[8:1]							
2x65	2x6D	2x75	2x7D	2DBOX_VW							
2x66	2x6E	2x76	2x7E	2DBOX_HNUM				2DBOX_VNUM			
2x67	2x6F	2x77	2x7F	2DBOX_CURHP				2DBOX_CURVP			

Notes 1. 2DB0 ~ 2DB3 stand for 2D arrayed box 0 to 3.

For 2D Arrayed Box & Motion Detector

Address				BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
VIN0	VIN1	VIN2	VIN3								
2x80	2xA0	2xC0	2xE0	MD_DIS	MD_REFFLD	BD_CELSENS		BD_LVSENS			
2x81	2xA1	2xC1	2xE1	2DBOX_HINV	2DBOX_VINV	MD_FLD		MD_ALIGN			
2x82	2xA2	2xC2	2xE2	MD_CELLSENS		MASK_MODE	MD_LVSENS				
2x83	2xA3	2xC3	2xE3	MD_STRB_EN	MD_STRB	MD_SPEED					
2x84	2xA4	2xC4	2xE4	MD_DET_PERIOD							
2x85	2xA5	2xC5	2xE5	MD_TMPSENS				MD_SPSENS			
2x86	2xA6	2xC6	2xE6	MD_MASK[15:8]							
2x88	2xA8	2xC8	2xE8								
2x8A	2xAA	2xCA	2xEA								
2x8C	2xAC	2xCC	2xEC								
2x8E	2xAE	2xCE	2xEE								
2x90	2xB0	2xD0	2xF0								
2x92	2xB2	2xD2	2xF2								
2x94	2xB4	2xD4	2xF4								
2x96	2xB6	2xD6	2xF6								
2x98	2xB8	2xD8	2xF8								
2x9A	2xBA	2xDA	2xFA								
2x9C	2xBC	2xDC	2xFC								
2x87	2xA7	2xC7	2xE7	MD_MASK[7:0]							
2x89	2xA9	2xC9	2xE9								
2x8B	2xAB	2xCB	2xEB								
2x8D	2xAD	2xCD	2xED								
2x8F	2xAF	2xCF	2xEF								
2x91	2xB1	2xD1	2xF1								
2x93	2xB3	2xD3	2xF3								
2x95	2xB5	2xD5	2xF5								
2x97	2xB7	2xD7	2xF7								
2x99	2xB9	2xD9	2xF9								
2x9B	2xBB	2xDB	2xFB								
2x9D	2xBD	2xDD	2xFD								
2x9E				MD_PATH	0	0	DETCOL_EN	DETCOL_SEL			

Notes 1. VIN0 ~ VIN3 stand for video input 0 ~ video input 3.

Recommended Value

For Video Decoder

Address				NTSC				PAL			
VIN0	VIN1	VIN2	VIN3	1 CH	4 CH	9 CH	16 CH	1 CH	4 CH	9 CH	16 CH
0x00	0x40	0x80	0xC0	8'h00				8'h00			
0x01	0x41	0x81	0xC1	C4				84			
0x02	0x42	0x82	0xC2	A5				A5			
0x03	0x43	0x83	0xC3	1A				22			
0x04	0x44	0x84	0xC4	D0				D0			
0x05	0x45	0x85	0xC5	1A				22			
0x06	0x46	0x86	0xC6	D0				D0			
0x07	0x47	0x87	0xC7	88				88			
0x08	0x48	0x88	0xC8	20				20			
0x09	0x49	0x89	0xC9	06				05			
0x0A	0x4A	0x8A	0xCA	F0				20			
0x0B	0x4B	0x8B	0xCB	06				05			
0x0C	0x4C	0x8C	0xCC	F0				20			
0x0D	0x4D	0x8D	0xCD	00				0A			
0x0E	0x4E	0x8E	0xCE	D2				D2			
0x0F	0x4F	0x8F	0xCF	80				80			
0x10	0x50	0x90	0xD0	80				80			
0x11	0x51	0x91	0xD1	80				80			
0x12	0x52	0x92	0xD2	80				82			
0x13	0x53	0x93	0xD3	1F				2F			
0x14	0x54	0x94	0xD4	00	10	00	00	00	10	00	00
0x15	0x55	0x95	0xD5	00	21	32	33	00	20	32	33
0x16	0x56	0x96	0xD6	00				00	C0	00	00
0x17	0x57	0x97	0xD7	00				40			
0x18	0x58	0x98	0xD8	FF	7F	55	3F	FF	7F	55	3F
0x19	0x59	0x99	0xD9	FF				FF			
0x1A	0x5A	0x9A	0xDA	FF		-	-	FF		-	-
0x1B	0x5B	0x9B	0xDB	FF		-	-	FF		-	-
0x1C	0x5C	0x9C	0xDC	FF	7F	55	3F	FF	7F	55	3F
0x1D	0x5D	0x9D	0xDD	FF				FF			
0x1E	0x5E	0x9E	0xDE	FF		-	-	FF		-	-
0x1F	0x5F	0x9F	0xDF	FF		-	-	FF		-	-
0x20	0x60	0xA0	0xE0	07	07	07	57	0F	07	07	57
0x21	0x61	0xA1	0xE1	07				0F			
0x22	0x62	0xA2	0xE2	00				00			
0x23	0x63	0xA3	0xE3	11				11			
0x24	0x64	0xA4	0xE4	00				00			
0x25	0x65	0xA5	0xE5	D0				D0			
0x26	0x66	0xA6	0xE6	C8				E8			
0x27	0x67	0xA7	0xE7	00				00			
0x28	0x68	0xA8	0xE8	F0				20			
0x36				00	99	EE	FF	00	99	EE	FF
0x37				00	99	EE	FF	00	99	EE	FF
0x38				00				00			

Address				NTSC				PAL			
VIN0	VIN1	VIN2	VIN3	1 CH	4 CH	9 CH	16 CH	1 CH	4 CH	9 CH	16 CH
0x39				00				00			
0x3A				00				00			
0x3B				00				00			
0x3C				80				80			
0x3D				80				80			
0x3E				82				82			
0x3F				82				82			
0x77				00				00			
0x78				A0				A0			
0x79				00				00			
0x7A				00				00			
0x7B				00				00			
0x7C				08				08			
0x7D				00				00			
0xB8				00				00			
0xF8				0A				0A			
0xF9				40				40			
0xFA				3C				3C			
0xFB				10				10			
0xFC				00				00			
0xFD				00				00			

Notes 1. : Modified in TW2834 RevC

For Video Controller

Address				NTSC				PAL			
CH0	CH1	CH2	CH3	1 CH	4 CH	9 CH	16 CH	1 CH	4 CH	9 CH	16 CH
1x00				8'h00				8'h80			
1x01				00				00			
1x02				00				00			
1x03				00				00			
1x04				00				00			
1x05				84				84			
1x06				00				00			
1x07				00				00			
1x08				00				00			
1x09				00				00			
1x0A				00				00			
1x0B				D7				D7			
1x0C				00				00			
1x0D				00				00			
1x0E				00				00			
1x0F				A7				A7			
1x10				80				80			
1x18				81				81			
1x20				82				82			
1x28				83				83			
1x11	1x19	1x21	1x29	02				02			
1x12	1x1A	1x22	1x2A	00				00			
1x13	1x1B	1x23	1x2B	00				00			
1x14	1x1C	1x24	1x2C	00				00			
1x15	1x1D	1x25	1x2D	00				00			
1x16	1x1E	1x26	1x2E	00				00			
1x17	1x1F	1x27	1x2F	00				00			
1x30				00	00	00	00	00	00	00	00
1x31				B4	5A	3C	2D	B4	5A	3C	2D
1x32				00	00	00	00	00	00	00	00
1x33				78	3C	28	1E	90	48	30	24
1x34				00	5A	3C	2D	00	5A	3C	2D
1x35				B4	B4	78	5A	B4	B4	78	5A
1x36				00	00	00	00	00	00	00	00
1x37				78	3C	28	1E	90	48	30	24
1x38				00	00	78	5A	00	00	78	5A
1x39				B4	5A	B4	87	B4	5A	B4	87
1x3A				00	3C	00	00	00	48	00	00
1x3B				78	78	28	1E	90	90	30	24
1x3C				00	5A	00	87	00	5A	00	87
1x3D				B4	B4	3C	B4	B4	B4	3C	B4
1x3E				00	3C	28	00	00	48	30	00
1x3F				78	78	50	1E	90	90	60	24
1x40 ~ 1x4F				00				00			
1x50				00				00			

Address				NTSC				PAL			
CH0	CH1	CH2	CH3	1 CH	4 CH	9 CH	16 CH	1 CH	4 CH	9 CH	16 CH
1x51				00				00			
1x52				00				00			
1x53				00				00			
1x54				00				00			
1x55				84				84			
1x56				00				00			
1x57				00				00			
1x58				00				00			
1x59				00				00			
1x5A				00				00			
1x5B				00				00			
1x5C				00				00			
1x5D				00				00			
1x5E				00				00			
1x5F				A7				A7			
1x60				80		-	-	80		-	-
1x63				81		-	-	81		-	-
1x66				82		-	-	82		-	-
1x69				83		-	-	83		-	-
1x61	1x64	1x67	1x6A	02		-	-	-			
1x62	1x65	1x68	1x6B	00		-	-	-			
1x6C				00	FF	-	-	00	FF	-	-
1x6D				00	E4	-	-	00	E4	-	-
1x6E				00				00			
1x6F				00				00			
1x70				00				00			
1x71				00				00			
1x72				00				00			
1x73				00				00			
1x74				00				00			
1x75				00				00			
1x76				00				00			
1x77				00				00			
1x78				00				00			
1x79				FF				FF			
1x7A				00				00			
1x7B				00				00			
1x7C				F0				F0			
1x7D				00				00			
1x7E				77				77			
1x7F				21				21			
1x80				77				77			
1x81				11				11			
1x82				55				55			
1x83				01				01			
1x84				C0				C0			
1x85				10				10			

Address				NTSC				PAL			
CH0	CH1	CH2	CH3	1 CH	4 CH	9 CH	16 CH	1 CH	4 CH	9 CH	16 CH
1x86				00				00			
1x87				0D				0D			
1x88				20				20			
1x89				09				4C			
1x8A				AA				AA			
1x8B				00				00			
1x8C				08				08			
1x8D				22				22			
1x8E				00				00			
1x90 ~ 1xBF				00				00			
1xC0				50				50			
1xC1				40				40			
1xC2				00				00			
1xC3				1F				1F			
1xC4				E7				E7			
1xC5				EB				EB			
1xC6				10				10			
1xC7				00				00			
1xC8				00				00			
1xC9 ~ 1xDF				00				00			

Notes 1. Blanks have the same value of 1 CH.

2. All values are Hexa format.

For Motion Detector

Address				NTSC	PAL
VIN0	VIN1	VIN2	VIN3		
2x80	2xA0	2xC0	2xE0	8'h17	8'h17
2x81	2xA1	2xC1	2xE1	08	08
2x82	2xA2	2xC2	2xE2	6A	6A
2x83	2xA3	2xC3	2xE3	07	07
2x84	2xA4	2xC4	2xE4	00	00
2x85	2xA5	2xC5	2xE5	24	24

Notes 1. All values are Hexa format.

Register Description

VIN	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	0x00	DET_FORMAT *			DET_ COLOR *	LOCK_ COLOR *	LOCK_ GAIN *	LOCK_ OFST *	LOCK_ PLL *
1	0x40								
2	0x80								
3	0xC0								

Notes "*" stand for read only register

DET_FORMAT Status of video standard detection for analog input.

0 PAL-B/D
1 PAL-M
2 PAL-N
3 PAL-60
4 NTSC-M
5 NTSC-4.43
6 NTSC-N

DET_COLOR Status of color detection for analog input.

0 Color is not detected
1 Color is detected

LOCK_COLOR Status of locking for color demodulation loop.

0 Color demodulation loop is not locked
1 Color demodulation loop is locked

LOCK_GAIN Status of locking for AGC loop.

0 AGC loop is not locked
1 AGC loop is locked

LOCK_OFST Status of locking for clamping loop.

0 Claming loop is not locked
1 Claming loop is locked

LOCK_PLL Status of locking for horizontal PLL.

0 Horizontal PLL is not locked
1 Horizontal PLL is locked

VIN	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	0x01	IFMTMAN	IFORMAT			0	1	DET_ NONSTD *	DET_ FLD60 *
1	0x41								
2	0x81								
3	0xC1								

Notes "*" stand for read only register

IFMTMAN — Setting video standard manually with IFORMAT.

0 Detecting video standard of video input automatically (default)

1 Video standard is selected with IFORMAT

IFORMAT — Force to operate in a particular video standard when IFMTMAN = "1" or to free-run in a particular video standard on no-video status when IFMTMAN = "0".

0 PAL-B/D (default)

1 PAL-M

2 PAL-N

3 PAL-60

4 NTSC-M

5 NTSC-4.43

6 NTSC-N

DET_NONSTD — Status of non-standard video detection.

0 The incoming video source is standard

1 The incoming video source is non-standard

DET_FLD60 — Status of field frequency of incoming video.

0 50Hz field frequency

1 60Hz field frequency

VIN	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	0x02	AGC	PEDEST	1	0	GNTIME		OSTIME	
1	0x42								
2	0x82								
3	0xC2								

AGC — Control the AGC function for active video.

0 Disable the AGC (default)

1 Enable the AGC

PEDEST — Control pedestal level by 7.5 IRE.

0 No pedestal level (0 IRE is ITU-R BT.601 code 16) (default)

1 7.5 IRE setup level (7.5 IRE is ITU-R BT.601 code 16)

GNTIME — Control the time constant of gain tracking loop.

0 Slower

1 Slow (default)

2 Fast

3 Faster

OSTIME — Control the time constant of offset tracking loop.

0 Slower

1 Slow (default)

2 Fast

3 Faster

Path	VIN	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
X	0	0x07							HDELAY[9:8]	
	1	0x47								
	2	0x87								
	3	0xC7								
	0	0x03	HDELAY[7:0]							
	1	0x43								
	2	0x83								
	3	0xC3								
Y	0	0x07			HDELAY[9:8]					
	1	0x47								
	2	0x87								
	3	0xC7								
	0	0x05	HDELAY[7:0]							
	1	0x45								
	2	0x85								
	3	0xC5								

HDELAY This 10 bit register defines the starting location of horizontal active pixel with 1 pixel unit. The default value is decimal 32.

Path	VIN	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
X	0	0x07					HACITIVE[9:8]			
	1	0x47								
	2	0x87								
	3	0xC7								
	0	0x04	HACTIVE[7:0]							
	1	0x44								
	2	0x84								
	3	0xC4								
Y	0	0x07	HACTIVE[9:8]							
	1	0x47								
	2	0x87								
	3	0xC7								
	0	0x06	HACTIVE[7:0]							
	1	0x46								
	2	0x86								
	3	0xC6								

HACTIVE This 10 bit register defines the number of horizontal active pixel with 1 pixel unit. The default value is decimal 720.

VIN	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	0x08	0	0	HSWIDTH					
1	0x48								
2	0x88								
3	0xC8								

HSWIDTH This 6 bit register defines the width of horizontal sync output with 1 pixel unit. The default value is decimal 32.

Path	VIN	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
X	0	0x0D								VDELAY[8]
	1	0x4D								
	2	0x8D								
	3	0xCD								
	0	0x09	VDELAY[7:0]							
	1	0x49								
	2	0x89								
	3	0xC9								
Y	0	0x0D						VDELAY[8]		
	1	0x4D								
	2	0x8D								
	3	0xCD								
	0	0x0B	VDELAY[7:0]							
	1	0x4B								
	2	0x8B								
	3	0xCB								

VDELAY This 9 bit register defines the starting location of vertical active with 1 line unit. The default value is decimal 6. But VDELAY_Y value should be from 0 to decimal 14.for 60Hz system and from 0 to decimal 9 for 50Hz system.

Path	VIN	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
X	0	0x0D							VACTIVE[8]	
	1	0x4D								
	2	0x8D								
	3	0xCD								
	0	0x0A	VACTIVE[7:0]							
	1	0x4A								
	2	0x8A								
	3	0xCA								
Y	0	0x0D					VACTIVE[8]			
	1	0x4D								
	2	0x8D								
	3	0xCD								
	0	0x0C	VACTIVE[7:0]							
	1	0x4C								
	2	0x8C								
	3	0xCC								

VACTIVE — This 9 bit register defines the number of vertical active lines with 1 line unit. The default value is decimal 240. But VACTIVE_Y value should be greater than 240.

VIN	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	0x0D	HPLLMAN	HPLLTIME						
1	0x4D								
2	0x8D								
3	0xCD								

HPLLMAN Setting horizontal PLL time constant with HPLLTIME.

0 Automatic horizontal tracking mode (default)

1 Horizontal PLL time constant is fixed with HPLLTIME

HPLLTIME Control the time constant of horizontal PLL when HPLLMAN = “1”.

0 Slow

: :

4 Typical (default)

: :

7 Fast

VIN	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	0x0E	FLDMODE		VSMODE	FLDPOL	HSPOL	VSPOL	1	0
1	0x4E								
2	0x8E								
3	0xCE								

FLDMODE Select the field flag generation mode.

0 Field flag is detected from incoming video (default)

1 Field flag is generated from small accumulator of detected field

2 Field flag is generated from medium accumulator of detected field

3 Field flag is generated from large accumulator of detected field

VSMODE Control the VS and field flag timing.

0 VS and field flag is aligned with vertical sync (default)

1 VS and field flag is aligned with HS

FLDPOL Select the FLD polarity.

0 Odd field is high (default)

1 Even field is high

HSPOL Select the HS polarity.

0 Low for sync duration (default)

1 High for sync duration

VSPOL Select the VS polarity.

0 Low for sync duration (default)

1 High for sync duration

VIN	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	0x0F	HUE							
1	0x4F								
2	0x8F								
3	0xCF								

HUE Control the hue information. The resolution is 1.4° / step.

0	-180°
:	:
128	0° (default)
:	:
255	180°

VIN	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	0x10	SAT							
1	0x50								
2	0x90								
3	0xD0								

SAT Control the color saturation. The resolution is 0.8% / step.

0	0%
:	:
128	100% (default)
:	:
255	200%

VIN	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	0x11	CONT							
1	0x51								
2	0x91								
3	0xD1								

CONT Control the contrast. The resolution is 0.8% / step.

0 0%

: :

128 100% (default)

: :

255 200%

VIN	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	0x12	BRT							
1	0x52								
2	0x92								
3	0xD2								

BRT Control the brightness. The resolution is 0.2IRE / step.

0 -25IRE

: :

128 0IRE (default)

: :

255 25IRE

VIN	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	0x13	IFCOMP		CLPF		ACCTIME		APCTIME	
1	0x53								
2	0x93								
3	0xD3								

IFCOMP — Select the IF-compensation filter mode.

0 No compensation (default)
1 +1 dB/ MHz
2 +2 dB/ MHz
3 +3 dB/ MHz

CLPF — Select the Color LPF mode.

0 550KHz bandwidth
1 750KHz bandwidth (default)
2 950KHz bandwidth
3 1.1MHz bandwidth

ACCTIME — Control the time constant of auto color control loop.

0 Slower
1 Slow
2 Fast
3 Faster (default)

APCTIME — Control the time constant of auto phase control loop.

0 Slower
1 Slow
2 Fast
3 Faster (default)

VIN	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	0x14	YPEAK_Y		YPEAK_X		YPEAK_ FLT_Y	YPEAK_ FLT_X	CKIL	
1	0x54								
2	0x94								
3	0xD4								

YPEAK — Control the luminance peaking for display and record path.

0 No peaking (default)
1 31.25%
2 62.5%
3 93.75%

YPEAK_FLT — Select the luminance peaking filter mode for display and record path.

0 4~5MHz frequency band (default)
1 2~4MHz frequency band

CKIL — Control the color killing mode.

0 Auto detection mode (default)
1 Auto detection mode
2 Color is always alive
3 Color is always killed

VIN	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	0x15	VSFLT_Y		VSFLT_X		HSFLT_Y		HSFLT_X	
1	0x55								
2	0x95								
3	0xD5								

VSFLT Select the vertical anti-aliasing filter mode for display and record path.

0,1 Full bandwidth (default)

2 0.25 Line-rate bandwidth

3 0.18 Line-rate bandwidth

HSFLT Select the horizontal anti-aliasing filter mode for display and record path.

0 Full bandwidth (default)

1 2 MHz bandwidth

2 1.5 MHz bandwidth

3 1 MHz bandwidth

Path	VIN	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
X	0	0x16	YBWI	COMBMD		HSFRM	0	0	0	0
	1	0x56								
	2	0x96								
	3	0xD6								
Y	0	0x17								
	1	0x57								
	2	0x97								
	3	0xD7								

YBWI Select the luminance trap filter mode.

0 Narrow bandwidth trap filter mode (default)

1 Wide bandwidth trap filter mode

COMBMD Select the adaptive comb filter mode.

0,1 Adaptive comb filter mode (default)

2 Force trap filter mode

3 Not supported

HSFRM Select the special horizontal anti-aliasing filter mode for frame CIF display mode that means 1/2 H scaling but full V scaling picture.

0 Disable the special horizontal anti-aliasing filter. (default)

1 Enable the special horizontal anti-aliasing filter for frame CIF display mode

Path	VIN	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]

X	0	0x18	VSCALE[15:8]
	1	0x58	
	2	0x98	
	3	0xD8	
	0	0x19	VSCALE[7:0]
	1	0x59	
	2	0x99	
	3	0xD9	
Y	0	0x1A	VSCALE[15:8]
	1	0x5A	
	2	0x9A	
	3	0xDA	
	0	0x1B	VSCALE[7:0]
	1	0x5B	
	2	0x9B	
	3	0xDB	

VSCALE The 16 bit register defines a vertical scaling ratio. The actual vertical scaling ratio is VSCALE/(2^16 – 1). The default value is 0xFFFF.

Path	VIN	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
X	0	0x1C	HSCALE[15:8]							
	1	0x5C								
	2	0x9C								
	3	0xDC								
	0	0x1D	HSCALE[7:0]							
	1	0x5D								
	2	0x9D								
	3	0xDD								
Y	0	0x1E	HSCALE[15:8]							
	1	0x5E								
	2	0x9E								
	3	0xDE								
	0	0x1F	HSCALE[7:0]							
	1	0x5F								
	2	0x9F								
	3	0xDF								

HSCALE The 16 bit register defines a horizontal scaling ratio. The actual horizontal scaling ratio is HSCALE/(2^16 – 1). The default value is 0xFFFF.

Path	VIN	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]

X	0	0x20	0	VFLT_MD	VBW	PAL_DLY	ODD_EN	EVEN_EN	1
	1	0x60							
	2	0xA0							
	3	0xE0							
Y	0	0x21							
	1	0x61							
	2	0xA1							
	3	0xE1							

VFLT_MD — Select the additional vertical scaling filter mode.

0 Vertical poly-phase mode (default)

1 Additional vertical bandwidth reduction mode with VBW bits

VBW — Control the vertical bandwidth when VSFLT_MD = “1”.

0 Wider (default)

1 Wide

2 Narrow

3 Narrower

PAL_DLY — Select the PAL delay line mode.

0 Vertical scaling mode is selected in chrominance path (default)

1 PAL delay line mode is selected in chrominance path

ODD_EN — Control the valid signal in ODD field.

0 Valid signal is always disabled in ODD field

1 Normal operation (default)

EVEN_EN — Control the valid signal in EVEN field.

0 Valid signal is always disabled in EVEN field

1 Normal operation (default)

VIN	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	0x22	BLKEN	BLKCOL	0	LMTOUT	SW_ RESET	ANA_SW	DEC_PATH_X	
1	0x62								
2	0xA2								
3	0xE2								

BLKEN — Control the blank output.
- 0 Blank color is disabled (default)
- 1 Blank color is enabled

BLKCOL — Select the blank color when BLKEN = “1”.
- 0 Blue color (default)
- 1 Black color

LMTOUT — Control the range of output level.
- 0 Output ranges are limited to 2 ~ 254 (default)
- 1 Output ranges are limited to 16 ~ 239

SW_RESET — Reset the system by software except control registers.
This bit is cleared by itself in a few clocks after enabled
- 0 Normal operation (default)
- 1 Enable soft reset

ANA_SW — Select the analog video input using switch.
- 0 VIN_A channel is selected (default)
- 1 VIN_B channel is selected

DEC_PATH_X — Select the video input for each decoder path in display path.
- 0 Video input from internal video decoder on VIN0 pins (default)
- 1 Video input from internal video decoder on VIN1 pins
- 2 Video input from internal video decoder on VIN2 pins
- 3 Video input from internal video decoder on VIN3 pins

VIN	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	0x23	0	0	0	1	0	0	0	1
1	0x63								
2	0xA3								
3	0xE3								

This is reserved register.
For normal operation, the above value should be set in this register.

PBIN	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	0x26							HDELAY_PB[9:8]	
1	0x66								
2	0xA6								
3	0xE6								
0	0x24	HDELAY_PB[7:0]							
1	0x64								
2	0xA4								
3	0xE4								

HDELAY_PB — This 10 bit register defines the starting location of horizontal active pixel with 1 pixel unit. The default value is decimal 0. This register is enabled only when the PB_SYNC_EN (0x26, 0x66, 0xA6, 0xE6) = “1”.

PBIN	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	0x26					HACTIVE_PB[9:8]			
1	0x66								
2	0xA6								
3	0xE6								
0	0x25	HACTIVE_PB[7:0]							
1	0x65								
2	0xA5								
3	0xE5								

HACTIVE_PB — This 10 bit register defines the number of horizontal active pixel with 1 pixel unit. The default value is decimal 720. This register is enabled only when the PB_SYNC_EN (0x26, 0x66, 0xA6, 0xE6) = “1”.

PBIN	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	0x26	PB_SCL_EN	PB_SYNC_EN						
1	0x66								
2	0xA6								
3	0xE6								

PB_SCL_EN Enable the independent anti-aliasing filter mode for playback input path.
For the details, the application note (page 6 ~ 13) can be referred to.
0 Disable the independent anti-aliasing filter mode for playback input path
In this case, it is controlled by anti-aliasing filter mode of VIN path (default)
1 Enable the independent anti-aliasing filter mode for playback input path

PB_SYNC_EN Enable the independent H/V sync control mode for playback input path.
0 Disable the independent H/V sync control mode for playback input path
In this case, it is controlled by H/V sync mode of VIN path (default)
1 Enable the independent H/V sync control for playback input path

PBIN	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	0x26				VDELAY_PB[8]				
1	0x66								
2	0xA6								
3	0xE6								
0	0x27	VDELAY_PB[7:0]							
1	0x67								
2	0xA7								
3	0xE7								

VDELAY_PB This 9 bit register defines the starting location of vertical active with 1 line unit. The default value is decimal 0. This register is enabled only when the PB_SYNC_EN (0x26, 0x66, 0xA6, 0xE6) = “1”.

PBIN	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	0x26			VACTIVE_PB[8]					
1	0x66								
2	0xA6								
3	0xE6								
0	0x28	VACTIVE_PB[7:0]							
1	0x68								
2	0xA8								
3	0xE8								

VACTIVE_PB This 9 bit register defines the number of vertical active lines with 1 line unit. The default value is decimal 240. This register is enabled only when the PB_SYNC_EN (0x26, 0x66, 0xA6, 0xE6) = “1”.

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x36	VSFLT_PB1		HSFLT_PB1		VSFLT_PB0		HSFLT_PB0	
0x37	VSFLT_PB3		HSFLT_PB3		VSFLT_PB2		HSFLT_PB2	

VSFLT_PB Select the vertical anti-aliasing filter mode for playback path only when the PB_SCL_EN = “1”.

0,1 Full bandwidth (default)

2 0.25 Line-rate bandwidth

3 0.18 Line-rate bandwidth

HSFLT_PB Select the horizontal anti-aliasing filter mode for playback path only when the PB_SCL_EN = “1”.

0 Full bandwidth (default)

1 2 MHz bandwidth

2 1.5 MHz bandwidth

3 1 MHz bandwidth

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x38	MAN_PB_CROP	PB_CROP_MD	PB_ACT_MD		PB_CH_EN			

MAN_PB_CROP Select manual cropping mode for playback input

0 Auto cropping mode with fixed cropping position (default)

1 Manual cropping mode with HDELAY/HACTIVE and VDELAY/VACTIVE

PB_CROP_MD Select the cropping mode for playback input

0 Normal record mode or frame record mode (default)

1 Cropping for DVR record mode or DVR frame record mode input

PB_ACT_MD Select the horizontal active size for playback input when MAN_PB_CROP is low

0 720 pixels (default)

1 704 pixels

2/3 640 pixels

PB_CH_EN Select the playback input for each channel in display path

PB_CH_EN[3:0] stand for Input 3 to 0

0 Decoder path input (default)

1 Playback path input

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x39	PB_PATH_CH3		PB_PATH_CH2		PB_PATH_CH1		PB_PATH_CH0	

PB_PATH_CH Select the playback input for each playback path if PB_4CH_MD = “1”.

0 Playback input 0 from PBIN [7:0] pin (default)

1 Playback input 1 from VDOUTY [7:0] pin

2 Playback input 2 from DATAY [15:8] pin

3 Playback input 3 from DATAY [7:0] pin

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x3A	PB_FLDPOL				PB_NOVID			

PB_FLDPOL Select the FLD polarity of playback input
PB_FLDPOL[3:0] stand for Input 3 to 0
0 Even field is high
1 Odd field is high

PB_NOVID Force No-Video status to playback input
PB_NOVID[3:0] stands for Input 3 to 0
0 Bypass the playback input
1 Force No-Video status to playback input

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x3B	0				PB_EC_656	0	0	PB_4CH_MD

PB_EC_656 Enable the error correction mode for SAV/EAV code of playback input
0 Enable the error correction mode
1 Bypass

PB_4CH_MD Select 4ch playback mode
0 Playback 1ch mode
1 Playback 4ch mode

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x3C	U_GAIN							

U_GAIN Adjust gain for U (Cb) component of VIN0 ~ VIN3.
The resolution is 0.8% / step.

0	0%
:	:
128	100% (default)
:	:
255	200%

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x3D	V_GAIN							

V_GAIN Adjust gain for V (Cr) component of VIN0 ~ VIN3.
The resolution is 0.8% / step.

0	0%
:	:
128	100% (default)
:	:
255	200%

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x3E	U_OFF							

U_OFF U (Cb) offset adjustment register of VIN0 ~ VIN3.
The resolution is 0.4% / step.

0	-50%
:	:
128	0% (default)
:	:
255	50%

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x3F	V_OFF							

V_OFF V (Cr) offset adjustment register of VIN0 ~ VIN3.
The resolution is 0.4% / step.

0	-50%
:	:
128	0% (default)
:	:
255	50%

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x77	0	0	0	0	0	0	0	0

This is reserved register.
For normal operation, the above value should be set in this register.

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x78	1	0	1	ANA_CH_EN	ADC_PWDN			

ANA_CH_EN — Enable the selectable interface of ADC output to change the analog input pin interface. This bit is related with the ANA_CH (0xBA) register.

0 Fixed interface of ADC output (default)

1 Selectable interface of ADC output with the ANA_CH (0xBA) register

ADC_PWDN — Power down the ADC of video input.

ADC_PWDN [3:0] stands for VIN3 to VIN0.

0 Normal (default)

1 Power down

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x79	0	0	0	0	0	0	0	0
0x7A	0	0	0	0	0	0	0	0

This is reserved register.

For normal operation, the above value should be set in this register.

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x7B	FLDOS_ 3Y	FLDOS_ 2Y	FLDOS_ 1Y	FLDOS_ 0Y	FLDOS_ 3X	FLDOS_ 2X	FLDOS_ 1X	FLDOS_ 0X

FLDOS — Remove the field offset between ODD and EVEN field. The number stands for VIN3 to VIN0 and X, Y stand for display and record path.

0 Normal operation (default)

1 Remove the field offset between ODD and EVEN field

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x7C	0	0	0	0	1	0	0	0

This is reserved register.

For normal operation, the above value should be set in this register.

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x7D	0	0	0	0	0	PB_SDEL_EN	PB_SDEL	

PB_SDEL_EN Enable the variable parsing mode of ITU-R BT.656 data for playback input

0 Disable the variable parsing mode

1 Enable the variable parsing mode

PB_SDEL Control the start point of active video from ITU-R BT.656 digital playback input when PB_SDEL_EN = “1”

0 No delay

1 1ck delay of 27MHz

2 2ck delay of 27MHz

3 3ck delay of 27MHz

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xB8	0	0	0	0	0	0	NOVID_MODE	

NOVID_MODE Select the No Video signal generation mode

0 Slower (default)

1 Slow

2 Fast

3 Faster

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xB9	FLD3*	FLD2*	FLD1*	FLD0*	VAV3*	VAV2*	VAV1*	VAV0*

Notes “*” stand for read only register

FLD Status of the field flag for each decoder path.

0 Odd field

1 Even field

VAV Status of the vertical active video signal for each decoder path

0 Vertical blanking time

1 Vertical active time

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xBA	ANA_CH3		ANA_CH2		ANA_CH1		ANA_CH0	

ANA_CH — Select the ADC output for each decoder path when ANA_CH_EN = “1”.
This register is useful to change the analog input pin interface.

0 ADC output from VIN0 (default)
1 ADC output from VIN1
2 ADC output from VIN2
3 ADC output from VIN3

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xF8	HAV_VALID	0	AUTO_ BGND	0	C_CORE		Y_H_CORE	

HAV_VALID — Select the VALID output mode.

0 Valid data indicator only for active data (default)
1 Valid data indicator for both active data and ITU-R 656 timing codes

AUTO_BGND — Select the decoder blanking mode.

0 Manual blanking mode (default)
1 Automatic blanking mode when No-video is detected.

C_CORE — Coring to reduce the noise in the chrominance.

0 No coring
1 Coring value is within 128 +/- 1 range
2 Coring value is within 128 +/- 2 range (default)
3 Coring value is within 128 +/- 4 range

Y_H_CORE — Coring to reduce the high frequency noise in the luminance.

0 No coring
1 Coring value is within +/- 1 range
2 Coring value is within +/- 2 range (default)
3 Coring value is within +/- 4 range

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xF9	0	CDEL			0	0	0	0

CDEL — Adjust the group delay of chrominance relative to luminance.

0 -2.0 pixel
1 -1.5 pixel
2 -1.0 pixel
3 -0.5 pixel
4 0.0 pixel (default)
5 0.5 pixel
6 1.0 pixel
7 1.5 pixel

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xFA	0	0	1	1	1	1	0	0
0xFB	0	0	0	1	0	0	0	0

This is reserved register.
For normal operation, the above value should be set in this register.

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xFC	AFIL_BYP				0	0	0	0

AFIL_BYP — Bypass the analog anti-aliasing filter.
AFIL_BYP [3:0] stands for VIN3 to VIN0.

0 Enable the analog anti-aliasing filter (default)
1 Bypass the analog anti-aliasing filter

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xFD	0	0	0	0	0	0	0	0

This is reserved register.
For normal operation, the above value should be set in this register.

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xFE	DEV_ID *					REV_ID *		

Notes "*" stand for read only register

DEV_ID The TW2834 product ID code is 00010.

REV_ID The revision number

0 BAPA2-GE

1 BAPA3-GE

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1x00	SYS_5060	OVERLAY	LINK _LAST_X	LINK _LAST_Y	LINK_EN_X	LINK_EN_Y	LINK_NUM	

SYS_5060 Select the standard format for video controller.

0 60Hz, 525 line format (default)

1 50Hz, 625 line format

OVERLAY Control the overlay between display and record path.

0 Disable the overlay (default)

1 Enable the overlay

LINK_LAST Define the lowest slaver chip in chip-to-chip cascade operation.

0 Master or middle slaver chip (default)

1 The lowest slaver chip

LINK_EN Control the chip-to-chip cascade operation for display and record path.

0 Disable the cascade operation (default)

1 Enable the cascade operation

LINK_NUM Define the stage number of chip-to-chip cascade connection.

0 Master chip (default)

1 1st slaver chip

2 2nd slaver chip

3 3rd slaver chip

Path	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
X	1x01	0	0	0	0	0	0	0	0

This is reserved register.
For normal operation, the above value should be set in this register.

Path	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
X	1x02	TBLINK	SAVE_ADDR						

TBLINK — Control the blink period of channel boundary.

0 Blink for every 30 fields (default)

1 Blink for every 60 fields

SAVE_ADDR — Define the save address of SDRAM.

The Unit Address has 4Mbit memory space.

0-3 Reserved for normal operation. Do not use this address.

4-15 Available address for 64M SDRAM

4-31 Available address for 128M SDRAM

4-63 Available address for 256M SDRAM

4-127 Available address for 512M SDRAM

Path	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
X	1x03	RECALL_FLD	SAVE_FLD		SAVE_HID	SAVE_REQ			

RECALL_FLD Select the field or frame data when recalling picture.
- 0 Recall frame data from SDRAM (default)
- 1 Recall field data from SDRAM

SAVE_FLD Select the field or frame data to save.
- 0 Save Odd Field data to SDRAM (default)
- 1 Save Even field data to SDRAM
- 2 Save Any Field data to SDRAM
- 3 Save Frame (Odd and Even Field) data to SDRAM

SAVE_HID Control the priority to save picture.
- 0 Save picture as shown in screen (default)
- 1 Save picture even though hidden by other picture

SAVE_REQ Request to save for each channel.
SAVE_REQ[3:0] stands for channel 3 to 0
- 0 None operation (default)
- 1 Request to start saving picture

Path	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
X	1x04	0	STRB_FLD		DUAL_PAGE	STRB_REQ			

STRB_FLD Control the field mode for strobe operation.
- 0 Capture odd field only (default)
- 1 Capture even field only
- 2 Capture first field of any field
- 3 Capture frame

DUAL_PAGE Set dual page mode.
- 0 Normal strobe operation for each channel (default)
- 1 Enable dual page operation

STRB_REQ Request strobe operation.
STRB_REQ[3:0] stands for channel 3 to 0
- 0 None operation (default)
- 1 Request to start strobe operation

Path	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
X	1x05	NOVID_MODE		0	0	0	ADDR_OUT_EN	INVALID_MODE	

NOVID_MODE Select the Indication method for No-Video detected channel

0 Bypass (default)

1 Capture last image

2 Blanked with blank color

3 Capture last image and blink channel boundary

ADDR_OUT_EN Control the address pin function of display path for playback 4ch mode

0 Playback 4ch mode for ADDR_X[12:11], BA1_X Pin. (default)

1 Normal mode for ADDR_X[12:11], BA1_X Pin.

INVALID_MODE Indication mode for no channel area

In horizontal and vertical active region

0 Background layer with background color (default)

1 Y = 0, Cb/Cr = 128

2 Y/Cb/Cr = 0

3 Y/Cb/Cr = 0

In horizontal and vertical blanking region

0 Y = 16, Cb/Cr = 128 (default)

1 Background layer with background color

2 Y = 0, Cb = {0, F, V, 0, Cascade, linenum[8:7]}, Cr = {0, linenum[6:0]}

3 Y/Cb/Cr = 0

Path	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
X	1x06	MUX_MODE	0	MUX_FLD		0	0	0	0

MUX_MODE Define the switch operation mode
- 0 Switch still mode (default)
- 1 Switch live mode

MUX_FLD Select the field mode when switch still mode
- 0 Odd Field (default)
- 1 Even Field
- 2,3 Capture Frame

Path	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
X	1x07	STRB_AUTO	0	0	INTR_REQX	INTR_CH			

STRB_AUTO Enable automatic strobe mode when FUNC_MODE = “1”
- 0 User strobe mode (default)
- 1 Automatic strobe mode

INTR_REQX Request to start the interrupt switch operation in display path
- 0 None operation (default)
- 1 Request to start the interrupt switch operation in display path

INTR_CH Channel number for interrupt switch operation

INTR_CH[3:2] represents the stage of cascaded chips for interrupt switch operation
- 0 Master chip (default)
- 1 1st slaver chip
- 2 2nd slaver chip
- 3 3rd slaver chip

INTR_CH[1:0] represents the channel number for interrupt switch operation
- 0 Channel 0 (default)
- 1 Channel 1
- 2 Channel 2
- 3 Channel 3

Path	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
X	1x08	MUX_OUT_CH0 *				MUX_OUT_CH1 *			
	1x09	MUX_OUT_CH2 *				MUX_OUT_CH3 *			

MUX_OUT_CH0 Channel information in current field/frame for interrupt switch operation

MUX_OUT_CH1 Channel information in next field/frame for interrupt switch operation

MUX_OUT_CH2 Channel information after 2 fields for interrupt switch operation

MUX_OUT_CH3 Channel information after 3 fields for interrupt switch operation

MUX_OUT_CH [3:2] represents the stage of cascaded chips for interrupt switch operation

0 Master chip (default)

1 1st slaver chip

2 2nd slaver chip

3 3rd slaver chip

MUX_OUT_CH [1:0] represents the channel number for interrupt switch operation

0 Channel 0 (default)

1 Channel 1

2 Channel 2

3 Channel 3

Path	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
X	1x0A	CHID_MUX_OUT *							

CHID_MUX_OUT Channel ID of current field/frame in interrupt switch operation

CHID_MUX_OUT [7] represents the channel ID latch enable pulse

0->1 Rising edge for channel ID Update

1->0 Falling edge after 16 clock * 18.5 ns from rising edge

CHID_MUX_OUT [6] represents the updated picture in interrupt switch operation

0 No Updated

1 Updated by new switching

CHID_MUX_OUT [5] represents the field mode in interrupt switch operation

0 Frame Mode

1 Field Mode

CHID_MUX_OUT [4] represents the analog switch path

0 Analog switch 0 path

1 Analog switch 1 path

CHID_MUX_OUT [3:2] represents the stage of cascaded chips for interrupt switch operation

0 Master chip

1 1st slaver chip

2 2nd slaver chip

3 3rd slaver chip

CHID_MUX_OUT [1:0] represents the channel number for interrupt switch operation

0 Channel 0

1 Channel 1

2 Channel 2

3 Channel 3

Path	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
X	1x0B	ZM_EVEN_OS		ZM_ODD_OS		FR_EVEN_OS		FR_ODD_OS	

ZM_EVEN_OS Even field offset coefficient when zoom is enabled

0 No Offset
1 + 0.25 Offset
2 + 0.5 Offset
3 + 0.75 Offset (default)

ZM_ODD_OS Odd field offset coefficient when zoom is enabled

0 No Offset
1 + 0.25 Offset (default)
2 + 0.5 Offset
3 + 0.75 Offset

FR_EVEN_OS Even field offset coefficient when the enhancement is enabled

0 No Offset
1 + 0.25 Offset (default)
2 + 0.5 Offset
3 + 0.75 Offset

FR_ODD_OS Odd field offset coefficient when the enhancement is enabled

0 No Offset
1 + 0.25 Offset
2 + 0.5 Offset
3 + 0.75 Offset (default)

Path	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
X	1x0C	ZMENA	0	ZMBNDCOL		ZMBNDEN	ZMAREAEN	ZMAREA	

ZMENA — Enable the zoom function.

0 Disable the zoom function (default)

1 Enable the zoom function

ZMBNDCOL — Define the boundary color for zoomed area

0 0% Black

1 25% Gray

2 75% Gray (default)

3 100% White

ZMBNDEN — Enable the boundary of zoomed area.

0 Disable the boundary of zoomed area (default)

1 Enable the boundary of zoomed area

ZMAREAEN — Enable the mark of zoomed area

0 Disable the mark of zoom area (default)

1 Enable the mark of zoom area

ZMAREA — Control the effect of zoomed area.

0 10 IRE Bright up for inside of zoomed area (default)

1 20 IRE Bright up for inside of zoomed area

2 10 IRE Bright up for outside of zoomed area

3 20 IRE Bright up for outside of zoomed area

Path	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
X	1x0D	ZOOMH							

ZOOMH Define the horizontal left point of zoomed area. 4 pixels/step.

0 Left end value (default)

: :

2) Right end value

Path	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
X	1x0E	ZOOMV							

ZOOMV Define the vertical top point of zoom area. 2 lines/step.

0 Top end value (default)

: :

120 Bottom end value for 60Hz, 525 lines system

: :

3) Bottom end value for 50Hz, 625 lines system

Path	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
X	1x0F	FRZ_FLD		BNDCOL		BGDCOL		BLKCOL	

FRZ_FLD — Select the image for freeze function or for last image capture on video loss.

0 Last image
1 Last image of 1 field before
2 Last image of 2 fields before (default)
3 Last image of 3 fields before

BNDCOL — Define the boundary color of channel.

0 0% Black
1 25% Gray
2 75% Gray
3 100% White (default)

Channel boundary color is changed according to this value when boundary is blinking.

0 100% White
1 100% White
2 0% Black
3 0% Black (default)

BGDCOL — Define the background color.

0 0% Black
1 40% Gray (default)
2 75% Gray
3 Blue (100% Amplitude 100% Saturation)

BLKCOL — Define the color of the blanked channel.

0 0% Black
1 40% Gray
2 75% Gray
3 Blue (100% Amplitude 100% Saturation) (default)

Path	CH	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
X	0	1x10	CH_EN	POP_UP	FUNC_MODE		DMCH_EN	DMCH_ PATH	RESERVED	
	1	1x18								
	2	1x20								
	3	1x28								

CH_EN — Enable the channel.
- 0 Disable the channel (default)
- 1 Enable the channel

POP_UP — Enable pop-up.
- 0 Disable pop-up (default)
- 1 Enable pop-up

FUNC_MODE — Select the operation mode.
- 0 Live mode (default)
- 1 Strobe mode
- 2-3 Switch mode

DMCH_EN — Enable the dummy channel when the corresponding channel is enabled.
- 0 Disable the dummy channel (default)
- 1 Enable the dummy channel

DMCH_PATH — Select the main or dummy channel when dummy channel is enabled.
- 0 Main channel for channel input (default)
- 1 Dummy channel for channel input

RESERVED — The following value should be set for proper operation.
- 1x10 0
- 1x18 1
- 1x20 2
- 1x28 3

Path	CH	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
X	0	1x11	RECALL_EN	FREEZE	H_MIRROR	V_MIRROR	ENHANCE	BLANK	BOUND	BLINK
	1	1x19								
	2	1x21								
	3	1x29								

RECALL_EN — Enable the recall function of main channel.
- 0 Disable the recall function (default)
- 1 Enable the recall function

FREEZE — Enable the freeze function of main channel.
- 0 Normal operation (default)
- 1 Enable the freeze function

H_MIRROR — Enable the horizontal mirroring function of main channel.
- 0 Normal operation (default)
- 1 Enable the horizontal mirroring function

V_MIRROR — Enable the vertical mirroring function of main channel.
- 0 Normal operation (default)
- 1 Enable the vertical mirroring function

ENHANCE — Enable the image enhancement function of main channel.
- 0 Normal operation (default)
- 1 Enable the image enhancement function

BLANK — Enable the blank of main channel.
- 0 Disable the blank (default)
- 1 Enable the blank

BOUND — Enable the channel boundary of main channel.
- 0 Disable the channel boundary
- 1 Enable the channel boundary (default)

BLINK — Enable the boundary blink of main channel when boundary is enabled.
- 0 Disable the boundary blink (default)
- 1 Enable the boundary blink

Path	CH	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
X	0	1x12	0	RECALL_ADDR						
	1	1x1A								
	2	1x22								
	3	1x2A								

RECALL_ADDR Define the recall address for main channel.

0-3 Reserved address. Do not use this value

4-15 Available address for 64M SDRAM

4-31 Available address for 128M SDRAM

4-63 Available address for 256M SDRAM

4-127 Available address for 512M SDRAM

Path	CH	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
X	0	1x13	RECALL_DM	FREEZE_DM	H_MIRROR_DM	V_MIRROR_DM	ENHANCE_DM	BLANK_DM	BOUND_DM	BLINK_DM
	1	1x1B								
	2	1x23								
	3	1x2B								

RECALL_DM Enable the recall function of dummy channel.
- 0 Disable the recall function (default)
- 1 Enable the recall function

FREEZE_DM Enable the freeze function of dummy channel.
- 0 Normal operation (default)
- 1 Enable the freeze function

H_MIRROR_DM Enable the horizontal mirroring function of dummy channel.
- 0 Normal operation (default)
- 1 Enable the horizontal mirroring function

V_MIRROR_DM Enable the vertical mirroring function of dummy channel.
- 0 Normal operation (default)
- 1 Enable the vertical mirroring function

ENHANCE_DM Enable the image enhancement function of dummy channel.
- 0 Normal operation (default)
- 1 Enable the image enhancement function

BLANK_DM Enable the blank of dummy channel.
- 0 Disable the blank (default)
- 1 Enable the blank

BOUND_DM Enable the channel boundary of dummy channel.
- 0 Disable the channel boundary
- 1 Enable the channel boundary (default)

BLINK_DM Enable the boundary blink of dummy channel when boundary is enabled.
- 0 Disable the boundary blink (default)
- 1 Enable the boundary blink

Path	CH	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
X	0	1x14	0	RECALL_ADDR_DM						
	1	1x1C								
	2	1x24								
	3	1x2C								

RECALL_ADDR_DM Define the recall address for dummy channel.

0-3	Reserved address. Do not use this value
4-15	Available address for 64M SDRAM
4-31	Available address for 128M SDRAM
4-63	Available address for 256M SDRAM
4-127	Available address for 512M SDRAM

Path	CH	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
X	0	1x15	0	0	0	0	0	0	0	0
	1	1x1D								
	2	1x25								
	3	1x2D								

This is reserved register.

For normal operation, the above value should be set in this register.

Path	CH	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
X	0	1x16	PB_AUTO_EN	0	PB_STOP	EVENT_PB	PB_CH_NUM			
	1	1x1E	0							
	2	1x26	0							
	3	1x2E	0							

PB_AUTO_EN Enable the auto strobe and auto cropping function for playback input

0 Disable the auto strobe/cropping function (default)

1 Enable the auto strobe/cropping function

PB_STOP Disable the auto strobe operation for playback input

0 Normal operation (default)

1 Disable the auto strobe operation for playback input

EVEN_PB Enable the event strobe function for playback input

0 Disable the event strobe function for playback input

1 Enable the event strobe function for playback input

PB_CH_NUM Select the channel number from playback input for display

PB_CH_NUM[3:2] represents the stage of cascaded chips

0 Master chip

1 1st slaver chip

2 2nd slaver chip

3 3rd slaver chip

PB_CH_NUM[1:0] represents the channel number

0 Channel 0

1 Channel 1

2 Channel 2

3 Channel 3

Path	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
X	1x2F	0	0	0	0	0	0	0	0

This is reserved register.

For normal operation, the above value should be set in this register.

Path	CH	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
X	0	1x30	PICHL							
	1	1x34								
	2	1x38								
	3	1x3C								
	0	1x40	PICHL_DM							
	1	1x44								
	2	1x48								
	3	1x4C								

PICHL Define the horizontal left position of channel

0 Left end (default)

: :

4) Right end

Path	CH	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
X	0	1x31	PICHR							
	1	1x35								
	2	1x39								
	3	1x3D								
	0	1x41	PICHR_DM							
	1	1x45								
	2	1x49								
	3	1x4D								

PICHR Define the horizontal right position of channel region

0 Left end (default)

: :

5) Right end

Path	CH	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
X	0	1x32	PICVT							
	1	1x36								
	2	1x3A								
	3	1x3E								
	0	1x42	PICVT_DM							
	1	1x46								
	2	1x4A								
	3	1x4E								

PICVT Define the vertical top position of channel region.

0 Top end (default)

: :

120 Bottom end for 60Hz system

: :

6) Bottom end for 50Hz system

Path	CH	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
X	0	1x33	PICVB							
	1	1x37								
	2	1x3B								
	3	1x3F								
	0	1x43	PICVB_DM							
	1	1x47								
	2	1x4B								
	3	1x4F								

PICVB Define the vertical bottom position of channel region.

0 Top end (default)

: :

120 Bottom end for 60Hz system

: :

7) Bottom end for 50Hz system

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1x50	MPPSET_X				MPPSET_Y			

MPPSET_X Select the function for MPPDEC_X[3:0] pins.

MPPSET_Y Select the function for MPPDEC_Y[3:0] pins.

For the following 0~5 value, MPPDEC0 ~ MPPDEC3 data comes from VIN0 ~ VIN3 and for 6~F value, comes from CH0 ~ CH3.

0 Input Mode (default)
1 Horizontal sync
2 Vertical sync
3 Field flag
4 Video loss
5 Motion detection
6 Blind detection
7 Strobe acknowledge of display path
8 Strobe acknowledge of record path
9 Not supported
A Not supported
B LSB 4 bits of Channel ID information in record path for switch mode
  [3:2] Stage of cascaded chips
  [1:0] Video input path
C MSB 4 bits of Channel ID information in record path for switch mode
  [3] Channel ID Latch Enable Pulse
  [2] New switching Information
  [1] Switch mode for Field or Frame
  [0] Analog Switch Path Information
D Not supported
E Channel Information of Queue in record path for switch mode
  [3:2] Stage of cascaded chips
  [1:0] Channel number
F Encoder Timing
  [3] HSENC
  [2] VSENC
  [1] FLDENC
  [0] LINK

Path	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Y	1x51	0	FRAME_OP	FRAME_FLD	DIS_MODE	0	0	SIZE_MODE	

FRAME_OP — Select the frame operation mode for record path.

0 Normal operation mode (Default)

1 Frame operation mode

DIS_MODE — Select the record mode depending on FRAME_OP.

When FRAME_OP = 0

0 Normal record mode (Default)

1 DVR normal record Mode

When FRAME_OP = 1

0 Frame record mode

1 DVR frame record mode

FRAME_FLD — Select the displayed field when FRAME_OP = “1”.

0 Odd field is displayed (default)

1 Even field is displayed

SIZE_MODE — Select the active pixel size per line

0 720 pixels (default)

1 704 pixels

2 640 pixels

3 640 pixels

Path	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Y	1x52	TBLINK	0	0	0	0	0	0	0

TBLINK Control the blink period of channel boundary.

0 Blink for every 30 fields (default)

1 Blink for every 60 fields

Path	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Y	1x53	0	0	0	0	0	0	0	0

This is reserved register.

For normal operation, the above value should be set in this register.

Path	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Y	1x54	0	STRB_FLD		DUAL_PAGE	STRB_REQ			

STRB_FLD — Control the field mode for strobe operation.

0 Capture odd field only (default)

1 Capture even field only

2 Capture first field of any field

3 Capture frame

DUAL_PAGE — Set dual page mode.

0 Normal strobe operation for each channel (default)

1 Enable the dual page operation

STRB_REQ — Request strobe operation.

STRB_REQ[3:0] represents the channel 3 to 0

0 None operation (default)

1 Request to start strobe operation

Path	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Y	1x55	NOVID_MODE		0	CH_START	0	MEM_OP_ _EN	INVALID_MODE	

NOVID_MODE Select the indication method for no video detected channel

0 Bypass (default)

1 Capture last image

2 Blanked with blank color

3 Capture last image and blink channel boundary

CH_START Enable the digital channel ID in horizontal boundary of channel

0 Disable the digital channel ID in horizontal boundary (default)

1 Enable the digital channel ID in horizontal boundary

MEM_OP_EN Disable 4 channel record output mode

0 Enable 4 channel record output mode (default)

1 Disable 4 channel record output mode

INVALID_MODE No channel area indication

In horizontal and vertical active region

0 Background layer with background color (default)

1 Y = 0, Cb/Cr = 128

2 Y/Cb/Cr = 0

3 Y/Cb/Cr = 0

In horizontal and vertical blanking region

0 Y = 16, Cb/Cr = 128 (default)

1 Background layer with background color

2 Y = 0, Cb = {0, F, V, 0, Cascade, linenum[8:7]}, Cr = {0, linenum[6:0]}

3 Y/Cb/Cr = 0

Path	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Y	1x56	MUX_MODE	TRIG_MODE	MUX_FLD		PIN_TRIG_MD		0	0

MUX_MODE Define the switch mode.
- 0 Switch channel with still picture (default)
- 1 Switch channel with live picture

TRIG_MODE Define the switch trigger mode.
- 0 MUX with external trigger from host (default)
- 1 MUX with internal trigger

MUX_FLD Control the capturing field for switch operation.
- 0 Capture odd field only (default)
- 1 Capture even field only
- 2 Capture frame
- 3 Capture frame

PIN_TRIG_MD Select the triggering input when external trigger mode
- 0 Triggering by EXT_TRIG register
- 1 Triggering by positive edge of TRIGGER pin
- 2 Triggering by negative edge of TRIGGER pin
- 3 Triggering by both positive and negative edge of TRIGGER pin

Path	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Y	1x57	STRB_AUTO	QUE_SIZE						

STRB_AUTO Enable for Auto Strobe Mode for FUNC_MODE = 1
- 0 Auto Strobe Disable (default)
- 1 Auto Strobe Enable

QUE_SIZE Define the actual using queue size.
- 0 Queue size = 1 (default)
- : :
- 8) Queue size = 128

Path	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Y	1x58	QUE_PERIOD [7:0]							
	1x59	QUE_PERIOD [9:8]		EXT_TRIG	INTR_REQY	MUX_WR_CH			

QUE_PERIOD Trigger period for internal trigger mode.

0 Trigger period = 1 field (default)

: :

1023 Trigger period = 1024 fields

EXT_TRIG Make trigger when TRIG_MODE = “0”.

0 None operation (default)

1 Request to start MUX with external trigger mode

INTR_REQY Request to start the switch operation with interrupt in record path

0 None operation (default)

1 Request to start the switch operation with interrupt

MUX_WR_CH Channel number to be written in internal MUX queue or in interrupt trigger.

MUX_WR_CH[3:2] stands for stage of cascaded chips

0 Master chip (default)

1 1st slaver chip

2 2nd slaver chip

3 3rd slaver chip

MUX_WR_CH[1:0] stands for channel number

0 Channel 0 (default)

1 Channel 1

2 Channel 2

3 Channel 3

Path	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Y	1x5A	QUE_WR	QUE_ADDR						

QUE_WR Control to write internal queue data.

0 None operation (default)

1 Request to start writing QUE_CH in internal queue of QUE_ADDR

QUE_ADDR Define the queue address.

0 1st queue address (default)

: :

9) 128th queue address

Path	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Y	1x5B	0	Q_POS_RD_CTL	Q_DATA_RD_CTL		MUX_SKIP_EN	ACCU_TRIG	QUE_CNT_RST	QUE_POS_RST
	1x5C	MUX_SKIP_CH[15:8]							
	1x5D	MUX_SKIP_CH[7:0]							

Q_POS_RD_CTL Control the read mode of the QUE_ADDR
- 0 Current queue address of internal queue (default)
- 1 Written value into the QUE_ADDR

Q_DATA_RD_CTL Control the read mode of the MUX_WR_CH
- 0 Current queue data of internal queue (default)
- 1 Written value into the MUX_WR_CH
- 2,3 Queue data at the QUE_ADDR

MUX_SKIP_EN Enable the switch skip mode
- 0 Disable the switch skip mode
- 1 Enable the switch skip mode

ACCU_TRIG Adjust the switch timing in external triggering via the TRIGGER pin
- 0 Output is delayed in 4 fields from triggering (default)
- 1 Output is matched with triggering

QUE_CNT_RST Reset the internal field counter to count queue period.
- 0 None operation (default)
- 1 Reset the field counter

QUE_POS_RST Reset the queue address.
- 0 None operation (default)
- 1 Reset the queue address and restart address

MUX_SKIP_CH Define the switch skip channel

MUX_SKIP_CH[15:0] stands for channel 15 ~ 0 including cascaded chip
- 0 Normal operation (default)
- 1 Skip channel

Path	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Y	1x5E	CHID_MUX_OUT *							

Notes "*" stand for read only register

CHID_MUX_OUT Channel ID of current field/frame in switch operation

CHID_MUX_OUT [7] represents the channel ID latch enable pulse

0->1 Rising edge for updating the channel ID

1->0 Falling edge after 16 clock * 18.5 ns from rising edge

CHID_MUX_OUT [6] represents Updated Picture in switch operation

0 No Updated

1 Updated by New Switching

CHID_MUX_OUT [5] represents the field mode in switch operation

0 Frame mode

1 Field mode

CHID_MUX_OUT [4] represents analog switching path

0 Analog switching 0 path

1 Analog switching 1 path

CHID_MUX_OUT [3:2] represents the stage of cascaded chip for switch operation

0 Master chip

1 1st slaver chip

2 2nd slaver chip

3 3rd slaver chip

CHID_MUX_OUT [1:0] represents the channel number for switch operation

0 Channel 0

1 Channel 1

2 Channel 2

3 Channel 3

Path	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Y	1x5F	FRZ_FLD		BNDCOL		BGDCOL		BLKCOL	

FRZ_FLD Select the image with freeze function or with last capture on video loss.

0 Last image
1 Last image of 1 field before
2 Last image of 2 fields before (default)
3 Last image of 3 fields before

BNDCOL Define the boundary color of channel.

0 0% Black
1 25% Gray
2 75% Gray
3 100% White (default)

Channel boundary color is changed according to this value when boundary is blinking.

0 100% White
1 100% White
2 0% Black
3 0% Black (default)

BGDCOL Define the background color.

0 0% Black
1 40% Gray (default)
2 75% Gray
3 Blue (100% Amplitude 100% Saturation)

BLKCOL Define the color for blanked channel.

0 0% Black
1 40% Gray
2 75% Gray
3 Blue (100% Amplitude 100% Saturation) (default)

Path	CH	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Y	0	1x60	CH_EN	POP_UP	FUNC_MODE		0	0	DEC_PATH_Y	
	1	1x63								
	2	1x66								
	3	1x69								

CH_EN Enable the channel.

0 Disable the channel (default)

1 Enable the channel

POP_UP Enable pop-up.

0 Disable pop-up (default)

1 Enable pop-up

FUNC_MODE Select the operation mode.

0 Live mode (default)

1 Strobe mode

2-3 Switch mode

DEC_PATH_Y Select the video input for each channel.

0 Video input from internal video decoder on VIN0 pins (default)

1 Video input from internal video decoder on VIN1 pins

2 Video input from internal video decoder on VIN2 pins

3 Video input from internal video decoder on VIN3 pins

Path	CH	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Y	0	1x61	0	FREEZE	H_MIRROR	V_MIRROR	ENHANCE	BLANK	BOUND	BLINK
	1	1x64								
	2	1x67								
	3	1x6A								

FREEZE — Enable the freeze function of main channel.
- 0 Normal operation (default)
- 1 Enable the freeze function

H_MIRROR — Enable the horizontal mirroring function of main channel.
- 0 Normal operation (default)
- 1 Enable the horizontal mirroring function

V_MIRROR — Enable the vertical mirroring function of main channel.
- 0 Normal operation (default)
- 1 Enable the vertical mirroring function

ENHANCE — Enable the image enhancement function of main channel.
- 0 Normal operation (default)
- 1 Enable the image enhancement function

BLANK — Enable the blank of main channel.
- 0 Disable the blank (default)
- 1 Enable the blank

BOUND — Enable the channel boundary of main channel.
- 0 Disable the channel boundary
- 1 Enable the channel boundary (default)

BLINK — Enable the boundary blink of main channel when boundary is enabled.
- 0 Disable the boundary blink (default)
- 1 Enable the boundary blink

Path	CH	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Y	0	1x62	0	0	0	0	0	0	0	0
	1	1x65								
	2	1x68								
	3	1x6B								

This is reserved register.
For normal operation, the above value should be set in this register.

Path	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Y	1x6C	PIC_SIZE3		PIC_SIZE2		PIC_SIZE1		PIC_SIZE0	

PIC_SIZE Define the channel size when normal record mode or DVR normal record mode

0 QUAD size
1 Full size for horizontal and Half size for vertical size
2 Half size for horizontal and Full size for vertical size
3 Full size

When Frame record mode or DVR frame record mode

0 CIF size (Half size for horizontal and Full size for vertical size)
1 Full size in frame record mode or DVR frame record mode
2/3 Not Available

Path	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Y	1x6D	PIC_POS3		PIC_POS2		PIC_POS1		PIC_POS0	

PIC_POS

Define the channel start position

When Normal record mode

0 No offset for both horizontal and vertical direction
1 Half offset for horizontal and no offset for vertical direction
2 No offset for horizontal and half offset for vertical direction
3 Half offset for horizontal and half offset for vertical direction

When Frame record mode

0 No offset for both horizontal and vertical direction
1 Half offset for horizontal and no offset for vertical direction
2 No offset for horizontal and field offset for vertical direction
3 Half offset for horizontal and field offset for vertical direction

When DVR normal record mode

0 No offset for both horizontal and vertical direction
1 1/4 Quarter offset for vertical direction
2 Half offset for vertical direction
3 3/4 Quarter offset for vertical direction

When DVR Frame record mode

0 No offset for both horizontal and vertical direction
1 Half offset for vertical direction
2 Field offset for vertical direction
3 Field and half offset for vertical direction

Path	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Y	1x6E	MUX_OUT_CH0 *				MUX_OUT_CH1 *			
	1x6F	MUX_OUT_CH2 *				MUX_OUT_CH3 *			

MUX_OUT_CH0 Channel Information in current field/frame for switch operation

MUX_OUT_CH1 Channel Information in next field/frame for switch operation

MUX_OUT_CH2 Channel Information after 2 fields for switch operation

MUX_OUT_CH3 Channel Information after 3 fields for switch operation

MUX_OUT_CH [3:2] represents the stage of cascaded chips

0 Master chip (default)

1 1st slaver chip

2 2nd slaver chip

3 3rd slaver chip

MUX_OUT_CH [1:0] represents the channel number

0 Channel 0 (default)

1 Channel 1

2 Channel 2

3 Channel 3

Path	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Y	1x70	POS_CTL_EN	POS_TRIG_MODE	POS_TRIG	POS_INTR	0	POS_RD_CTL	POS_DATA_RD_CTL	

POS_CTL_EN Enable the position/popup control

0 Disable the position/popup control (default)

1 Enable the position/popup control

POS_TRIG_MODE Select the position/popup trigger mode

0 External trigger mode (default)

1 Internal trigger mode

POS_TRIG Request the external trigger on external trigger mode

0 None Operation (default)

1 Request to start position/popup control in external trigger mode

POS_INTR Request to start position/popup control with interrupt

0 None Operation (default)

1 Request to start position/popup control with interrupt

INTR_REQ Request interrupt MUX

0 None operation (default)

1 Request to start MUX with interrupt

1 Request to start position/popup control with interrupt

POS_RD_CTL Control the read mode for the POS_QUE_ADDR

0 Current queue address for internal position/popup queue (default)

1 Written value into the POS_QUE_ADDR

POS_DATA_RD_CTL Control the read mode for the POS_CH

0 Current Queue Data for Internal Queue (default)

1 Written POS_CH value

2 Queue Data of the POS_QUE_ADDR

3 Queue Data of the POS_QUE_ADDR

Path	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Y	1x71	POS_QUE_PER[9:8]		POS_FLD_MD	POS_QUE_SIZE				
	1x72	POS_QUE_PER [7:0]							

POS_QUE_SIZE Select the position/popup queue size

0 Queue size = 1 (default)

: :

10) Queue size = 32

POS_FLD_MD Select the position/popup queue period unit

0 Frame (default)

1 Field

POS_QUE_PER Trigger period for internal trigger mode.

0 Trigger period = 1 field or frame (default)

: :

11) Trigger period = 1024 fields or frames

Path	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Y	1x73	POS_CH0				POS_CH1			
	1x74	POS_CH2				POS_CH3			

POS_CH Define the channel for each region

POS_CH0 stands for No offset region of both H/V

POS_CH1 stands for half offset of H

POS_CH2 stands for half offset of V

POS_CH3 stands for half offset of both H/V

POS_CH [3:2] stands for the order of cascade chips

0 Master chip (default)

1 1st slaver chip

2 2nd slaver chip

3 3rd slaver chip

POS_CH [1:0] stands for the channel number

0 Channel 0 (default)

1 Channel 1

2 Channel 2

3 Channel 3

Path	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Y	1x75	POS_QUE_WR	POS_CNT_RST	POS_QUE_RST	POS_QUE_ADDR				

POS_QUE_WR Control to write internal position queue data
0 None operation (default)
1 Write data into the POS_CH register at the POS_QUE_ADDR

POS_CNT_RST Reset the internal field counter to count queue period for position queue.
0 None operation (default)
1 Reset the field counter

POS_QUE_RST Reset the queue address for position queue.
0 None operation (default)
1 Reset the queue address and restart address

POS_QUE_ADDR Define the queue address.
0 1st queue address (default)
: :
12) 32nd queue address

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1x76	FLD_OP				DVR_IN			

FLD_OP Enable Field to Frame Conversion mode.
FLD_OP[3:0] stands for the channel 3 to channel 0
0 Normal operation (default)
1 Enable Field to Frame Conversion mode

DVR_IN Enable DVR to Normal Conversion mode.
DVR_IN[3:0] stand for the channel 3 to channel 0
0 Normal operation (default)
1 DVR to Normal Conversion mode

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1x77	0	0	0	0	0	0	0	0

This is reserved register.
For normal operation, the above value should be set in this register.

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1x78	0	0	0	0	0	IRQPOL	IRQRPT	0

IRQPOL Select the IRQ polarity.
0 Active high (default)
1 Active low

IRQRPT Select the IRQ mode.
IRQ pin maintains the state “1” until the interrupt request is cleared (default)
Interrupt request is repeated with 5msec period via IRQ pin when interrupt is not cleared in long time.

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1x79	IRQENA_NOVID				IRQENA_MOTION			

IRQENA_NOVID Interrupt enable for corresponding video-loss detection.
IRQENA_NOVID[3:0] stand for VIN3 to VIN0.
0 Interrupt is disabled (default)
1 Interrupt is enabled

IRQENA_MOTION Interrupt enable for corresponding motion detection.
IRQENA_MOTION [3:0] stand for VIN3 to VIN0.
0 Interrupt is disabled (default)
1 Interrupt is enabled

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1x7A	IRQCLR_NOVID				IRQCLR_MDBD			

IRQCLR_NOVID Setting “1” to clear interrupt request for corresponding video-loss detection. This bit is cleared by itself in a few clocks after setting “1”.
IRQCLR_NOVID [3:0] stand for VIN3 to VIN0.

IRQCLR_MDBD Setting “1” to clear interrupt request for corresponding motion and blind detection. This bit is cleared by itself in a few clocks after setting “1”.
IRQENA_MD_BD [3:0] stand for VIN3 to VIN0.

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1x7B	DET_NOVID *				DET_MOTION *			

Notes "*" stand for read only register

DET_NOVID Status of video loss detection.
DET_NOVID[3:0] stand for VIN3 to VIN0.
0 Video is alive
1 Video loss is detected

DET_MOTION Status of motion detection.
DET_MOTION[3:0] stand for VIN3 to VIN0.
0 No motion
1 Motion is detected

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1x7C	IRQENA_BLIND				DET_BLIND *			

Notes "*" stand for read only register

IRQENA_BLIND Interrupt enable for corresponding blind detection.
IRQENA_BLIND[3:0] stand for VIN3 to VIN0.
0 Interrupt is disabled (default)
1 Interrupt is enabled

DET_BLIND Status of blind detection.
DET_BLIND[3:0] stand for VIN3 to VIN0.
0 No blinded video
1 Blind video is detected

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1x7D	MCLK_FR_Y		MCLK_PH_Y	0	MCLK_FR_X		MCLK_PH_X	0

MCLK_FR_X Control the clock frequency of the CLK54MEMX Pin

MCLK_FR_Y Control the clock frequency of the CLK54MEMY Pin

0 54 MHz (default)

1 27 MHz

2 27 MHz

3 27 MHz

MCLK_PH_X Control the clock phase of the CLK54MEMX pin

MCLK_PH_Y Control the clock phase of the CLK54MEMY pin

0 None operation (default)

1 Phase Inverting

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1x7E	MCLKDEL_Y				MCLKDEL_X			

MCLKDEL_X Control the clock delay of the CLK54MEMX pin

MCLKDEL_Y Control the clock delay of the CLK54MEMY pin

The delay can be controlled by 1ns.

The default value is 0.

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1x7F	MEM_INIT	0	1	0	0	0	0	1

MEM_INIT Initialize operation mode of SDRAM.

This is cleared by itself after setting “1”.

0 None operation (default)

1 Request to start initializing operation mode of SDRAM

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1x80	ENC_IN_X		ENC_IN_Y		CCIR_IN_X		CCIR_IN_Y	

ENC_IN

Select the video data input of video encoder for analog output.

0 Display path video data without OSD and mouse overlay (default)

1 Display path video data with OSD and mouse overlay

2 Record path video data without OSD and mouse overlay

3 Record path video data with OSD and mouse overlay

CCIR_IN

Select the video data input of ITU-R BT 656 encoder for digital output.

0 Display path video data without OSD and mouse overlay (default)

1 Display path video data with OSD and mouse overlay

2 Record path video data without OSD and mouse overlay

3 Record path video data with OSD and mouse overlay

When realtime output mode for VDOUTY Pin (1x83, BYPASS_Y = 11b),
Select the video data output of VDOUTY Pin.
When Timing Multiplexed with 54MHz via CCIR_OUT_Y[1] = 1

0/1 Video Input 0/1

2/3 Video Input 2/3

When 27MHz output mode via CCIR_OUT_SEL_Y[1] = 0

0 Video Input 0

1 Video Input 1

2 Video Input 2

3 Video Input 3

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1x81	DAC_PD_YX	DAC_OUT_YX			DAC_PD_CX	DAC_OUT_CX		
1x82	DAC_PD_YY	DAC_OUT_YY			DAC_PD_CY	DAC_OUT_CY		

DAC_PD

Enable the power down of DAC.

0 Normal operation (default)

1 Enable power down of DAC

DAC_OUT

Define the analog video format.

DAC_OUT[2] represents the selected path for output.

0 Display path (default)

1 Record path

DAC_OUT[1:0] represents the selected mode for output.

0 No Output (default)

1 CVBS

2 Luminance

3 Chrominance

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1x83	0	CCIR_601	CCIR_OUT_X		BYPASS_Y		CCIR_OUT_Y	

CCIR_601 Define the digital data output format.

0 ITU-R BT.656 mode (default)

1 ITU-R BT.601 mode

BYPASS_Y Define the digital data output format for VDOUTY Pin.

13) Normal Operation (default)

1 Reserved

2 Reserved

3 Decoder Data Bypass for Realtime Output

CCIR_OUT Define the mode of ITU-R BT.656 digital output.

The default value is “0” for CCIR_OUT_X, but “1” for CCIR_OUT_Y.

When ITU-R BT.656 is selected (CCIR_601 = 0)

0 Display path video data with single output mode (27MHz)

1 Record path video data with single output mode (27MHz)

2 Display and Record path video data with dual output mode (54MHz)

3 Record and Display path video data with dual output mode (54MHz)

When ITU-R BT.601 is selected (CCIR_601 = 1)

0 Display path video data with single output mode (13.5MHz)

1 Record path video data with single output mode (13.5MHz)

2 Dual output mode with Display and Record path video data (27MHz)

3 Dual output mode with Record and Display path video data (27MHz)

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1x84	ENC_ MODE	CCIR_LMT	ENC_VS	ENC_FLD	CCIR_ FLDPOL	ENC_ HSPOL	ENC_ VSPOL	ENC_ FLDPOL

ENC_MODE Define the operation mode of video encoder.
- 0 Slave mode operation (default)
- 1 Master mode operation

CCIR_LMT Control the data range of ITU-R BT 656 output.
- 0 Bypass (default)
- 1 Data range is limited to 1 ~ 254 code

ENC_VS Define the vertical sync detection type.
- 0 Detect vertical sync from VSENC pin (default)
- 1 Detect vertical sync from combination of HSENC and FLDEN pins

ENC_FLD Define the field polarity detection type
- 0 Detect field polarity from FLDENC pin (default)
- 1 Detect field polarity from combination of HSENC and VSENC pins

CCIR_FLDPOL Control the field polarity of ITU-R BT 656 output.
- 0 High for even field (default)
- 1 High for odd field

ENC_HSPOL Control the horizontal sync polarity.
- 0 Active low (default)
- 1 Active high

ENC_VSPOL Control the vertical sync polarity.
- 0 Active low (default)
- 1 Active high

ENC_FLDPOL Control the field polarity.
- 0 Even field is high (default)
- 1 Odd field is high

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1x85	ENC_VSOFF		ENC_VSDEL					

ENC_VSOFF Compensate the field offset for first active video line.

0 Apply same ENC_VSDEL for odd and even field (default)

1 Apply {ENC_VSDEL+1} for odd and ENC_VSDEL for even field

2 Apply ENC_VSDEL for odd and {ENC_VSDEL +1} for even field

3 Apply ENC_VSDEL for odd and {ENC_VSDEL +2} for even field

ENC_VSDEL Control the line delay of vertical sync from active video by 1 line/step.

0 No delayed

: :

32 32 line delay (default)

: :

14) 63 line delay

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1x86	ENC_HSDEL[9:2]							
1x87	ENC_HSDEL[1:0]		0	ACTIVE_VDEL				

ENC_HSDEL Control the pixel delay of horizontal sync from active video by 1/2 pixel/step.

0 No delayed

: :

128 64 pixel delay (default)

: :

1023 255 pixel delay

ACTIVE_VDEL Control the line delay of active video by 1 line/step.

0 - 11 Lines delayed

: :

12 0 Line delayed (default)

: :

15) + 13 Lines delayed

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1x88	0	CCIR_STD	ACTIVE_HDEL					

CCIR_STD Select ITU-R BT656 standard format for 60Hz system.

0 240 line for odd and even field (Default)

1 244 line for odd and 243 line for even field (ITU-R BT.656 standard)

ACTIVE_HDEL Control the pixel delay of active video by 1 pixel/step.

0 - 32 Pixel delay

: :

32 0 Pixel delay (default)

: :

16) + 31 Pixel delay

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1x89	ENC_FSC		0	0	1	ENC_ PHALT	ENC_ ALTRST	ENC_ PED

ENC_FSC Set color sub-carrier frequency for video encoder.

0 3.57954545 MHz (default)

1 4.43361875 MHz

2 3.57561149 MHz

3 3.58205625 MHz

ENC_PHALT Set phase alternation.

0 Disable phase alternation for line-by-line (default)

1 Enable phase alternation for line-by-line

ENC_ALTRST Reset phase alternation for every 8 field

0 Disable phase alternation reset for every 8 field (default)

1 Enable phase alternation reset for every 8 field

ENC_PED Set 7.5IRE for pedestal level

0 Disable 7.5 IRE for pedestal level

1 Enable 7.5 IRE for pedestal level (default)

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1x8A	ENC_CBW_X		ENC_YBW_X		ENC_CBW_Y		ENC_YBW_Y	

ENC_CBW Control the chrominance bandwidth of video encoder.

0 0.8 MHz

1 1.15 MHz

2 1.35 MHz (default)

3 1.35 MHz

ENC_YBW Control the luminance bandwidth of video encoder.

0 Narrow bandwidth

1 Narrower bandwidth

2 Wide bandwidth (default)

3 Middle band width

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1x8B	0	0	ENC_ BAR_X	ENC_ CKILL_X	0	0	ENC_ BAR_Y	ENC_ CKILL_Y

ENC_BAR Enable the test pattern output.

0 Normal operation (default)

1 Internal color bar with 100% amplitude 100 % saturation

ENC_CKILL Enable the color killing function

0 Normal operation (default)

1 Color is killed

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1x8C	ENC_HS_LINK	0	0	0	VDOUTY_MODE	HOUT *	VOUT *	FOUT*

Notes "*" stand for read only register

ENC_HS_LINK Control the function of the HSENC pin.
- 0 Encoder Horizontal Sync (default)
- 1 Link pin for cascade connection

VDOUTY_MODE Control the I/O direction of the VDOUTY pins.
- 0 Input mode for 4 ch playback input (default)
- 1 Output mode for normal application

HOUT Horizontal sync for Encoder Timing

VOUT Vertical sync for Encoder Timing

FOUT Field polarity for Encoder Timing

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1x8D	ECLK_FR_Y		ECLK_PH_Y		ECLK_FR_X		ECLK_PH_X	

ECLK_FR_X Control the clock frequency of CLK27ENCX pin

ECLK_FR_Y Control the clock frequency of CLK27ENCY pin

0 54MHz

1 27MHz

2 27MHz

3 13.5MHz

ECLK_PH_X Control the clock phase of CLK27ENCX pin

ECLK_PH_Y Control the clock phase of CLK27ENCY pin

0 None operation (default)

1 None operation when clock frequency is not 13.5MHz
90 degree shift when clock frequency is 13.5MHz

2 Phase Inverting

3 Phase Inverting when clock frequency is not 13.5MHz
270 degree shift when clock frequency is 13.5MHz

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1x8E	ECLKDEL_Y				ECLKDEL_X			

ECLKDEL_X Control the clock delay of CLK27ENCX pin

ECLKDEL_Y Control the clock delay of CLK27ENCY pin

The delay can be controlled by 1ns.

The default value is 0.

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1x90	FONT_WR_DATA[63:56]							
1x91	FONT_WR_DATA[55:48]							
1x92	FONT_WR_DATA[47:40]							
1x93	FONT_WR_DATA[39:32]							
1x94	FONT_WR_DATA[31:24]							
1x95	FONT_WR_DATA[23:16]							
1x96	FONT_WR_DATA[15:8]							
1x97	FONT_WR_DATA[7:0]							

FONT_WR_DATA Font data for 1 line of 1 font.
The default value is 0.

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1x98	0	FONT_WR_INDEX						

FONT_WR_INDEX Define the font index.
0 Index 0 (default)
: :
17) Index 127

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1x99	FONT_WR_PAGE				FONT_WR_LINE			

FONT_WR_PAGE Define the font page to be written.
0 Page 0 (default)
: :
15 Page 15

FONT_WR_LINE Define the font line to be written.
0 1st Line (default)
: :
18) 16th Line

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1x9A	FONT_ REQ_X	FONT_ REQ_Y	0	0	0	FONT_WR_TYPE		FONT_ WR_FLD

FONT_REQ Request to start writing font into SDRAM.
This bit is cleared by itself after a few clocks.
0 None operation (default)
1 Request to start writing font

FONT_WR_TYPE Select the font type to be written
0 128 index mode
1 85 index mode
2 64 index mode

FONT_WR_FLD Select the font field to be written.
0 Odd field (default)
1 Even field

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1x9B	CHAR_ PATH	CHAR_WR_MODE		CHAR_VLOC				

CHAR_PATH Select the path of the display RAM to write character attribute.
0 Write the display RAM of display path (default)
1 Write the display RAM of record path

CHAR_WR_MODE Select the write mode of the display RAM.
0 Write Character Attribute
1 Write 1 Character Line Attribute
2 Write All Character Line Attribute
3 Write All Character Line Attribute

CHAR_VLOC Define the vertical position of the displayed character.
0 1st character in the vertical direction (default)
: :
19) 29th character in the vertical direction

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1x9C	0		CHAR_RD_FLD		CHAR_RD_PAGE			
	0		CHAR_VF_SIZE		CHAR_HF_SIZE			
	0		CHAR_HLOC					

Notes 1. The property of 1x9C address depends on CHAR_WR_MODE value.
2. The data property of 1x9C depends on order of writing.

FONT_RD_FLD Define font field to be displayed
0 Character is not displayed (default)
1 Even field font is used for both odd and even field
2 Odd field font is used for both odd and even field
3 Both odd and even field font is used for frame display

FONT_RD_PAGE Define the font page to be displayed
0 Page 0 (default)
: :
15 Page 15

FONT_VF_SIZE Define the dot size of font for vertical direction
0 10 Line (default)
: :
3 16 Line

FONT_HF_SIZE Define the horizontal pixel resolution and size of font
0 8 dots with 360 pixels resolution (default)
1 10 dots with 360 pixels resolution
2 12 dots with 360 pixels resolution
3 14 dots with 360 pixels resolution
4 16 dots with 360 pixels resolution
5 16 dots with 720 pixels resolution
6 20 dots with 720 pixels resolution
7 24 dots with 720 pixels resolution
8 28 dots with 720 pixels resolution
9 - 32 dots with 720 pixels resolution

CHAR_HLOC Define the horizontal position of displayed character.
0 1st character horizontally (default)
: :
20) 45th character horizontally

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1x9D	0	0	0	0	MIX	BLINK	CLASS3_COL	
	FONT_TYPE	CHAR_INDEX						

Notes 1. It should be written in pairs because the data of 1x9D consist of 2 bytes.
2. It is written into display RAM with CHAR_HLOC, CHAR_VLOC, and CHAR_PATH.

MIX — Enable the alpha blending
- 0 Disable the alpha blending
- 1 Enable the alpha blending with video data

BLINK — Enable the Blink
- 0 Disable the blink
- 1 Enable the blink

CLASS3_COL — Select the color of class3
- 0 CLASS3COL0 in register 1xA7~1xAA
- 1 CLASS3COL1 in register 1xA7~1xAA
- 2 CLASS3COL2 in register 1xA7~1xAA
- 3 CLASS3COL3 in register 1xA7~1xAA

FONT_TYPE — Select the font type
- 0 Character type
- 1 Bitmap type

CHAR_INDEX — Select the font index
- 0 1st index
- : :
- 21) 128th index

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1xA0	RAMCLR_X	RAMCLR_Y	BLK_TIME		CLASS0 ENA_X	CLASS0 ENA_Y	B_CLASS0 DIS_X	B_CLASS0 DIS_Y

RAMCLR — Clear the display RAM.
This bit is cleared by itself after finishing display RAM clear.
0 None operation (default)
1 Request to start clearing display RAM

BLK_TIME — Select the blink period
0 0.25 second (default)
1 0.5 second
2 1 sec
3 2 sec

CLASS0ENA — Enable class 0 in character mode.
0 Disable class 0 (default)
1 Enable class 0

B_CLASS0DIS — Disable class 0 in bitmap mode
0 Enable class 0 (default)
1 Disable class 0

Path	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
X	1xA1	CHAR_VSPC				CHAR_HSPC			
Y	1xA3								

CHAR_VSPC Vertical space in the displayed characters.

0 No Space (default)

: :

15 15 Lines space

CHAR_HSPC Horizontal space in the displayed characters.

0 No space (default)

: :

22) 30 Pixels space

Path	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
X	1xA2	CHAR_VDEL				CHAR_HDEL			
Y	1xA4								

CHAR_VDEL Vertical offset to first displayed character.

0 No offset (default)

: :

15 15 Lines offset

CHAR_HDEL Horizontal offset to first displayed character.

0 No offset (default)

: :

23) 30 Pixels offset

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1xA5	CHAR_MIX_C				CHAR_MIX_B			

CHAR_MIX_C Control the alpha blending mode with video data in character mode.
CHAR_MIX_C[3:0] stands for class 3 to 0.
0 Disable alpha blending function (default)
1 Enable alpha blending function

CHAR_MIX_B Control the alpha blending mode with video data in bitmap mode.
CHAR_MIX_B[3:0] stands for class 3 to 0.
0 Disable alpha blending function (default)
1 Enable alpha blending function

The alpha blending Level is controlled via the ALPHA_OSD (1xBA) register.

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1xA6	CHAR_BLK_C				CHAR_BLK_B			

CHAR_BLK_C Control the blink for character mode.
CHAR_BLK_C[3:0] stands for class 3 to 0.
0 Disable blink function (default)
1 Enable blink function

CHAR_BLK_B Control the blink for bitmap mode.
CHAR_BLK_B[3:0] stands for class 3 to 0.
0 Disable blink function (default)
1 Enable blink function

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1xA7	CLASS3COL1_C				CLASS 3COL0_C			
1xA8	CLASS3COL3_C				CLASS 3COL2_C			
1xA9	CLASS3COL1_B				CLASS 3COL0_B			
1xAA	CLASS3COL3_B				CLASS 3COL2_B			
1xAB	CLASS2COL_C				CLASS2COL_B			
1xAC	CLASS1COL_C				CLASS1COL_B			
1xAD	CLASS0COL_C				CLASS0COL_B			

CLASS3COL0_C Color selection 0 of class 3 for character mode

CLASS3COL1_C Color selection 1 of class 3 for character mode

CLASS3COL2_C Color selection 2 of class 3 for character mode

CLASS3COL3_C Color selection 3 of class 3 for character mode

CLASS3COL0_B Color selection 0 of class 3 for bitmap mode

CLASS3COL1_B Color selection 1 of class 3 for bitmap mode

CLASS3COL2_B Color selection 2 of class 3 for bitmap mode

CLASS3COL3_B Color selection 3 of class 3 for bitmap mode

CLASS2COL_C Color selection of class 2 for character mode

CLASS2COL_B Color selection of class 2 for bitmap mode

CLASS1COL_C Color selection of class 1 for character mode

CLASS1COL_B Color selection of class 1 for bitmap mode

CLASS0COL_C Color selection of class 0 for character mode

CLASS0COL_B Color selection of class 0 for bitmap mode

Color selection table

0 White (75% Amplitude 100% Saturation) (default)
1 Yellow (75% Amplitude 100% Saturation)
2 Cyan (75 % Amplitude 100 Saturation)
3 Green (75% Amplitude 100% Saturation)
4 Magenta (75% Amplitude 100% Saturation)
5 Red (75% Amplitude 100% Saturation)
6 Blue (75% Amplitude 100% Saturation)
7 0% Black
8 100% White
9 50% Gray
10 25% Gray
11 Blue (75% Amplitude 75% Saturation)
12 Defined by CLUT0
13 Defined by CLUT1
14 Defined by CLUT2
15 Defined by CLUT3

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1xAE	CLUT0_Y							
1xAF	CLUT0_CB							
1xB0	CLUT0_CR							
1xB1	CLUT1_Y							
1xB2	CLUT1_CB							
1xB3	CLUT1_CR							
1xB4	CLUT2_Y							
1xB5	CLUT2_CB							
1xB6	CLUT2_CR							
1xB7	CLUT3_Y							
1xB8	CLUT3_CB							
1xB9	CLUT3_CR							

CLUT0_Y	Y component for user defined color 0 (default : 0)
CLUT0_CB	Cb component for user defined color 0 (default : 0)
CLUT0_CR	Cr component for user defined color 0 (default : 0)
CLUT1_Y	Y component for user defined color 1 (default : 0)
CLUT1_CB	Cb component for user defined color 1 (default : 0)
CLUT1_CR	Cr component for user defined color 1 (default : 0)
CLUT2_Y	Y component for user defined color 2 (default : 0)
CLUT2_CB	Cb component for user defined color 2 (default : 0)
CLUT2_CR	Cr component for user defined color 2 (default : 0)
CLUT3_Y	Y component for user defined color 3 (default : 0)
CLUT3_CB	Cb component for user defined color 3 (default : 0)
CLUT3_CR	Cr component for user defined color 3 (default : 0)

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1xBA	0	0	0	0	T_CASCADE_EN	0	ALPHA_OSD	

T_CASCADE_EN Enable the infinity cascade mode for display path

0 Normal operation (default)

1 Enable the infinity cascade mode for display path

ALPHA_OSD Select alpha blending mode for OSD

0 50% (default)

1 50%

2 75%

3 25%

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1xBB	0	0	BYP_MPP	0	1	0	DEC_BYP_EN	

BYP_MPP Enable the decoder bypass mode using {MPPDEC_Y, MPPDEC_X}

0 Normal Operation (default)

1 Enable the decoder bypass mode using MPPDEC

DEC_BYP_EN Enable the decoder bypass mode using SDRAM interface of Y Path

0 Disable the decoder bypass mode (default)

1 Enable the decoder bypass mode with scaled display path

2 Enable the decoder bypass mode with scaled record path

3 Enable the decoder bypass mode with full D1

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1xBC	0	0	0	0	0	0	0	0

This is reserved register.

For normal operation, the above value should be set in this register.

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1xC0	0	0	0	VIS_RIC_EN	0	0	0	

VIS_RIC_EN Enable Run-in Clock of Analog channel ID during VBI

0 Disable Run-in Clock (default)

1 Enable Run-in Clock

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1xC1	VIS_ENA	VIS_EC _EN	VIS_CODE _EN	VIS_MIX_EN	VIS_SEL			

VIS_ENA Enable the Analog channel ID during vertical blanking interval

0 Disable the Analog channel ID (default)

1 Enable the Analog channel ID

VIS_EC_EN Enable the error correction mode for Auto channel ID

0 Disable the error correction mode for Auto channel ID (default)

1 Enable the error correction mode for Auto channel ID

VIS_CODE_EN Enable the Digital channel ID during VBI

0 Disable the Digital channel ID (default)

1 Enable the Digital channel ID

VIS_MIX_EN Select the Analog channel ID Format

0 Analog Channel ID Format 1 (default)

1 Analog Channel ID Format 2

VIS_SEL Select the kind of channel ID when VIS_MIX_EN = 0

VIS_SEL[3] stand for 8^{th} ~ 7^{th} line among of 8 line with analog channel ID.

VIS_SEL[2] stand for 6^{th} ~ 5^{th} line among of 8 line with analog channel ID.

VIS_SEL[1] stand for 4^{th} ~ 3^{rd} line among of 8 line with analog channel ID.

VIS_SEL[0] stand for 2^{nd} ~ 1^{st} line among of 8 line with analog channel ID.

0 Auto Channel ID

1 User Channel ID

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1xC2	VIS_H_OS							
1xC3	0	0	0	VIS_PIXEL_WIDTH				
1xC4	VIS_LINE_WIDTH			VIS_LINE_OS				
1xC5	VIS_HIGH_VAL							
1xC6	VIS_LOW_VAL							

VIS_H_OS Horizontal start offset for Analog channel ID

0 No Offset (default)

: :

255 255 pixels Offset

VIS_PIXEL_WIDTH Pixel width of each bit for Analog channel ID

0 1 pixel (default)

: :

31 32 pixels

VIS_LINE_WIDTH Line width for Analog channel ID

0 1 line (default)

: :

7 8 lines

VIS_LINE_OS Vertical start offset from field sync transition for Analog channel ID

0 No offset (default)

: :

24) 31 lines

VIS_HIGH_VAL Magnitude for bit “1” of Analog channel ID

VIS_LOW_VAL Magnitude for bit “0” of Analog channel ID

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1xC9	AUTO_VBI_DET	VBI_EC_ON	VBI_CODE_EN	VIS_RIC_ON	VBI_MIX_ON	VBI_FLT_EN	0	VBI_RD_CTL

AUTO_VBI_DET Select the Analog channel ID detection mode for playback input
0 Manual Analog channel ID detection mode (default)
1 Automatic Analog channel ID detection mode

VBI_EC_ON Enable the error correction mode for Auto channel ID
0 Disable the error correction for Auto channel ID (default)
1 Enable the error correction for Auto channel ID

VBI_CODE_EN Enable the Digital channel ID detection mode for playback input
0 Disable the Digital channel ID detection mode (default)
1 Enable the Digital channel ID detection mode

VBI_RIC_ON Select the Run-in clock mode for Analog channel ID
0 No Run-in Clock mode (default)
1 Run-in Clock mode

VBI_MIX_ON Select the Analog channel ID format for playback input
0 Analog Channel ID format 1 (default)
1 Analog Channel ID format 2

VBI_FLT_EN Select the filter mode for playback input
0 Bypass (default)
1 Enable the filter

VBI_RD_CTL Control the read mode of channel ID for Channel ID CODEC
0 Read the Written Data into VIS_MAN registers (1xD0 ~ 1xDF)
Read the encoded ID data from AUTO_CHID registers. (1xE0 ~ 1xE3)
25) Read the decoded ID data from VIS_MAN registers (1xD0 ~ 1xDF)
Read the decoded ID data from AUTO_CHID registers (1xE0 ~ 1xE3)

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1xCA	VBI_PIXEL_H_OS							
1xCB	VBI_FLD_OS		VAV_CHK	VBI_PIXEL_HW				

VBI_PIXEL_H_OS Horizontal start offset of Analog channel ID

When Manual Analog channel ID detection mode (AUTO_VBI_DET = 0)

0 No offset (Not supported in No Run-in Clock mode) (default)

: :

26) 255 pixel offset

When Auto Analog channel ID detection mode (AUTO_VBI_DET = 1)

This register notifies the detected horizontal start offset for Analog channel ID.

VBI_FLD_OS Vertical start line offset of Analog channel ID for field polarity

0 Apply same VBI_LINE_OS to odd and even field (default)

1 Apply { VBI_LINE_OS +1} to odd and VBI_LINE_OS to even field

2 Apply VBI_LINE_OS to odd and {VBI_LINE_OS +1} to even field

3 Apply VBI_LINE_OS to odd and {VBI_LINE_OS +2} to even field

VAV_CHK Enable the channel ID detection in vertical active period

0 Channel ID detection for VBI period only

1 Channel ID detection for VBI and vertical active period

VBI_PIXEL_HW Pixel width for each bit of Analog channel ID

0 1 pixel (default)

: :

27) 32 pixels

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1xCC	VBI_LINE_WIDTH			VBI_LINE_OS				
1xCD	VBI_MID_VAL							
1xCE	CHID_VALID *							
1xCF	CHID_TYPE *							

Notes "*" stand for read only register

VBI_LINE_WIDTH Line width for Analog channel ID

When Manual Analog Channel ID detection mode (AUTO_VBI_DET = 0)

0 1 line (default)

: :

28) 8 lines

When Auto Analog channel ID detection mode (AUTO_VBI_DET = 1)

This register notifies the detected line width for Analog channel ID.

VBI_LINE_OS Vertical start offset from field sync transition for Analog channel ID

0 No offset (default)

: :

29) 31 lines

VBI_MID_VAL Threshold level to define bit "0" or bit "1" from Analog channel ID

CHID_VALID Status of validity for detected channel ID

CHID_VALID[7:0] stand for 8th ~ 1st line from Analog channel ID

0 Not Valid

1 Valid

CHID_TYPE Indicates the detected channel ID type

CHID_VALID[7:0] stand for 8th ~ 1st line from Analog channel ID

0 Auto Channel ID

1 User Channel ID

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1xD0	VIS_MAN0[15:8]							
1xD1	VIS_MAN0[7:0]							
1xD2	VIS_MAN1[15:8]							
1xD3	VIS_MAN1[7:0]							
1xD4	VIS_MAN2[15:8]							
1xD5	VIS_MAN2[7:0]							
1xD6	VIS_MAN3[15:8]							
1xD7	VIS_MAN3[7:0]							
1xD8	VIS_MAN4[15:8]							
1xD9	VIS_MAN4[7:0]							
1xDA	VIS_MAN5[15:8]							
1xDB	VIS_MAN5[7:0]							
1xDC	VIS_MAN6[15:8]							
1xDD	VIS_MAN6[7:0]							
1xDE	VIS_MAN7[15:8]							
1xDF	VIS_MAN7[7:0]							
1xE0	AUTO_CHID0							
1xE1	AUTO_CHID1							
1xE2	AUTO_CHID2							
1xE3	AUTO_CHID3							

Notes "*" stand for read only register

VIS_MAN

Define the User Channel ID for each line

VIS_MAN0 stand for the channel ID of 1st line for Channel ID

VIS_MAN1 stand for the channel ID of 2nd line for Channel ID

VIS_MAN2 stand for the channel ID of 3rd line for Channel ID

VIS_MAN3 stand for the channel ID of 4th line for Channel ID

VIS_MAN4 stand for the channel ID of 5th line for Channel ID

VIS_MAN5 stand for the channel ID of 6th line for Channel ID

VIS_MAN6 stand for the channel ID of 7th line for Channel ID

VIS_MAN7 stand for the channel ID of 8th line for Channel ID

Read mode depends on VBI_RD_CTL register

0 Written User Channel ID

1 Decoded Channel ID

AUTO_CHID

Auto Channel ID Data Information

For read mode, it depends on VBI_RD_CTL register

0 Encoded Auto Channel ID in record path

1 Decoded Auto Channel ID from playback input

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
2x00	CUR_ ON_X	CUR_ ON_Y	CUR_ TYPE	CUR_ SUB	CUR_ BLINK	0	CUR_HP[0]	CUR_VP[0]
2x01	CUR_HP[8:1]							
2x02	CUR_VP[8:1]							

CUR_ON Enable the mouse pointer.

0 Disable mouse pointer (default)

1 Enable mouse pointer

CUR_TYPE Select the mouse type

0 Small mouse pointer (default)

1 Large mouse pointer

CUR_SUB Control inside style of mouse pointer.

0 Transparent (default)

1 Filled with white color

CUR_BLINK Enable blink of mouse pointer.

0 Disable blink (default)

1 Enable blink with 0.5 second period

CUR_HP Horizontal location of mouse pointer.

0 0 Pixel position (default)

: :

360 720 Pixels position

CUR_VP Vertical location of mouse pointer.

0 0 Line position (default)

: :

30) 288 Line position

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
2x03	BOX_TYPE	BOX_EMP	0	0	ALPHA_2DBOX		ALPHA_BOX	

BOX_TYPE Select the single box type.

0 Flat type (default)

1 3D type

BOX_EMP Enable the emphasis on box plane.

0 Disable the emphasis (default)

1 Enable the emphasis

ALPHA_2DBOX Select alpha blending mode for 2D Box

1 50% (default)

2 50%

3 75%

4 25%

ALPHA_BOX Select alpha blending mode for Box

0 50% (default)

1 50%

2 75%

3 25%

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
2x04	BOX_BNDCOL							

BOX_BNDCOL Select the box boundary color as the following table
The default value is 0.

Boundary		Control Register			Color Description	
		BOX_TYPE	BOX_OBND	BOX_IBND	Register	Color
Outer		0 (Flat Type)	0	X	BOX_ BNDCOL [7:4]	Outer Boundary off
			1			0~10 : 0, 10, 20, 30, 40, 50, 60, 70, 80, 90, 100 IRE Gray 11~14 : User defined Color (1xAF ~ 1xB9) 15 : Same as plane color with 20IRE down of luminance
Inner			X	0	BOX_ BNDCOL [3:0]	Inner Boundary off
				1		0~10 : 0, 10, 20, 30, 40, 50, 60, 70, 80, 90, 100 IRE Gray 11~14 : User defined Color (1xAF ~ 1xB9). 15 : Same as plane color with 20IRE up of luminance
Outer	Left & Top	1 (3D Type)	0	X	BOX_ BNDCOL [7:6]	Boundary off
			1	0		0~3 : 90, 80, 70, 60 IRE Gray
			1	1		0~3 : 0, 10, 20, 30 IRE Gray
	Right & Bottom		0	X	BOX_ BNDCOL [5:4]	Boundary off
			1	0		0~3 : 0, 10, 20, 30 IRE Gray
			1	1		0~3 : 90, 80, 70, 60 IRE Gray
Inner	Left & Top		0	0	BOX_ BNDCOL [3:2]	Boundary off
			1	0		Same as inner area
			1	1		0~3 : 30, 40, 50, 60 IRE Gray
	Right & Bottom		0	0	BOX_ BNDCOL [1:0]	Boundary off
			1	0		0~3 : 30, 40, 50, 60 IRE Gray
			1	1		0~3 : 70, 60, 50, 40 IRE Gray

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
2x05	BOX_PLNCOL1				BOX_PLNCOL0			
2x06	BOX_PLNCOL3				BOX_PLNCOL2			
2x07	BOX_PLNCOL5				BOX_PLNCOL4			
2x08	BOX_PLNCOL7				BOX_PLNCOL6			
2x09	BOX_PLNCOL9				BOX_PLNCOL8			
2x0A	BOX_PLNCOLB				BOX_PLNCOLA			
2x0B	BOX_PLNCOLD				BOX_PLNCOLC			
2x0C	BOX_PLNCOLF				BOX_PLNCOLE			

BOX_PLNCOL Define the box plane color for each box

"x" in the BOX_PLNCOLx stands for box number

Color selection table

0 White (75% Amplitude 100% Saturation) (default)
1 Yellow (75% Amplitude 100% Saturation)
2 Cyan (75 % Amplitude 100 Saturation)
3 Green (75% Amplitude 100% Saturation)
4 Magenta (75% Amplitude 100% Saturation)
5 Red (75% Amplitude 100% Saturation)
6 Blue (75% Amplitude 100% Saturation)
7 0% Black
8 100% White
9 50% Gray
10 25% Gray
11 Blue (75% Amplitude 75% Saturation)
12 Defined by CLUT0
13 Defined by CLUT1
14 Defined by CLUT2
15 Defined by CLUT3

Box	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	2x10	BOX_ EN_X	BOX _EN_Y	BOX_ OBND	BOX_ IBND	BOX_ PLNMIX	BOX_ PLN_EN		
1	2x15								
2	2x1A								
3	2x1F								
4	2x24								
5	2x29								
6	2x2E								
7	2x33								
8	2x38								
9	2x3D								
10	2x42								
11	2x47								
12	2x4C								
13	2x51								
14	2x56								
15	2x5B								

BOX_EN Enable the box

0 Disable the box (default)

1 Enable the box

BOX_OBND Enable the outer boundary.

Refer to the box boundary color in 2x04.

0 Disable (default)

1 Enable

BOX_IBND Enable the inner boundary.

Refer to the box boundary color in 2x04.

0 Disable the inner boundary (default)

1 Enable the inner boundary

BOX_PLNMIX Enable alpha blending for box plane with video data.

0 Disable alpha blending (default)

1 Enable alpha blending with ALPHA_BOX register (2x03)

BOX_PLNEN Enable the box plane

Refer to the box plane color in 2x05 ~ 2x0C.

0 Disable the box plane (default)

1 Enable the box plane

Box	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	2x10							BOX_ HL[0]	
1	2x15								
2	2x1A								
3	2x1F								
4	2x24								
5	2x29								
6	2x2E								
7	2x33								
8	2x38								
9	2x3D								
10	2x42								
11	2x47								
12	2x4C								
13	2x51								
14	2x56								
15	2x5B								
0	2x11	BOX_ HL[8:1]							
1	2x16								
2	2x1B								
3	2x20								
4	2x25								
5	2x2A								
6	2x2F								
7	2x34								
8	2x39								
9	2x3E								
10	2x43								
11	2x48								
12	2x4D								
13	2x52								
14	2x57								
15	2x5C								

BOX_HL Define the horizontal left location of box.

0 Left end (default)

: :

2) Right end

Box	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	2x12	BOX_HW							
1	2x17								
2	2x1B								
3	2x21								
4	2x26								
5	2x2B								
6	2x30								
7	2x35								
8	2x3A								
9	2x3E								
10	2x44								
11	2x49								
12	2x4E								
13	2x53								
14	2x58								
15	2x5D								

BOX_HW Define the horizontal size of box.

0 0 Pixel width (default)

: :

3) 720 Pixels width

Box	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	2x10								BOX_ VT[0]
1	2x15								
2	2x1A								
3	2x1F								
4	2x24								
5	2x29								
6	2x2E								
7	2x33								
8	2x38								
9	2x3D								
10	2x42								
11	2x47								
12	2x4C								
13	2x51								
14	2x56								
15	2x5B								
0	2x13	BOX_ VT[8:1]							
1	2x18								
2	2x1D								
3	2x22								
4	2x27								
5	2x2C								
6	2x31								
7	2x36								
8	2x3B								
9	2x40								
10	2x45								
11	2x4A								
12	2x4F								
13	2x54								
14	2x59								
15	2x5E								

BOX_VT Define the vertical top location of box.

0 Vertical top (default)

: :

4) Vertical bottom

Box	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	2x14	BOX_VW							
1	2x19								
2	2x1E								
3	2x23								
4	2x28								
5	2x2D								
6	2x32								
7	2x37								
8	2x3C								
9	2x41								
10	2x46								
11	2x4B								
12	2x50								
13	2x55								
14	2x5A								
15	2x5F								

BOX_VW Define the vertical size of box.

0 0 Lines height (default)

: :

5) 288 Lines height

2Dbox	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	2x60	2DBOX _EN_X	2DBOX _EN_Y	2DBOX _MODE	2DBOX_ DETEN	2DBOX _MSKEN	2DBOX _MIX	2DBOX _CUREN	2DBOX _BNDEN
1	2x68								
2	2x70								
3	2x78								

2DBOX_EN Enable the 2Dbox

0 Disable the 2D box (default)

1 Enable the 2D box

2DBOX_MODE Define the operation mode of 2D arrayed box.

0 Table mode (default)

1 Motion display mode

2DBOX_DETEN Enable the detection plane of 2D arrayed box.

When 2DBOX_MODE = “0”

0 Disable the detection plane of 2D arrayed box (default)

1 Enable the detection plane of 2D arrayed box

When 2DBOX_MODE = “1”

0 Display the motion detection result with inner boundary

1 Display the motion detection result with plane

2DBOX_MSKEN Enable the mask plane of 2D arrayed box.

0 Disable the mask plane of 2D arrayed box (default)

1 Enable the mask plane of 2D arrayed box

2DBOX_MIX Enable to alpha blending for 2D arrayed box plane with video data.

0 Disable to alpha blending (default)

1 Enable to alpha blending with ALPHA_2DBOX setting (2x03)

2DBOX_CUREN Enable the cursor cell inside 2D arrayed box.

0 Disable the cursor cell (default)

1 Enable the cursor cell

2DBOX_BNDEN Enable the boundary of 2D arrayed box.

0 Disable the boundary (default)

1 Enable the boundary

2Dbox	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	2x61	2DBOX_PLNCOL				2DBOX_BNDCOL			
1	2x69								
2	2x71								
3	2x79								

2DBOX_BNDCOL Define the color of 2D arrayed box boundary

0 0 % Black (default)
1 25% Gray
2 50% Gray
3 75% White

Define the displayed color for cursor cell and motion-detected region

0,1 75% White (default)
2,3 0% Black

2DBOX_PLNCOL Define the color of 2D arrayed box plane.

Color selection table

0 White (75% Amplitude 100% Saturation) (default)
1 Yellow (75% Amplitude 100% Saturation)
2 Cyan (75 % Amplitude 100 Saturation)
3 Green (75% Amplitude 100% Saturation)
4 Magenta (75% Amplitude 100% Saturation)
5 Red (75% Amplitude 100% Saturation)
6 Blue (75% Amplitude 100% Saturation)
7 0% Black
8 100% White
9 50% Gray
10 25% Gray
11 Blue (75% Amplitude 75% Saturation)
12 Defined by CLUT0
13 Defined by CLUT1
14 Defined by CLUT2
15 Defined by CLUT3

2Dbox	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	2x61							2DBOX_ HL[0]	
1	2x69								
2	2x71								
3	2x79								
0	2x62	2DBOX_HL[8:1]							
1	2x6A								
2	2x72								
3	2x7A								

2DBOX_HL Define the horizontal left location of 2D arrayed box.

0 Horizontal left end (default)

: :

6) Horizontal right end

2Dbox	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	2x63	2DBOX_HW							
1	2x6B								
2	2x73								
3	2x7B								

2DBOX_HW Define the horizontal size of 2D arrayed box.

0 0 Pixel width (default)

: :

7) 510 Pixels width

2Dbox	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	2x61								2DBOX_ VT[0]
1	2x69								
2	2x71								
3	2x79								
0	2x64	2DBOX_VT[8:1]							
1	2x6C								
2	2x74								
3	2x7C								

2DBOX_VT Define the vertical top location of 2D arrayed box.

0 Vertical top end (default)

: :

240 Vertical bottom end for 60Hz system

: :

8) Vertical bottom end for 50Hz system

2Dbox	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	2x65	2DBOX_VW							
1	2x6D								
2	2x75								
3	2x7D								

2DBOX_VW Define the vertical size of 2D arrayed box.

0 0 Line height (default)

: :

9) 255 Lines height

2Dbox	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	2x66	2DBOX_HNUM				2DBOX_VNUM			
1	2x6E								
2	2x76								
3	2x7E								

2DBOX_VNUM Define the row number of 2D arrayed box.

For motion display mode, 11 is recommended.

0 1 Row

: :

11 12 Row (default)

: :

10) 16 Rows

2DBOX_HNUM Define the column number of 2D arrayed box.

For motion display mode, 15 is recommended.

0 1 Column

: :

11) 16 Columns (default)

2Dbox	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	2x67	2DBOX_CURHP				2DBOX_CURVP			
1	2x6F								
2	2x77								
3	2x7F								

2DBOX_CURHP Define the horizontal location of cursor cell within 2DBOX_HNUM.

0 1st Column (default)

: :

12) 16th Column

2DBOX_CURVP Define the vertical location of cursor cell within 2DBOX_VNUM.

0 1st Row (default)

: :

13) 16th Row

VIN	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	2x80	MD_DIS	MD _REFFLD	BD_CELSENS		BD_LVSENS			
1	2xA0								
2	2xC0								
3	2xE0								

MD_DIS Disable the motion and blind detection.

0 Enable motion and blind detection (default)

1 Disable motion and blind detection

MD_REFFLD Control the updating time of reference field for motion detection.

0 Update reference field at every field (default)

1 Update reference field according to MD_SPEED

BD_CELSENS Define the threshold of cell for blind detection.

0 Low threshold (More sensitive) (default)

: :

3 High threshold (Less sensitive)

BD_LVSENS Define the threshold of level for blind detection.

0 Low threshold (More sensitive) (default)

: :

14) High threshold (Less sensitive)

VIN	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	2x81	2DBOX _HINV	2DBOX _VINV	MD_FLD		MD_ALGIN			
1	2xA1								
2	2xC1								
3	2xE1								

2DBOX_HINV Horizontal mirroring for 2D arrayed box.

0 Normal operation (default)

1 Enable horizontal mirroring

2DBOX_VINV Vertical mirroring for 2D arrayed box.

0 Normal operation (default)

1 Enable vertical mirroring

MD_FLD Select the field for motion detection.

0 Detecting motion for only odd field (default)

1 Detecting motion for only even field

2 Detecting motion for any field

3 Detecting motion for both odd and even field

MD_ALGIN Adjust the horizontal start position for motion detection.

0 0 Pixel shift (default)

: :

15) 15 Pixels shift

VIN	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	2x82	MD_CELSENS		MASK _MODE	MD_LVSENS				
1	2xA2								
2	2xC2								
3	2xE2								

MD_CELSENS Define the threshold of sub-cell number for motion detection.

0 Motion detected if 1 sub-cell has motion (More sensitive) (default)

1 Motion detected if 2 sub-cells have motion

2 Motion detected if 3 sub-cells have motion

3 Motion detected if 4 sub-cells have motion (Less sensitive)

MASK_MODE Define the read mode of MD_MASK register.

0 Read the motion detection result (default)

1 Read the mask information

MD_LVSENS Control the level sensitivity of motion detector.

0 More sensitive

: :

8 Middle sensitive (default)

: :

16) Less sensitive

VIN	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	2x83	MD_ STRB_EN	MD_STRB	MD_SPEED					
1	2xA3								
2	2xC3								
3	2xE3								

MD_STRB_EN Select the motion detection mode

0 Automatic motion detection trigger

1 Manual motion detection trigger

MD_STRB Request to start motion detection on manual motion detection trigger

0 None Operation (default)

1 Request to start for Motion Detection

MD_SPEED Control the velocity of motion detector.

Large value is suitable for slow motion detection.

0 1 field/frame intervals (default)

1 2 field/frame intervals

: :

61 62 field/frame intervals

62 63 field/frame intervals

63 Not supported

VIN	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	2x84	MD_DET_PERIOD							
1	2xA4								
2	2xC4								
3	2xE4								

MD_DET_PERIOD Control the Motion Monitoring Period for Motion Interrupt

0 1 field/frame intervals

: :

17) 256 field/frame intervals

VIN	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	2x85	MD_TMPSENS				MD_SPSENS			
1	2xA5								
2	2xC5								
3	2xE5								

MD_TMPSENS Control the temporal sensitivity of motion detector.

0 More Sensitive (default)

: :

15 Less Sensitive

MD_SPSENS Control the spatial sensitivity of motion detector.

0 More Sensitive (default)

: :

18) Less Sensitive

Row	Index				Motion Detection Mask Control for VIN							
	VIN0	VIN1	VIN2	VIN3	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1	2x86	2xA6	2xC6	2xE6	MD_MASK[15:8]							
2	2x88	2xA8	2xC8	2xE8								
3	2x8A	2xAA	2xCA	2xEA								
4	2x8C	2xAC	2xCC	2xEC								
5	2x8E	2xAE	2xCE	2xEE								
6	2x90	2xB0	2xD0	2xF0								
7	2x92	2xB2	2xD2	2xF2								
8	2x94	2xB4	2xD4	2xF4								
9	2x96	2xB6	2xD6	2xF6								
10	2x98	2xB8	2xD8	2xF8								
11	2x9A	2xBA	2xDA	2xFA								
12	2x9C	2xBC	2xDC	2xFC								
1	2x87	2xA7	2xC7	2xE7	MD_MASK[7:0]							
2	2x89	2xA9	2xC9	2xE9								
3	2x8B	2xAB	2xCB	2xEB								
4	2x8D	2xAD	2xCD	2xED								
5	2x8F	2xAF	2xCF	2xEF								
6	2x91	2xB1	2xD1	2xF1								
7	2x93	2xB3	2xD3	2xF3								
8	2x95	2xB5	2xD5	2xF5								
9	2x97	2xB7	2xD7	2xF7								
10	2x99	2xB9	2xD9	2xF9								
11	2x9B	2xBB	2xDB	2xFB								
12	2x9D	2xBD	2xDD	2xFD								

MD_MASK — Motion Mask/Detection Cell for VIN

MD_MASK[15] is right end and MD_MASK[0] is left end of column.

Writing mode

0 Non-masking cell for motion detection (default)

1 Masking cell for motion detection

Reading mode when MASK_MODE = “0”

0 Motion is not detected for cell

1 Motion is detected for cell

Reading mode when MASK_MODE = “1”

0 Non-masked cell

1 Masked cell

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
2x9E	MD_PATH	0	0	DETCOL_EN	DETCOL_SEL			

MD_PATH Select the path to store motion detection information

0 Display path

1 Record path

DETCOL_EN Enable the different color for detection plane of 2D arrayed Box

0 Same as plane color (default)

1 Different color with the DETCOL_SEL register

DETCOL_SEL Select the color for detection plane when DETCOL_EN = 1

Color selection table

0 White (75% Amplitude 100% Saturation) (default)

1 Yellow (75% Amplitude 100% Saturation)

2 Cyan (75 % Amplitude 100 Saturation)

3 Green (75% Amplitude 100% Saturation)

4 Magenta (75% Amplitude 100% Saturation)

5 Red (75% Amplitude 100% Saturation)

6 Blue (75% Amplitude 100% Saturation)

7 0% Black

8 100% White

9 50% Gray

10 25% Gray

11 Blue (75% Amplitude 75% Saturation)

12 Defined by CLUT0

13 Defined by CLUT1

14 Defined by CLUT2

15 Defined by CLUT3

Parametric Information

DC Electrical Parameters

Table 11 Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VDDADC (measured to VSSADC)	VDD_{ADCM}			3.5	V
VDDDAC (measured to VSSDAC)	VDD_{DACM}			3.5	V
VDDI (measured to VSSI)	VDD_{IM}			3.5	V
VDDO (measured to VSSO)	VDD_{OM}			4.6	V
Voltage on Any Digital Data Pin (See the note below)	-	VSSO–0.5		6.0	V
Analog Input Voltage for ADC	-	VDD_{ADCM}–0.5		VDD_{ADCM}+0.5	V
Analog Input Voltage for DAC		VDD_{DACM}–0.5		VDD_{DACM}+0.5	V
Storage Temperature	T_S	– 65		150	° C
Junction Temperature	T_J	0		125	° C
Vapor Phase Soldering (15 Seconds)	T_{VSOL}			220	° C

NOTE: Long-term exposure to absolute maximum ratings may affect device reliability, and permanent damage may occur if operate exceeding the rating. The device should be operated under recommended operating condition.

Table 12 Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
VDDADC (measured to VSSADC)	VDD_{ADC}	2.25	2.5	2.75	V
VDDDAC (measured to VSSDAC)	VDD_{DAC}	2.25	2.5	2.75	V
VDDI (measured to VSSI)	VDD_I	2.25	2.5	2.75	V
VDDO (measured to VSSO)	VDD_O	3.0	3.3	3.6	V
Maximum $\|VDD_I – VDD_{ADC}\|$				0.3	V
Maximum $\|VDD_I – VDD_{DAC}\|$				0.3	V
Maximum $\|VDD_{ADC} – VDD_{DAC}\|$				0.3	V
Maximum $\|VDD_O – VDD_{ADC}\|$				1.05	V
Maximum $\|VDD_O – VDD_{DAC}\|$				1.05	V
Maximum $\|VDD_O – VDD_I\|$				1.05	V
Analog VIN Amplitude Range (AC coupling required)		0.5	1.0	2.0	V
Ambient Operating Temperature	T_A	0		70	° C

Table 13 DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Digital Inputs					
Input High Voltage (TTL)	V_{IH}	2.0		5.5	V
Input Low Voltage (TTL)	V_{IL}	-0.3		0.8	V
Input Leakage Current (@V_I=2.5V or 0V)	I_L			±1	µA
Input Capacitance	C_{IN}		6		pF
Digital Outputs					
Output High Voltage	V_{OH}	2.4			V
Output Low Voltage	V_{OL}			0.4	V
High Level Output Current (@V_{OH}=2.4V)	I_{OH}	5.7	11.6	18.6	mA
Low Level Output Current (@V_{OL}=0.4V)	I_{OL}	4.1	6.7	8.2	mA
Tri-state Output Leakage Current (@V_O=2.5V or 0V)	I_{OZ}			±1	µA
Output Capacitance	C_O		6		pF
Analog Pin Input Capacitance	C_A		6		pF

Table 14 Supply Current and Power Dissipation

Parameter	Symbol	Min	Typ	Max	Units
Analog Supply Current (2.5V)	I_{DDA}		200	220	mA
Digital Internal Supply Current (2.5V)	I_{DDI}		640	700	mA
Digital I/O Supply Current (3.3V)	I_{DDO}		27	30	mA
Total Power Dissipation	Pd		2.2	2.4	W

Table 15 Thermal Characteristics of 208 QFP Package

Parameter	θ_{JA} (C/W)			ψ_{JT} (C/W)	θ_{JC} (C/W)
	0 m/s	1 m/s	2 m/s		
208 QFP	14.7	11.6	10.6	0.6	4.7

NOTE: θ_{JA} is under air velocity 0, 1, 2 m/s and ψ_{JT} is in still air.

θ_{JA} : Thermal resistance from junction to ambient

ψ_{JT} : Thermal characterization parameter from junction to top center

θ_{JC} : Thermal resistance from junction to case

AC Electrical Parameters

Table 16 Clock Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units
Delay from CLK54I to CLK27ENC	1	4.7		12.5	ns
Hold from CLK27ENC (27MHz) to Data	2a	17			ns
Delay from CLK27ENC (27MHz) to Data	2b			21	ns
Hold from CLK54I to Data	3a	8			ns
Delay from CLK54I to Data	3b			12	ns
Setup from PBIN to PBCLK	4a	5			ns
Hold from PBCLK to PBIN	4b	5			ns

Note : Cload = 25pF.

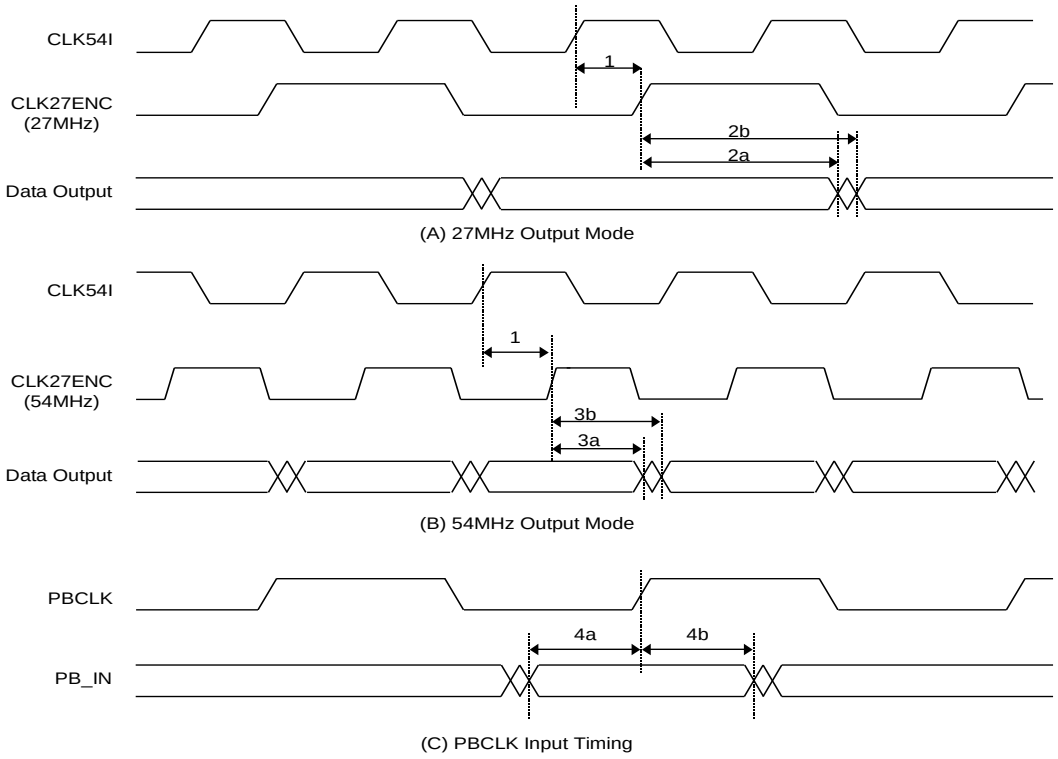


Fig 78 Clock Timing Diagram

Table 17. Serial Interface Timing

Parameter	Symbol	Min	Typ	Max	Units
Bus Free Time between STOP and START	t_{BF}	1.3			us
SDAT setup time	t_{sSDAT}	100			ns
SDAT hold time	t_{hSDAT}	0		0.9	us
Setup time for START condition	t_{sSTA}	0.6			us
Setup time for STOP condition	t_{sSTOP}	0.6			us
Hold time for START condition	t_{hSTA}	0.6			us
Rise time for SCLK and SDAT	t_R			300	ns
Fall time for SCLK and SDAT	t_F			300	ns
Capacitive load for each bus line	C_{BUS}			400	pF
SCLK clock frequency	f_{SCLK}			400	KHz

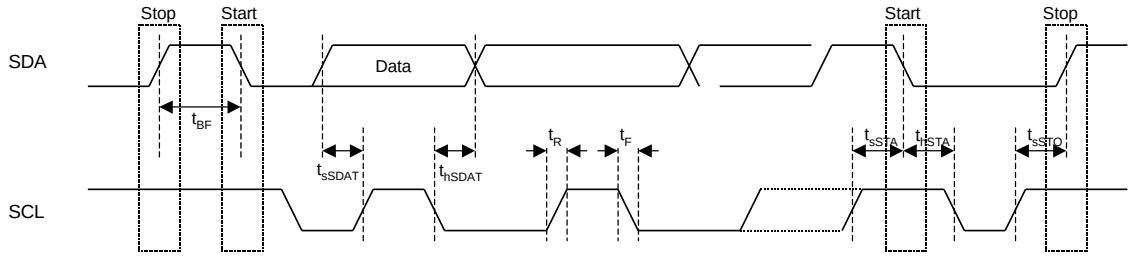


Fig 79. Serial Interface Timing Diagram

Table 18 Parallel Interface Timing Parameter

Parameter	Symbol	Min	Typ	Max	Units
CSB setup until AEN active	Tsu(1)	10			ns
PDATA setup until AEN,WENB active	Tsu(2)	10			ns
AEN, WENB, RENB active pulse width	Tw	40			ns
CSB hold after WENB, RENB inactive	Th(1)	60			ns
PDATA hold after AEN,WENB inactive	Th(2)	20			ns
PDATA delay after RENB active	Td(1)			12	ns
PDATA delay after RENB inactive	Td(2)	60			ns
CSB inactive pulse width	Tcs	60			ns
RENB active delay after AEN inactive RENB active delay after RENB inactive	Trd	60			ns

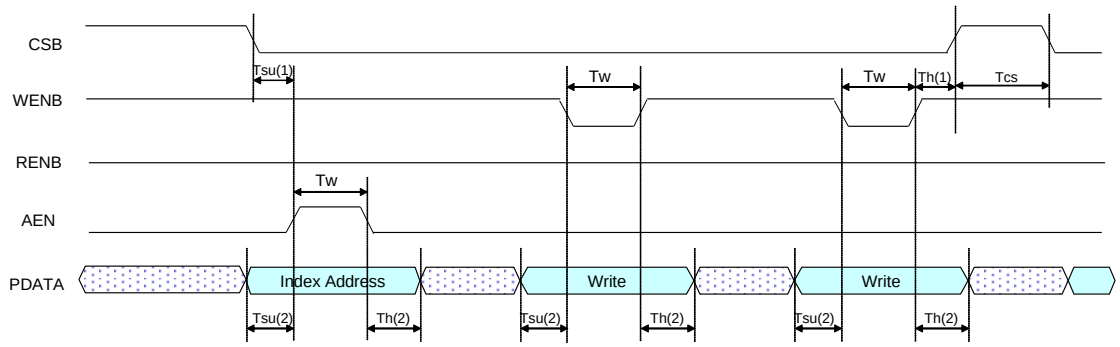


Fig 80 Write timing of parallel interface with auto index increment mode

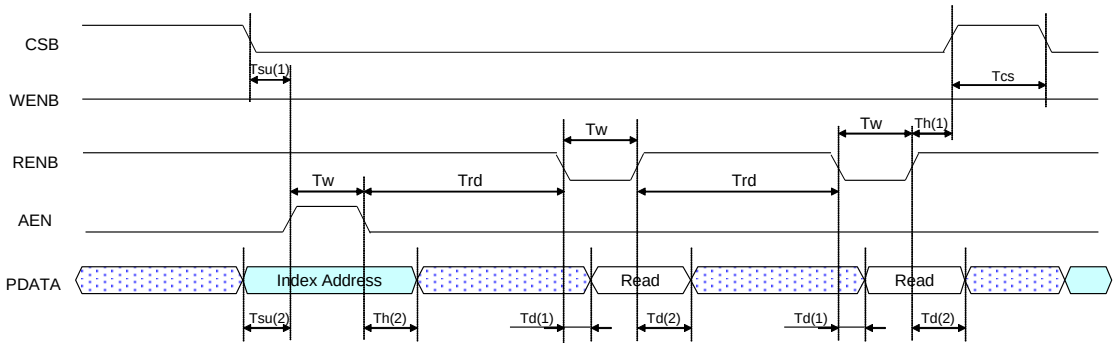


Fig 81 Read timing of parallel interface with auto index increment mode

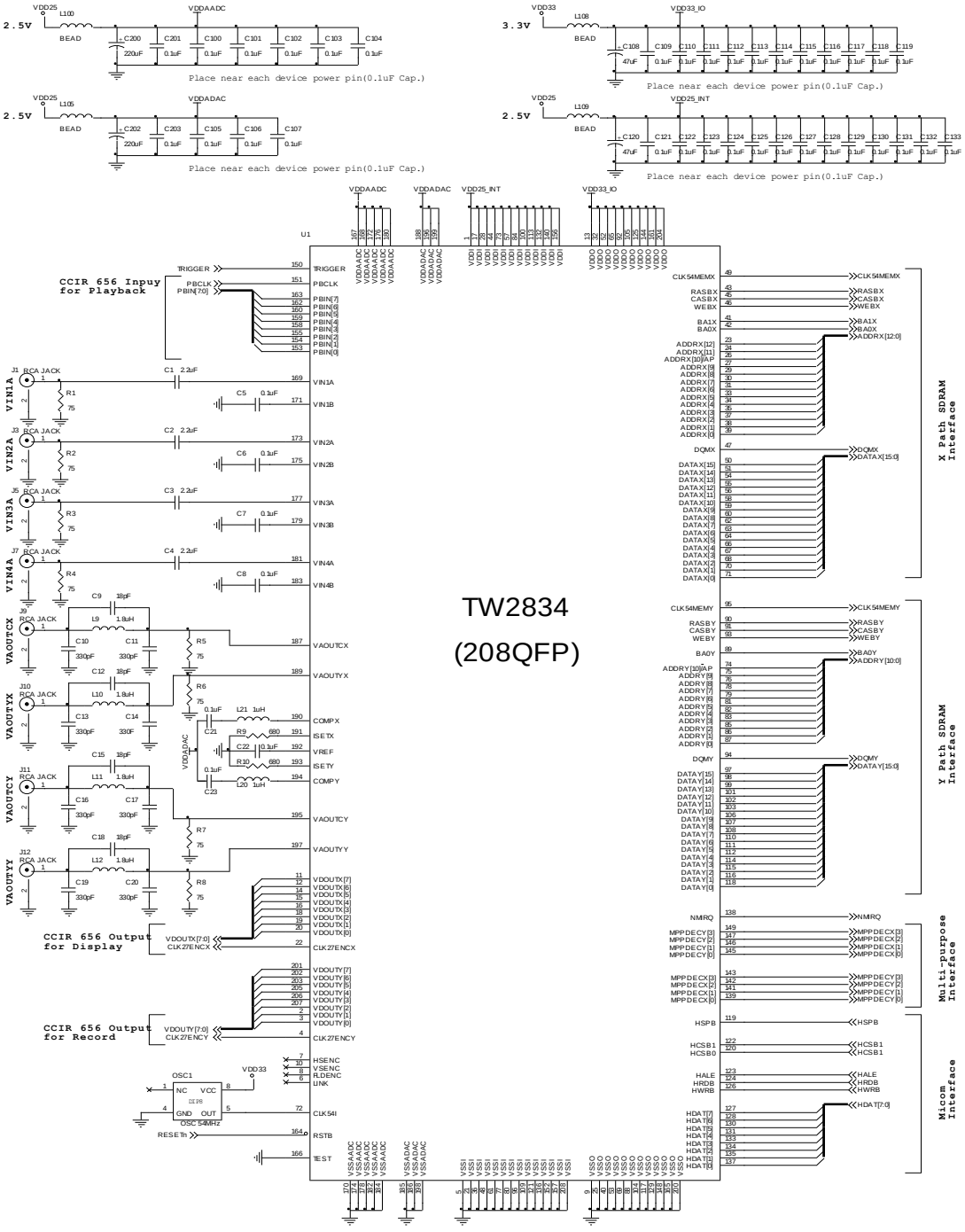
Table 19.Analog Performance Parameter

Parameter	Symbol	Min	Typ	Max	Units
ADC characteristics					
Differential gain	D_{GA}			3	%
Differential phase	D_{pA}			2	deg
Channel Cross-talk	α_{ctA}			-50	dB
DAC characteristic					
Differential gain	D_{GD}			3	%
Differential phase	D_{pD}			2	deg
Channel Cross-talk	α_{ctA}			-50	dB

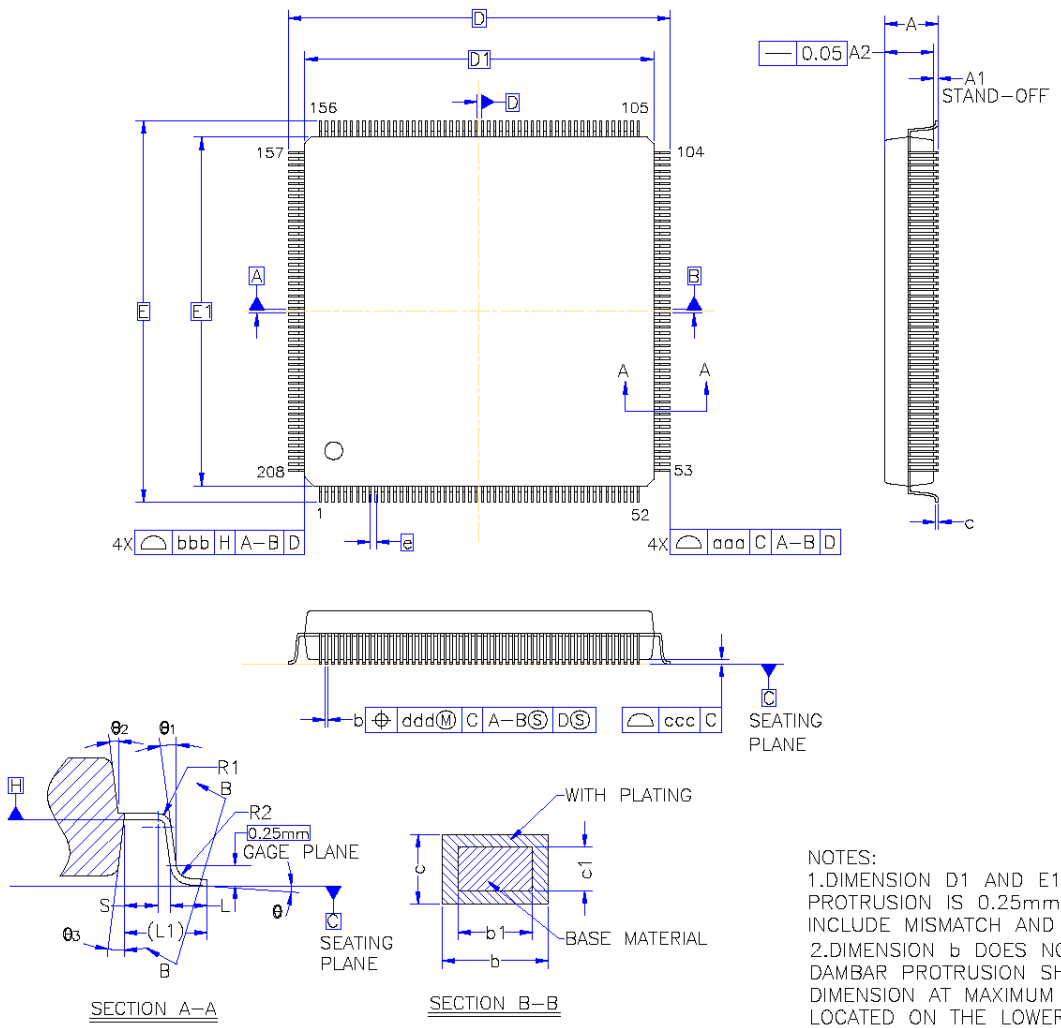
Table 20.Decoder Performance Parameter

Parameter	Symbol	Min	Typ	Max	Units
Horizontal PLL permissible static deviation	Δf_H			±6	%
Color Sub-carrier PLL lock in range	Δf_{SC}	±800			Hz
Video level tracking range	AGC	-6		18	dB
Color level tracking range	ACC	-6		30	dB
Oscillator Input					
Nominal frequency	f_{OSC}		54		MHz
Permissible frequency deviation	$\Delta f_{OSC}/f_{OSC}$			±100	ppm
Duty cycle	dt_{OSC}			60	%

Application Schematic



Package Dimension



ALL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	4.00	—	—	0.157
A1	0.25	0.32	0.40	0.010	0.013	0.016
A2	3.20	3.40	3.60	0.126	0.134	0.142
D	30.60 BASIC			1.205 BASIC		
D1	28.00 BASIC			1.102 BASIC		
E	30.60 BASIC			1.205 BASIC		
E1	28.00 BASIC			1.102 BASIC		
R2	0.08	—	0.25	0.003	—	0.01
R1	0.08	—	—	0.003	—	—
θ	0°	3.5°	8°	0°	3.5°	8°
θ1	0°	—	—	0°	—	—
θ2	5°	—	16°	5°	—	16°
θ3	5°	—	16°	5°	—	16°
c	0.09	—	0.20	0.004	—	0.008
c1	0.09	0.15	0.16	0.004	0.006	0.006
L1	1.30 REF			0.052 REF		
L	0.45	0.60	0.75	0.018	0.024	0.030
S	0.20	—	—	0.008	—	—
b	0.17	—	0.27	0.007	—	0.011
b1	0.17	0.20	0.23	0.007	0.008	0.009
e	0.50 BSC.			0.020 BSC.		
aaa	0.25			0.010		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

NOTES:
1.DIMENSION D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION.ALLOW PROTRUSION IS 0.25mm PER SIDE.DIMENSIONS D1 AND E1 DO INCLUDE MISMATCH AND ARE DETERMINED AT DATUM PLANE H;
2.DIMENSION b DOES NOT INVLUDE DAMBAR PROTRUSION.ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT;

Revision History

Table 21 Datasheet Revision History

Revision	Date	Description	Product Code
FN7739.0	Feb. 1, 2011	Assigned file number FN7739 to datasheet as this will be the first release with an Intersil file number. Replaced header and footer with Intersil header and footer. No changes to datasheet content.	

Table 22. List of Revision Point in TW2834 RevC

No.	Issue	TW2834 RevB	TW2834 RevC
1	Switching Queue	Limited switching channel order in switching queue for 16 channel cascade application	Free switching channel order in switching queue for 16 channel cascade application
2	Quad MUX	Supports Quad MUX by frame unit	Supports Quad MUX by field unit (Page 72, 73, 153, 185)
3	Alpha Blending	Supports only half-tone	Supports the alpha blending with 25%, 50% and 75% level (Page 84, 86, 88, 209, 217)
4	Vertical Active Line	Supports fixed 240 lines for ITU-R BT.656 output in 60Hz system	Also supports 244 lines in odd field and 243 in even field for ITU-R BT. 656 standard in 60Hz system. (Page 95, 195)
5	Memory Clock Frequency	Supports only 54MHz	Supports both 54MHz and 27MHz (Page 189)
6	Channel ID Decoding	Supported only in VBI Period	Supported in both VBI and Vertical active period (Page 25, 213)
7	Playback Stop	No stop mode for auto strobe in playback input	Supports stop mode for auto strobe in playback input (Page 59, 165)
8	Variable 656 Data Parsing for Playback Input	Supports fixed ITU-R BT.656 data parsing for playback input	Supports variable ITU-R BT.656 data parsing for playback input (Page 145)
9	Independent Scaling Filter and Sync Control for Playback Path	Controlled by the scaling filter and sync control register of VIN path	Controlled by the independent scaling filter and sync control register of Playback path (Page 136,137,138,139)