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April 1st, 2010 Renesas Electronics Corporation

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MOS FIELD EFFECT POWER TRANSISTORS Phase-out/Discontinued μ PA1700A

SWITCHING N-CHANNEL POWER MOS FET INDUSTRIAL USE

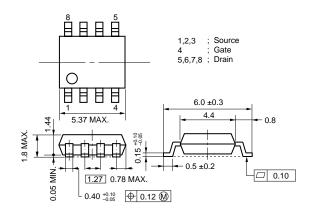
DESCRIPTION

The μ PA1700A is N-Channel MOS Field Effect Transistor designed for DC/DC converters and power management of notebook computers.

FEATURES

- Low On-Resistance $R_{DS(on)1}=27m\Omega~MAX.~(V_{GS}=10~V,~I_{D}=3.5~A)$ $R_{DS(on)2}=50m\Omega~MAX.~(V_{GS}=4~V,~I_{D}=3.5~A)$
- Low Input Capacitance Ciss = 820 pF TYP.
- Built-in G-S Protection Diode
- Small and Surface Mount Package (Power SOP8)

PACKAGE DRAWING (Unit: mm)



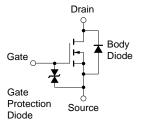
ABSOLUTE MAXIMUM RATINGS (TA = 25°C, all terminals are connected)

Drain to Source Voltage	VDSS	30	V
Gate to Source Voltage	Vgss	±20	V
Drain Current (DC)	I _{D(DC)}	±7.0	Α
Drain Current (pulse) Note1	D(pulse)	±28	Α
Total Power Dissipation $(TA = 25^{\circ}C)^{Note2}$	PT	2.0	W
Channel Temperature	Tch	150	°C
Storage Temperature	Tstg	-55 to +150	°C

Notes 1. PW \leq 10 μ s, Duty Cycle \leq 1%

2. Mounted on ceramic substrate of 1200 mm² x 1.7 mm

EQUIVALENT CIRCUIT



The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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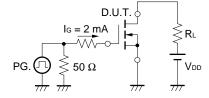


ELECTRICAL CHARACTERISTICS (TA = 25°C, all terminals are connected)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source On-state Resistance	R _{DS(on)1}	Vgs = 10 V, Ip = 3.5 A		18	27	mΩ
	RDS(on)2	Vgs = 4 V, ID = 3.5 A		28	50	mΩ
Gate to Source Cut-off Voltage	VGS(off)	V _{DS} = 10 V, I _D = 1 mA	1.0	1.6	2.0	V
Forward Transfer Admittance	yfs	V _{DS} = 10 V, I _D = 3.5 A	5.0	9.0		S
Drain Leakage Current	Inss	Vps = 30 V, Vgs = 0 V			10	μΑ
Gate to Source Leakage Current	lgss	Vgs = ±20 V, Vps = 0 V			±10	μΑ
Input Capacitance	Ciss	Vps = 10 V		820		pF
Output Capacitance	Coss	V _G S = 0 V		350		pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		160		pF
Turn-On Delay Time	td(on)	ID = 3.5 A		18		ns
Rise Time	t r	V _{GS(on)} = 10 V		98		ns
Turn-Off Delay Time	t _{d(off)}	V _{DD} = 15 V		57		ns
Fall Time	t _f	$R_G = 10 \Omega$		32		ns
Total Gate Charge	Q _G	ID = 7.0 A		20		nC
Gate to Source Charge	Qgs	V _{DD} = 24 V		2.4		nC
Gate to Drain Charge	Q _{GD}	Vgs = 10 V		5.6		nC
Body Diode Forward Voltage	V _{F(S-D)}	IF = 7.0 A, VGS = 0 V		0.79		V
Reverse Recovery Time	trr	IF = 7.0 A, VGS = 0 V		36		ns
Reverse Recovery Charge	Qrr	di/dt = 100 A/μs		35		nC

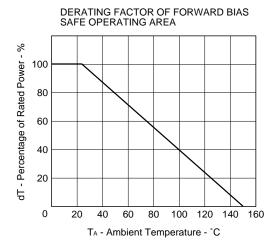
TEST CIRCUIT 1 SWITCHING TIME

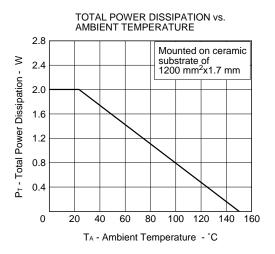
TEST CIRCUIT 2 GATE CHARGE

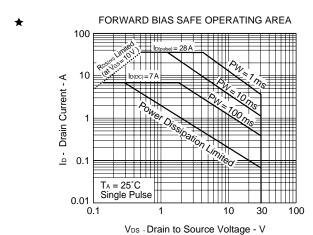




TYPICAL CHARACTERISTICS (TA = 25 °C)

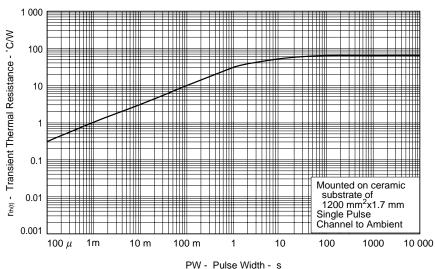


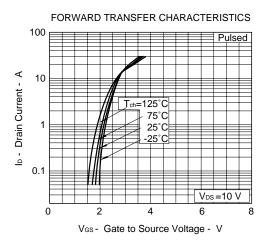


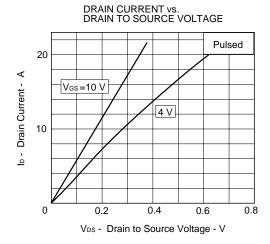


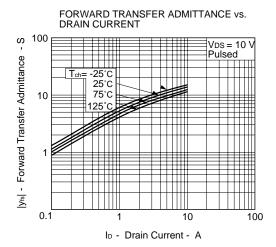
Note: Mounted on ceramic substrate of 1200 mm²x1.7 mm

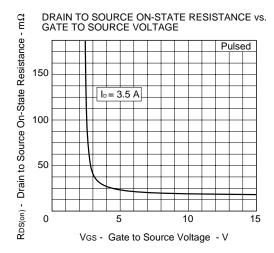
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

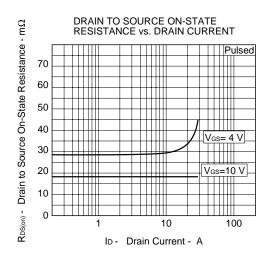


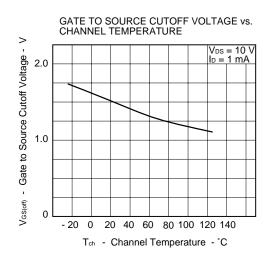


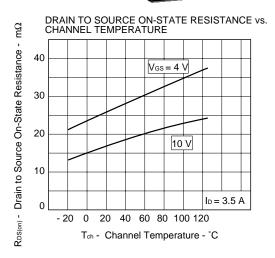


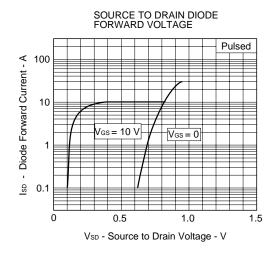


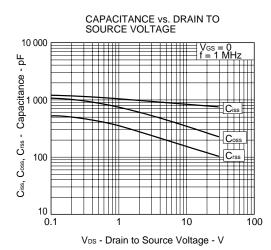


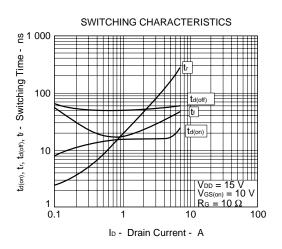


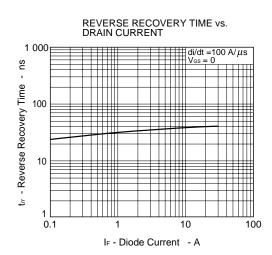


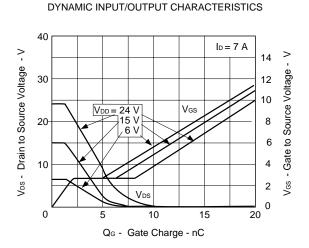














REFERENCE

Document Name	Document No.
NEC semiconductor device reliability / quality control system	C11745E
Quality grade on NEC semiconductor devices	C11531E
Semiconductor device mounting technology manual	C10535E
Semiconductor device package manual	C10943X
Guide to quality assurance for semiconductor devices	MEI-1202
Application circuits using Power MOS FET	TEA-1035
Safe operating area of Power MOS FET	TEA-1037

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