

To our customers,

Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: <http://www.renesas.com>

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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Not recommended
for new design

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MOS FIELD EFFECT TRANSISTOR

μ PA2200T1M

N-CHANNEL MOS FET FOR SWITCHING

DESCRIPTION

The μ PA2200T1M is N-channel MOS Field Effect Transistor designed for power management applications of portable equipments, such as load switch.

FEATURES

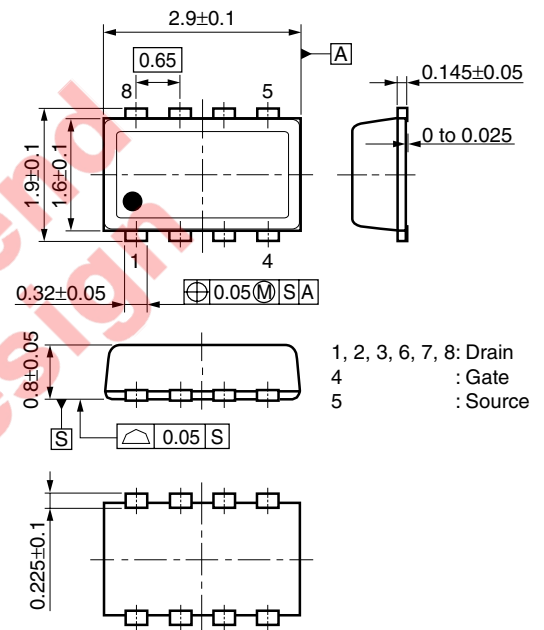
- Low on-state resistance
 $R_{DS(on)1} = 23 \text{ m}\Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 8 \text{ A)}$
 $R_{DS(on)2} = 31 \text{ m}\Omega \text{ MAX. (} V_{GS} = 4.5 \text{ V, } I_D = 4 \text{ A)}$
- Built-in gate protection diode
- 4.5 V Gate drive available

ORDERING INFORMATION

PART NUMBER	PACKING	PACKAGE
μ PA2200T1M-T1-AT ^{Note}	8 mm embossed taping	8-pin VSOF (1629)
μ PA2200T1M-T2-AT ^{Note}	3000 p/reel	0.011 g TYP.

Note Pb-free (This product does not contain Pb in external electrode and other parts.)

PACKAGE DRAWING (Unit: mm)

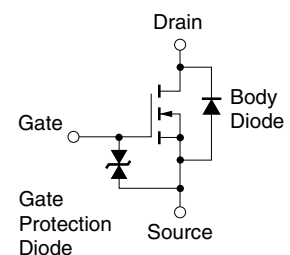


ABSOLUTE MAXIMUM RATINGS (T_A = 25°C, All terminals are connected.)

Drain to Source Voltage (V _{GS} = 0 V)	V _{DSS}	30	V
Gate to Source Voltage (V _{DS} = 0 V)	V _{GSS}	±20	V
Drain Current (DC)	I _{D(DC)}	±8	A
Drain Current (pulse) ^{Note1}	I _{D(pulse)}	±32	A
Total Power Dissipation ^{Note2}	P _{T1}	1.1	W
Total Power Dissipation (PW = 5 sec) ^{Note2}	P _{T2}	2.5	W
Channel Temperature	T _{ch}	150	°C
Storage Temperature	T _{stg}	-55 to +150	°C

- Notes 1.** PW ≤ 10 μs, Duty Cycle ≤ 1%
2. Mounted on glass epoxy board of 25.4 mm x 25.4 mm x 0.8 mm

EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

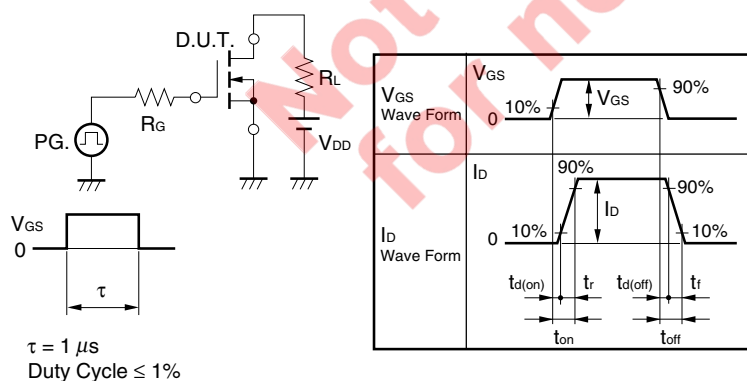
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ELECTRICAL CHARACTERISTICS (TA = 25°C, All terminals are connected.)

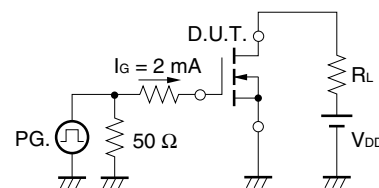
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 30 V, V _{GS} = 0 V			1	μA
Gate Leakage Current	I _{GSS}	V _{GS} = ±20 V, V _{DS} = 0 V			±10	μA
Gate to Source Cut-off Voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1 mA	1.0		2.5	V
Forward Transfer Admittance ^{Note}	y _{fs}	V _{DS} = 10 V, I _D = 4 A	3			S
Drain to Source On-state Resistance ^{Note}	R _{DS(on)1}	V _{GS} = 10 V, I _D = 8 A		18	23	mΩ
	R _{DS(on)2}	V _{GS} = 4.5 V, I _D = 4 A		23	31	mΩ
Input Capacitance	C _{iss}	V _{DS} = 10 V,		870		pF
Output Capacitance	C _{oss}	V _{GS} = 0 V,		160		pF
Reverse Transfer Capacitance	C _{rss}	f = 1 MHz		80		pF
Turn-on Delay Time	t _{d(on)}	V _{DD} = 15 V, I _D = 4 A,		9.2		ns
Rise Time	t _r	V _{GS} = 10 V,		3.4		ns
Turn-off Delay Time	t _{d(off)}	R _G = 10 Ω		31.7		ns
Fall Time	t _f			5.3		ns
Total Gate Charge	Q _G	V _{DD} = 24 V,		8.7		nC
Gate to Source Charge	Q _{GS}	V _{GS} = 5 V,		3.0		nC
Gate to Drain Charge	Q _{GD}	I _D = 8 A		3.2		nC
Body Diode Forward Voltage ^{Note}	V _{F(S-D)}	I _F = 8 A, V _{GS} = 0 V		0.85	1.2	V
Reverse Recovery Time	t _{rr}	I _F = 8 A, V _{GS} = 0 V,		22		ns
Reverse Recovery Charge	Q _{rr}	di/dt = 100 A/μs		15		nC

Note Pulsed

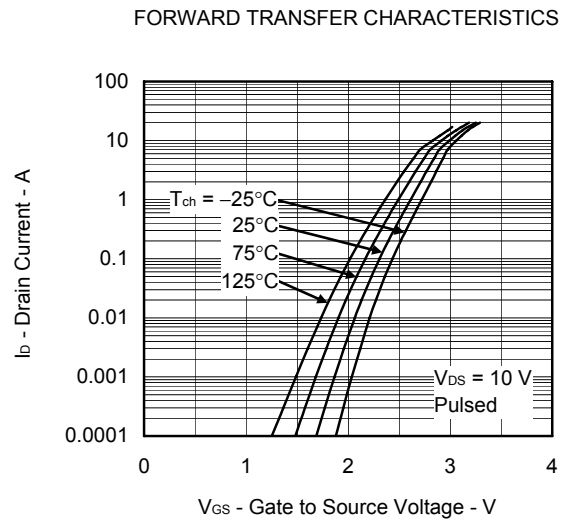
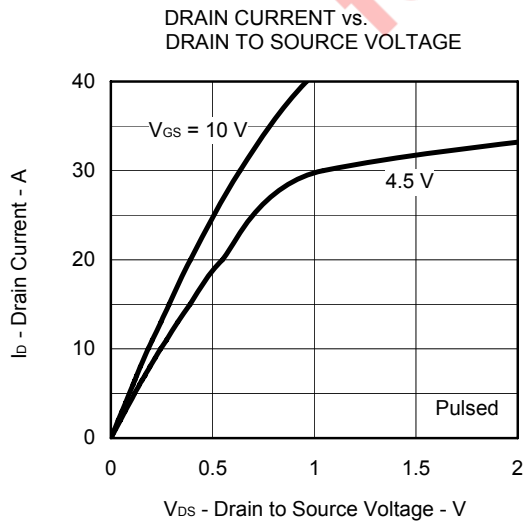
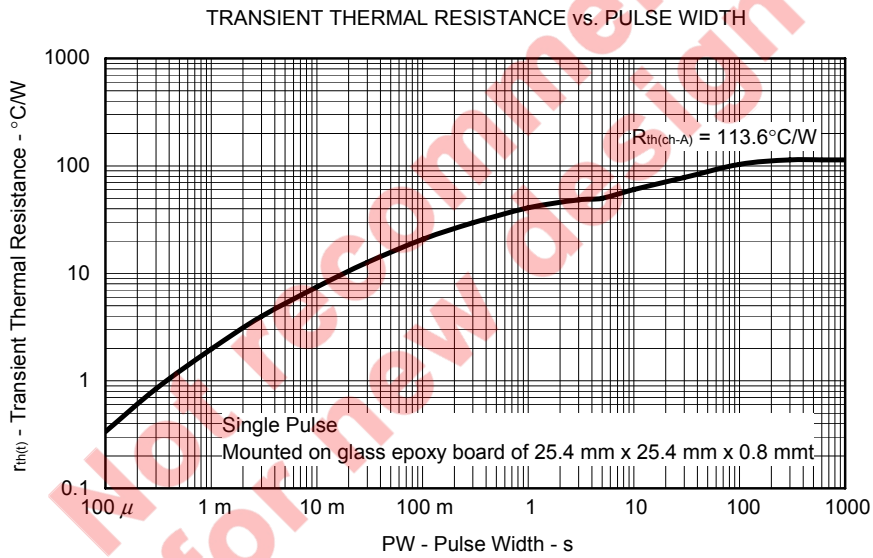
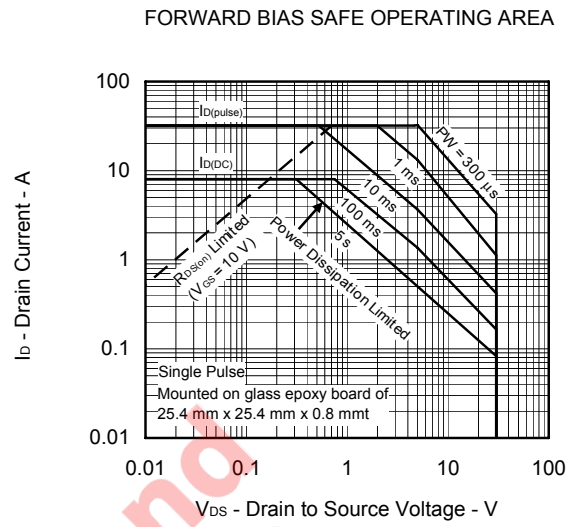
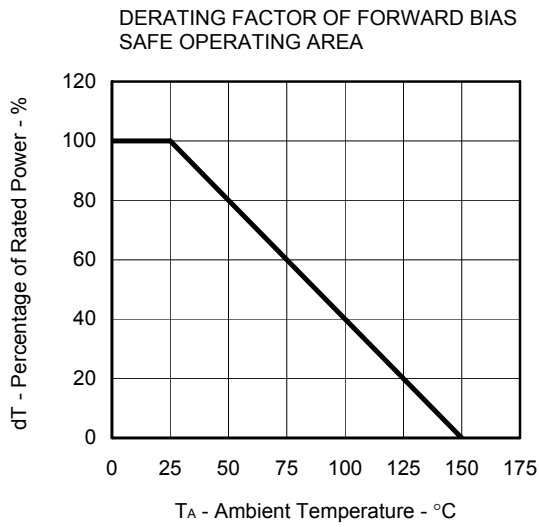
TEST CIRCUIT 1 SWITCHING TIME



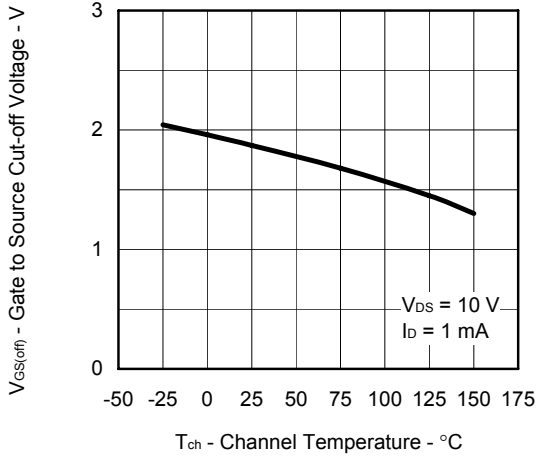
TEST CIRCUIT 2 GATE CHARGE



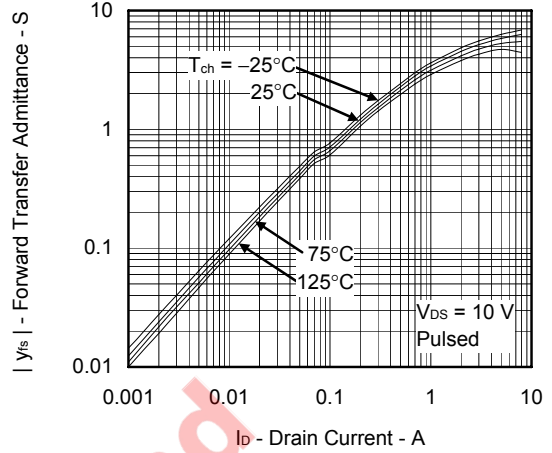
TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$)



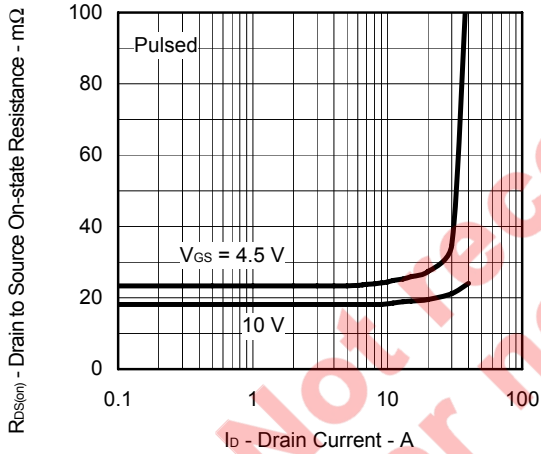
GATE TO SOURCE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



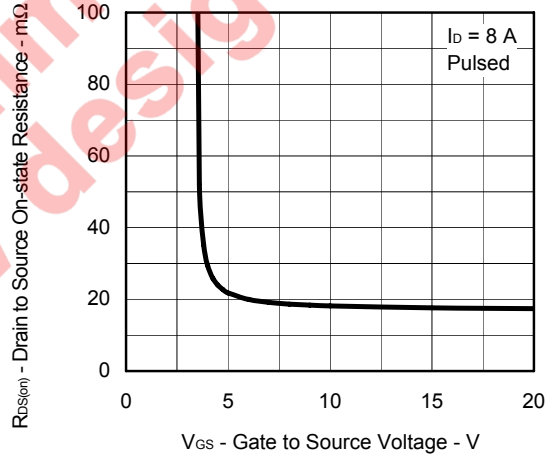
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



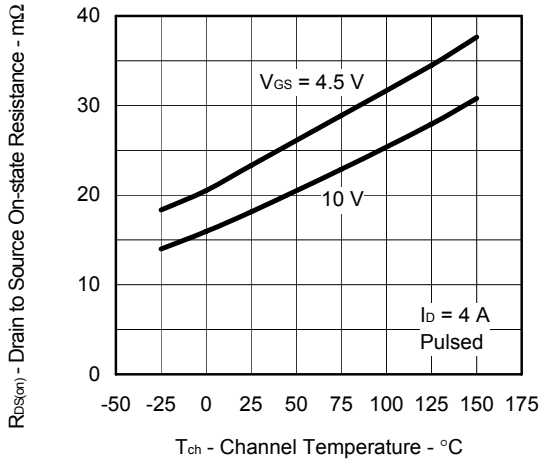
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



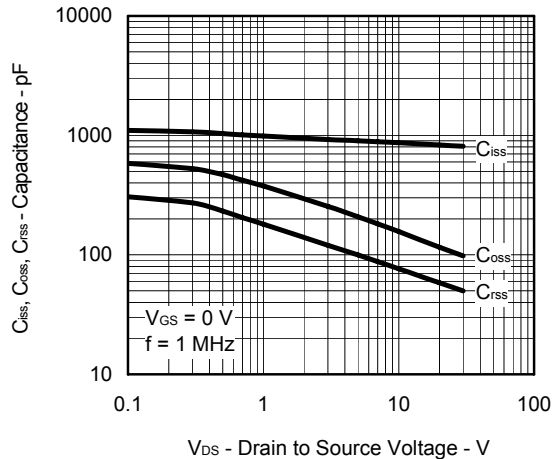
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



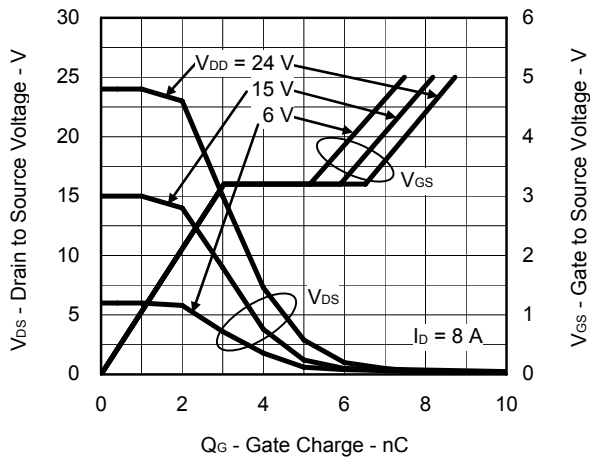
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



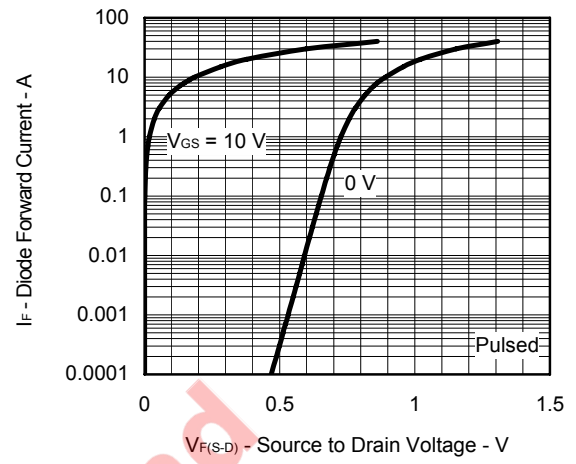
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE



Not recommended for new design

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