

To our customers,

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## Old Company Name in Catalogs and Other Documents

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April 1<sup>st</sup>, 2010  
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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**Phase-out/Discontinued**

**N-CHANNEL MOS FIELD EFFECT TRANSISTOR  
FOR SWITCHING**

**DESCRIPTION**

The μ PA2502, which has a heat spreader, is N-channel MOS Field Effect Transistor designed for DC/DC converter and power management applications of notebook computers.

**FEATURES**

- μ PA2502 has a thin surface mount package with a heat spreader. The land size is same as 8-pin TSSOP.
- Low on-state resistance  
 $R_{DS(on)1} = 12.0 \text{ m}\Omega \text{ MAX. (} V_{GS} = 10.0 \text{ V, } I_D = 7.0 \text{ A)}$   
 $R_{DS(on)2} = 18.0 \text{ m}\Omega \text{ MAX. (} V_{GS} = 4.5 \text{ V, } I_D = 7.0 \text{ A)}$
- Low  $C_{iss}$ : 760 pF TYP. ( $V_{DS} = 10.0 \text{ V, } V_{GS} = 0 \text{ V}$ )

**ORDERING INFORMATION**

PART NUMBER	PACKAGE
μ PA2502TM	8PIN HWSO

**ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub> = 25°C)**

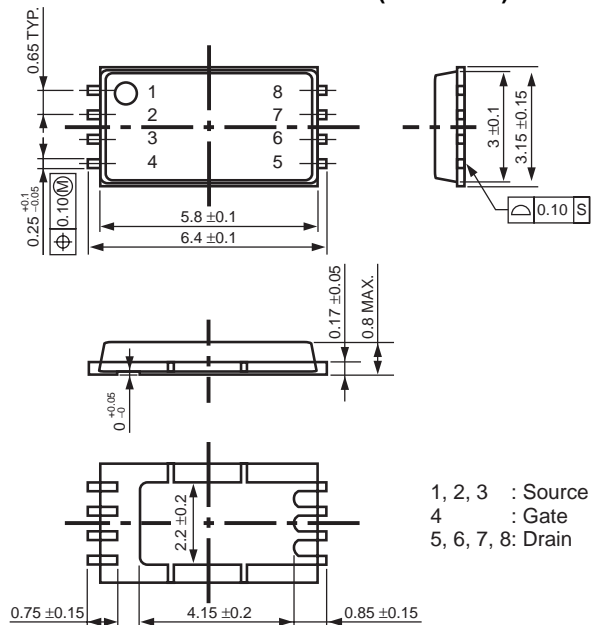
Drain to Source Voltage ( $V_{GS} = 0 \text{ V}$ )	$V_{DSS}$	30.0	V
Gate to Source Voltage ( $V_{DS} = 0 \text{ V}$ )	$V_{GSS}$	±20.0	V
Drain Current (DC) <sup>Note1</sup>	$I_{D(DC)}$	±13.0	A
Drain Current (pulse) <sup>Note2</sup>	$I_{D(pulse)}$	±52.0	A
Total Power Dissipation <sup>Note1</sup>	$P_T$	2.7	W
Channel Temperature	$T_{ch}$	150	°C
Storage Temperature	$T_{stg}$	-55 to +150	°C
Single Avalanche Current <sup>Note3</sup>	$I_{AS}$	13.0	A
Single Avalanche Energy <sup>Note3</sup>	$E_{AS}$	16.9	mJ

- Notes**
1. Mounted on FR-4 board of 25 cm<sup>2</sup> x 1.6 mm, PW ≤ 10 sec
  2. PW ≤ 10 μs, Duty Cycle ≤ 1%
  3. Starting  $T_{ch} = 25^\circ\text{C}$ ,  $V_{DD} = 15.0 \text{ V}$ ,  $R_G = 25 \Omega$ ,  $V_{GS} = 20.0 \rightarrow 0 \text{ V}$

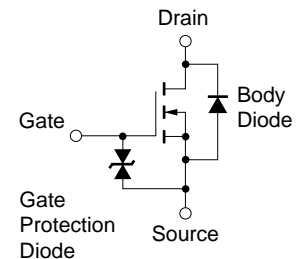
**Remark** The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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**PACKAGE DRAWING (Unit: mm)**



**EQUIVALENT CIRCUIT**

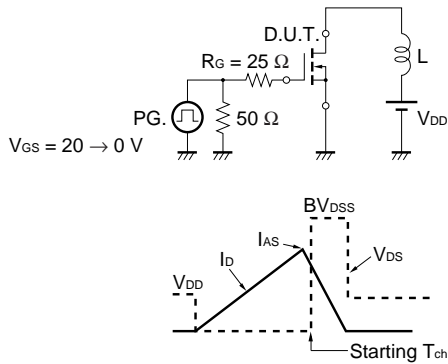


**ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25°C)**

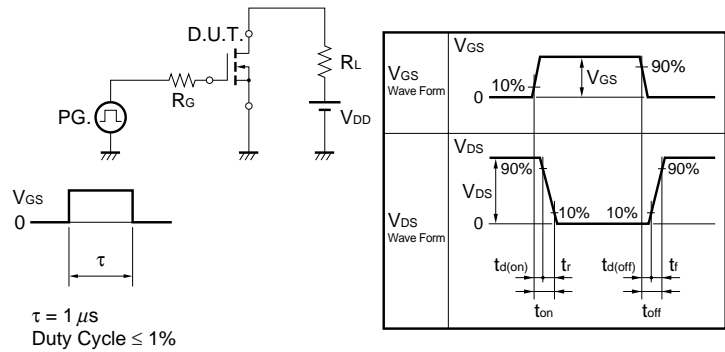
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 30.0 V, V <sub>GS</sub> = 0 V			1.0	μA
Gate Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±20.0 V, V <sub>DS</sub> = 0 V			±10.0	μA
Gate Cut-off Voltage	V <sub>GS(off)</sub>	V <sub>DS</sub> = 10.0 V, I <sub>D</sub> = 1.0 mA	1.50		2.50	V
Forward Transfer Admittance <b>Note</b>	y <sub>fs</sub>	V <sub>DS</sub> = 10.0 V, I <sub>D</sub> = 7.0 A	5			S
Drain to Source On-state Resistance <b>Note</b>	R <sub>DS(on)1</sub>	V <sub>GS</sub> = 10.0 V, I <sub>D</sub> = 7.0 A		9.3	12.0	mΩ
	R <sub>DS(on)2</sub>	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 7.0 A		13.1	18.0	mΩ
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 10.0 V		760		pF
Output Capacitance	C <sub>oss</sub>	V <sub>GS</sub> = 0 V		300		pF
Reverse Transfer Capacitance	C <sub>rss</sub>	f = 1.0 MHz		100		pF
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 15.0 V, I <sub>D</sub> = 7.0 A		14		ns
Rise Time	t <sub>r</sub>	V <sub>GS</sub> = 10.0 V		3		ns
Turn-off Delay Time	t <sub>d(off)</sub>	R <sub>G</sub> = 10 Ω		32		ns
Fall Time	t <sub>f</sub>			4		ns
Total Gate Charge	Q <sub>G</sub>	V <sub>DD</sub> = 15.0 V		8.5		nC
Gate to Source Charge	Q <sub>GS</sub>	V <sub>GS</sub> = 5.0 V		2.8		nC
Gate to Drain Charge	Q <sub>GD</sub>	I <sub>D</sub> = 13.0 A		3.5		nC
Body Diode Forward Voltage <b>Note</b>	V <sub>F(S-D)</sub>	I <sub>F</sub> = 13.0 A, V <sub>GS</sub> = 0 V		0.84		V
Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 13.0 A, V <sub>GS</sub> = 0 V		27		ns
Reverse Recovery Charge	Q <sub>rr</sub>	di/dt = 100 A/μs		24		nC

**Note** Pulsed: PW ≤ 350 μs, Duty Cycle ≤ 2%

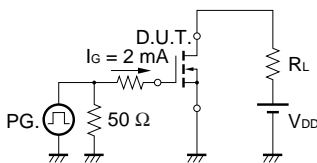
**TEST CIRCUIT 1 AVALANCHE CAPABILITY**



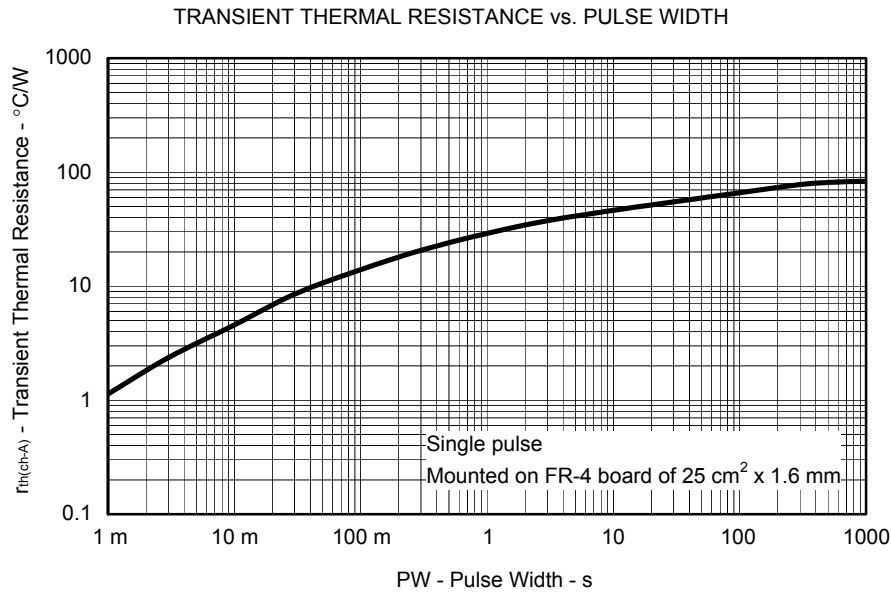
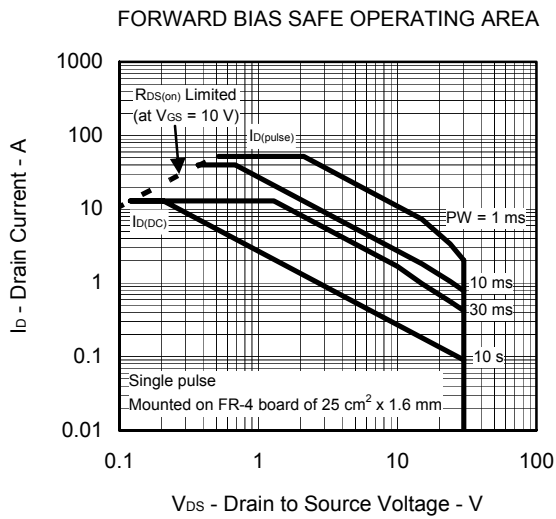
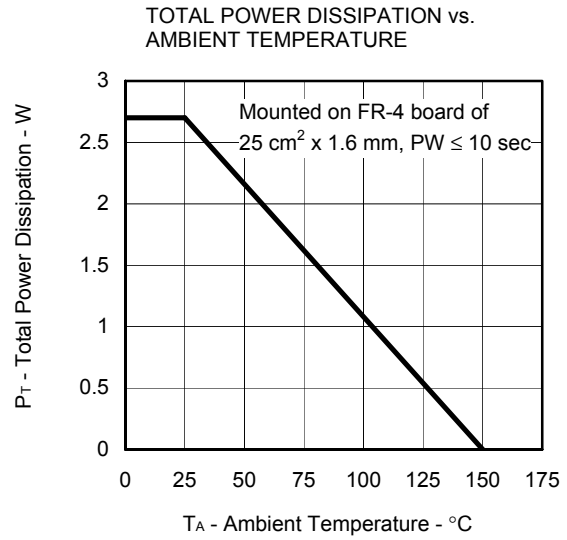
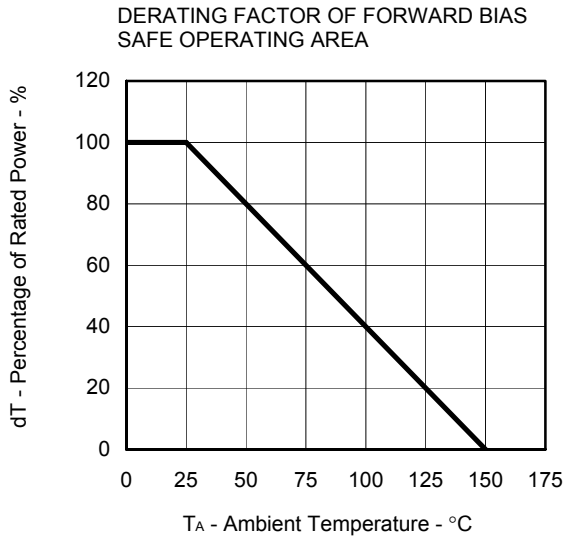
**TEST CIRCUIT 2 SWITCHING TIME**



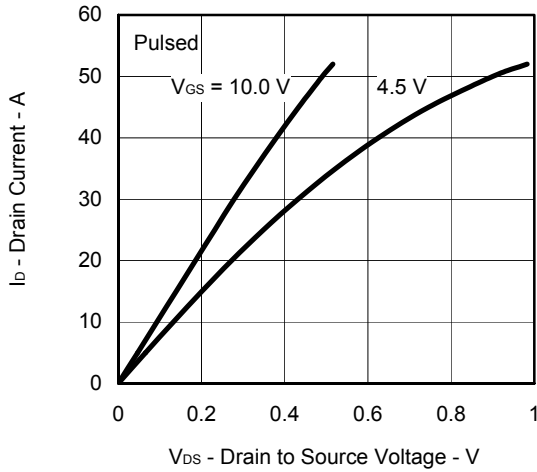
**TEST CIRCUIT 3 GATE CHARGE**



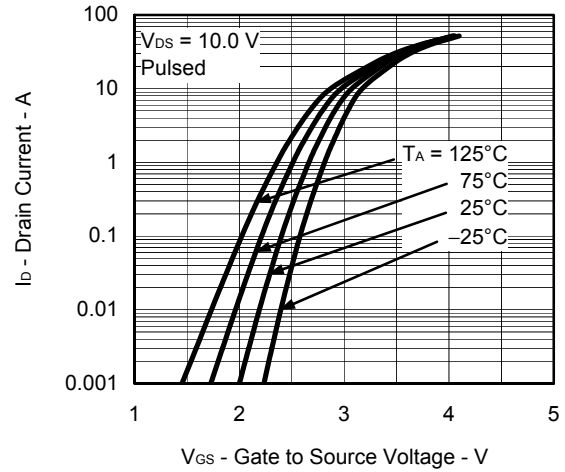
**TYPICAL CHARACTERISTICS (T<sub>A</sub> = 25°C)**



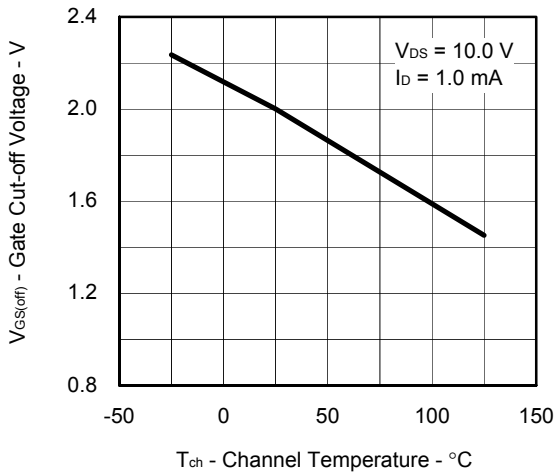
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



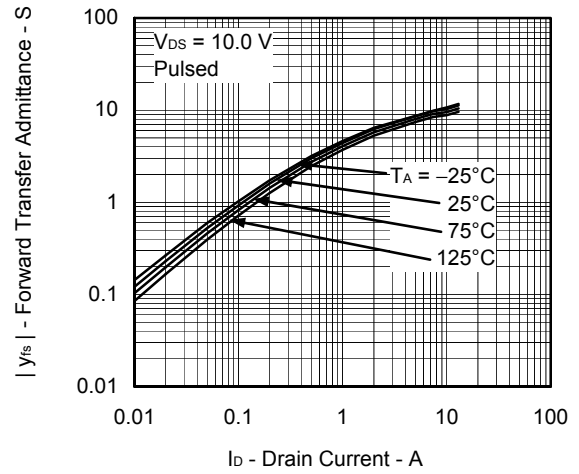
FORWARD TRANSFER CHARACTERISTICS



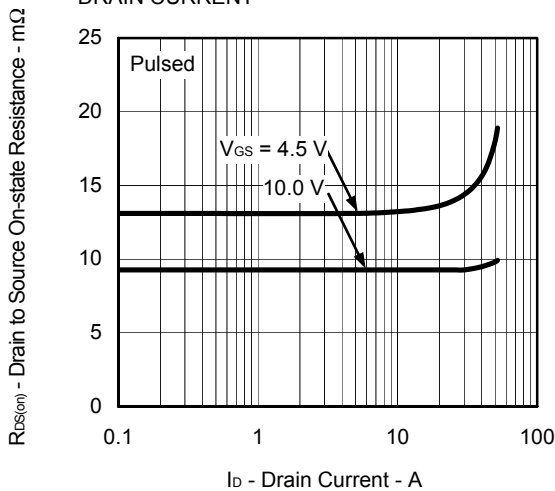
GATE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



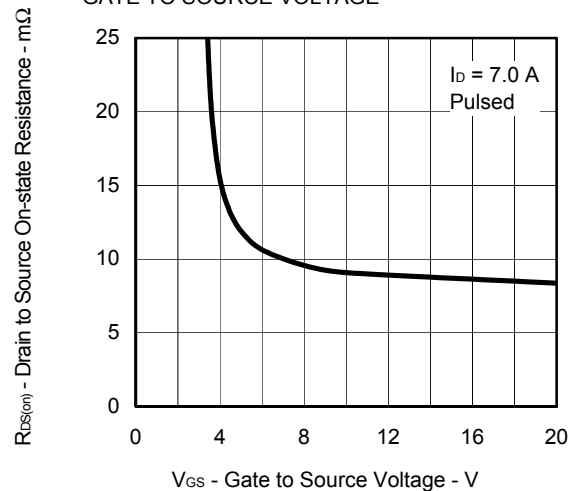
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



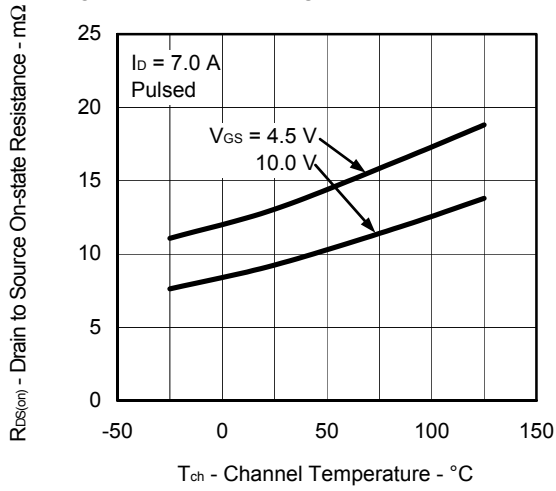
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



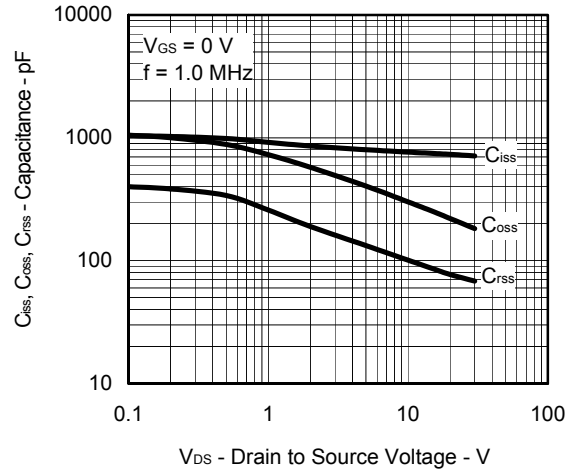
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



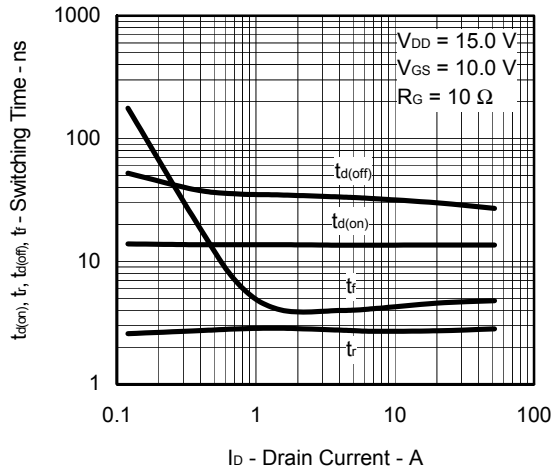
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



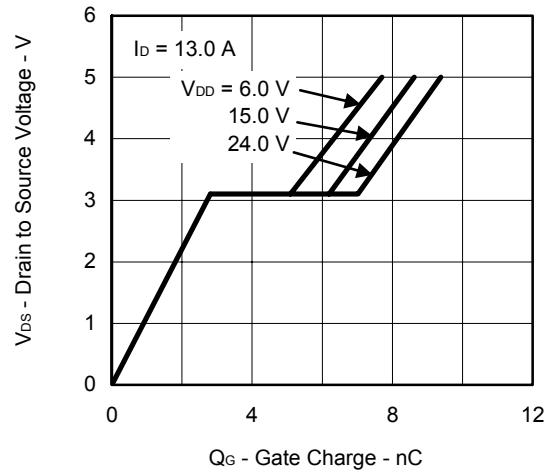
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



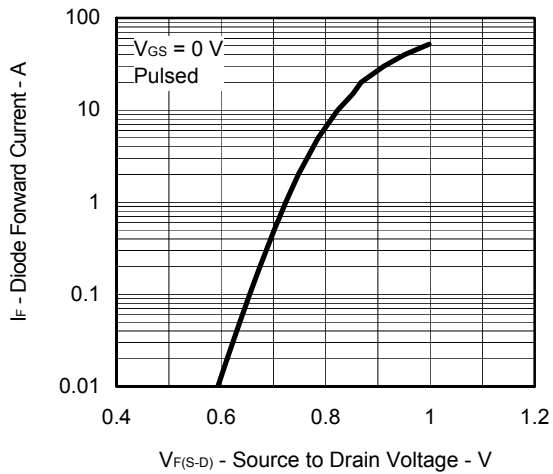
SWITCHING CHARACTERISTICS



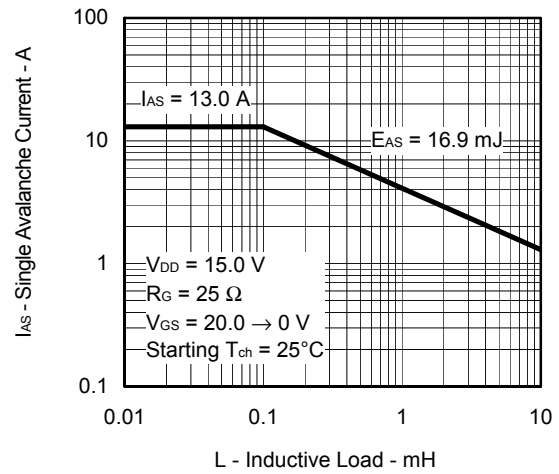
DYNAMIC INPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE

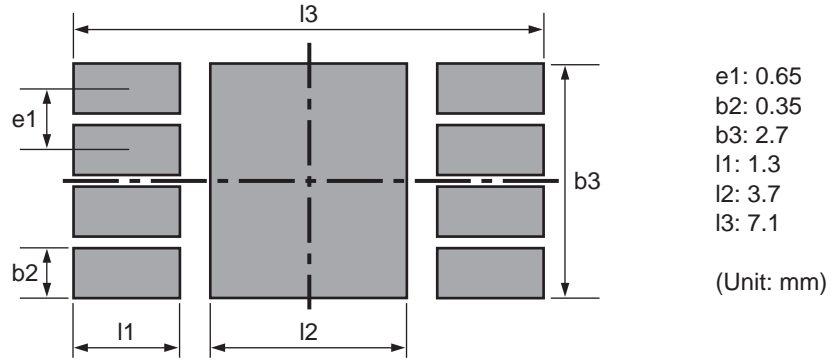


SINGLE AVALANCHE CURRENT vs. INDUCTIVE LOAD



**EXAMPLE OF THE LAND PATTERN**

Please optimize the land pattern in consideration of density, appearance of solder fillets, common difference, etc in an actual design.





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