

To our customers,

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## Old Company Name in Catalogs and Other Documents

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April 1<sup>st</sup>, 2010  
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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**Phase-out/Discontinued**

**P-CHANNEL MOS FIELD EFFECT TRANSISTOR  
FOR SWITCHING**

**DESCRIPTION**

The μ PA2510, which has a heat spreader, is P-channel MOS Field Effect Transistor designed for power management applications of notebook computers.

**FEATURES**

- μ PA2510 has a thin surface mount package with a heat spreader. The land size is same as 8-pin TSSOP.
- Low on-state resistance  
 $R_{DS(on)1} = 10.1 \text{ m}\Omega \text{ MAX. (} V_{GS} = -10.0 \text{ V, } I_D = -9.0 \text{ A)}$   
 $R_{DS(on)2} = 14.0 \text{ m}\Omega \text{ MAX. (} V_{GS} = -4.5 \text{ V, } I_D = -9.0 \text{ A)}$
- Low  $C_{iss}$ : 3000 pF TYP. ( $V_{DS} = -10.0 \text{ V, } V_{GS} = 0 \text{ V}$ )

**ORDERING INFORMATION**

PART NUMBER	PACKAGE
μ PA2510TM	8PIN HWSO

**ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub> = 25°C)**

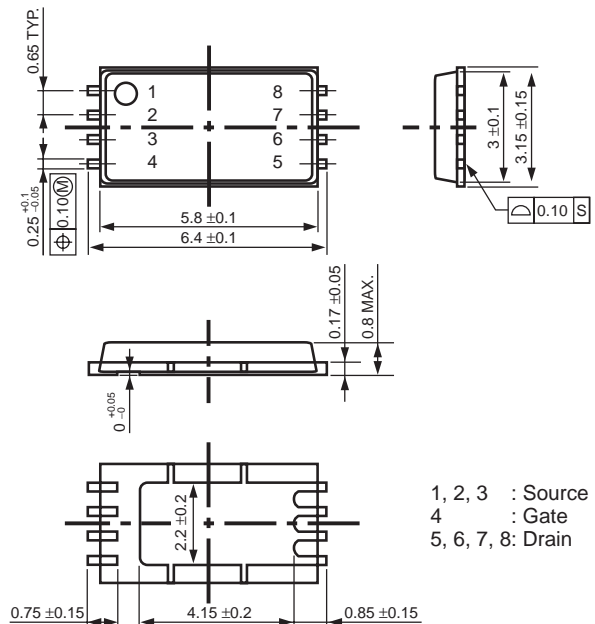
Drain to Source Voltage ( $V_{GS} = 0 \text{ V}$ )	$V_{DSS}$	-30.0	V
Gate to Source Voltage ( $V_{DS} = 0 \text{ V}$ )	$V_{GSS}$	±20.0	V
Drain Current (DC) <sup>Note1</sup>	$I_{D(DC)}$	±18.0	A
Drain Current (pulse) <sup>Note2</sup>	$I_{D(pulse)}$	±72.0	A
Total Power Dissipation <sup>Note1</sup>	$P_T$	2.7	W
Channel Temperature	$T_{ch}$	150	°C
Storage Temperature	$T_{stg}$	-55 to +150	°C
Single Avalanche Current <sup>Note3</sup>	$I_{AS}$	-18.0	A
Single Avalanche Energy <sup>Note3</sup>	$E_{AS}$	32.4	mJ

- Notes**
1. Mounted on FR-4 board of 25 cm<sup>2</sup> x 1.6 mm, PW ≤ 10 sec
  2. PW ≤ 10 μs, Duty Cycle ≤ 1%
  3. Starting  $T_{ch} = 25^\circ\text{C}$ ,  $V_{DD} = -30 \text{ V}$ ,  $R_G = 25 \Omega$ ,  $V_{GS} = -20.0 \rightarrow 0 \text{ V}$

**Remark** The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

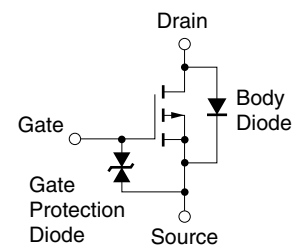
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**PACKAGE DRAWING (Unit: mm)**



1, 2, 3 : Source  
 4 : Gate  
 5, 6, 7, 8: Drain

**EQUIVALENT CIRCUIT**

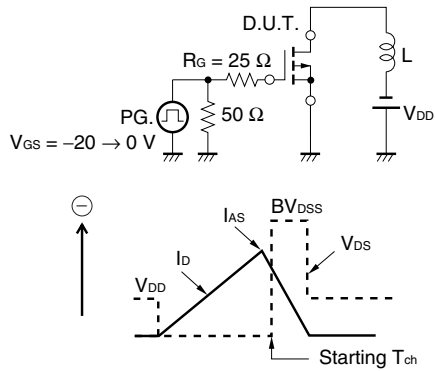


**ELECTRICAL CHARACTERISTICS (TA = 25°C)**

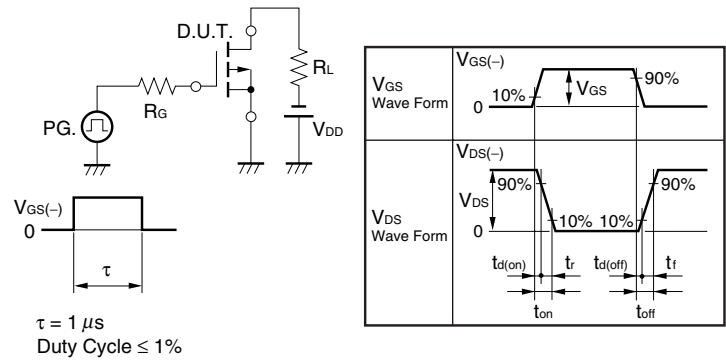
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = -30.0\text{ V}, V_{GS} = 0\text{ V}$			-1.0	$\mu\text{A}$
Gate Leakage Current	$I_{GSS}$	$V_{GS} = \pm 20.0\text{ V}, V_{DS} = 0\text{ V}$			$\pm 10.0$	$\mu\text{A}$
Gate Cut-off Voltage	$V_{GS(off)}$	$V_{DS} = -10.0\text{ V}, I_D = -1.0\text{ mA}$	-1.0		-2.5	V
Forward Transfer Admittance <b>Note</b>	$ y_{fs} $	$V_{DS} = -10.0\text{ V}, I_D = -9.0\text{ A}$	12			S
Drain to Source On-state Resistance <b>Note</b>	$R_{DS(on)1}$	$V_{GS} = -10.0\text{ V}, I_D = -9.0\text{ A}$		7.5	10.1	$\text{m}\Omega$
	$R_{DS(on)2}$	$V_{GS} = -4.5\text{ V}, I_D = -9.0\text{ A}$		9.5	14.0	$\text{m}\Omega$
Input Capacitance	$C_{iss}$	$V_{DS} = -10.0\text{ V}$		3000		pF
Output Capacitance	$C_{oss}$	$V_{GS} = 0\text{ V}$		940		pF
Reverse Transfer Capacitance	$C_{rss}$	$f = 1.0\text{ MHz}$		500		pF
Turn-on Delay Time	$t_{d(on)}$	$V_{DD} = -15.0\text{ V}, I_D = -9.0\text{ A}$		12		ns
Rise Time	$t_r$	$V_{GS} = -10.0\text{ V}$		18		ns
Turn-off Delay Time	$t_{d(off)}$	$R_G = 10\ \Omega$		270		ns
Fall Time	$t_f$			170		ns
Total Gate Charge	$Q_G$	$V_{DD} = -24.0\text{ V}$		70		nC
Gate to Source Charge	$Q_{GS}$	$V_{GS} = -10.0\text{ V}$		8		nC
Gate to Drain Charge	$Q_{GD}$	$I_D = -18.0\text{ A}$		22		nC
Body Diode Forward Voltage <b>Note</b>	$V_{F(S-D)}$	$I_F = 18.0\text{ A}, V_{GS} = 0\text{ V}$		0.85		V
Reverse Recovery Time	$t_{rr}$	$I_F = 18.0\text{ A}, V_{GS} = 0\text{ V}$		80		ns
Reverse Recovery Charge	$Q_{rr}$	$di/dt = 100\text{ A}/\mu\text{s}$		68		nC

**Note** Pulsed:  $PW \leq 350\ \mu\text{s}$ , Duty Cycle  $\leq 2\%$

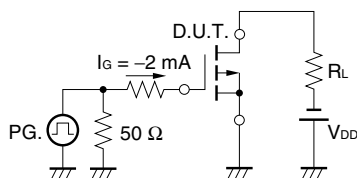
**TEST CIRCUIT 1 AVALANCHE CAPABILITY**



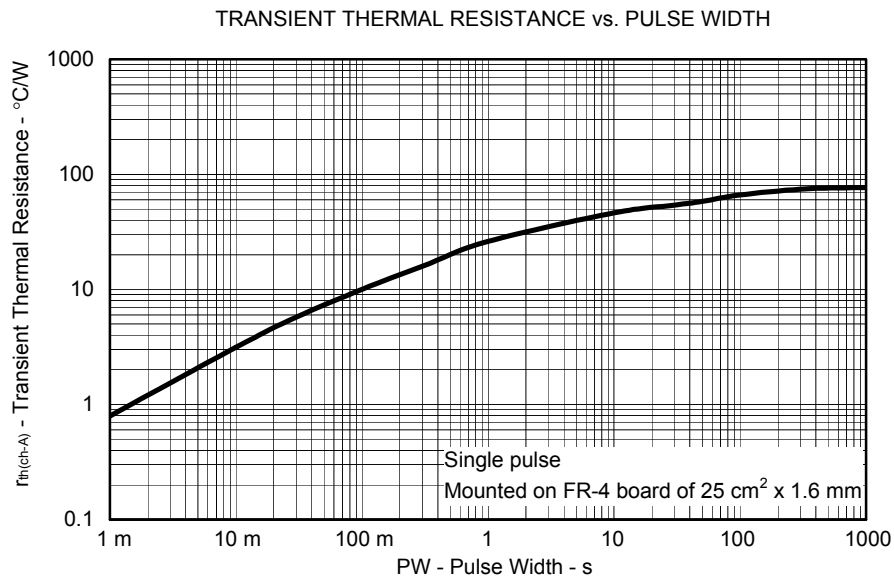
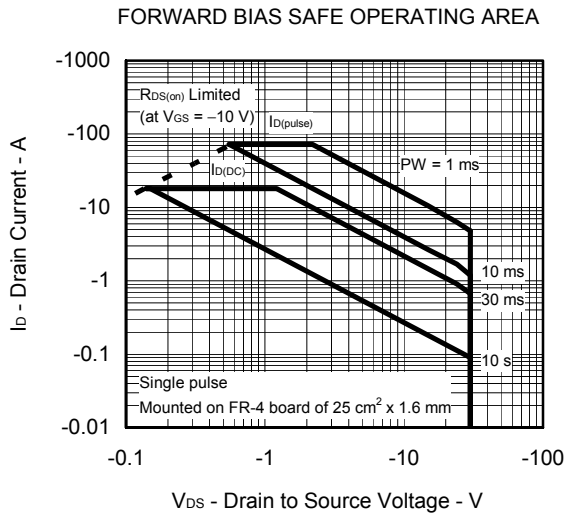
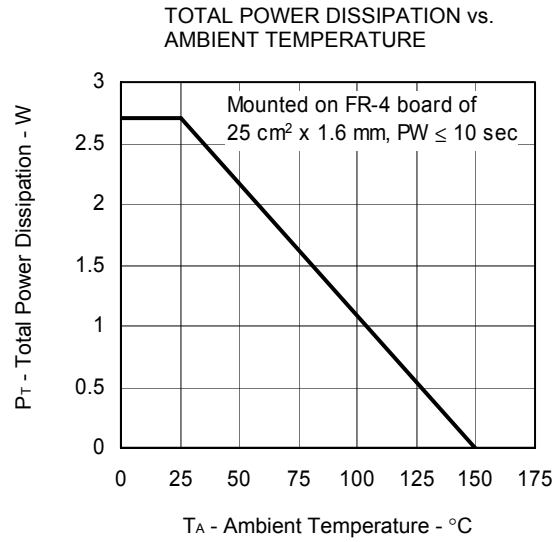
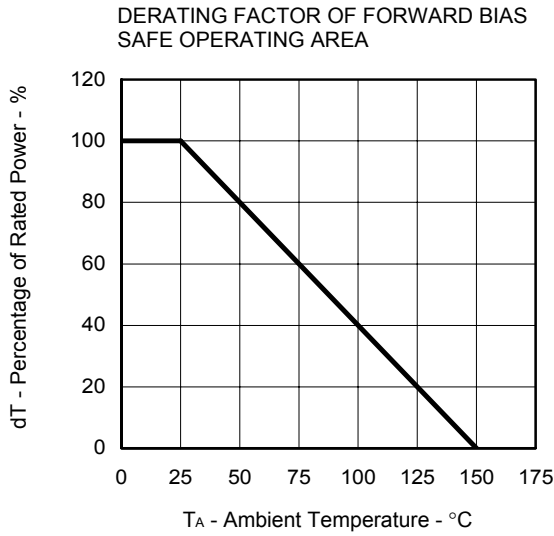
**TEST CIRCUIT 2 SWITCHING TIME**



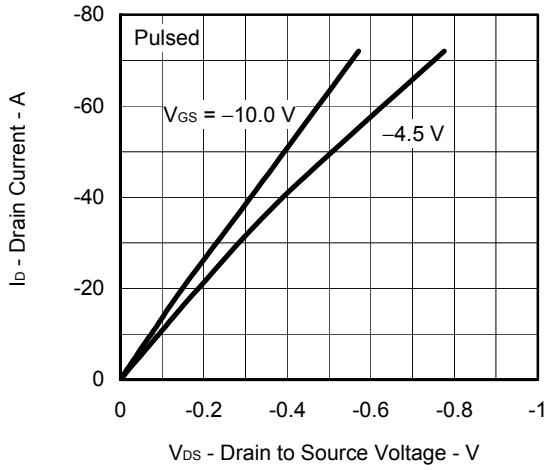
**TEST CIRCUIT 3 GATE CHARGE**



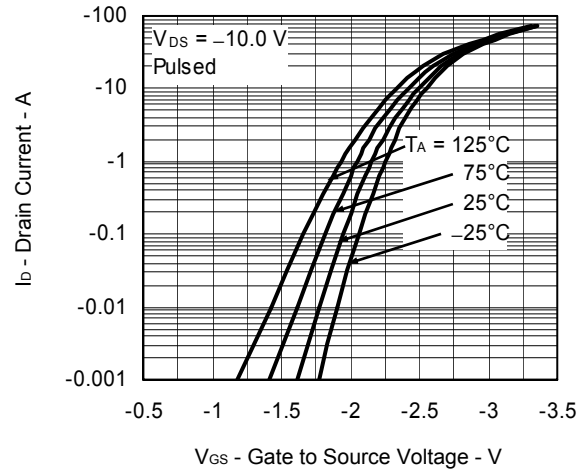
**TYPICAL CHARACTERISTICS (T<sub>A</sub> = 25°C)**



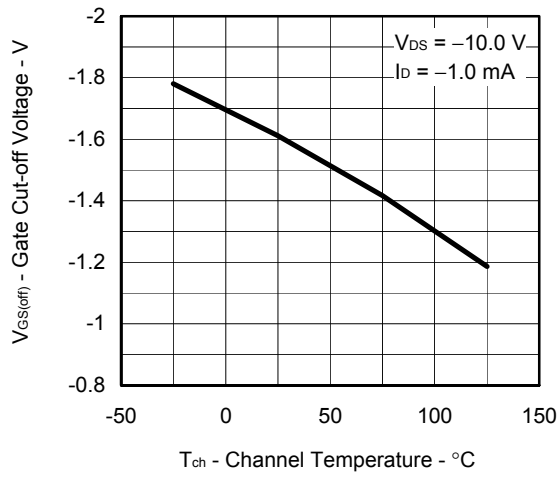
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



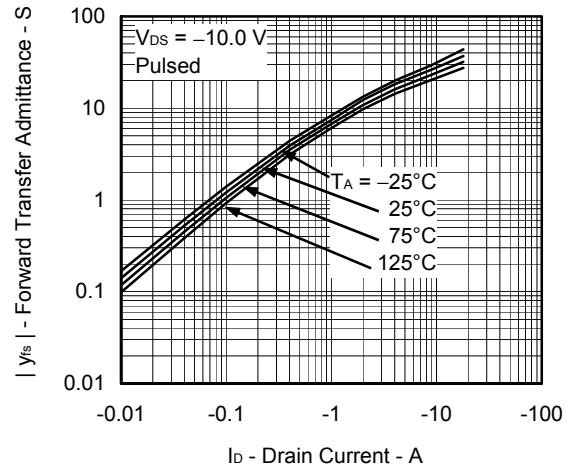
FORWARD TRANSFER CHARACTERISTICS



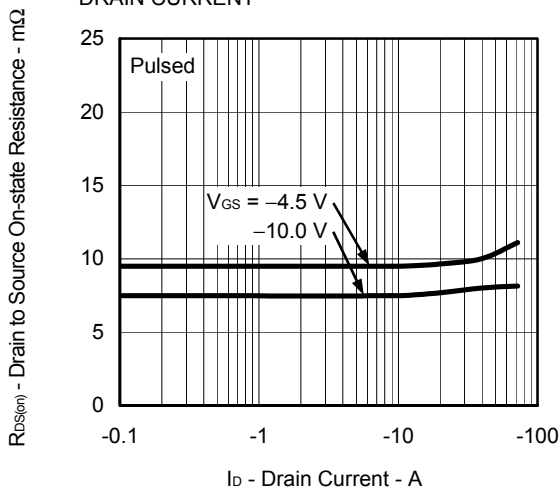
GATE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



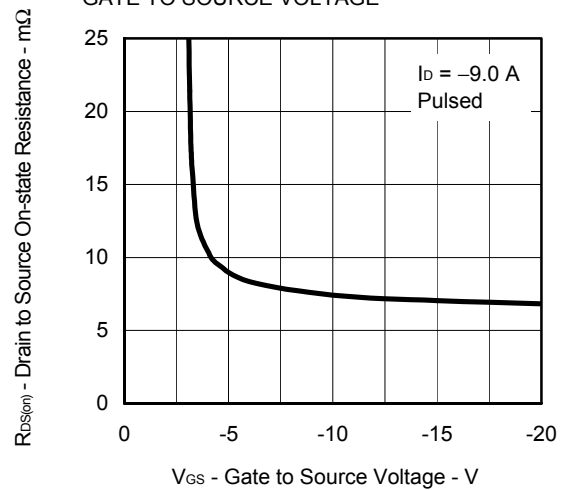
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



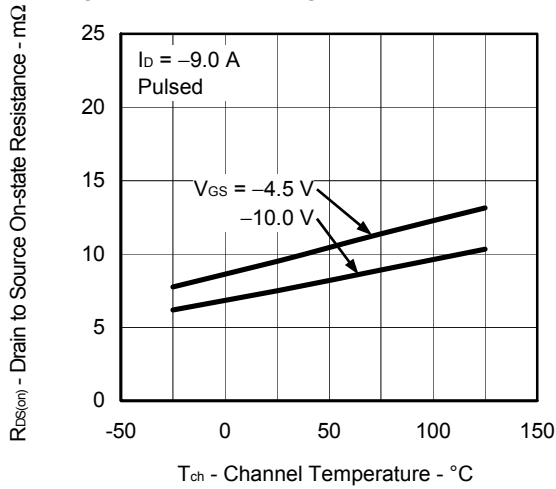
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



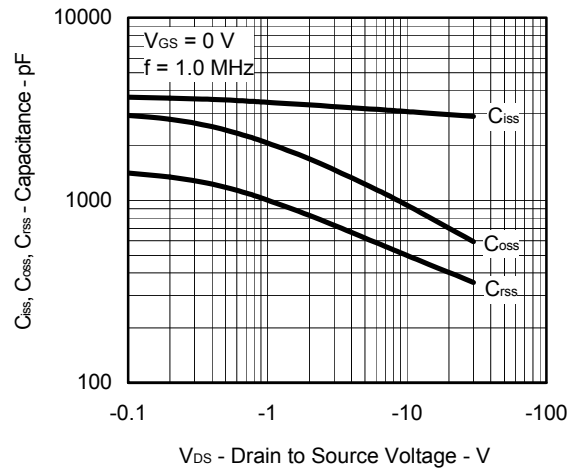
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



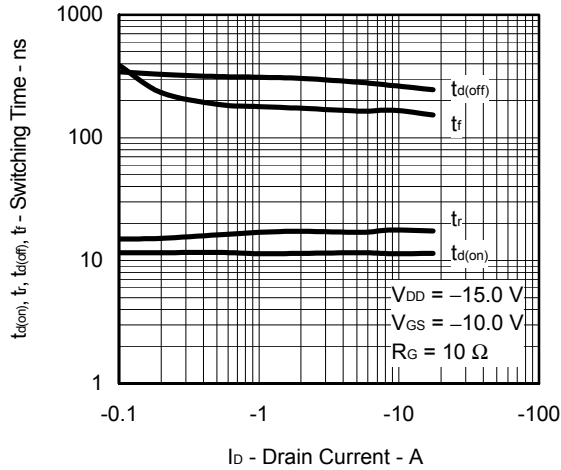
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



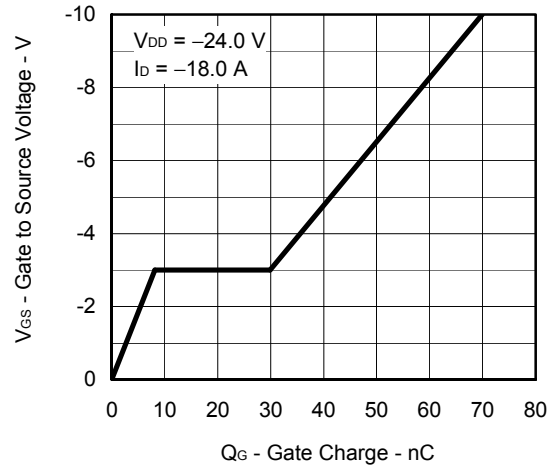
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



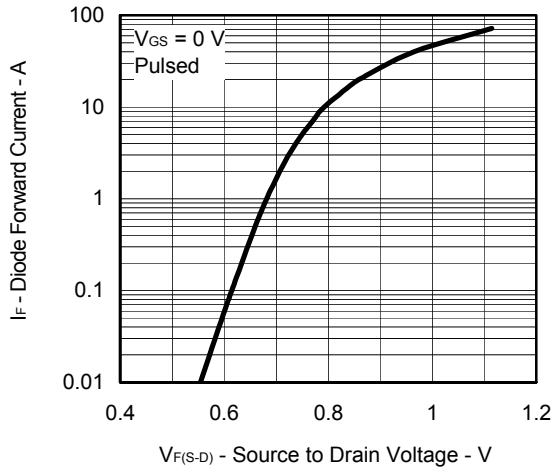
SWITCHING CHARACTERISTICS



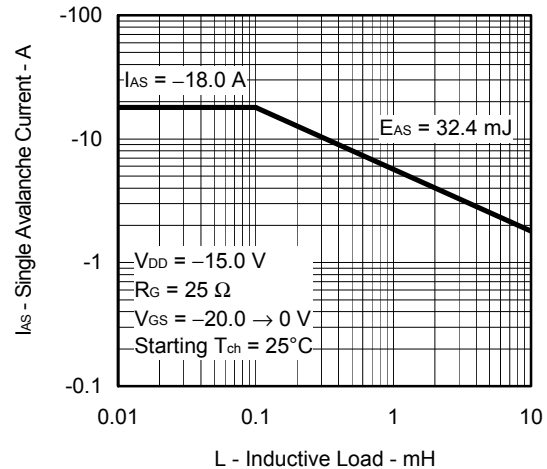
DYNAMIC INPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE

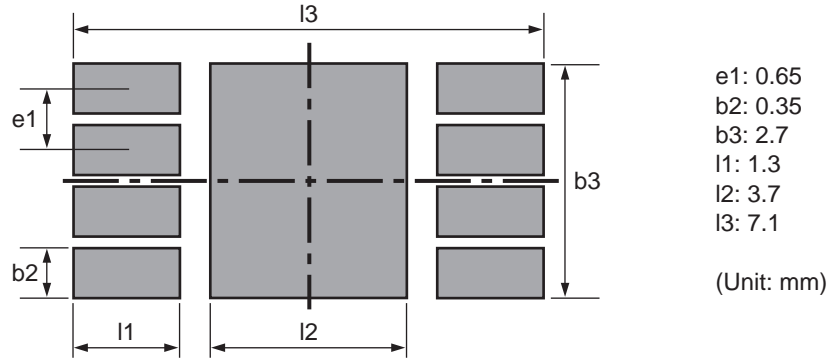


SINGLE AVALANCHE CURRENT vs. INDUCTIVE LOAD



**EXAMPLE OF THE LAND PATTERN**

Please optimize the land pattern in consideration of density, appearance of solder fillets, common difference, etc in an actual design.





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