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Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: <http://www.renesas.com>

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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Not recommended
for new design

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SWITCHING
 N-CHANNEL POWER MOSFET

DESCRIPTION

The μ PA2709GR is N-channel MOS Field Effect Transistor designed for DC/DC converter and power management applications of notebook computer.

FEATURES

- Low on-state resistance
 $R_{DS(on)1} = 10.5 \text{ m}\Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 7.0 \text{ A)}$
 $R_{DS(on)2} = 15 \text{ m}\Omega \text{ MAX. (} V_{GS} = 4.5 \text{ V, } I_D = 7.0 \text{ A)}$
- Low Q_{GD} : $Q_{GD} = 3.3 \text{ nC TYP. (} V_{DD} = 15 \text{ V, } I_D = 13 \text{ A)}$
- Built-in gate protection diode
- Small and surface mount package (Power SOP8)

ORDERING INFORMATION

PART NUMBER	PACKAGE
μ PA2709GR-E1-A ^{Note}	Power SOP8
μ PA2709GR-E2-A ^{Note}	Power SOP8

Note Pb-free (This product does not contain Pb in external electrode and other parts.)

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$, All terminals are connected.)

Drain to Source Voltage ($V_{GS} = 0 \text{ V}$)	V_{DSS}	30	V
Gate to Source Voltage ($V_{DS} = 0 \text{ V}$)	V_{GSS}	± 20	V
Drain Current (DC)	$I_{D(DC)}$	± 13	A
Drain Current (pulse) ^{Note1}	$I_{D(pulse)}$	± 52	A
Total Power Dissipation ^{Note2}	P_{T1}	1.1	W
Total Power Dissipation ($PW = 10 \text{ sec}$) ^{Note2}	P_{T2}	2.5	W
Channel Temperature	T_{ch}	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	$-55 \text{ to } +150$	$^\circ\text{C}$
Single Avalanche Current ^{Note3}	I_{AS}	13	A
Single Avalanche Energy ^{Note3}	E_{AS}	17	mJ

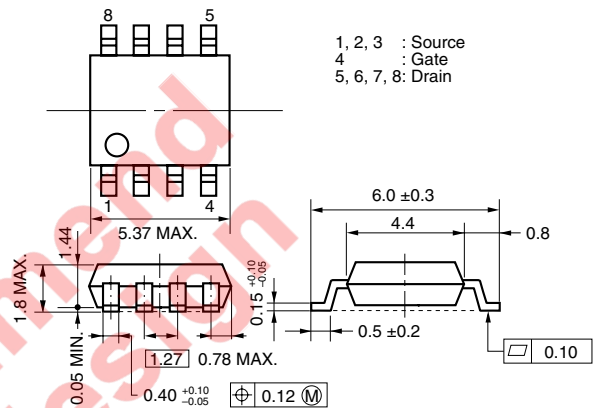
Notes 1. $PW \leq 10 \mu\text{s}$, Duty Cycle $\leq 1\%$

2. Mounted on glass epoxy board of 25.4 mm x 25.4 mm x 0.8 mm

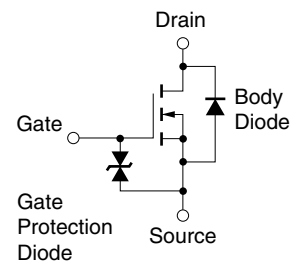
3. Starting $T_{ch} = 25^\circ\text{C}$, $V_{DD} = 15 \text{ V}$, $R_G = 25 \Omega$, $V_{GS} = 20 \rightarrow 0 \text{ V}$, $L = 100 \mu\text{H}$

Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

PACKAGE DRAWING (Unit: mm)



EQUIVALENT CIRCUIT



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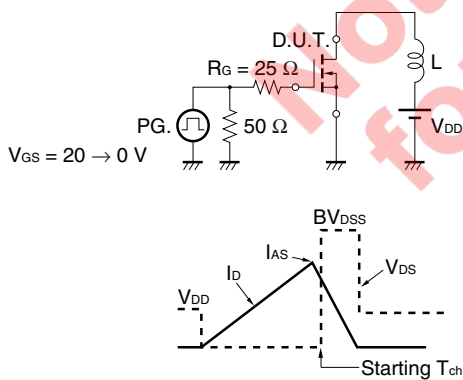
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ELECTRICAL CHARACTERISTICS (T_A = 25°C, All terminals are connected.)

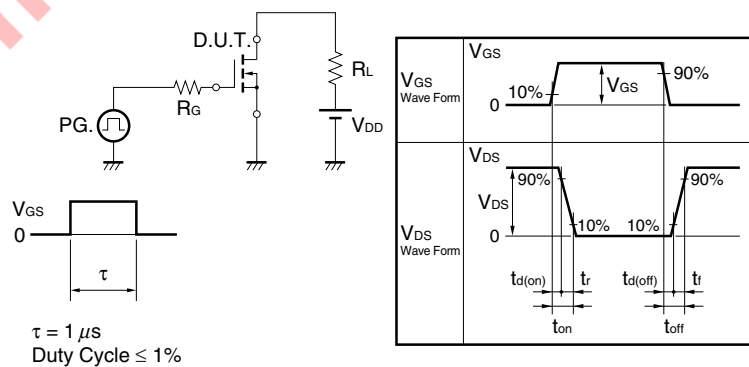
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 30 V, V _{GS} = 0 V			10	μA
Gate Leakage Current	I _{GSS}	V _{GS} = ±20 V, V _{DS} = 0 V			±10	μA
Gate Cut-off Voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1 mA	1.5		2.5	V
Forward Transfer Admittance ^{Note}	y _{fs}	V _{DS} = 10 V, I _D = 7.0 A	7			S
Drain to Source On-state Resistance ^{Note}	R _{DS(on)1}	V _{GS} = 10 V, I _D = 7.0 A		8.3	10.5	mΩ
	R _{DS(on)2}	V _{GS} = 4.5 V, I _D = 7.0 A		10.6	15	mΩ
Input Capacitance	C _{iss}	V _{DS} = 10 V		1270		pF
Output Capacitance	C _{oss}	V _{GS} = 0 V		320		pF
Reverse Transfer Capacitance	C _{rss}	f = 1 MHz		110		pF
Turn-on Delay Time	t _{d(on)}	V _{DD} = 15 V, I _D = 7.0 A		10		ns
Rise Time	t _r	V _{GS} = 10 V		5.3		ns
Turn-off Delay Time	t _{d(off)}	R _G = 10 Ω		40		ns
Fall Time	t _f			7.8		ns
Total Gate Charge	Q _G	V _{DD} = 15 V		11		nC
Gate to Source Charge	Q _{GS}	V _{GS} = 5 V		3.8		nC
Gate to Drain Charge	Q _{GD}	I _D = 13 A		3.3		nC
Body Diode Forward Voltage ^{Note}	V _{F(S-D)}	I _F = 13 A, V _{GS} = 0 V		0.8		V
Reverse Recovery Time	t _{rr}	I _F = 13 A, V _{GS} = 0 V		25		ns
Reverse Recovery Charge	Q _{rr}	di/dt = 100 A/μs		22		nC
Gate Resistance	R _G	f = 1 MHz		1.2		Ω

Note Pulsed

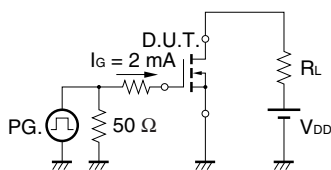
TEST CIRCUIT 1 AVALANCHE CAPABILITY



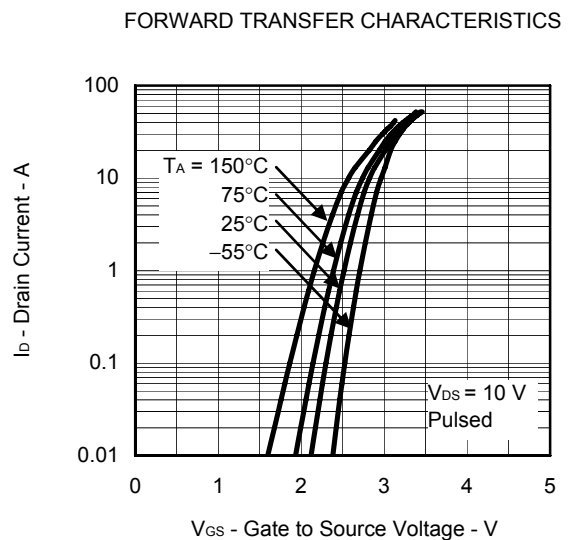
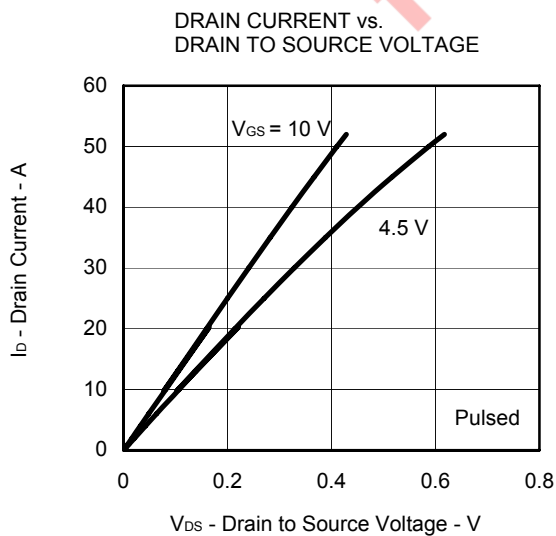
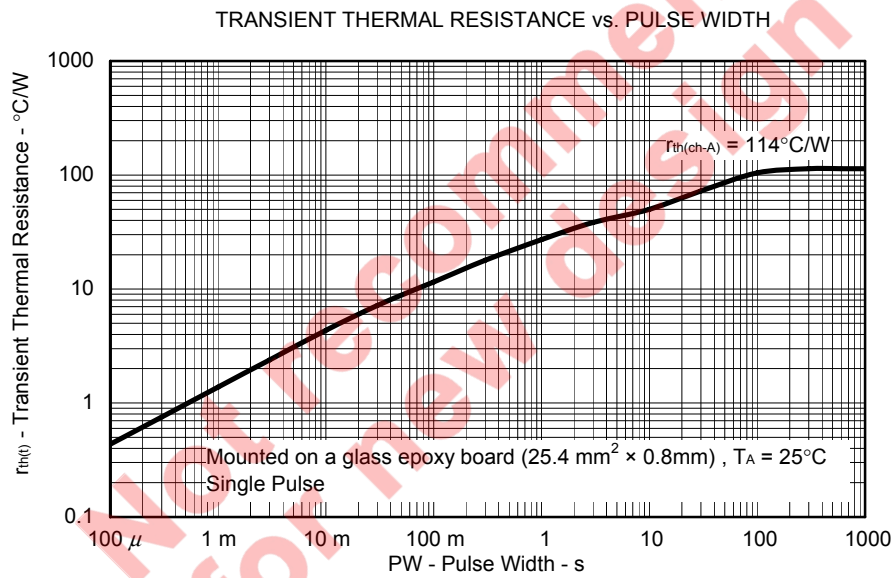
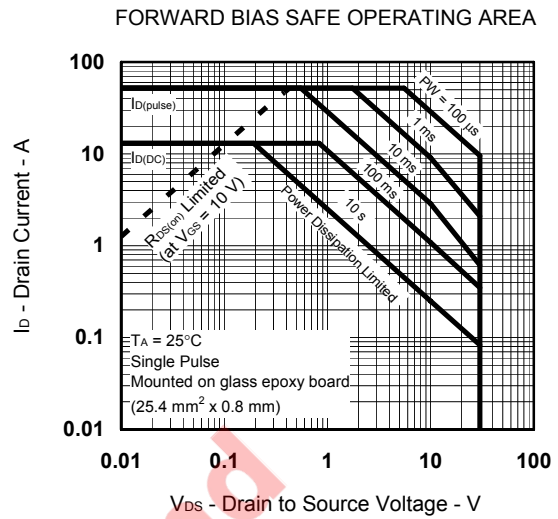
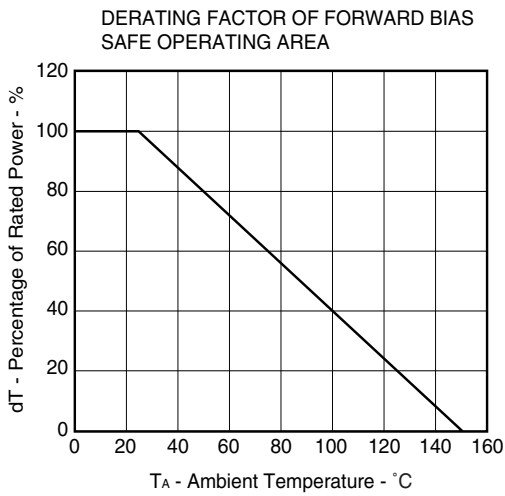
TEST CIRCUIT 2 SWITCHING TIME



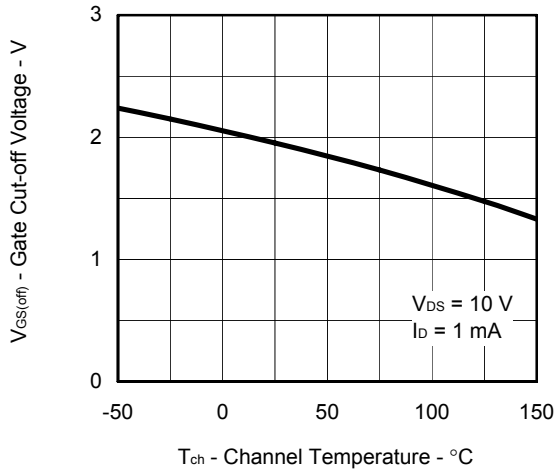
TEST CIRCUIT 3 GATE CHARGE



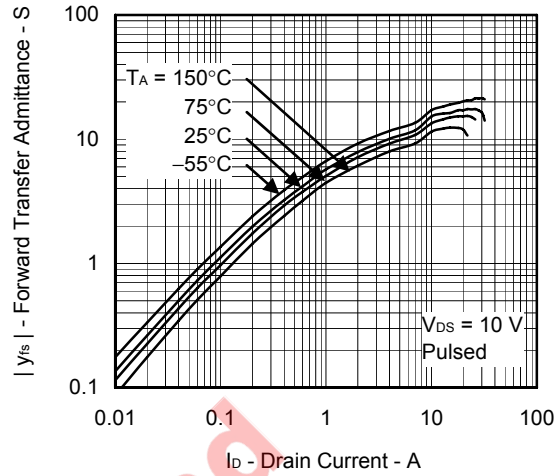
TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$)



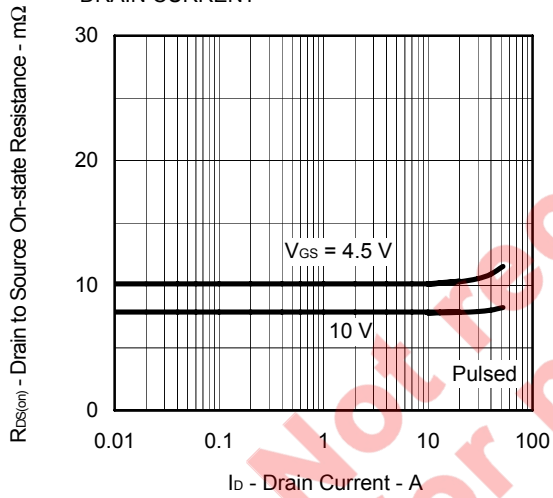
GATE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



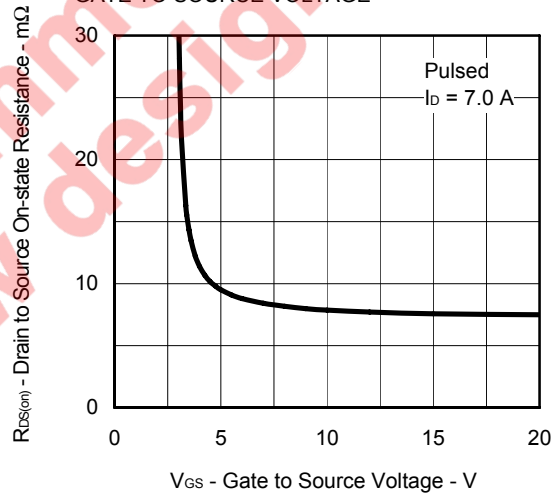
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



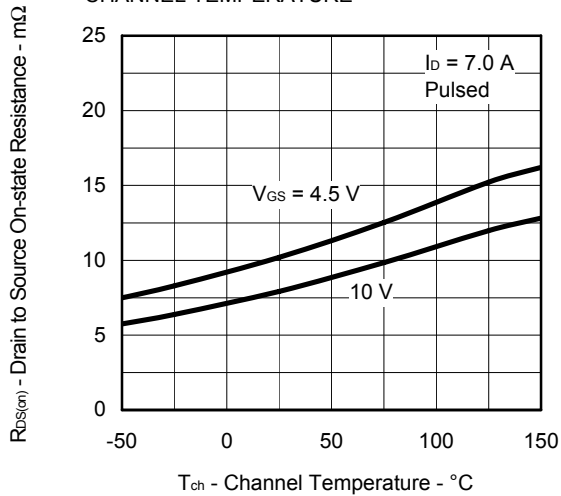
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



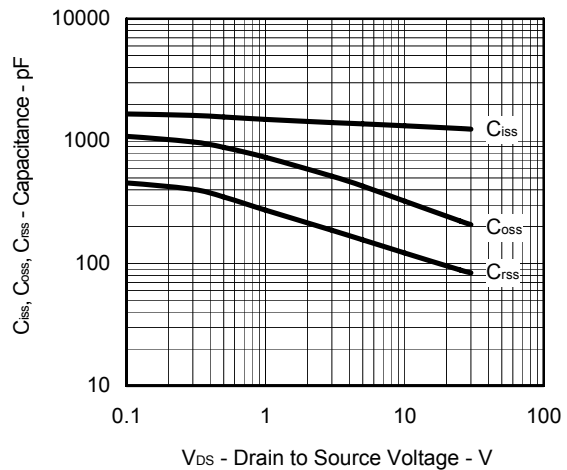
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



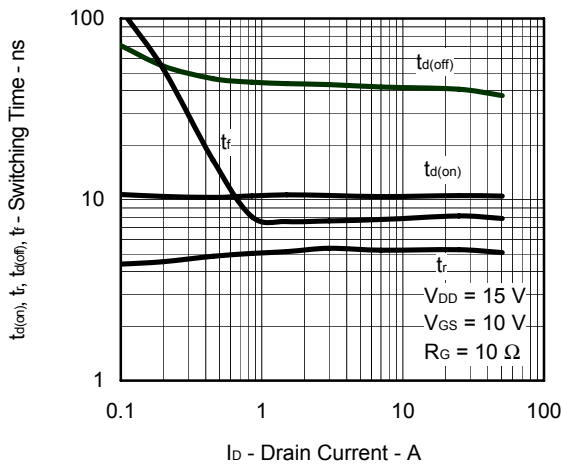
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



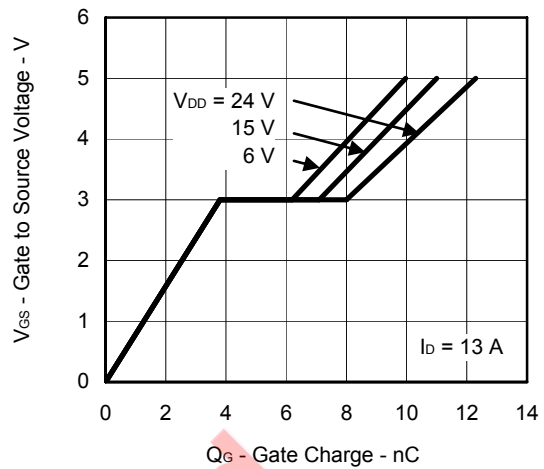
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



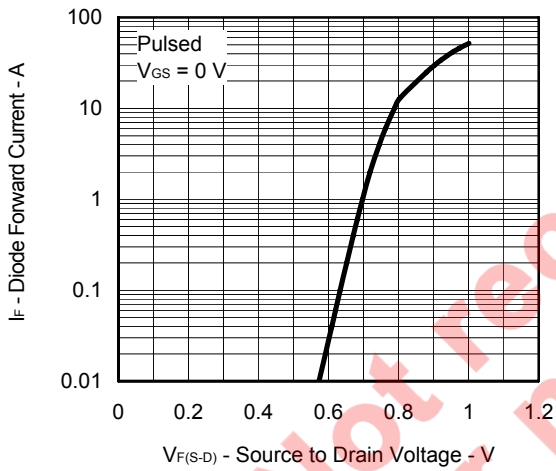
SWITCHING CHARACTERISTICS



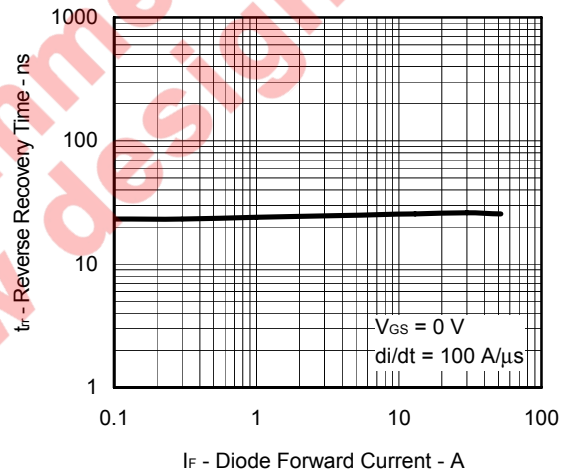
DYNAMIC INPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE



REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT



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