

To our customers,

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## Old Company Name in Catalogs and Other Documents

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April 1<sup>st</sup>, 2010  
Renesas Electronics Corporation

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# MOS FIELD EFFECT TRANSISTOR

## $\mu$ PA2718AGR

### SWITCHING

#### P-CHANNEL POWER MOS FET

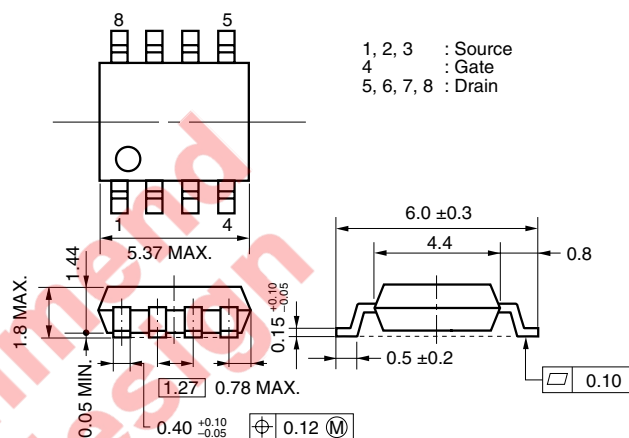
#### DESCRIPTION

The  $\mu$ PA2718AGR is P-Channel MOS Field Effect Transistor designed for power management applications of notebook computers and Lithium-Ion battery protection circuit.

#### FEATURES

- Low on-state resistance  
 $R_{DS(on)1} = 9.0 \text{ m}\Omega \text{ MAX. (} V_{GS} = -10 \text{ V, } I_D = -6.5 \text{ A)}$   
 $R_{DS(on)2} = 14.5 \text{ m}\Omega \text{ MAX. (} V_{GS} = -4.5 \text{ V, } I_D = -6.5 \text{ A)}$
- Low input capacitance  
 $C_{iss} = 2810 \text{ pF TYP.}$
- Built-in gate protection diode
- Small and surface mount package (Power SOP8)

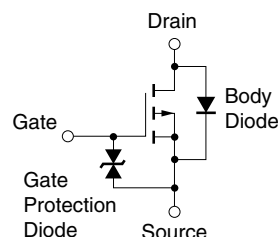
PACKAGE DRAWING (Unit: mm)



#### ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub> = 25°C, All terminals are connected.)

Drain to Source Voltage (V <sub>GS</sub> = 0 V)	V <sub>DSS</sub>	-30	V
Gate to Source Voltage (V <sub>DS</sub> = 0 V)	V <sub>GSS</sub>	±20	V
Drain Current (DC)	I <sub>D(DC)</sub>	±13	A
Drain Current (pulse) <sup>Note1</sup>	I <sub>D(pulse)</sub>	±130	A
Total Power Dissipation <sup>Note2</sup>	P <sub>T1</sub>	2	W
Total Power Dissipation <sup>Note3</sup>	P <sub>T2</sub>	2	W
Channel Temperature	T <sub>ch</sub>	150	°C
Storage Temperature	T <sub>stg</sub>	-55 to +150	°C
Single Avalanche Current <sup>Note4</sup>	I <sub>AS</sub>	-13	A
Single Avalanche Energy <sup>Note4</sup>	E <sub>AS</sub>	16.9	mJ

#### EQUIVALENT CIRCUIT



**Notes 1.** PW ≤ 10 μs, Duty Cycle ≤ 1%

2. Mounted on ceramic substrate of 1200 mm<sup>2</sup> x 2.2 mm
3. Mounted on glass epoxy board of 25.4 mm x 25.4 mm x 0.8 mm, PW = 10 sec
4. Starting T<sub>ch</sub> = 25°C, V<sub>DD</sub> = -15 V, R<sub>G</sub> = 25 Ω, L = 100 μH, V<sub>GS</sub> = -20 → 0 V

**Remark** The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

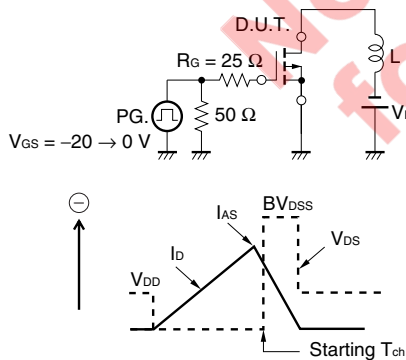
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**ELECTRICAL CHARACTERISTICS (TA = 25°C, All terminals are connected.)**

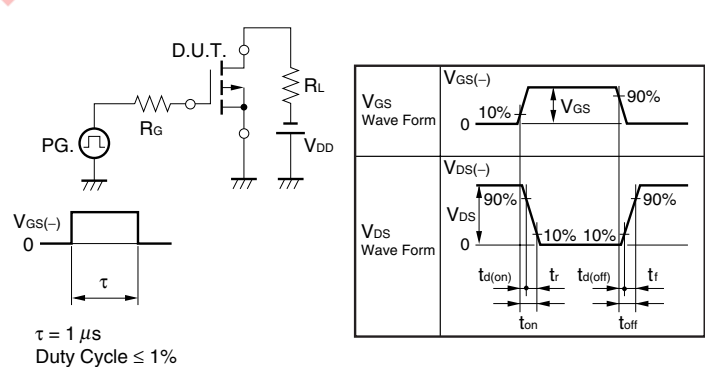
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I <sub>bss</sub>	V <sub>DS</sub> = -30 V, V <sub>GS</sub> = 0 V			-1	μA
Gate Leakage Current	I <sub>gss</sub>	V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0 V			±10	μA
Gate to Source Cut-off Voltage	V <sub>GS(off)</sub>	V <sub>DS</sub> = -10 V, I <sub>D</sub> = -1 mA	-1.0		-2.5	V
Forward Transfer Admittance <b>Note</b>	y <sub>fs</sub>	V <sub>DS</sub> = -10 V, I <sub>D</sub> = -6.5 A	9			S
Drain to Source On-state Resistance <b>Note</b>	R <sub>DS(on)1</sub>	V <sub>GS</sub> = -10 V, I <sub>D</sub> = -6.5 A		7.2	9.0	mΩ
	R <sub>DS(on)2</sub>	V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -6.5 A		9.9	14.5	mΩ
	R <sub>DS(on)3</sub>	V <sub>GS</sub> = -4.0 V, I <sub>D</sub> = -6.5 A		11.8	18.2	mΩ
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = -10 V		2810		pF
Output Capacitance	C <sub>oss</sub>	V <sub>GS</sub> = 0 V		710		pF
Reverse Transfer Capacitance	C <sub>rss</sub>	f = 1 MHz		460		pF
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = -15 V, I <sub>D</sub> = -6.5 A		13		ns
Rise Time	t <sub>r</sub>	V <sub>GS</sub> = -10 V		18		ns
Turn-off Delay Time	t <sub>d(off)</sub>	R <sub>G</sub> = 10 Ω		510		ns
Fall Time	t <sub>f</sub>			310		ns
Total Gate Charge	Q <sub>G</sub>	V <sub>DD</sub> = -24 V		67		nC
Gate to Source Charge	Q <sub>GS</sub>	V <sub>GS</sub> = -10 V		6.5		nC
Gate to Drain Charge	Q <sub>GD</sub>	I <sub>D</sub> = -13 A		19		nC
Body Diode Forward Voltage <b>Note</b>	V <sub>F(S-D)</sub>	I <sub>F</sub> = 13 A, V <sub>GS</sub> = 0 V		0.84		V
Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 13 A, V <sub>GS</sub> = 0 V		180		ns
Reverse Recovery Charge	Q <sub>rr</sub>	di/dt = 50 A/μs		14		nC

**Note** Pulsed

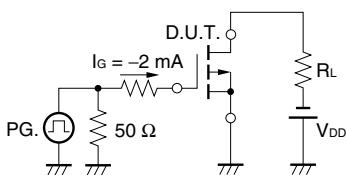
**TEST CIRCUIT 1 AVALANCHE CAPABILITY**



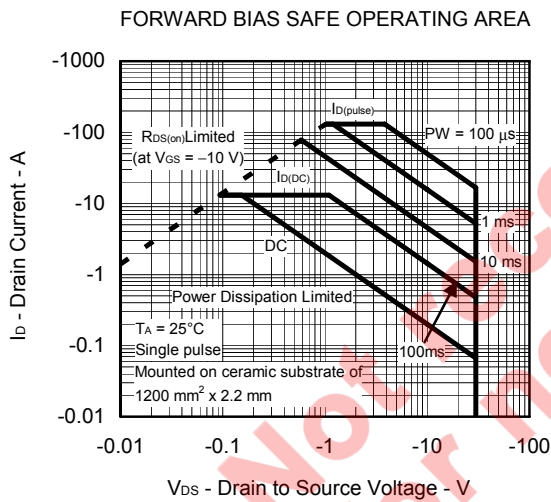
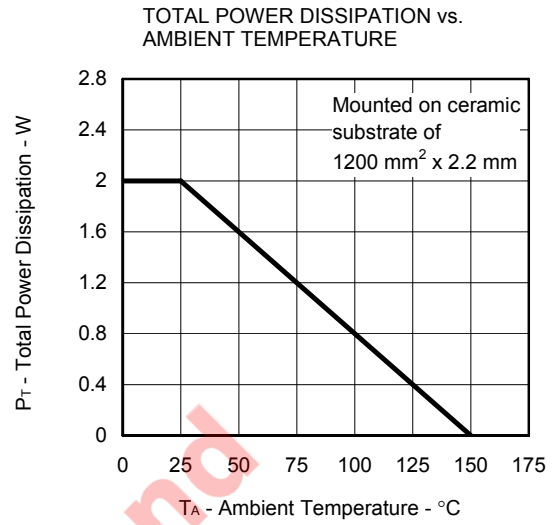
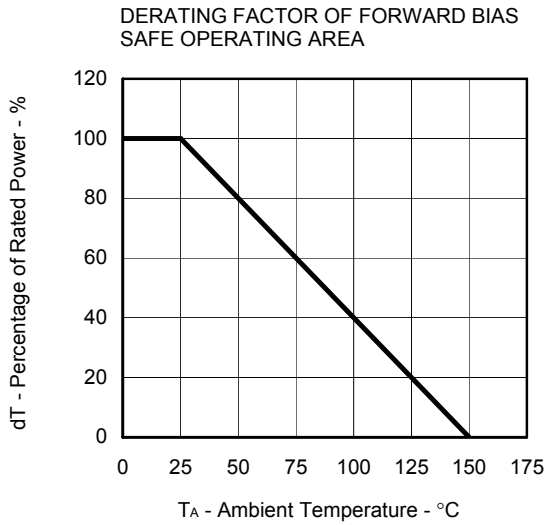
**TEST CIRCUIT 2 SWITCHING TIME**



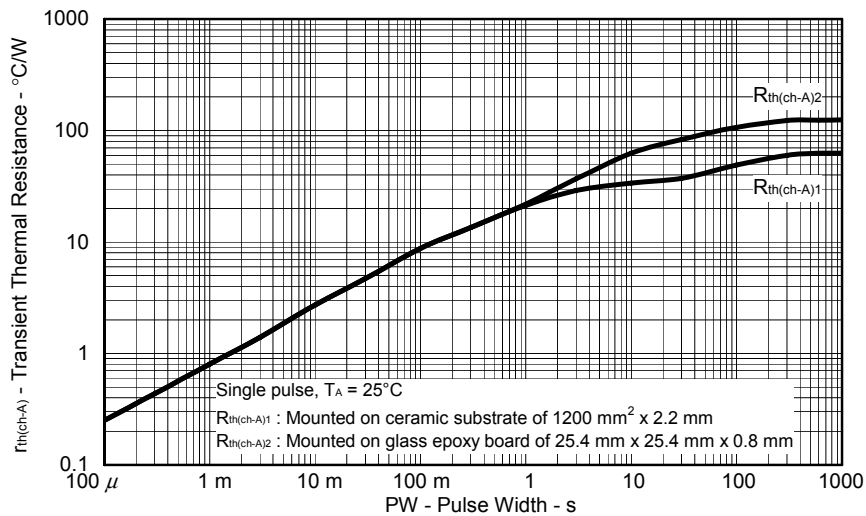
**TEST CIRCUIT 3 GATE CHARGE**



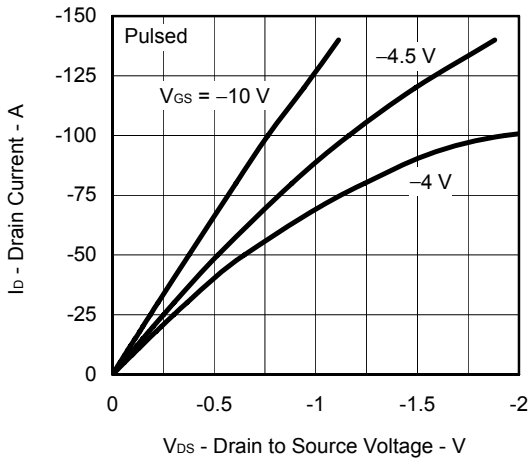
ELECTRICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ )



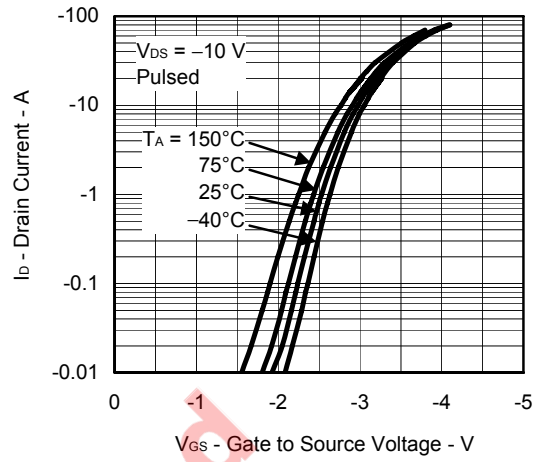
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



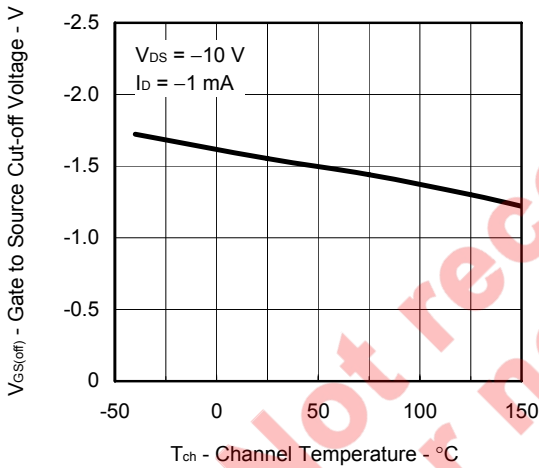
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



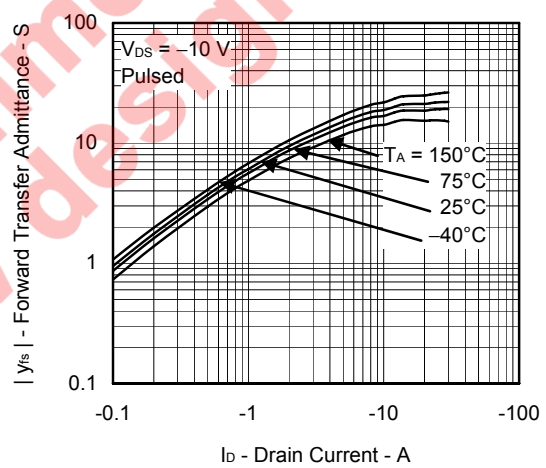
FORWARD TRANSFER CHARACTERISTICS



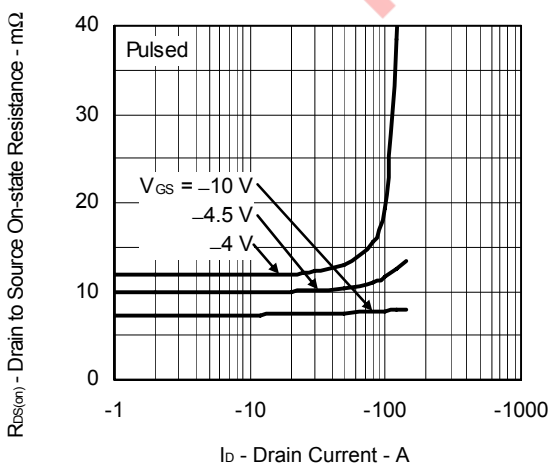
GATE TO SOURCE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



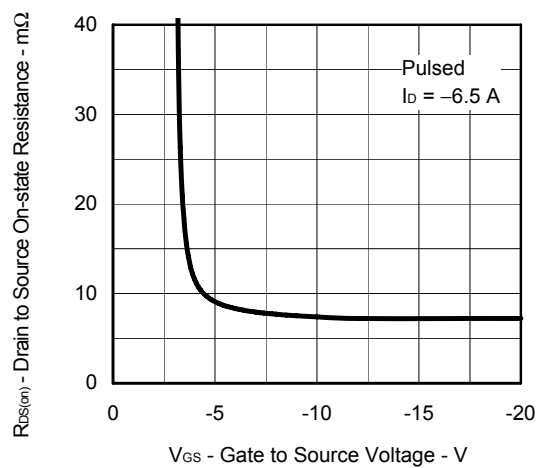
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



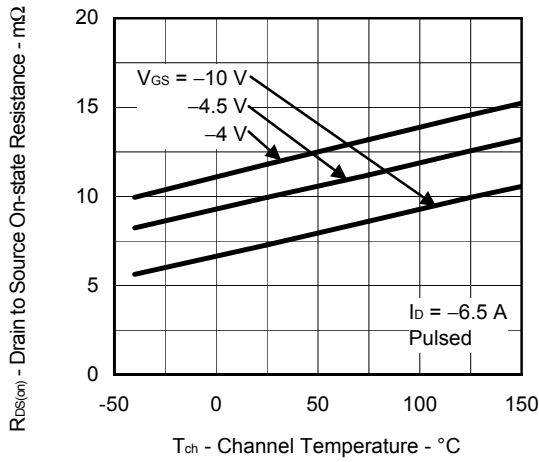
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



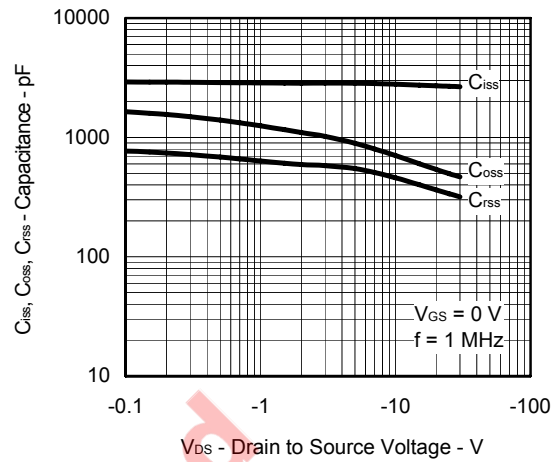
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



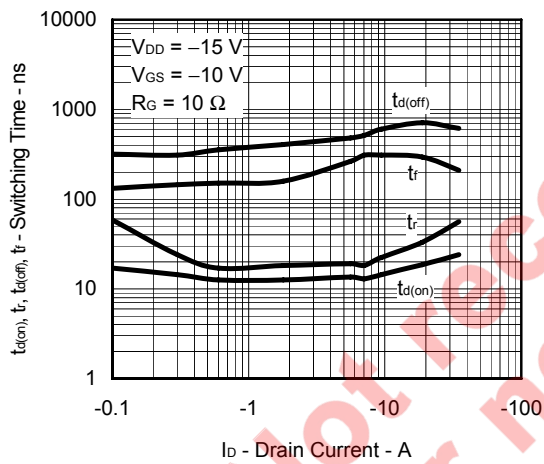
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



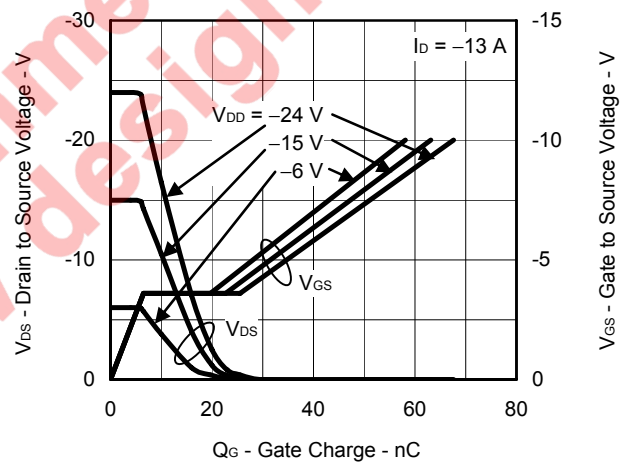
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



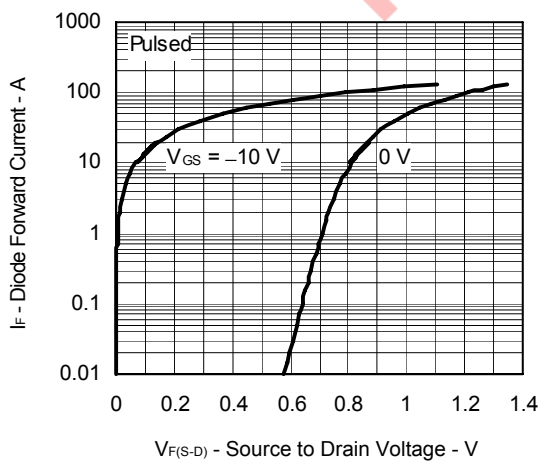
SWITCHING CHARACTERISTICS



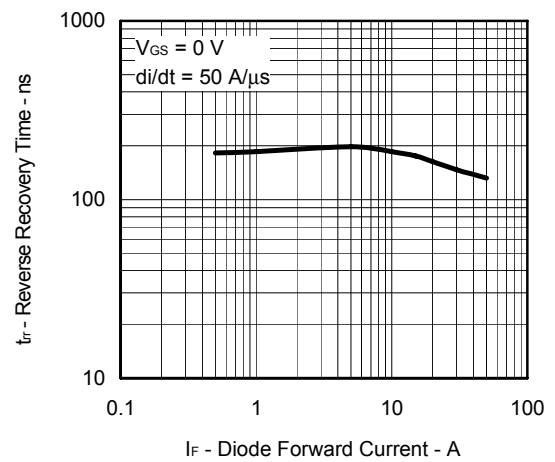
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



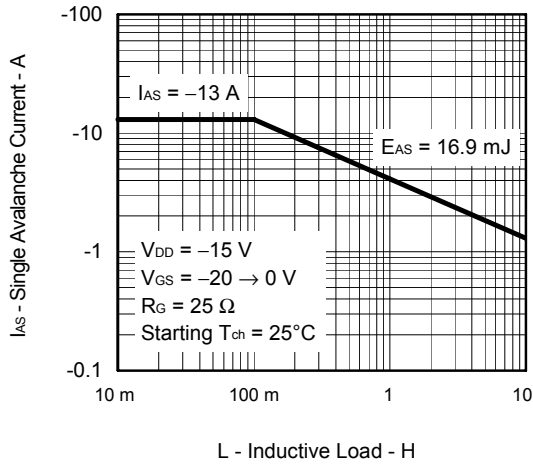
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



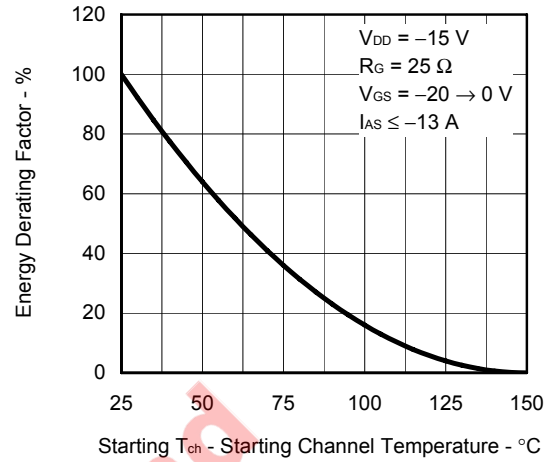
REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT



SINGLE AVALANCHE CURRENT vs. INDUCTIVE LOAD



SINGLE AVALANCHE ENERGY DERATING FACTOR



**ORDERING INFORMATION**

PART NUMBER	LEAD PLATING	PACKING	PACKAGE
μ PA2718AGR-E1-AT <sup>Note</sup>	Pure Sn (Tin)	Tape 2500 p/reel	Power SOP8
μ PA2718AGR-E2-AT <sup>Note</sup>			0.08 g TYP.

**Note** Pb-free (This product does not contain Pb in external electrode and other parts.)

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