μPA2737GR

P-channel MOSFET
–30 V, –11 A, 13 mΩ

R07DS1317EJ0100
Rev.1.00
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Description

The μPA2737GR is P-channel MOS Field Effect Transistor designed for DC/DC converter and power management applications of portable equipment.

Features

- V_{DSS} = –30 V (T_A = 25°C)
- Low on-state resistance
  — $R_{DS(on)}$ = 13 mΩ MAX. (V_{GS} = –10 V, I_D = –11 A)
- 4.5 V Gate-drive available
- Small and surface mount package (SOP-8)
- Pb-free and Halogen free

SOP-8

Ordering Information

Part No.	LEAD PLATING	PACKING	Package
μPA2737GR-E1-AX	Ni / Pd / Au	Tape 2500 p/reel	SOP-8 0.085 g TYP.
μPA2737GR-E2-AX			

Absolute Maximum Ratings (T_A = 25°C)

Item	Symbol	Ratings	Unit
Drain to Source Voltage (V_{GS} = 0 V)	V_{DSS}	–30	V
Gate to Source Voltage (V_{DS} = 0 V)	V_{GSS}	∓20	V
Drain Current (DC)	$I_{D(DC)}$	∓11	A
Drain Current (pulse) *1	$I_{D(pulse)}$	∓110	A
Total Power Dissipation *2	P_{T1}	1.1	W
Total Power Dissipation (PW = 10 sec) *2	P_{T2}	2.5	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	–55 to +150	°C
Single Avalanche Current *3	I_{AS}	11	A
Single Avalanche Energy *3	E_{AS}	12.1	mJ

Thermal Resistance

Channel to Ambient Thermal Resistance *2	$R_{th(ch-A)}$	114	°C/W

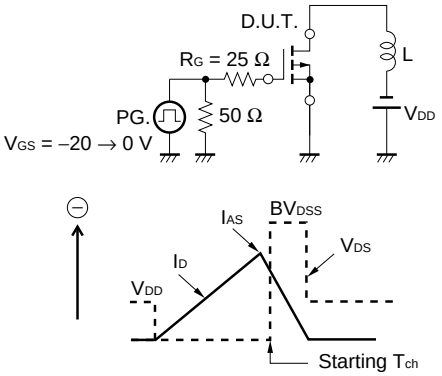
Notes: *1. PW ≤ 10 μs, Duty Cycle ≤ 1%
*2. Mounted on a glass epoxy board of 25.4 mm x 25.4 mm x 0.8 mmt
*3. Starting T_{ch} = 25°C, V_{DD} = –15 V, R_G = 25 Ω, V_{GS} = –20 → 0 V, L = 100 μH

Electrical Characteristics (T_A = 25°C)

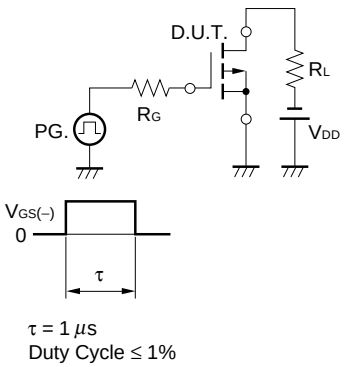
Item	Symbol	MIN.	TYP.	MAX.	Unit	Test Conditions
Zero Gate Voltage Drain Current	I_{DSS}			−1	μA	V_{DS} = −30 V, V_{GS} = 0 V
Gate Leakage Current	I_{GSS}			∓100	nA	V_{GS} = ∓20 V, V_{DS} = 0 V
Gate Cut-off Voltage	$V_{GS(off)}$	−1.0		−2.5	V	V_{DS} = −10 V, I_D = −1 mA
Forward Transfer Admittance *1	$\|y_{fs}\|$	4.5			S	V_{DS} = −10 V, I_D = −5.5 A
Drain to Source On-state Resistance *1	$R_{DS(on)1}$		9.7	13	mΩ	V_{GS} = −10 V, I_D = −11 A
	$R_{DS(on)2}$		17	25	mΩ	V_{GS} = −4.5 V, I_D = −11 A
Input Capacitance	C_{iss}		1750		pF	V_{DS} = −10 V,
Output Capacitance	C_{oss}		850		pF	V_{GS} = 0 V,
Reverse Transfer Capacitance	C_{rss}		770		pF	f = 1 MHz
Turn-on Delay Time	$t_{d(on)}$		20		ns	V_{DD} = −15 V, I_D = −5.5 A,
Rise Time	t_r		32		ns	V_{GS} = −10 V,
Turn-off Delay Time	$t_{d(off)}$		70		ns	R_G = 10 Ω
Fall Time	t_f		55		ns	
Total Gate Charge	Q_G		45		nC	V_{DD} = −24 V,
Gate to Source Charge	Q_{GS}		2.5		nC	V_{GS} = −10 V,
Gate to Drain Charge	Q_{GD}		23		nC	I_D = −11 A
Body Diode Forward Voltage *1	$V_{F(S-D)}$		0.85		V	I_F = 11 A, V_{GS} = 0 V
Reverse Recovery Time	t_{rr}		49		ns	I_F = 11 A, V_{GS} = 0 V,
Reverse Recovery Charge	Q_{rr}		48		nC	di/dt = 100 A/μs

Note: *1. Pulsed

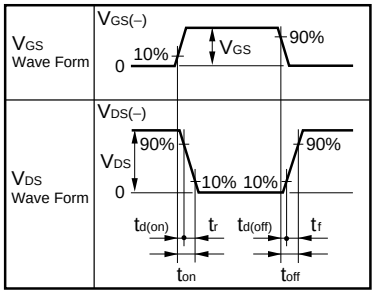
TEST CIRCUIT 1 AVALANCHE CAPABILITY



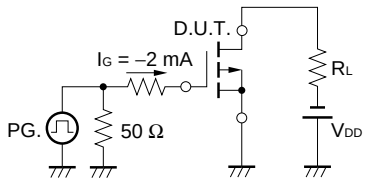
TEST CIRCUIT 2 SWITCHING TIME



τ = 1 μs
Duty Cycle ≤ 1%

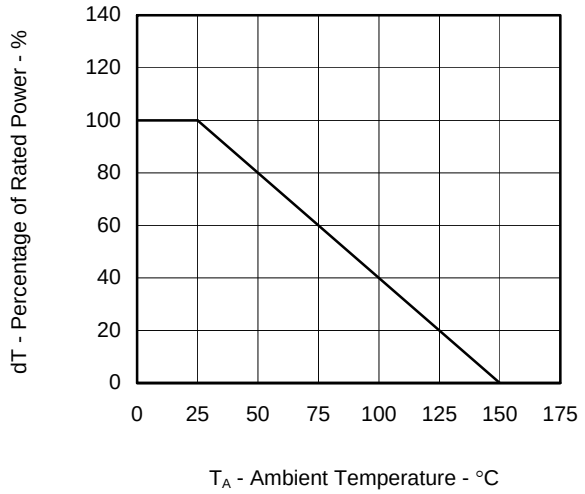


TEST CIRCUIT 3 GATE CHARGE

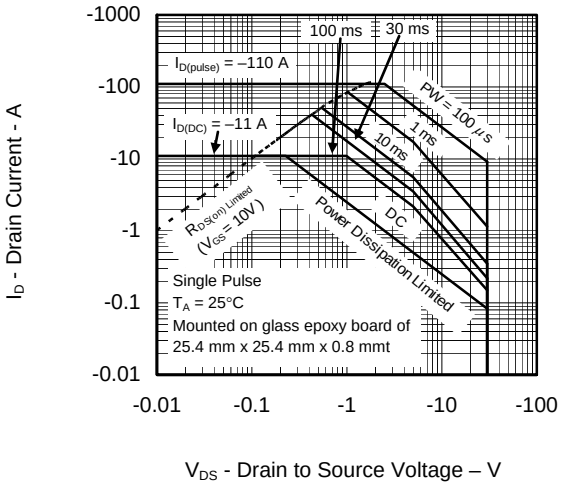


TYPICAL CHARACTERISTICS (T_A = 25°C)

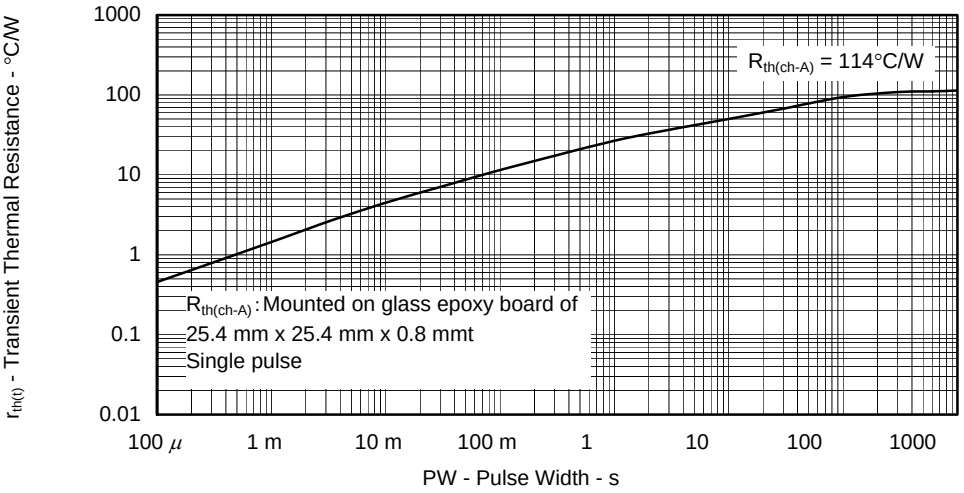
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



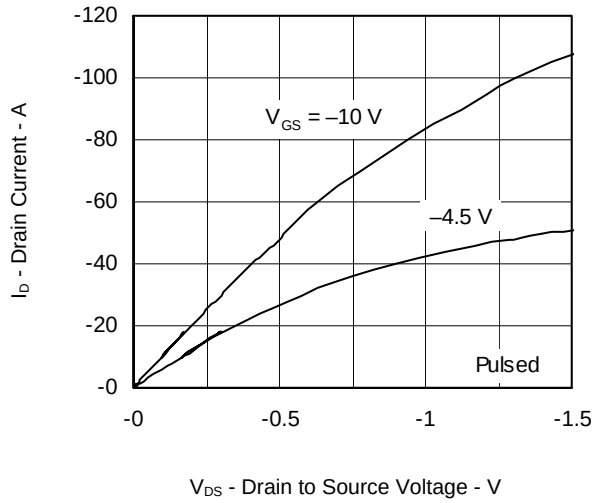
FORWARD BIAS SAFE OPERATING AREA



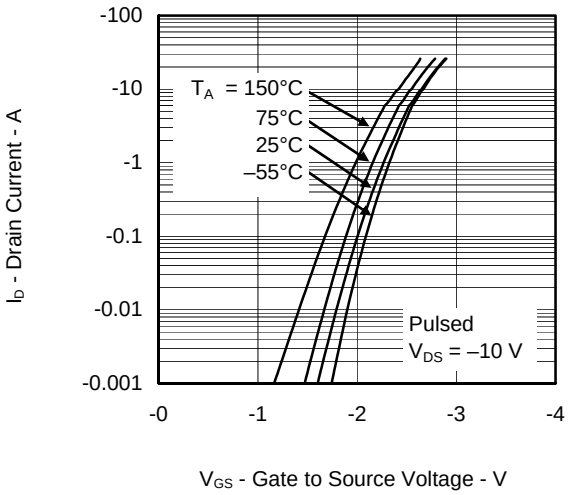
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



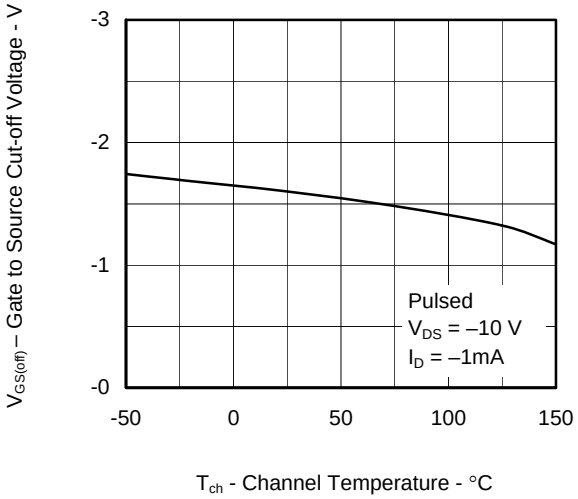
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



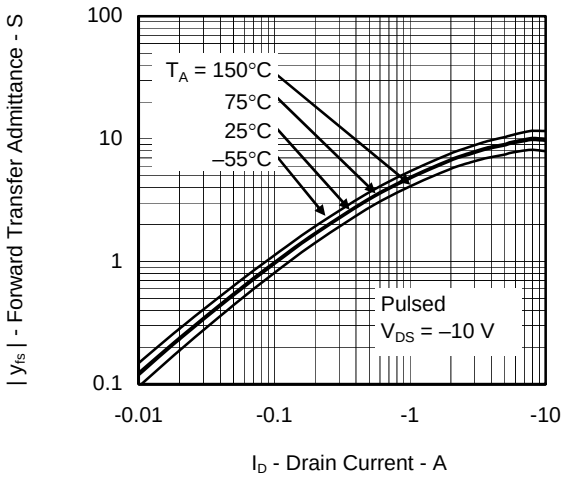
FORWARD TRANSFER CHARACTERISTICS



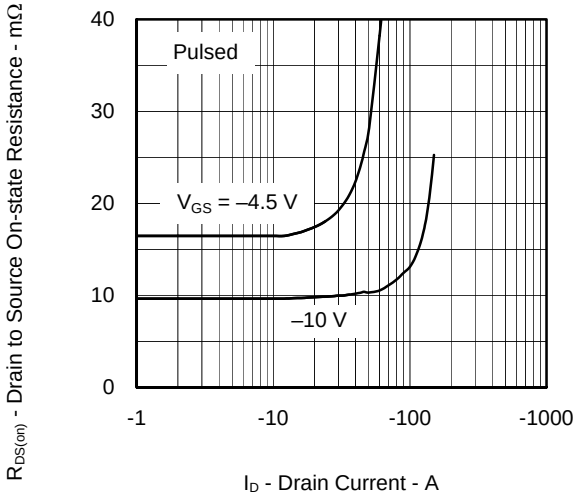
GATE TO SOURCE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



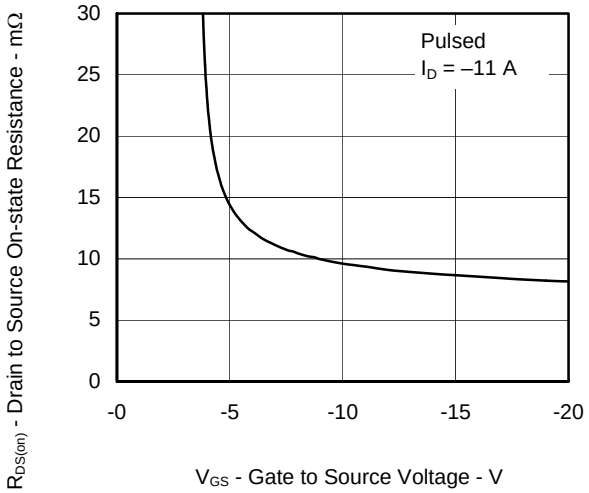
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



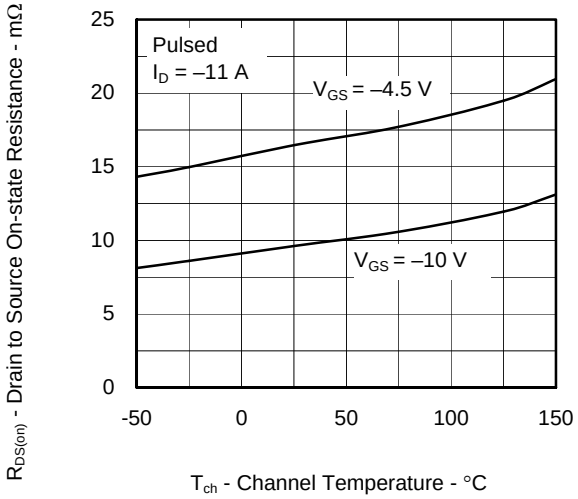
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



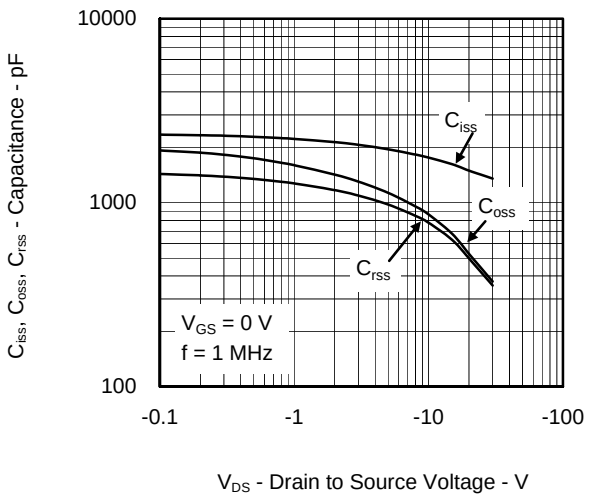
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



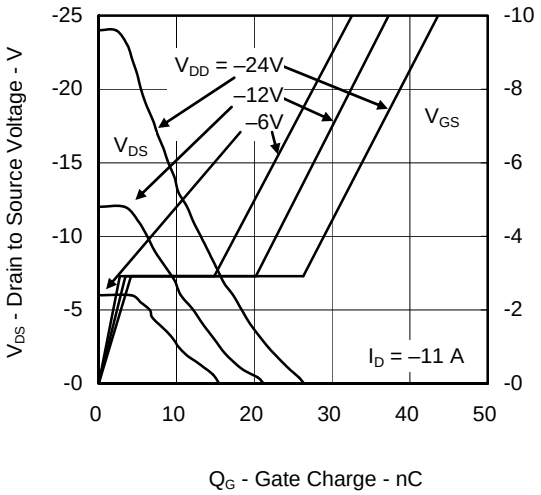
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



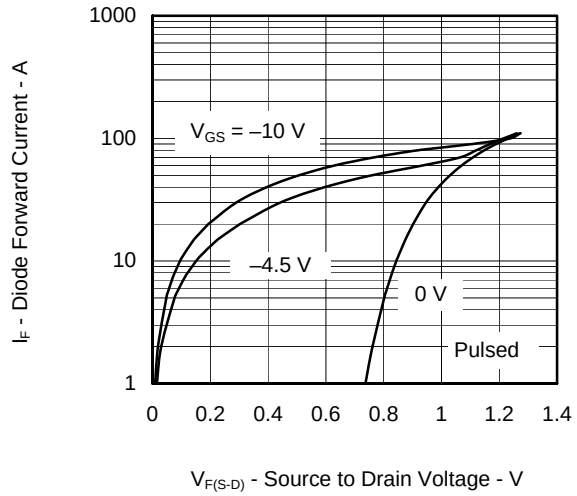
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



DYNAMIC INPUT/OUTPUT CHARACTERISTICS



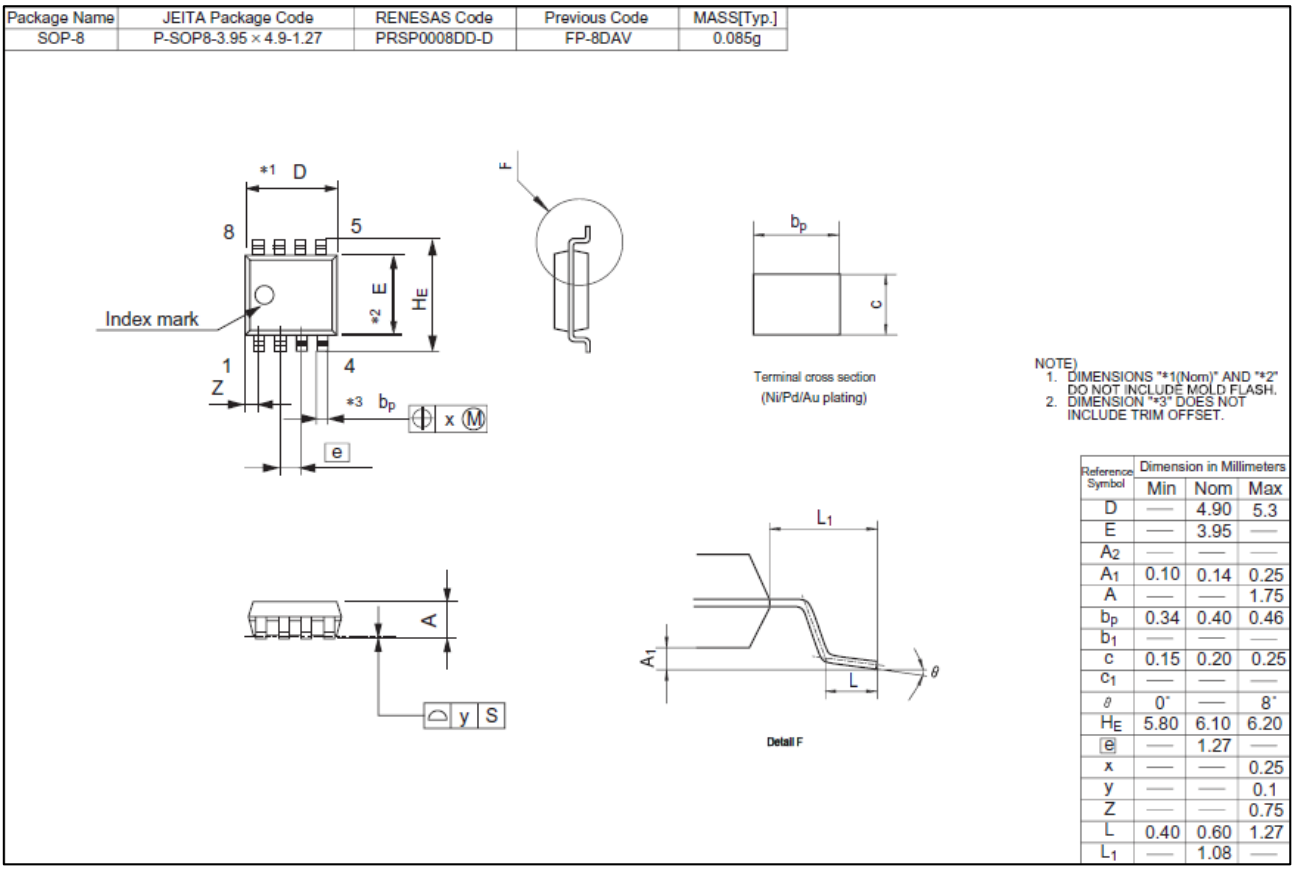
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



Package Drawings (Unit: mm)

SOP-8

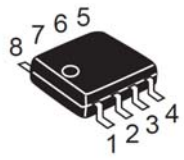
Package Name	JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
SOP-8	P-SOP8-3.95 × 4.9-1.27	PRSP0008DD-D	FP-8DAV	0.085g

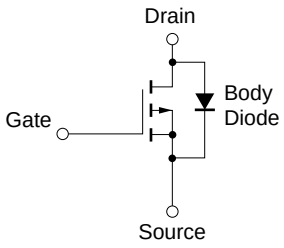


NOTE)
1. DIMENSIONS "*1(Nom)" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	4.90	5.3
E	—	3.95	—
A_2	—	—	—
A_1	0.10	0.14	0.25
A	—	—	1.75
b_p	0.34	0.40	0.46
b_1	—	—	—
c	0.15	0.20	0.25
c_1	—	—	—
θ	0°	—	8°
H_E	5.80	6.10	6.20
e	—	1.27	—
x	—	—	0.25
y	—	—	0.1
Z	—	—	0.75
L	0.40	0.60	1.27
L_1	—	1.08	—

Equivalent Circuit





1, 2, 3	Source
4	Gate
5, 6, 7, 8	Darin

Remark Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

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