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April 1st, 2010 Renesas Electronics Corporation

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MOS FIELD EFFECT TRANSISTOR μ PA2746UT1A

SWITCHING N-CHANNEL POWER MOSFET

DESCRIPTION

The μ PA2746UT1A is N-channel MOS Field Effect Transistor designed for DC/DC converter applications.

FEATURES

- Low on-state resistance
- RDS(on)1 = 3.0 m Ω MAX. (VGS = 10 V, ID = 45 A)
- RDS(on)2 = $4.5 \text{ m}\Omega$ MAX. (VGS = 4.5 V, ID = 23 A)
- Low QG
- Thin type surface mount package with heat spreader (8-pin HVSON)
- RoHS Compliant
- Halogen Free

ABSOLUTE MAXIMUM RATINGS (TA = 25°C, All terminals are connected.)

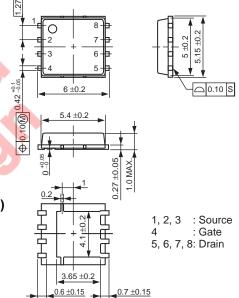
Drain to Source Voltage (V _{GS} = 0 V)	VDSS	30	V
Gate to Source Voltage (V _{DS} = 0 V)	Vgss	±20	V
Drain Current (DC) (Tc = 25°C)	ID(DC)	±45	Α
Drain Current (pulse) Note1	ID(pulse)	±190	Α
Total Power Dissipation Note2	PT1	1.5	W
Total Power Dissipation (PW = 10 sec) Note2	Рт2	4.6	W
Total Power Dissipation (Tc = 25°C)	Рт3	83	W
Channel Temperature	Tch	150	°C
Storage Temperature	Tstg	-55 to +150	°C
Single Avalanche Current Note3	las	40	Α
Single Avalanche Energy Note3	Eas	160	mJ

THERMAL RESISTANCE

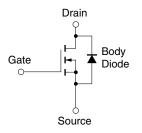
Channel to Ambient Thermal Resistance Note2	Rth(ch-A)	83.3	°C/W
Channel to Case (Drain) Thermal Resistance	Rth(ch-C)	1.5	°C/W

- **Notes 1.** PW \leq 10 μ s, Duty Cycle \leq 1%
 - 2. Mounted on a glass epoxy board of 25.4 mm x 25.4 mm x 0.8 mmt
 - 3. Starting T_{ch} = 25°C, V_{DD} = 15 V, R_G = 25 Ω , V_{GS} = 20 \rightarrow 0 V, L = 100 μ H

PACKAGE DRAWING (Unit: mm)



EQUIVALENT CIRCUIT



Remark Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

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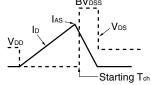
ELECTRICAL CHARACTERISTICS (TA = 25°C, All terminals are connected.)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	IDSS	V _{DS} = 30 V, V _{GS} = 0 V			10	μΑ
Gate Leakage Current	Igss	V _{GS} = ±16 V, V _{DS} = 0 V			±100	nA
Gate to Source Cut-off Voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1 mA	1.5		2.5	V
Forward Transfer Admittance Note	yfs	V _{DS} = 10 V, I _D = 23 A	19			S
Drain to Source On-state Resistance Note	RDS(on)1	V _{GS} = 10 V, I _D = 45 A		2.4	3.0	mΩ
	RDS(on)2	V _{GS} = 4.5 V, I _D = 23 A		3.6	4.5	mΩ
Input Capacitance	Ciss	V _{DS} = 15 V,		3190	4150	pF
Output Capacitance	Coss	V _{GS} = 0 V,		540	700	pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		245	370	pF
Turn-on Delay Time	t _{d(on)}	V _{DD} = 15 V, I _D = 23 A,		26		ns
Rise Time	tr	V _{GS} = 10 V,		14		ns
Turn-off Delay Time	t _{d(off)}	R _G = 10 Ω		85		ns
Fall Time	tf			15		ns
Total Gate Charge QG		V _{GS} = 10 V		52	78	nC
	QG	V _{GS} = 5 V		27	41	nC
Gate to Source Charge	Qgs	V _{DD} = 15 V		11		nC
Gate to Drain Charge	Q _{GD}	I _D = 45 A		9.4		nC
Body Diode Forward Voltage Note	V _{F(S-D)}	I _F = 45 A, V _{GS} = 0 V		0.83		V
Reverse Recovery Time	trr	I _F = 45 A, V _{GS} = 0 V,		37		ns
Reverse Recovery Charge	Qrr	di/dt = 100 A/μs		35		nC
Gate Resistance	Rg	f = 1 MHz		1.9	2.9	Ω

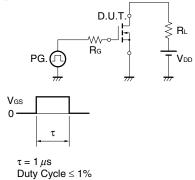
Note Pulsed

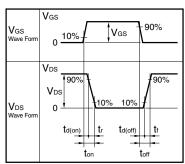
TEST CIRCUIT 1 AVALANCHE CAPABILITY

$\begin{array}{c|c} & D.U.T. \\ \hline R_G = 25 \ \Omega \\ \hline V_{GS} = 20 \rightarrow 0 \ V \end{array} \begin{array}{c} D.U.T. \\ \hline \geqslant 50 \ \Omega \\ \hline \end{array} \begin{array}{c} V_{DD} \\ \hline \end{array}$



TEST CIRCUIT 2 SWITCHING TIME





TEST CIRCUIT 3 GATE CHARGE

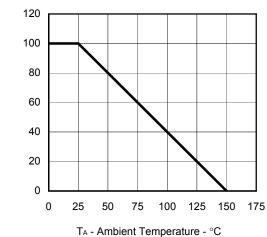


- Percentage of Rated Power - %

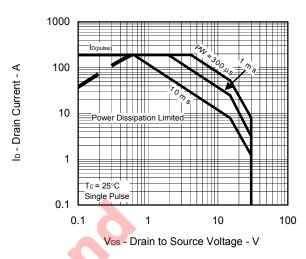
b - Drain Current - A

TYPICAL CHARACTERISTICS (TA = 25°C)

DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



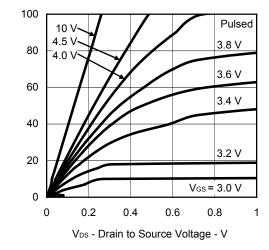
FORWARD BIAS SAFE OPERATING AREA



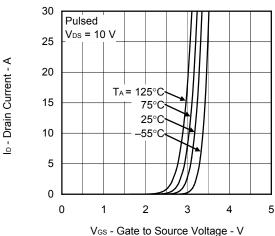
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



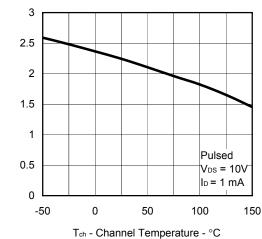
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



FORWARD TRANSFER CHARACTERISTICS

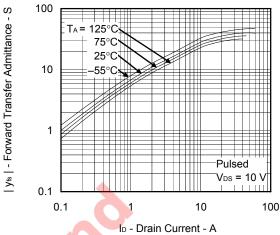


GATE TO SOURCE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



Ros(m) - Drain to Source On-state Resistance - m

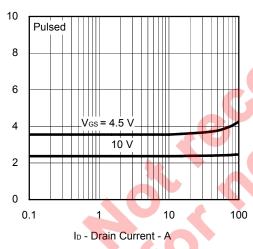
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



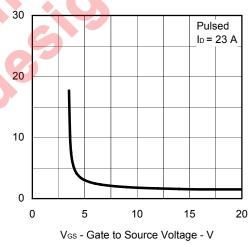


 $R_{DS(m)}$ - Drain to Source On-state Resistance - $m\Omega$

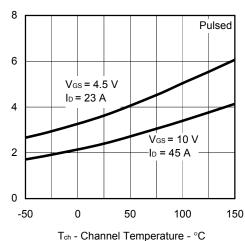
DRAIN TO SOURCE ON-STATE RESISTANCE vs. **DRAIN CURRENT**



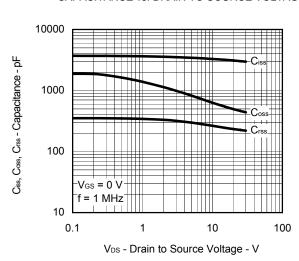
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE

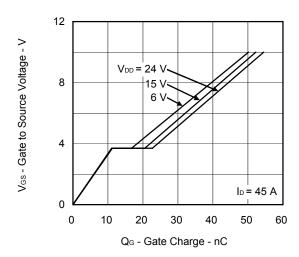


CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE

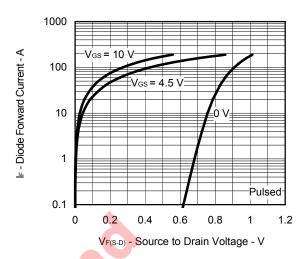


RDS(01) - Drain to Source On-state Resistance - m\Omega

DYNAMIC INPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE



ORDERING INFORMATION

PART NUMBER	LEAD PLATING	PACKING	PACKAGE
μPA2746UT1A-E1-AY Note	Dura Ca	Tono 2000 n/mod	8-pin HVSON (6051)
μPA2746UT1A-E2-AY Note	Pure Sn	Tape 3000 p/reel	0.10 g TYP.

Note Pb-free (This product does not contain Pb in the external electrode.)

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