To our customers,

Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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DATA SHEET

BIPOLAR ANALOG INTEGRATED CIRCUIT

μPC2756TB

MIXER+OSCILLATOR SILICON MMIC FOR FREQUENCY DOWNCONVERTER OF L BAND WIRELESS RECEIVER

DESCRIPTION

The μPC2756TB is a silicon monolithic integrated circuit designed as L band frequency downconverter for receiver stage of wireless systems. The IC consists of mixer and local oscillator. This IC operates at 3 V.

This IC is manufactured using NEC's 20GHz f_T NESAT™ III silicon bipolar process. This process uses silicon nitride passivation film and gold electrodes. These materials can protect chip surface from external pollution and prevent corrosion/migration. Thus, this IC has excellent performance, uniformity and reliability.

FEATURES

- Wideband operation : f_{RFin} = 0.1 to 2.0 GHz
- Supply voltage : V_{CC} = 2.7 to 3.3 V
- Low current consumption : I_{CC} = 6.0 mA TYP. @V_{CC} = 3.0 V
- Minimized carrier leakage : Due to double balanced mixer
- Equable output impedance : Single-end push-pull IF amplifier
- Equable temperature-drift oscillator : Differential amplifier type oscillator
- High-density surface mounting : 6-pin super minimold package (2.0 × 1.25 × 0.9 mm)

APPLICATIONS

- Data carrier up to 2.0 GHz MAX.
- Wireless LAN up to 2.0 GHz MAX.

ORDERING INFORMATION

Part Number	Package	Marking	Supplying Form
μPC2756TB-E3	6-pin super minimold	C1W	• Embossed tape 8 mm wide • 1, 2, 3 pins face the perforation side of the tape • Qty 3 kpcs/reel

Remark To order evaluation samples, please contact your local NEC sales office.
Part number for sample order: μPC2756TB

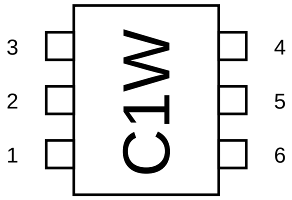
Caution Electro-static sensitive devices

Document No. P12807EJ3V0DS00 (3rd edition)
Date Published February 2001 N CP(K)
Printed in Japan

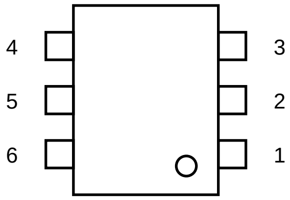
The mark ★ shows major revised points

PIN CONNECTIONS

(Top View)



(Bottom View)



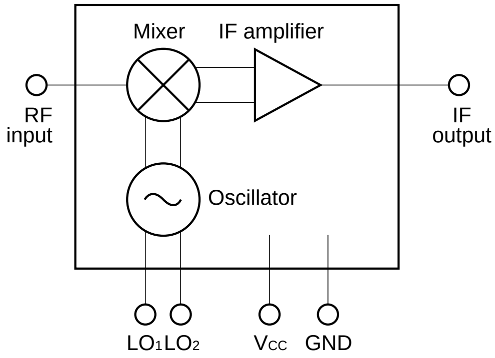
Pin No.	Pin Name
1	RFinput
2	GND
3	LO_1
4	LO_2
5	V_{CC}
6	IFoutput

PRODUCT LINE-UP (T_A = +25℃, V_{CC} = 3.0 V, $Z_S = Z_L$ = 50 Ω)

Parameter / Part Number	V_{CC} (V)	I_{CC} (mA)	0.9 GHz CG (dB)	1.6 GHz CG (dB)	0.9 GHz NF (dB)	1.6 GHz NF (dB)	f_{RFin} (GHz)	f_{IFout} (GHz)	f_{OSC} (GHz)	Package
μPC2756T	2.7 to 3.3	6.0	14	14	10	13	0.1 to 2.0	10 to 300	to 2.2	6-pin minimold
μPC2756TB										6-pin super minimold

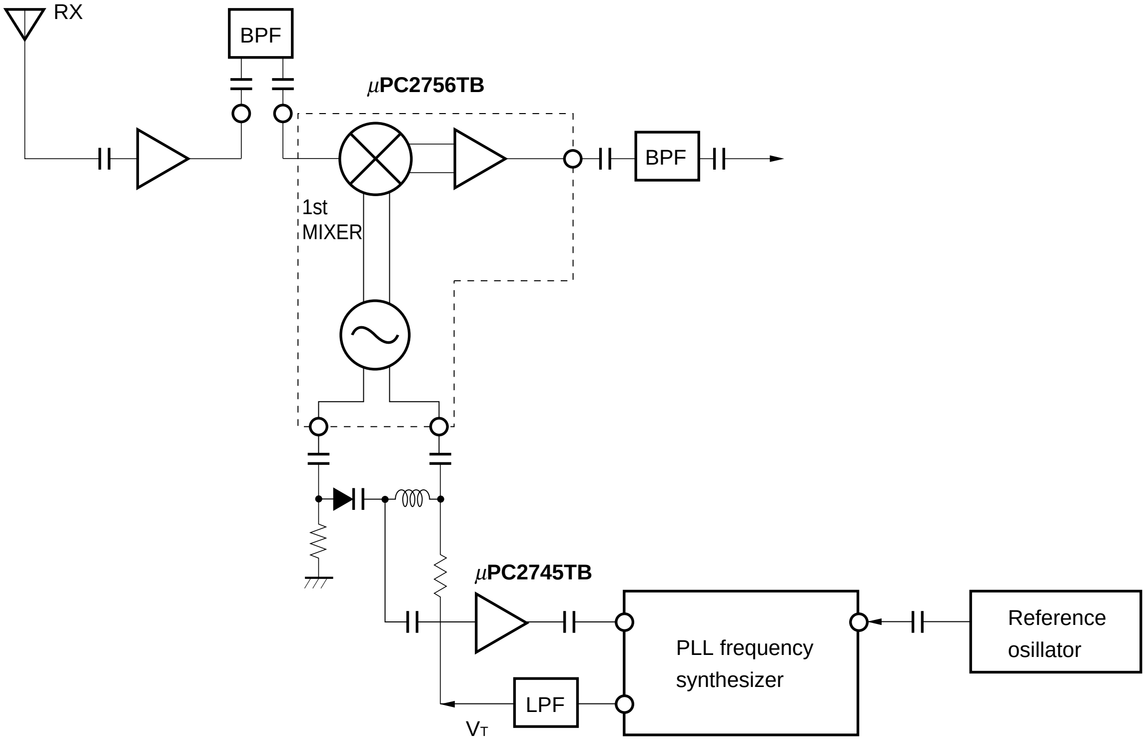
Remark Typical performance. Please refer to ELECTRICAL CHARACTERISTICS in detail.

INTERNAL BLOCK DIAGRAM



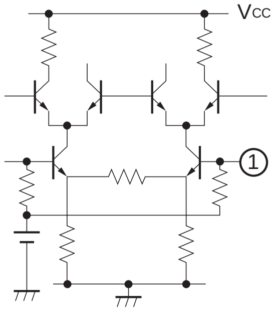
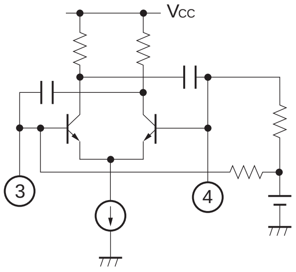
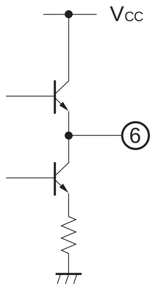
Remark Oscillator tank circuit must be externally attached to LO_1 and LO_2 pins.

μPC2756TB LOCATION EXAMPLE IN THE SYSTEM



This document is to be specified for μPC2756TB. For the other part number mentioned in this document, please refer to the data sheet of each part number.

PIN EXPLANATION

Pin No.	Pin Name	Applied Voltage (V)	Pin Voltage (V)[Note]	Function and Application	Equivalent Circuit
1	RFinput	–	1.2	This pin is RF input for mixer designed as double balance type. This circuit contributes to suppress spurious signal with minimum LO and bias power consumption. Also this symmetrical circuit can keep specified performance insensitive to process-condition distribution. This pin must be externally coupled to front stage with capacitor for DC cut.	
2	GND	0	–	Must be connected to the system ground with minimum inductance. Ground pattern on the board should be formed as wide as possible. (Track length should be kept as short as possible.)	
3	LO$_1$	–	1.2	These pins are both base-collector of oscillator. This oscillator is designed as differential amplifier type. 3 pin and 4 pin should be externally equipped with tank resonator circuit in order to oscillate with feedback loop. Also this symmetrical circuit can keep specified performance insensitive to process-condition distribution. Each pin must be externally coupled to tank circuit with capacitor for DC cut.	
4	LO$_2$	–	1.2		
5	V$_{CC}$	2.7 to 3.3	–	Supply voltage 3.0 ± 0.3 V for operation. Must be connected bypass capacitor (e.g. 1 000 pF) to minimize ground impedance.	
6	IFoutput	–	1.7	This pin is output from IF buffer amplifier designed as single-ended push-pull type. This pin is assigned for emitter follower output with low-impedance. This pin must be externally coupled to next stage with capacitor for DC cut.	

Note Pin voltage is measured at V$_{CC}$ = 3.0 V

APPLICATION

This IC is guaranteed on the test circuit constructed with 50 Ω equipment and transmission line. This IC, however, does not have 50 Ω input/output impedance, but electrical characteristics such as conversion gain and intermodulation distortion are described herein on these conditions without impedance matching. So, you should understand that conversion gain and intermodulation distortion at input level will vary when you improve VS of RF input with external circuit (50 Ω termination or impedance matching).

External circuits of the IC are explained in a following application note.

- To RF and IF port : Application Note “**Usage and Application Characteristics of μPC2757T, μPC2758T and μPC8112T, 3-V Power Supply, 1.9-GHz Frequency Down Converter ICs for Cellular/Cordless Telephone and Portable Wireless Communication”(P11997E)**

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Rating	Unit
Supply Voltage	V_{CC}	T_A = +25 °C	5.5	V
★ Power Dissipation	P_D	Mounted on double-sided copper clad 50 × 50 × 1.6 mm epoxy glass PWB, T_A = +85°C	270	mW
Operating Ambient Temperature	T_A		–40 to +85	°C
Storage Temperature	T_{stg}		–55 to +150	°C

RECOMMENDED OPERATING RANGE

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply Voltage	V_{CC}	2.7	3.0	3.3	V

ELECTRICAL CHARACTERISTICS (T_A = +25°C, V_{CC} = 3.0 V, $Z_S = Z_L$ = 50 Ω, Test circuit)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Circuit Current	I_{CC}	No signals	3.5	6.0	8.0	mA
RF Input Frequency	f_{RFin}	CG ≥ (CG1 –3 dB), f_{IFout} = 150 MHz constant	0.1	–	2.0	GHz
IF Output Frequency	f_{IFout}	CG ≥ (CG1 –3 dB), f_{RFin} = 0.9 GHz constant	10	–	300	MHz
Conversion Gain 1	CG1	f_{RFin} = 0.9 GHz, f_{IFout} = 150 MHz, P_{RFin} = –40 dBm	11	14	17	dB
Conversion Gain 2	CG2	f_{RFin} = 1.6 GHz, f_{IFout} = 20 MHz, P_{RFin} = –40 dBm	11	14	17	dB
SSB Noise Figure 1	SSB•NF1	f_{RFin} = 0.9 GHz, f_{IFout} = 150 MHz, SSB mode	–	10	13	dB
SSB Noise Figure 2	SSB•NF2	f_{RFin} = 1.6 GHz, f_{IFout} = 20 MHz, SSB mode	–	13	16	dB
Saturated Output Power 1	$P_{O(sat)\,1}$	f_{RFin} = 0.9 GHz, f_{IFout} = 150 MHz, P_{RFin} = –10 dBm	–11	–8	–	dBm
Saturated Output Power 2	$P_{O(sat)\,2}$	f_{RFin} = 1.6 GHz, f_{IFout} = 20 MHz, P_{RFin} = –10 dBm	–15	–12	–	dBm

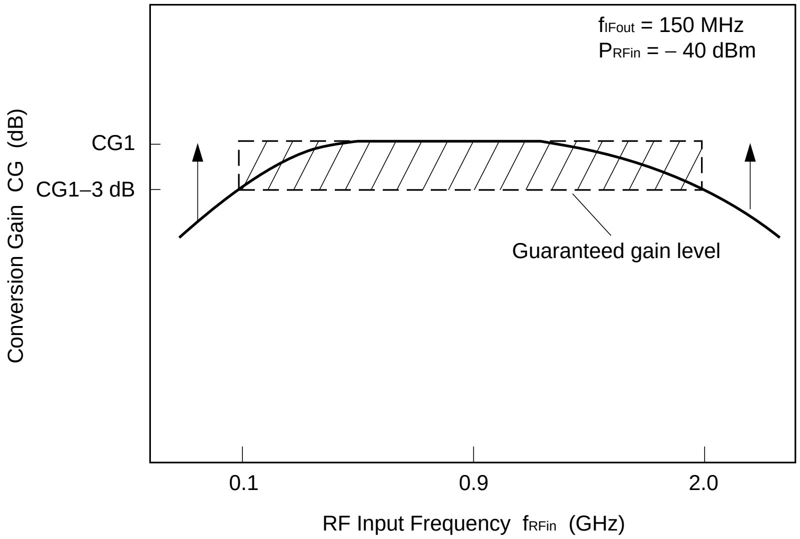
STANDARD CHARACTERISTICS FOR REFERENCE (Unless otherwise specified, T_A = +25°C, V_{CC} = 3.0 V, $Z_S = Z_L$ = 50 Ω)

Parameter	Symbol	Conditions	Reference	Unit
Output 3rd Order Intercept Point	OIP_3	f_{RFin} = 0.8 to 2.0 GHz, f_{IFout} = 0.1 GHz, Cross point IP.	+4.0	dBm
Phase Noise	PN	f_{OSC} = 1.9 GHz^{Note}	–68	dBc/Hz
LO Leakage at RFinput Pin	LO_{rf}	f_{LOin} = 0.8 to 2.0 GHz	–35	dB
LO Leakage at IFoutput Pin	LO_{if}	f_{LOin} = 0.8 to 2.0 GHz	–23	dB
Maximum Oscillating Frequency	$f_{OSCMAX.}$	V-Di: 1SV210, L: 7 nH^{Note}	2.2	GHz

Note On application circuit example.

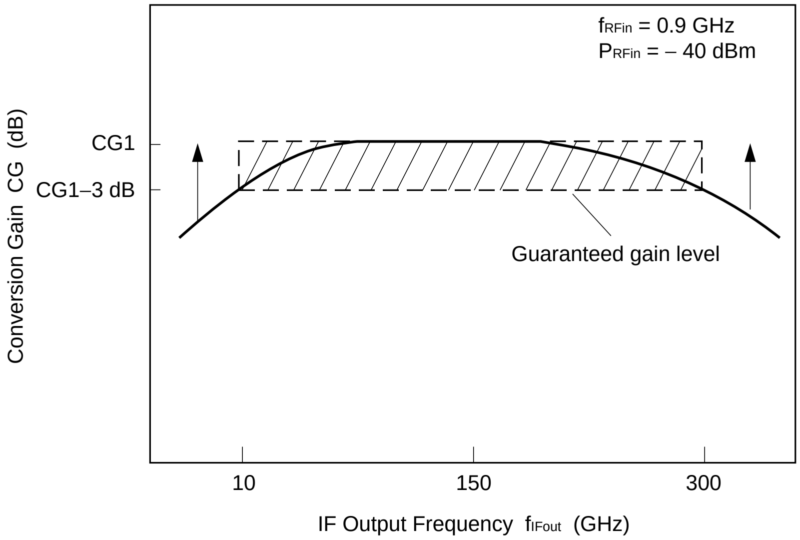
SCHEMATIC SUPPLEMENT FOR RF, IF SPECIFICATIONS

RF Frequency Response



	MIN.	TYP.	MAX.	Unit
CG1	11	14	17	dB
CG1-3 dB	8	11	14	dB

IF Frequency Response



TEST CIRCUIT

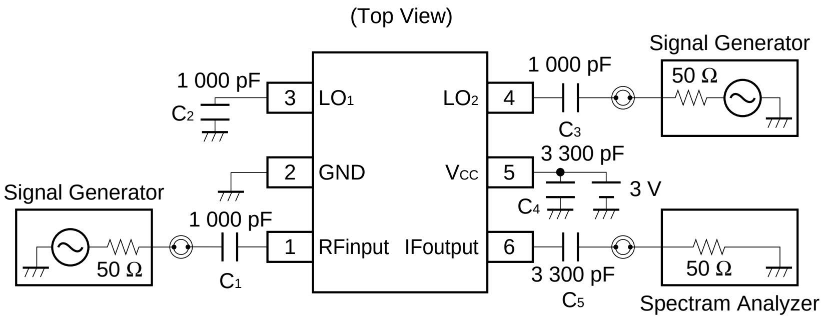
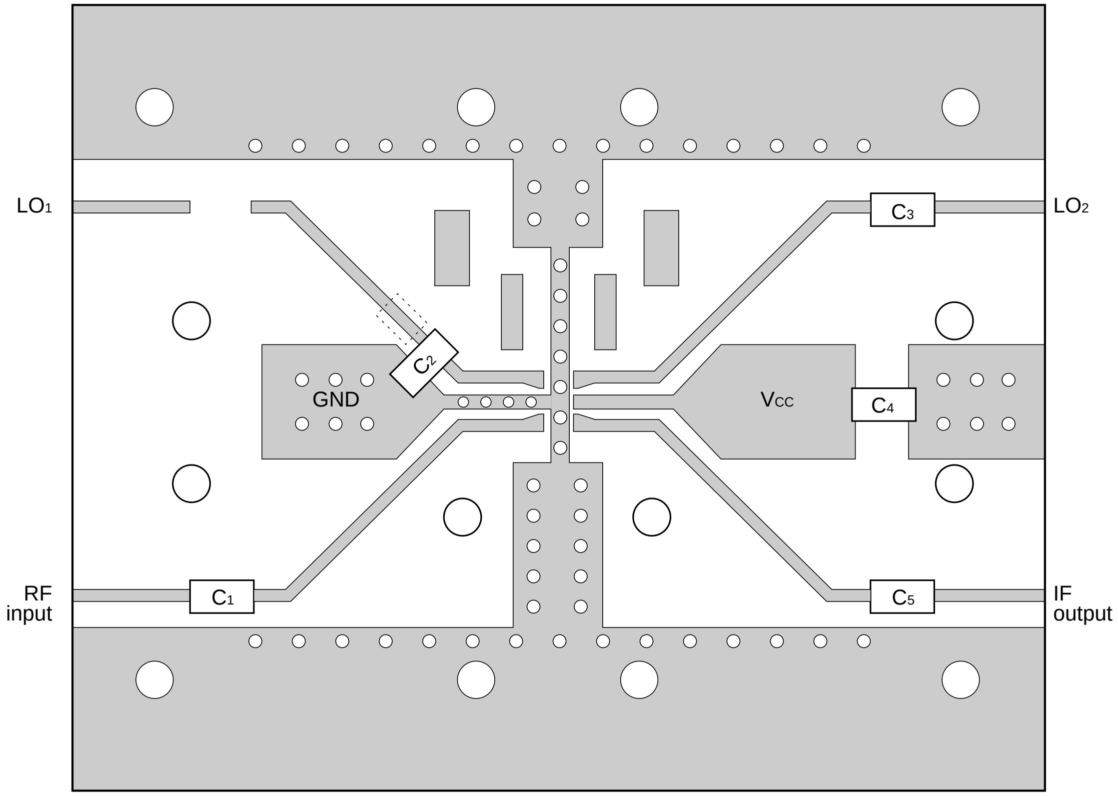


ILLUSTRATION OF THE TEST CIRCUIT ASSEMBLED ON EVALUATION BOARD



COMPONENT LIST

	Value
C_1 to C_3	1 000 pF
C_4, C_5	3 300 pF

Notes

(1) 35 × 42 × 0.4 mm double copper clad polyimide board.
(2) Back side: GND pattern
(3) Solder plated on pattern
(4) ○ ◯: Through holes
(5) ⬚ pattern should be removed on this testing.

APPLICATION CIRCUIT EXAMPLE

(Top View)

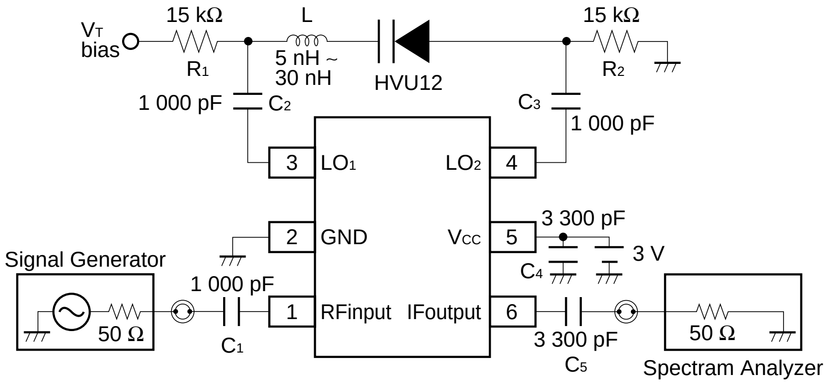
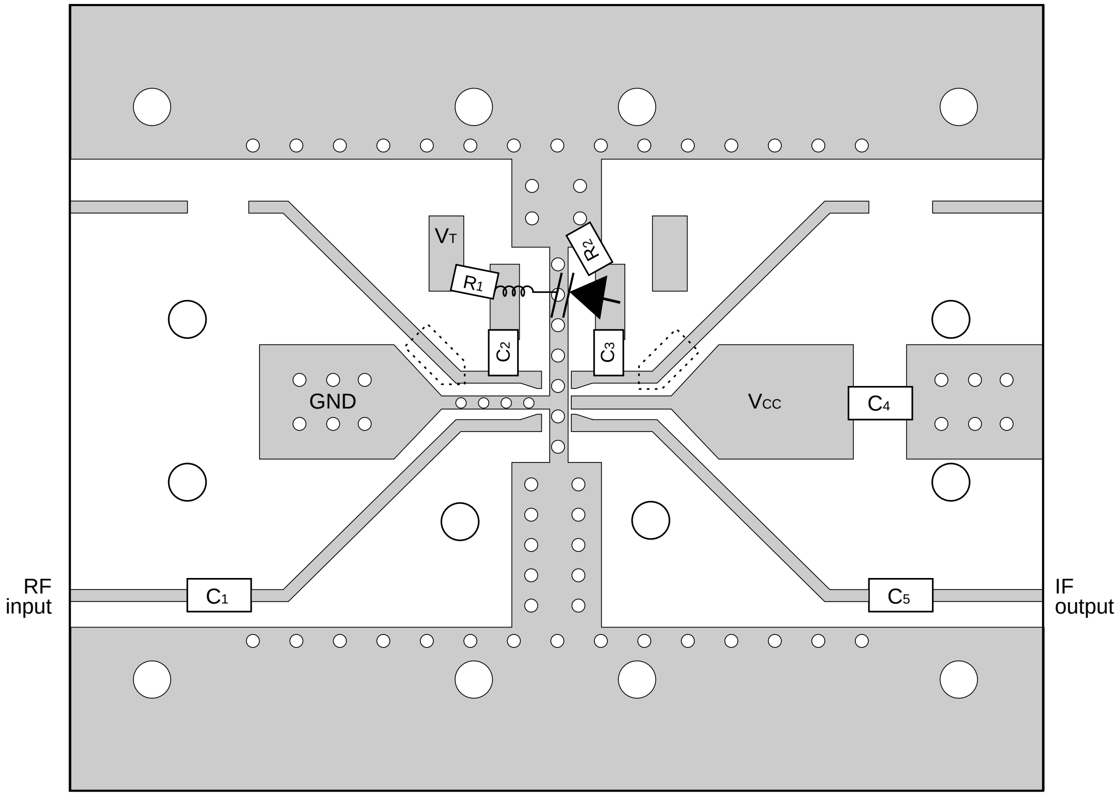


ILLUSTRATION OF THE APPLICATION CIRCUIT ASSEMBLED ON EVALUATION BOARD



COMPONENT LIST

	Value
C$_1$ to C$_3$	1 000 pF
C$_4$, C$_5$	3 300 pF
R$_1$, R$_2$	15 kΩ
L	5 nH to 30 nH
V-Di	HVU12

Notes

(1) 35 × 42 × 0.4 mm double copper clad polyimide board.

(2) Back side: GND pattern

(3) Solder plated on pattern

(4) ○ ◯: Through holes

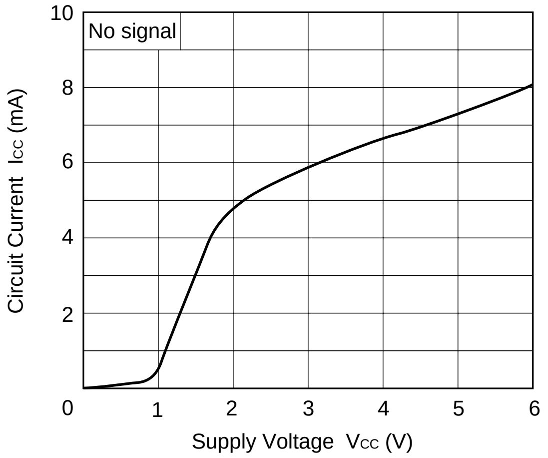
(5) ⬚ pattern should be removed on this testing.

The application circuits and their parameters are for reference only and are not intended for use in actual design-ins.

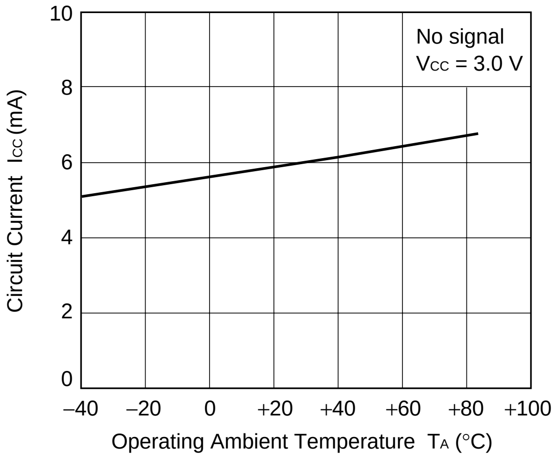
★ TYPICAL CHARACTERISTICS (Unless otherwise specified, T_A = +25°C)

– ON THE TEST CIRCUIT –

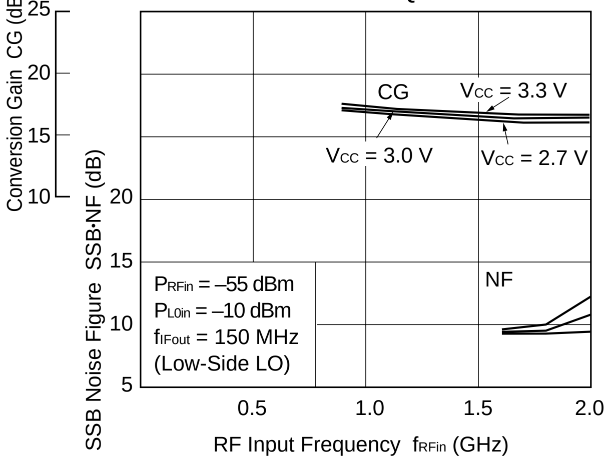
CIRCUIT CURRENT vs. SUPPLY VOLTAGE



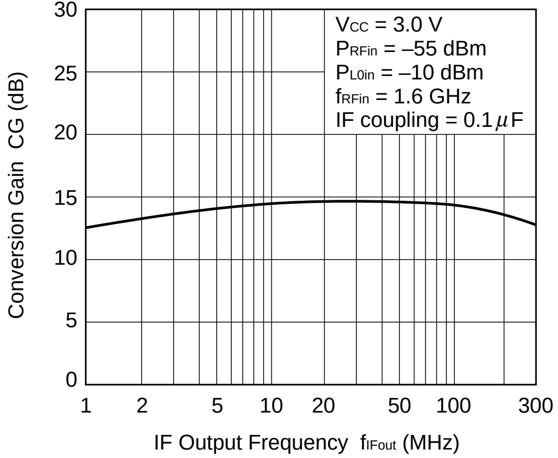
CIRCUIT CURRENT vs. OPERATING AMBIENT TEMPERATURE



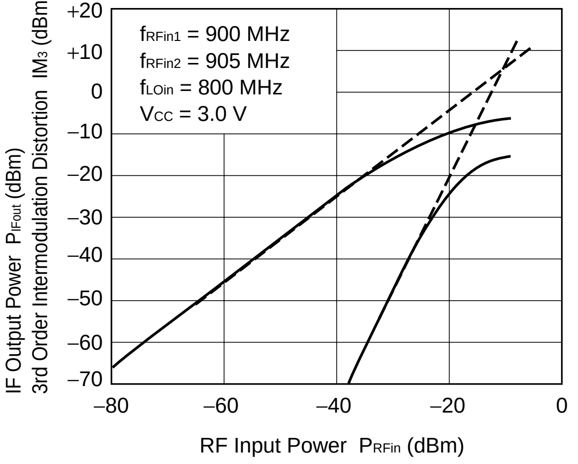
CONVERSION GAIN, SSB NOISE FIGURE vs. RF INPUT FREQUENCY



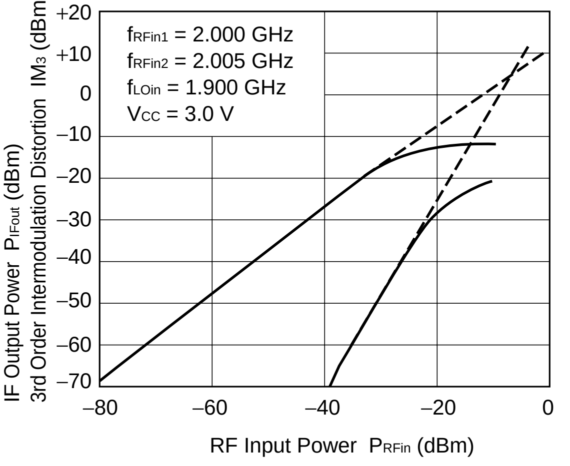
CONVERSION GAIN vs. IF OUTPUT FREQUENCY



IF OUTPUT POWER, IM3 vs. RF INPUT POWER

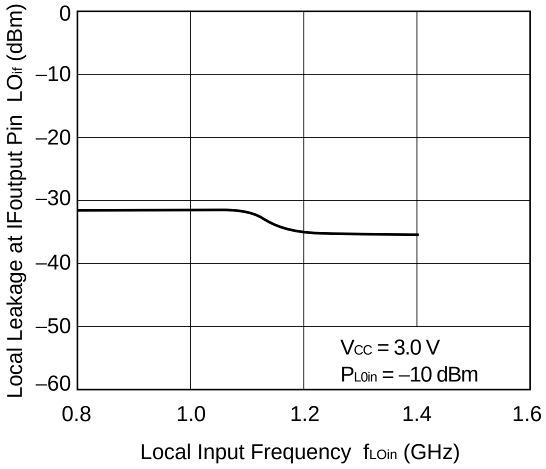


IF OUTPUT POWER, IM3 vs. RF INPUT POWER

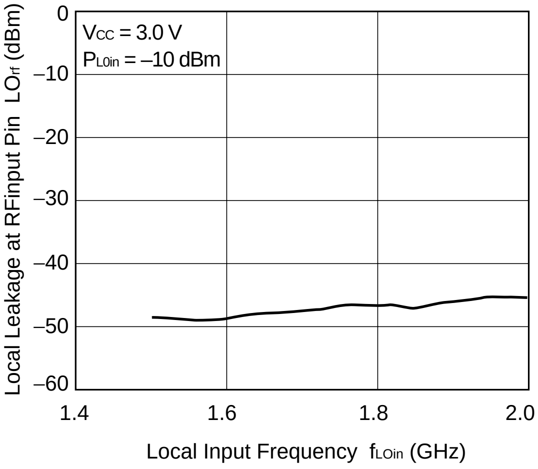


– ON THE APPLICATION CIRCUIT –

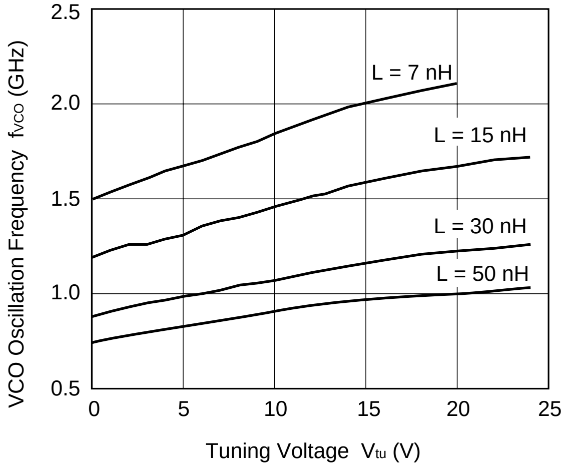
LO LEAKAGE AT IFoutput PIN vs.
LOCAL INPUT FREQUENCY



LO LEAKAGE AT RFinput PIN vs.
LOCAL INPUT FREQUENCY

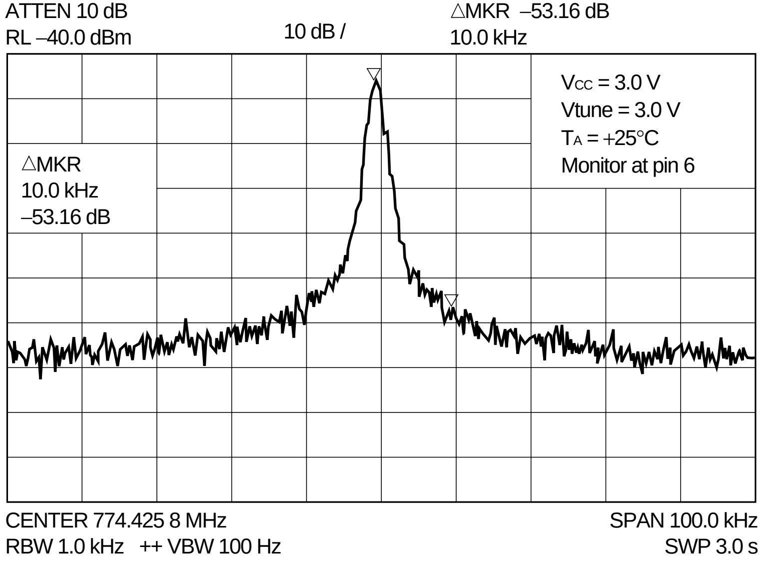


VCO OSCILLATION FREQUENCY vs.
TUNING VOLTAGE

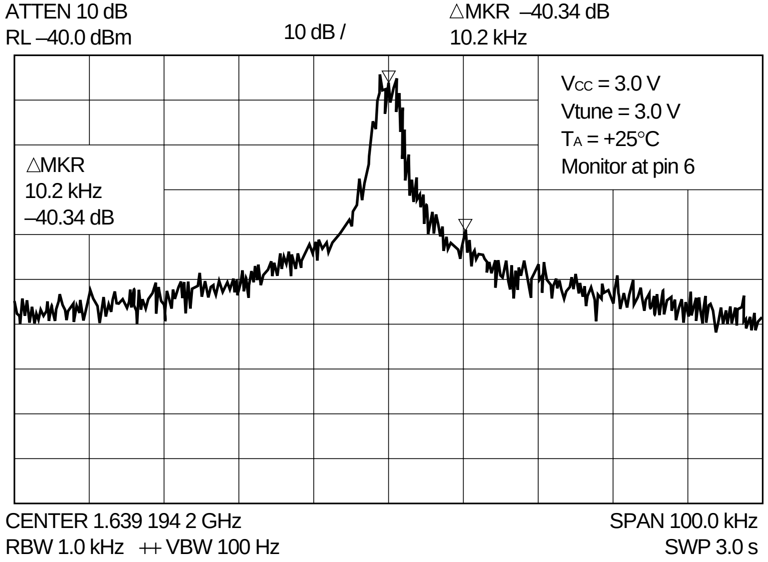


– ON THE APPLICATION CIRCUIT –

VCO Phase Noise (f_{VCO} = 774.425 8 MHz center)



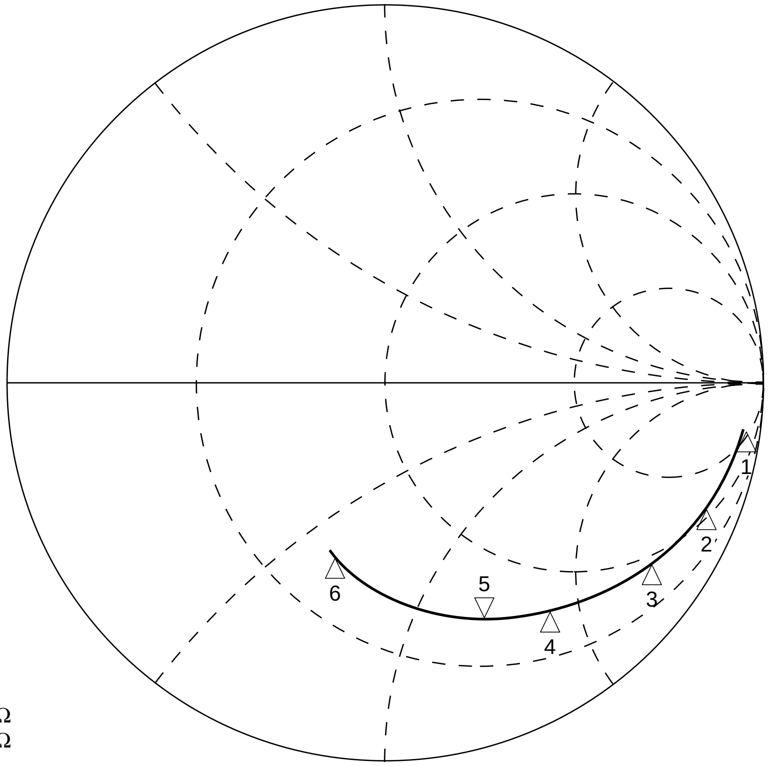
VCO Phase Noise (f_{VCO} = 1.639 194 2 GHz center)



Remark The graphs indicate nominal characteristics.

S-PARAMETERS (VCC = 3.0 V)

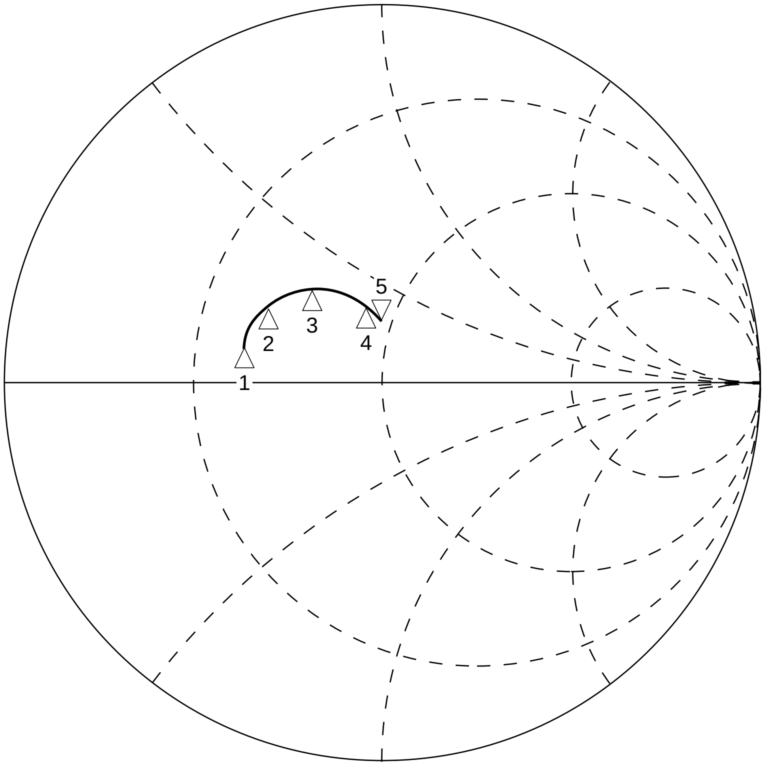
RFinput Pin



$\overset{\triangle}{1}$: 100 MHz 519.8 Ω – j 1.1 Ω
$\overset{\triangle}{2}$: 500 MHz 59.3 Ω – j 281.0 Ω
$\overset{\triangle}{3}$: 900 MHz 38.3 Ω – j 157.0 Ω
$\overset{\triangle}{4}$: 1 500 MHz 31.5 Ω – j 90.1 Ω
$\overset{\triangle}{5}$: 1 900 MHz 28.5 Ω – j 67.9 Ω
$\overset{\triangle}{6}$: 3 000 MHz 25.7 Ω – j 31.7 Ω

START 0.100000000 GHz
STOP 3.100000000 GHz

IFoutput Pin

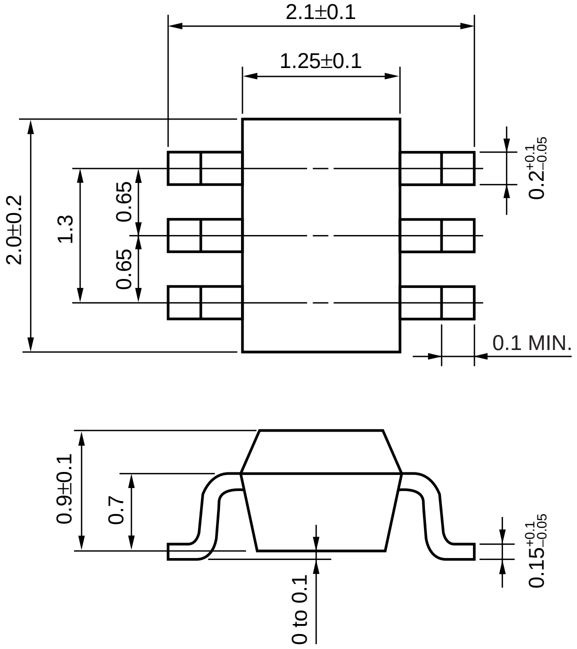


$\overset{\triangle}{1}$: 50 MHz 22.5 Ω + j 6.1 Ω
$\overset{\triangle}{2}$: 80 MHz 24.2 Ω + j 11.3 Ω
$\overset{\triangle}{3}$: 130 MHz 30.2 Ω + j 16.6 Ω
$\overset{\triangle}{4}$: 240 MHz 42.6 Ω + j 17.5 Ω
$\overset{\triangle}{5}$: 300 MHz 46.6 Ω + j 15.6 Ω

START 0.050000000 GHz
STOP 0.300000000 GHz

★ PACKAGE DIMENSIONS

6-PIN SUPER MINIMOLD (UNIT: mm)



NOTE ON CORRECT USE

(1) Observe precautions for handling because of electro-static sensitive devices.
(2) Form a ground pattern as widely as to minimize ground impedance (to prevent abnormal oscillation).
(3) Keep the track length between the ground pins as short as possible.
(4) Connect a bypass capacitor (example 1 000 pF) to the V_{CC} pin.
(5) To construct oscillator, tank circuit must be externally attached to pin 3 and pin 4.

RECOMMENDED SOLDERING CONDITIONS

This product should be soldered under the following recommended conditions. For soldering methods and conditions other than those recommended below, contact your NEC sales representative.

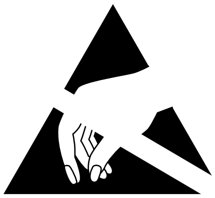
Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared Reflow	Package peak temperature: 235°C or below Time: 30 seconds or less (at 210°C) Count: 3, Exposure limit: None[Note]	IR35-00-3
VPS	Package peak temperature: 215°C or below Time: 40 seconds or less (at 200°C) Count: 3, Exposure limit: None[Note]	VP15-00-3
Wave Soldering	Soldering bath temperature: 260°C or below Time: 10 seconds or less Count: 1, Exposure limit: None[Note]	WS60-00-1
Partial Heating	Pin temperature: 300°C or below Time: 3 seconds or less (per side of device) Exposure limit: None[Note]	–

Note After opening the dry pack, keep it in a place below 25°C and 65% RH for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating).

For details of recommended soldering conditions for surface mounting, refer to information document **SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL (C10535E)**.

[MEMO]



ATTENTION

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FOR HANDLING
ELECTROSTATIC
SENSITIVE
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