

UPC4570

Ultra Low-Noise, High Speed, Wide Band, Dual Operational Amplifier

DESCRIPTION

UPC4570 is a high performance version of general-purpose low-noise operational amplifier UPC258, 4558. Various characteristics such as band, slew rate, including input equivalent noise were greatly improve in comparison to UPC258 and 4558. It is also possible to operate the amplifier with stability for gain of 1 (total feedback or unity gain)

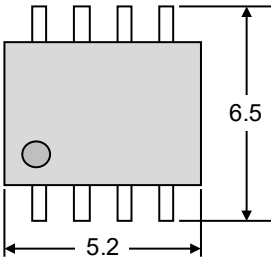
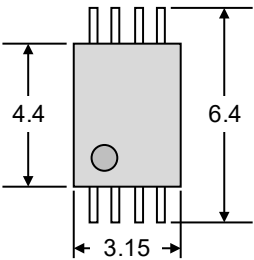
Therefore, it is ideal for application circuits such as audio preamplifiers, equalizers, tone controls, active filters.

Under this product series, there is also a quad type UPC4574 with equivalent characteristics

FEATURES

- Input Equivalent Noise Voltage (f = 1 kHz) 4.5 nV/√Hz (TYP.)
- Total Harmonic Distortion Rate (f = 20 Hz ~ 20 kHz) 0.002 % (TYP.)
- Slew Rate 7 V/μs (TYP.)
- Gain Bandwidth Product GBW (f = 100 kHz) 15 MHz (TYP.)
- Input Offset Voltage ±0.3 mV (TYP.)
- Operating Ambient Temperature
UPC4570G2 : -20 ~ +80 °C
UPC4570GR : -40 ~ +85 °C
- Internal Frequency Compensation

PRODUCT LINEUP

Package	Standard SOP	TSSOP
Subject Part Number	UPC4570G2	UPC4570GR-9LG
Outline Comparison	Unit : mm 	Unit : mm 
(Mounting Area Ratio)	(100 %)	(60 %)

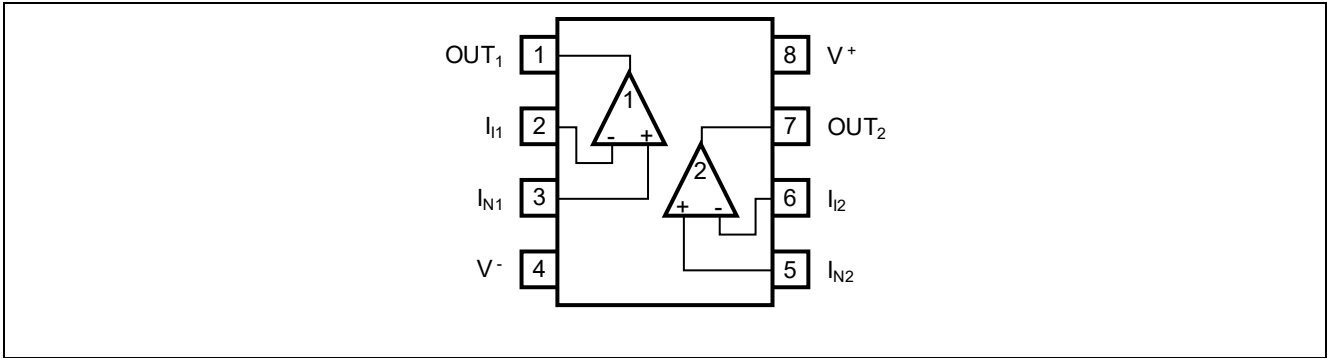
ORDERING INFORMATION

Order Name ⁽¹⁾	Selected Grade	Package
UPC4570G2-AP	Standard	8-pin plastic SOP (5.72 mm (225))
UPC4570GR-9LG-A	Standard	8-pin plastic TSSOP (5.72 mm (225))

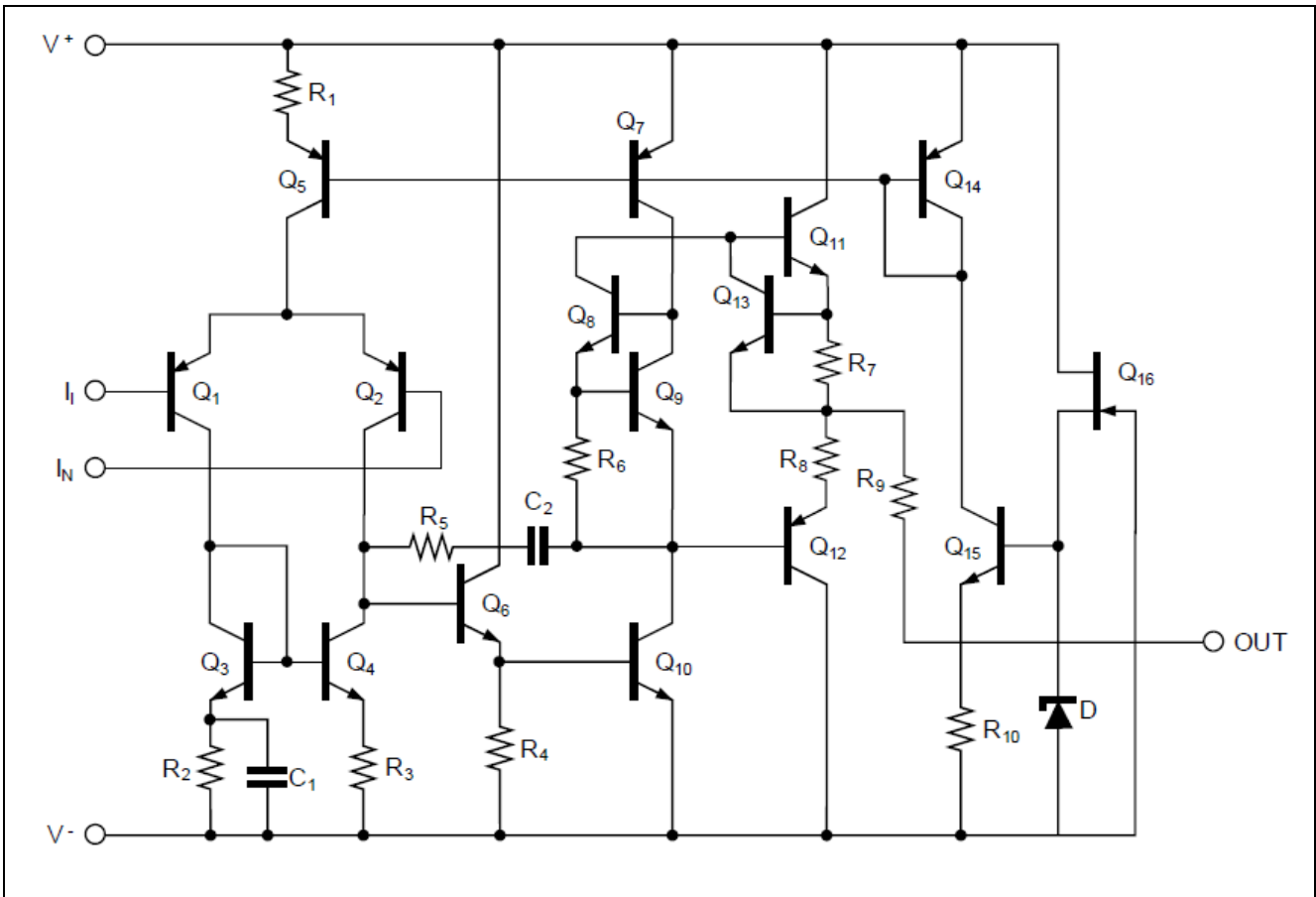
(1) Order names containing E1 or E2 indicate that the packaging format is embossed taping.

Pin 1 of E1 is on draw-out side, and pin 1 of E2 is at take-up side.

PIN CONFIGURATION (Top View)



EQUIVALENT CIRCUIT (1/2 Circuit)



ABSOLUTE MAXIMUM RATINGS(T_A = 25 °C)

Parameter	Symbol	UPC4570G2	UPC4570GR-9LG	Unit
Power Supply Voltage ^{Note 1}	V ⁺ - V ⁻	-0.3 ~ +36		V
Differential Input Voltage	V _{ID}	±30		V
Input Voltage ^{Note 2}	V _I	V ⁻ -0.3 ~ V ⁺ +0.3		V
Output Applied Voltage ^{Note 3}	V _O	V ⁻ -0.3 ~ V ⁺ +0.3		V
Total Power Dissipation ^{Note 4}	P _T	440		mW
Output Short Circuit Duration ^{Note 5}	t _s	10		s
Operating Ambient Temperature	T _A	-20 ~ +80	-40 ~ +85	°C
Storage Temperature	T _{stg}	-55 ~ +125		°C

[Note] 1. Note that reverse connections of the power supply may damage the ICs.

2. The input terminal must be applied within the input voltage range to avoid deteriorating or damaging the device characteristic. Do not exceed the ratings including during transition state such as ON/OFF, etc. The Op-Amp input voltage must operate within the electrical characteristics range of input common-mode voltage.

3. The output terminal must be applied within the output voltage range to avoid deteriorating or damaging the device characteristic. Do not exceed the ratings including during transition state such as ON/OFF, etc. The Op-Amp output voltage must operate within the electrical characteristics range of maximum output voltage.

4. This is the value when the glass epoxy substrate (size: 100 mm x 100 mm, thickness: 1 mm, 15% of the substrate area where only one side is copper foiled is filling wired) is mounted.

Note that restrictions will be made to the following conditions for each product, and the de-rating ratio depending on the operating ambient temperature.

UPC4570G2 : This is the value at T_A ≤ 25 °C. Derate at -4.4 mW/°C when T_A > 25 °C

UPC4570GR : This is the value at T_A ≤ 44 °C. Derate at -5.5 mW/°C when T_A > 44 °C

5. A short circuit at the V⁺ side may destroy the IC. Please use below the total loss and the de-rating of Note 4.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Power Supply Voltage	V^{\pm}	± 4		± 16	V
Output Current	I_o			± 10	mA
Source Resistance	R_s			50	k Ω
Capacitive Load ($A_v = +1$)	C_L			100	pF

ELECTRICAL CHARACTERISTICS

(T_A = 25 °C, V[±] = ±15 V)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Test Condition
Input Offset Voltage	V_{IO}		± 0.3	± 5	mV	$R_S \leq 50 \Omega$
Input Offset Current	I_{IO}		± 10	± 100	nA	
Input Bias Current ^{Note 6}	I_B		100	400	nA	
Large Signal Voltage Gain	A_v	30000	300000			$R_L \geq 2 \text{ k}\Omega$, $V_o = \pm 10 \text{ V}$
Circuit Current ^{Note 7}	I_{CC}		5	8	mA	
Common Mode Rejection Ratio	CMR	80	100		dB	
Supply Voltage Rejection Ratio	SVR	80	100		dB	
Output Voltage Swing	V_{om}	± 12	± 13.4		V	$R_L \geq 10 \text{ k}\Omega$
Output Voltage Swing	V_{om}	± 10	± 12.8		V	$R_L \geq 2 \text{ k}\Omega$
Common Mode Input Voltage Range	V_{ICM}	± 12	± 14		V	
Slew Rate	SR	5	7		V/ μ s	$R_L \geq 2 \text{ k}\Omega$
Gain Bandwidth Product	GBW	10	15		MHz	$f_o = 100 \text{ kHz}$
Unity Gain Frequency	f_{unity}		7		MHz	open loop
Phase Margin	ϕ_{unity}		50		Deg	open loop
Total Harmonic Distortion	THD		0.002		%	$V_o = 3 V_{r.m.s.}$, $f = 20 \text{ Hz} \sim 20 \text{ kHz}$ (Figure 1)
Input Equivalent Noise Voltage	V_n		0.9		μ V _{r.m.s.}	RIAA (Figure 2)
Input Equivalent Noise Voltage	V_n		0.53	0.65	μ V _{r.m.s.}	FLAT + JIS A, $R_S = 100 \Omega$ (Figure 3)
Input Equivalent Noise Voltage Density	e_n		5.5		nV/ $\sqrt{\text{Hz}}$	$f_o = 10 \text{ Hz}$, $R_S = 100 \Omega$
Input Equivalent Noise Voltage Density	e_n		4.5		nV/ $\sqrt{\text{Hz}}$	$f_o = 1 \text{ kHz}$, $R_S = 100 \Omega$
Input Equivalent Noise Current Density	i_n		0.7		pA/ $\sqrt{\text{Hz}}$	$f_o = 1 \text{ kHz}$
Channel Separation			120		dB	$f = 20 \text{ Hz} \sim 20 \text{ kHz}$

【Note】 6. The current flow direction of the input bias is out from the IC because the first stage of the IC composed of PNP transistor.

7. Current flowing through the internal circuit. This current flow regardless of the channel used.

MEASUREMENT CIRCUIT

Figure 1: Total Harmonic Distortion Measurement Circuit

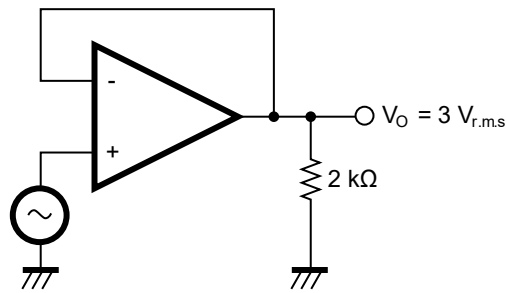


Figure 2: Noise Measurement Circuit (RIAA)

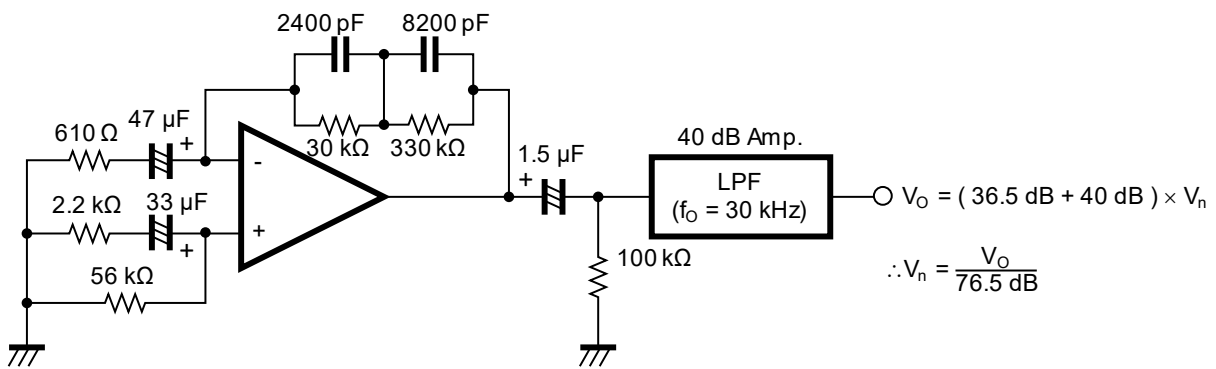
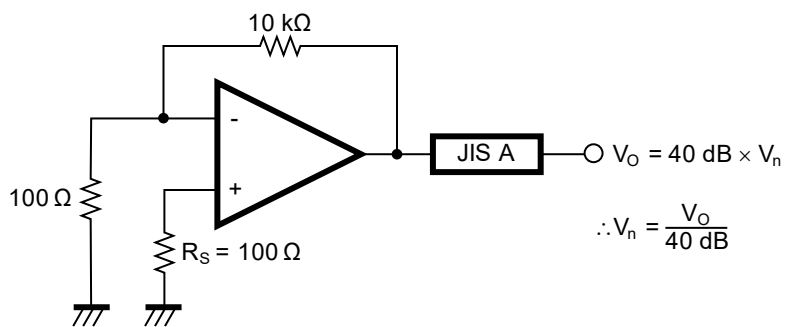
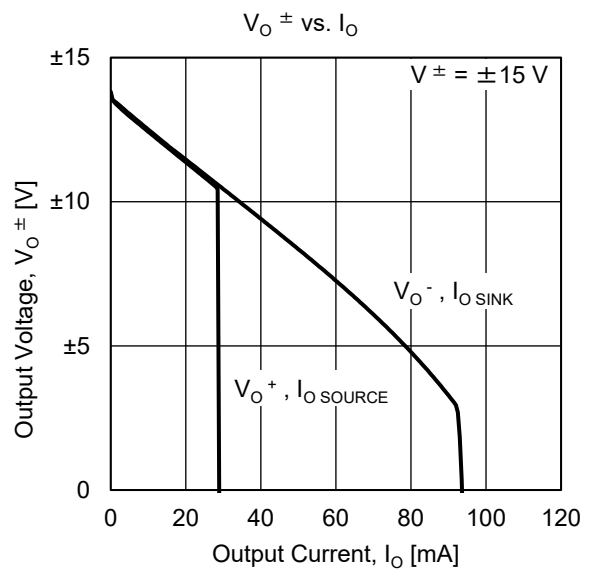
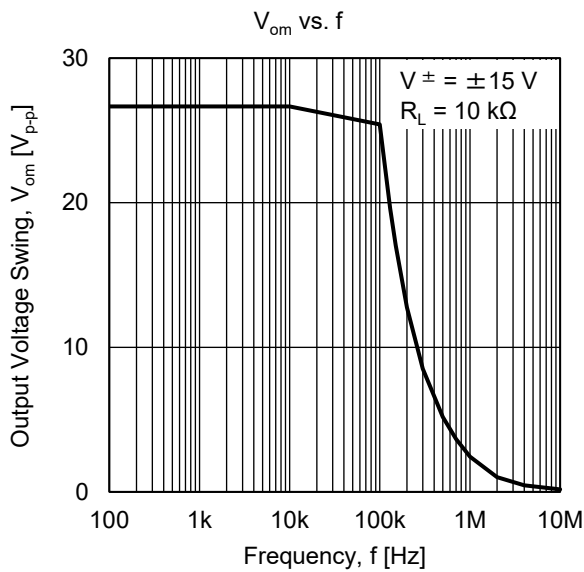
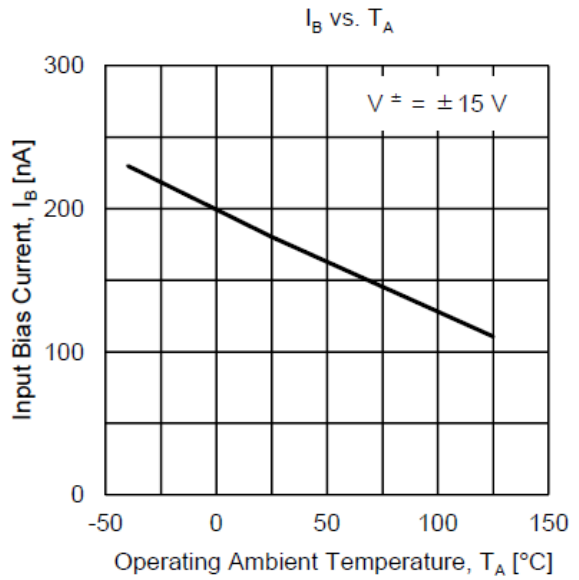
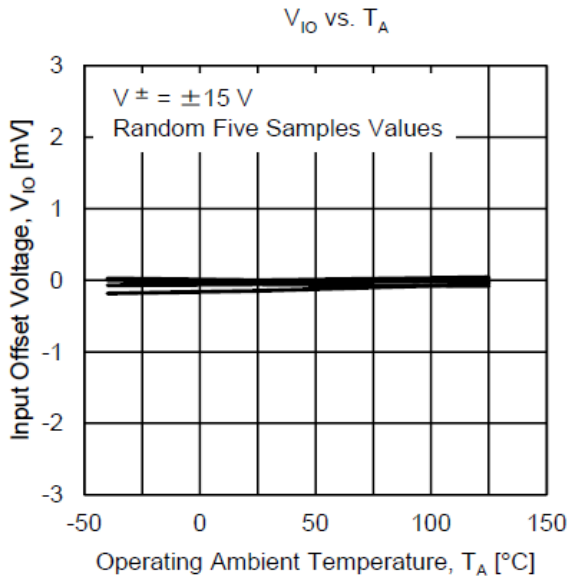
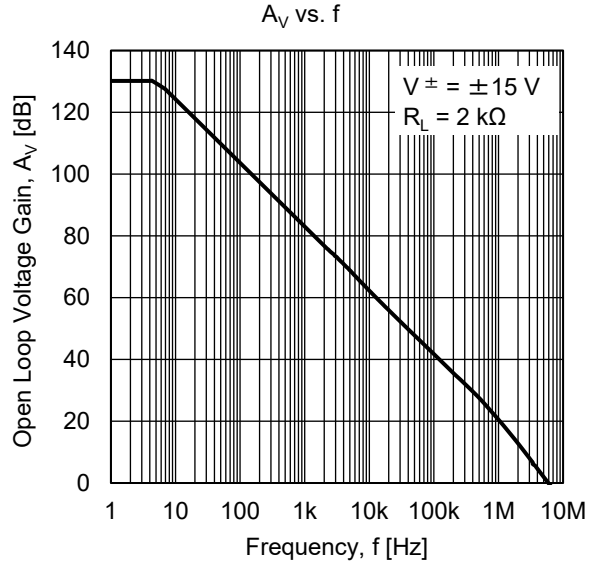
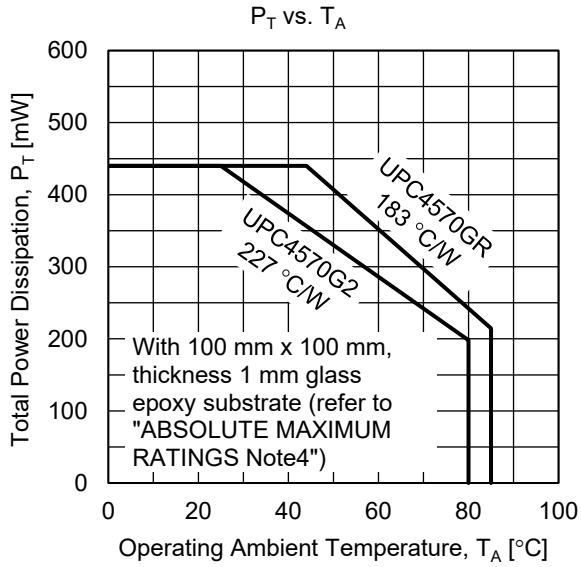
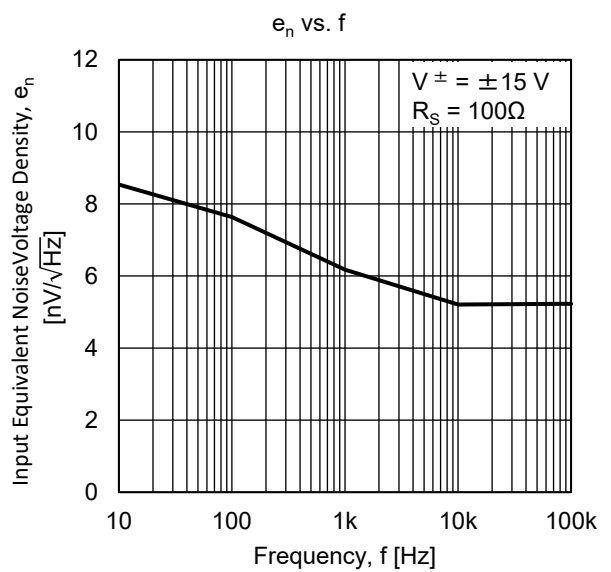
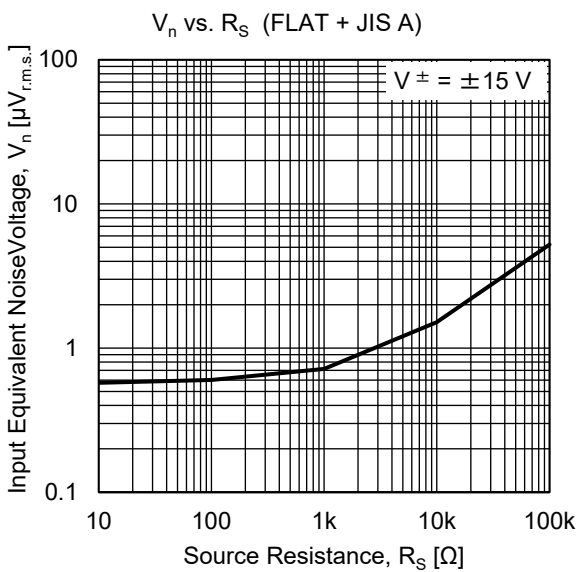
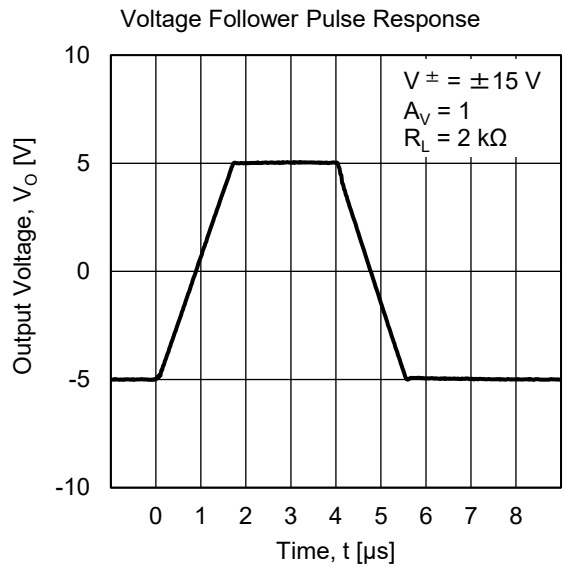
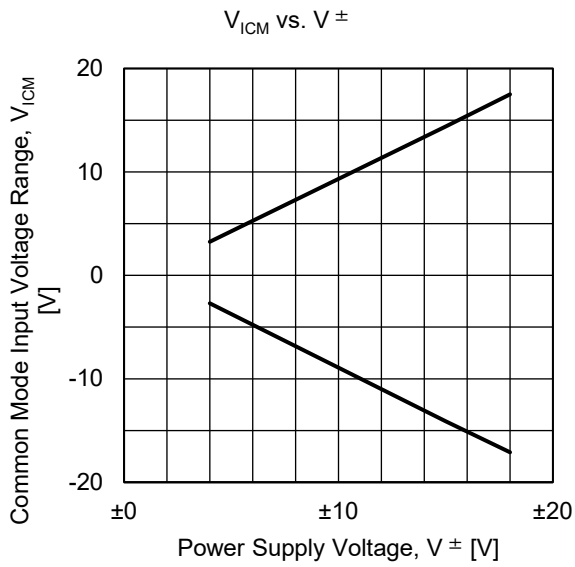
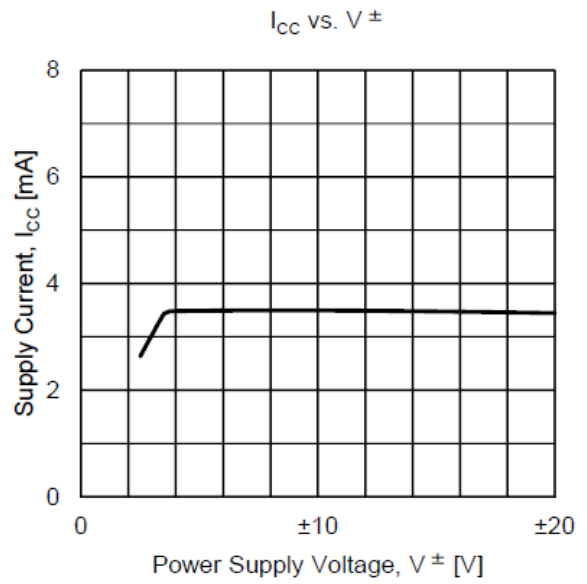
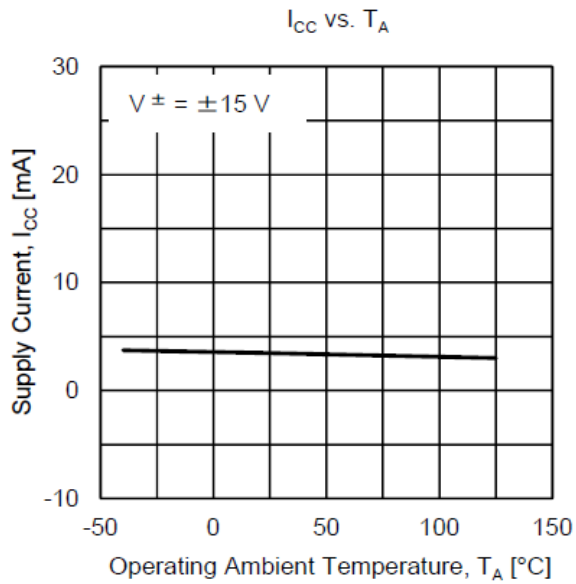


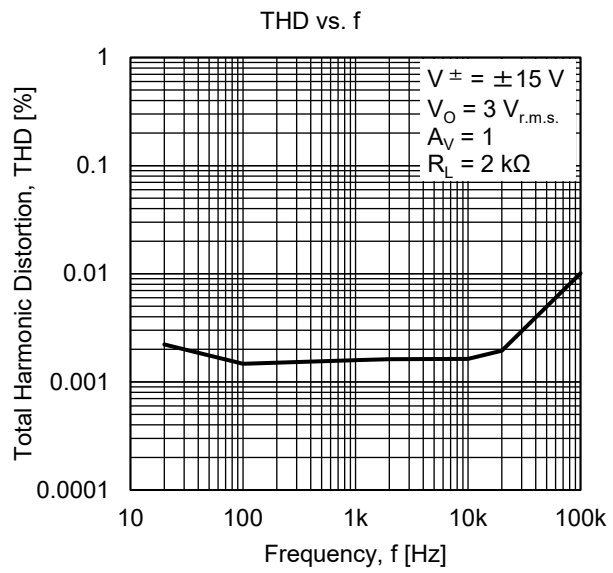
Figure 3: Noise Measurement Circuit (FLAT+JIS A)



ELECTRICAL CHARACTERISTICS



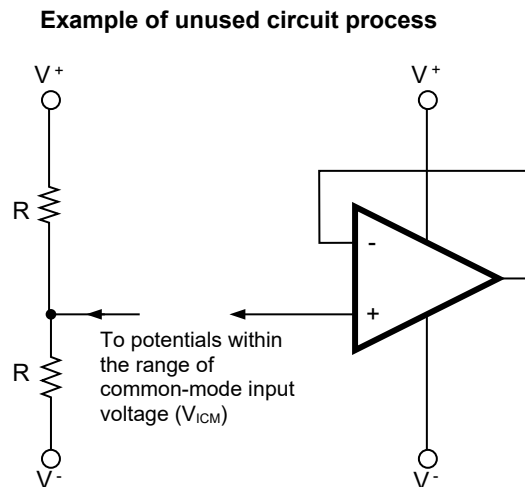




USE WITH PRECAUTIONS

- **Managing unused circuits**

If there is an unused circuit, the following connection is recommended.



Remark: In this example, an intermediate potential between V^+ and V^- is applied.

- **Power Supply (Dual Power Supply / Single Power Supply)**

The op amp operates when a predetermine voltage is applied between $V^+ - V^-$. Therefore, while it operates from a single power supply ($V^- = \text{GND}$), it is not possible to operate the input and output near GND. So please be careful of the common-mode input voltage range and maximum output voltage.

- **Ratings of input/output pin voltage**

When the voltage of input/output pin exceeds the absolute maximum rating, the parasitic diode within the IC may conduct, causing characteristics degradation or damage. In addition, if the input pin is lower than V^- , or the output pin exceeds the power supply voltage, it is recommended to make a clamping circuit using a diode with low forward voltage (e.g.: Schottky diode) as protection.

- **Range of common-mode input voltage**

When the supply voltage does not meet the condition of electrical characteristics, the range of common-mode input voltage is as follows.

$$V_{ICM} (\text{TYP.}): V^- + 1 \sim V^+ - 1 [\text{V}] (T_A = 25^\circ\text{C}).$$

During designing, do include some tolerance by considering temperature characteristics etc.

- **Maximum output voltage**

The TYP. value range of the maximum output voltage when the supply voltage does not meet the condition of electrical characteristics is as follows:

$$V_{om}^+ (\text{TYP.}): V^+ - 1.6 [\text{V}] (T_A = 25^\circ\text{C}), \quad V_{om}^- (\text{TYP.}): V^- + 1.6 [\text{V}] (T_A = 25^\circ\text{C})$$

During designing, do include some tolerance by considering characteristics variation, temperature characteristics and so on. In addition, also note that the output voltage range ($V_{om}^+ - V_{om}^-$) will become narrow when the output current increases.

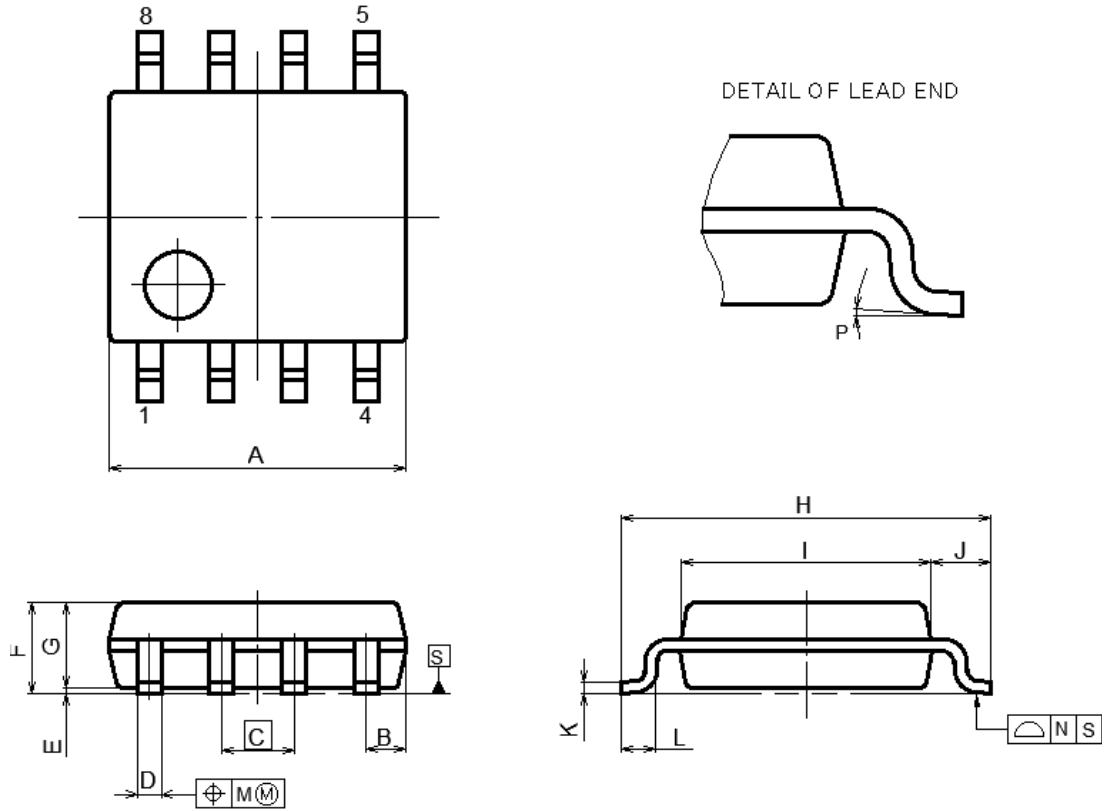
- **Handling of ICs**

When stress is added to ICs due to warpage or bending of a board, the characteristic may fluctuates due to piezoelectric (piezo) effect. Therefore, pay attention to warpage or bending of a board.

PACKAGE DRAWINGS

8-PIN PLASTIC SOP

JEITA Package code	RENESAS code	MASS (TYP.) [g]
P-LSOP8-4.4×5.2-1.27	PLSP0008DE-A	0.09[g]



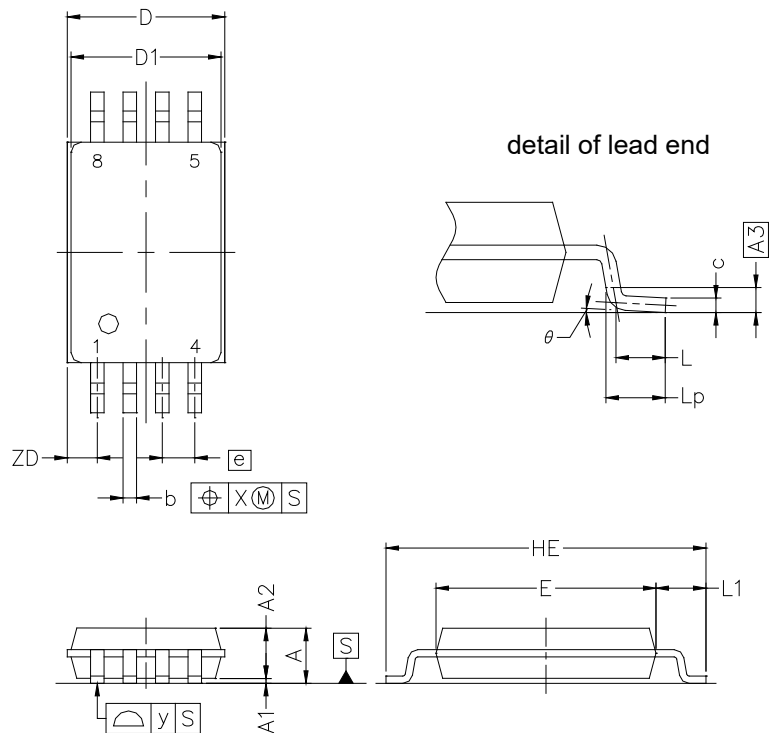
NOTE
 EACH LEAD CENTERLINE IS LOCATED WITHIN 0.12 MM OF ITS TRUE POSITION(T.P.) AT MAXIMUM MATERIAL CONDITION.

(UNIT:mm)

ITEM	DIMENSIONS
A	5.2±0.17
B	0.78MAX
C	1.27(T.P)
D	0.40±0.05
E	0.1±0.1
F	1.59±0.21
G	1.49
H	6.5±0.3
I	4.4±0.1
J	1.05±0.15
K	0.2±0.07
L	0.6±0.20
M	0.1MAX
N	0.1MAX
P	4°±4°

8-PIN PLASTIC TSSOP

JEITA Package code	RENESAS code	Previous code	MASS(TYP.) [g]
P-TSSOP8-0225-0.65	PTSP0008JD-A	P8GR-65-9LG	—



(Unit : mm)

NOTE

Each lead centerline is located within 0.10 mm of its true position at maximum material condition.

ITEM	MILLIMETERS
D	3.15 ±0.15
D1	3.00 ±0.10
E	4.40 ±0.10
HE	6.40 ±0.20
A	1.20 MAX.
A1	0.10 ±0.05
A2	1.00 ±0.05
A3	0.25
b	0.24 ^{+0.06} _{-0.05}
c	0.145 ±0.055
L	0.5
Lp	0.60 ±0.15
L1	1.00 ±0.20
θ	3° ^{+5°} _{-3°}
e	0.65
x	0.10
y	0.10
ZD	0.60

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