

μPC4572MF-DAA

Low Supply Voltage, Ultra Low-Noise, High Speed,
Wide Band, Low I_B Dual Operational Amplifier
 $V_n = 0.8 \mu V_{r.m.s.}$, $SR = 6 V/\mu s$, $GBW = 16 MHz$, $V_{IO} = \pm 0.3 mV$

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Rev.1.00
Jul 25, 2012

Description

The μPC4572MF-DAA is a dual wide band, ultra low noise operational amplifier designed for low supply voltage operation of +4 V to +14 V single supply and ±2 V to ±7 V split supplies. Using high h_{FE} PNP transistors for the input circuit, Input bias current and input equivalent noise are better than conventional wide band operational amplifier.

The μPC4572 MF-DAA is an excellent choice for preamplifiers and active filters in audio, instrumentation, and communication circuit.

Features

- Ultra low noise ($f = 1 kHz$): $4.0 nV/\sqrt{Hz}$ (TYP.)
- Input equivalent noise voltage: $0.8 \mu V_{r.m.s.}$ (TYP.)
- Total harmonic distortion: 0.002% (TYP.)
- High slew rate : $6 V/\mu s$ (TYP.)
- Gain bandwidth product ($f = 100 kHz$): 16 MHz (TYP.)
- Low input bias current: 100 nA (TYP.)
- Input offset voltage : $\pm 0.3 mV$ (TYP.)
- Low supply voltage: $\pm 2 V$ to $\pm 7 V$ (Split)
+4 V to +14 V (Single, $V^- = GND$)
- Internal frequency compensation

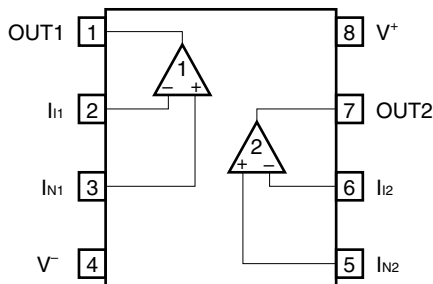
Ordering Information

Part Number	Package	Package Code (Previous Package Code)	Package Abbreviation	Supplying Form
μPC4572MF-DAA-E1-AT ^{*1}	8-pin plastic SOP (3.9 × 4.9)	PRSP0008DM-A (-)	MF	<ul style="list-style-type: none"> • 12 mm wide embossed taping • Pin 1 on draw-out side • 2500 p/reel

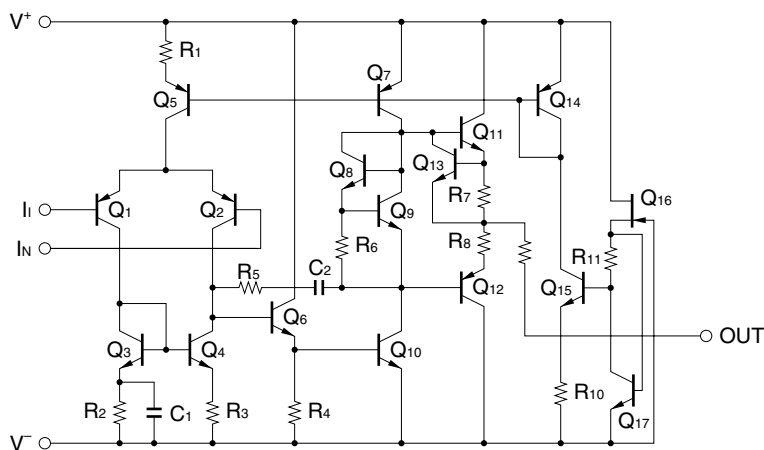
Note: *1. Pb-free (This product does not contain Pb in the external electrode and other parts.)

Caution: Do not use the products in applications such as the transportation equipment (a car, a train, a ship, etc.) where “Special quality grade” is required, because the products are placed in a quality grade “standard” to be required at general devices.

Pin Configuration (Top View)



Equivalent Circuit (for Each Circuit)



Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Ratings	Unit
Voltage between V ⁺ and V ⁻ *1	V ⁺ - V ⁻	-0.3 to +15	V
Differential Input Voltage	V _{ID}	±10	V
Input Voltage *2	V _I	V ⁻ - 0.3 to V ⁺ + 0.3	V
Output Applied Voltage *3	V _O	V ⁻ - 0.3 to V ⁺ + 0.3	V
Total Power Dissipation *4	P _T	440	mW
Output Short Circuit Duration (vs. GND) *5	t _s	10	s
Operating Ambient Temperature	T _A	-40 to +85	°C
Storage Temperature	T _{stg}	-55 to +125	°C

Notes: *1. Note that reverse connections of the power supply may damage ICs.

*2. The input voltage is allowed to input without damage or destruction independent of the magnitude of V⁺. Either input signal is not allowed to go negative by more than 0.3 V. In addition, the input voltage that operates normally as an operational amplifier is within the Common Mode Input Voltage range of an electrical characteristic.

*3. A range where input voltage can be applied to an output pin externally with no deterioration or damage to the feature (characteristic). The input voltage can be applied regardless of the electric supply voltage. This specification which includes the transition state such as electric power ON/OFF must be kept.

*4. This is the value in T_A ≤ 56°C of when the glass epoxy substrate (size: 100 mm x 100 mm, thickness: 1 mm, 15% of the substrate area where only one side is copper foiled is filling wired) is mounted. Derate at -6.4 mW/°C when T_A > 56°C. In the condition same as the above, Junction - ambient thermal resistance R_{th(J-A)} = 156°C/W.

*5. Only as for V⁺ ≤ 15V and any 1 channel. Please use the product within the derating condition or Total Power Dissipation, which are showed in Note 4.

Recommended Operating Conditions

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Power Supply Voltage (Split)	V^{\pm}	±2	±5	±7	V
Supply Voltage ($V^- = \text{GND}$)	V^+	+4	+5 to +12	±14	V
Output Current	I_O			±10	mA
Capacitive Load ($A_V = +1$)	C_L			100	pF

Electrical Characteristics ($V^{\pm} = \pm 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Conditions
Input Offset Voltage	V_{IO}		±0.3	±5	mV	$R_S \leq 50 \Omega$
Input Offset Current	I_{IO}		±10	±100	nA	
Input Bias Current *1	I_B		100	400	nA	
Large Signal Voltage Gain	A_V	10000	100000			$R_L \geq 2 \text{ k}\Omega$, $V_O = \pm 2 \text{ V}$
Supply Current *2	I_{CC}		4.5	7	mA	$I_O = 0 \text{ A}$
Common Mode Rejection Ratio	CMR	70	90		dB	
Supply Voltage Rejection Ratio	SVR	70	85		dB	
Output Voltage (High)	V_{OH}	±3.3	±3.7		V	$R_L \geq 10 \text{ k}\Omega$
Output Voltage (Low)	V_{OL}	±3.0	±3.5		V	$R_L \geq 2 \text{ k}\Omega$
Common Model Input Voltage Range	V_{ICM}	±3.5	±4		V	
Output Short Circuit Current	I_O	±15	±20		mA	$R_L = 0 \Omega$
Slew Rate	SR	3.5	6		V/ μs	$R_L \geq 2 \text{ k}\Omega$, $A_V = +1$
Gain Bandwidth Product	GBW	10	16		MHz	$f_O = 100 \text{ kHz}$
Unity Gain Frequency	f_{unity}		9		MHz	open loop
Phase Margin	ϕ_{unity}		60		degree	open loop
Total Harmonic Distortion	THD		0.002		%	$V_O = 1 \text{ V}_{r.m.s.}$, $f = 20 \text{ Hz to } 20 \text{ kHz}$ (Fig.1)
Input Equivalent Noise Voltage	V_n		0.8		$\mu\text{V}_{r.m.s.}$	RIAA (Fig.2)
			0.5	0.65	$\mu\text{V}_{r.m.s.}$	FLAT+JIS A, $R_S = 100 \Omega$ (Fig.3)
Input Equivalent Noise Voltage Density	e_n		4.5		nV/ $\sqrt{\text{Hz}}$	$f_O = 10 \text{ Hz}$
			4.0		nV/ $\sqrt{\text{Hz}}$	$f_O = 1 \text{ kHz}$
Input Equivalent Noise Current Density	i_n		0.7		pA/ $\sqrt{\text{Hz}}$	$f_O = 1 \text{ kHz}$
Channel Separation			120		dB	$f = 20 \text{ Hz to } 20 \text{ kHz}$
Average V_{IO} Temperature Drift	$\Delta V_{IO}/\Delta T$		±2		$\mu\text{V}/^{\circ}\text{C}$	

Notes: *1. Input bias currents flow out from IC. Because each current is base current of PNP-transistor on input stage.

*2. This is a current that flows in the internal circuit. This current flows irrespective of the existence of use.

Electrical Characteristics ($V^+ = +5\text{ V}$, $V^- = \text{GND}$, $T_A = 25^\circ\text{C}$)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Conditions
Input Offset Voltage	V_{IO}		± 0.3	± 5	mV	$R_S \leq 50\ \Omega$
Input Offset Current	I_{IO}		± 10	± 100	nA	
Input Bias Current ^{*1}	I_B		100	400	nA	
Large Signal Voltage Gain	A_V	8000	80000			
Supply Current ^{*2}	I_{CC}		4	6	mA	$I_O = 0\ \text{A}$
Common Mode Rejection Ratio	CMR	60	75		dB	
Supply Voltage Rejection Ratio	SVR	60	70		dB	
Output Voltage (High)	V_{OH}	3.2	3.5		V	$R_L \geq 2\ \text{k}\Omega$ (R_L to $1/2\ V^+$)
Output Voltage (Low)	V_{OL}		1.3	1.6	V	$R_L \geq 2\ \text{k}\Omega$ (R_L to $1/2\ V^+$)
Common Model Input Voltage Range	V_{ICM}	1.5		3.5	V	
Slew Rate	SR		4		V/ μs	$R_L \geq 2\ \text{k}\Omega$, $A_V = +1$
Gain Band Width Product	GBW		12		MHz	

Notes: *1. Input bias currents flow out from IC. Because each current is base current of PNP-transistor on input stage.

*2. This is a current that flows in the internal circuit. This current flows irrespective of the existence of use.

MEASUREMENT CIRCUIT

Figure1 Total Harmonic Distortion Measurement Circuit

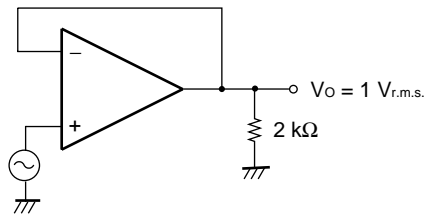


Figure2 Noise Measurement Circuit (RIAA)

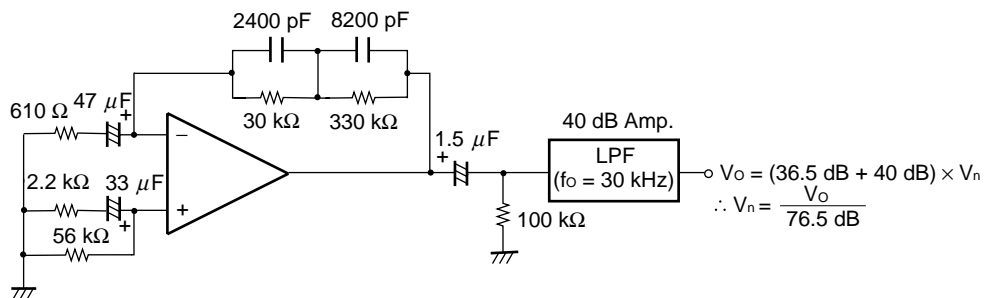
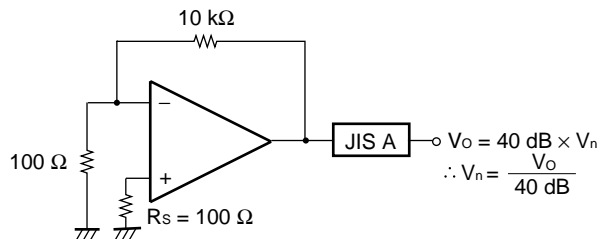
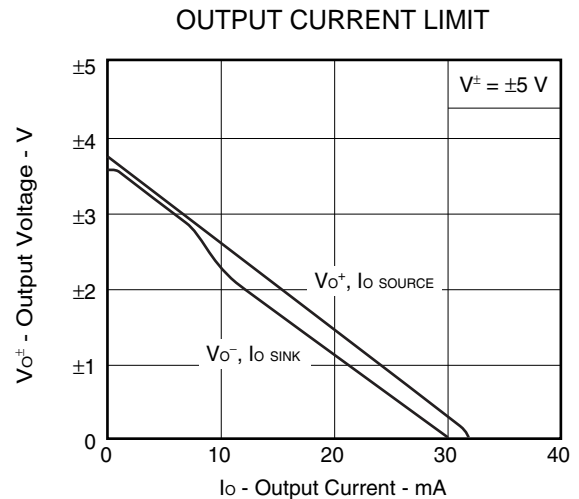
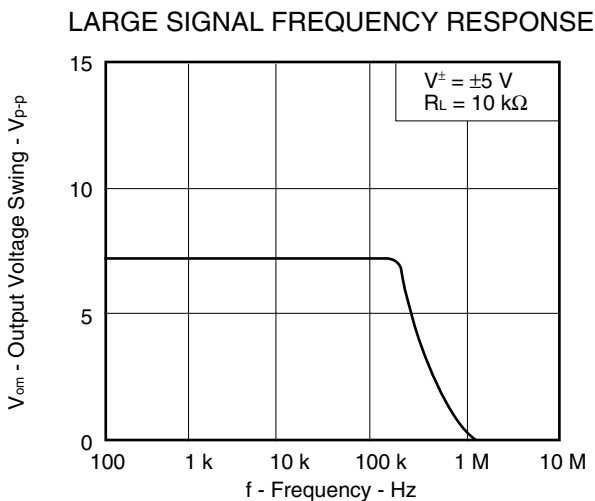
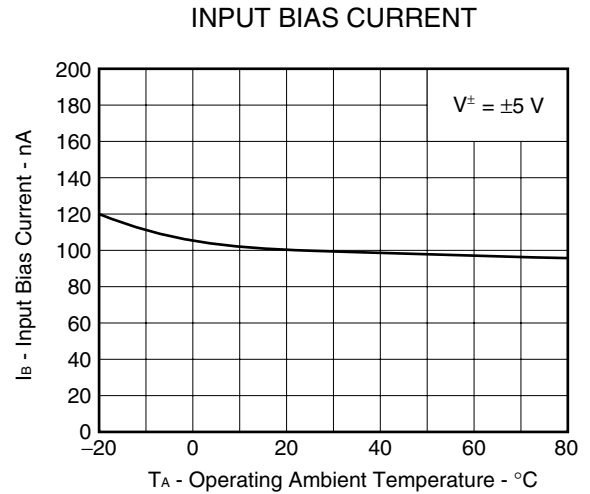
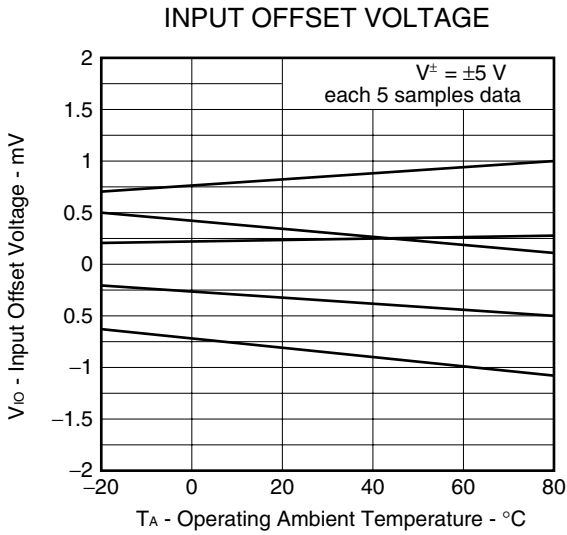
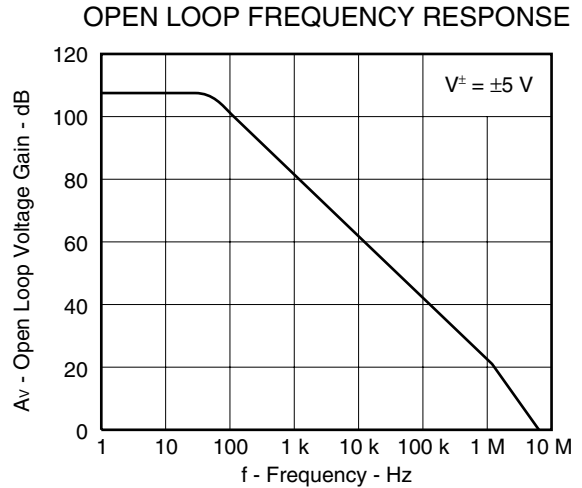
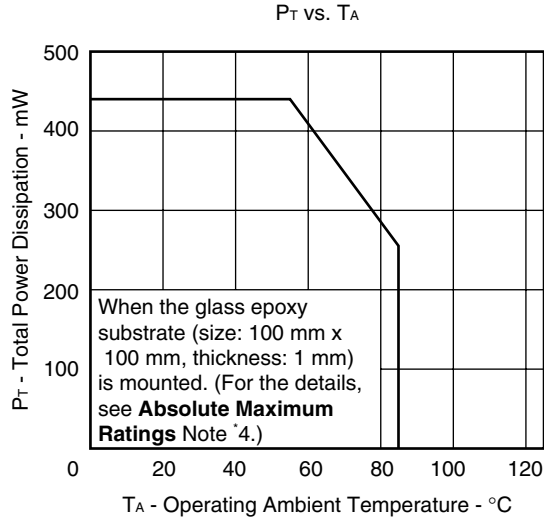


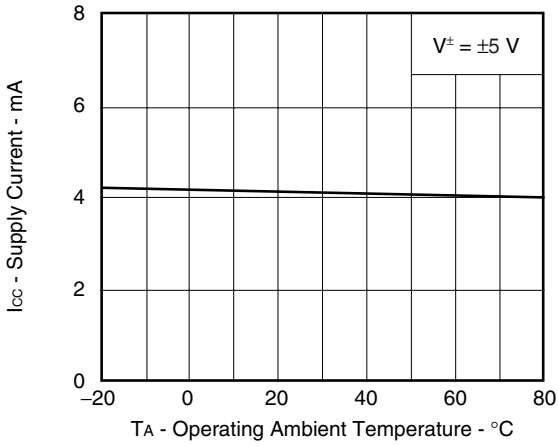
Figure3 Noise Measurement Circuit (FLAT+JIS A)



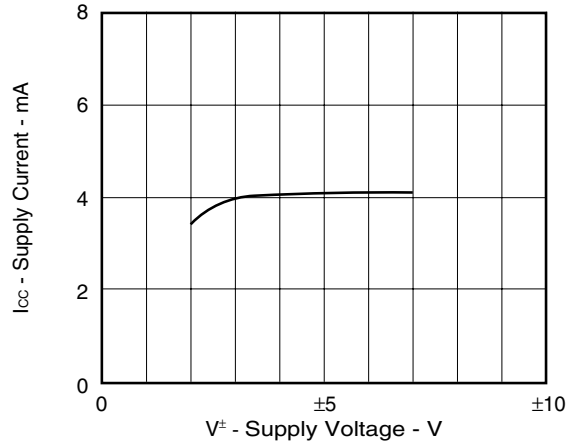
Typical Characteristics (T_A = 25°C, TYP.) (Reference value)



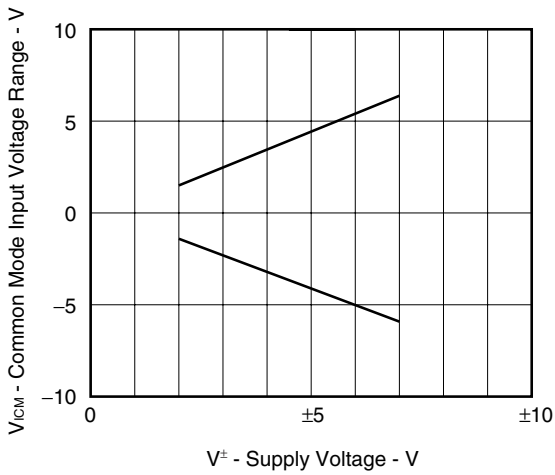
SUPPLY CURRENT vs. TEMPERATURE



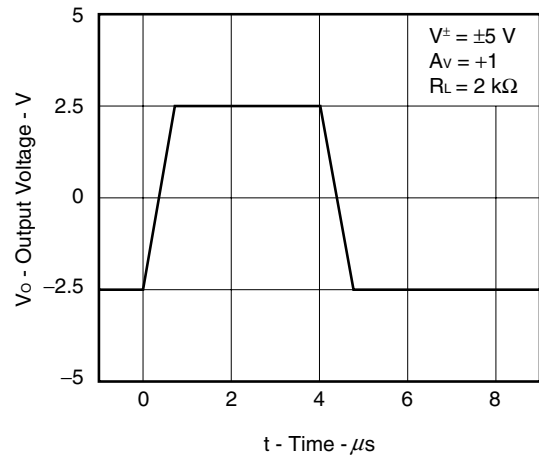
SUPPLY CURRENT vs. SUPPLY VOLTAGE



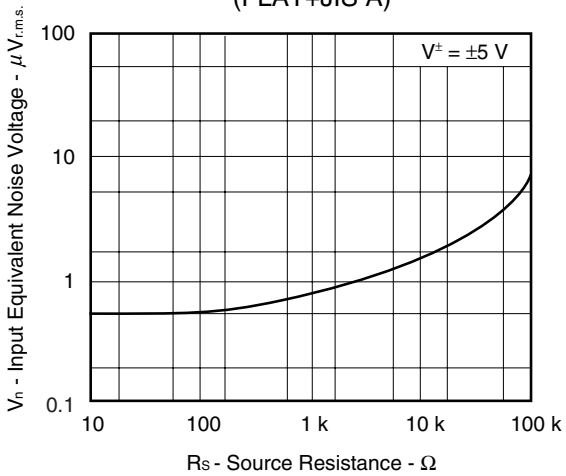
COMMON MODE INPUT VOLTAGE RANGE



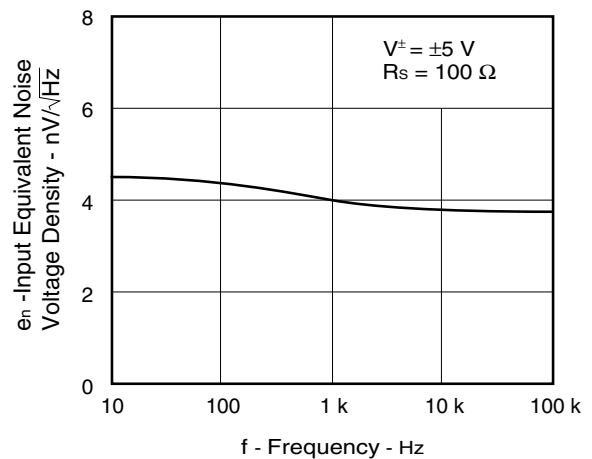
VOLTAGE FOLLOWER PULSE RESPONSE

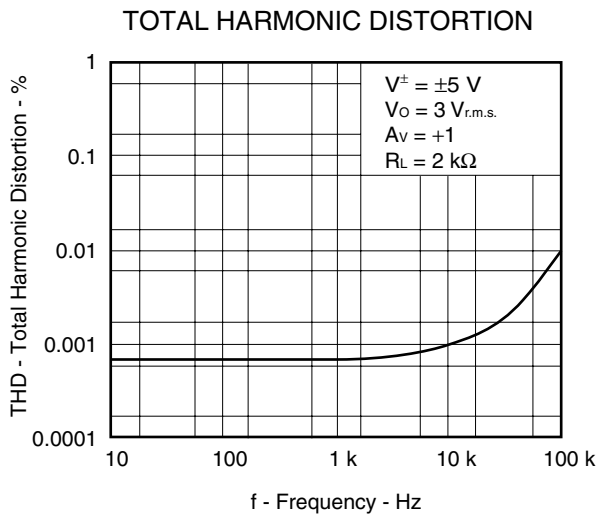


INPUT EQUIVALENT NOISE VOLTAGE (FLAT+JIS A)



INPUT EQUIVALENT NOISE VOLTAGE DENSITY



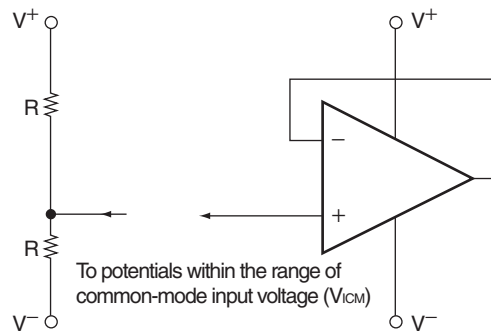


PRECAUTIONS FOR USE

- **The process of unused circuits**

If there is an unused circuit, the following connection is recommended.

Process example of unused circuits



Remark A midpoint potential of V⁺ and V⁻ is applied to this example.

- **Power supply used (Split/Single)**

The input voltage should be allowed to input without damage or destruction. Even during the transition period of supply voltage, power on/off etc., this specification should be kept. The normal operation will establish when the both inputs are within the Common Mode Input Voltage Range of electrical characteristics.

- **Ratings of input/output pin voltage**

When the voltage of input/output pin exceeds the absolute maximum rating, it may cause degradation of characteristics or damages, by a conduction of a parasitic diode within an IC. In addition, when the input pin may be lower than V⁻, or the output pin may exceed the power supply voltage, it is recommended to make a clamp circuit by a diode whose forward voltage is low (e.g.: Schottky diode) for protection.

- **Range of common-mode input voltage**

When the supply voltage does not meet the condition of electrical characteristics, the range of common-mode input voltage is as follows.

V_{ICM} (TYP.): V⁻ + 1 (V) to V⁺ - 1 (V) (T_A = 25°C)

During designing, temperature characteristics for use with allowance.

- **The maximum output voltage**

The range of the TYP. value of the maximum output voltage when the supply voltage does not meet the condition of electrical characteristics is as follows:

V_{om⁺} (TYP.): V⁺ - 1.3 (V) (T_A = 25°C), V_{om⁻} (TYP.): V⁻ + 1.3 (V) (T_A = 25°C)

During designing, consider variations in characteristics and temperature characteristics for use with allowance.

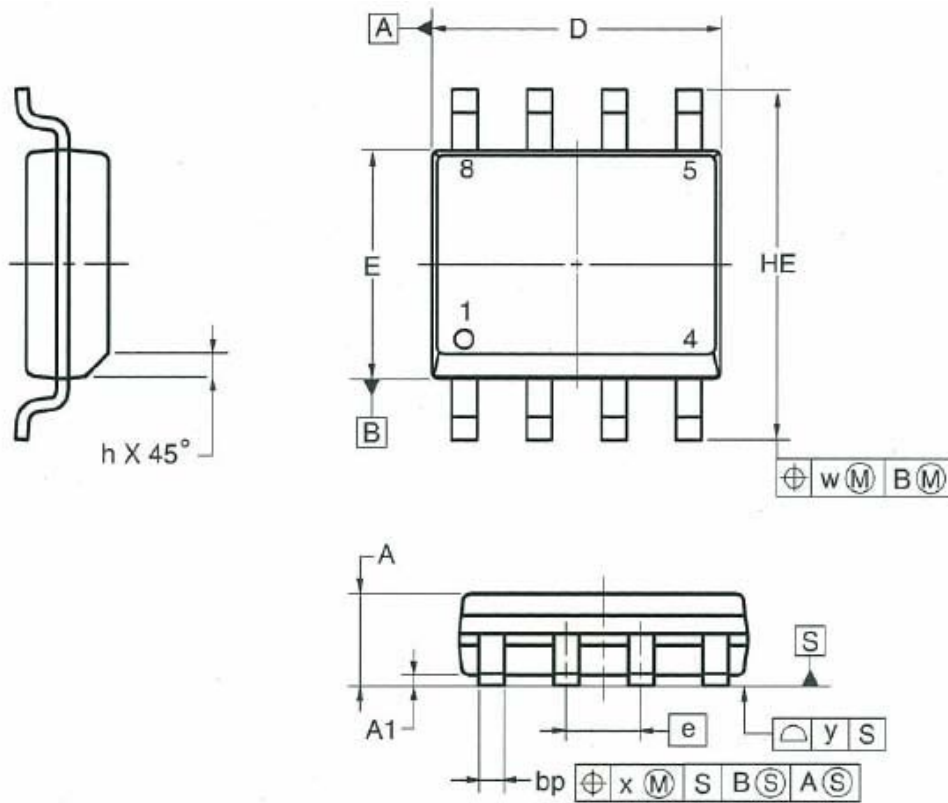
In addition, also note that the output voltage range (V_{om⁺} - V_{om⁻}) becomes narrow when an output current increases.

- **Handling of ICs**

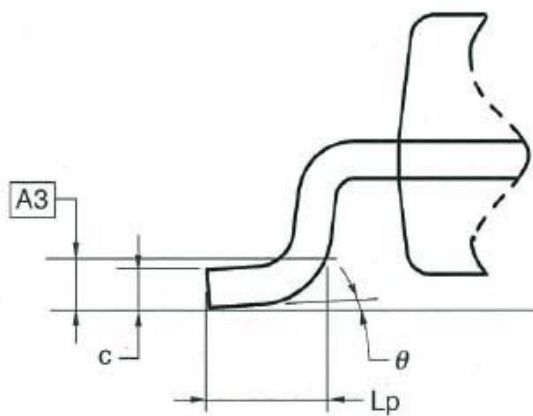
When stress is added to ICs due to warpage or bending of a board, the characteristic fluctuates due to piezoelectric effect. Therefore, pay attention to warpage or bending of a board.

Package Drawings

8-pin Plastic SOP (3.9 × 4.9)



detail of lead end



(UNIT:mm)

ITEM	DIMENSIONS
D	4.80 to 5.00
E	3.80 to 4.00
HE	5.80 to 6.20
e	1.27
bp	0.35 to 0.49
A	1.35 to 1.75
A1	0.10 to 0.25
A3	0.25
c	0.19 to 0.25
Lp	0.40 to 1.25
h	0.25 to 0.50
w	0.25
x	0.25
y	0.10
θ	0° to 7°

Revision History	μPC4572MF-DAA Data Sheet
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Rev.	Date	Description	
		Page	Summary
1.00	Jul 25, 2012	–	First Edition Issued

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