

# μPC812, 4092

High Stability, Low Offset Voltage

R03DS0147EJ0100

J-FET Input Dual Operational Amplifier

Rev.1.00  
2019.06.13

## DESCRIPTION

μPC812, 4092 are unique J-FET input dual operational amplifiers that uses a high-speed PNP transistor ( $f_T = 300 \text{ MHz}$ ) for the output stage to achieve fast response and high stability.

The resistor-trimming method proven in other Renesas High-Precision Op-Amp and High-Precision reference voltage is incorporate in this Op-Amp input stage, thus producing an excellent low offset voltage characteristics that has surpasses conventional general purpose op-amp in spite of being JFET input.

Depending on the operating ambient temperature, μPC812 is suitable to communication application while μPC4092 is for general-purpose usage. In addition to this series of line-up, single channel type operational amplifier, μPC811, 4091 with the same circuit configuration are also available.

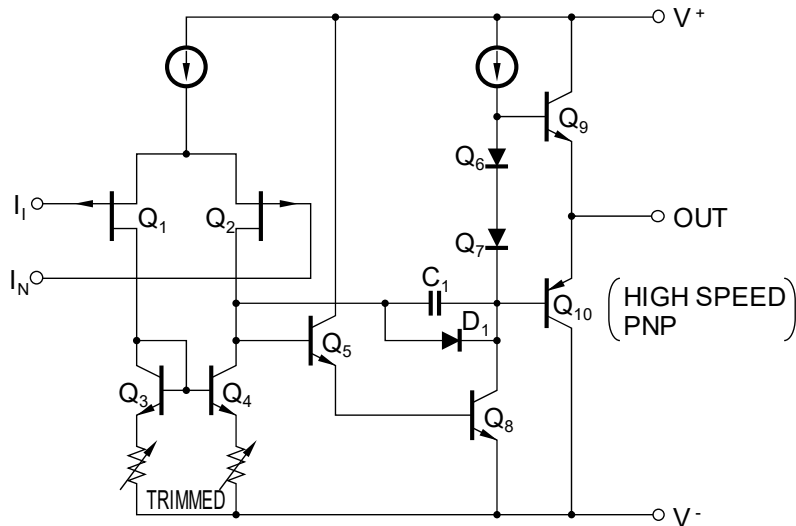
## FEATURES

- Input Offset Voltage  $\pm 1 \text{ mV (TYP.) } (\pm 3 \text{ mV MAX.)}$
- $V_{IO}$  Temperature Drift  $\pm 7 \text{ } \mu\text{V}/^\circ\text{C (TYP.)}$
- Input Bias Current  $50 \text{ pA (TYP.)}$
- Slew Rate  $15 \text{ V}/\mu\text{s (TYP.)}$
- Unity Gain Frequency  $4 \text{ MHz (TYP.)}$
- Input Equivalent Noise Voltage Density  $19 \text{ nV}/\sqrt{\text{Hz}} \text{ (TYP.) (f = 1 kHz)}$
- Stable operation against capacitive load (Capacitive Load at  $10000 \text{ pF}$ ,  $A_v = +1$ )
- Built-In Phase Compensation Circuit
- Built-In Output Short Circuit Protection
- Standard Dual Op-Amp terminal connection (pin compatible)

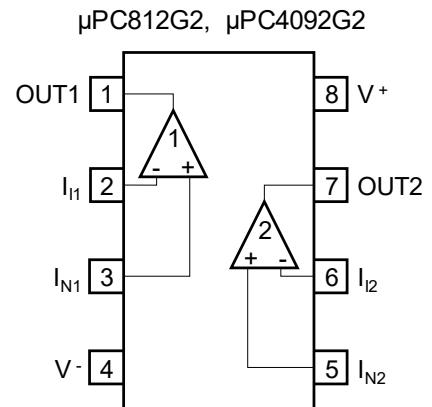
## ORDERING INFORMATION

Ordering Name	Package
μPC812G2-A	8-pin plastic SOP ( 5.72 mm ( 225 ))
μPC4092G2-A	8-pin plastic SOP ( 5.72 mm ( 225 ))

**EQUIVALENT CIRCUIT**



**PIN CONFIGURATION (Top View)**



**ABSOLUTE MAXIMUM RATINGS (TA = 25 °C)**

PARAMETER	SYMBOL	μPC812G2	μPC4092G2	UNIT
Supply Voltage <sup>Note1</sup>	V <sup>+</sup> - V <sup>-</sup>	-0.3 ~ +36		V
Differential Input Voltage	V <sub>ID</sub>	±30		V
Input Voltage <sup>Note2</sup>	V <sub>I</sub>	V <sup>-</sup> -0.3 ~ V <sup>+</sup> +0.3		V
Output Applied Voltage <sup>Note3</sup>	V <sub>O</sub>	V <sup>-</sup> -0.3 ~ V <sup>+</sup> +0.3		V
Total Power Dissipation <sup>Note4</sup>	P <sub>T</sub>	440		mW
Output Short Circuit Duration <sup>Note5</sup>		Indefinite		s
Operating Ambient Temperature	T <sub>A</sub>	-40 ~ +85	-20 ~ +80	°C
Storage Temperature	T <sub>stg</sub>	-55 ~ +125		°C

- [Note]**
- Note that reverse connections of the power supply may damage the ICs.
  - The input terminal must be apply within the input voltage range to avoid deteriorating or damaging the device characteristic. Do not exceed the ratings including during transition state such as ON/OFF, etc. The Op-Amp input voltage must operates within the electrical characteristics range of input common-mode voltage.
  - The output terminal must be apply within the output voltage range to avoid deteriorating or damaging the device characteristic. Do not exceed the ratings including during transition state such as ON/OFF, etc. The Op-Amp output voltage must operates within the electrical characteristics range of maximum output voltage.
  - This is the value at T<sub>A</sub> ≤ +25 °C. De-rate value at -4.4 mW/°C when T<sub>A</sub> > 25 °C
  - Please use the total loss and the de-rating value from Note 4.

**RECOMMENDED OPERATING CONDITIONS**

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Power Supply Voltage	V <sup>±</sup>	±5		±16	V
Load Current	I <sub>o</sub>			±10	mA
Load Capacitance ( When A <sub>v</sub> = +1 )	C <sub>L</sub>			10000 <sup>Note6</sup>	pF

- [Note]**
- This is the value when the feedback resistor (R<sub>f</sub>) = 0 Ω. The higher the R<sub>f</sub> value, the more likely it is to oscillate due to the influence of the input capacitance. So connect a capacitor of about 100 pF in parallel with R<sub>f</sub>

**ELECTRICAL CHARACTERISTICS** ( $T_A = 25\text{ }^\circ\text{C}$ ,  $V^\pm = \pm 15\text{ V}$ )

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Input Offset Voltage	$V_{IO}$		$\pm 1$	$\pm 3$	mV	$R_s \leq 50\ \Omega$
Input Offset Current <sup>Note 7</sup>	$I_{IO}$		$\pm 25$	$\pm 100$	pA	
Input Bias Current <sup>Note 7</sup>	$I_B$		50	200	pA	
Large Signal Voltage Gain	$A_V$	25000	200000			$R_L \geq 2\text{ k}\Omega$ , $V_O = \pm 10\text{ V}$
Circuit Current <sup>Note 8</sup>	$I_{CC}$		5	6.8	mA	$I_O = 0\text{ A}$
Common Mode Rejection Ratio	CMR	70	100		dB	
Supply Voltage Rejection Ratio	SVR	70	100		dB	
Output Voltage Swing	$V_{om}$	$\pm 12$	+14.0 -13.3		V	$R_L \geq 10\text{ k}\Omega$
Output Voltage Swing	$V_{om}$	$\pm 10$	+13.5 -12.8		V	$R_L \geq 2\text{ k}\Omega$
Common Mode Input Voltage Range	$V_{ICM}$	$\pm 11$	+14 -12		V	
Slew Rate	SR		15		V/ $\mu$ s	$A_V = 1$
Unity Gain Frequency	$f_{unity}$		4		MHz	
Input Equivalent Noise Voltage Density	$e_n$		19		nV/ $\sqrt{\text{Hz}}$	$R_s = 100\ \Omega$ , $f = 1\text{ kHz}$
Channel Separation			120		dB	
Input Offset Voltage	$V_{IO}$			$\pm 5$	mV	$R_s \leq 50\ \Omega$ , $T_A = -20 \sim +70\text{ }^\circ\text{C}$
Average $V_{IO}$ Temperature Drift	$\Delta V_{IO}/\Delta T$		$\pm 7$		$\mu\text{V}/^\circ\text{C}$	$T_A = -20 \sim +70\text{ }^\circ\text{C}$
Input Offset Current <sup>Note 7</sup>	$I_{IO}$			$\pm 2$	nA	$T_A = -20 \sim +70\text{ }^\circ\text{C}$
Input Bias Current <sup>Note 7</sup>	$I_B$			7	nA	$T_A = -20 \sim +70\text{ }^\circ\text{C}$

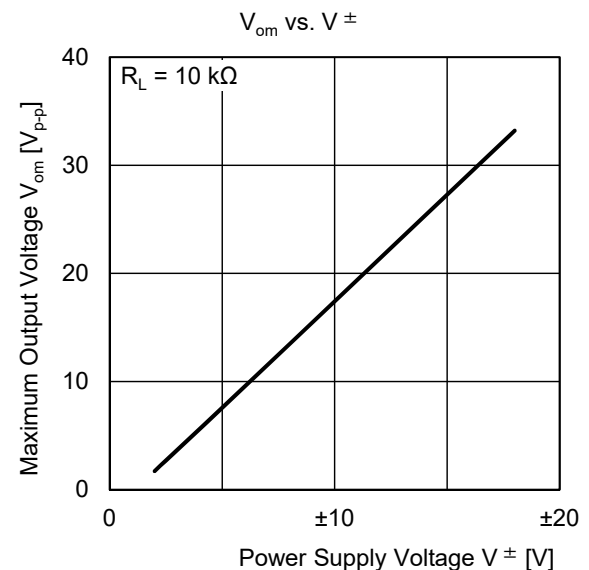
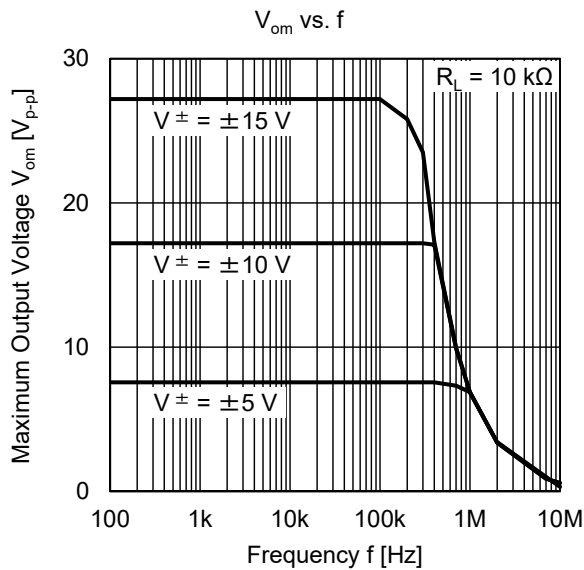
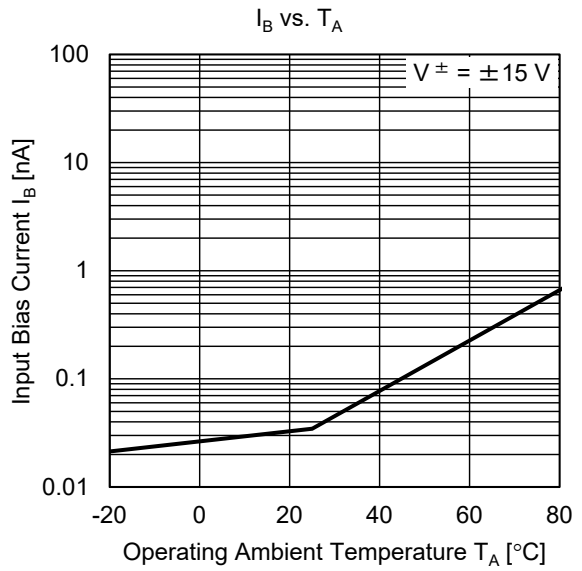
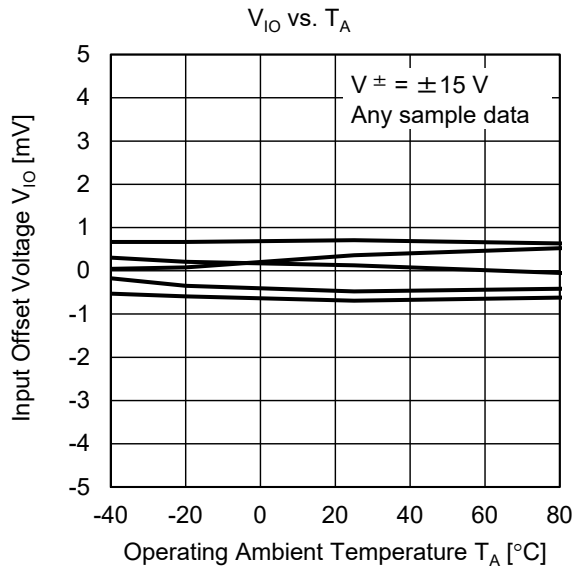
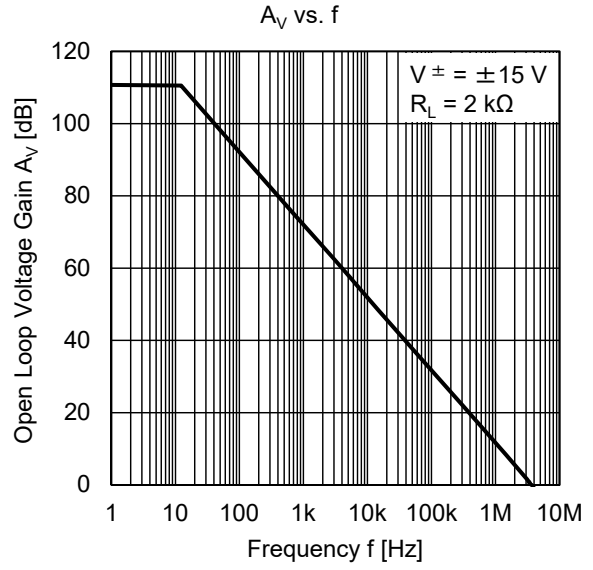
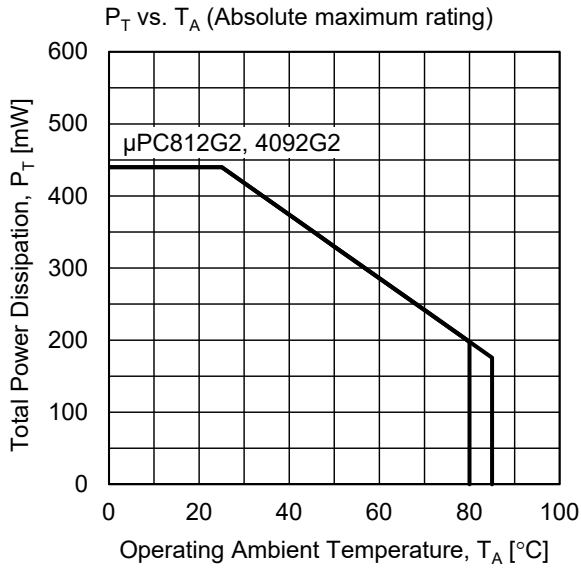
**[Note]** 7. The direction of the input bias current is the same direction that flows into the IC because the first stage is composed of Pch J-FET. When  $T_J = 25\text{ }^\circ\text{C}$  or higher, it increases exponentially with increase in temperature (please see  $I_B - T_A$  characteristics). During measurement, please kindly take care of  $T_J \cong T_A$

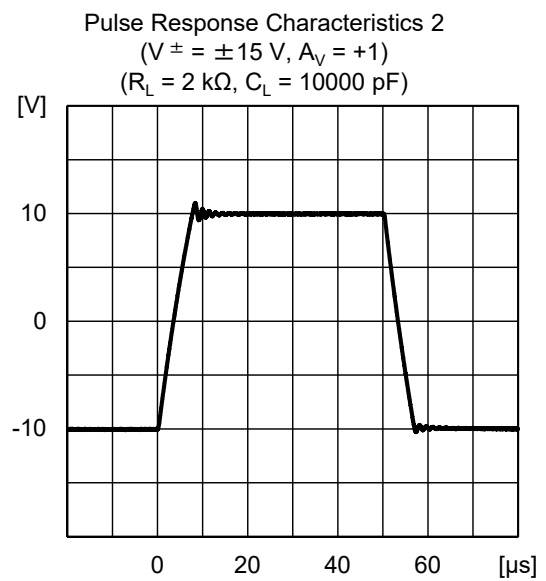
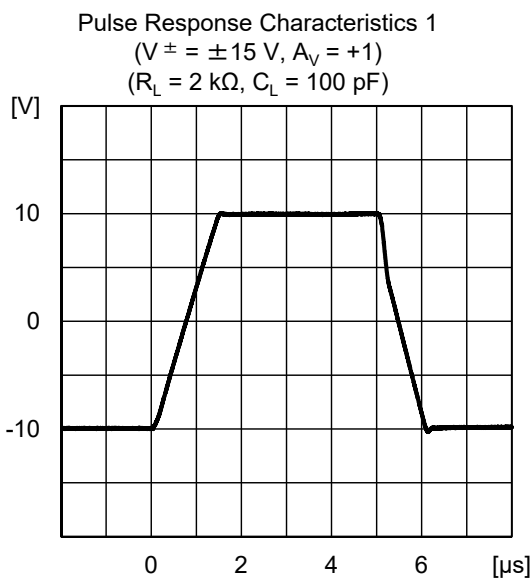
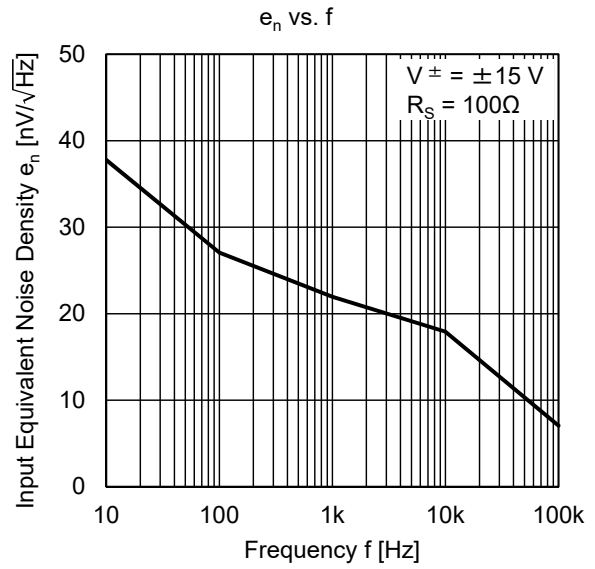
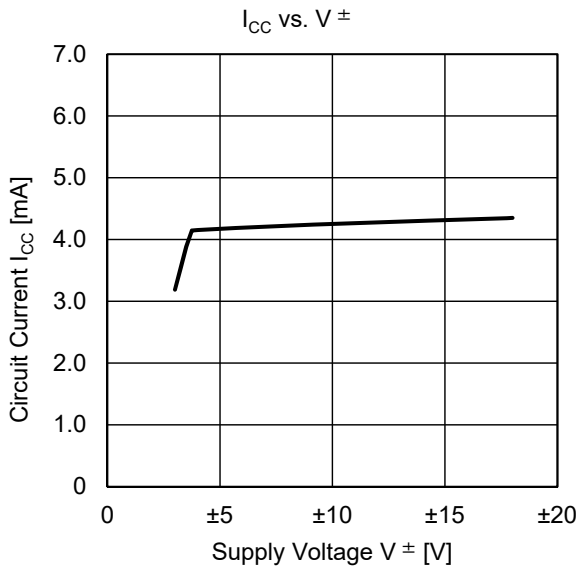
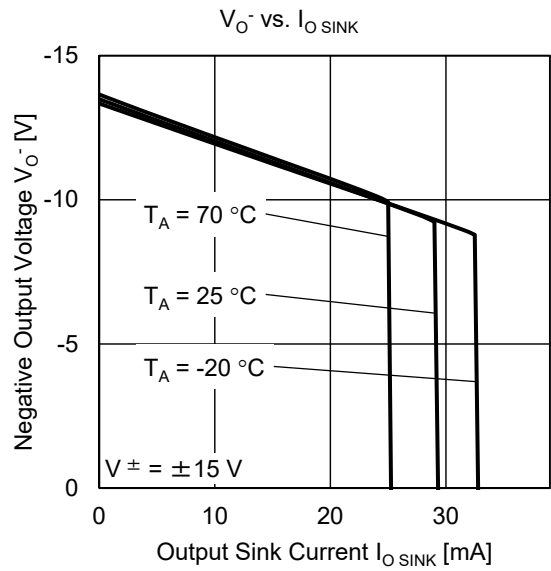
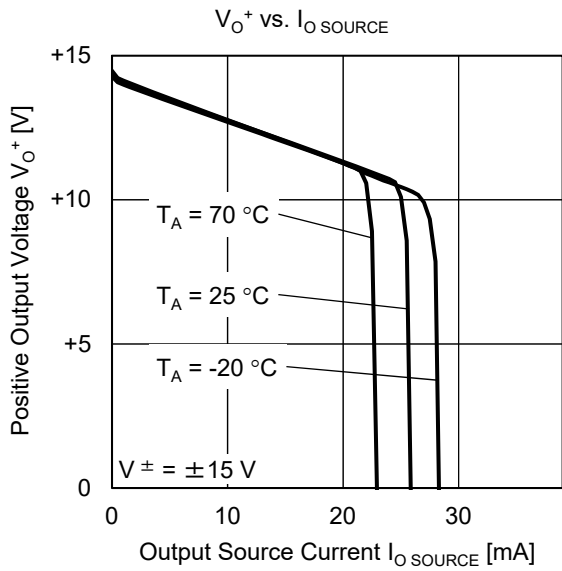
8. It is the current that flows into the internal circuit. This current flows irrespective of the channel usage.

**Caution**

Since μPC812, 4092 have high input impedance characteristics, please be careful of insulation between the terminals on the board

**ELECTRICAL CHARACTERISTICS CURVE (T<sub>A</sub> = 25 °C, TYP.)**

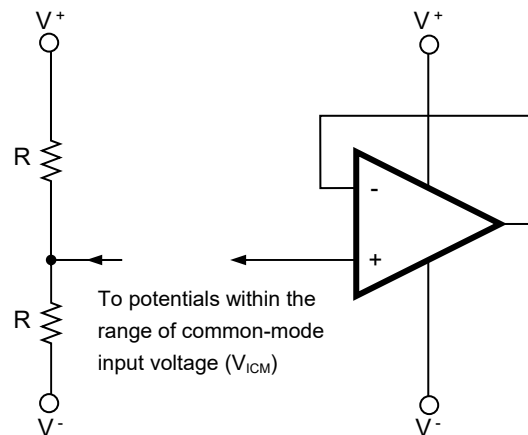




## USE WITH PRECAUTIONS

- Managing unused circuits  
If there is an unused circuit, the following connection is recommended.

### Example of handling unused circuit



Note in this example, an intermediate voltage of V+ and V- is applied.

- Power Supply (Dual Power Supply / Single Power Supply)**

The op amp operates when a predetermine voltage is applied between V+ - V-. Therefore, while it operates from a single power supply (V- = GND), it is not possible to operate the input and output near GND. So please be careful of the common-mode input voltage range and maximum output voltage.

- Ratings of input/output pin voltage**

When the voltage of input/output pin exceeds the absolute maximum rating, the parasitic diode within the IC may conduct, causing characteristics degradation or damage. In addition, if the input pin is lower than V-, or the output pin exceeds the power supply voltage, it is recommended to make a clamping circuit using a diode with low forward voltage (e.g.: Schottky diode) as protection.

- Range of common-mode input voltage**

When the supply voltage does not meet the condition of electrical characteristics, the range of common-mode input voltage is as follows.

$$V_{ICM} \text{ (TYP.)} : V^- + 3 \sim V^+ - 1 \text{ [V]} (T_A = 25^\circ \text{C})$$

During designing, do include some margin by considering characteristics variation, temperature characteristics etc.

- Maximum Output Voltage**

The TYP. value range of the maximum output voltage when the supply voltage does not meet the condition of electrical characteristics is as follows:

$$V_{om+} \text{ (TYP.)} : V^+ - 1 \text{ [V]} (T_A = 25^\circ \text{C}), V_{om-} \text{ (TYP.)} : V^- + 1.7 \text{ [V]} (T_A = 25^\circ \text{C})$$

During designing, do include some margin by considering characteristics variation, temperature characteristics and so on. In addition, also note that the output voltage range (Vom+ - Vom-) will become narrow when the output current increases.

- Handling of ICs**

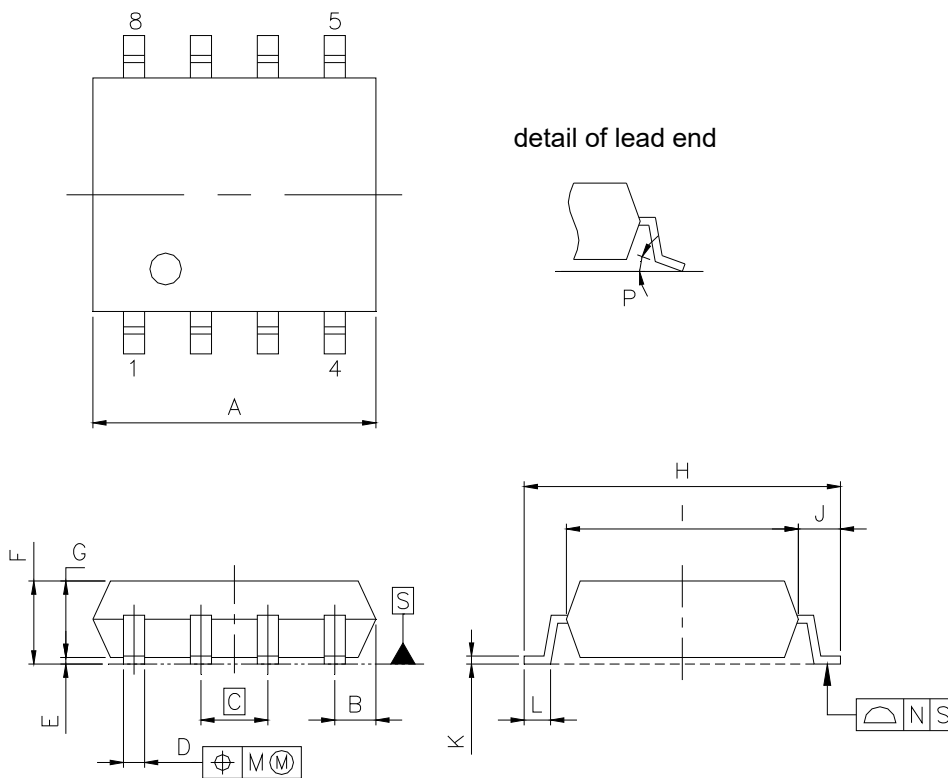
When stress is added to the ICs due to warpage or bending of a board, the characteristic may fluctuates due to piezoelectric (piezo) effect. Therefore, pay attention to warpage or bending of a board.

### PACKAGE DRAWINGS

#### 8-PIN PLASTIC SOP

JEITA Package code	RENESAS code	Previous code	MASS (TYP.) [g]
P-SOP8-0225-1.27	PRSP0008DL-A	S8GM-50-225B	0.08

Unit : mm



**NOTE**

Each lead centerline is located within 0.12 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	5.2 <sup>+0.17</sup> <sub>-0.20</sub>
B	0.78 MAX
C	1.27 (T.P)
D	0.42 <sup>+0.08</sup> <sub>-0.07</sub>
E	0.1 ±0.1
F	1.59 ±0.21
G	1.49
H	6.5 ±0.3
I	4.4 ±0.15
J	1.1 ±0.2
K	0.17 <sup>+0.08</sup> <sub>-0.07</sub>
L	0.6 ±0.2
M	0.12
N	0.10
P	3° <sup>+7°</sup> <sub>-3°</sub>

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