To our customers,

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April 1st, 2010
Renesas Electronics Corporation

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MOS INTEGRATED CIRCUIT

Phase-out/Discontinued

μPD161641

240-OUTPUT TFT-LCD GATE DRIVER

DESCRIPTION

The μPD161641 is a TFT-LCD gate driver. Because this gate driver has a level shift circuit for logic input, it can output a high gate scanning voltage in response to a CMOS-level input.

FEATURES

- High breakdown voltage output (V_T-V_B = 37 V MAX.)
- 3.0 V CMOS level input
- Number of output: 240

★ ORDERING INFORMATION

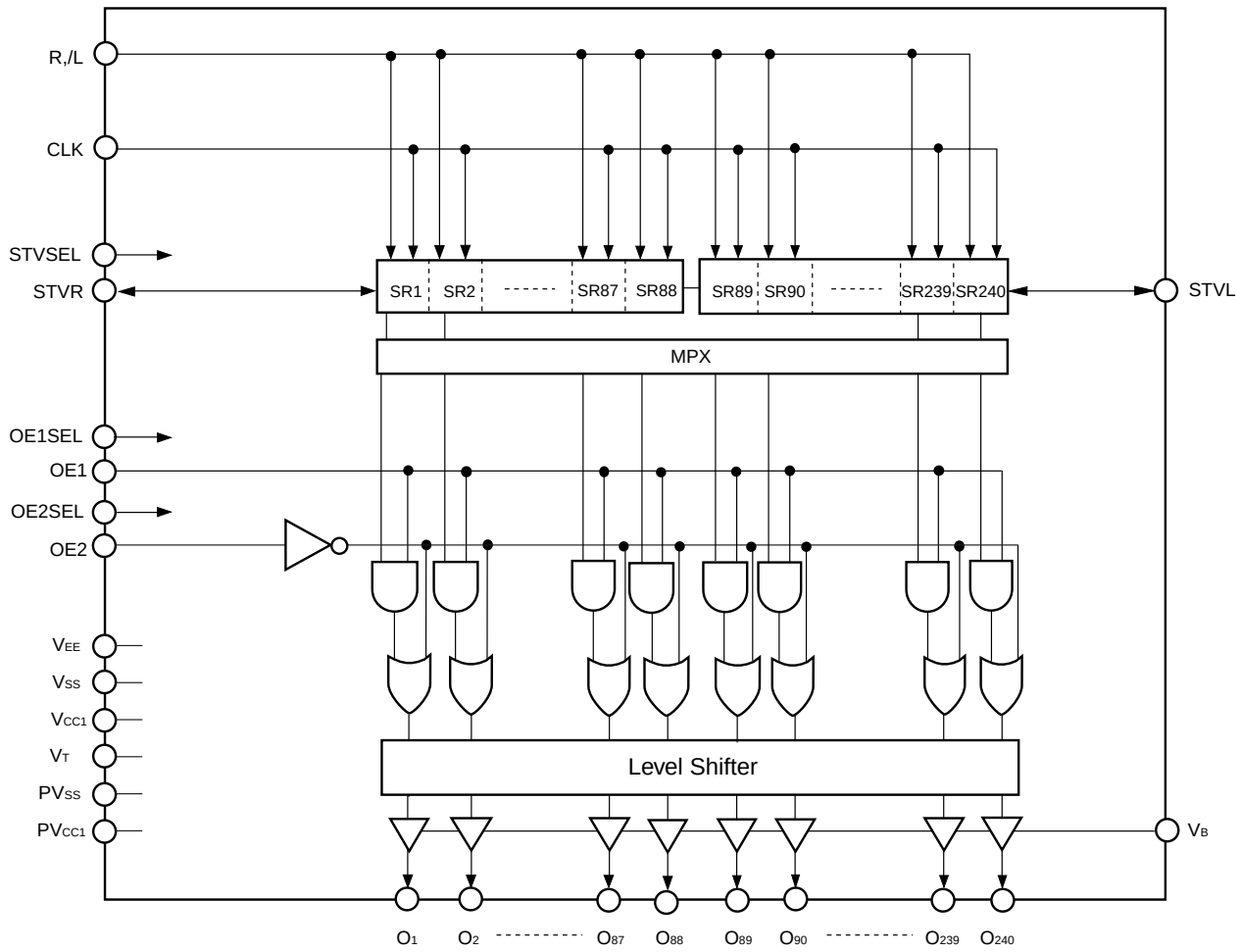
Part number	Package
μPD161641N-xxx	TCP (TAB package)
μPD161641P	Chip

Remark Purchasing the above chip entails the exchange of documents such as a separate memorandum or product quality, so please contact one of our sales representatives.

Document No. S15678EJ1V0DS00 (1st edition)
Date Published July 2002 NS CP(K)
Printed in Japan

The mark ★ shows major revised points.

1. BLOCK DIAGRAM



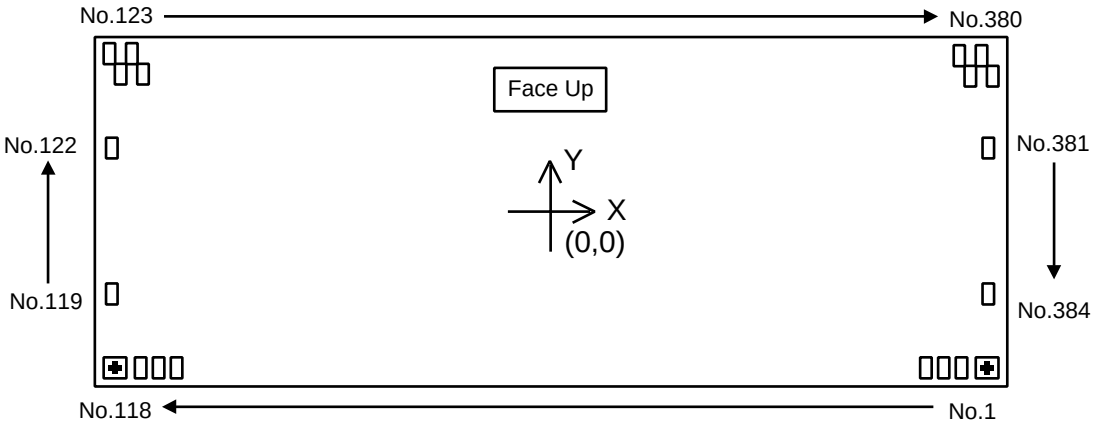
Remark /xxx indicates active low signal.

2. PIN CONFIGURATION (Pad Layout)

Chip size: 9.4 x 3.5 mm^2

Bump size: INPUT (include input side dummy and short-side dummy): 49 x 85 μm^2

OUTPUT (include output side dummy): 35 x 94 μm^2



Alignment Mark

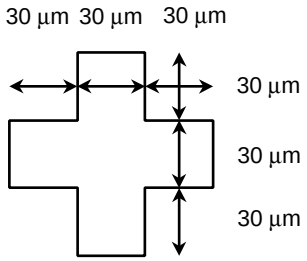


Table 2 1. Pad Layout (1/4)

Gate Inputs 75 μm pich			
Pad No.	Pad Name	X [mm]	Y [mm]
-	Alignment Mark	4.5650	-1.6145
1	DUMMY	4.3875	-1.6145
2	DUMMY	4.3125	-1.6145
3	DUMMY	4.2375	-1.6145
4	DUMMY	4.1625	-1.6145
5	DUMMY	4.0875	-1.6145
6	DUMMY	4.0125	-1.6145
7	DUMMY	3.9375	-1.6145
8	DUMMY	3.8625	-1.6145
9	DUMMY	3.7875	-1.6145
10	DUMMY	3.7125	-1.6145
11	DUMMY	3.6375	-1.6145
12	DUMMY	3.5625	-1.6145
13	DUMMY	3.4875	-1.6145
14	DUMMY	3.4125	-1.6145
15	DUMMY	3.3375	-1.6145
16	DUMMY	3.2625	-1.6145
17	DUMMY	3.1875	-1.6145
18	DUMMY	3.1125	-1.6145
19	PVCC1	3.0375	-1.6145
20	OE1SEL	2.9625	-1.6145
21	OE1SEL	2.8875	-1.6145
22	OE1SEL	2.8125	-1.6145
23	OE1SEL	2.7375	-1.6145
24	OE1SEL	2.6625	-1.6145
25	PVSS	2.5875	-1.6145
26	OE2SEL	2.5125	-1.6145
27	OE2SEL	2.4375	-1.6145
28	OE2SEL	2.3625	-1.6145
29	OE2SEL	2.2875	-1.6145
30	OE2SEL	2.2125	-1.6145
31	DUMMY	2.1375	-1.6145
32	PVCC1	2.0625	-1.6145
33	STVSEL	1.9875	-1.6145
34	STVSEL	1.9125	-1.6145
35	STVSEL	1.8375	-1.6145
36	STVSEL	1.7625	-1.6145
37	STVSEL	1.6875	-1.6145
38	PVSS	1.6125	-1.6145
39	R,/L	1.5375	-1.6145
40	R,/L	1.4625	-1.6145
41	R,/L	1.3875	-1.6145
42	R,/L	1.3125	-1.6145
43	R,/L	1.2375	-1.6145
44	PVCC1	1.1625	-1.6145
45	DUMMY	1.0875	-1.6145
46	VT	1.0125	-1.6145
47	VT	0.9375	-1.6145
48	VT	0.8625	-1.6145
49	VT	0.7875	-1.6145
50	VT	0.7125	-1.6145
51	DUMMY	0.6375	-1.6145
52	DUMMY	0.5625	-1.6145
53	VCC1	0.4875	-1.6145
54	VCC1	0.4125	-1.6145
55	VCC1	0.3375	-1.6145
56	VCC1	0.2625	-1.6145
57	VCC1	0.1875	-1.6145
58	DUMMY	0.1125	-1.6145
59	DUMMY	0.0375	-1.6145
60	DUMMY	-0.0375	-1.6145
61	VSS	-0.1125	-1.6145
62	VSS	-0.1875	-1.6145
63	VSS	-0.2625	-1.6145
64	VSS	-0.3375	-1.6145
65	VSS	-0.4125	-1.6145

Gate Inputs 75 μm pich			
Pad No.	Pad Name	X [mm]	Y [mm]
66	DUMMY	-0.4875	-1.6145
67	DUMMY	-0.5625	-1.6145
68	DUMMY	-0.6375	-1.6145
69	DUMMY	-0.7125	-1.6145
70	VEE	-0.7875	-1.6145
71	VEE	-0.8625	-1.6145
72	VEE	-0.9375	-1.6145
73	VEE	-1.0125	-1.6145
74	VEE	-1.0875	-1.6145
75	DUMMY	-1.1625	-1.6145
76	DUMMY	-1.2375	-1.6145
77	VB	-1.3125	-1.6145
78	VB	-1.3875	-1.6145
79	VB	-1.4625	-1.6145
80	VB	-1.5375	-1.6145
81	VB	-1.6125	-1.6145
82	DUMMY	-1.6875	-1.6145
83	DUMMY	-1.7625	-1.6145
84	DUMMY	-1.8375	-1.6145
85	STVR	-1.9125	-1.6145
86	STVR	-1.9875	-1.6145
87	STVR	-2.0625	-1.6145
88	STVR	-2.1375	-1.6145
89	STVR	-2.2125	-1.6145
90	DUMMY	-2.2875	-1.6145
91	STVL	-2.3625	-1.6145
92	STVL	-2.4375	-1.6145
93	STVL	-2.5125	-1.6145
94	STVL	-2.5875	-1.6145
95	STVL	-2.6625	-1.6145
96	DUMMY	-2.7375	-1.6145
97	CLK	-2.8125	-1.6145
98	CLK	-2.8875	-1.6145
99	CLK	-2.9625	-1.6145
100	CLK	-3.0375	-1.6145
101	CLK	-3.1125	-1.6145
102	DUMMY	-3.1875	-1.6145
103	OE1	-3.2625	-1.6145
104	OE1	-3.3375	-1.6145
105	OE1	-3.4125	-1.6145
106	OE1	-3.4875	-1.6145
107	OE1	-3.5625	-1.6145
108	DUMMY	-3.6375	-1.6145
109	OE2	-3.7125	-1.6145
110	OE2	-3.7875	-1.6145
111	OE2	-3.8625	-1.6145
112	OE2	-3.9375	-1.6145
113	OE2	-4.0125	-1.6145
114	DUMMY	-4.0875	-1.6145
115	DUMMY	-4.1625	-1.6145
116	DUMMY	-4.2375	-1.6145
117	DUMMY	-4.3125	-1.6145
118	DUMMY	-4.3875	-1.6145
–	Alignment Mark	-4.5650	-1.6145

Table 2–1. Pad Layout (2/4)

Gate Outputs 35 μm pich			
Pad No.	Pad Name	X [mm]	Y [mm]
123	DUMMY	-4.4975	1.6100
124	DUMMY	-4.4625	1.4800
125	DUMMY	-4.4275	1.6100
126	DUMMY	-4.3925	1.4800
127	DUMMY	-4.3575	1.6100
128	DUMMY	-4.3225	1.4800
129	DUMMY	-4.2875	1.6100
130	DUMMY	-4.2525	1.4800
131	DUMMY	-4.2175	1.6100
132	240	-4.1825	1.4800
133	239	-4.1475	1.6100
134	238	-4.1125	1.4800
135	237	-4.0775	1.6100
136	236	-4.0425	1.4800
137	235	-4.0075	1.6100
138	234	-3.9725	1.4800
139	233	-3.9375	1.6100
140	232	-3.9025	1.4800
141	231	-3.8675	1.6100
142	230	-3.8325	1.4800
143	229	-3.7975	1.6100
144	228	-3.7625	1.4800
145	227	-3.7275	1.6100
146	226	-3.6925	1.4800
147	225	-3.6575	1.6100
148	224	-3.6225	1.4800
149	223	-3.5875	1.6100
150	222	-3.5525	1.4800
151	221	-3.5175	1.6100
152	220	-3.4825	1.4800
153	219	-3.4475	1.6100
154	218	-3.4125	1.4800
155	217	-3.3775	1.6100
156	216	-3.3425	1.4800
157	215	-3.3075	1.6100
158	214	-3.2725	1.4800
159	213	-3.2375	1.6100
160	212	-3.2025	1.4800
161	211	-3.1675	1.6100
162	210	-3.1325	1.4800
163	209	-3.0975	1.6100
164	208	-3.0625	1.4800
165	207	-3.0275	1.6100
166	206	-2.9925	1.4800
167	205	-2.9575	1.6100
168	204	-2.9225	1.4800
169	203	-2.8875	1.6100
170	202	-2.8525	1.4800
171	201	-2.8175	1.6100
172	200	-2.7825	1.4800
173	199	-2.7475	1.6100
174	198	-2.7125	1.4800
175	197	-2.6775	1.6100
176	196	-2.6425	1.4800
177	195	-2.6075	1.6100
178	194	-2.5725	1.4800
179	193	-2.5375	1.6100
180	192	-2.5025	1.4800
181	191	-2.4675	1.6100
182	190	-2.4325	1.4800
183	189	-2.3975	1.6100
184	188	-2.3625	1.4800
185	187	-2.3275	1.6100
186	186	-2.2925	1.4800
187	185	-2.2575	1.6100
188	184	-2.2225	1.4800

Gate Outputs 35 μm pich			
Pad No.	Pad Name	X [mm]	Y [mm]
189	183	-2.1875	1.6100
190	182	-2.1525	1.4800
191	181	-2.1175	1.6100
192	180	-2.0825	1.4800
193	179	-2.0475	1.6100
194	178	-2.0125	1.4800
195	177	-1.9775	1.6100
196	176	-1.9425	1.4800
197	175	-1.9075	1.6100
198	174	-1.8725	1.4800
199	173	-1.8375	1.6100
200	172	-1.8025	1.4800
201	171	-1.7675	1.6100
202	170	-1.7325	1.4800
203	169	-1.6975	1.6100
204	168	-1.6625	1.4800
205	167	-1.6275	1.6100
206	166	-1.5925	1.4800
207	165	-1.5575	1.6100
208	164	-1.5225	1.4800
209	163	-1.4875	1.6100
210	162	-1.4525	1.4800
211	161	-1.4175	1.6100
212	160	-1.3825	1.4800
213	159	-1.3475	1.6100
214	158	-1.3125	1.4800
215	157	-1.2775	1.6100
216	156	-1.2425	1.4800
217	155	-1.2075	1.6100
218	154	-1.1725	1.4800
219	153	-1.1375	1.6100
220	152	-1.1025	1.4800
221	151	-1.0675	1.6100
222	150	-1.0325	1.4800
223	149	-0.9975	1.6100
224	148	-0.9625	1.4800
225	147	-0.9275	1.6100
226	146	-0.8925	1.4800
227	145	-0.8575	1.6100
228	144	-0.8225	1.4800
229	143	-0.7875	1.6100
230	142	-0.7525	1.4800
231	141	-0.7175	1.6100
232	140	-0.6825	1.4800
233	139	-0.6475	1.6100
234	138	-0.6125	1.4800
235	137	-0.5775	1.6100
236	136	-0.5425	1.4800
237	135	-0.5075	1.6100
238	134	-0.4725	1.4800
239	133	-0.4375	1.6100
240	132	-0.4025	1.4800
241	131	-0.3675	1.6100
242	130	-0.3325	1.4800
243	129	-0.2975	1.6100
244	128	-0.2625	1.4800
245	127	-0.2275	1.6100
246	126	-0.1925	1.4800
247	125	-0.1575	1.6100
248	124	-0.1225	1.4800
249	123	-0.0875	1.6100
250	122	-0.0525	1.4800
251	121	-0.0175	1.6100
252	DUMMY	0.0175	1.4800
253	DUMMY	0.0525	1.6100
254	DUMMY	0.0875	1.4800

Table 2–1. Pad Layout (3/4)

Gate Outputs 35 μm pich			
Pad No.	Pad Name	X [mm]	Y [mm]
255	DUMMY	0.1225	1.6100
256	DUMMY	0.1575	1.4800
257	DUMMY	0.1925	1.6100
258	120	0.2275	1.4800
259	119	0.2625	1.6100
260	118	0.2975	1.4800
261	117	0.3325	1.6100
262	116	0.3675	1.4800
263	115	0.4025	1.6100
264	114	0.4375	1.4800
265	113	0.4725	1.6100
266	112	0.5075	1.4800
267	111	0.5425	1.6100
268	110	0.5775	1.4800
269	109	0.6125	1.6100
270	108	0.6475	1.4800
271	107	0.6825	1.6100
272	106	0.7175	1.4800
273	105	0.7525	1.6100
274	104	0.7875	1.4800
275	103	0.8225	1.6100
276	102	0.8575	1.4800
277	101	0.8925	1.6100
278	100	0.9275	1.4800
279	99	0.9625	1.6100
280	98	0.9975	1.4800
281	97	1.0325	1.6100
282	96	1.0675	1.4800
283	95	1.1025	1.6100
284	94	1.1375	1.4800
285	93	1.1725	1.6100
286	92	1.2075	1.4800
287	91	1.2425	1.6100
288	90	1.2775	1.4800
289	89	1.3125	1.6100
290	88	1.3475	1.4800
291	87	1.3825	1.6100
292	86	1.4175	1.4800
293	85	1.4525	1.6100
294	84	1.4875	1.4800
295	83	1.5225	1.6100
296	82	1.5575	1.4800
297	81	1.5925	1.6100
298	80	1.6275	1.4800
299	79	1.6625	1.6100
300	78	1.6975	1.4800
301	77	1.7325	1.6100
302	76	1.7675	1.4800
303	75	1.8025	1.6100
304	74	1.8375	1.4800
305	73	1.8725	1.6100
306	72	1.9075	1.4800
307	71	1.9425	1.6100
308	70	1.9775	1.4800
309	69	2.0125	1.6100
310	68	2.0475	1.4800
311	67	2.0825	1.6100
312	66	2.1175	1.4800
313	65	2.1525	1.6100
314	64	2.1875	1.4800
315	63	2.2225	1.6100
316	62	2.2575	1.4800
317	61	2.2925	1.6100
318	60	2.3275	1.4800
319	59	2.3625	1.6100

Gate Outputs 35 μm pich			
Pad No.	Pad Name	X [mm]	Y [mm]
320	58	2.3975	1.4800
321	57	2.4325	1.6100
322	56	2.4675	1.4800
323	55	2.5025	1.6100
324	54	2.5375	1.4800
325	53	2.5725	1.6100
326	52	2.6075	1.4800
327	51	2.6425	1.6100
328	50	2.6775	1.4800
329	49	2.7125	1.6100
330	48	2.7475	1.4800
331	47	2.7825	1.6100
332	46	2.8175	1.4800
333	45	2.8525	1.6100
334	44	2.8875	1.4800
335	43	2.9225	1.6100
336	42	2.9575	1.4800
337	41	2.9925	1.6100
338	40	3.0275	1.4800
339	39	3.0625	1.6100
340	38	3.0975	1.4800
341	37	3.1325	1.6100
342	36	3.1675	1.4800
343	35	3.2025	1.6100
344	34	3.2375	1.4800
345	33	3.2725	1.6100
346	32	3.3075	1.4800
347	31	3.3425	1.6100
348	30	3.3775	1.4800
349	29	3.4125	1.6100
350	28	3.4475	1.4800
351	27	3.4825	1.6100
352	26	3.5175	1.4800
353	25	3.5525	1.6100
354	24	3.5875	1.4800
355	23	3.6225	1.6100
356	22	3.6575	1.4800
357	21	3.6925	1.6100
358	20	3.7275	1.4800
359	19	3.7625	1.6100
360	18	3.7975	1.4800
361	17	3.8325	1.6100
362	16	3.8675	1.4800
363	15	3.9025	1.6100
364	14	3.9375	1.4800
365	13	3.9725	1.6100
366	12	4.0075	1.4800
367	11	4.0425	1.6100
368	10	4.0775	1.4800
369	9	4.1125	1.6100
370	8	4.1475	1.4800
371	7	4.1825	1.6100
372	6	4.2175	1.4800
373	5	4.2525	1.6100
374	4	4.2875	1.4800
375	3	4.3225	1.6100
376	2	4.3575	1.4800
377	1	4.3925	1.6100
378	DUMMY	4.4275	1.4800
379	DUMMY	4.4625	1.6100
380	DUMMY	4.4975	1.4800

Table 2–1. Pad Layout (4/4)

Gate Right 75 μm pich			
Pad No.	Pad Name	X [mm]	Y [mm]
381	DUMMY	4.5825	1.1250
382	DUMMY	4.5825	0.3750
383	DUMMY	4.5825	-0.3750
384	DUMMY	4.5825	-1.1250

Gate Left 75 μm pich			
Pad No.	Pad Name	X [mm]	Y [mm]
119	DUMMY	-4.5825	-1.1250
120	DUMMY	-4.5825	-0.3750
121	DUMMY	-4.5825	0.3750
122	DUMMY	-4.5825	1.1250

3. PIN FUNCTIONS

(1/2)

Symbol	Pin Name	Pad No.	I/O	Function
O_1 to O_{240}	Driver output	132 to 251, 258 to 377	Output	Scan signal output pins that drive the gate electrode of a TFT-LCD. The status of each output pin changes in synchronization with the rising edge of shift clock. The output voltage of the driver is V_T-V_B.
STVR, STVL	Start pulse input/output	85 to 89, 91 to 95	I/O	Input/output pin of the internal shift register. Read of start pulse signal is set at rising edge of shift clock, and outputs a scanning signal from a driver output pin. In addition, the effective level of a STVR/STVL pin is determined by setup of STVSEL pin. Moreover, an input/output level is V_{CC1}-V_{SS} (logic level). STVSEL = L: Start pulse is set to low level by the 240th falling edge of shift clock, and is set to a high level by the 241st falling edge.
STVSEL	Start pulse input effective level selection	33 to 37	Input	The effective level of the start pulse signal inputted into STVR/STVL is selected. STVSEL = L: Low level STVSEL = H: High level
CLK	Shift clock input	97 to 101	Input	Shift clock input for the internal shift register. The contents of internal shift register is shifted at the rising edge of CLK. Connect to GCLK pin of source driver.
R,/L	Shift direction switching input	39 to 43	Input	Shift direction switching input pin of the internal shift register. R,/L = H (right shift): STVR → O_1 → O_2 ··· O_{239} → O_{240} → STVL R,/L = L (left shift): STVL → O_{240} → O_{239} ··· O_2 → O_1 → STVR
OE1	Enable input	103 to 107	Input	Input of the level selected by OE1SEL fixes a driver output to a low level (input of a low level fixes driver output to low level at the time of OE1SEL = L). However, shift register is not cleared. Moreover, output enable operation is asynchronous on a clock. Connect with GOE1 pin of sauce driver.
OE1SEL	OE1 effective level selection	20 to 24	Input	This pin selects effective level of OE1 pin. OE1SEL = L: Low level OE1SEL = H: High level
OE2	Enable input	109 to 113	Input	Input of the level selected by OE2SEL fixes a driver output to a high level (input of a low level fixes driver output to high level at the time of OE2SEL = L). However, shift register is not cleared. Moreover, output enable operation is asynchronous on a clock. Connect with GOE2 pin of sauce driver.
OE2SEL	OE2 effective level selection	26 to 30	Input	This pin selects effective level of OE2 pin. OE2SEL = L: Low level OE2SEL = H: High level

(2/2)

Symbol	Name	Pad No.	I/O	Function
V_T	Positive power supply for driver	48 to 50	–	Positive power supply for level shifter and output buffer. Positive power supply for Liquid crystal.
V_{EE}	Negative power supply for logic	70 to 74	–	Negative power supply for level shifter.
V_B	Negative power supply for driver	77 to 81	–	Negative power supply for output buffer. Negative power supply for Liquid crystal.
V_{CC1}	Positive power supply for logic	53 to 57	–	Positive power supply for logic circuit.
V_{SS}	Ground	61 to 65	–	Connect to the system ground.
PV_{CC1}	Pull-up power supply	19, 32, 44	–	Pull-up power supply for mode setting pins (R,/L, STVSEL, OE1SEL, OE2SEL).
PV_{SS}	Pull-down power supply	25, 38	–	Pull-down power supply for mode setting pins (R,/L, STVSEL, OE1SEL, OE2SEL).

4. MODE DESCRIPTION

Output Mode Selection

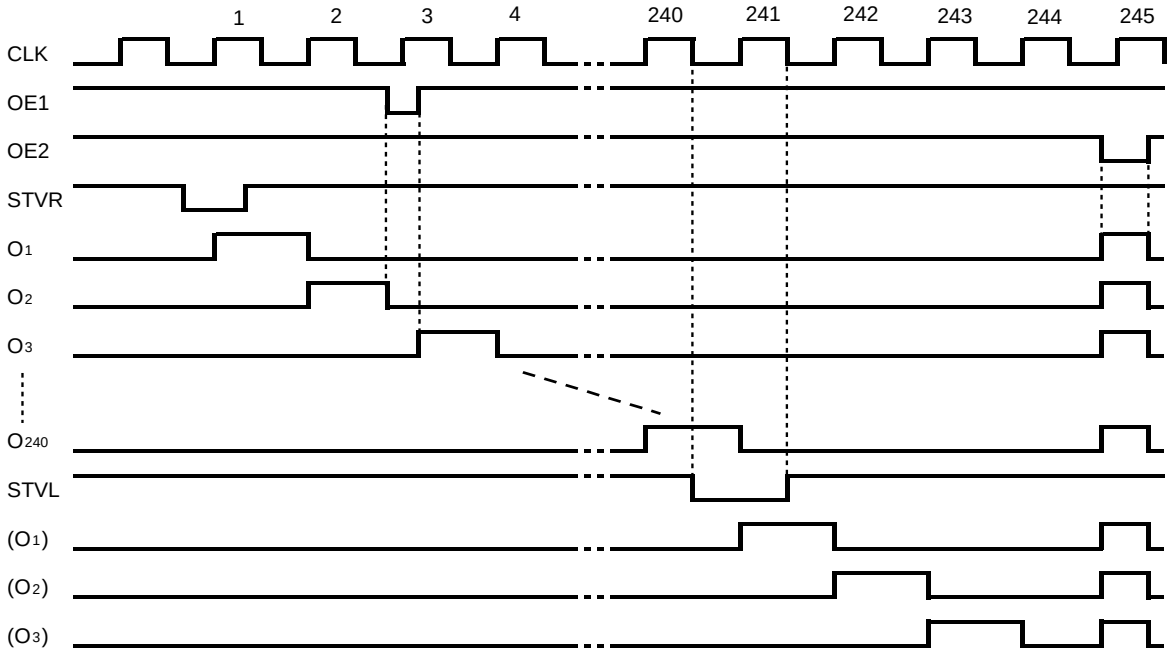
R,/L	STVR	STVL	Scan Direction
H	Input	Output	1→240
L	Output	Input	240→1

Remark H: V_{CC1}, L: V_{SS}

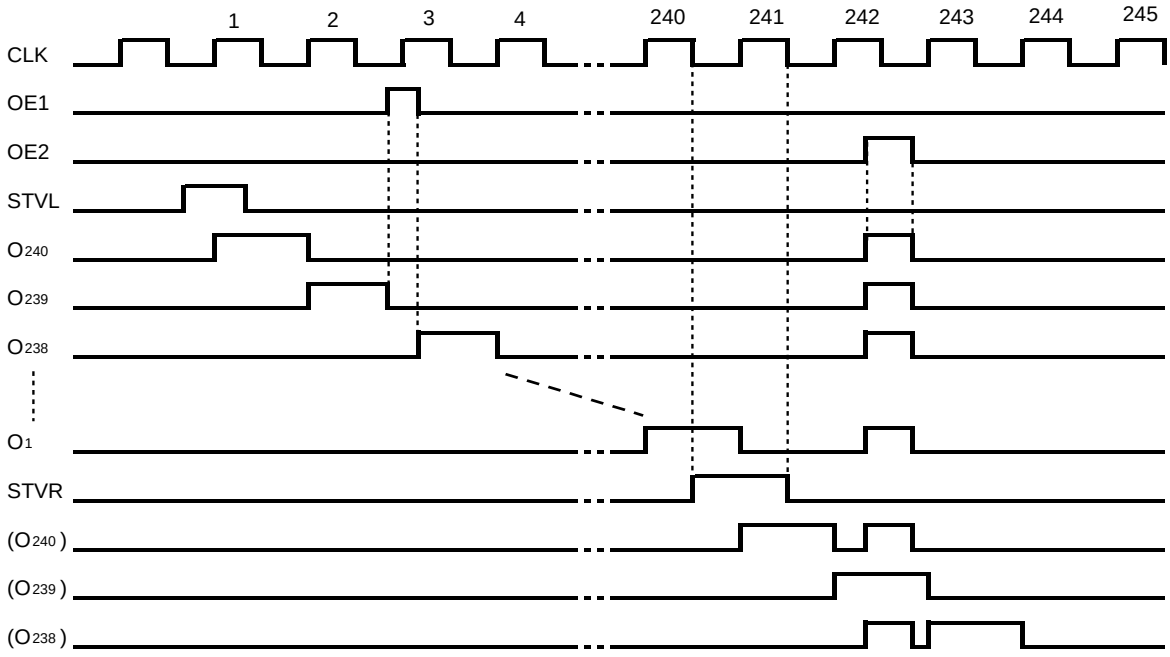
5. TIMING CHART

The timing chart in each conditions is shown as follows.

R,/L = H, STVSEL = L, OE1SEL = L, OE2SEL = L



R,/L = L, STVSEL = H, OE1SEL = H, OE2SEL = H



6. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C, V_{SS} = 0 V)

Parameter	Symbol	Rating	Unit
Supply Voltage	V_T	–0.5 to +23	V
Supply Voltage	V_{CC1}	–0.5 to +7.0	V
Supply Voltage	V_T-V_{EE}	–0.5 to +40	V
Supply Voltage	V_{EE}	V_T–38 to +0.5	V
Supply Voltage	V_B	V_{EE}+0.5 to +0.5	V
Input Voltage Note	V_I	–0.5 to V_{CC1}+0.5	V
Operating Ambient Temperature	T_A	–40 to +85	°C
Storage Temperature	T_{stg}	–55 to +150	°C

Note R,/L, CLK, STVR, STVL, OE1, OE2, STVSEL, OE1SEL, OE2SEL

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Recommended Operating Conditions (T_A = –40 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply Voltage	V_T	8.5	15	20.5	V
Supply Voltage	V_{EE}	–16.5	–15	–13.5	V
Supply Voltage	V_B	V_{EE}+1		V_{EE}+12	V
Supply Voltage	V_T-V_{EE}	22		37	V
Supply Voltage	V_{CC1}	2.5	2.7	3.6	V
Input Voltage Note	V_I	0		V_{CC1}	V

Note R,/L, CLK, STVR, STVL, OE1, OE2, STVSEL, OE1SEL, OE2SEL

Electrical Characteristics (T_A = –40 to +85°C, V_{CC1} = 2.5 to 3.6 V, V_T = 15 V, V_{EE} = –15 V, V_B = –11 V, V_{SS} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
High Level Input Voltage	V_{IH1}	R,/L, CLK, STVR, STVL, OE1, OE2, STVSEL , OE1SEL , OE2SEL	0.8 V_{CC1}		V_{CC1}	V
Low Level Input Voltage	V_{IL1}		0		0.2 V_{CC1}	V
High Level Output Voltage	V_{OH}	STVR, STVL, I_{OH} = –40 μA	V_{CC1} – 0.4		V_{CC1}	V
Low Level Output Voltage	V_{OL}	STVR, STVL, I_{OH} = +40 μA	0		0.4	V
Output ON Resistance	R_{ON1}	O_1 to O_{240}			1.0	kΩ
Input Current	I_{I1}	Logic input pin			±1.0	μA
Dynamic Current 1	I_{CC1}	V_{CC1}, **Note**			200	μA
Dynamic Current 2	I_T	V_T, **Note**			100	μA
Dynamic Current 3	I_{EE}	V_{EE}, **Note**			100	μA
Static Current **Note**	I_{SS}	V_{CC1}, V_T in stand-by mode			10	μA

Note f_{CLK} = 45.5 kHz, output no load

Switching Characteristics (T_A = –40 to +85°C, V_{CC1} = 2.5 to 3.6 V, V_T = 15 V, V_{EE} = –15 V, V_B = –11 V, V_{SS} = 0 V)

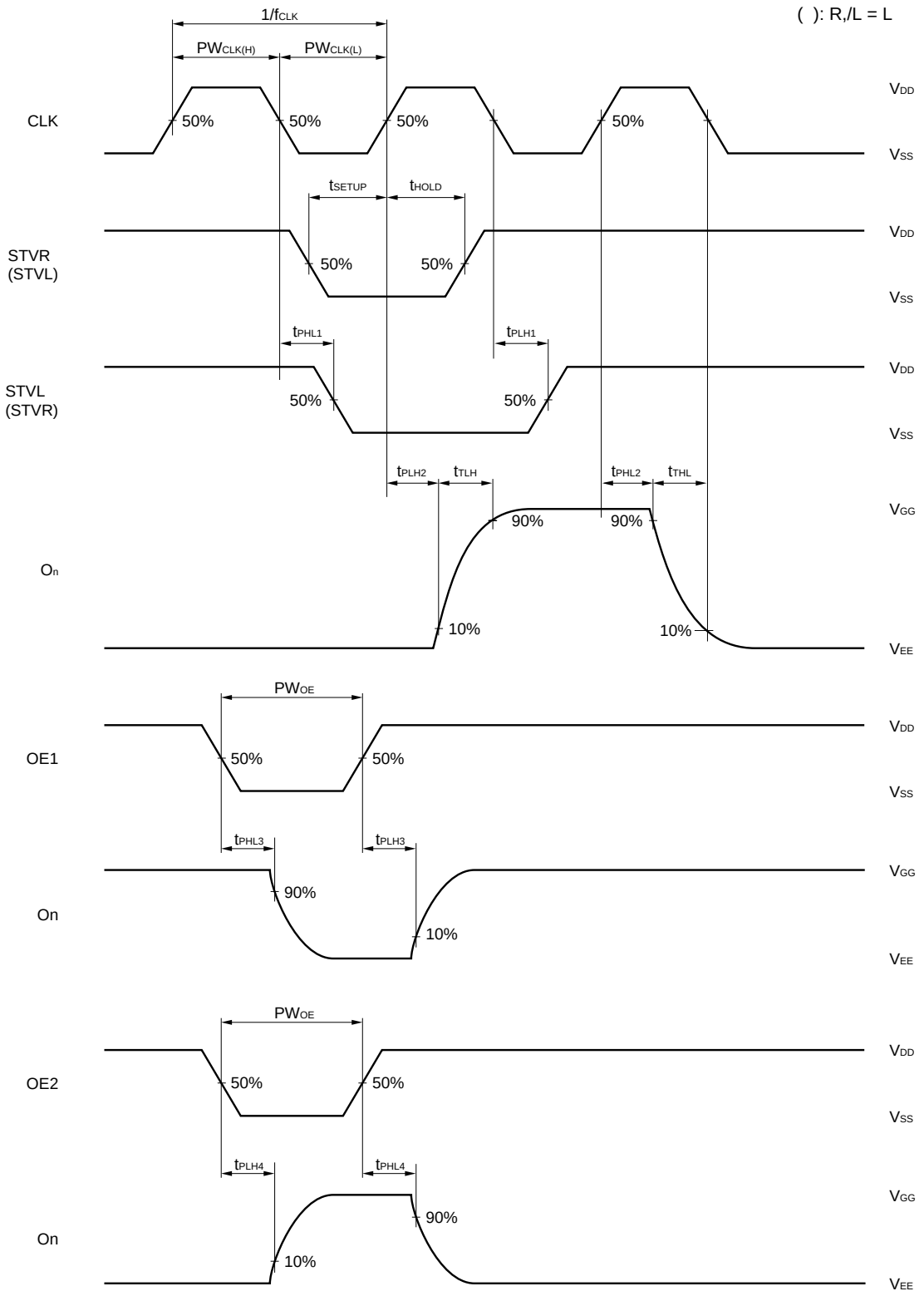
Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Cascade Output Delay Time	t_{PHL1}	C_L = 20 pF,			800	ns
	t_{PLH1}	CLK → STVL (STVR)			800	ns
Driver Output Delay Time 1	t_{PHL2}	C_L = 300 pF,			500	ns
	t_{PLH2}	CLK → O_n			500	ns
Driver Output Delay Time2	t_{PHL3}	C_L = 300 pF,			500	ns
	t_{PLH3}	OE1 → On			500	ns
Driver Output Delay Time 3	t_{PHL4}	C_L = 300 pF,			500	ns
	t_{PLH4}	OE2 → On			500	ns
Output Rise Time	t_{TLH}	C_L = 300 pF			800	ns
Output Fall Time	t_{THL}				800	ns
Input Capacitance	C_I	T_A = 25°C			15	pF
Clock Frequency	f_{CLK}	When connected in cascade			500	kHz

Timing Requirement (T_A = –40 to +85°C, V_{CC1} = 2.5 to 3.6 V, V_T = 15 V, V_{EE} = –15 V, V_B = –11 V, V_{SS} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Clock Pulse High Period	$PW_{CLK(H)}$		500			ns
Clock Pulse Low Period	$PW_{CLK(L)}$		500			ns
Enable Pulse High Period	PW_{OE}	OE1, OE2	1			μs
Data Setup Time	t_{SETUP}	STVR (STVL) ↓ →CLK↑	200			ns
Data Hold Time	t_{HOLD}	CLK↑→STVR (STVL) ↑	200			ns

Remark The rise and fall times of logic input must be t_r = t_f = 20 ns (10 to 90%)

Switching Characteristics Waveform (R,/L = H, STVSEL = L, OE1SEL = L, OE2SEL = L)



[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

★ **Reference Documents**

NEC Semiconductor Device Reliability/Quality Control System (C10983E)

Quality Grades On NEC Semiconductor Devices (C11531E)