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RENESAS

MOS INTEGRATED CIRCUIT

μPD780226, 780228

8-BIT SINGLE-CHIP MICROCONTROLLERS

DESCRIPTION

The μPD780226 and μPD780228 are members of the μPD780228 Subseries of the 78K/0 Series.

The FIP™ (VFD) controller/driver and N-ch open-drain port of the conventional μPD78044H Subseries have been enhanced for the μPD780228 Subseries.

A flash memory version, the μPD78F0228, that can operate within the same power supply voltage range as the mask ROM version, and various development tools are under development.

The details of functions are described in the following user's manuals. Be sure to read them before designing.

μPD780228 Subseries User's Manual : U12012E
78K/0 Series User's Manual Instructions : IEU-1372

FEATURES

- I/O ports: 72 (sixteen N-ch open-drain I/O ports)
- Internal high-capacity ROM and RAM

Item / Part Number	Program memory (ROM)	Data memory		
		Internal high-speed RAM	Internal expanded RAM	FIP display RAM
μPD780226	48 Kbytes	1024 bytes	512 bytes	96 bytes
μPD780228	60 Kbytes			

- Minimum instruction execution time can be changed from high-speed (0.4 μs) to low-speed (6.4 μs)
- FIP controller/driver: 48 display outputs (Universal grid supported)
- 8-bit resolution A/D converter: eight channels
- Serial interface: one channel
- Timer: Four channels
- Power supply voltage: V_{DD} = 4.5 to 5.5 V

APPLICATIONS

Compact-type integrated system components, separate-type system components, tuners, cassette tape decks, compact disc players, audio amplifiers, etc.

ORDERING INFORMATION

Part Number	Package
μPD780226GF-×××-3BA	100-pin plastic QFP (14 × 20 mm)
μPD780228GF-×××-3BA	100-pin plastic QFP (14 × 20 mm)

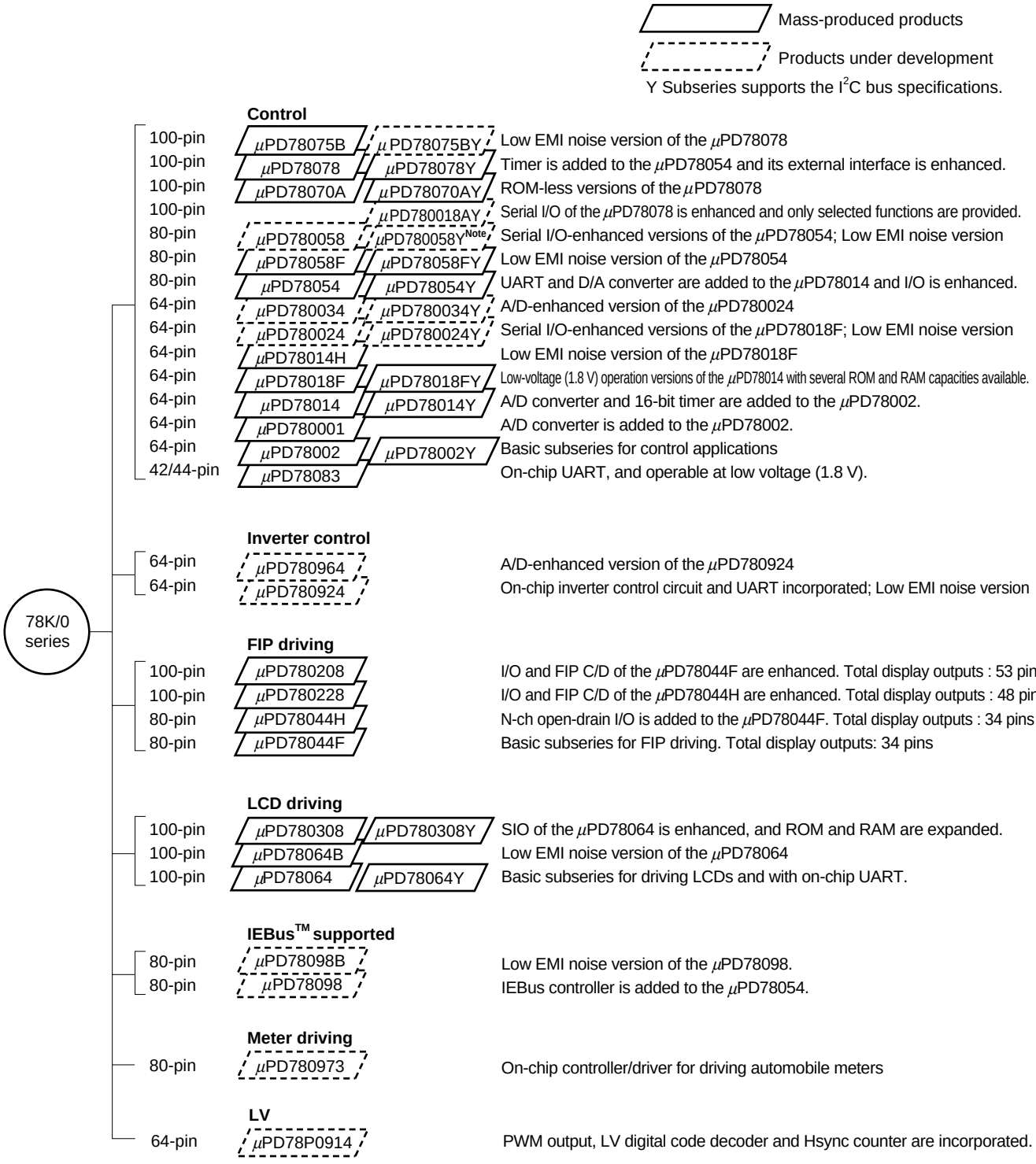
Remark ××× indicates the ROM code suffix.

Document No. U11797EJ1V0DS00 (1st edition)
Date Published July 1997 N
Printed in Japan

The mark ★ shows major revised points.

★ 78K/0 Series Development

The following shows the 78K/0 Series products development. Subseries names are shown inside frames.



Note Under planning

The following table shows the differences among subseries functions.

Subseries name \ Function		ROM capacity	Timer				8-bit A/D	10-bit A/D	8-bit D/A	Serial interface	I/O	V_{DD} MIN. value	External expansion
			8-bit	16-bit	Watch	WDT							
Control	μPD78075B	32K to 40K	4 ch	1 ch	1 ch	1 ch	8 ch	—	2 ch	3 ch (UART: 1 ch)	88	1.8 V	Available
	μPD78078	48K to 60K											
	μPD78070A	—									61	2.7 V	
	μPD780058	24K to 60K	2 ch						2 ch	3 ch (Time division UART: 1 ch)	68	1.8 V	
	μPD78058F	48K to 60K								3 ch (UART: 1 ch)	69	2.7 V	
	μPD78054	16K to 60K										2.0 V	
	μPD780034	8K to 32K					—	8 ch	—	3 ch (UART: 1 ch, Time division 3-wire: 1 ch)	51	1.8 V	
	μPD780024						8 ch	—					
	μPD78014H									2 ch	53		
	μPD78018F	8K to 60K											
	μPD78014	8K to 32K										2.7 V	
	μPD780001	8K		—	—					1 ch	39		—
	μPD78002	8K to 16K			1 ch		—				53		Available
	μPD78083				—		8 ch			1 ch (UART: 1 ch)	33	1.8 V	—
Inverter control	μPD780964	8K to 32K	3 ch	**Note**	—	1 ch	—	8 ch	—	2 ch (UART: 2 ch)	47	2.7 V	Available
	μPD780924						8 ch	—					
FIP driving	μPD780208	32K to 60K	2 ch	1 ch	1 ch	1 ch	8 ch	—	—	2 ch	74	2.7 V	—
	μPD780228	48K to 60K	3 ch	—	—					1 ch	72	4.5 V	
	μPD78044H	32K to 48K	2 ch	1 ch	1 ch						68	2.7 V	
	μPD78044F	16K to 40K								2 ch			
LCD driving	μPD780308	48K to 60K	2 ch	1 ch	1 ch	1 ch	8 ch	—	—	3 ch (Time division UART: 1 ch)	57	2.0 V	—
	μPD78064B	32K								2 ch (UART: 1 ch)			
	μPD78064	16K to 32K											
IEBus supported	μPD78098B	40K to 60K	2 ch	1 ch	1 ch	1 ch	8 ch	—	2 ch	3 ch (UART: 1 ch)	69	2.7 V	Available
	μPD78098	32K to 60K											
Meter driving	μPD780973	24K to 32K	3 ch	1 ch	1 ch	1 ch	5 ch	—	—	2 ch (UART: 1 ch)	56	4.5 V	—
LV	μPD78P0914	32K	6 ch	—	—	1 ch	8 ch	—	—	2 ch	54	4.5 V	Available

Note 10-bit timer: 1 channel

FUNCTION OVERVIEW

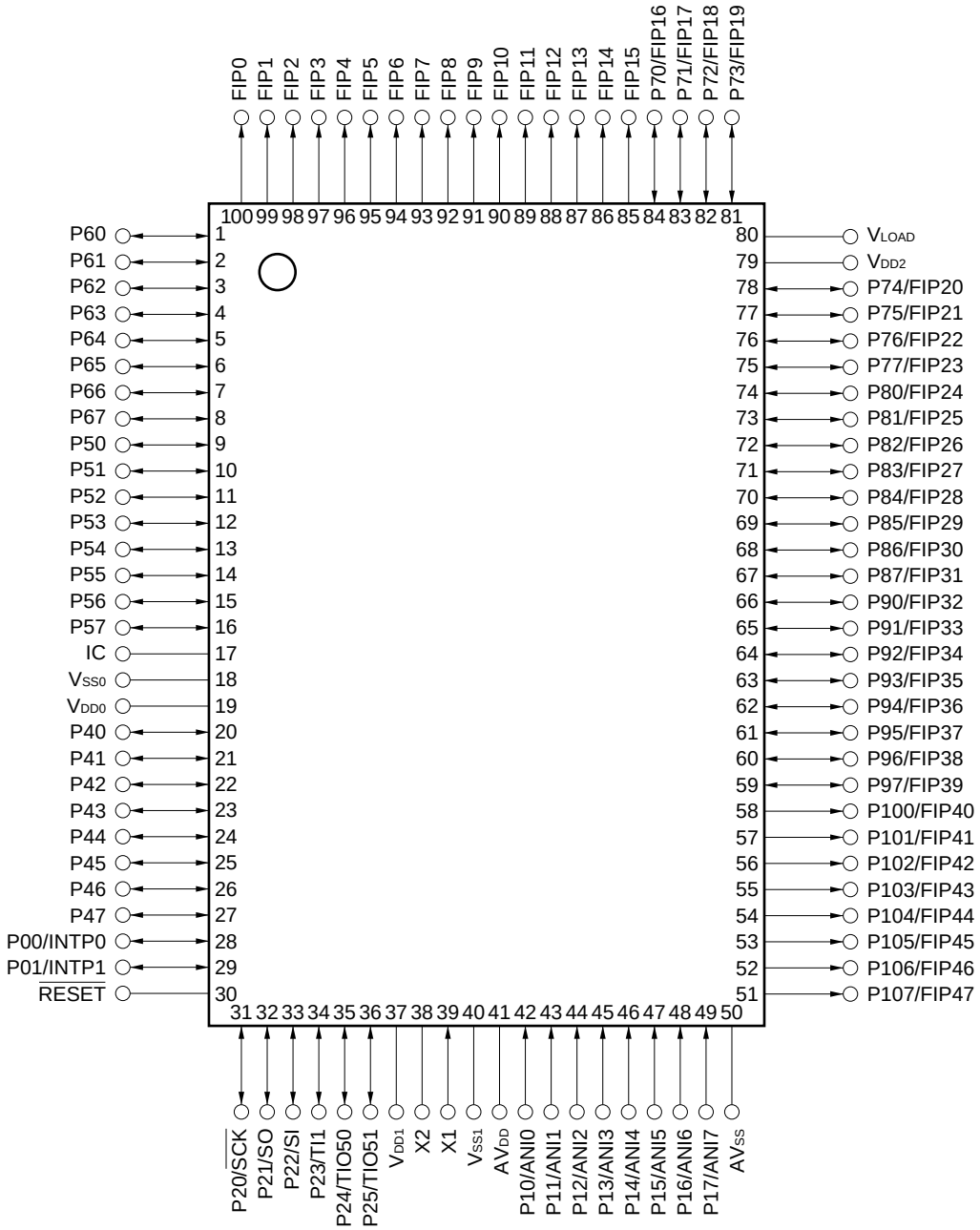
Item \ Product Name		μPD780226	μPD780228
Internal memory	ROM	48 Kbytes	60 Kbytes
	High-speed RAM	1024 bytes	
	Expansion RAM	512 bytes	
	FIP display RAM	96 bytes	
General-purpose register		8 bits × 32 registers (8 bits × 8 registers × 4 banks)	
Minimum instruction execution time		• On-chip minimum instruction execution time variable function • 0.4 μs/0.8 μs/1.6 μs/3.2 μs/6.4 μs (@ 5.0-MHz operation with main system clock)	
Instruction set		• Multiply/divide (8 bits × 8 bits, 16 bits ÷ 8 bits) • Bit manipulate (set, reset, test, Boolean operation)	
I/O ports (including alternate function pins for FIP)		Total : 72 • CMOS inputs : 8 • CMOS I/Os : 16 • N-ch open-drain I/Os : 16 • P-ch open-drain I/Os : 24 • P-ch open-drain outputs : 8	
FIP controller/driver		Total of display outputs : 48 • 10-mA display current : 16 • 3-mA display current : 32	
A/D converter		• 8-bit resolution × 8 channels • Power supply voltage: AV_{DD} = 4.5 to 5.5 V	
Serial interface		3-wired serial interface I/O mode: 1 channel	
Timer		• 8-bit remote control timer : 1 channel • 8-bit PWM timer : 2 channels • Watchdog timer : 1 channel	
Timer output		2 (8-bit PWM output is available)	
Vectored interrupt sources	Maskable	Internal: 6, external: 4	
	Non-maskable	Internal: 1	
	Software	1	
Power supply voltage		V_{DD} = 4.5 to 5.5 V	
Package		100-pin plastic QFP (14 × 20 mm)	

CONTENTS

1. PIN CONFIGURATION (TOP VIEW)

• 100-pin plastic QFP (14 × 20 mm)

μPD780226GF-×××-3BA, 780228GF-×××-3BA



Cautions 1. Connect directly the IC (Internally Connected) pin to V_{SS1}.

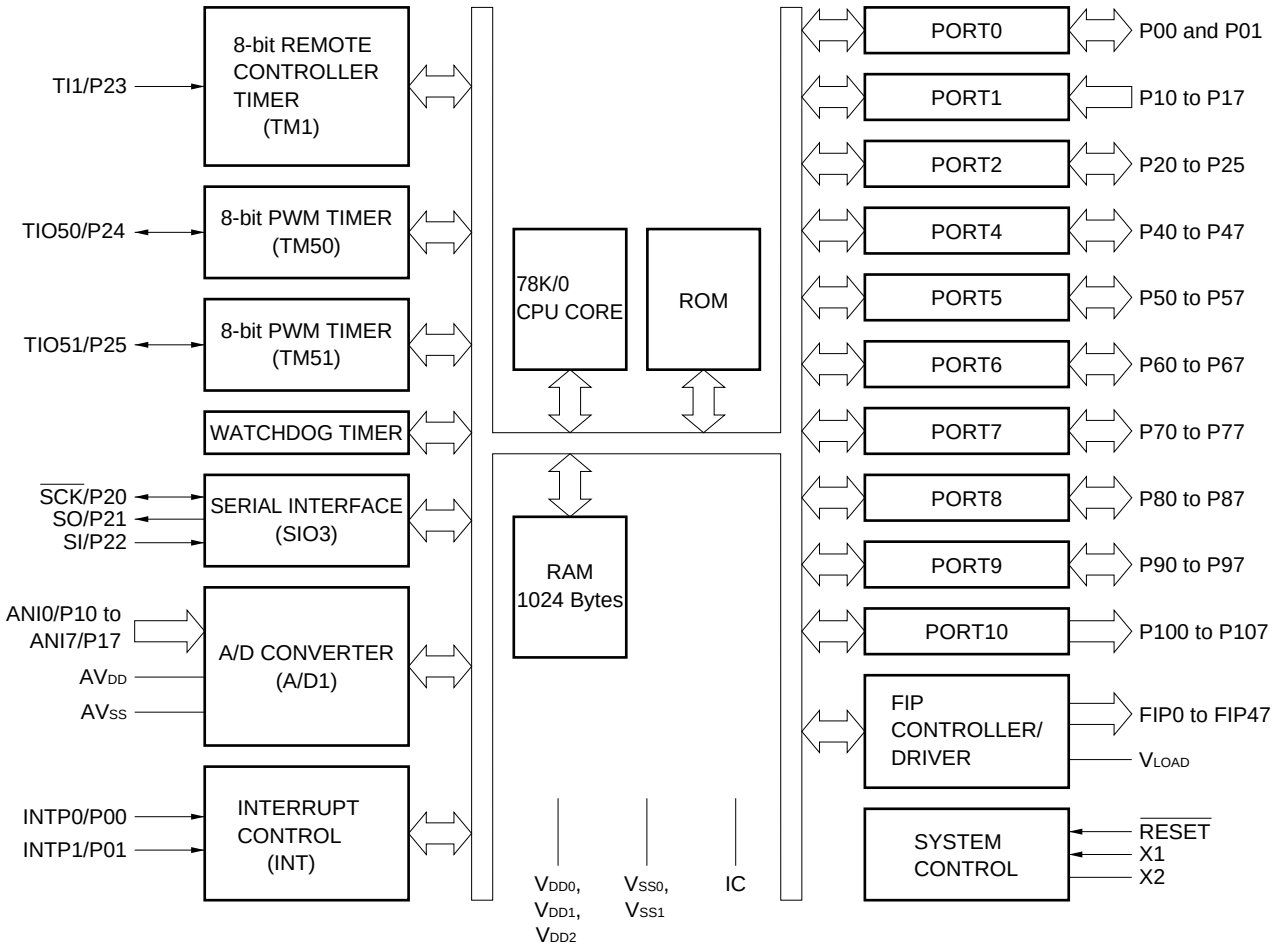
2. Connect AV_{DD} pin to V_{DD1}.

3. Connect AV_{SS} pin to V_{SS1}.

Remark When the μPD780226 or μPD780228 is used in application fields that require reduction of the noise from inside the microcontroller, the implementation of noise reduction measures, such as supplying voltage to V_{DD0} and V_{DD1} individually and connecting V_{SS0} and V_{SS1} to different ground lines, is recommended.

ANI0 to ANI7	:	Analog Input	P80 to P87	:	Port 8
AV_{DD}	:	Analog Power Supply	P90 to P97	:	Port 9
AV_{SS}	:	Analog Ground	P100 to P107	:	Port 10
FIP0 to FIP47	:	Fluorescent Indicator Panel	$\overline{RESET}$	:	Reset
IC	:	Internally Connected	SCK	:	Serial Clock
INTP0 and INTP1	:	Interrupt from Peripherals	SI	:	Serial Input
P00 and P01	:	Port 0	SO	:	Serial Output
P10 to P17	:	Port 1	TI1	:	Timer Input
P20 to P25	:	Port 2	TIO50 and TIO51	:	Timer Input/Output
P40 to P47	:	Port 4	V_{DD0} to V_{DD2}	:	Power Supply
P50 to P57	:	Port 5	V_{LOAD}	:	Negative Power Supply
P60 to P67	:	Port 6	V_{SS0} and V_{SS1}	:	Ground
P70 to P77	:	Port 7	X1, and X2	:	Crystal

2. BLOCK DIAGRAM



Remark The internal ROM capacity differs depending on the product.

3. PIN FUNCTION LIST

3.1 Port Pins (1/2)

Pin Name	I/O	Function	After Reset	Alternate Function
P00	I/O	Port 0. 2-bit I/O port. Input/output can be specified bit-wise. When used as an input port, an on-chip pull-up resistor can be connected by means of software.	Input	INTP0
P01				INTP1
P10 to P17	Input	Port 1. 8-bit input only port.	Input	ANI0 to ANI7
P20	I/O	Port 2. 6-bit I/O port. Input/output can be specified bit-wise. When used as an input port, an on-chip pull-up resistor can be connected by means of software.	Input	$\overline{\text{SCK}}$
P21				SO
P22				SI
P23				TI1
P24				TIO50
P25				TIO51
P40 to P47	I/O	Port 4. 8-bit I/O port. Input/output can be specified bit-wise. LEDs can be driven directly. When used as an input port, an on-chip pull-up resistor can be connected by means of software.	Input	—
P50 to P57	I/O	Port 5. N-ch open-drain 8-bit medium-voltage I/O port. Input/output can be specified bit-wise. LEDs can be driven directly. A pull-up resistor can be incorporated bit-wise by mask option.	Input	—
P60 to P67	I/O	Port 6. N-ch open-drain 8-bit medium-voltage I/O port. Input/output can be specified bit-wise. LEDs can be driven directly. A pull-up resistor can be incorporated bit-wise by mask option.	Input	—

3.1 Port Pins (2/2)

Pin Name	I/O	Function	After Reset	Alternate Function
P70 to P77	I/O	Port 7. P-ch open-drain 8-bit high-voltage I/O port. Input/output can be specified bit-wise. LEDs can be driven directly. A pull-down resistor can be incorporated bit-wise by mask option.	Input	FIP16 to FIP23
P80 to P87	I/O	Port 8. P-ch open-drain 8-bit high-voltage I/O port. Input/output can be specified bit-wise. A pull-down resistor can be incorporated bit-wise by mask option.	Input	FIP24 to FIP31
P90 to P97	I/O	Port 9. P-ch open-drain 8-bit high-voltage I/O port. Input/output can be specified bit-wise. A pull-down resistor can be incorporated bit-wise by mask option.	Input	FIP32 to FIP39
P100 to P107	Output	Port 10. P-ch open-drain 8-bit high-voltage I/O port. A pull-down resistor can be incorporated bit-wise by mask option.	Output	FIP40 to FIP47

3.2 Non-port Pins

Pin Name	I/O	Function	After Reset	Alternate Function
INTP0	Input	Effective edge (rising edge, falling edge, or both rising and falling edges) can be specified. External interrupt request input.	Input	P00
INTP1				P01
$\overline{SCK}$	I/O	Serial interface serial clock I/O.	Input	P20
SO	Output	Serial interface serial data output.	Input	P21
SI	Input	Serial interface serial data input.	Input	P22
TI1	Input	8-bit remote control timer (TM1) timer input.	Input	P23
TIO50	I/O	8-bit PWM timer (TM50) capture trigger input/timer output.	Input	P24
TIO51	I/O	8-bit PWM timer (TM51) capture trigger input/timer output.	Input	P25
FIP0 to FIP15	Output	FIP controller/driver high-voltage withstand large current output.	Output	—
FIP16 to FIP23			Input	P70 to P77
FIP24 to FIP31				P80 to P87
FIP32 to FIP39				P90 to P97
FIP40 to FIP47				P100 to P107
V_{LOAD}	—	FIP controller/driver pull-down resistor connection.	—	—
$\overline{RESET}$	Input	System reset input.	—	—
X1	Input	Crystal connection for main system clock oscillation.	—	—
X2	—		—	—
ANI0 to ANI7	Input	A/D converter analog input.	Input	P10 to P17
AV_{DD}	—	A/D converter analog power supply (the same potential with V_{DD1}).	—	—
AV_{SS}	—	A/D converter ground potential (the same potential with V_{SS1}).	—	—
V_{DD0}	—	Positive power supply for ports.	—	—
V_{DD1}	—	Positive power supply except for ports, analog, and FIP controller/driver.	—	—
V_{DD2}	—	Positive power supply for FIP controller/driver.	—	—
V_{SS0}	—	Ground potential for ports.	—	—
V_{SS1}	—	Ground potential except for ports and analog.	—	—
IC	—	Internal connection. Connect directly to V_{SS1} pin.	—	—

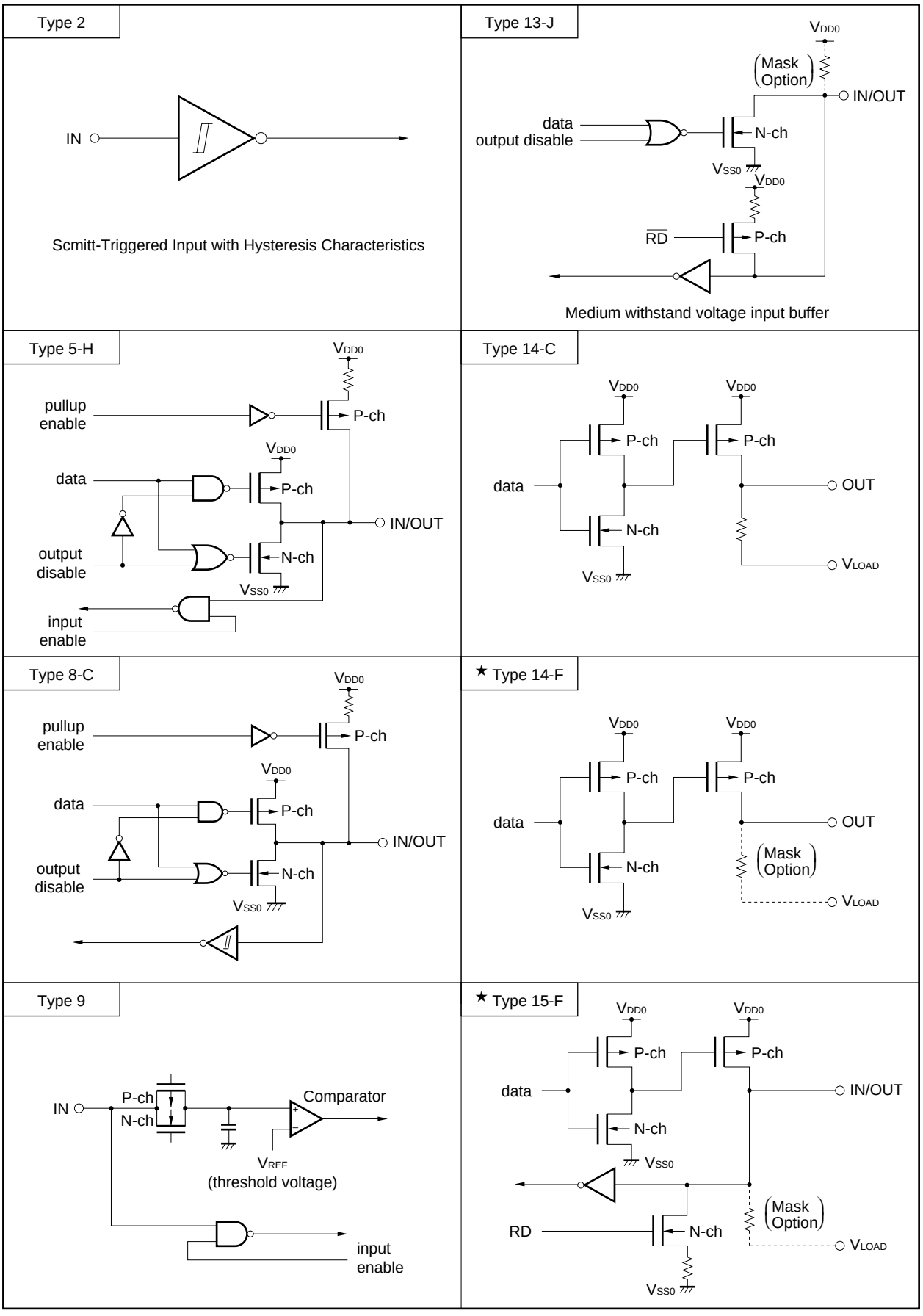
3.3 Pin I/O Circuits and Recommended Connection of Unused Pins

The I/O circuit type of each pin and the recommended connection of unused pins are shown in Table 3-1. For the I/O circuit configuration of each type, see Figure 3-1.

Table 3-1. Types of Pin I/O Circuits

	Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pins
	P00/INTP0	8-C	I/O	Individually connect to V_{SS0} via a resistor.
	P01/INTP1			
	P10/ANI0 to P17/ANI7	9	Input	
	P20/$\overline{SCK}$	8-C	I/O	Individually connect to V_{DD0} or V_{SS0} via a resistor.
	P21/SO	5-H		
	P22/SI	8-C		
	P23/TI1			
	P24/TIO50			
	P25/TIO51			
	P40 to P47			
	P50 to P57	13-J	I/O	Individually connect to V_{DD0} via a resistor.
	P60 to P67			
★	P70/FIP16 to P77/FIP23	15-F	I/O	Individually connect to V_{DD0} or V_{SS0} via a resistor.
	P80/FIP24 to P87/FIP31			
	P90/FIP32 to P97/FIP39			
★	P100/FIP40 to P107/FIP47	14-F	Output	
	FIP0 to FIP15	14-C	Output	
	$\overline{RESET}$	2	Input	—
	AV_{DD}	—	—	Connect to VDD1.
	AV_{SS}			Connect to V_{SS1}.
	A_{LOAD}			
	IC			Connect to V_{SS1} directly.

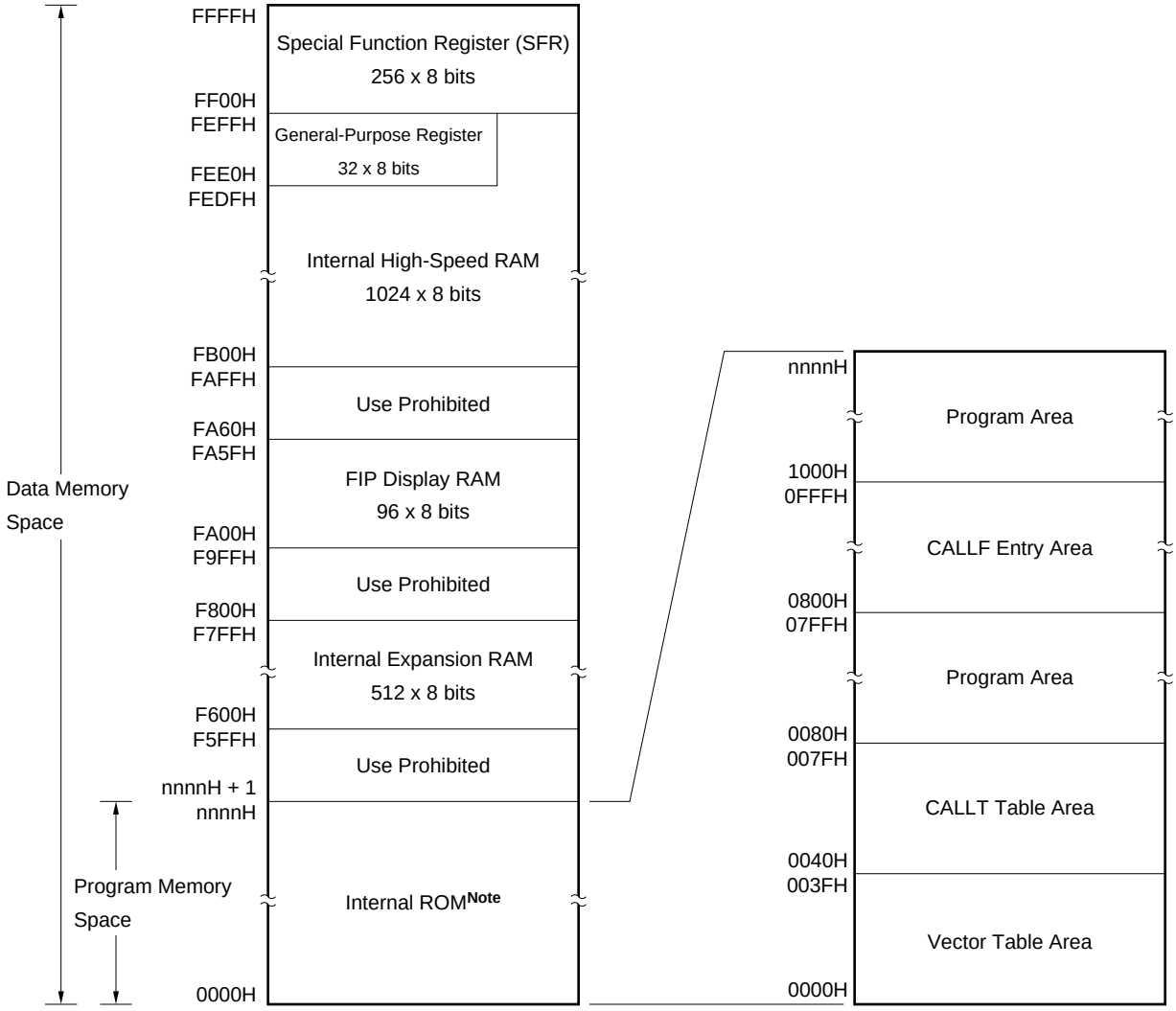
Figure 3-1. Pin I/O Circuits



4. MEMORY SPACE

The memory map of the μPD780226 and μPD780228 is shown in Figure 4-1.

Figure 4-1. Memory Map



Note The internal ROM capacity differs depending on the product (see the table below).

Part Number	Internal ROM Last Address nnnnH
μPD780226	BFFFH
μPD780228	EFFFH

5. PERIPHERAL HARDWARE FUNCTION FEATURES

5.1 Port

There are five kinds of I/O ports.

• CMOS inputs (Port 1)	: 8
• CMOS I/Os (Ports 0, 2, 4)	: 16
• N-ch open-drain I/Os (Ports 5, 6)	: 16
• P-ch open-drain I/Os (Ports 7 to 9)	: 24
• P-ch open-drain outputs (Port 10)	: 8
Total	: 72

Table 5-1. Functions of Ports

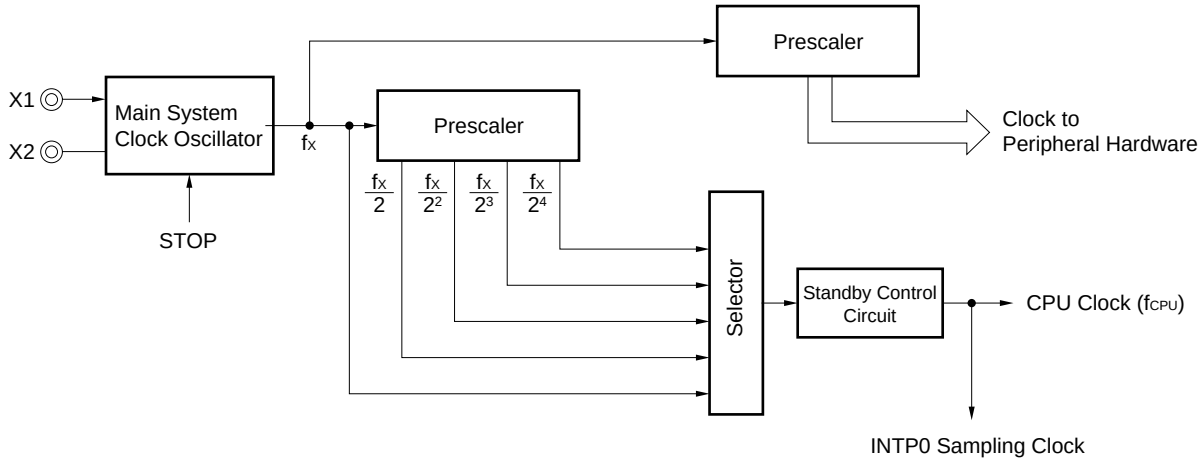
Name	Pin Name	Function
Port 0	P00 and P01	I/O port. Input/output is specifiable bit-wise. When using as an input port, an on-chip resistor can be connected by means of software.
Port 1	P10 to P17	Input only port.
Port 2	P20 to P25	I/O port. Input/output is specifiable bit-wise. When using as an input port, an on-chip resistor can be connected by means of software.
Port 4	P40 to P47	I/O port. Input/output is specifiable bit-wise. When using as an input port, an on-chip resistor can be connected by means of software. LEDs can be driven directly.
Port 5	P50 to P57	N-ch open-drain medium-voltage I/O port. Input/output is specifiable bit-wise. A pull-up resistor can be incorporated bit-wise by mask option. LEDs can be driven directly.
Port 6	P60 to P67	N-ch open-drain medium-voltage I/O port. Input/output is specifiable bit-wise. A pull-up resistor can be incorporated bit-wise by mask option. LEDs can be driven directly.
Port 7	P70 to P77	P-ch open-drain high-voltage I/O port. Input/output is specifiable bit-wise. A pull-down resistor can be incorporated bit-wise by mask option.
Port 8	P80 to P87	P-ch open-drain high-voltage I/O port. Input/output is specifiable bit-wise. A pull-down resistor can be incorporated bit-wise by mask option.
Port 9	P90 to P97	P-ch open-drain high-voltage I/O port. Input/output is specifiable bit-wise. A pull-down resistor can be incorporated bit-wise by mask option.
Port 10	P100 to P107	P-ch open-drain high-voltage output port. A pull-down resistor can be incorporated bit-wise by mask option.

5.2 Clock Generator

The minimum instruction execution time can be changed.

- 0.4 μs/0.8 μs/1.6 μs/3.2 μs/6.4 μs (@ 5.0-MHz operation with main system clock)

Figure 5-1. Clock Generator Block Diagram



5.3 Timer/Event Counter

Four timer/event counter channels are incorporated.

- 8-bit remote control timer : 1 channel
- 8-bit PWM timer : 2 channels
- Watchdog timer : 1 channel

Table 5-2. Types and Functions of Timer/Event Counters

		8-bit Remote/ Control Timer	8-bit PWM Timer	Watchdog Timer
Type	Interval timer	–	2 channels	1 channel
	External event counter	–	2 channels	–
Function	Timer output	–	2 outputs	–
	PWM output	–	2 outputs	–
	Pulse width measurement	1 input	2 inputs	–
	Square wave output	–	2 outputs	–
	Interrupt request	2	2	1

Figure 5-2. 8-Bit Remote Control Timer Block Diagram

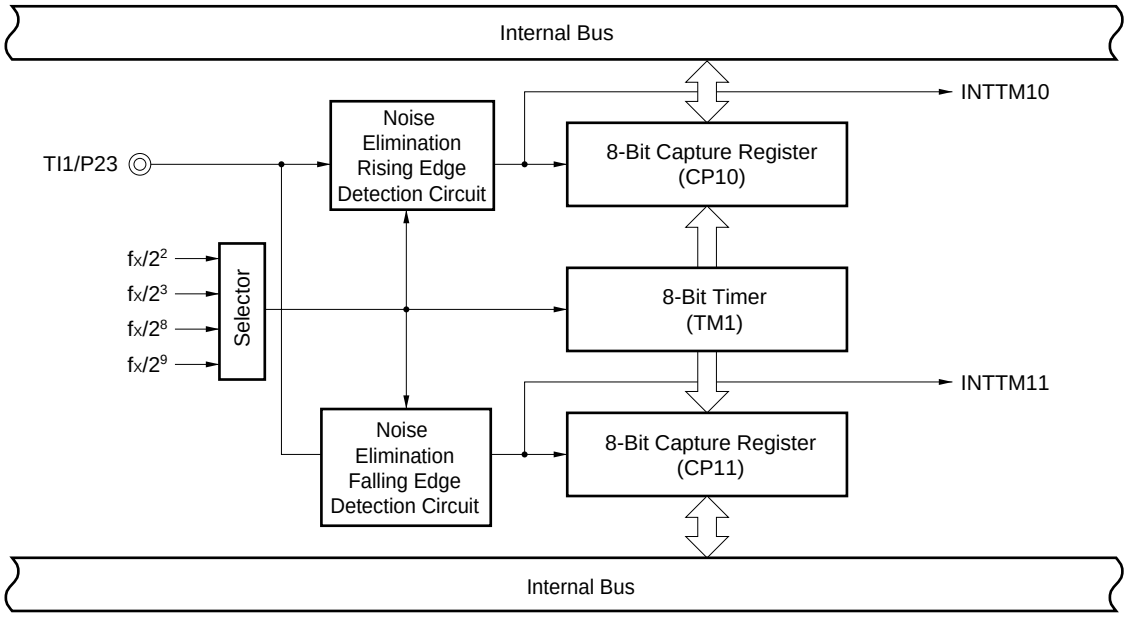


Figure 5-3. 8-Bit PWM Timer Block Diagram

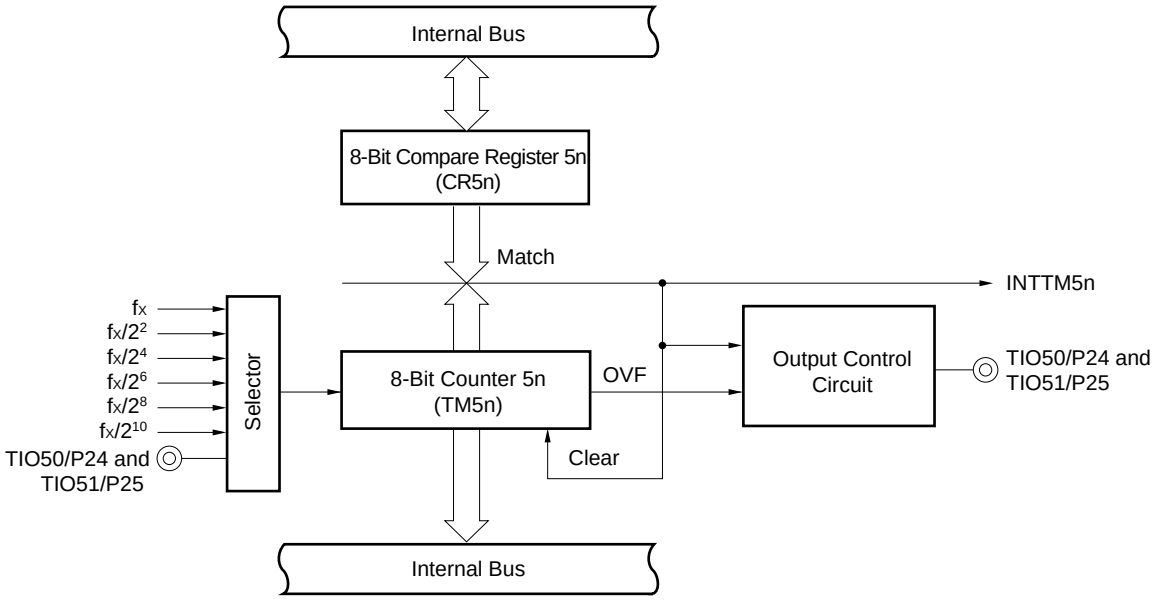
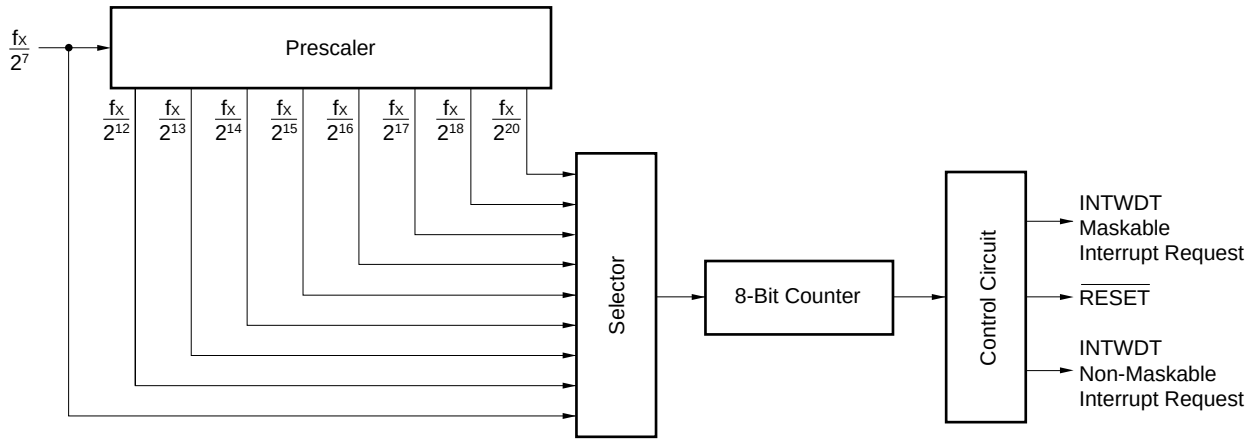


Figure 5-4. Watchdog Timer Block Diagram

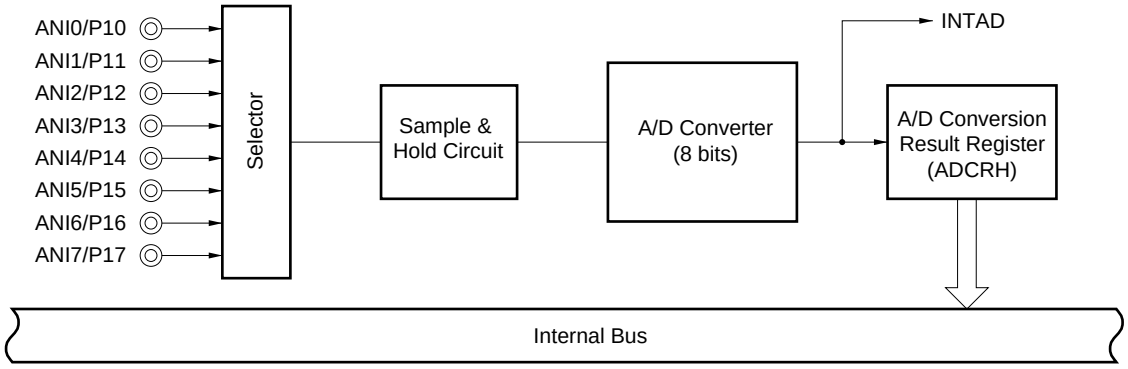


5.4 A/D Converter

An 8-bit resolution 8-channel A/D converter is incorporated.

A/D conversion starts by software only.

Figure 5-5. A/D Converter Block Diagram

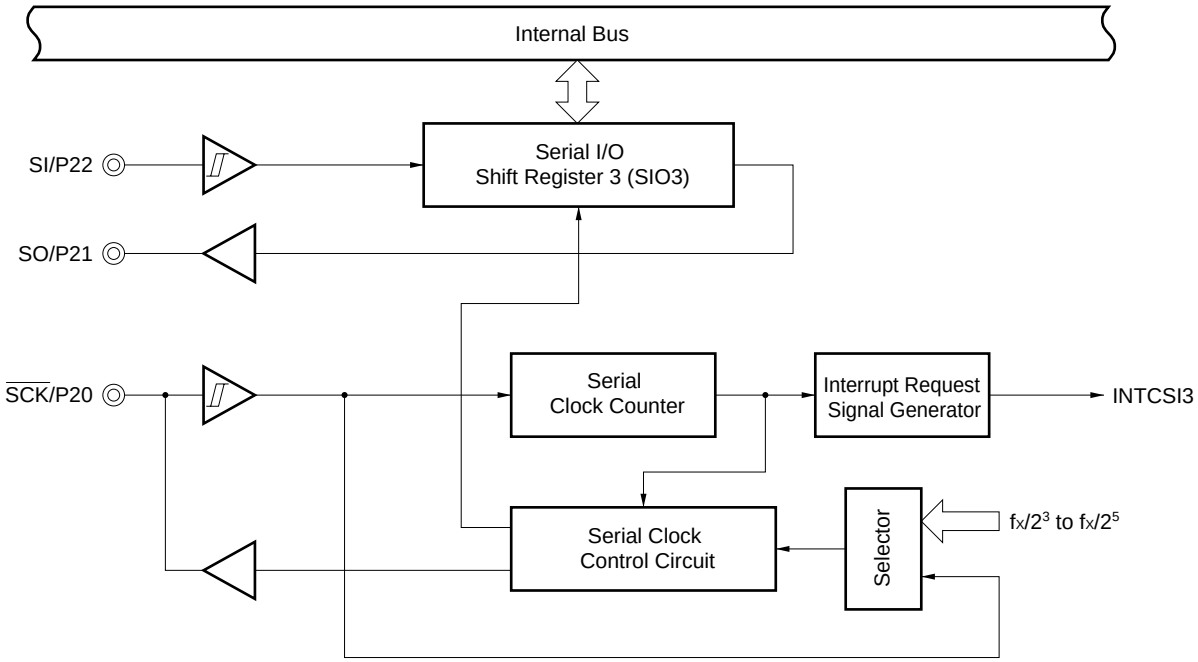


5.5 Serial Interface

A 1-channel clocked serial interface is incorporated.

The serial interface operates in the MSB-first fixed 3-wired serial I/O mode.

Figure 5-6. Serial Interface Block Diagram



5.6 FIP Controller/Driver

An FIP controller/driver with the following functions is incorporated.

(a) Total number of display outputs: 48. Output of 16 patterns is enabled.

(b) 96-byte display RAM is provided to enable display signal output by reading display data automatically (direct memory access).

(c) A port pin which is not used for FIP display can be used as an output port or an I/O port (except for FIP 0 to FIP 15, which are FIP output only pins).

(d) The luminance can be adjusted in 8 stages with display mode register 1 (DSPM1).

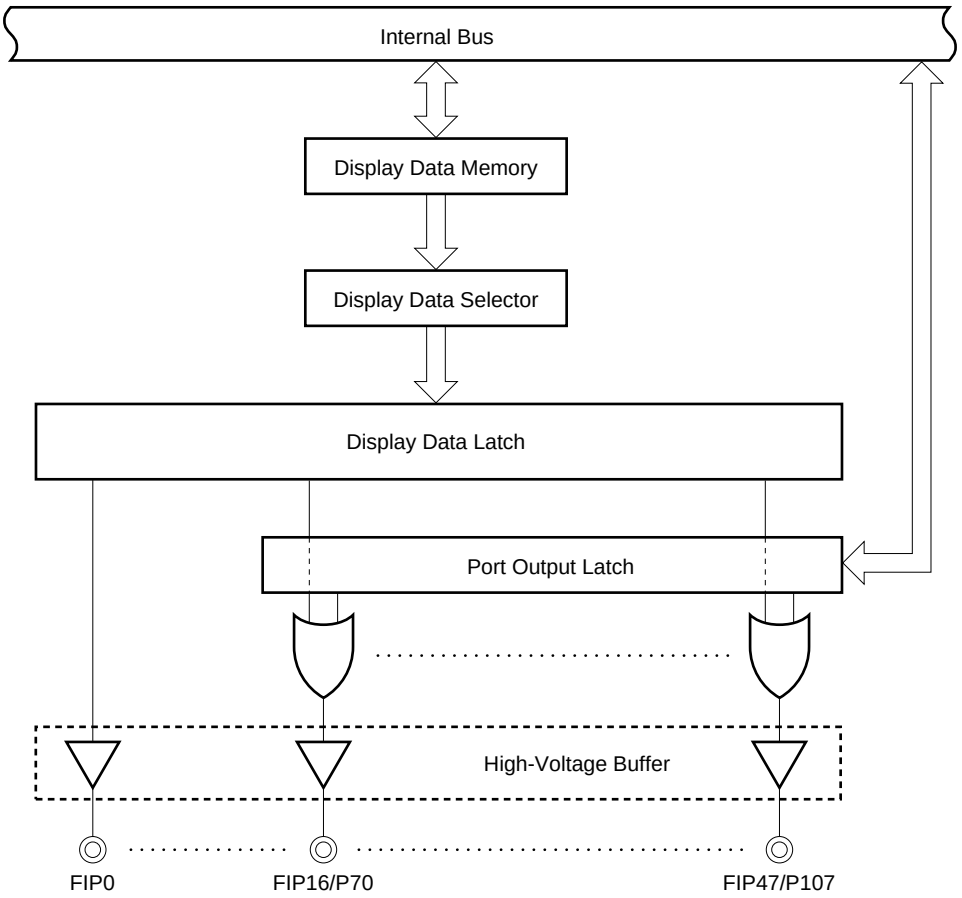
(e) Hardware taking into consideration the key scan application is incorporated.

(f) Whether the key scan timing is inserted or not is selectable.

(g) A high-voltage output buffer (FIP driver) that can drive the FIP directly is incorporated.

(h) The FIP output pin can incorporate the pull-down resistor by mask option (A pull-down resistor is preinstalled to pins FIP0 to 15).

Figure 5-7. FIP Controller/Driver Block Diagram



6. INTERRUPT FUNCTIONS

There are twelve interrupt functions of three different kinds, as shown below.

- Non-maskable : 1
- Maskable : 10
- Software : 1

Table 6-1. Interrupt Source List

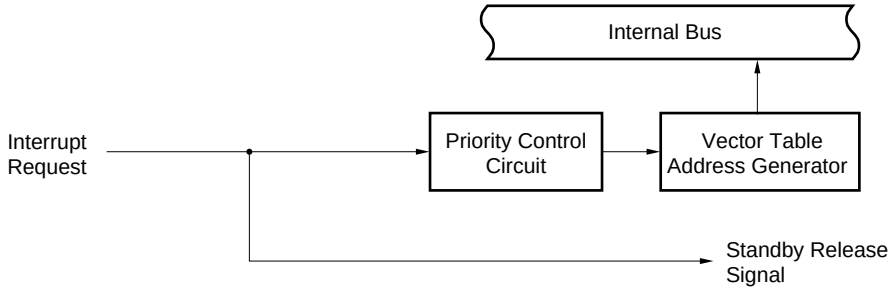
Interrupt Type	Default Priority Note 1	Interrupt Source		Internal/ External	Vector Table Address	Basic Configuration Type Note 2
		Name	Trigger			
Non-maskable	—	INTWDT	Watchdog timer overflow (when watchdog timer mode 1 is selected)	Internal	0004H	(A)
Maskable	0	INTWDT	Watchdog timer overflow (when interval timer mode is selected)			(B)
	1	INTP0	Pin input edge detection	External	0006H	(C)
	2	INTP1			0008H	
	3	INTTM10	Timer input edge detection		000AH	(D)
	4	INTTM11			000CH	
	5	INTKS	Key scan timing from FIP controller/driver	Internal	000EH	(B)
	6	INTCSI3	Serial interface transfer termination		0010H	
	7	INTTM50	8-bit timer (TM50) match		0012H	
	8	INTTM51	8-bit timer (TM51) match		0014H	
	9	INTAD	A/D conversion termination		0016H	
Software	—	BRK	BRK instruction execution	—	003EH	(E)

Notes 1. Default priority is a priority order when more than one maskable interrupt requests are generated simultaneously. 0 is the highest priority and 9 the lowest priority.

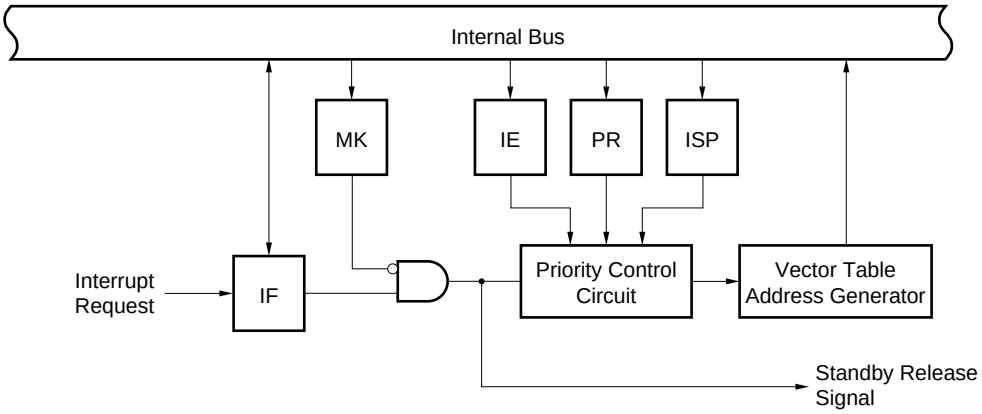
2. Basic configuration types (A) to (E) correspond to those shown in Figure 6-1.

Figure 6-1. Basic Interrupt Function Configuration (1/2)

(A) Internal non-maskable interrupt



(B) Internal maskable interrupt



(C) External maskable interrupt (INTP0, INTP1)

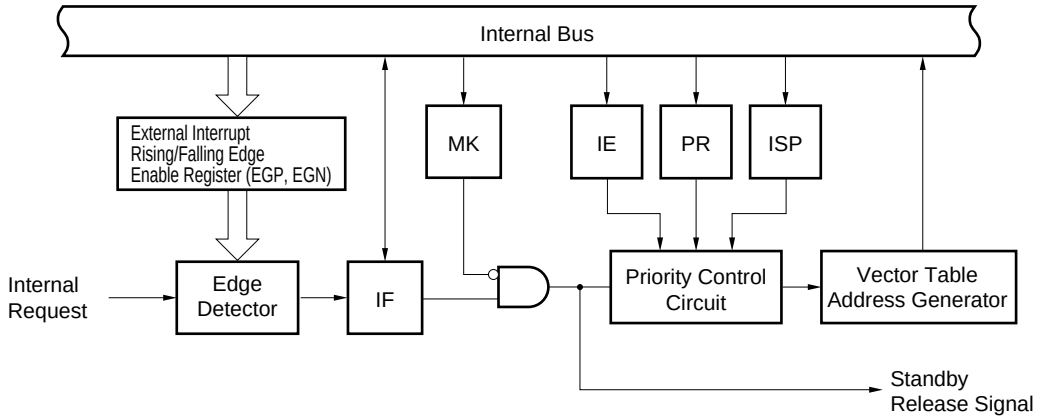
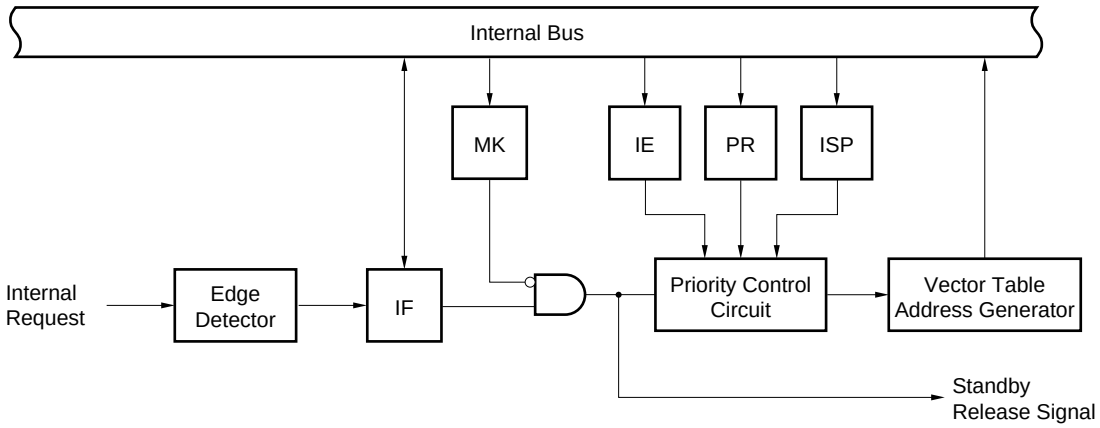
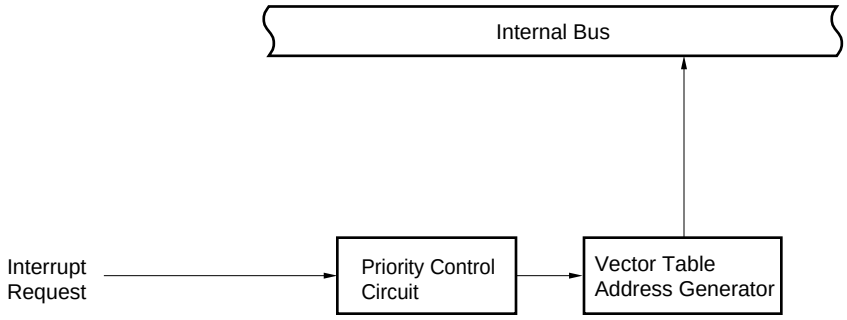


Figure 6-1. Basic Interrupt Function Configuration (2/2)

(D) External maskable interrupt



(E) Software interrupt



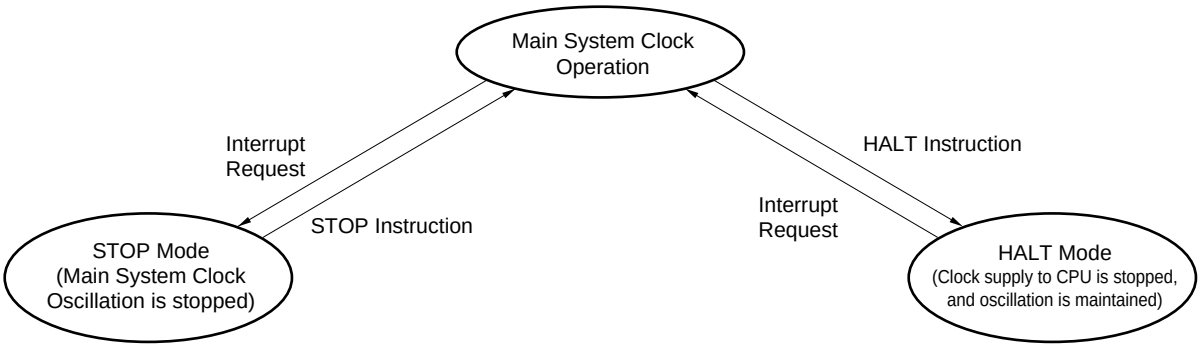
IF : Interrupt request flag
IE : Interrupt enable flag
ISP : In-service priority flag
MK : Interrupt mask flag
PR : Priority specification flag

7. STANDBY FUNCTION

The standby function is a function to reduce the current consumption. There are the following two kinds of standby functions.

- HALT mode : Halts the CPU operating clock and can reduce the average consumption current by intermittent operation along with normal operation.
- STOP mode : Halts the main system clock oscillation. Halts all operations with the main system clock and sets ultra-low power dissipation state with the subsystem clock only.

Figure 7-1. Standby Function



8. RESET FUNCTION

There are the following two kinds of resetting methods.

- External reset by the $\overline{\text{RESET}}$ input
- Internal reset by watchdog timer runaway time detection

9. INSTRUCTION SET

(1) 8-bit instructions

MOV, XCH, ADD, ADDC, SUB, SUBC, AND, OR, XOR, CMP, MULU, DIVUW, INC, DEC, ROR, ROL, RORC, ROLC, ROR4, ROL4, PUSH, POP, DBNZ

1st operand \ 2nd operand	#byte	A	r Note	sfr	saddr	!addr16	PSW	[DE]	[HL]	[HL+byte] [HL+B] [HL+C]	$addr16	1	None
A	ADD ADDC SUB SUBC AND OR XOR CMP		MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP		ROR ROL RORC ROLC	
r	MOV	MOV ADD ADDC SUB SUBC AND OR XOR CMP											INC DEC
B, C											DBNZ		
sfr	MOV	MOV											
saddr	MOV ADD ADDC SUB SUBC AND OR XOR CMP	MOV									DBNZ		INC DEC
!addr16		MOV											
PSW	MOV	MOV											PUSH POP
[DE]		MOV											
[HL]		MOV											ROR4 ROL4
[HL+byte] [HL+B] [HL+C]		MOV											
X													MULU
C													DIVUW

Note Except r = A

(2) 16-bit instructions

MOVW, XCHW, ADDW, SUBW, CMPW, PUSH, POP, INCW, DECW

1st operand \ 2nd operand	#word	AX	rp Note	sfrp	saddrp	!addr16	SP	None
AX	ADDW SUBW CMPW		MOVW XCHW	MOVW	MOVW	MOVW	MOVW	
rp	MOVW	MOVW Note						INCW,DECW PUSH, POP
sfrp	MOVW	MOVW						
saddrp	MOVW	MOVW						
!addr16		MOVW						
SP	MOVW	MOVW						

Note Only when rp = BC, DE, HL

(3) Bit manipulation instructions

MOV1, AND1, OR1, XOR1, SET1, CLR1, NOT1, BT, BF, BTCLR

1st operand \ 2nd operand	A.bit	sfr.bit	saddr.bit	PSW.bit	[HL].bit	CY	$addr16	None
A.bit						MOV1	BT BF BTCLR	SET1 CLR1
sfr.bit						MOV1	BT BF BTCLR	SET1 CLR1
saddr.bit						MOV1	BT BF BTCLR	SET1 CLR1
PSW.bit						MOV1	BT BF BTCLR	SET1 CLR1
[HL].bit						MOV1	BT BF BTCLR	SET1 CLR1
CY	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1			SET1 CLR1 NOT1

(4) Call instruction/branch instructions

CALL, CALLF, CALLT, BR, BC, BNC, BZ, BNZ, BT, BF, BTCLR, DBNZ

1st operand \ 2nd operand	AX	!addr16	!addr11	[addr5]	$addr16
Basic instruction	BR	CALL BR	CALLF	CALLT	BR, BC, BNC, BZ, BNZ
Compound instruction					BT, BF, BTCLR DBNZ

(5) Other instructions

ADJBA, ADJBS, BRK, RET, RETI, RETB, SEL, NOP, EI, DI, HALT, STOP

★ 10. ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

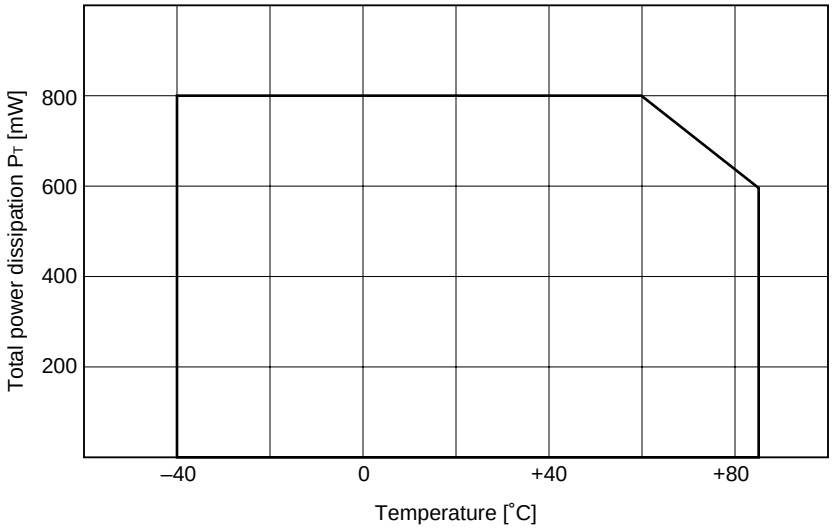
Parameter	Symbol	Conditions		Rating	Unit
Supply voltage	V_{DD}			–0.3 to +6.5	V
	V_{LOAD}			V_{DD} – 40 to V_{DD} + 0.3	V
	AV_{DD}			–0.3 to V_{DD} + 0.3	V
	AV_{SS}			–0.3 to +0.3	V
Input voltage	V_{I1}	P00, P01, P10 to P17 (except analog input pin), P20 to P25, P40 to P47, X1, X2, $\overline{\text{RESET}}$		–0.3 to V_{DD} + 0.3	V
	V_{I2}	P50 to P57, P60 to P67	N-ch open drain	–0.3 to +13 Note 1	V
	V_{I3}	P70 to P77, P80 to P87, P90 to P97	P-ch open drain	V_{DD} – 40 to V_{DD} + 0.3	V
Output voltage	V_{O1}	P00, P01, P10 to P17, P20 to P25, P40 to P47		–0.3 to V_{DD} + 0.3	V
	V_{O2}	P50 to P57, P60 to P67	N-ch open drain	–0.3 to +13 Note 1	V
	V_{OD}	P70 to P77, P80 to P87, P90 to P97, P100 to P107	P-ch open drain	V_{DD} – 40 to V_{DD} + 0.3	V
Analog input voltage	V_{AN}	ANI0 to ANI7	Analog input pins	AV_{SS} to AV_{DD}	V
High-level output current	I_{OH}	1 pin of P00, P01, P20 to P25, P40 to P47		–10	mA
		Total for P00, P01, P20 to P25, P40 to P47		–30	mA
		1 pin of FIP0 to FIP15		–15	mA
		1 pin of FIP16 to FIP47 (P7 to P10)		–5	mA
		Total for FIP0 to FIP47		–225	mA
Low-level output current	I_{OL}	1 pin of P00, P01, P20 to P25	r.m.s.	10	mA
		1 pin of P40 to P47, P50 to P57, P60 to P67	r.m.s.	20	mA
		Total for P00, P01, P20 to P25, P40 to P47, P50 to P57, P60 to P67	r.m.s.	260	mA
Total power dissipation	P_T Note 2	T_A = –40 to +60°C		800	mW
		T_A = +85°C		600	mW
Operating ambient temperature	T_A			–40 to +85	°C
Storage temperature	T_{stg}			–65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded for even a single parameter, even momentarily. In other words, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions which ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, alternate-function pin characteristics are the same as port pin characteristics.

Notes 1. With the mask option, the range of the internal pull-up resistor pin is –0.3 to V_{DD} +0.3.

2. Total power dissipation differs depending on the temperature (see the following figure).



How to calculate total power dissipation

Total power dissipation of the μPD780226 and 780228 can be divided to the following three. The sum of the three power dissipation should be less than the total power dissipation PT rated in the above figure (80% or less of ratings is recommended).

<1> CPU power dissipation: calculate V_{DD} (MAX.) × I_{DD} (MAX.).

<2> Output pin power dissipation: Power dissipation when maximum current flows into FIP output pins.

<3> Pull-down resistor power dissipation: Power dissipation by the pull-down resistors incorporated in FIP output pins by mask option.

The following is how to calculate total power dissipation for the example in Figure 10-1.

Example Assume the following conditions:

V_{DD} = 5.5 V, 5.0-MHz oscillation

Supply current (I_{DD}) = 21.0 mA

FIP output: 11 grids × 10 segments (Blanking width = 1/16)
Maximum current at the grid pin is 10 mA.
Maximum current at the segment pin is 3 mA.
At the key scan timing, FIP output pin is OFF.

FIP output voltage: grid V_{OD} = V_{DD} – 2 V (voltage drop of 2 V)
segments V_{OD} = V_{DD} – 0.5 V (voltage drop of 0.5 V)

Fluorescent display control voltage (V_{LOAD}) = –35 V

Mask option pull-down resistor = 25 kΩ

By placing the above conditions in calculation <1> to <3>, the total dissipation can be worked out.

<1> CPU power dissipation: 5.5 V × 21.0 mA = 115.5 mW

<2> Output pin power dissipation:

Grid $(V_{DD} - V_{OD}) \times \frac{\text{Total current value of each grid}}{\text{The number of grids + 1}} \times (1 - \text{Blanking width})$

$= 2\text{ V} \times \frac{10\text{ mA} \times 11\text{ Grids}}{11\text{ Grids + 1}} \times (1 - \frac{1}{16}) = 17.2\text{ mW}$

Segment $(V_{DD} - V_{OD}) \times \frac{\text{Total segment current value of illuminated dots}}{\text{The number of grids +1}} \times (1 - \text{Blanking width})$

$= 0.5\text{ V} \times \frac{3\text{ mA} \times 31\text{ Dots}}{11\text{ Grids + 1}} \times (1 - \frac{1}{16}) = 3.6\text{ mW}$

<3> Pull-down resistor power dissipation:

Grid $\frac{(V_{OD} - V_{LOAD})^2}{\text{Pull-down resistor value}} \times \frac{\text{The number of grids}}{\text{The number of grids + 1}} \times (1 - \text{Blanking width})$

$= \frac{(5.5\text{ V} - 2\text{ V} - (-35\text{ V}))^2}{25\text{ k}\Omega} \times \frac{11\text{ Grids}}{11\text{ Grids + 1}} \times (1 - \frac{1}{16}) = 50.9\text{ mW}$

Segment $\frac{(V_{OD} - V_{LOAD})^2}{\text{Pull-down resistor value}} \times \frac{\text{The number of illuminated dots}}{\text{The number of grids + 1}} \times (1 - \text{Blanking width})$

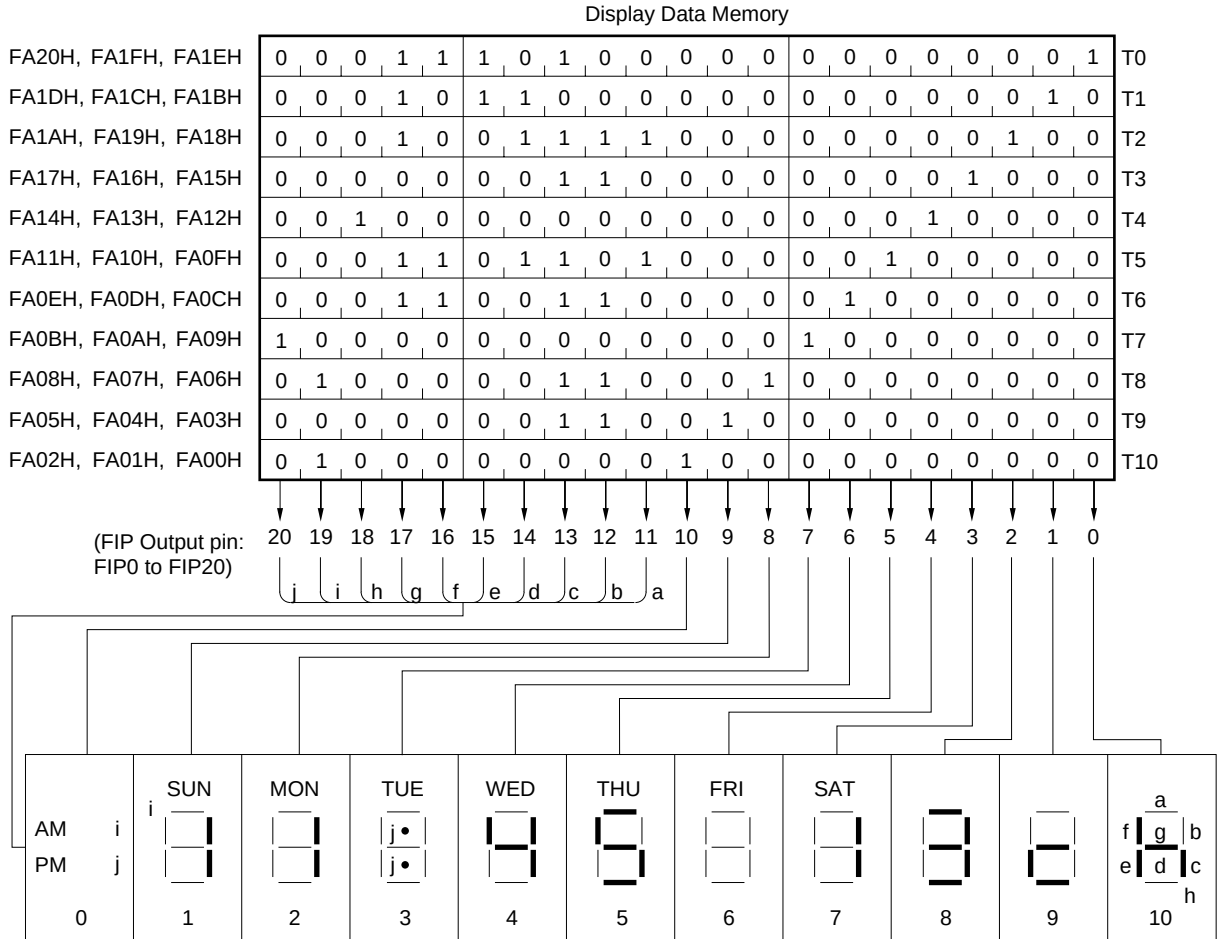
$= \frac{(5.5\text{ V} - 0.5\text{ V} - (-35\text{ V}))^2}{25\text{ k}\Omega} \times \frac{31\text{ dots}}{11\text{ Grids + 1}} \times (1 - \frac{1}{16}) = 155.0\text{ mW}$

Total power dissipation = <1> + <2> + <3> = 115.5 + 17.2 + 3.6 + 50.9 + 155.0 = 342.2 mW

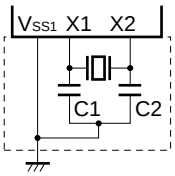
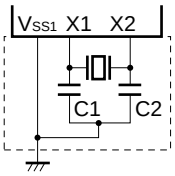
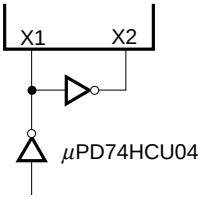
In this example, the total power dissipation does not exceed the rating of the total power dissipation, so there is no problem in power dissipation.

However, when the total power dissipation exceeds the rating of the total power dissipation, it is necessary to lower the power dissipation. To reduce power dissipation, reduce the number of pull-down resistors.

Figure 10-1. Display Example of 10 Segments-11 Digits



MAIN SYSTEM CLOCK OSCILLATION CIRCUIT CHARACTERISTICS (T_A = –40 to +85°C, V_{DD} = 4.5 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f_X)Note 1	V_{DD} = Oscillation voltage range	1		5	MHz
		Oscillation stabilization timeNote 2	After V_{DD} reaches the minimum value of oscillation voltage range			4	ms
Crystal resonator		Oscillation frequency (f_X)Note 1		1		5	MHz
		Oscillation stabilization timeNote 2				10	ms
External clock		X1 input frequency (f_X)Note 1		1		5	MHz
		X1 input high-/low-level width (t_{XH}/t_{XL})		85		500	ns

Notes 1. Only the oscillator characteristics are shown. See **AC CHARACTERISTICS** for instruction execution times.

2. This is the time required for oscillation to stabilize after reset, or STOP mode release.

Caution When the main system clock oscillator is used, the following should be noted concerning wiring in the area in the figure enclosed by a broken line to prevent the influence of wiring capacitance, etc.

- **The wiring should be kept as short as possible.**
- **No other signal lines should be crossed.**
- **Keep away from lines carrying a high fluctuating current.**
- **The oscillator capacitor grounding point should always be at the same potential as VSS1.**
- **Do not connect to a ground pattern carrying a high current.**
- **A signal should not be taken from the oscillator.**

RECOMMENDED OSCILLATOR CONSTANT

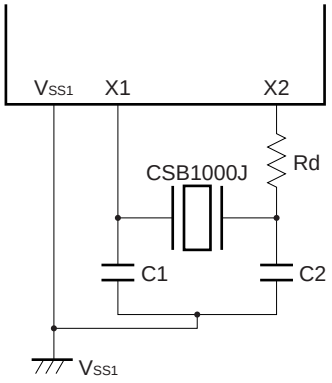
MAIN SYSTEM CLOCK: CERAMIC RESONATOR (T_A = –40 to +85°C)

Manufacturer	Product Name	Frequency (MHz)	Circuit Constant		Oscillator Voltage Range		Remark
			C1 (pF)	C2 (pF)	MIN. (V)	MAX. (V)	
Murata Mfg. Co., Ltd. Toyama	CSB1000J	1.000	100	100	4.5	5.5	Rd = 5.6 kΩ **Note**
	CSA2.00MG040	2.000	100	100	4.5	5.5	
	CST2.00MG040	2.000	—	—	4.5	5.5	Built-in capacitor
	CSA4.19MG	4.194	30	30	4.5	5.5	
	CST4.19MGW	4.194	—	—	4.5	5.5	Built-in capacitor
	CSA5.00MG	5.000	30	30	4.5	5.5	
	CST5.00MGW	5.000	—	—	4.5	5.5	Built-in capacitor
TDK Corp.	CCR1000K2	1.00	100	100	4.5	5.5	
	CCR4.19MC3	4.19	—	—	4.5	5.5	Built-in capacitor, surface-mount type
	FCR4.19MC5	4.19	—	—	4.5	5.5	Built-in capacitor
	CCR5.0MC3	5.00	—	—	4.5	5.5	Built-in capacitor, surface-mount type
	FCR5.0MC5	5.00	—	—	4.5	5.5	Built-in capacitor
Matsushita Electronics Components Co., Ltd.	EFOEC2004A4	2.00	—	—	4.5	5.5	Built-in capacitor
	EFOEC4194A4	4.19	—	—	4.5	5.5	Built-in capacitor
	EFOEC5004A4	5.00	—	—	4.5	5.5	Built-in capacitor

Note When using the CSB1000J (1.000 MHz) of Murata Mfg. Co., Ltd. Toyama for a ceramic resonator, a restrict resistor of 5.6 kΩ is required (see **Example of Main System Clock Recommended Circuit** below). When using other recommended resonators, a restrict resistor is not required.

Caution The oscillation circuit constants and oscillation voltage range indicate conditions for stable oscillation. However, they do not guarantee accuracy of the oscillation frequency. If the application circuit requires accuracy of the oscillation frequency, it is necessary to set the oscillation frequency in the application circuit. For this, it is necessary to directly contact the manufacturer of the resonator being used.

Example of Main System Clock Recommended Circuit (CSB1000J of Murata Mfg. Co., Ltd. Toyama)



CAPACITANCE (T_A = 25°C, V_{DD} = V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	f = 1 MHz Unmeasured pins returned to 0 V	P10 to P17			15	pF
Output capacitance	C_{OUT}	f = 1 MHz Unmeasured pins returned to 0 V	P100 to P107, FIP0 to FIP15			35	pF
Input/output capacitance	C_{IO}	f = 1 MHz Unmeasured pins returned to 0 V	P00, P01, P20 to P27			15	pF
			P40 to P47, P50 to P57, P60 to P67			20	pF
			P70 to P77, P80 to P87, P90 to P97			35	pF

Remark Unless otherwise specified, the characteristics of alternate-function pins are the same as those of port pins.

DC CHARACTERISTICS (T_A = –40 to +85°C, V_{DD} = 4.5 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
High-level input voltage	V_{IH1}	P00, P01, P10 to P17, P20 to P25, P40 to P47, $\overline{\text{RESET}}$		0.7V_{DD}		V_{DD}	V
	V_{IH2}	P50 to P57, P60 to P67		0.7V_{DD}		12	V
	V_{IH3}	P70 to P77, P80 to P87, P90 to P97		0.7V_{DD}		V_{DD}	V
	V_{IH4}	X1, X2		V_{DD} – 0.5		V_{DD}	V
Low-level input voltage	V_{IL1}	P00, P01, P10 to P17, P20 to P25, $\overline{\text{RESET}}$		0		0.2V_{DD}	V
	V_{IL2}	P40 to P47, P50 to P57, P60 to P67		0		0.3V_{DD}	V
	V_{IL3}	P70 to P77, P80 to P87, P90 to P97		V_{DD} – 35		0.3V_{DD}	V
	V_{IL4}	X1, X2		0		0.4	V
High-level output voltage	V_{OH}	I_{OH} = –1 mA		V_{DD} – 1.0		V_{DD}	V
		I_{OH} = –100 μA		V_{DD} – 0.5		V_{DD}	V
Low-level output voltage	V_{OL1}	P00, P01, P20 to P25	I_{OL} = 400 μA			0.5	V
	V_{OL2}	P40 to P47	I_{OL} = 10 mA		0.4	2.0	V
	V_{OL3}	P50 to P57, P60 to P67	I_{OL} = 15 mA		0.4	2.0	V
High-level input leakage current	I_{LIH1}	P00, P01, P10 to P17, P20 to P25, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, $\overline{\text{RESET}}$	V_{IN} = V_{DD}			3	μA
	I_{LIH2}	X1, X2				20	μA
	I_{LIH3}	P50 to P57, P60 to P67	V_{IN} = 13 V			10	μA
	I_{LIH4}	P70 to P77, P80 to P87, P90 to P97				3	μA
Low-level input leakage current	I_{LIL1}	P00, P01, P10 to P17, P20 to P25, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, $\overline{\text{RESET}}$	V_{IN} = 0 V			–3	μA
	I_{LIL2}	X1, X2				–20	μA
	I_{LIL3}	P50 to P57, P60 to P67				–3[Note 1]	μA
	I_{LIL4}	P70 to P77, P80 to P87, P90 to P97	V_{IN} = –35 V			–10	μA
High-level output leakage current[Note 2]	I_{LOH1}	P00, P01, P20 to P25, P40 to P47, P70 to P77, P80 to P87, P90 to P97, P100 to P107, FIP0 to FIP15	V_{OUT} = V_{DD}			3	μA
	I_{LOH2}	P50 to P57, P60 to P67	V_{OUT} = 15 V			80	μA
Low-level output leakage current[Note 2]	I_{LOL1}	P00, P01, P20 to P25, P40 to P47, P50 to P57, P60 to P67	V_{OUT} = 0 V			–3	μA
	I_{LOL2}	P70 to P77, P80 to P87, P90 to P97, P100 to P107, FIP0 to FIP15	V_{OUT} = V_{LOAD} = V_{DD} – 35 V			–10	μA

Notes 1. For P50 to P57 and P60 to P67 without on-chip pull-up resistor (specifiable by mask option), a low-level input leakage current of –200 μA (MAX.) flows only during the 1st clock after an instruction has been executed to read out ports 5 and 6 (P5, P6) or port mode registers 5 and 6 (PM5, PM6). Outside the period of 1 clock following executing a read-out instruction, the current is –3 μA (MAX.).

2. This current excludes the current which flows in the on-chip pull-up/pull-down resistor.

Remark Unless otherwise specified, the characteristics of alternate-function pins are the same as those of port pins.

DC CHARACTERISTICS (T_A = –40 to +85°C, V_{DD} = 4.5 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
FIP output current	I_{OD}	FIP0 to FIP15	$V_{OD} = V_{DD} – 2$ V			–10	mA
		FIP16 to FIP47				–3	mA
Software pull-up resistance	R_1	P00, P01, P20 to P25, P40 to P47	V_{IN} = 0 V	10	30	100	kΩ
On-chip mask option pull-up resistance	R_2	P50 to P57, P60 to P67		20	40	90	kΩ
On-chip pull-down resistance	R_3	FIP0 to FIP15	$V_{OD} – V_{LOAD}$ = 35 V	25	70	135	kΩ
On-chip mask option pull-down resistance	R_4	FIP16 to FIP47		25	70	135	kΩ
Power supply current [Note]	I_{DD1}	5.0-MHz crystal oscillation Operating mode	PCC = 00H		7	21	mA
	I_{DD2}	5.0-MHz crystal oscillation HALT mode			1.5	4.5	mA
	I_{DD3}	STOP mode			1	30	μA

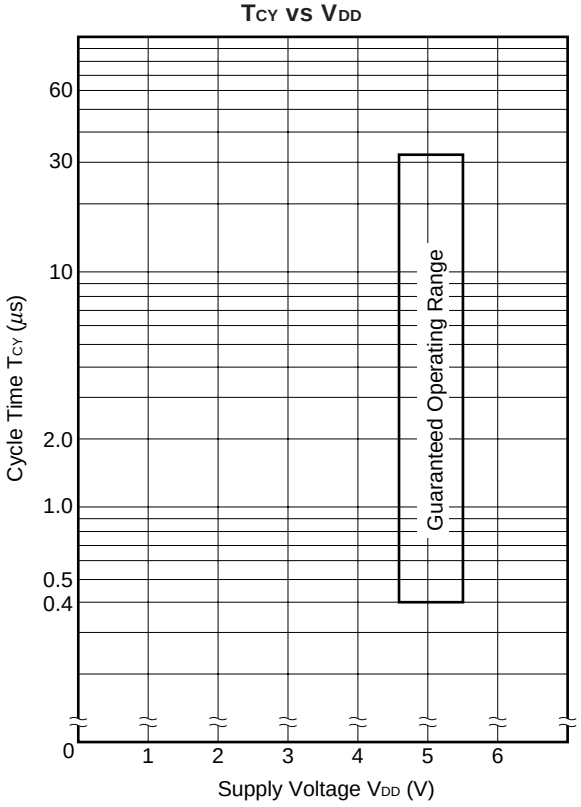
Note This current excludes the port current and the current which flows in the FIP output pin, on-chip pull-up resistor (mask option), and on-chip pull-down resistor (mask option).

Remark Unless otherwise specified, the characteristics of alternate-function pins are the same as those of port pins.

AC CHARACTERISTICS

(1) Basic Operation (T_A = –40 to +85°C, V_{DD} = 4.5 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Cycle time (minimum instruction execution time)	T_{CY}	Operated with main system clock	0.4		32	μs
Interrupt request input high-/low-level width	t_{INTH} t_{INTL}	INTP0, INTP1	10			μs
$\overline{RESET}$ low-level width	t_{RSL}		10			μs



(2) Timer/Counter (T_A = –40 to +85°C, V_{DD} = 4.5 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
TI1 input high-/low-level width	t_{TI1H} t_{TI1L}		$2/F_{count}$ +0.2[Note]			μs
TIO50, TIO51 input high-/low-level width	t_{TI5H} t_{TI5L}		0.1			μs
TIO50, TIO51 input frequency	f_{TI5}				4	MHz

Note F_{COUNT} is the frequency of the count clock selected by TM1 (the frequency can be selected from $f_X/4$, $f_X/8$, $f_X/256$, and $f_X/512$).

(3) Serial Interface (T_A = –40 to +85°C, V_{DD} = 4.5 to 5.5 V)

(a) 3-wire serial I/O mode ($\overline{SCK}$: Internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ cycle time	t_{KCY1}		800			ns
$\overline{SCK}$ high-/low-level width	t_{KH1} t_{KL1}		$t_{KCY1}/2 - 50$			ns
SI setup time (to $\overline{SCK}\uparrow$)	t_{SIK1}		100			ns
SI hold time (from $\overline{SCK}\uparrow$)	t_{KSI1}		400			ns
SO output delay time from $\overline{SCK}\downarrow$	t_{KSO1}	C = 100 pF**Note**			300	ns

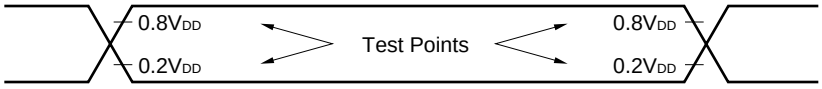
Note C is a load capacitance of the $\overline{SCK}$ and SO output line.

(b) 3-wire serial I/O mode ($\overline{SCK}$: External clock input)

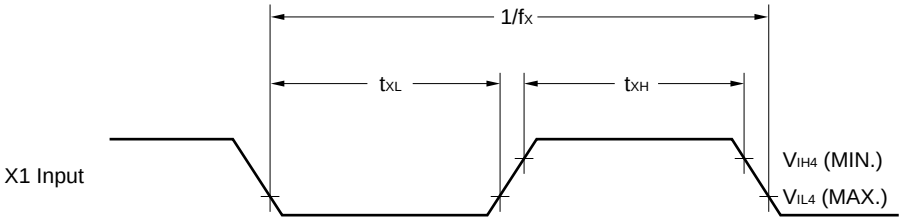
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ cycle time	t_{KCY2}		800			ns
$\overline{SCK}$ high-/low-level width	t_{KH2} t_{KL2}		400			ns
SI setup time (to $\overline{SCK}\uparrow$)	t_{SIK2}		100			ns
SI hold time (from $\overline{SCK}\uparrow$)	t_{KSI2}		400			ns
SO output delay time from $\overline{SCK}\downarrow$	t_{KSO2}	C = 100 pF**Note**			300	ns
$\overline{SCK}$ rise/fall time	t_{R2} t_{F2}				1	μs

Note C is a load capacitance of the SO output line.

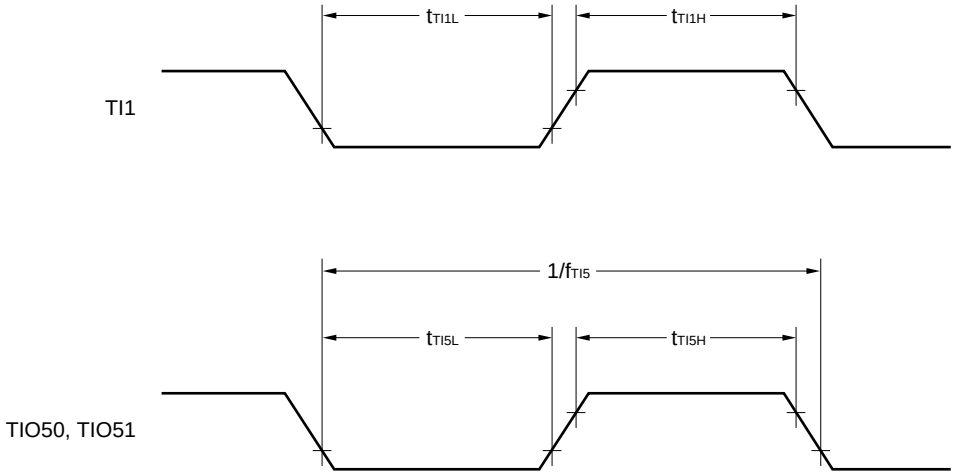
AC Timing Test Point (Excluding X1 Input)



Clock Timing

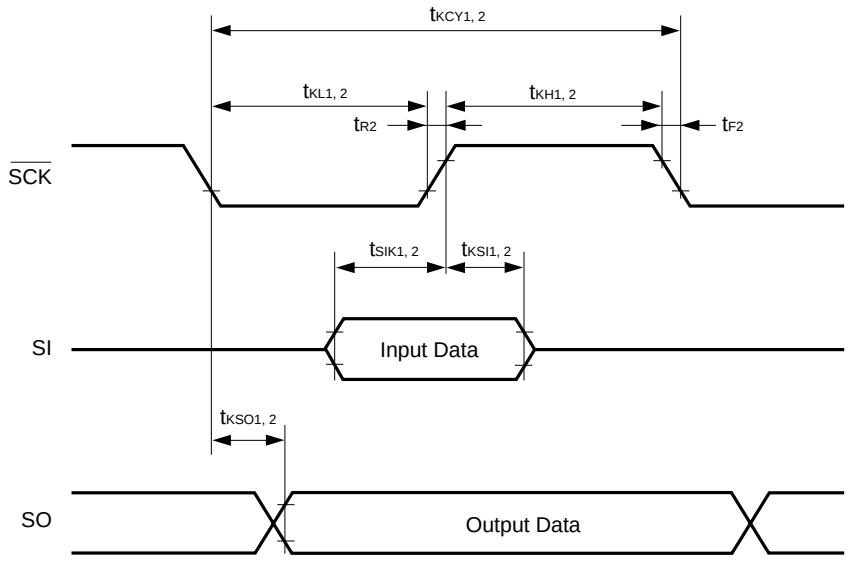


TI Timing



Serial Transfer Timing

3-Wire Serial I/O Mode:



A/D CONVERTER CHARACTERISTICS (T_A = –40 to +85°C, AV_{DD} = V_{DD} = 4.0 to 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution					8	bit
Total error Note 1					±1.0	%
Conversion time Note 2	t_{CONV}	1 MHz ≤ f_X ≤ 5.0 MHz	14		144	μs
Analog input voltage	V_{IAN}		AV_{SS}		AV_{DD}	V
Resistance between AV_{DD} and AV_{SS}	R_{REF}	When A/D conversion is not operated.		24.7		kΩ

Notes 1. Quantization error (±1/2LSB) is not included. This parameter is indicated as the ratio to the full-scale value.

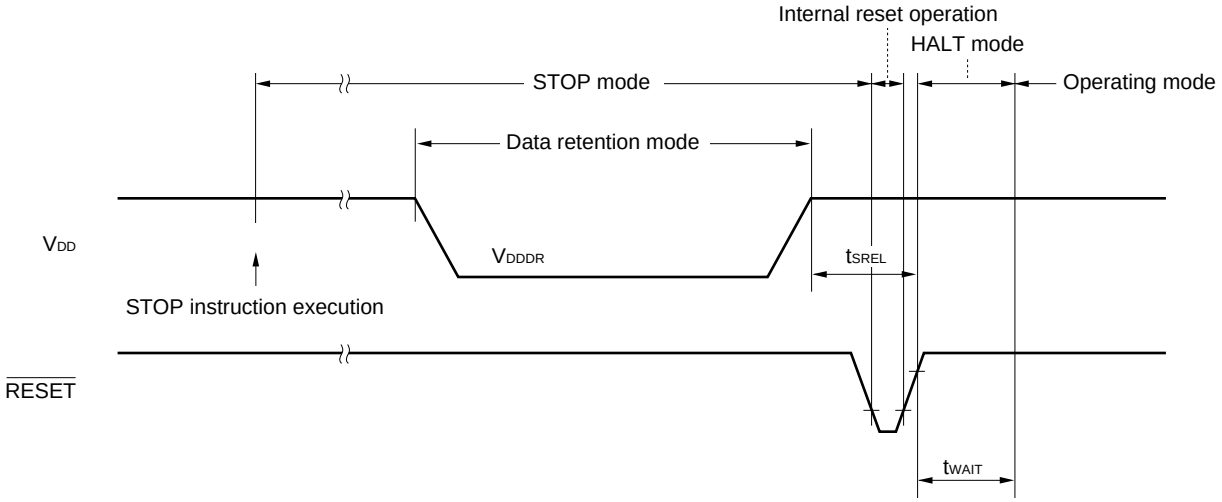
2. Set the A/D conversion time to 14 μs or more.

DATA MEMORY STOP MODE LOW SUPPLY VOLTAGE DATA RETENTION CHARACTERISTICS (T_A = –40 to +85°C)

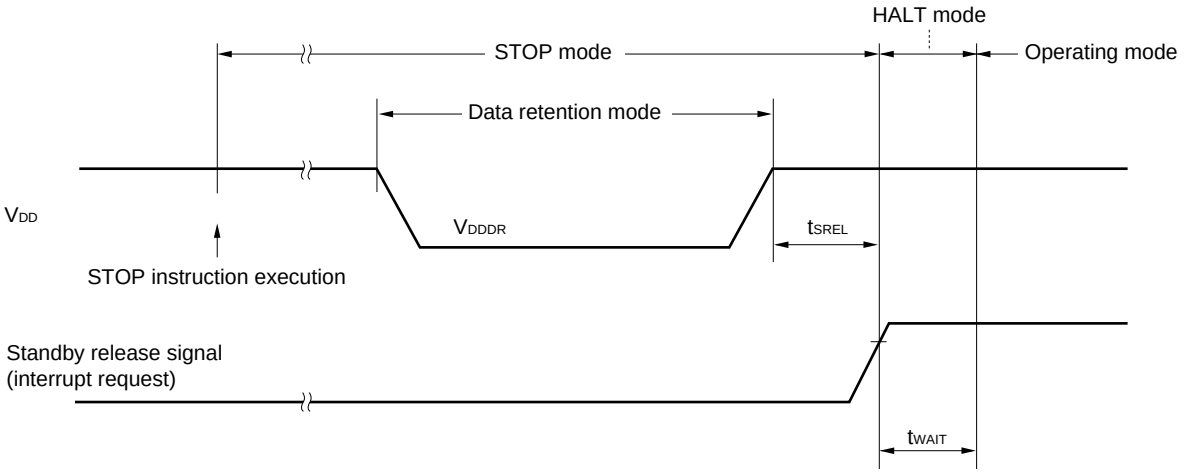
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		2.0		5.5	V
Data retention supply current	I_{DDDR}	V_{DDDR} = 2.0 V		0.1	10	μA
Release signal set time	t_{SREL}		0			μs
Oscillation stabilization wait time	t_{WAIT}	Release by $\overline{RESET}$		$2^{16}/f_X$		ms
		Release by interrupt request		**Note**		ms

Note $2^{11}/f_X$, $2^{13}/f_X$ to $2^{16}/f_X$ can be selected by bits 0 to 2 (OSTS0 to OSTS2) of oscillation stabilization time select register (OSTS).

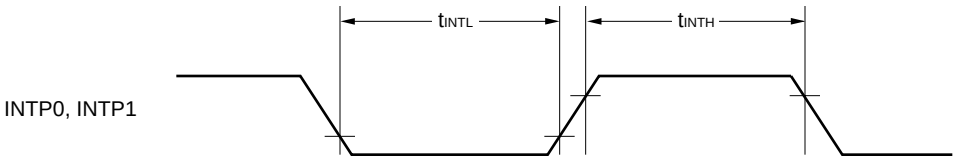
Data Retention Timing (STOP mode release by $\overline{RESET}$)



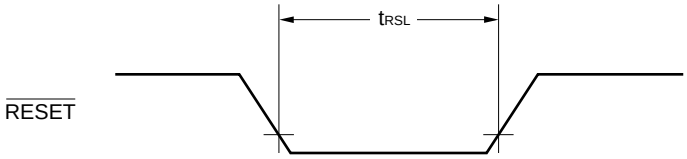
Data Retention Timing (standby release signal: STOP mode release by interrupt signal)



Interrupt Request Input Timing

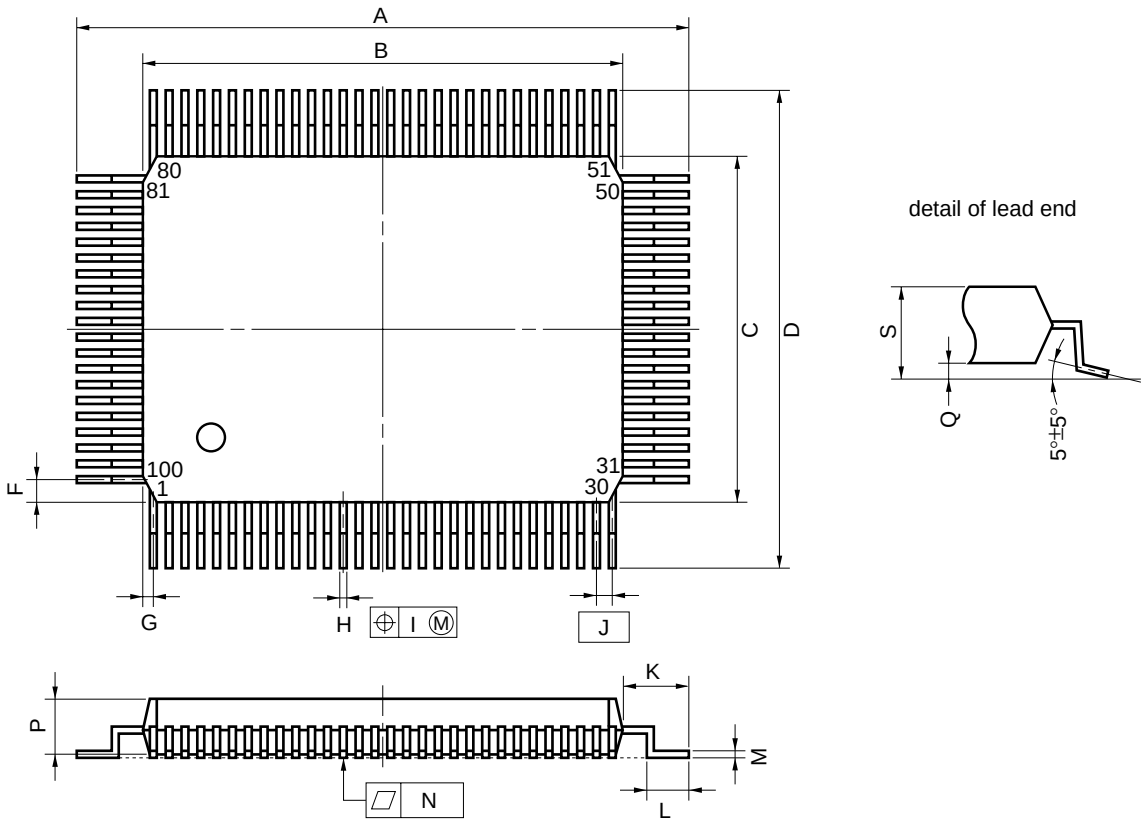


$\overline{\text{RESET}}$ Input Timing



11. PACKAGE DRAWING

100 PIN PLASTIC QFP (14 × 20)



P100GF-65-3BA1-2

NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	23.6±0.4	0.929±0.016
B	20.0±0.2	$0.795^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.6±0.4	0.693±0.016
F	0.8	0.031
G	0.6	0.024
H	$0.30^{\pm 0.10}$	$0.012^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.65 (T.P.)	0.026 (T.P.)
K	1.8±0.2	$0.071^{+0.008}_{-0.009}$
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
S	3.0 MAX.	0.119 MAX.

★ **Remark** The shape and material of the ES version are the same as those of the corresponding mass-produced product.

★ 12. RECOMMENDED SOLDERING CONDITIONS

The conditions listed below shall be met when soldering the μPD780226 and 780228.

For details of the recommended soldering conditions, refer to the document **Semiconductor Device Mounting Technology Manual (C10535E)**.

Please consult with an NEC sales representative in case any other soldering process is used, or in case soldering is done under different conditions.

Table 12-1. Soldering Conditions for Surface-Mount Type

μPD780226GF-×××-3BA: 100-pin plastic QFP (14 × 20 mm)
μPD780228GF-×××-3BA: 100-pin plastic QFP (14 × 20 mm)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Duration: 30 sec. max. (at 210°C or above), Number of times: Thrice max.	IR35-00-3
VPS	Package peak temperature: 215°C, Duration: 40 sec. max. (at 200°C or above), Number of times: Thrice max.	VP15-00-3
Wave soldering	Solder bath temperature: 260°C max. Duration: 10 sec. max. Number of times: Once Preliminary heat temperature: 120°C max. (Package surface temperature)	WS60-00-1
Partial heating	Pin temperature: 300°C max., Duration: 3 sec. max. (per device side)	—

Caution Using more than one soldering method should be avoided (except in the case of partial heating).

APPENDIX A. DEVELOPMENT TOOLS

The following development tools are available for system development using the μPD780226, 780228.

Language Processing Software

RA78K/0 Notes 1, 2, 3, 4	78K/0 Series common assembler package
CC78K/0 Notes 1, 2, 3, 4	78K/0 Series common C compiler package
DF780228 Notes 1, 2, 3, 4, 8	μPD780228 Subseries common device file
CC78K/0-L Notes 1, 2, 3, 4	78K/0 Series common C compiler library source file

★ Flash Memory Writing Tools

Flashpro II (type number FL-PR2)	Dedicated flash memory writer
FA-100GF	Adapter to write data to the flash memory

★ Debugging Tools

IE-78001-R-A Note 8	78K/0 Series common in-circuit emulator
IE-78K0-SL-P01 Note 8	I/O board to emulate the μPD780228 Subseries product
IE-780228-SL-EM4 Note 8	Probe board to emulate the μPD780228 Subseries product
EP-100GF-SL	Emulation probe for 100-pin plastic QFP (GF-3BA type)
NQPACK100RB	Coversion socket for 100-pin plastic QFP (GF-3BA type) to mount a device on a target system board
YQPACK100RB	Adapter used to connect the NQPACK100RB with the EP-100GF-SL
HQPACK100RB	Cover of the NQPACK100RB when device is mounted
SM78K/0 Notes 5, 6, 7	78K/0 Series common system simulator
ID78K0 Notes 4, 5, 6, 7	IE-78001-R-A integrated debugger
DF780228 Notes 4, 5, 6, 7, 8	μPD780228 Subseries common device file

Notes 1. PC-9800 Series (MS-DOS™) based
2. IBM PC/AT™ and compatibles (PC DOS™/IBM DOS™/MS-DOS) based
3. HP9000 Series 300™ (HP-UX™) based
4. HP9000 Series 700™ (HP-UX) based, SPARCstation™ (SunOS™) based, EWS-4800 series (EWS-UX/V) based
5. PC-9800 Series (MS-DOS + Windows™) based
6. IBM PC/AT and compatibles (PC DOS/IBM DOS/MS-DOS + Windows) based
7. NEWS™ (NEWS-OS™) based
8. Under development

Remarks 1. The RA78K/0, CC78K/0, SM78K0, ID78K0, and RX78K/0 are used in combination with the DF780228.
2. Flashpro II and FA-100GF are products of Naitou Densei Machidaseisakusho Co., Ltd.
3. The NQPACK100RB, YQPACK100RB, and HQPACK100RB are products of TOKYO ELETECH Co., Ltd. (Tokyo (03) 5295-1661). Consult an NEC sales representative for purchase.

Real-Time OSs

RX78K/0 Notes 1, 2, 3, 4	78K/0 Series real-time OS
MX78K0 Notes 1, 2, 3, 4	78K/0 Series OS

Fuzzy Inference Development Support Systems

FE9000 Note 1, FE9200 Note 5	Fuzzy knowledge data creation tool
FT9080 Note 1, FT9085 Note 2	Translator
FI78K0 Notes 1, 2	Fuzzy inference module
FD78K0 Notes 1, 2	Fuzzy inference debugger

Notes 1. PC-9800 Series (MS-DOS) based
2. IBM PC/AT and compatibles (PC DOS/IBM DOS/MS-DOS) based
3. HP9000 Series 300 (HP-UX) based
4. HP9000 Series 700 (HP-UX) based, SPARCstation (SunOS) based, EWS-4800 Series (EWS-UX/V) based
5. IBM PC/AT and compatibles (PC DOS/IBM DOS/MS-DOS + Windows) based

APPENDIX B. RELATED DOCUMENTS

Device Related Documents

Document Name	Document No. (English)	Document No. (Japanese)
μPD780228 Subseries User's Manual	U12012E	U12012J
μPD780226, 780228 Data Sheet	This manual	U11797J
μPD78F0228 Preliminary Product Information	U11971E	U11971J
78K/0 Series User's Manual Instructions	IEU-1372	U12326J
78K/0 Series Instruction Table	—	U10903J
78K/0 Series Instruction Set	—	U10904J
★ 78K/0 Series Application Note Basics (II)	U10121E	U10121J

Development Tool Related Documents (User's Manual)

Document Name		Document No. (English)	Document No. (Japanese)
RA78K Series Assembler Package	Operation	EEU-1399	EEU-809
	Language	EEU-1404	EEU-815
RA78K Series Structured Assembler Preprocessor		EEU-1402	EEU-817
★ RA78K0 Assembler Package	Operation	U11802E	U11802J
★	Assembly Language	U11801E	U11801J
★	Structured assembly language	U11789E	U11789J
CC78K Series C Compiler	Operation	EEU-1280	EEU-656
	Language	EEU-1284	EEU-655
CC78K0 C Compiler	Operation	U11517E	U11517J
	Language	U11518E	U11518J
CC78K/0 C Compiler Application Note	Programming know-how	EEA-1208	EEA-618
CC78K Series Library Source File		—	U12322J
IE-78001-R-A		Planned	Planned
IE-78K0-SL-P01		Planned	Planned
IE-780228-SL-EM4		Planned	Planned
EP-100GF-SL		Planned	Planned
SM78K0 System Simulator Windows-based	Reference	U10181E	U10181J
SM78K Series System Simulator	External parts user open interface specifications	U10092E	U10092J
ID78K0 Integrated Debugger EWS-based	Reference	—	U11151J
ID78K0 Integrated Debugger PC-based	Reference	U11539E	U11539J
ID78K0 Integrated Debugger Windows-based	Guide	U11649E	U11649J

Caution The above related documents are subject to change without notice. Be sure to use the latest documents when starting design.

Embedded Software Related Documents (User's Manuals)

Document Name		Document No. (English)	Document No. (Japanese)
78K/0 Series Real-time OS	Basics	—	U11537J
	Installation	—	U11536J
78K/0 Series OS MX78K0	Basics	—	U12257J
Fuzzy Knowledge Data Creation Tool		EEU-1438	EEU-829
78K/0, 78K/II, 87AD Series Fuzzy Inference Development Support System Translator		EEU-1444	EEU-862
78K/0 Series Fuzzy Inference Development Support System Fuzzy Inference Module		EEU-1441	EEU-858
78K/0 Series Fuzzy Inference Development Support System Fuzzy Inference Debugger		EEU-1458	EEU-921

Other Related Documents

Document Name	Document No. (English)	Document No. (Japanese)
IC Package Manual	C10943X	
Semiconductor Device Mounting Technology Manual	C10535E	C10535J
Quality Grades on NEC Semiconductor Devices	C11531E	C11531J
NEC Semiconductor Device Reliability/Quality Control System	C10983E	C10983J
Electrostatic Discharge (ESD) Test	—	MEM-539
Guide to Quality Assurance for Semiconductor Devices	MEI-1202	C11893J
Microcomputer Product Series Guide	—	U11416J

Caution The above related documents are subject to change without notice. Be sure to use the latest documents when starting design.

[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

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Fax: 800-729-9288

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