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RENESAS

MOS INTEGRATED CIRCUIT

μPD789046

8-BIT SINGLE-CHIP MICROCONTROLLER

The μPD789046 is a μPD789046 Subseries (small-scale, general-purpose applications) product of the 78K/0S Series.

A flash memory version (μPD78F9046) that can operate within the same power supply voltage range as the mask ROM version, and various development tools are being developed.

Detailed function descriptions are provided in the following user's manuals. Be sure to read them before designing.

μPD789046 Subseries User's Manual: U13600E
78K/0S Series Instructions User's Manual: U11047E

FEATURES

- Internal ROM: 16 Kbytes
- Internal high-speed RAM: 512 bytes
- Minimum instruction execution time can be changed from high-speed (0.4 μs: @ 5.0-MHz operation with main system clock) to ultra-low-speed (122 μs: @ 32.768-kHz operation with subsystem clock)
- I/O ports: 34
- Serial interface: 1 channel
  Switchable between 3-wire serial I/O and UART modes
- Timer: 4 channels
  - 16-bit timer counter: 1 channel
  - 8-bit timer/event counter: 1 channel
  - Watch timer: 1 channel
  - Watchdog timer: 1 channel
- Vectored interrupt source: 12
- Power supply voltage: V_{DD} = 1.8 to 5.5 V
- Operating ambient temperature: T_A = −40 to +85°C

APPLICATIONS

Cordless phones, etc.

ORDERING INFORMATION

Part Number	Package
μPD789046GB-×××-8ES	44-pin plastic LQFP (10 × 10)
★ μPD789046GB-×××-8ES-A	44-pin plastic LQFP (10 × 10)

Remark 1. ××× indicates ROM code suffix.

★ **2.** Products with -A at the end of the part number are lead-free products.

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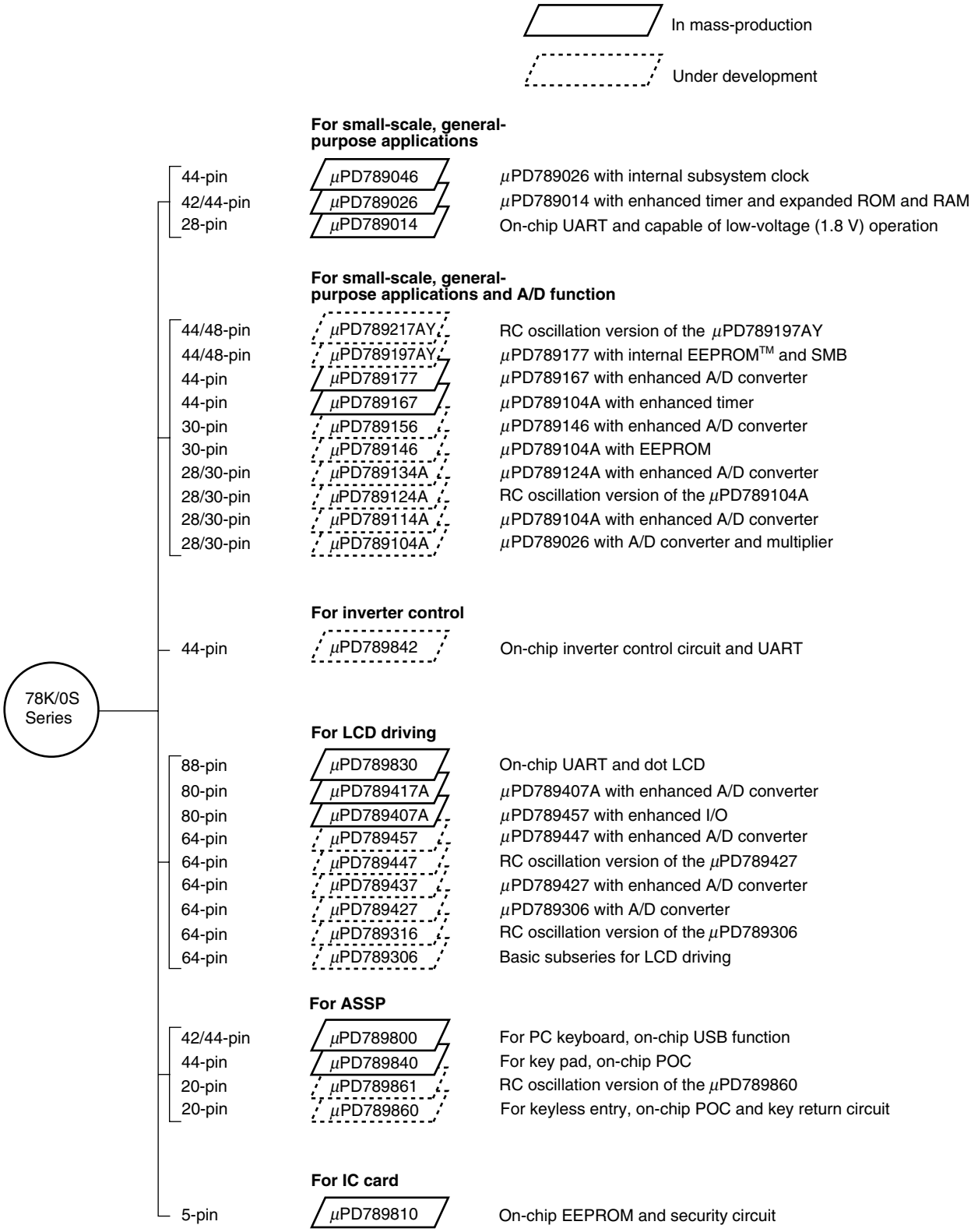
Document No. U13380EJ1V2DS00 (1st edition)
Date Published August 2005 N CP(K)
Printed in Japan

The mark ★ shows major revised points.

★ 78K/0S SERIES LINEUP

The products in the 78K/0S Series are listed below. The names enclosed in boxes are subseries names.



The major functional differences among the subseries are listed below.

Subseries Name \ Function		ROM Capacity	Timer				8-bit A/D	10-bit A/D	Serial Interface	I/O	V_{DD} Min. Value	Remarks
			8-bit	16-bit	Watch	WDT						
Small-scale, general-purpose applications	μPD789046	16 K	1 ch	1 ch	1 ch	1 ch	–	–	1 ch (UART: 1 ch)	34	1.8 V	–
	μPD789026	4 K to 16 K			–							
	μPD789014	2 K to 4 K	2 ch	–						22		
Small-scale, general-purpose applications and A/D function	μPD789217AY	16 K to 24 K	3 ch	1 ch	1 ch	1 ch	–	8 ch	2 ch UART: 1 ch SMB: 1 ch	31	1.8 V	RC oscillation version, on-chip EEPROM
	μPD789197AY											On-chip EEPROM
	μPD789177								1 ch (UART: 1 ch)			–
	μPD789167						8 ch	–				
	μPD789156	8 K to 16 K	1 ch		–		–	4 ch		20		On-chip EEPROM
	μPD789146						4 ch	–				
	μPD789134A	2 K to 8 K					–	4 ch				RC oscillation version
	μPD789124A						4 ch	–				
	μPD789114A						–	4 ch				–
	μPD789104A						4 ch	–				
Inverter control	μPD789842	8 K to 16 K	3 ch	**Note**	1 ch	1 ch	8 ch	–	1 ch (UART: 1 ch)	30	4.0 V	–
LCD driving	μPD789830	24 K	1 ch	1 ch	1 ch	1 ch	–	–	1 ch (UART: 1 ch)	30	2.7 V	–
	μPD789417A	12 K to 24 K	3 ch					7 ch		43	1.8 V	
	μPD789407A						7 ch	–		25		
	μPD789457	16 K to 24 K	2 ch				–	4 ch	2 ch (UART: 1 ch)			RC oscillation version
	μPD789447						4 ch	–				
	μPD789437						–	4 ch				–
	μPD789427						4 ch	–				
	μPD789316	8 K to 16 K					–			23		RC oscillation version
	μPD789306											–
ASSP	μPD789800	8 K	2 ch	1 ch	–	1 ch	–	–	2 ch (USB: 1 ch)	31	4.0 V	–
	μPD789840						4 ch		1 ch	29	2.8 V	
	μPD789861	4 K		–			–		–	14	1.8 V	RC oscillation version
	μPD789860											–
IC card	μPD789810	6 K	–	–	–	1 ch	–	–	–	1	2.7 V	On-chip EEPROM

Note 10-bit timer: 1 channel

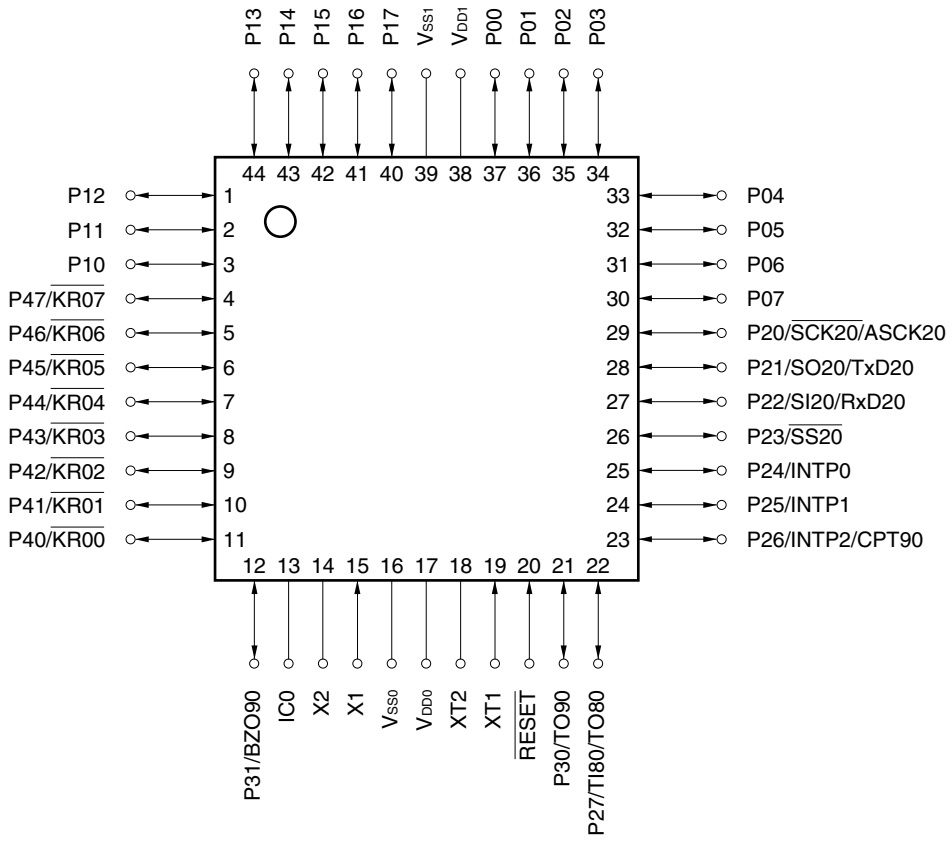
OVERVIEW OF FUNCTIONS

Item		Function
Internal memory	ROM	16 Kbytes
	High-speed RAM	512 bytes
Minimum instruction execution time		• 0.4/1.6 μs (@ 5.0-MHz operation with main system clock) • 122 μs (@ 32.768-kHz operation with subsystem clock)
General-purpose registers		8 bits × 8 registers
Instruction set		• 16-bit operation • Bit manipulation (set, reset, and test), etc.
I/O ports		CMOS input/output: 34
Serial interface		Switchable between 3-wire serial I/O and UART modes: 1 channel
Timers		• 16-bit timer counter: 1 channel • 8-bit timer/event counter: 1 channel • Watch timer: 1 channel • Watchdog timer: 1 channel
Timer output		2
Vectored interrupt sources	Maskable	Internal: 7, external: 4
	Non-maskable	Internal: 1
Power supply voltage		V_{DD} = 1.8 to 5.5 V
Operating ambient temperature		T_A = −40 to +85°C
Package		44-pin plastic LQFP (10 × 10 mm)

CONTENTS

1. PIN CONFIGURATION (Top View)

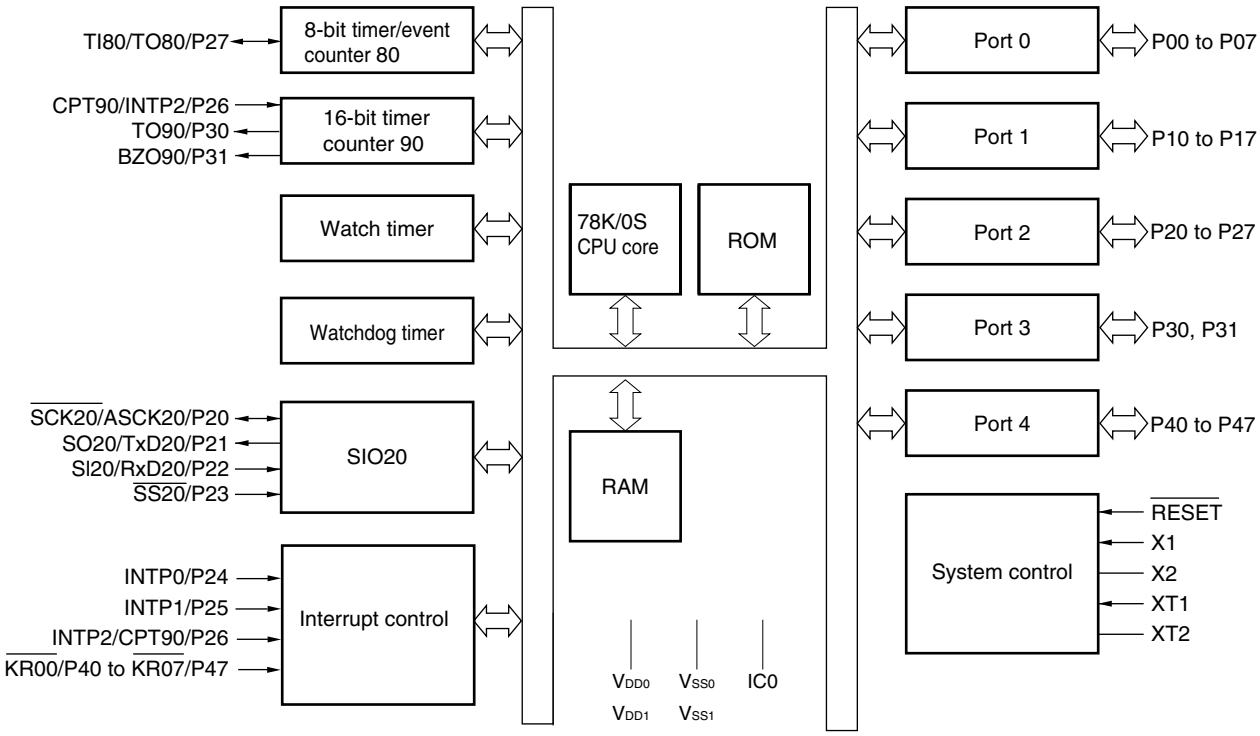
- **44-pin plastic LQFP (10 × 10)**



Caution Connect the IC0 (Internally Connected) pin directly to V_{SS0} or V_{SS1} pin.

ASCK20:	Asynchronous Serial Input
BZO90:	Buzzer Output
CPT90:	Capture Trigger Input
IC0:	Internally Connected
INTP0 to INTP2:	Interrupt from Peripherals
$\overline{KR00}$ to $\overline{KR07}$:	Key Return
P00 to P07:	Port 0
P10 to P17:	Port 1
P20 to P27:	Port 2
P30, P31:	Port 3
P40 to P47:	Port 4
$\overline{RESET}$:	Reset
RxD20:	Receive Data
$\overline{SCK20}$:	Serial Clock
SI20:	Serial Input
SO20:	Serial Output
$\overline{SS20}$:	Chip Select Input
TI80:	Timer Input
TO80, TO90:	Timer Output
TxD20:	Transmit Data
V_{DD0}, V_{DD1}:	Power Supply
V_{SS0}, V_{SS1}:	Ground
X1, X2:	Crystal (Main System Clock)
XT1, XT2:	Crystal (Subsystem Clock)

2. BLOCK DIAGRAM



3. PIN FUNCTIONS

3.1 Port Pins

Pin Name	I/O	Function	After Reset	Alternate Function
P00 to P07	I/O	Port 0 8-bit input/output port Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by means of software.	Input	–
P10 to P17	I/O	Port 1 8-bit input/output port Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by means of software.	Input	–
P20	I/O	Port 2 8-bit input/output port Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be specified by means of software.	Input	$\overline{\text{SCK20}}$/ASCK20
P21				SO20/TxD20
P22				SI20/RxD20
P23				$\overline{\text{SS20}}$
P24				INTP0
P25				INTP1
P26				INTP2/CPT90
P27				TI80/TO80
P30	I/O	Port 3 2-bit input/output port Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by means of software.	Input	TO90
P31				BZO90
P40 to P47	I/O	Port 4 8-bit input/output port Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by means of software.	Input	$\overline{\text{KR00}}$ to $\overline{\text{KR07}}$

3.2 Non-Port Pins

Pin Name	I/O	Function	After Reset	Alternate Function
INTP0	Input	External interrupt input for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified	Input	P24
INTP1				P25
INTP2				P26/CPT90
$\overline{KR00}$ to $\overline{KR07}$	Input	Detection of key return signal	Input	P40 to P47
SI20	Input	Serial interface serial data input	Input	P22/RxD20
SO20	Output	Serial interface serial data output	Input	P21/TxD20
$\overline{SCK20}$	I/O	Serial interface serial clock input/output	Input	P20/ASCK20
$\overline{SS20}$	Input	Serial interface chip select input	Input	P23
ASCK20	Input	Asynchronous serial interface serial clock input	Input	P20/$\overline{SCK20}$
RxD20	Input	Asynchronous serial interface serial data input	Input	P22/SI20
TxD20	Output	Asynchronous serial interface serial data output	Input	P21/SO20
TI80	Input	External count clock input to 8-bit timer (TM80)	Input	P27/TO80
TO80	Output	8-bit timer (TM80) output	Input	P27/TI80
TO90	Output	16-bit timer (TM90) output	Input	P30
BZO90	Output	16-bit timer (TM90) buzzer output	Input	P31
CPT90	Input	Capture edge input	Input	P26/INTP2
X1	Input	Connecting crystal resonator for main system clock oscillation	–	–
X2	–		–	–
XT1	Input	Connecting crystal resonator for subsystem clock oscillation	–	–
XT2	–		–	–
V_{DD0}	–	Positive power supply for ports	–	–
V_{DD1}	–	Positive power supply except ports	–	–
V_{SS0}	–	Ground potential for ports	–	–
V_{SS1}	–	Ground potential except ports	–	–
$\overline{RESET}$	Input	System reset input	Input	–
IC0	–	Internally connected. Connect directly to V_{SS0} or V_{SS1}.	–	–

3.3 Pin I/O Circuits and Recommended Connection of Unused Pins

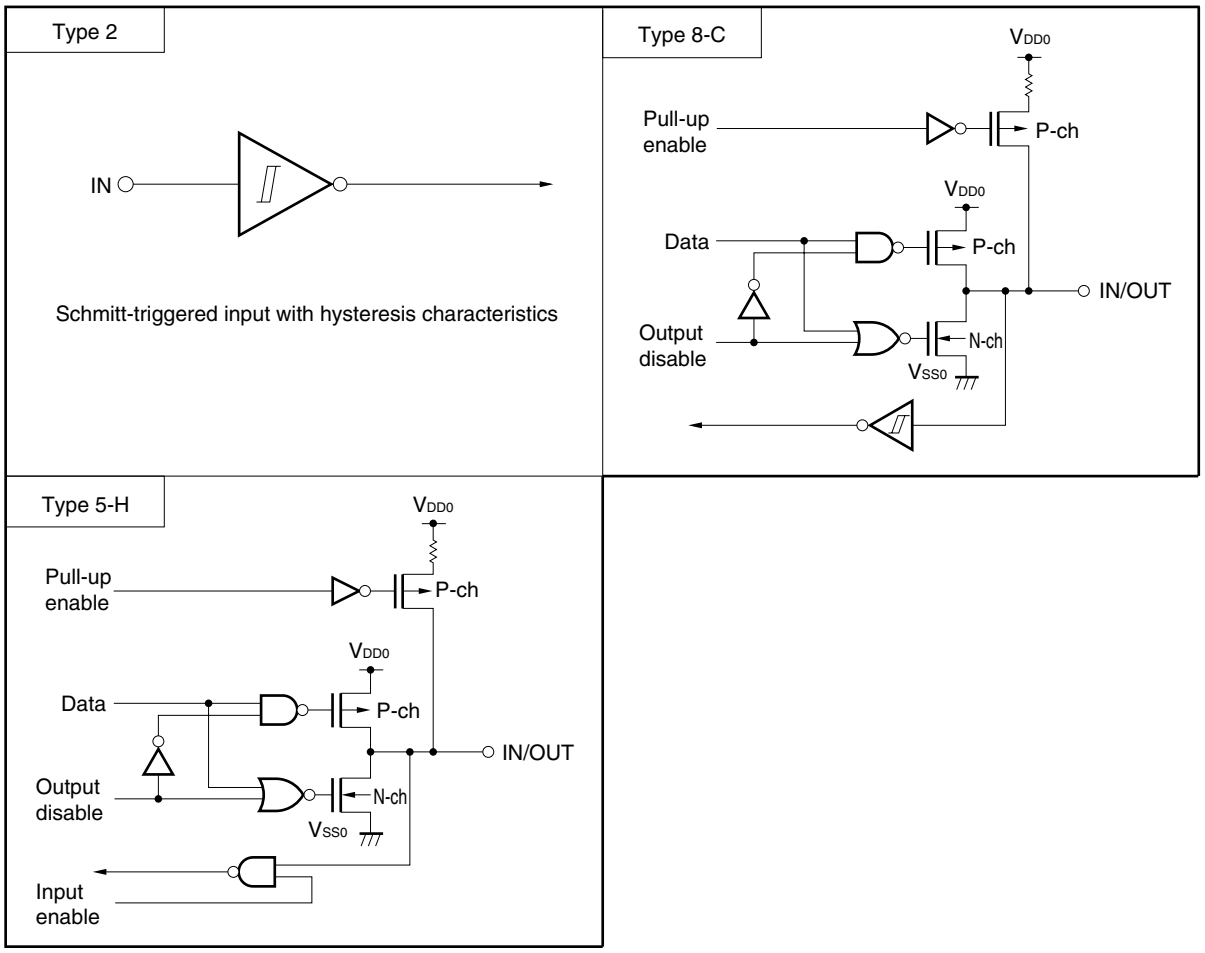
The input/output circuit type of each pin and recommended connection of unused pins are shown in Table 3-1.

For the input/output circuit configuration of each type, refer to Figure 3-1.

Table 3-1. Types of Pin Input/Output Circuits and Recommended Connection of Unused Pins

Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pins
P00 to P07	5-H	I/O	Input: Independently connect to V_{DD0}, V_{DD1}, V_{SS0}, or V_{SS1} via a resistor. Output: Leave open.
P10 to P17			
P20/$\overline{SCK20}$/ASCK20	8-C		
P21/SO20/TxD20			
P22/SI20/RxD20			
P23/$\overline{SS20}$			
P24/INTP0			
P25/INTP1			
P26/INTP2/CPT90			
P27/TI80/TO80			
P30/TO90	5-H		
P31/BZO90			
P40/$\overline{KR00}$ to P47/$\overline{KR07}$	8-C		
XT1	–	Input	Connect to V_{SS0} or V_{SS1}.
XT2		–	Leave open.
$\overline{RESET}$	2	Input	–
IC	–	–	Connect directly to V_{SS0} or V_{SS1}.

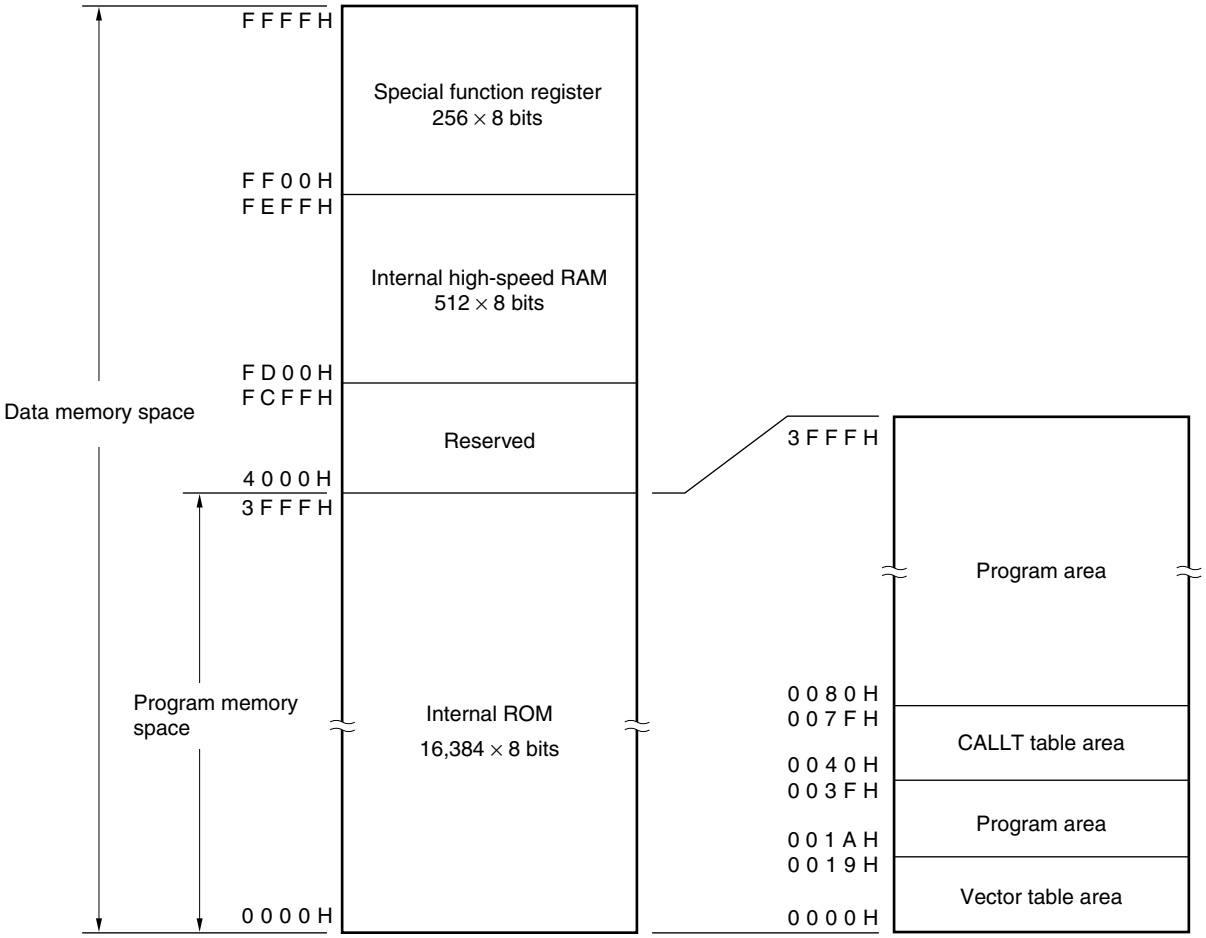
Figure 3-1. Pin Input/Output Circuits



4. MEMORY SPACE

The μPD789046 can access 64 Kbytes of memory space. Figure 4-1 shows the memory map.

Figure 4-1. Memory Map



5. PERIPHERAL HARDWARE FUNCTIONS

5.1 Ports

The μPD789046 is provided with the following I/O ports and various controls are available.

Table 5-1. Port Functions

Port Name	Pin Name	Function
Port 0	P00 to P07	Input/output port. Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by means of software.
Port 1	P10 to P17	Input/output port. Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by means of software.
Port 2	P20 to P27	Input/output port. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be specified by means of software.
Port 3	P30, P31	Input/output port. Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by means of software.
Port 4	P40 to P47	Input/output port. Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by means of software.

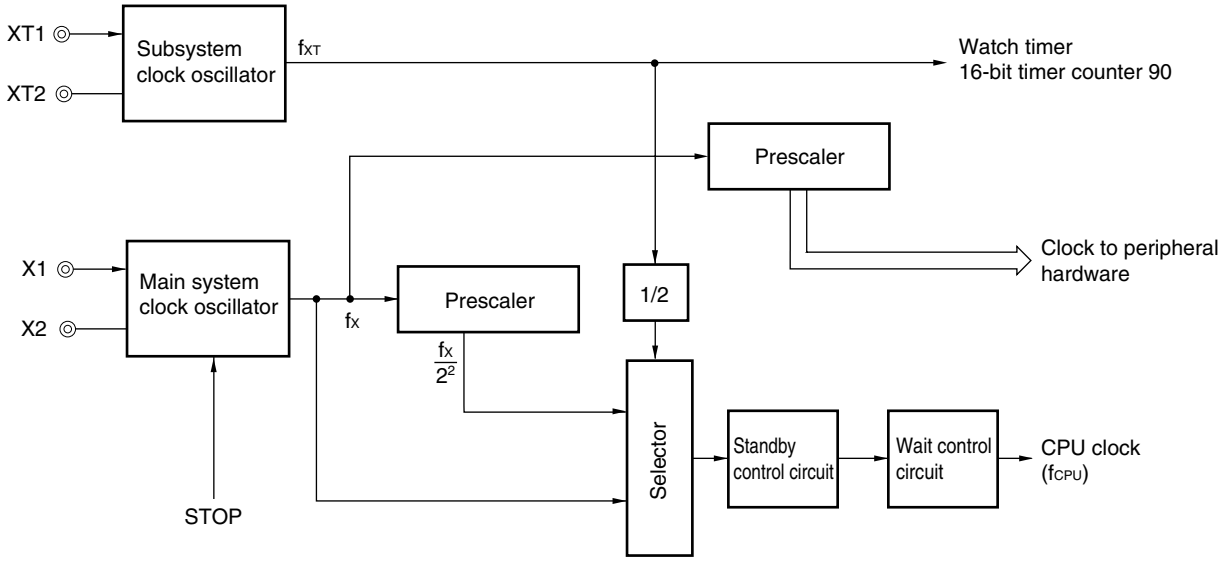
5.2 Clock Generator

A system clock generator is incorporated.

The minimum instruction execution time can be changed.

- 0.4 μs/1.6 μs (@ 5.0-MHz operation with main system clock)
- 122 μs (@ 32.768-kHz operation with subsystem clock)

Figure 5-1. Clock Generator Block Diagram



5.3 Timers

Four timer channels are incorporated.

- 16-bit timer counter 90 (TM90): 1 channel
- 8-bit timer/event counter 80 (TM80): 1 channel
- Watch timer (WT): 1 channel
- Watchdog timer (WDT): 1 channel

Table 5-2. Operations of Timers

		TM90	TM80	WT	WDT
Operation mode	Interval timer	–	1 channel	1 channel	1 channel
	External event counter	–	1 channel	–	–
Function	Timer output	1 output	1 output	–	–
	Square wave output	–	1 output	–	–
	PWM output	–	1 output	–	–
	Buzzer output	1 output	–	–	–
	Capture	1 input	–	–	–
	Interrupt request	1	1	1	1

Figure 5-2. Block Diagram of 16-Bit Timer Counter 90

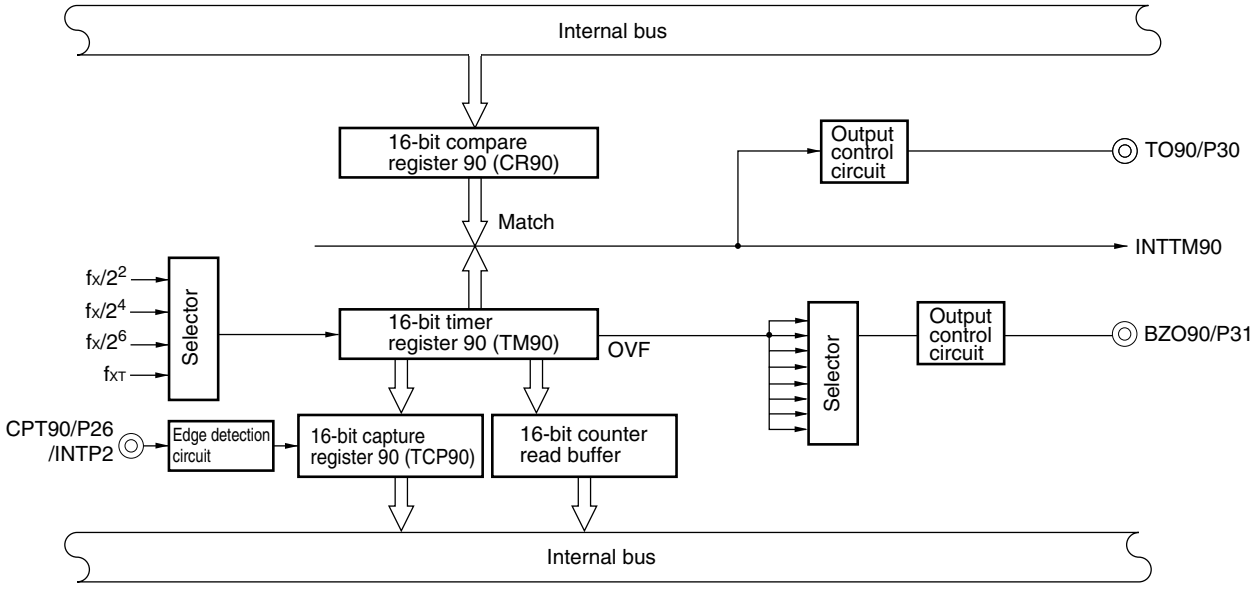


Figure 5-3. Block Diagram of 8-Bit Timer/Event Counter 80

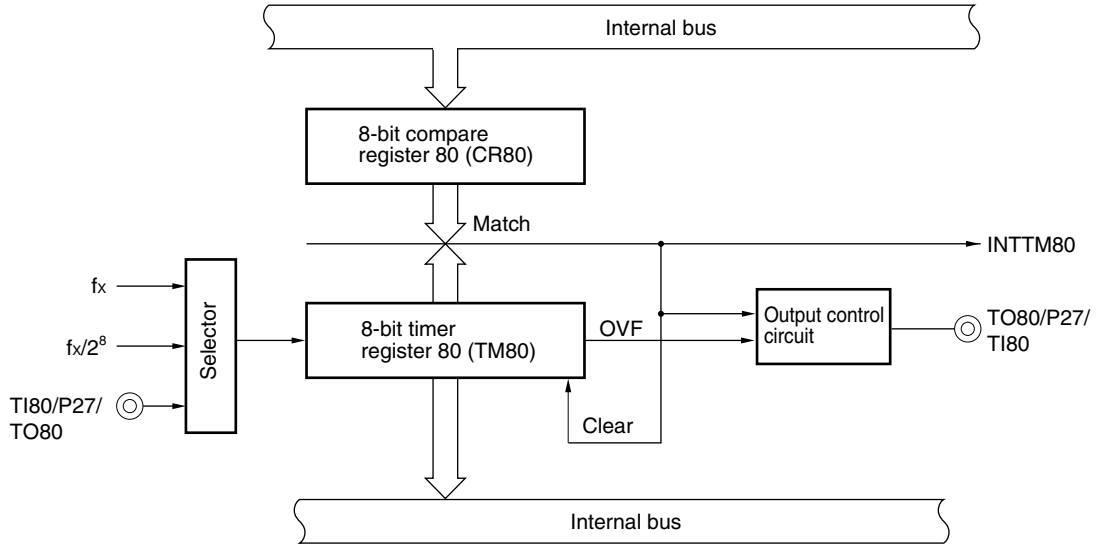
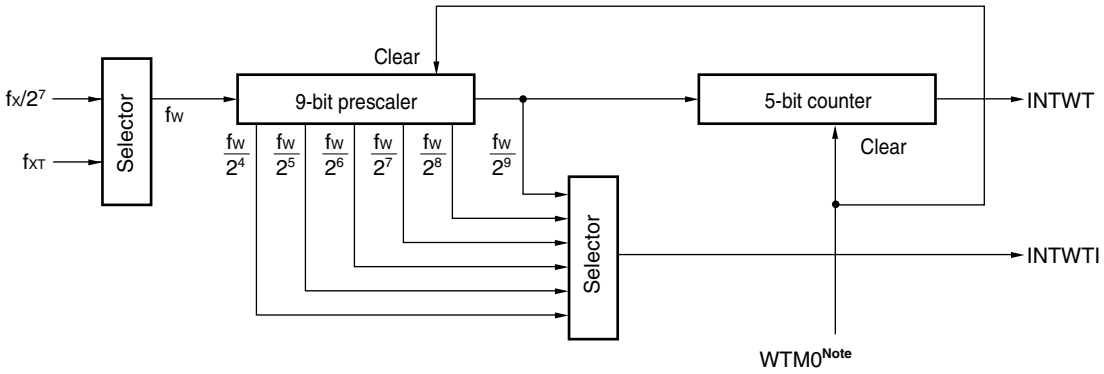
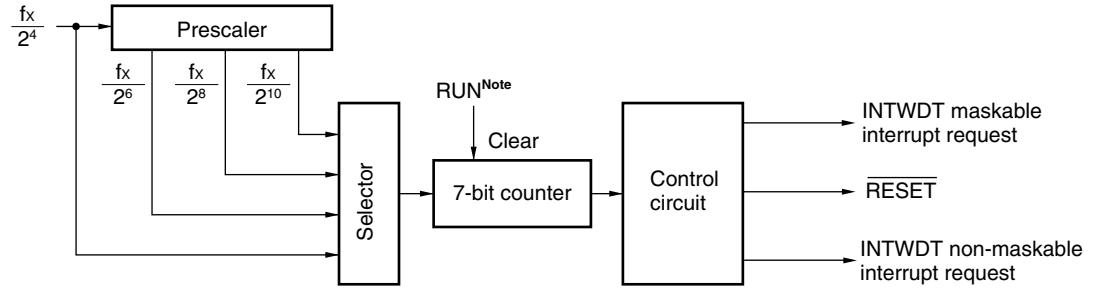


Figure 5-4. Watch Timer Block Diagram



Note Bit 0 of watch timer mode control register (WTM)

Figure 5-5. Watchdog Timer Block Diagram



Note Bit 7 of watchdog timer mode register (WDTM)

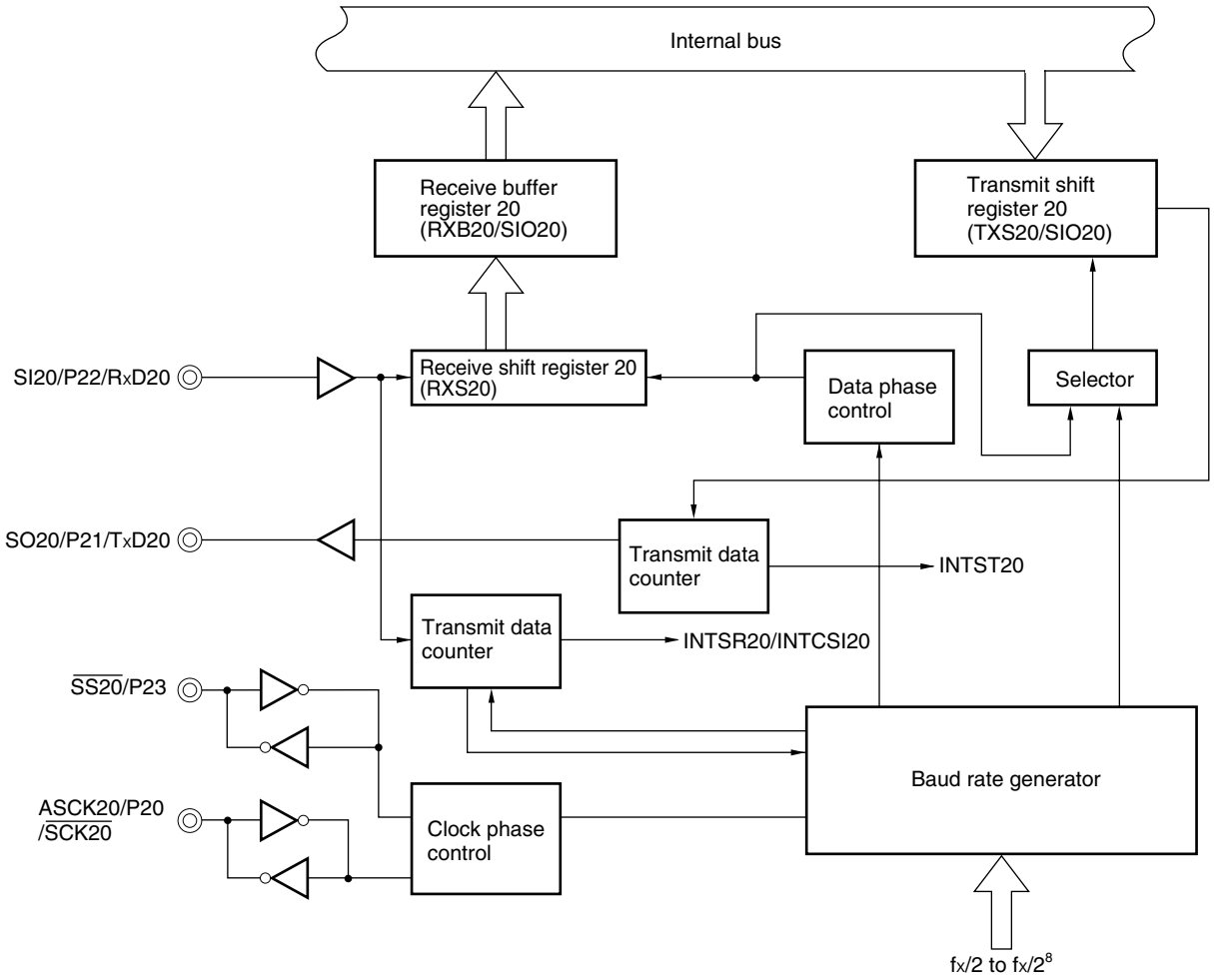
5.4 Serial Interface

One serial interface channel is incorporated.

Serial interface 20 has the following three types of modes.

- Operation stop mode: Can reduce power consumption
- 3-wire serial I/O mode: Switchable between MSB-first and LSB-first transmission
- Asynchronous serial interface (UART) mode: On-chip dedicated baud rate generator

Figure 5-6. Serial Interface Block Diagram



6. INTERRUPT FUNCTIONS

A total of 12 interrupt sources are provided, divided into the following two types.

- Non-maskable: 1
- Maskable: 11

Table 6-1. Interrupt Sources

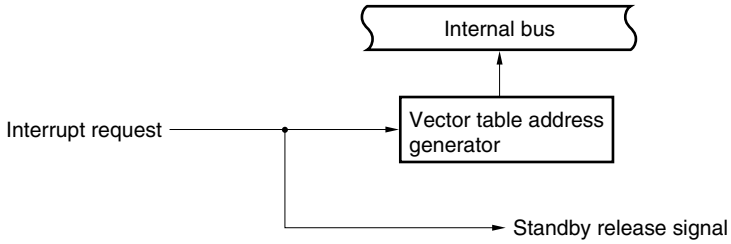
Interrupt Type	Priority[Note 1]	Interrupt Source		Internal/External	Vector Table Address	Basic Configuration Type[Note 2]
		Name	Trigger			
Non-maskable	–	INTWDT	Watchdog timer overflow (with watchdog timer mode 1 selected)	Internal	0004H	(A)
Maskable	0	INTWDT	Watchdog timer overflow (with interval timer mode selected)			(B)
	1	INTP0	Pin input edge detection	External	0006H	(C)
	2	INTP1			0008H	
	3	INTP2			000AH	
	4	INTSR20	End of serial interface 20 UART reception	Internal	000CH	(B)
		INTCSI20	End of serial interface 20 3-wire SIO transfer reception			
	5	INTST20	End of serial interface 20 UART transmission		000EH	
	6	INTWT	Watch timer interrupt		0010H	
	7	INTWTI	Interval timer interrupt		0012H	
	8	INTTM80	Generation of matching signal of 8-bit timer/event counter 80		0014H	
	9	INTTM90	Generation of matching signal of 16-bit timer counter 90		0016H	
	10	INTKR00	Detection of key return signal	External	0018H	(C)

Notes 1. Priority is the priority order when several maskable interrupts are generated at the same time. 0 is the highest order and 10 is the lowest order.

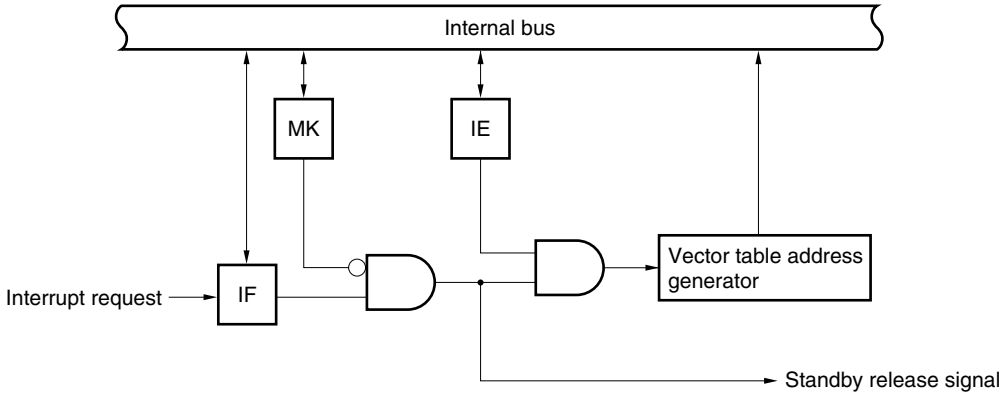
2. Basic configuration types (A) to (C) correspond to (A) to (C) in Figure 6-1.

Figure 6-1. Basic Configuration of Interrupt Functions

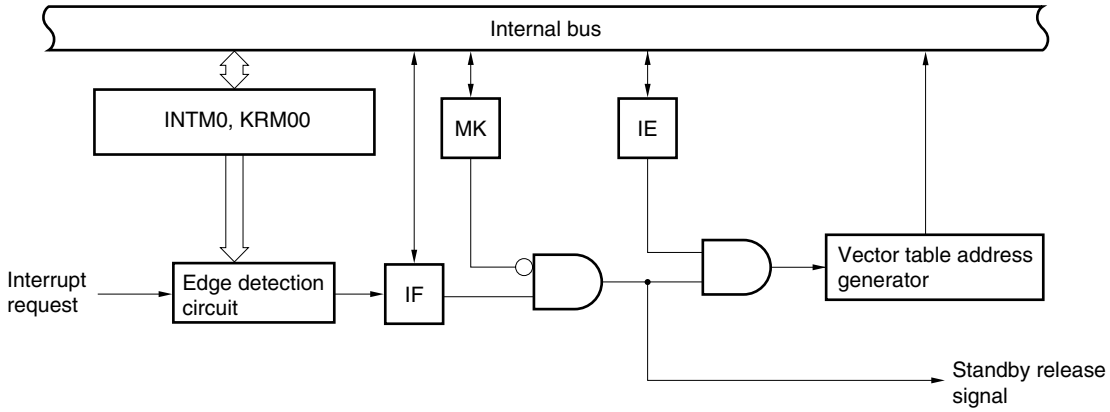
(A) Internal non-maskable interrupt



(B) Internal maskable interrupt



(C) External maskable interrupt



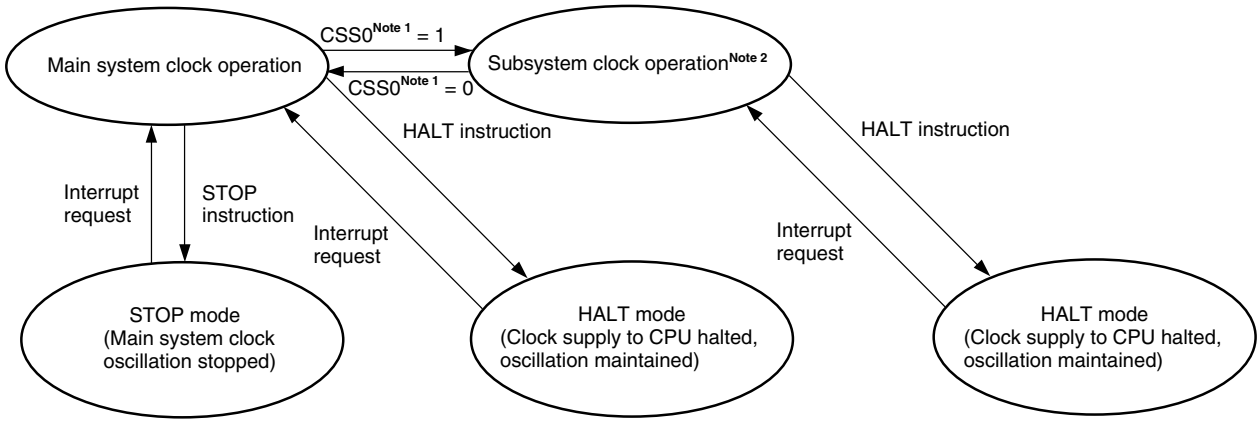
INTM0: External interrupt mode register 0
KRM00: Key return mode register 00
IF: Interrupt request flag
IE: Interrupt enable flag
MK: Interrupt mask flag

7. STANDBY FUNCTIONS

The following two standby functions are available for further reduction of system current consumption.

- HALT mode: In this mode, the CPU operation clock is stopped. The average current consumption can be reduced by intermittent operation by combining this mode with the normal operation mode.
- STOP mode: In this mode, oscillation of the main system clock is stopped. All the operations performed on the main system clock are suspended, resulting in extremely small current consumption.

Figure 7-1. Standby Functions



Notes 1. Bit 4 of subclock control register (CSS)

2. The current consumption can be reduced by stopping the main system clock. When the CPU is operating on the subsystem clock, set the bit 7 (MCC) of processor clock control register (PCC) to stop the main system clock. The STOP instruction cannot be used.

Caution When the main system clock is stopped and the device is operating on the subsystem clock, wait until the oscillation stabilization time has been secured by the program before switching back to the main system clock.

8. RESET FUNCTIONS

The following two reset methods are available.

- External reset by $\overline{\text{RESET}}$ signal input
- Internal reset by watchdog timer runaway time detection

9. INSTRUCTION SET OVERVIEW

The instruction set for the μPD789046 is listed later.

9.1 Legend

9.1.1 Operand formats and descriptions

The description made in the operand field of each instruction conforms to the operand format for the instructions listed below (the details conform with the assembler specification). If more than one operand format is listed for an instruction, one is selected. Uppercase letters, #, !, $, and a pair of [and] are used to specify keywords, which must be written exactly as they appear. The meanings of these special characters are as follows:

- #: Immediate data specification
- $: Relative address specification
- !: Absolute address specification
- [and]: Indirect address specification

Immediate data should be described using appropriate values or labels. The specification of values and labels must be accompanied by #, !, $, or a pair of [and].

Operand registers, expressed as r or rp in the formats, can be described using both functional names (X, A, C, etc.) and absolute names (R0, R1, R2, and other names listed in Table 9-1).

Table 9-1. Operand Formats and Descriptions

Format	Description
r rp sfr	X (R0), A (R1), C (R2), B (R3), E (R4), D (R5), L (R6), H (R7) AX (RP0), BC (RP1), DE (RP2), HL (RP3) Special function register symbol
saddr saddrp	FE20H to FF1FH: Immediate data or label FE20H to FF1FH: Immediate data or label (even addresses only)
addr16 addr5	0000H to FFFFH: Immediate data or label (only even addresses for 16-bit data transfer instructions) 0040H to 007FH: Immediate data or label (even addresses only)
word byte bit	16-bit immediate data or label 8-bit immediate data or label 3-bit immediate data or label

9.1.2 Descriptions of operation field

A : A register; 8-bit accumulator
X : X register
B : B register
C : C register
D : D register
E : E register
H : H register
L : L register
AX : AX register pair; 16-bit accumulator
BC : BC register pair
DE : DE register pair
HL : HL register pair
PC : Program counter
SP : Stack pointer
PSW : Program status word
CY : Carry flag
AC : Auxiliary carry flag
Z : Zero flag
IE : Interrupt request enable flag
NMIS : Flag to indicate that a non-maskable interrupt is being handled
( ) : Contents of a memory location indicated by a parenthesized address or register
X_H, X_L : Higher and lower 8 bits of a 16-bit register
^ : Logical product (AND)
∨ : Logical sum (OR)
$\veebar$: Exclusive OR
— : Inverted data
addr16 : 16-bit immediate data or label
jdisp8 : Signed 8-bit data (displacement value)

9.1.3 Descriptions of flag operation field

(blank) : No change
0 : To be cleared to 0
1 : To be set to 1
× : To be set or cleared according to the result
R : To be restored to the previous value

9.2 Operations

Mnemonic	Operand	Byte	Clock	Operation	Flag		
					Z	AC	CY
MOV	r, #byte	3	6	r ← byte			
	saddr, #byte	3	6	(saddr) ← byte			
	sfr, #byte	3	6	sfr ← byte			
	A, r Note 1	2	4	A ← r			
	r, A Note 1	2	4	r ← A			
	A, saddr	2	4	A ← (saddr)			
	saddr, A	2	4	(saddr) ← A			
	A, sfr	2	4	A ← sfr			
	sfr, A	2	4	sfr ← A			
	A, !addr16	3	8	A ← (addr16)			
	!addr16, A	3	8	(addr16) ← A			
	PSW, #byte	3	6	PSW ← byte	×	×	×
	A, PSW	2	4	A ← PSW			
	PSW, A	2	4	PSW ← A	×	×	×
	A, [DE]	1	6	A ← (DE)			
	[DE], A	1	6	(DE) ← A			
	A, [HL]	1	6	A ← (HL)			
	[HL], A	1	6	(HL) ← A			
	A, [HL + byte]	2	6	A ← (HL + byte)			
	[HL + byte], A	2	6	(HL + byte) ← A			
XCH	A, X	1	4	A ↔ X			
	A, r Note 2	2	6	A ↔ r			
	A, saddr	2	6	A ↔ (saddr)			
	A, sfr	2	6	A ↔ (sfr)			
	A, [DE]	1	8	A ↔ (DE)			
	A, [HL]	1	8	A ↔ (HL)			
	A, [HL + byte]	2	8	A ↔ (HL + byte)			
MOVW	rp, #word	3	6	rp ← word			
	AX, saddrp	2	6	AX ← (saddrp)			
	saddrp, AX	2	8	(saddrp) ← AX			
	AX, rp Note 3	1	4	AX ← rp			
	rp, AX Note 3	1	4	rp ← AX			

Notes 1. Except when r = A.

2. Except when r = A or X.

3. Only when rp = BC, DE, or HL.

Remark The instruction clock cycle is based on the CPU clock (f_{CPU}), specified in the processor clock control register (PCC).

Mnemonic	Operand	Byte	Clock	Operation	Flag		
					Z	AC	CY
XCHW	AX, rp Note	1	8	AX ↔ rp			
ADD	A, #byte	2	4	A, CY ← A + byte	×	×	×
	saddr, #byte	3	6	(saddr), CY ← (saddr) + byte	×	×	×
	A, r	2	4	A, CY ← A + r	×	×	×
	A, saddr	2	4	A, CY ← A + (saddr)	×	×	×
	A, !addr16	3	8	A, CY ← A + (addr16)	×	×	×
	A, [HL]	1	6	A, CY ← A + (HL)	×	×	×
	A, [HL + byte]	2	6	A, CY ← A + (HL + byte)	×	×	×
ADDC	A, #byte	2	4	A, CY ← A + byte + CY	×	×	×
	saddr, #byte	3	6	(saddr), CY ← (saddr) + byte + CY	×	×	×
	A, r	2	4	A, CY ← A + r + CY	×	×	×
	A, saddr	2	4	A, CY ← A + (saddr) + CY	×	×	×
	A, !addr16	3	8	A, CY ← A + (addr16) + CY	×	×	×
	A, [HL]	1	6	A, CY ← A + (HL) + CY	×	×	×
	A, [HL + byte]	2	6	A, CY ← A + (HL + byte) + CY	×	×	×
SUB	A, #byte	2	4	A, CY ← A – byte	×	×	×
	saddr, #byte	3	6	(saddr), CY ← (saddr) – byte	×	×	×
	A, r	2	4	A, CY ← A – r	×	×	×
	A, saddr	2	4	A, CY ← A – (saddr)	×	×	×
	A, !addr16	3	8	A, CY ← A – (addr16)	×	×	×
	A, [HL]	1	6	A, CY ← A – (HL)	×	×	×
	A, [HL + byte]	2	6	A, CY ← A – (HL + byte)	×	×	×
SUBC	A, #byte	2	4	A, CY ← A – byte – CY	×	×	×
	saddr, #byte	3	6	(saddr), CY ← (saddr) – byte – CY	×	×	×
	A, r	2	4	A, CY ← A – r – CY	×	×	×
	A, saddr	2	4	A, CY ← A – (saddr) – CY	×	×	×
	A, !addr16	3	8	A, CY ← A – (addr16) – CY	×	×	×
	A, [HL]	1	6	A, CY ← A – (HL) – CY	×	×	×
	A, [HL + byte]	2	6	A, CY ← A – (HL + byte) – CY	×	×	×
AND	A, #byte	2	4	A ← A ∧ byte	×		
	saddr, #byte	3	6	(saddr) ← (saddr) ∧ byte	×		
	A, r	2	4	A ← A ∧ r	×		
	A, saddr	2	4	A ← A ∧ (saddr)	×		
	A, !addr16	3	8	A ← A ∧ (addr16)	×		
	A, [HL]	1	6	A ← A ∧ (HL)	×		
	A, [HL + byte]	2	6	A ← A ∧ (HL + byte)	×		

Note Only when rp = BC, DE, or HL.

Remark The instruction clock cycle is based on the CPU clock (f_{CPU}), specified in the processor clock control register (PCC).

Mnemonic	Operand	Byte	Clock	Operation	Flag		
					Z	AC	CY
OR	A, #byte	2	4	A ← A ∨ byte	×		
	saddr, #byte	3	6	(saddr) ← (saddr) ∨ byte	×		
	A, r	2	4	A ← A ∨ r	×		
	A, saddr	2	4	A ← A ∨ (saddr)	×		
	A, !addr16	3	8	A ← A ∨ (addr16)	×		
	A, [HL]	1	6	A ← A ∨ (HL)	×		
	A, [HL + byte]	2	6	A ← A ∨ (HL + byte)	×		
XOR	A, #byte	2	4	A ← A ⊻ byte	×		
	saddr, #byte	3	6	(saddr) ← (saddr) ⊻ byte	×		
	A, r	2	4	A ← A ⊻ r	×		
	A, saddr	2	4	A ← A ⊻ (saddr)	×		
	A, !addr16	3	8	A ← A ⊻ (addr16)	×		
	A, [HL]	1	6	A ← A ⊻ (HL)	×		
	A, [HL + byte]	2	6	A ← A ⊻ (HL + byte)	×		
CMP	A, #byte	2	4	A – byte	×	×	×
	saddr, #byte	3	6	(saddr) – byte	×	×	×
	A, r	2	4	A – r	×	×	×
	A, saddr	2	4	A – (saddr)	×	×	×
	A, !addr16	3	8	A – (addr16)	×	×	×
	A, [HL]	1	6	A – (HL)	×	×	×
	A, [HL + byte]	2	6	A – (HL + byte)	×	×	×
ADDW	AX, #word	3	6	AX, CY ← AX + word	×	×	×
SUBW	AX, #word	3	6	AX, CY ← AX – word	×	×	×
CMPW	AX, #word	3	6	AX – word	×	×	×
INC	r	2	4	r ← r + 1	×	×	
	saddr	2	4	(saddr) ← (saddr) + 1	×	×	
DEC	r	2	4	r ← r – 1	×	×	
	saddr	2	4	(saddr) ← (saddr) – 1	×	×	
INCW	rp	1	4	rp ← rp + 1			
DECW	rp	1	4	rp ← rp – 1			
ROR	A, 1	1	2	$(CY, A_7 \leftarrow A_0, A_{m-1} \leftarrow A_m) \times 1$			×
ROL	A, 1	1	2	$(CY, A_0 \leftarrow A_7, A_{m+1} \leftarrow A_m) \times 1$			×
RORC	A, 1	1	2	$(CY \leftarrow A_0, A_7 \leftarrow CY, A_{m-1} \leftarrow A_m) \times 1$			×
ROLC	A, 1	1	2	$(CY \leftarrow A_7, A_0 \leftarrow CY, A_{m+1} \leftarrow A_m) \times 1$			×

Remark The instruction clock cycle is based on the CPU clock (f_{CPU}), specified in the processor clock control register (PCC).

Mnemonic	Operand	Byte	Clock	Operation	Flag		
					Z	AC	CY
SET1	saddr. bit	3	6	(saddr. bit) ← 1			
	sfr. bit	3	6	sfr. bit ← 1			
	A. bit	2	4	A. bit ← 1			
	PSW. bit	3	6	PSW. bit ← 1	×	×	×
	[HL]. bit	2	10	(HL). bit ← 1			
CLR1	saddr. bit	3	6	(saddr. bit) ← 0			
	sfr. bit	3	6	sfr. bit ← 0			
	A. bit	2	4	A. bit ← 0			
	PSW. bit	3	6	PSW. bit ← 0	×	×	×
	[HL]. bit	2	10	(HL). bit ← 0			
SET1	CY	1	2	CY ← 1			1
CLR1	CY	1	2	CY ← 0			0
NOT1	CY	1	2	CY ← $\overline{CY}$			×
CALL	!addr16	3	6	(SP – 1) ← (PC + 3)$_H$, (SP – 2) ← (PC + 3)$_L$, PC ← addr16, SP ← SP – 2			
CALLT	[addr5]	1	8	(SP – 1) ← (PC + 1)$_H$, (SP – 2) ← (PC + 1)$_L$, PC$_H$ ← (00000000, addr5 + 1), PC$_L$ ← (00000000, addr5), SP ← SP – 2			
RET		1	6	PC$_H$ ← (SP + 1), PC$_L$ ← (SP), SP ← SP + 2			
RETI		1	8	PC$_H$ ← (SP + 1), PC$_L$ ← (SP), PSW ← (SP + 2), SP ← SP + 3, NMIS ← 0	R	R	R
PUSH	PSW	1	2	(SP – 1) ← PSW, SP ← SP – 1			
	rp	1	4	(SP – 1) ← rp$_H$, (SP – 2) ← rp$_L$, SP ← SP – 2			
POP	PSW	1	4	PSW ← (SP), SP ← SP + 1	R	R	R
	rp	1	6	rp$_H$ ← (SP + 1), rp$_L$ ← (SP), SP ← SP + 2			
MOVW	SP, AX	2	8	SP ← AX			
	AX, SP	2	6	AX ← SP			
BR	!addr16	3	6	PC ← addr16			
	$addr16	2	6	PC ← PC + 2 + jdisp8			
	AX	1	6	PC$_H$ ← A, PC$_L$ ← X			

Remark The instruction clock cycle is based on the CPU clock (f$_{CPU}$), specified in the processor clock control register (PCC).

Mnemonic	Operand	Byte	Clock	Operation	Flag
					Z AC CY
BC	$addr16	2	6	PC ← PC + 2 + jdisp8 if CY = 1	
BNC	$addr16	2	6	PC ← PC + 2 + jdisp8 if CY = 0	
BZ	$addr16	2	6	PC ← PC + 2 + jdisp8 if Z = 1	
BNZ	$addr16	2	6	PC ← PC + 2 + jdisp8 if Z = 0	
BT	saddr. bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if (saddr. bit) = 1	
	sfr. bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if sfr. bit = 1	
	A. bit, $addr16	3	8	PC ← PC + 3 + jdisp8 if A. bit = 1	
	PSW. bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if PSW. bit = 1	
BF	saddr. bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if (saddr. bit) = 0	
	sfr. bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if sfr. bit = 0	
	A. bit, $addr16	3	8	PC ← PC + 3 + jdisp8 if A. bit = 0	
	PSW. bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if PSW. bit = 0	
DBNZ	B, $addr16	2	6	B ← B – 1, then PC ← PC + 2 + jdisp8 if B ≠ 0	
	C, $addr16	2	6	C ← C – 1, then PC ← PC + 2 + jdisp8 if C ≠ 0	
	saddr, $addr16	3	8	(saddr) ← (saddr) – 1, then PC ← PC + 3 + jdisp8 if (saddr) ≠ 0	
NOP		1	2	No Operation	
EI		3	6	IE ← 1 (Enable Interrupt)	
DI		3	6	IE ← 0 (Disable Interrupt)	
HALT		1	2	Set HALT Mode	
STOP		1	2	Set STOP Mode	

Remark The instruction clock cycle is based on the CPU clock (f_{CPU}), specified in the processor clock control register (PCC).

★ 10. ELECTRICAL SPECIFICATIONS

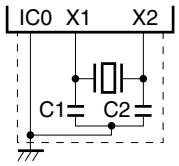
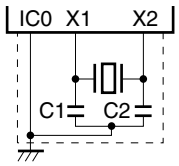
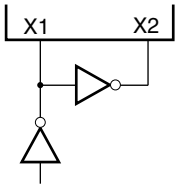
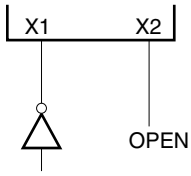
Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD}		−0.3 to +6.5	V
Input voltage	V_I		−0.3 to V_{DD} + 0.3	V
Output voltage	V_O		−0.3 to V_{DD} + 0.3	V
Output current, high	I_{OH}	Per pin	−10	mA
		Total for all pins	−30	mA
Output current, low	I_{OL}	Per pin	30	mA
		Total for all pins	160	mA
Operating ambient temperature	T_A		−40 to +85	°C
Storage temperature	T_{stg}		−65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

Main System Clock Oscillator Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f_X) Note 1	V_{DD} = oscillation voltage range	1.0		5.0	MHz
		Oscillation stabilization time Note 2	After V_{DD} reaches oscillation voltage range MIN.			4	ms
Crystal resonator		Oscillation frequency (f_X) Note 1		1.0		5.0	MHz
		Oscillation stabilization time Note 2	V_{DD} = 4.5 to 5.5 V			10	ms
						30	
External clock		X1 input frequency (f_X) Note 1		1.0		5.0	MHz
		X1 input high-/low-level width (t_{XH}, t_{XL})		85		500	ns
		X1 input frequency (f_X) Note 1	V_{DD} = 2.7 to 5.5 V	1.0		5.0	MHz
		X1 input high-/low-level width (t_{XH}, t_{XL})	V_{DD} = 2.7 to 5.5 V	85		500	ns

Notes 1. Indicates only oscillator characteristics. Refer to AC Characteristics for instruction execution time.

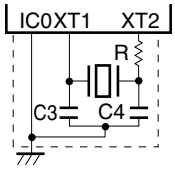
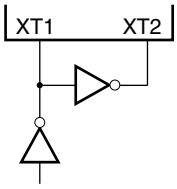
2. Time required to stabilize oscillation after reset or STOP mode release. Use the resonator that stabilizes oscillation within the oscillation wait time.

Cautions 1. When using the main system clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS0}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. When the main system clock is stopped and the device is operating on the subsystem clock, wait until the oscillation stabilization time has been secured by the program before switching back to the main system clock.

Subsystem Clock Oscillator Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		Oscillation frequency (f_{XT}) Note 1		32	32.768	35	kHz
		Oscillation stabilization time Note 2	V_{DD} = 4.5 to 5.5 V		1.2	2	s
						10	
External clock		XT1 input frequency (f_{XT}) Note 1		32		35	kHz
		XT1 input high-/low-level width (t_{XTH}, t_{XTL})		14.3		15.6	μs

Notes 1. Indicates only oscillator characteristics. Refer to AC Characteristics for instruction execution time.

2. Time required to stabilize oscillation after reset or STOP mode release. Use the resonator that stabilizes oscillation within the oscillation wait time.

Cautions 1. When using the subsystem clock oscillator, wire as follows in the area enclosed by the broken lines in the above figure to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS0}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. The subsystem clock oscillator is designed as a low-amplitude circuit for reducing current consumption, and is more prone to malfunction due to noise than the main system clock oscillator. Particular care is therefore required with the wiring method when the subsystem clock is used.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high	I_{OH}	Per pin				–1	mA
		Total for all pins				–15	mA
Output current, low	I_{OL}	Per pin				10	mA
		Total for all pins				80	mA
Input voltage, high	V_{IH1}	P00 to P07, P10 to P17, P30, P31	V_{DD} = 2.7 to 5.5 V	0.7V_{DD}		V_{DD}	V
				0.9V_{DD}		V_{DD}	V
	V_{IH2}	$\overline{\text{RESET}}$, P20 to P27, P40 to P47	V_{DD} = 2.7 to 5.5 V	0.8V_{DD}		V_{DD}	V
				0.9V_{DD}		V_{DD}	V
	V_{IH3}	X1, X2	V_{DD} = 4.5 to 5.5 V	V_{DD} – 0.5		V_{DD}	V
				V_{DD} – 0.1		V_{DD}	V
	V_{IH4}	XT1, XT2	V_{DD} = 4.5 to 5.5 V	V_{DD} – 0.5		V_{DD}	V
				V_{DD} – 0.1		V_{DD}	V
Input voltage, low	V_{IL1}	P00 to P07, P10 to P17, P30, P31	V_{DD} = 2.7 to 5.5 V	0		0.3V_{DD}	V
				0		0.1V_{DD}	V
	V_{IL2}	$\overline{\text{RESET}}$, P20 to P27, P40 to P47	V_{DD} = 2.7 to 5.5 V	0		0.2V_{DD}	V
				0		0.1V_{DD}	V
	V_{IL3}	X1, X2	V_{DD} = 4.5 to 5.5 V	0		0.4	V
				0		0.1	V
	V_{IL4}	XT1, XT2	V_{DD} = 4.5 to 5.5 V	0		0.4	V
				0		0.1	V
Output voltage, high	V_{OH}	V_{DD} = 4.5 to 5.5 V, I_{OH} = –1 mA		V_{DD} – 1.0			V
		I_{OH} = –100 μA		V_{DD} – 0.5			V
Output voltage, low	V_{OL}	V_{DD} = 4.5 to 5.5 V, I_{OL} = 10 mA				1.0	V
		I_{OL} = 400 μA				0.5	V
Input leakage current, high	I_{LIH1}	V_{IN} = V_{DD}	Pins other than X1, X2, XT1, XT2			3	μA
	I_{LIH2}		X1, X2, XT1, XT2			20	μA
Input leakage current, low	I_{LIL1}	V_{IN} = 0 V	Pins other than X1, X2, XT1, XT2			–3	μA
	I_{LIL2}		X1, X2, XT1, XT2			–20	μA
Output leakage current, high	I_{LOH}	V_{OUT} = V_{DD}				3	μA
Output leakage current, low	I_{LOL}	V_{OUT} = 0 V				–3	μA
Software pull-up resistor	R	V_{IN} = 0 V		50	100	200	kΩ

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Power supply current[Note 1]	I_{DD1}	5.0-MHz crystal oscillation operating mode (C1 = C2 = 22 pF)	V_{DD} = 5.0 V ±10%[Note 3]		1.8	3.2	mA
			V_{DD} = 3.0 V ±10%[Note 4]		0.45	0.9	mA
			V_{DD} = 2.0 V ±10%[Note 4]		0.25	0.45	mA
	I_{DD2}	5.0-MHz crystal oscillation HALT mode (C1 = C2 = 22 pF)	V_{DD} = 5.0 V ±10%[Note 3]		0.8	1.6	mA
			V_{DD} = 3.0 V ±10%[Note 4]		0.3	0.6	mA
			V_{DD} = 2.0 V ±10%[Note 4]		0.15	0.3	mA
	I_{DD3}	32.768-kHz crystal oscillation operating mode[Note 2] (C3 = C4 = 22 pF, R = 220 kΩ)	V_{DD} = 5.0 V ±10%		70	160	μA
			V_{DD} = 3.0 V ±10%		40	90	μA
			V_{DD} = 2.0 V ±10%		25	60	μA
	I_{DD4}	32.768-kHz crystal oscillation HALT mode[Note 2] (C3 = C4 = 22 pF, R = 220 kΩ)	V_{DD} = 5.0 V ±10%		20	55	μA
			V_{DD} = 3.0 V ±10%		5	25	μA
			V_{DD} = 2.0 V ±10%		2.5	12.5	μA
	I_{DD5}	STOP mode	V_{DD} = 5.0 V ±10%		0.1	10	μA
			V_{DD} = 3.0 V ±10%		0.05	5.0	μA
			T_A = 25°C		0.05	3.0	μA
			V_{DD} = 2.0 V ±10%		0.05	3.0	μA

Notes 1. The port current (including the current flowing through the on-chip pull-up resistor) is not included.

2. When the main system clock is stopped

3. High-speed mode operation (when processor clock control register (PCC) is set to 00H)

4. Low-speed mode operation (when PCC is set to 02H)

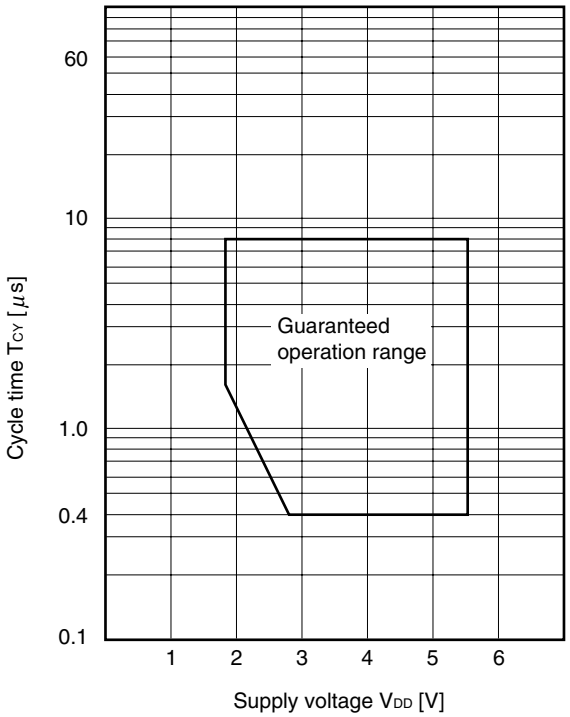
Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

AC Characteristics

(1) Basic operation (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Cycle time (Minimum instruction execution time)	T_{CY}	Operating with main system clock	V_{DD} = 2.7 to 5.5 V	0.4		8	μs
				1.6		8	μs
		Operating with subsystem clock		114	122	125	μs
TI80 input frequency	f_{TI}	V_{DD} = 2.7 to 5.5 V		0		4	MHz
				0		275	kHz
TI80 input high-/low-level width	t_{TIH}, t_{TIL}	V_{DD} = 2.7 to 5.5 V		0.1			μs
				1.8			μs
Interrupt input high-/low-level width	t_{INTH}, t_{INTL}	INTP0 to INTP2		10			μs
$\overline{\text{RESET}}$ input low-level width	t_{RSL}			10			μs

T_{CY} vs V_{DD} (main system clock)



(2) Serial interface

(a) 3-wire serial I/O mode ($\overline{SCK20}$...Internal clock)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK20}$ cycle time	t_{KCY1}	V_{DD} = 2.7 to 5.5 V		800			ns
				3,200			ns
$\overline{SCK20}$ high-/low-level width	t_{KH1}, t_{KL1}	V_{DD} = 2.7 to 5.5 V		t_{KCY1}/2–50			ns
				t_{KCY1}/2–150			ns
SI20 setup time (to $\overline{SCK20}$ ↑)	t_{SIK1}	V_{DD} = 2.7 to 5.5 V		150			ns
				500			ns
SI20 hold time (from $\overline{SCK20}$ ↑)	t_{KSI1}	V_{DD} = 2.7 to 5.5 V		400			ns
				600			ns
SO20 output delay time from $\overline{SCK20}$ ↓	t_{KSO1}	R = 1 kΩ, C = 100 pF[Note]	V_{DD} = 2.7 to 5.5 V	0		250	ns
				0		1,000	ns

Note R and C are the load resistance and load capacitance of the SO20 output line.

(b) 3-wire serial I/O mode ($\overline{SCK20}$...External clock)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK20}$ cycle time	t_{KCY2}	V_{DD} = 2.7 to 5.5 V		900			ns
				3,500			ns
$\overline{SCK20}$ high-/low-level width	t_{KH2}, t_{KL2}	V_{DD} = 2.7 to 5.5 V		400			ns
				1,600			ns
SI20 setup time (to $\overline{SCK20}$ ↑)	t_{SIK2}	V_{DD} = 2.7 to 5.5 V		100			ns
				150			ns
SI20 hold time (from $\overline{SCK20}$ ↑)	t_{KSI2}	V_{DD} = 2.7 to 5.5 V		400			ns
				600			ns
SO20 output delay time from $\overline{SCK20}$ ↓	t_{KSO2}	R = 1 kΩ, C = 100 pF[Note]	V_{DD} = 2.7 to 5.5 V	0		300	ns
				0		1,000	ns

Note R and C are the load resistance and load capacitance of the SO20 output line.

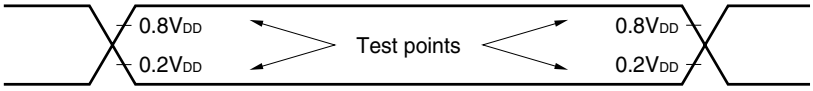
(c) UART mode (Dedicated baud rate generator output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		V_{DD} = 2.7 to 5.5 V			78,125	bps
					19,531	bps

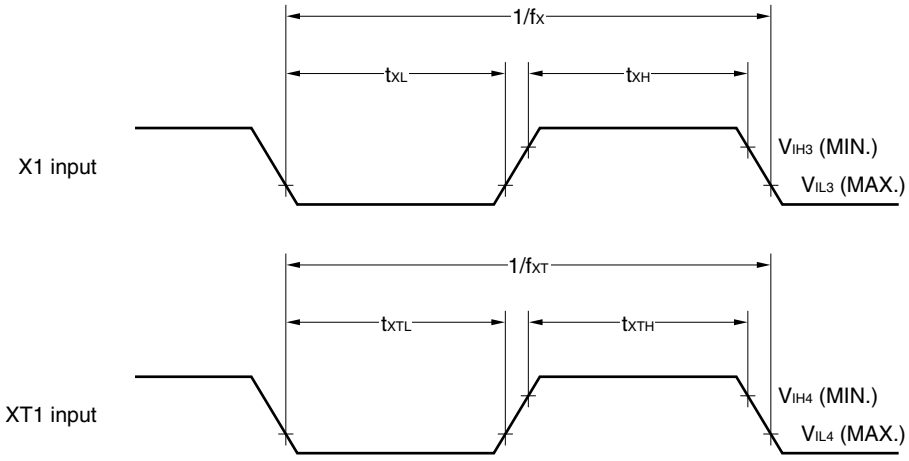
(d) UART mode (External clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
ASCK20 cycle time	t_{KCY3}	V_{DD} = 2.7 to 5.5 V	900			ns
			3,500			ns
ASCK20 high-/low-level width	t_{KH3}, t_{KL3}	V_{DD} = 2.7 to 5.5 V	400			ns
			1,600			ns
Transfer rate		V_{DD} = 2.7 to 5.5 V			39,063	bps
					9,766	bps
ASCK20 rise/fall time	t_R, t_F				1	μs

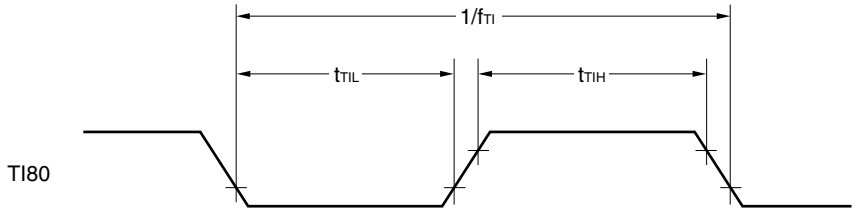
AC Timing Test Points (excluding X1 and XT1 inputs)



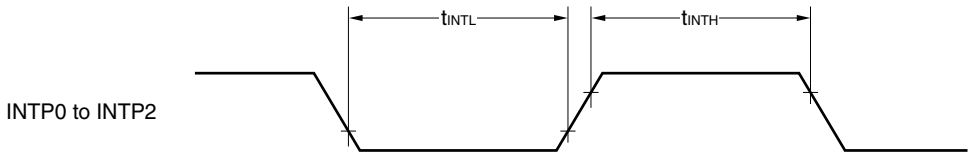
Clock Timing



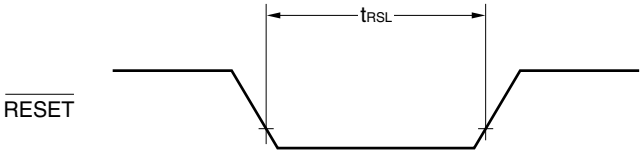
TI Timing



Interrupt Input Timing

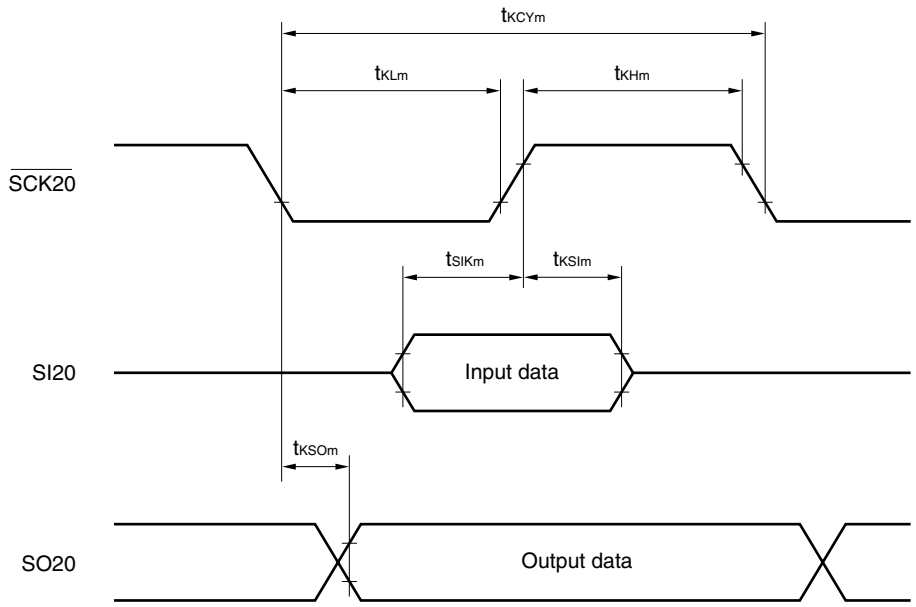


$\overline{\text{RESET}}$ Input Timing



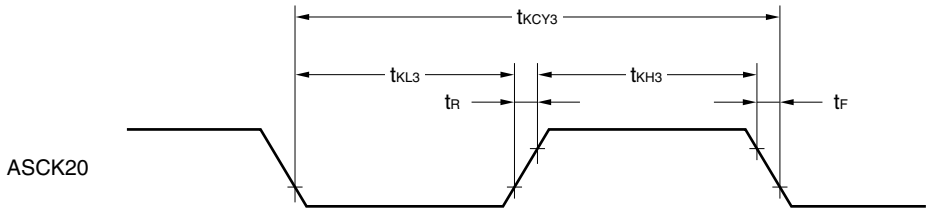
Serial Transfer Timing

3-wire serial I/O mode:



Remark m = 1, 2

UART mode (external clock input):



Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (T_A = –40 to +85°C)

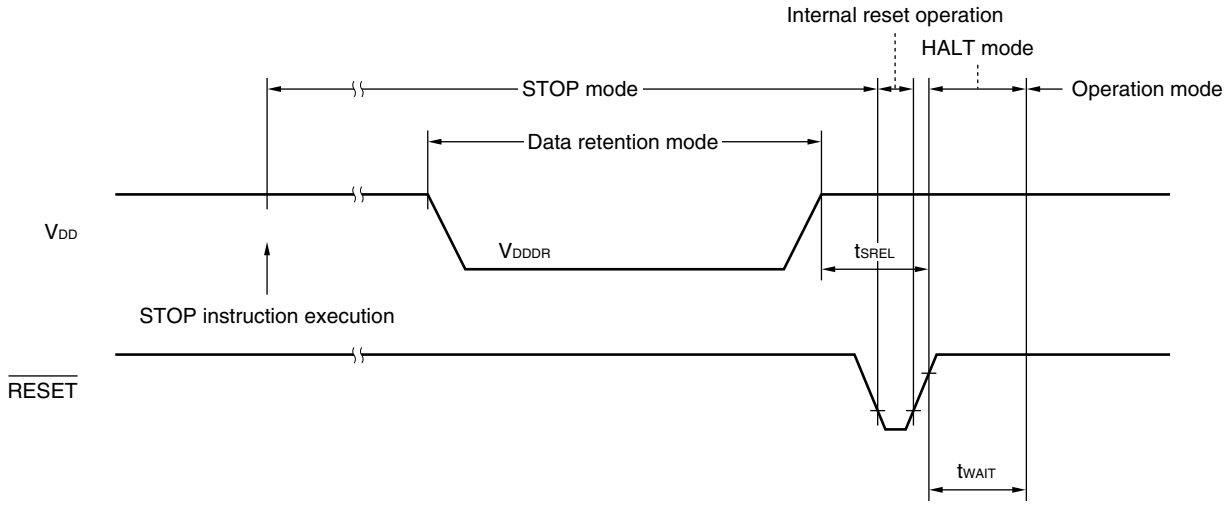
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention power supply voltage	V_{DDDR}		1.8		5.5	V
Release signal set time	t_{SREL}		0			μs
Oscillation stabilization wait time[Note 1]	t_{WAIT}	Release by $\overline{RESET}$		$2^{15}/f_X$		ms
		Release by interrupt request		**Note 2**		ms

Notes 1. Oscillation stabilization wait time is a time for stopping the CPU operation to prevent the unstable operation when the oscillation is started.

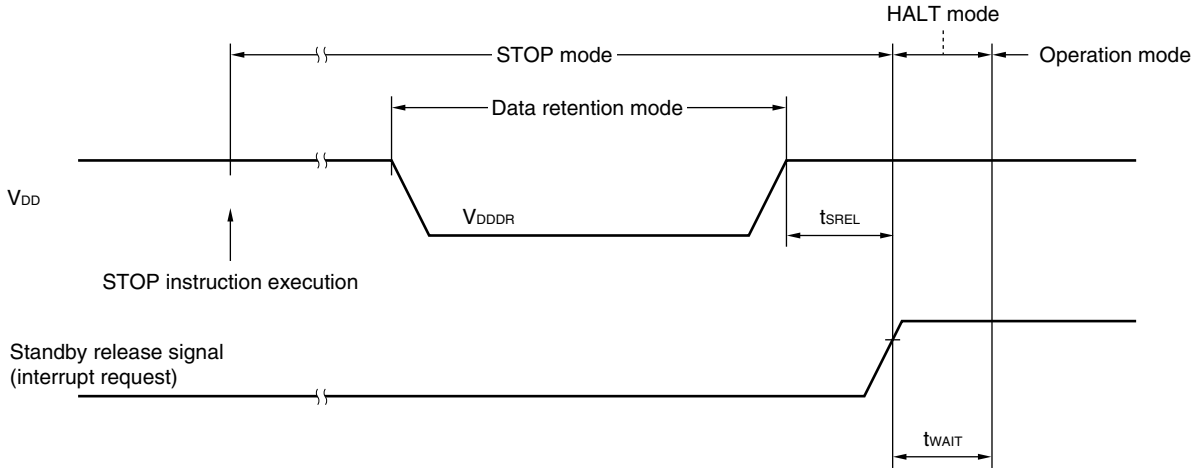
2. Selection of $2^{12}/f_X$, $2^{15}/f_X$, and $2^{17}/f_X$ is possible with bits 0 to 2 (OSTS0 to OSTS2) of the oscillation stabilization time select register (OSTS).

Remark f_X: Main system clock oscillation frequency

Data Retention Timing (STOP mode release by $\overline{RESET}$)

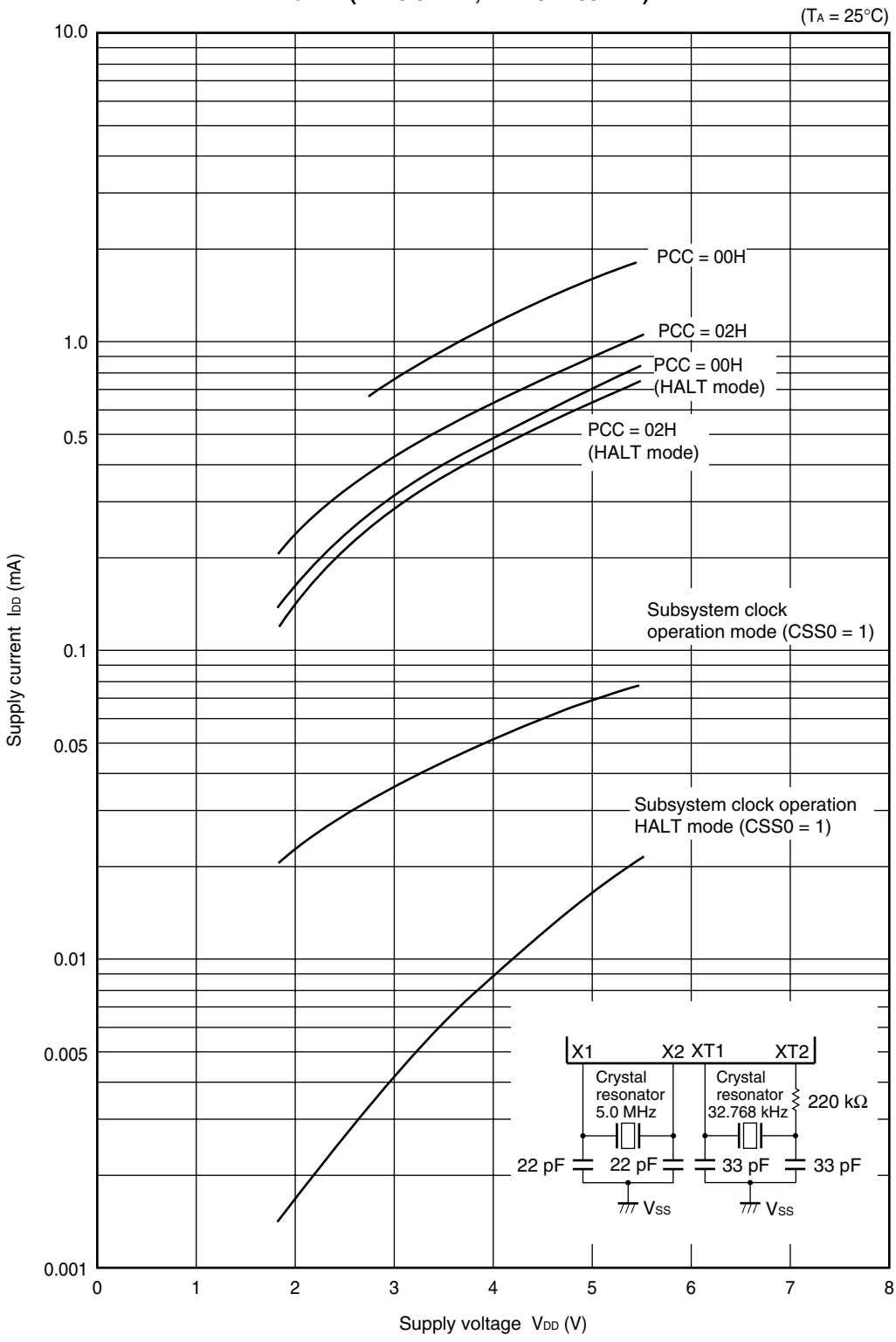


Data Retention Timing (Standby release signal: STOP mode release by interrupt signal)

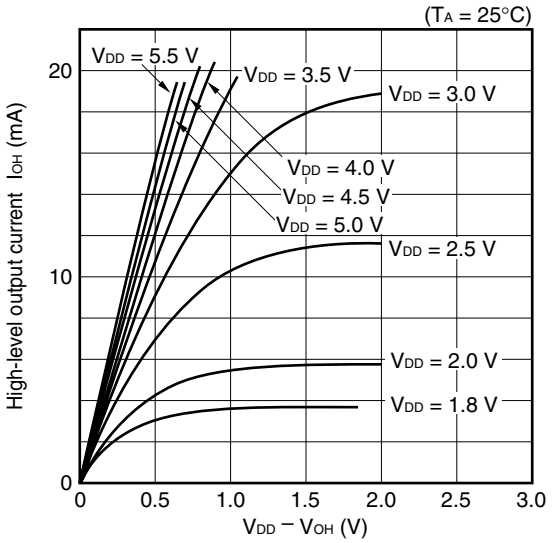


★ 11. CHARACTERISTICS CURVES

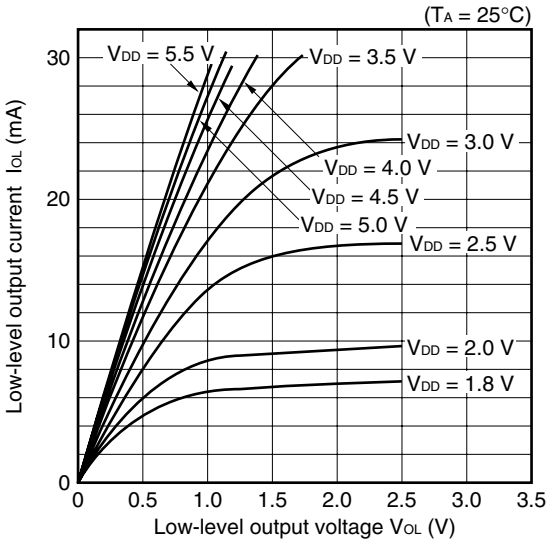
I_{DD} vs V_{DD} (f_X = 5.0 MHz, f_{XT} = 32.768 kHz)



I_{OH} vs $V_{DD} - V_{OH}$

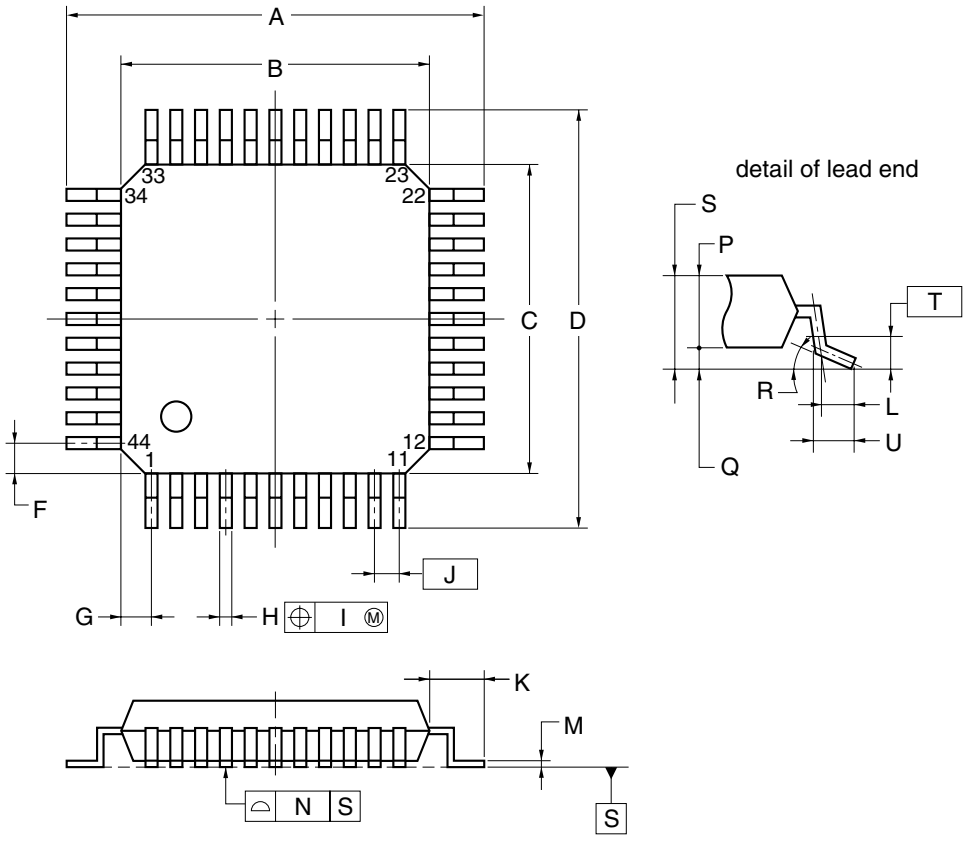


I_{OL} vs V_{OL}



★ 12. PACKAGE DRAWING

44 PIN PLASTIC QFP (10x10)



NOTE

Each lead centerline is located within 0.16 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	12.0±0.2
B	10.0±0.2
C	10.0±0.2
D	12.0±0.2
F	1.0
G	1.0
H	$0.37^{+0.08}_{-0.07}$
I	0.2
J	0.8 (T.P.)
K	1.0±0.2
L	0.5
M	$0.17^{+0.03}_{-0.06}$
N	0.10
P	1.4±0.05
Q	0.1±0.05
R	$3^{\circ}{}^{+4^{\circ}}_{-3^{\circ}}$
S	1.6 MAX.
U	0.6±0.15

S44GB-80-8ES-1

★ 13. RECOMMENDED SOLDERING CONDITIONS

The μPD789046 should be soldered and mounted under the following recommended conditions.

For soldering methods and conditions other than those recommended below, contact your NEC sales representative.

For technical information, see the following website.

Semiconductor Device Mount Manual (http://www.necel.com/pkg/en/mount/index.html)

Table 13-1. Surface Mounting Type Soldering Conditions

(1) μPD789046GB-xxx-8ES: 44-pin plastic LQFP (10 × 10)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 sec. Max. (at 210°C or higher), Count: two times or less	IR35-00-2
VPS	Package peak temperature: 215°C, Time: 40 sec. Max. (at 200°C or higher), Count: two times or less	VP15-00-2
Wave soldering	Solder bath temperature: 260°C Max., Time: 10 sec. Max., Count: once, Preheating temperature: 120°C Max. (package surface temperature)	WS60-00-1
Partial heating	Pin temperature: 350°C Max., Time: 3 sec. Max. (per pin row)	–

Caution Do not use different soldering methods together (except for partial heating).

(2) μPD789046GB-xxx-8ES-A: 44-pin plastic LQFP (10 × 10)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 260°C, Time: 60 seconds max. (at 220°C or higher), Count: Three times or less, Exposure limit: 7 days[Note] (after that, prebake at 125°C for 20 to 72 hours)	IR60-207-3
Wave soldering	For details, contact an NEC Electronics sales representative.	–
Partial heating	Pin temperature: 350°C max., Time: 3 seconds max. (per pin row)	–

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating).

Remark Products that have the part numbers suffixed by "-A" are lead-free products.

APPENDIX A. DEVELOPMENT TOOLS

The following development tools are available for system development using the μPD789046.

Language Processing Software

RA78K0S[Notes 1, 2, 3]	Assembler package common to 78K/0S Series
CC78K0S[Notes 1, 2, 3]	C compiler package common to 78K/0S Series
DF789046[Notes 1, 2, 3]	Device file for μPD789046 Subseries
CC78K0S-L[Notes 1, 2, 3]	C compiler library source file common to 78K/0S Series

★ Flash Memory Writing Tools

Flashpro III (Part No. FL-PR3[Note 4], PG-FP3)	Flash programmer dedicated to on-chip flash memory microcontroller
FA-44GB-8ES[Note 4]	Flash memory writing adapter for 44-pin plastic LQFP (GB-8ES type)

Notes 1. Based on the PC-9800 series (MS-DOS + Windows)

2. Based on the IBM PC/AT and compatibles (Japanese/English Windows)

3. Based on the HP9000 series 700 (HP-UX), SPARCstation (SunOS , Solaris™), and NEWS (NEWS-OS)

4. Products made by NAITO DENSEI MACHIDA MFG. CO., LTD. (+81-44-822-3813). Contact an NEC distributor regarding the purchase of these products.

Remark The RA78K0S and CC78K0S are used in combination with the DF789046.

Debugging Tools

IE-78K0S-NS In-circuit emulator	This in-circuit emulator is used to debug hardware or software when application systems which use the 78K/0S Series are developed. The IE-78K0S-NS supports the integrated debugger (ID78K0S-NS). The IE-78K0S-NS is used in combination with an interface adapter for connection to an AC adapter, emulation probe, or host machine.
IE-70000-MC-PS-B AC adapter	This adapter is used to supply power from a 100 to 240 V AC outlet.
IE-70000-98-IF-C Interface adapter	This adapter is required when a PC-9800 series PC (except notebook type) is used as the host machine for the IE-78K0S-NS (C bus supported).
★ IE-70000-CD-IF-A PC card/interface	These PC card and interface cable are required when a notebook PC is used as the host machine for the IE-78K0S-NS (PCMCIA socket supported).
IE-70000-PC-IF-C Interface adapter	This adapter is required when an IBM PC/AT™ or compatible is used as the host machine for the IE-78K0S-NS (ISA bus supported).
★ IE-70000-PCI-IF Interface adapter	This adapter is required when a PCI bus incorporated personal computer is used as the host machine for the IE-78K0S-NS.
IE-789046-NS-EM1 Emulation board	This board is used to emulate the peripheral hardware specific to the device. The IE-789046-NS-EM1 is used in combination with the in-circuit emulator.
NP-44GB[Note 3] ★ NP-44GB-TQ[Note 3]	This board is used to connect an in-circuit emulator to the target system. The board is dedicated to the 44-pin plastic LQFP (GB-8ES type).
SM78K0S[Notes 1, 2]	System simulator common to 78K/0S Series
ID78K0S-NS[Notes 1, 2]	Integrated debugger common to 78K/0S Series
DF789046[Notes 1, 2]	Device file for μPD789046 Subseries

Real-time OS

MX78K0S[Notes 1, 2]	OS for 78K/0S Series

Notes 1. Based on the PC-9800 series (MS-DOS + Windows)

2. Based on the IBM PC/AT and compatibles (Japanese/English Windows)

3. Products made by NAITO DENSEI MACHIDA MFG. CO., LTD. (+81-44-822-3813). Contact an NEC distributor regarding the purchase of these products.

Remark The SM78K0S is used in combination with the DF789046.

APPENDIX B. RELATED DOCUMENTS

Documents Related to Devices

Document Name	Document No.	
	Japanese	English
μPD789046 Data Sheet	U13380J	This manual
μPD78F9046 Preliminary Product Information	U13546J	U13546E
μPD789046 Subseries User's Manual	U13600J	U13600E
78K/0S Series Instructions User's Manual	U11047J	U11047E

Documents Related to Development Tools (User's Manuals)

Document Name		Document No.	
		Japanese	English
RA78K0S Assembler Package	Operation	U11622J	U11622E
	Assembly Language	U11599J	U11599E
	Structured Assembly Language	U11623J	U11623E
CC78K0S C Compiler	Operation	U11816J	U11816E
	Language	U11817J	U11817E
SM78K0S System Simulator Windows Based	Reference	U11489J	U11489E
SM78K Series System Simulator	External Part User Open Interface Specifications	U10092J	U10092E
ID78K0S-NS Integrated Debugger Windows Based	Reference	U12901J	U12901E
★ IE-78K0S-NS In-circuit Emulator		U13549J	U13549E
IE-789046-NS-EM1 Emulation Board		To be prepared	To be prepared

Documents Related to Embedded Software (User's Manuals)

Document Name		Document No.	
		Japanese	English
78K/0S Series OS MX78K0S	Fundamental	U12938J	U12938E

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document for designing.

Other Related Documents

Document Name	Document No.	
	Japanese	English
★ SEMICONDUCTORS SELECTION GUIDE Products & Packages	X13769X	
Semiconductor Device Mounting Technology Manual	**Note**	
Quality Grades on NEC Semiconductor Devices	C11531J	C11531E
NEC Semiconductor Device Reliability/Quality Control System	C10983J	C10983E
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892J	C11892E
Guide to Microcomputer-Related Products by Third Party	U11416J	–

Note See the “Semiconductor Device Mount Manual” website (http://www.necel.com/pkg/en/mount/index.html).

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document for designing.

NOTES FOR CMOS DEVICES

① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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