DATA SHEET

NEC

MOS INTEGRATED CIRCUIT

μPD70(F)3175

V850E/CA4™ HELIOS
32- bit RISC Microcontroller

DESCRIPTION

The V850E/CA4 Helios microcontroller is a member of NEC's V850 32-bit RISC family, which match the performance gains attainable with RISC-based controllers to the needs of embedded control applications. The V850 CPU offers easy pipeline handling and programming, resulting in compact code size comparable to 16-bit CISC CPUs.
The V850E/CA4 Helios offers an excellent combination of general purpose peripheral functions, like serial communication interfaces (UART, clocked SI) and measurement inputs (A/D converter), with dedicated CAN network support.
The device offers power-saving modes to manage the power consumption effectively under varying conditions.Thus equipped, the V850E/CA4 Helios is ideally suited for automotive applications, like Airbags. It is also an excellent choice for other applications where a combination of sophisticated peripheral functions and CAN network support is required.

Functions in detail are described in the following user's manuals. Be sure to read these manuals when you design your systems.

<V850E/CA4 User Manual> : <U16241EE1V0UM00>
<V850E Architecture Manual> : <U10243EJ6V0UM00>

FEATURES

- 32-bit RISC CPU with Harvard Architecture
- Full-CAN Interface: 2 channels
- Serial Interfaces: 5 channels
  - 3-wire mode: 3 channels
  - UART mode: 2 channels
- Timers: 6 channels
  - 16-bit multi purpose timer/event counter: 2 channels
  - 16-bit multi purpose timer: 2 channels
  - Watch timer: 1 channel
  - Watchdog timer: 1 channel
- 10-bit resolution A/D Converter: 14 channels
- I/O lines: 76
- Power supply voltage range:
  - $+4.5\ V \leq V_{DD} \leq +5.5\ V$
- Frequency range: up to 32 MHz
- Built-in low power saving mode
- Built-in clock oscillator circuit with internal PLL
- Temperature range:
  - -40 °C to +85 °C (μPD70F3175(A), μPD703175(A)-32/24, μPD703176(A)-32/24)
- Package:
  - 100 LQFP, 0.5 mm pin-pitch (14 × 14 mm)

ORDERING INFORMATION

Device	Part Number	Package	ROM	RAM	FCAN option	Oper. Frequency
V850E/CA4	μPD70F3175(A)-32	LQFP100 14 × 14 mm	256 K	12 K	2 Channels	-40°C ~ +85°C
	μPD703175(A)-32/24		256 K	12 K	2 Channels	-40°C ~ +85°C
	μPD703176(A)-32/24		192 K	10 K	2 Channels	-40°C ~ +85°C

The information contained in this document is released in advance of the production cycle for the device. The parameters for the device may change before final production, or NEC Corporation may, at its own discretion, withdraw the device prior to production.

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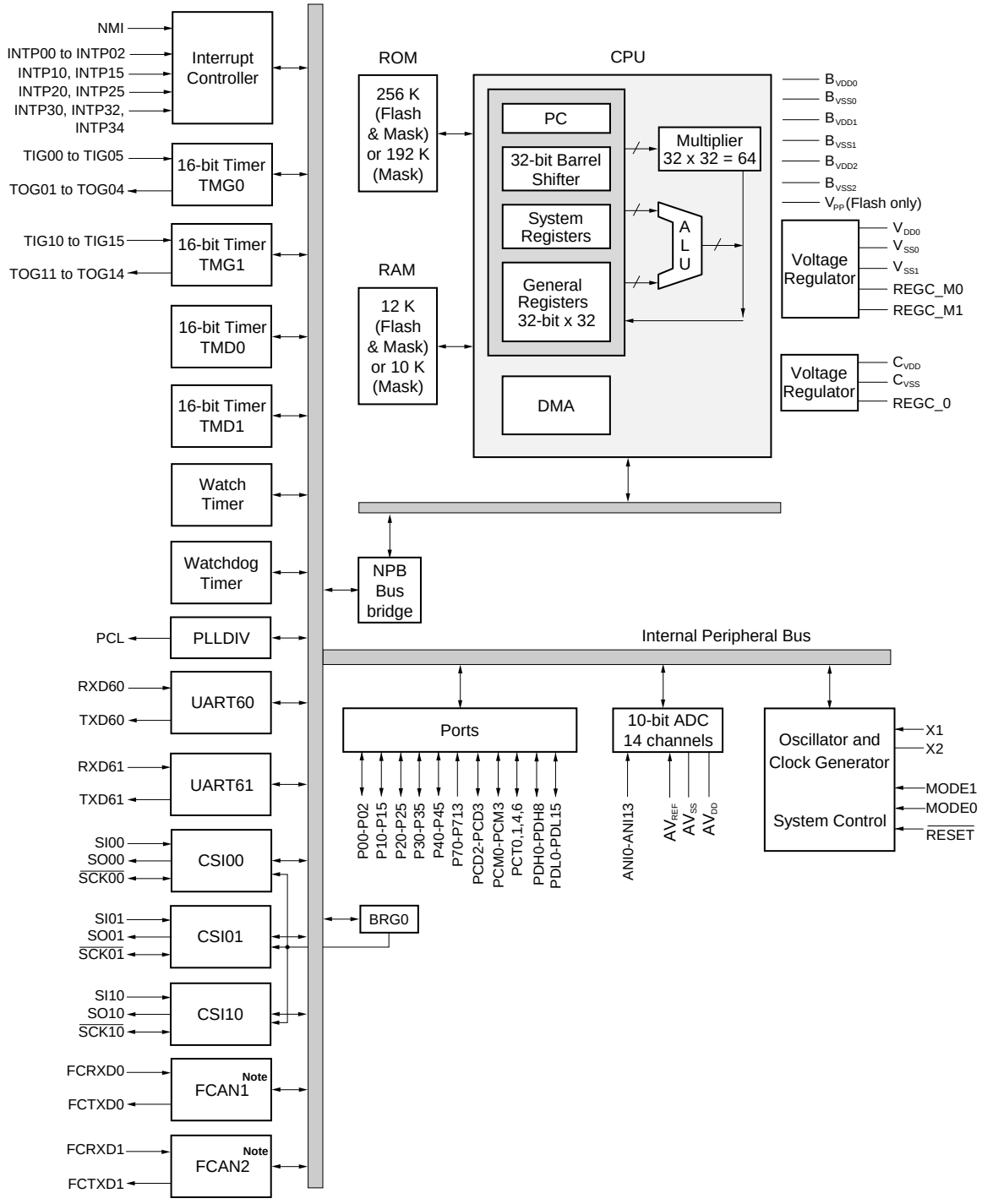
INTERNAL BLOCK DIAGRAM



Note: The CAN macro of this device fulfils the requirements according ISO 11898. Additionally the CAN macro was tested according to the test procedures required by ISO 16845. The CAN macro successfully passed all test patterns. Beyond these test patterns, other tests like robustness tests and processor interface tests as recommended by C&S/FH Wolfenbuettel have successfully been issued.

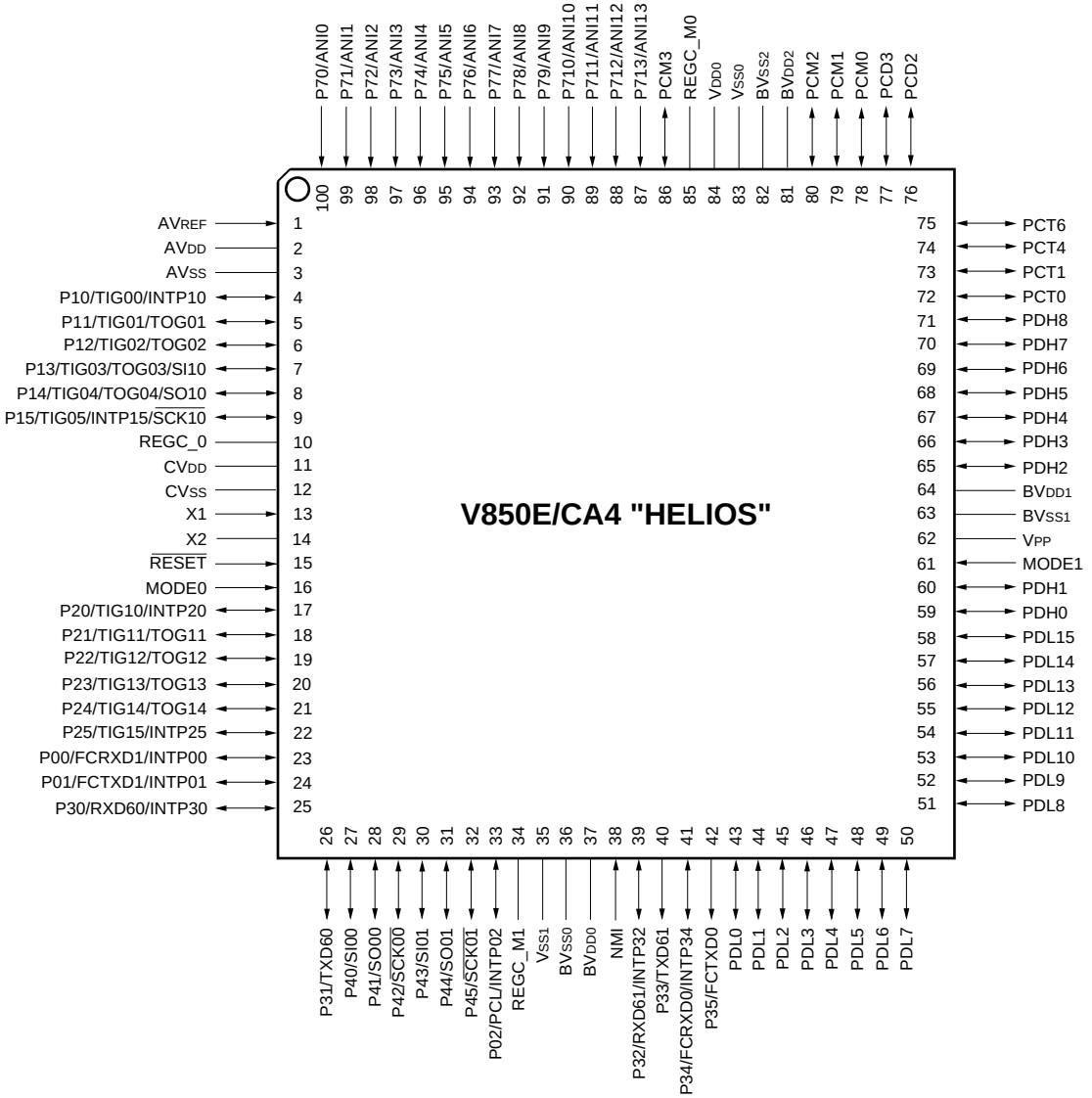
PIN IDENTIFICATION

ANI0 to ANI13	Analog Inputs
AV_{DD}	Analog Power Supply
AV_{SS}	Analog Ground
AV_{REF}	Analog reference Voltage supply
PCL	Processor Clock Output
FCRXD0, FCRXD1	CAN Receive Data for channel 0 and 1
FCTXD0, FCTXD1	CAN Transmit Data for channel 0 and 1
INTP00, INTP01, INTP02, INTP10, INTP15, INPT20, INTP25, INTP30, INTP32, INTP34	External Interrupt Input
NMI	Non-Maskable Interrupt Input
P00 to P02	Port 0
P10 to P15	Port 1
P20 to P25	Port 2
P30 to P35	Port 3
P40 to P45	Port 4
P70 to P713	Port 7
PCM0 to PCM3	Port CM
PCT0, PCT1, PCT4, PCT6	Port CT
PCD2 to PCD3	Port CD
PDL0 to PDL15	Port DL
PDH0 to PDH8	Port DH
RXD60, RXD61	UART Receive Data
TXD60, TXD61	UART Transmission Data
$\overline{SCK00}$, $\overline{SCK01}$, $\overline{SCK10}$	Synchronous Interface Clock
SI00, SI01, SI10	Synchronous Interface Input
SO00, SO01, SO10	Synchronous Interface Output
TOG01 to TOG04	Timer G0 Compare Output
TOG11 to TOG14	Timer G1 Compare Output
TIG00 to TIG05	Timer G0 Capture Input
TIG10 to TIG15	Timer G1 Capture Input
REGC_M0, REGC_M1	Main Regulator Output
REGC_O	Osc and PLL Regulator Output
MODE0, MODE1	Operation mode select
X1, X2	Main System Clock
$\overline{RESET}$	Reset Input
CV_{DD}, CV_{SS}	Oscillator and PLL power supply
V_{DD0}	Digital power supply for Flash, CPU and I/O buffer
V_{SS0}, V_{SS1}	Digital Ground for Flash, CPU and I/O buffer
BV_{SS0} to BV_{SS2}	I/O buffers Ground
BV_{DD0} to BV_{DD2}	I/O buffers supply
V_{PP}	Programming Voltage

PIN CONFIGURATION

- 100-Pin Plastic LQFP (0.5 mm pin pitch) (14 × 14 mm)

  - μPD70F3175(A)-32
  - μPD703175(A)-32/24
  - μPD703176(A)-32/24



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1. Pin Functions

1.1 Pin Functions

Table 1-1: Pin Functions (1/4)

Pin		Function		I/O	Driver Type
No.	Name	Default	Alternate		
1	AV_{REF}	Reference-Voltage supply pin for A/D converter	-	-	-
2	AV_{DD}	Power supply pin for A/D converter	-	-	-
3	AV_{SS}	Ground potential for A/D converter	-	-	-
4	P10/TIG00/ INTP10	Port 1: 6-bit input/output port	Timer G0 Capture Trigger 0 External interrupt input INTP10	I/O	5-K
5	P11/TIG01/TOG01		Timer G0 Capture Trigger 0 Timer G0 Compare Output 0	I/O	
6	P12/TIG02/TOG02		Timer G0 Capture Trigger 0 Timer G0 Compare Output 0	I/O	
7	P13/TIG03/ TOG03/SI10		Timer G0 Capture Trigger 0 Timer G0 Compare Output 0 CSI1 channel 0 serial data input	I/O	
8	P14/TIG04/ TOG04/SO10		Timer G0 Capture Trigger 0 Timer G0 Compare Output 0 CSI1 channel 0 serial data output	I/O	
9	P15/TIG05/ INTP15/$\overline{SCK10}$		Timer G0 Capture Trigger 0 External interrupt input INTP15 CSI1 channel 0 serial clock input	I/O	
10	REGC_O	Pin for external 3.3 V Regulating Capacitor	-	-	-
11	CV_{DD}	Power supply pin for oscillator and PLL	-	-	-
12	CV_{SS}	Ground potential pin for oscillator and PLL	-	-	-
13	X1	Resonator connection for clock	-	-	-
14	X2	Resonator connection for clock	-	-	-
15	$\overline{RESET}$	External System reset input	-	-	2
16	MODE0	MODE Definition Input pins	-	I	2

Table 1-1: Pin Functions (2/4)

Pin		Function		I/O	Driver Type
No.	Name	Default	Alternate		
17	P20/TIG10/ INTP20	Port 2: 6-bit input/output port	Timer G1 Capture Trigger 0 External interrupt input INTP20	I/O	5-K
18	P21/TIG11/TOG11		Timer G1 Capture Trigger 0 Timer G1 Compare Output 0	I/O	
19	P22/TIG12/TOG12		Timer G1 Capture Trigger 0 Timer G1 Compare Output 0	I/O	
20	P23/TIG13/TOG13		Timer G1 Capture Trigger 0 Timer G1 Compare Output 0	I/O	
21	P24/TIG14/TOG14		Timer G1 Capture Trigger 0 Timer G1 Compare Output 0	I/O	
22	P25/TIG15/ INTP25		Timer G1 Capture Trigger 0 External interrupt input INTP25	I/O	
23	P00/FCRXD1/ INTP00	Port 0: 3-bit input/output port	FCAN channel 1 serial data input External interrupt input INTP00	I/O	
24	P01/FCTXD1/ INTP01		FCAN channel 1 serial data output External interrupt input INTP01	I/O	
25	P30/RXD60/ INTP30	Port 3: 6-bit input/output port	UART60 asynchronous data input External interrupt input INTP30	I/O	
26	P31/TXD60		UART60 asynchronous data output	I/O	
27	P40/SI00	Port 4: 6-bit input/output port	CSI0 channel 0 serial data input	I/O	
28	P41/SO00		CSI0 channel 0 serial data output	I/O	
29	P42/$\overline{SCK00}$		CSI0 channel 0 serial clock input	I/O	
30	P43/SI01		CSI0 channel 1 serial data input	I/O	
31	P44/SO01		CSI0 channel 1 serial data output	I/O	
32	P45/$\overline{SCK01}$		CSI0 channel 1 serial clock input	I/O	
33	P02/PCL/INTP02	Port 0: 3-bit input/output port	Processor clock output External interrupt input INTP02	I/O	
34	REGC_M1	pin for external 3.3 V Regulating Capacitor	-	-	-
35	V_{SS1}	Ground potential pin for Flash, CPU and I/O buffers	-	-	-
36	BV_{SS0}	Ground potential pin for I/O buffers	-	-	-
37	BV_{DD0}	Power supply pin for I/O buffers	-	-	-
38	NMI	Non-maskable interrupt input pin	-	I	2
39	P32/RXD61/ INTP32	Port 3: 6-bit input/output port	UART61 asynchronous data input External interrupt input INTP32	I/O	5-K
40	P33/TXD61		UART61 asynchronous data output	I/O	
41	P34/FCRXD0/ INTP34		FCAN channel 0 serial data input External interrupt input INTP34	I/O	
42	P35/FCTXD0		FCAN channel 0 serial data output	I/O	

Table 1-1: Pin Functions (3/4)

Pin		Function		I/O	Driver Type
No.	Name	Default	Alternate		
43	PDL0	Port DL: 16-bit input/output port	-	I/O	5
44	PDL1		-	I/O	
45	PDL2		-	I/O	
46	PDL3		-	I/O	
47	PDL4		-	I/O	
48	PDL5		-	I/O	
49	PDL6		-	I/O	
50	PDL7		-	I/O	
51	PDL8		-	I/O	
52	PDL9		-	I/O	
53	PDL10		-	I/O	
54	PDL11		-	I/O	
55	PDL12		-	I/O	
56	PDL13		-	I/O	
57	PDL14		-	I/O	
58	PDL15		-	I/O	
59	PDH0	Port DH: 9-bit output port	-	I/O	
60	PDH1		-	I/O	
61	MODE1	MODE Definition Input pins	-	I/O	2
62	V_{PP} **Note**	High Voltage apply pin to program the device	-	-	-
63	BV_{SS1}	Ground potential pin for I/O buffers		-	-
64	BV_{DD1}	Power supply pin for I/O buffers		-	-
65	PDH2	Port DH: 9-bit output port	-	I/O	5
66	PDH3		-	I/O	
67	PDH4		-	I/O	
68	PDH5		-	I/O	
69	PDH6		-	I/O	
70	PDH7		-	I/O	
71	PDH8		-	I/O	
72	PCT0	Port CT: 4-bit input/output port	-	I/O	
73	PCT1		-	I/O	
74	PCT4		-	I/O	
75	PCT6		-	I/O	
76	PCD2	Port CD: 2-bit output port	-	I/O	
77	PCD3		-	I/O	
78	PCM0	Port CM: 4-bit output port	-	I/O	
79	PCM1		-	I/O	
80	PCM2		-	I/O	
81	BV_{DD2}	Power supply pin for I/O buffers	-	-	-

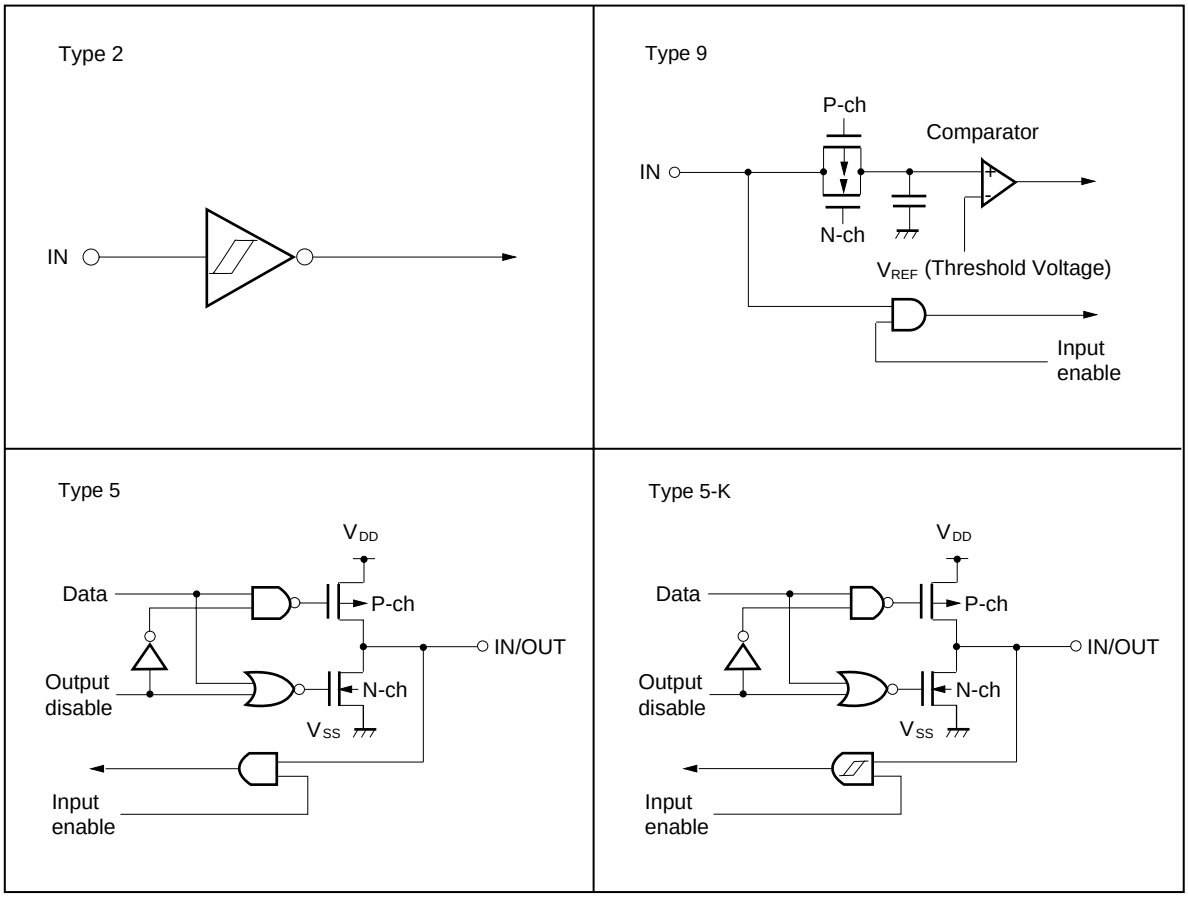
Table 1-1: Pin Functions (4/4)

Pin		Function		I/O	Driver Type
No.	Name	Default	Alternate		
82	BV_{SS2}	Ground potential pin for I/O buffers	-	-	-
83	V_{SS0}	Ground potential pin for Flash, CPU and I/O buffers	-	-	-
84	V_{DD0}	Power supply pin for Flash, CPU and I/O buffers	-	-	-
85	REGC_M0	pin for external 3.3 V Regulating Capacitor	-	-	-
86	PCM3	Port CM: 4-bit output port	-	I/O	5
87	P713/ANI13	Port 7: 14-bit input port	ANI13	I/O	9
88	P712/ANI12		ANI12	I/O	
89	P711/ANI11		ANI11	I/O	
90	P710/ANI10		ANI10	I/O	
91	P79/ANI9		ANI9	I/O	
92	P78/ANI8		ANI8	I/O	
93	P77/ANI7		ANI7	I/O	
94	P76/ANI6		ANI6	I/O	
95	P75/ANI5		ANI5	I/O	
96	P74/ANI4		ANI4	I/O	
97	P73/ANI3		ANI3	I/O	
98	P72/ANI2		ANI2	I/O	
99	P71/ANI1		ANI1	I/O	
100	P70/ANI0		ANI0	I/O	

Note: Only for μPD70F3175 (Flash product)

1.2 I/O Circuits

Figure 1-1: Input / Output Circuits



1.3 Port Pins

Table 1-2: Port Functions (1/3)

Port name	Pin name	Pin function after Reset In Single Chip Mode	If not used
P0	P00/FCRXD1/INTP00	Port Mode (input mode)	Independently connect to BV_{SS} or BV_{DD} via resistor Output: leave open
	P01/FCTXD1/INTP01		
	P02/PCL/INTP02		
P1	P10/TIG00/INTP10	Port Mode (input mode)	Independently connect to BV_{SS} or BV_{DD} via resistor Output: leave open
	P11/TIG01/TOG01		
	P12/TIG02/TOG02		
	P13/TIG03/TOG03/SI10		
	P14/TIG04/TOG04/SO10		
	P15/TIG05/INTP15/$\overline{SCK10}$		
P2	P20/TIG10/INTP20	Port Mode (input mode)	Independently connect to BV_{SS} or BV_{DD} via resistor Output: leave open
	P21/TIG11/T0G11		
	P22/TIG12/T0G12		
	P23/TIG13/T0G13		
	P24/TIG14/T0G14		
	P25/TIG15/INTP25		
P3	P30/RXD60/INTP30	Port Mode (input mode)	Independently connect to BV_{SS} or BV_{DD} via resistor Output: leave open
	P31/TXD60		
	P32/RXD61/INTP32		
	P33/TXD61		
	P34/FCRXD0/INTP34		
	P35/FCTXD0		
P4	P40/SI00	Port Mode (input mode)	Independently connect to BV_{SS} or BV_{DD} via resistor Output: leave open
	P41/SO00		
	P42/$\overline{SCK00}$		
	P43/SI01		
	P44/SO01		
	P45/$\overline{SCK01}$		

Table 1-2: Port Functions (2/3)

Port name	Pin name	Pin function after Reset In Single Chip Mode	If not used
P7	P70/ANI0	Port Mode (input mode)	Independently connect to AV_{SS} or AV_{DD} via resistor
	P71/ANI1		
	P72/ANI2		
	P73/ANI3		
	P74/ANI4		
	P75/ANI5		
	P76/ANI6		
	P77/ANI7		
	P78/ANI8		
	P79/ANI9		
	P710/ANI10		
	P711/ANI11		
	P712/ANI12		
	P713/ANI13		
PCT	PCT0	Port Mode (input mode)	Independently connect to BV_{SS} or BV_{DD} via resistor Output: leave open
	PCT1		
	PCT4		
	PCT6		
PDH	PDH0	Port Mode (input mode)	Independently connect to BV_{SS} or BV_{DD} via resistor Output: leave open
	PDH1		
	PDH2		
	PDH3		
	PDH4		
	PDH5		
	PDH6		
	PDH7		
	PDH8		
PCM	PCM0	Port Mode (input mode)	Independently connect to BV_{SS} or BV_{DD} via resistor Output: leave open
	PCM1		
	PCM2		
	PCM3		
PCD	PCD2	Port Mode (input mode)	Independently connect to BV_{SS} or BV_{DD} via resistor Output: leave open
	PCD3		

Table 1-2: Port Functions (3/3)

Port name	Pin name	Pin function after Reset In Single Chip Mode	If not used
PDL	PDL0	Port Mode (input mode)	Independently connect to BV_{SS} or BV_{DD} via resistor Output: leave open
	PDL1		
	PDL2		
	PDL3		
	PDL4		
	PDL5		
	PDL6		
	PDL7		
	PDL8		
	PDL9		
	PDL10		
	PDL11		
	PDL12		
	PDL13		
	PDL14		
	PDL15		

1.4 Non-port Pins

Table 1-3: Non-Port Functions

Pin Number	Pin name	Connection for normal operation	If not used
1	AV_{REF}	Analog voltage reference for A/D converter	-
2	AV_{DD}	Analog Power Supply	-
3	AV_{SS}	Analog Ground	Connect to BV_{SS}
10	REGC_O	Connect to CV_{SS} via a capacitor **Note 1**	-
11	CV_{DD}	Power supply pin for oscillator and PLL	-
12	CV_{SS}	Ground potential pin for oscillator and PLL	-
13	X1	Refer to Figure 3-2, “Oscillator Recommendations,” on page 24 for recommended circuit	-
14	X2		-
15	$\overline{RESET}$	External system reset input	-
16	MODE0	Connect to V_{SSn} via a resistor	-
34	REGC_M1	Connect to V_{SS1} via a capacitor **Note 2**	-
35	V_{SS1}	Ground potential pin for Flash, CPU and I/O buffers	-
36	BV_{SS0}	Ground potential pin for I/O buffers	-
37	BV_{DD0}	Power supply pin for I/O buffers	-
NMI	NMI	NMI	Independently connect to V_{SS} or V_{DD} via resistor
61	MODE1	Connect to V_{SSn} via a resistor	-
62	V_{PP} **Note 3**	On Flash devices connect V_{PP} to ground via a resistor.	On ROM devices connect directly to ground
63	BV_{SS1}	Ground potential pin for I/O buffers	
64	BV_{DD1}	Power supply pin for I/O buffers	
81	BV_{DD2}	Power supply pin for I/O buffers	-
82	BV_{SS2}	Ground potential pin for I/O buffers	-
83	V_{SS0}	Ground potential pin for Flash, CPU and I/O buffers	-
84	V_{DD0}	Power supply pin for Flash, CPU and I/O buffers	-
85	REGC_M0	Connect to REGC_M1 pin with the shortest way (lowest impedance)	-

Notes: 1. NEC specifies to connect a minimum 330 nF Capacitor.

2. NEC specifies to connect a minimum 1 µF Capacitor.

3. Only for µPD70F3175 (Flash product)

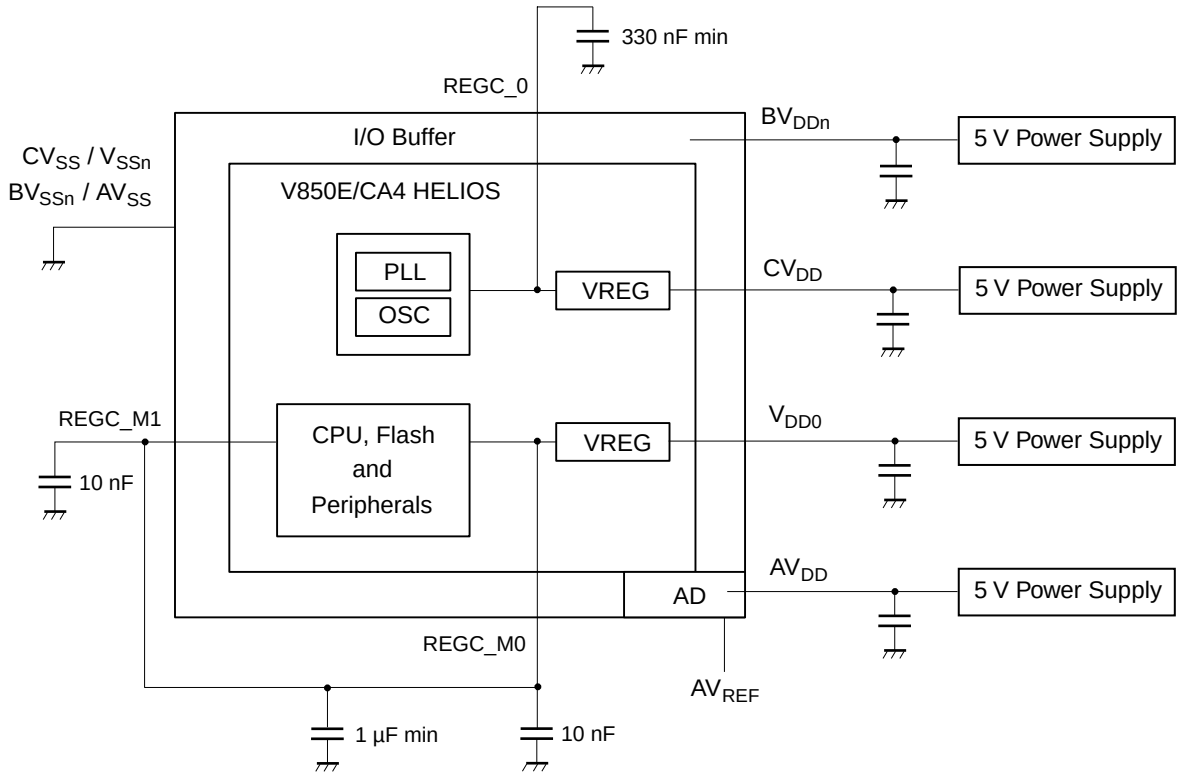
Cautions: 1. On REGC-pin and each pin of V_{DDn}, a capacitor has to be attached as tight as possible to the pin.

2. The capacitors used should have only very low serial impedance.

3. All ground pin have to be connected together.

4. For EMI optimization, NEC recommends to separate power supply for V_{DDn}, CV_{DDn} and BV_{DD} (refer to Figure 1-2, “Power Supply Connection,” on page 17).

Figure 1-2: Power Supply Connection



2. Programming Flash Memory

The device μPD70F3175 supports the programming of the internal flash in two ways: Either by using the *flash*MASTER programming tool or by performing self-programming using software functions and I/O communications.
For programming details about both methods, see the User's Manual. For timing characteristics about the initial programming using *flash*MASTER and some more electrical data about the Flash Memory, please see 3.7 "Flash EPROM Characteristics" on page 30.

3. Electrical Specifications

3.1 Absolute Maximum Ratings

3.1.1 Flash version

(T_A = +25°C, V_{SSx} = CV_{SS} = BV_{SSx} = 0 V)

Table 3-1: Absolute Maximum Ratings

Parameter		Symbol	Test Conditions	Ratings	Unit
Supply voltage		V_{DD0}		-0.5 to +6.0	V
		CV_{DD}		-0.5 to +6.0	V
		CV_{SS}		-0.5 to +0.5	V
		BV_{DDn}		-0.5 to +6.0	V
		BV_{SSn}		-0.5 to +0.5	V
		AV_{DD}	$AV_{DD} \le V_{DD0}$ + 0.5 V	-0.5 to +5.5	V
		AV_{SS}		-0.5 to +0.5	V
Input voltage		V_I (all except X1, X2, AV_{REF})	$V_I < BV_{DDx}$ + 0.5 V	-0.5 to +6.0	V
		AV_{REF}	$AV_{REF} \le AV_{DD}$	-0.5 to +0.5	V
		V_{PP}	Flash programming mode	-0.5 to +8.5	V
Input voltage	alphabetical Ports	V_{AN}	$V_{AN} < AV_{DD}$ +0.5 V	-0.5 to +6.0	V
Output current low	1 pin	I_{OL}		4.0	mA
	All pins			50	mA
Output current high	1 pin	I_{OH}		-4.0	mA
	All pins			-50	mA
Operating temperature		T_{OPR}	μPD70F3175(A)	-40 ~ +85	°C
Storage temperature		T_{STGB}	Before programming	-55 ~ +150	°C
		T_{STGA}	After programming	-55 ~ +125	°C

3.1.2 Mask version

(T_A = +25°C, V_{SSx} = CV_{SS} = BV_{SSx} = 0 V)

Table 3-2: Absolute Maximum Ratings

Parameter		Symbol	Test Conditions	Ratings	Unit
Supply voltage		V_{DD0}		-0.5 to +6.0	V
		CV_{DD}		-0.5 to +6.0	V
		CV_{SS}		-0.5 to +0.5	V
		BV_{DDn}		-0.5 to +6.0	V
		BV_{SSn}		-0.5 to +0.5	V
		AV_{DD}	$AV_{DD} < V_{DD0}$ + 0.5 V	-0.5 to +5.5	V
		AV_{SS}		-0.5 to +0.5	V
Input voltage		V_I (all except X1, X2, AV_{REF})	$V_I < BV_{DDx}$ + 0.5 V	-0.5 to +6.0	V
		AV_{REF}	$AV_{REF} < AV_{DD}$	-0.5 to +0.5	V
Input voltage	alphabetical Ports	V_{AN}	$V_{AN} < AV_{DD}$ +0.5 V	-0.5 to +6.0	V
Output current low	1 pin	I_{OL}		4.0	mA
	All pins			50	mA
Output current high	1 pin	I_{OH}		-4.0	mA
	All pins			-50	mA
Operating temperature		T_{OPR}	μPD703175(A), μPD703176A)	-40 ~ +85	°C
Storage temperature		T_{STG}		-65 ~ +150	°C

3.2 General Characteristics

3.2.1 Oscillator Characteristics

(T_A= -40 ~ +85°C, V_{DD0} = CV_{DD} = BV_{DDx} = 4.5 V to 5.5 V, V_{SSx} = CV_{SS} = BV_{SSx} = 0 V)

Table 3-3: Oscillator Characteristics

Resonator	Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Crystal oscillator	Oscillator Frequency (f_{XX})	f_{OSC}		6		8	MHz
	Oscillation Stabilization time	T_{OST}	After V_{DD0} reaches, oscillator voltage range MIN. 4.5 V			TBD **Note**	ms
Ceramic oscillator	Oscillator Frequency (f_{XX})	f_{OSC}		6		8	MHz
	Oscillation Stabilization time	T_{OST}	After V_{DD0} reaches, oscillator voltage range MIN. 4.5 V			TBD **Note**	ms

Note: Max. stabilization time depends to particular crystal or Ceramic characteristics.

3.2.2 PLL Characteristics

(T_A= -40 ~ +85°C)

Table 3-4: PLL Characteristics

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
PLL lock time	T_{PLL}	OSC MODE PLL on and PLL off			1	ms

3.2.3 I/O Capacitances

(T_A = 25°C, V_{DD5x} = V_{SS5x} = 0 V)

Table 3-5: I/O Capacitances

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	f_C = 1 MHz Unmeasured pins returned to 0 V			15	pF
Input/output capacitance	C_{IO}				15	pF
Output capacitance	C_O				15	pF

3.3 Operating Conditions

Table 3-6: Operating Conditions

Clock Mode	Operation Mode	Operating Temperature (T_A)	Supply Voltage (V_{DDx})	Inside Operation Clock Frequency
OSC Mode, PLL on	ALL Modes	-40 ~ +85°C	4.5 V ≤ V_{DDx} ≤ 5.5 V	12 MHz ≤ f_{CPU} ≤ 32 MHz
OSC Mode, PLL off				6 MHz ≤ f_{CPU} ≤ 8 MHz

3.4 DC Characteristics

(T_A = -40 ~ +85°C, V_{DD0} = CV_{DD} = BV_{DDx} = 4.5 V to 5.5 V, V_{SSx} = CV_{SS} = BV_{SSx} = 0 V)

Table 3-7: DC Characteristics

Parameter		Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
High level Input voltage	P00-P02, P10-P15, P20-P25, P30-P35, P40-P45, $\overline{\text{RESET}}$	V_{IH1}		0.8 BV_{DDx}		BV_{DDx}	V
Low level Input voltage		V_{IL1}		BV_{SSx}		0.2 BV_{DDx}	V
High level Input voltage	PDL0-PDL15, PDH0-PDH8, PCM0-PCM3, PCD2-PCD3, PCT0, PCT1, PCT4, PCT6, NMI	V_{IH2}		0.7 BV_{DDx}		BV_{DDx}	V
Low level Input voltage		V_{IL2}		BV_{SSx}		0.3 BV_{DDx}	V
High level Input voltage	P70-P713 (Port shared with ANIx**Note**	V_{IHT}		0.7 BV_{DDx}		BV_{DDx}	V
Low level Input voltage		V_{ILT}		0		0.3 BV_{DDx}	V
High level Output voltage		V_{OH1}	I_{OH} = -3.0 mA	BV_{DDx}-1.0		BV_{DDx}	V
Low level Output voltage		V_{OL1}	I_{OL} = 3.0 mA	0		0.4	V
High level Input leakage current	V_I = BV_{DDx} V_I = REGC_O	I_{LIH}	V_I = V_{DD5}			5	μA
Low level Input leakage current		I_{LIL}	V_I = 0 V			-5	μA

Note: P7 can only be use as digital input port when AV_{DD} = V_{DD}.

Table 3-8: Power Supply Currents

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Supply Current **Note 1** Flash version	I_{DD1}	Operating mode **Note 2**		100	150	mA
	I_{DD2}	HALT mode **Note 3**		50	75	mA
	I_{DD3}	IDLE mode		9	13.5	mA
	I_{DD4}	WATCH mode **Note 4**		1	1.5	mA
	I_{DD5}	STOP mode		50	300	μA
Supply Current **Note 1** mask 32 MHz version	I_{DD1}	Operating mode **Note 2**		100	150	mA
	I_{DD2}	HALT mode **Note 3**		50	75	mA
	I_{DD3}	IDLE mode		9	13.5	mA
	I_{DD4}	WATCH mode **Note 4**		1	1.5	mA
	I_{DD5}	STOP mode		50	300	μA
Supply Current **Note 1** mask 24 MHz version	I_{DD1}	Operating mode **Note 2**		75	113	mA
	I_{DD2}	HALT mode **Note 3**		38	56	mA
	I_{DD3}	IDLE mode		7	10.5	mA
	I_{DD4}	WATCH mode **Note 4**		1	1.5	mA
	I_{DD5}	STOP mode		50	300	μA

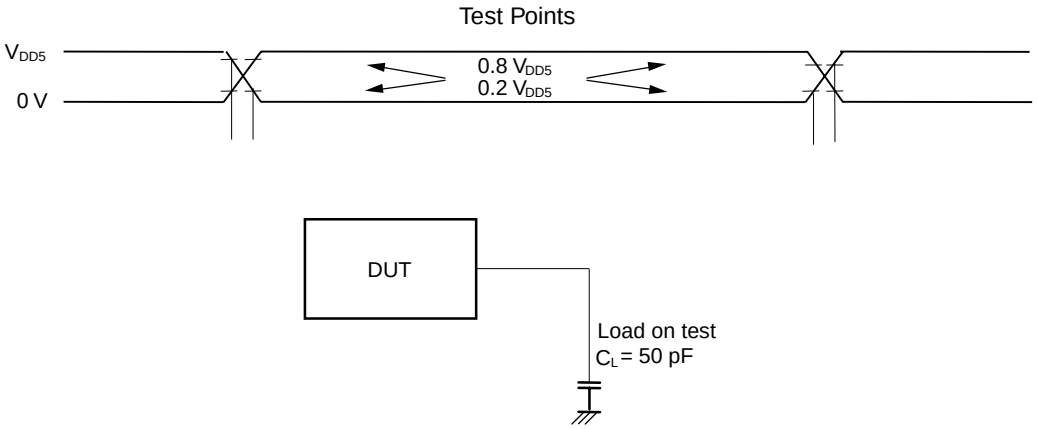
Notes:
1. AV_{REF} current, port current are not included.
2. $f_{CPU} = 4f_{XX}$: f_{XX} = 8 MHz for 32 MHz version, f_{XX} = 6 MHz for 24 MHz, peripheral functions operating
3. f_{XX} = 8 MHz, CPU stopped, peripheral functions operating with highest speed with PLL multiplied clock.
4. f_{XX} = 8 MHz, CPU stopped, all peripheral functions stopped (Watch timer and Watchdog timer operating).

3.5 AC Characteristics

3.5.1 General

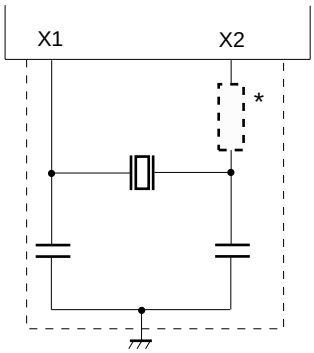
(T_A = -40 ~ +85°C, V_{DD0} = CV_{DD} = BV_{DDx} = 4.5 V to 5.5 V, V_{SSx} = CV_{SS} = BV_{SSx} = 0 V)

Figure 3-1: AC Test Input Waveform, AC Test Load Condition



3.5.2 Oscillator Recommendations

Figure 3-2: Oscillator Recommendations



*: This resistor is optional and depends of resonator supplier

Note: Values of capacitors depends on used resonator and must be specified in cooperation with manufacturer.

3.5.3 Clock

Table 3-9: Clock AC Characteristics

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
X1, X2 oscillator frequency	f_{OSC}	OSC MODE	6	8	MHz

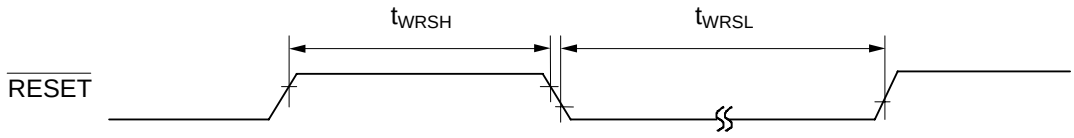
3.5.4 RESET (power up/down sequence)

Table 3-10: Reset Timing

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
$\overline{\text{RESET}}$ high-level width	t_{WRSH}		500		ns
$\overline{\text{RESET}}$ low-level width	t_{WRSLW}	During WATCH mode	1		ms
	t_{WRSL0}	After power on, during STOP mode	TBD **Note**		ms
	t_{WRSL1}	Other than above	500		ns

Note: The maximum time depends on the oscillation stabilization time of the external oscillator.

Figure 3-3: Reset Timing



3.5.5 Standby Mode Characteristics

Table 3-11: Standby Mode Timing

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
WATCH mode release time	t_{WATCH}	After WATCH mode release	1 **Note**		ms
STOP mode release time	t_{STOP}	After STOP mode release	TBD **Note**		ms

Note: This is the minimum time required for internal stabilization. If STOP mode is released by reset, OSC stabilization must be ensured by active reset (please see Table 3-10, “Reset Timing,” on page 25).

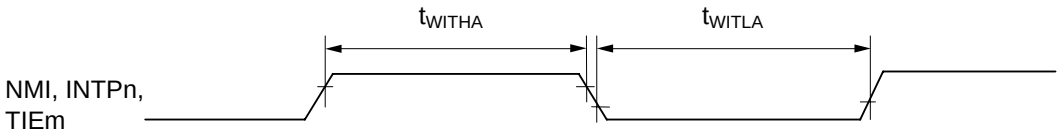
3.5.6 Interrupt Timing

Table 3-12: Interrupt Timing

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
NMI, INTPn, TIEm high-level width	t_{WITHA}		500		ns
NMI, INTPn, TIEm low-level width	t_{WITLA}		500		ns

Remark: n = 0 - 10
m = 1 - 4

Figure 3-4: Interrupt Timing



3.6 Peripheral Function Characteristics

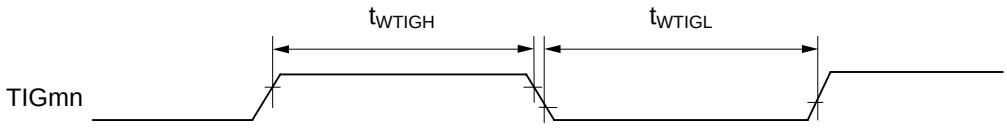
3.6.1 Timer G

Table 3-13: Timer G Characteristics

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
TIGmn input high-level width **Note**	t_{WTIGH}		TMGn count clock × 2 + 20		ns
TIGmn input low-level width **Note**	t_{WTIGL}		TMGn count clock × 2 + 20		ns

Note: n = 0, 1 and m = 0,..., 5

Figure 3-5: Timer G Characteristics



3.6.2 CSI

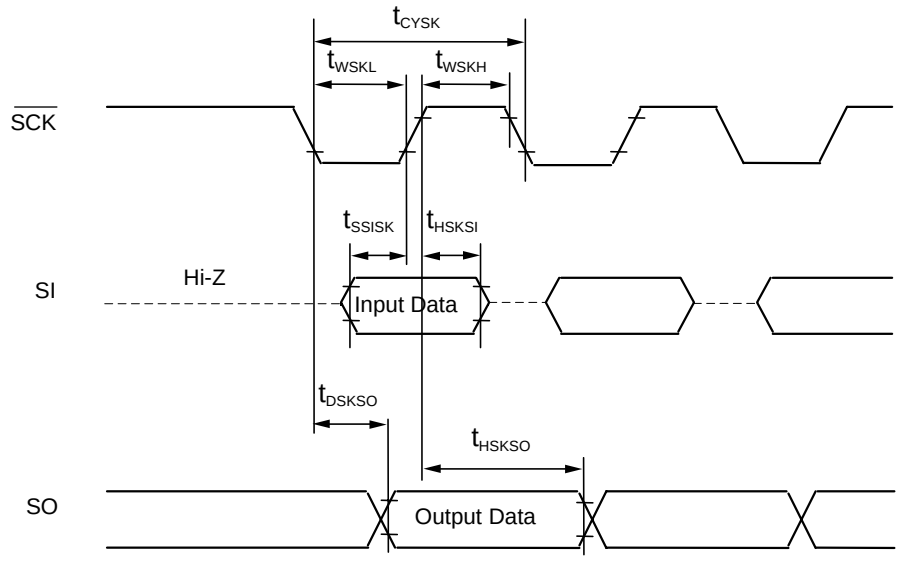
Table 3-14: CSI Master Mode Characteristics

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
$\overline{SCK}$ cycle time	t_{CYSK}	Output	125		ns
$\overline{SCK}$ high level width	t_{WSKH}	Output	0.5 t_{CYSK} - 10		ns
$\overline{SCK}$ low level width	t_{WSKL}	Output	0.5 t_{CYSK} - 10		ns
SI set up time (to $\overline{SCK}$ ↑)	t_{SSISK}		40		ns
SI hold time (from $\overline{SCK}$ ↑)	t_{HSKSI}		30		ns
SO output delay time (from $\overline{SCK}$ ↓)	t_{DSKSO}			30	ns
SO output hold time (from $\overline{SCK}$ ↑)	t_{HSKSO}		5		ns

Table 3-15: CSI Slave Mode Characteristics

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
$\overline{SCK}$ cycle time	t_{CYSK}	Input	125		ns
$\overline{SCK}$ high level width	t_{WSKH}	Input	0.5 t_{CYSK} - 10		ns
$\overline{SCK}$ low level width	t_{WSKL}	Input	0.5 t_{CYSK} - 10		ns
SI set up time (to $\overline{SCK}$ ↑)	t_{SSISK}		40		ns
SI hold time (from $\overline{SCK}$ ↑)	t_{HSKSI}		30		ns
SO output delay time (from $\overline{SCK}$ ↓)	t_{DSKSO}			50	ns
SO output hold time (from $\overline{SCK}$ ↑)	t_{HSKSO}		t_{WSKH}		ns

Figure 3-6: CSI Slave Mode Characteristics



3.6.3 UART

Table 3-16: UART Characteristics

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
Transfer rate	T_{UART}	$f_{Periferal} \geq 5$ MHz		312500	bps

3.6.4 FCAN

Table 3-17: FCAN Characteristics

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
Transfer rate	T_{FCAN}	$f_{CPU} \geq 16$ MHz		1	Mbps

3.6.5 A/D Converter

Table 3-18: A/D Converter Characteristics

(T_A = -40 ~ +85°C, $V_{VDD5x} = V_{AVDD}$ = 4.5 ~ 5.5 V, $V_{SS5x} = V_{AVSS}$ = 0 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Resolution	-				10	Bit
Overall Error **Note 1**	-				± 3	LSB
Conversion Time **Note 2**	t_{CONV}		5		12	μs
Analog Input Voltage	V_{IAN}				AV_{REF}	V
Reference Voltage	AV_{REF}				AV_{DD}	V
Reference Voltage input current **Note 4**	I_{AVREF}	$AV_{REF} = AV_{DD}$		1	2	mA

Notes: 1. Quantization error is not included

2. t_{CONV} depends on register ADSCM1

3. t_{SAM} depends on register ADSCM1

4. If ADC is set to standby mode, AV_{REF} can be disconnected externally (left open) to reduce current consumption.

3.7 Flash EPROM Characteristics

Table 3-19: Flash EPROM Programming Characteristics Basic Specification

Parameter	Symbol	Test conditions	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{DD}		4.5		5.5	V
	V_{PPL}	Low input	-0.3		+0.3	V
	V_{PPH}	Programming mode	7.5	7.8	8.1	V
Supply current	I_{PP1}			60	90	mA
Maximum times of reprogramming	C_{WRT}				100	times
Write time	t_{IWRTW}	Word (32-bit)		20	200	μs
Erase time	t_{ERASCB}	Block (128 K)		0.2	20	s
	t_{ERASCC}	Chip (256 K)		0.4	40	s
Programming temperature	t_{PRG}		0		+70	°C

Table 3-20: Flash EPROM Serial Programming Operation Characteristics

Parameter	Symbol	Test conditions	MIN.	TYP.	MAX.	Unit
V_{DD0} ↑ setup time to V_{PP} ↑	t_{VDD5SU}		1.0			ms
V_{DD5X} ↑ hold time to V_{PP} ↑	t_{VDD5HD}		1.0			ms
V_{DD5X} ↑ setup time to $\overline{RESET}$ ↑	t_{DRRR}		10			μs
V_{PP}↑ setup time to $\overline{RESET}$ ↑	t_{PSRRF}		1			μs
$\overline{RESET}$ ↑ count start setup time (to V_{PPH} level)	t_{RFOF}	$V_{PP} = V_{PPH}$, $T = 1/f_{XX}$	5T + 500			μs
Times of V_{PP} counting	t_{COUNT}				10	ms
V_{PP} count High level width	t_{CH}		1			μs
V_{PP} count low level width	t_{CL}		1			μs

Note: $T = 1 / f_{CPU}$

Figure 3-7: V_{DD0} Setup / Hold Time for V_{PP} Terminal

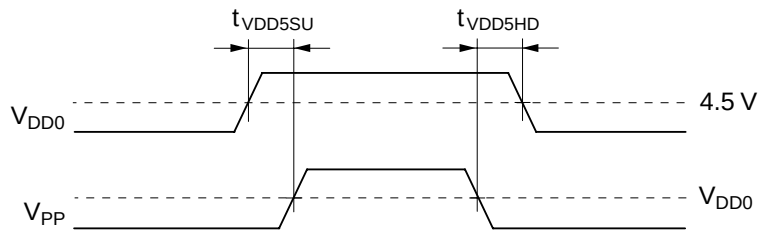
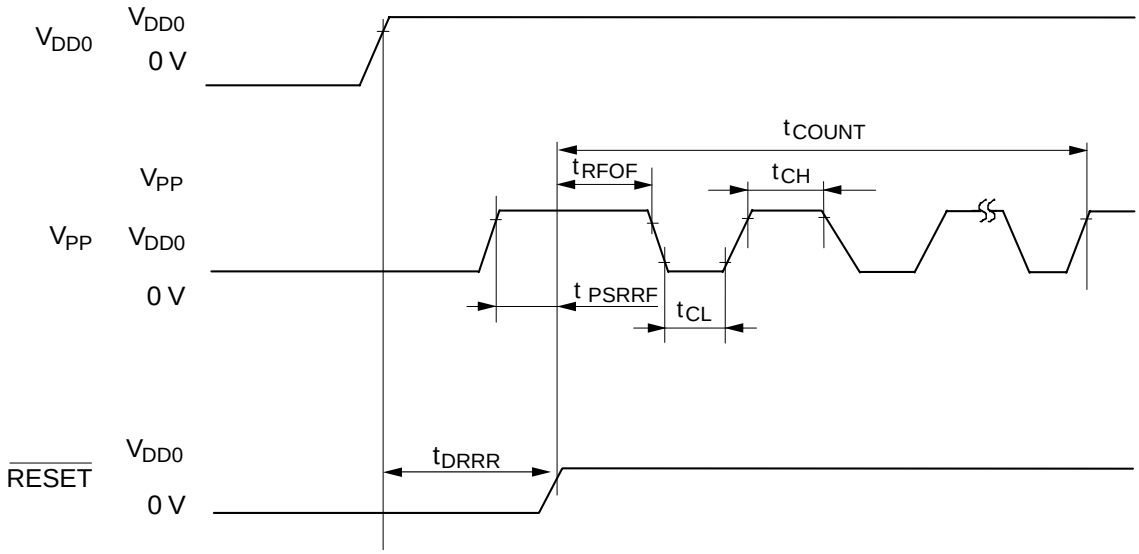


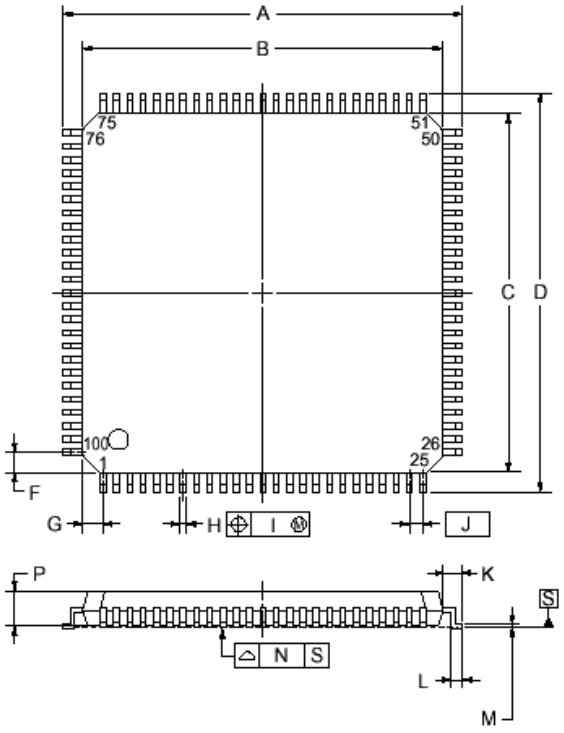
Figure 3-8: Flash EPROM Serial Programming Operation Characteristics

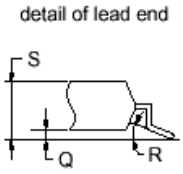


4. Package Drawing

- 100-PIN PLASTIC LQFP (FINE PITCH) (14 × 14)

Figure 4-1: Package Drawing





ITEM	MILLIMETERS
A	16.00±0.20
B	14.00±0.20
C	14.00±0.20
D	16.00±0.20
F	1.00
G	1.00
H	$0.22^{+0.05}_{-0.04}$
I	0.08
J	0.50 (T.P.)
K	1.00±0.20
L	0.50±0.20
M	$0.17^{+0.03}_{-0.07}$
N	0.08
P	1.40±0.05
Q	0.10±0.05
R	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$
S	1.60 MAX.

S100GC-50-8EU, 8EA-2

5. Revision History

Version	Date	Author	Remarks

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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