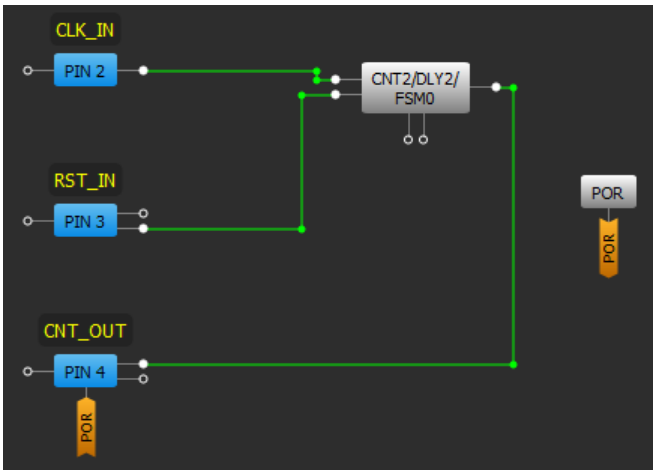
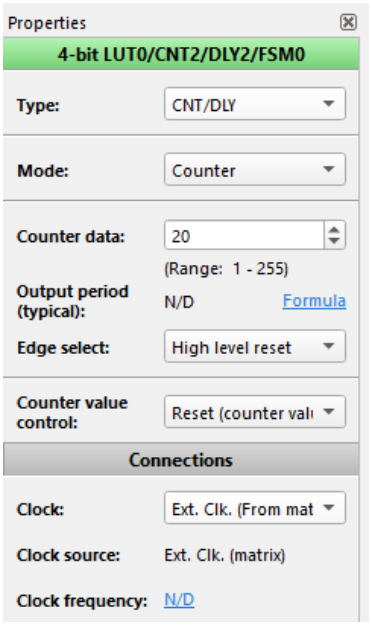
SLG46108

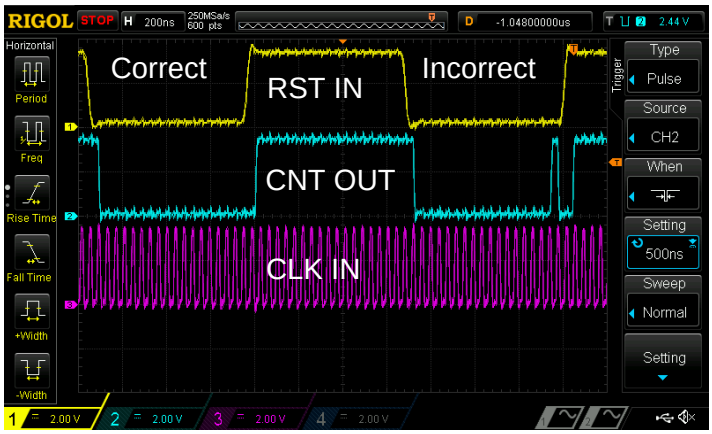
ISSUE 1: Incorrect Counter Operation after the Reset
Functional Block Affected: Counter

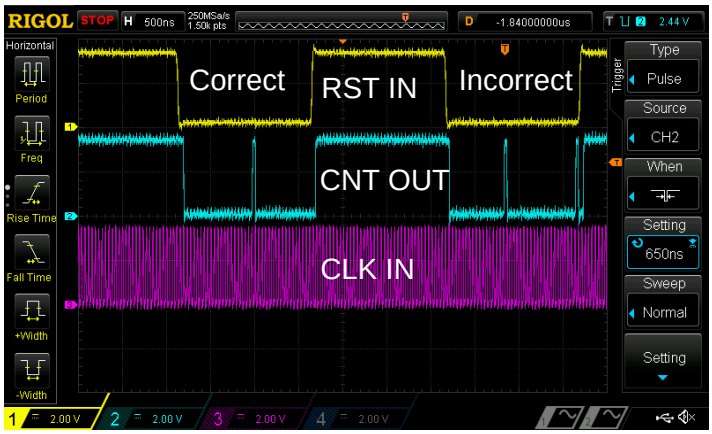
Description:

If the Counter Reset is asserted at the same time as a rising clock edge, it is possible that the Counter Data will be reset incorrectly and the counter output may appear faster than expected, it doesn't depend on Edge select option. This phenomenon appears more often as the clock frequency increases.



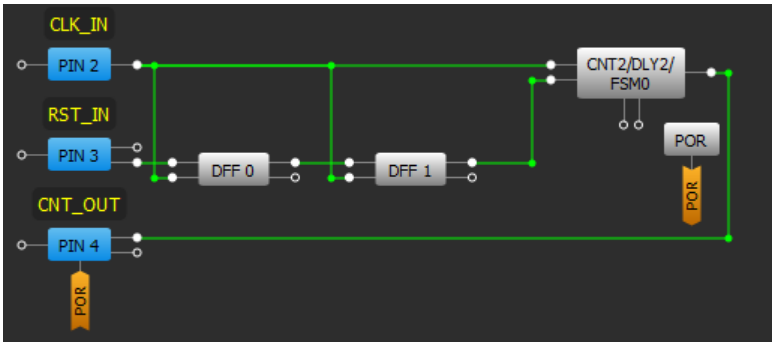






Workaround:

- Synchronize the RESET input of the Counter with its CLK using 2 DFF cells as shown in the image below.



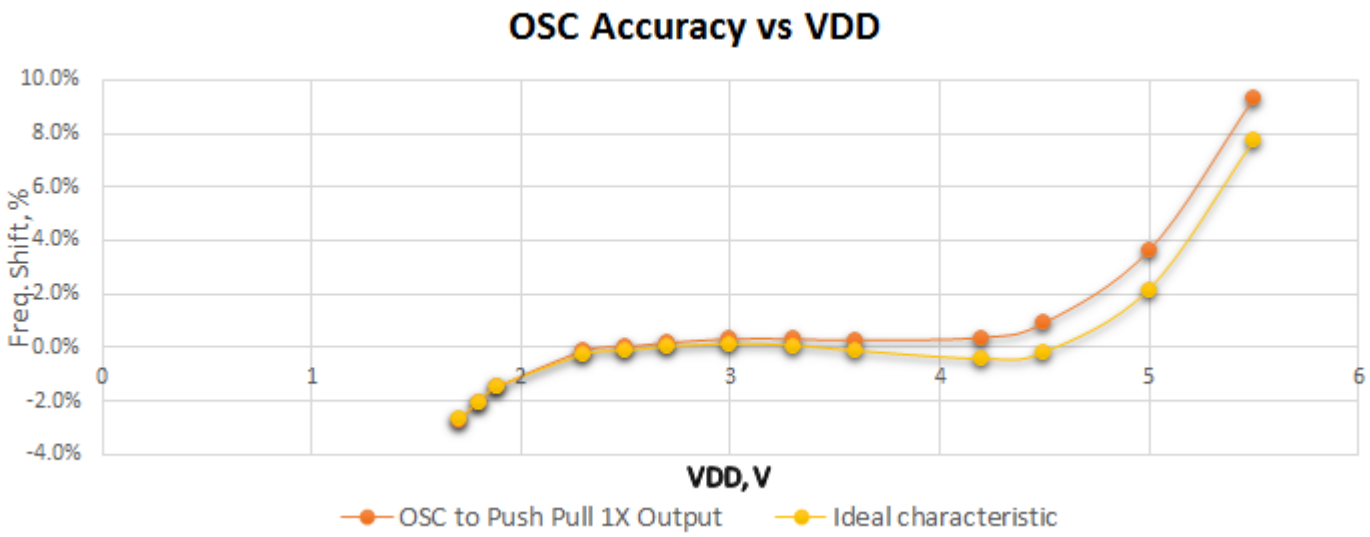
ISSUE 2: VDD Noise Influences OSC Variation
Functional Blocks Affected: OSC, Counter/Delay

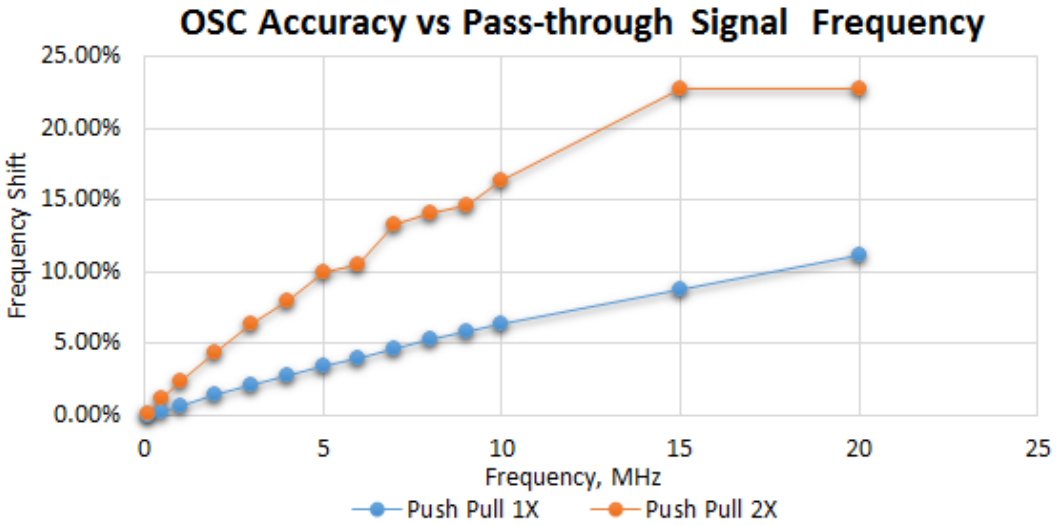
Description:

White applying some high frequency noise to the VDD, OSC inaccuracy may increase. The same behavior is also present in cases where high frequency switches are outputted from the chip using the Push Pull type driver. See, test results below.

Additional frequency Shift by different PINs.

VDD =5 V Trim VDD = 3.3 V	Push Pull 1X	Push Pull 2X	Push Pull 1X	Push Pull 2X
OUT PIN #	f shifted, %	f shifted, %	average	average
4	1.42 %	3.63 %	1.52 %	3.81 %
6	1.67 %	4.03 %		
7	1.62 %	3.98 %		
8	1.38 %	3.59 %		
4 … 8	6.73 %	11.98 %		





Workaround:

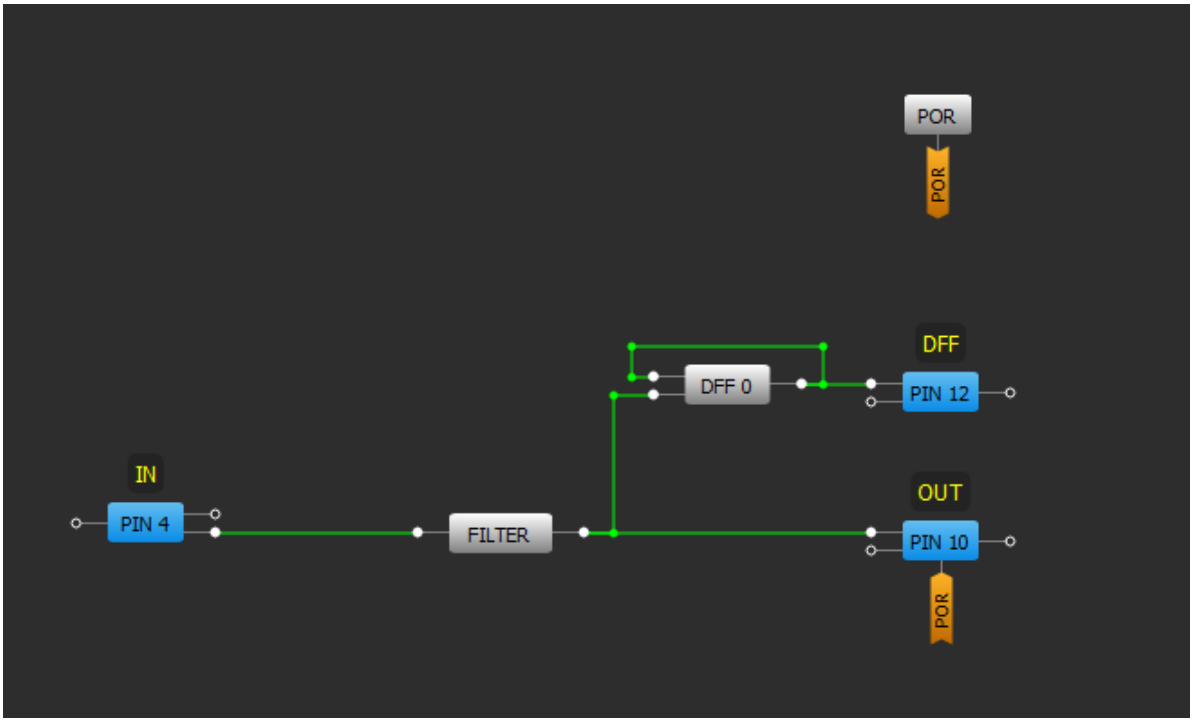
Currently there are no viable workarounds for this issue.
However, the issue can be minimized by doing the following:

- Only use frequencies lower than 2 MHz when switching the output.
- Do not use parallel PIN connections to output high speed switching signals.

ISSUE 3: FILTER Cell Does Not Filter Out Glitches
Functional Block Affected: FILTER

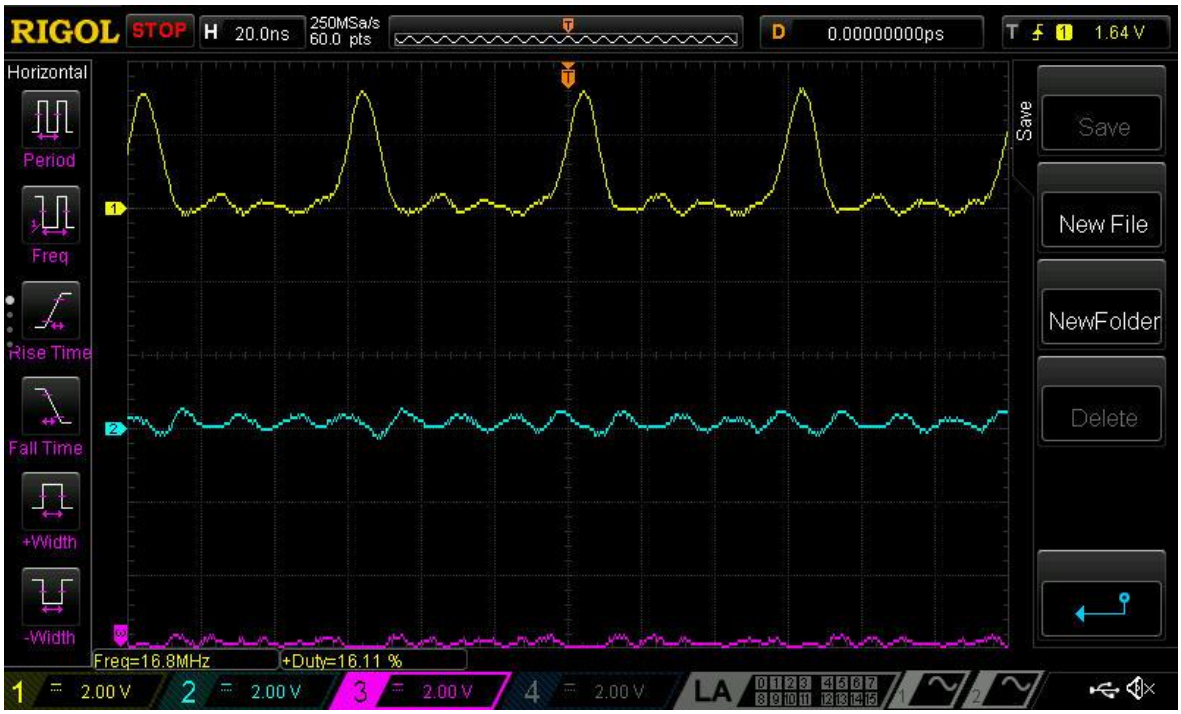
Description:

If clock type high frequency input comes in, the FILTER cell may not filter out it. There are several factors like input frequency, duty cycle and LOW duration in such signal that may lead to its passing through FILTER block.



Channel 1 (yellow/top line) – PIN#4 (IN).
Channel 2 (light blue/2nd line) – PIN#10 (OUT).
Channel 3 (magenta /3rd line) – PIN#12 (DFF).

1. Period is 60 ns. Pulse width is 10 ns, DC = 16.7 % (correct functionality).



2. Period is 60 ns. Pulse width is 20 ns, DC = 33.3 % (incorrect functionality).

3. Period is 60 ns. Pulse width is 30 ns, DC = 50 % (incorrect functionality).

4. Period is 60 ns. Pulse width is 40 ns, DC = 66.67 % (correct functionality).

Workaround:

Currently there is no workaround for this issue. Filter block is good at filtering short spontaneous glitches. It is intended to be used in series connection before the delay cell to avoid its latching (see issue #3).

ISSUE 4: Input Glitch Pattern Combination into DLYs Fails to Trigger Auto Power On of 25 kHz or 2 MHz OSC

Functional Blocks Affected: 25 kHz/2 MHz OSC

Effect:

Specific combinations of DLY inputs can fail to trigger Auto Power On to enable 25 kHz or 2 MHz OSC. Other OSC generators (25 MHz) do not have issue with Auto Power On setting.

Conditions:

Auto Power On can potentially fail to enable OSC when all following conditions are present together:

1. 25 kHz or 2 MHz OSC is in Auto Power On mode.
2. DLYs are clocked by such OSC.
3. Input to one more such DLY have glitches < 200 ns.
4. OR of OSC trigger signals from all DLYs clocked by same OSC together form a long+short glitch pattern with precise (ns) timings as shown in Figure 1. The trigger signal generation per DLY is detailed in section Description.
5. During glitch period, no other DLY is active, meaning has already enabled OSC.

Description:

OSC generators have an Auto Power On mode which can be selected to automatically power on the OSC only when needed, such as when a DLY needs to count OSC cycles to time the delay output, thereby reducing quiescent power. Each individual DLY starts waiting in an inactive state, and when upon receiving an input edge (of polarity set by DLY configuration) then sets its individual trigger signal high. For example, in a rising-edge DLY, a rising edge input sets this trigger high. For a falling-edge, the situation is inverted. In either case (or both edge DLY), the individual DLY trigger is reset if either an opposite edge is detected (therefore,

canceling the DLY function) or the DLY finishes timing its output upon reaching the desired count per its setting. Therefore, an input pulse shorter than the DLY time is filtered out. The global Auto Power On circuitry then takes the OR of all the individual DLY triggers and subsequently sends the master enable signal to activate the OSC.

For this chip, the Auto Power On circuitry of the 25 kHz/2 MHz generators contains a circuit errata, which can potentially fail to power on the OSC for a specific pattern and timing of the OR of all related DLY trigger signals. The pattern is shown in Figure 1 (boxed in red) and consists of a relatively longer pulse (~145 ns) followed by a shorter (~5 ns) glitch of opposite polarity.

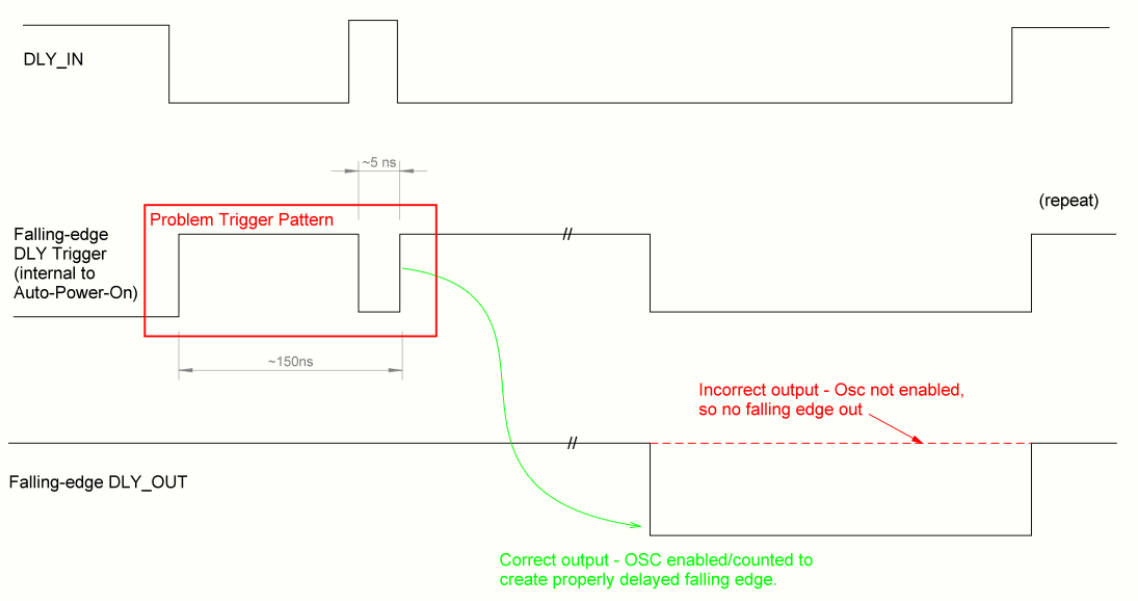


Figure 1: Problem Trigger Pattern

The error is difficult to capture as the timing must be exact within ns, and short (ns) pulses are difficult to generate glitch precise enough to induce the problem. GPIO naturally filter out ns pulses, so for purposes of errata capture, two simultaneous falling-edge DLY circuits (as shown in Figure 2) were used. By lining up two delays precisely at a particular timing relationship, we can use the internal Auto Power On (OR logic) to generate the glitch pattern necessary to cause the error.

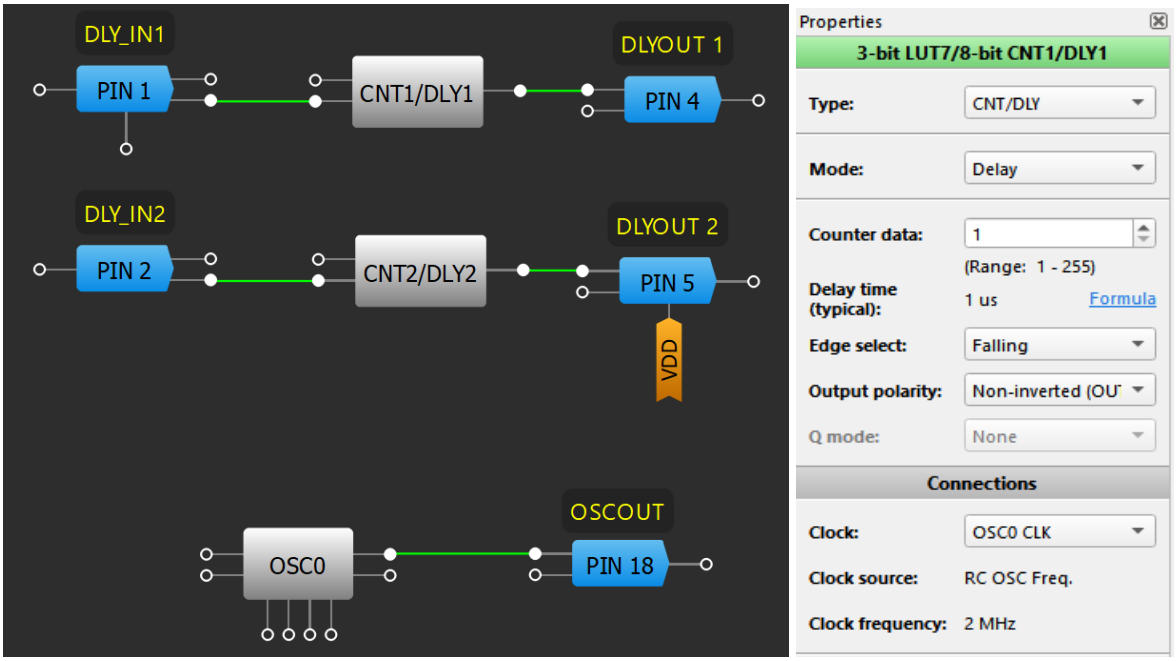


Figure 2: Test Circuit

Figure 3 shows a series of DLY output events are missing, where the OSC is correspondingly not triggering when it was supposed to. Figure 4 is a zoom in of the boxed region from Figure 3. The total glitch/chatter time was measured in this case at 152 ns. By using the composite OR of the two delay channels, we can asynchronously strobe with tiny frequency variations, and so tune the timing to induce this errata. Note that the error is not persistent – the system is recovered when all DLYs are returned to inactive state, such as when input of falling edge DLY goes high, thus canceling delay, or after DLY out finishes.

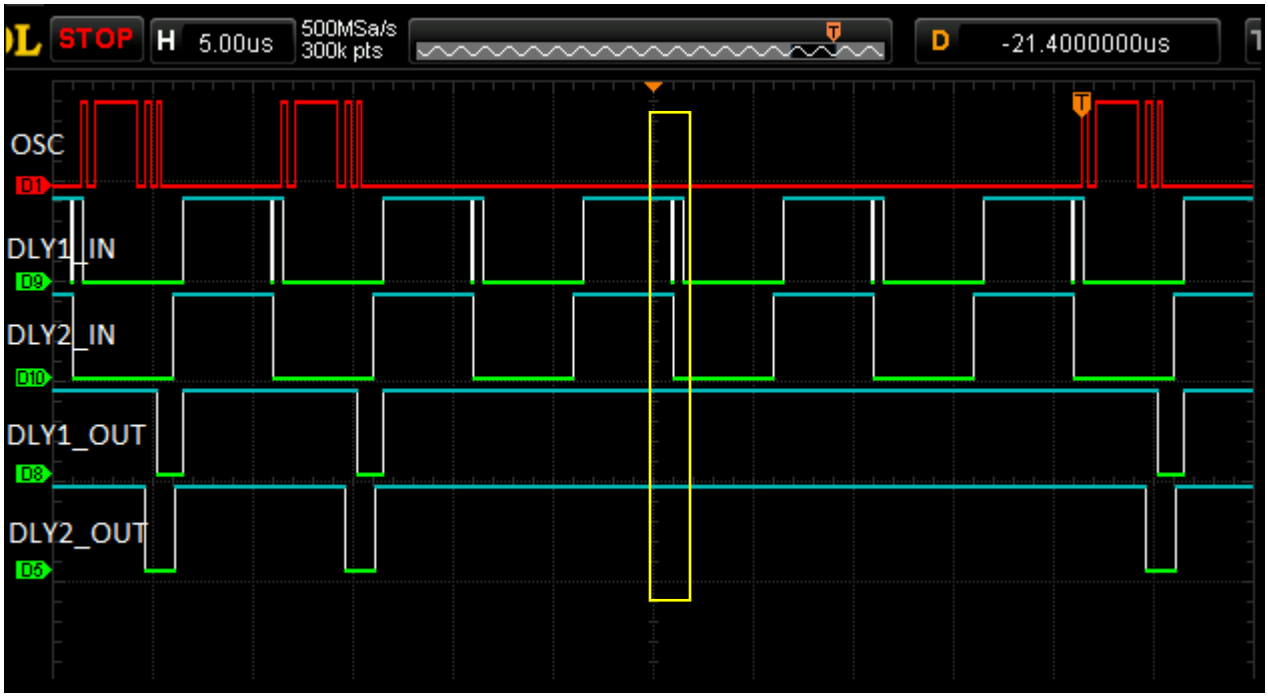


Figure 3: Errata Capture (Zoom Out)

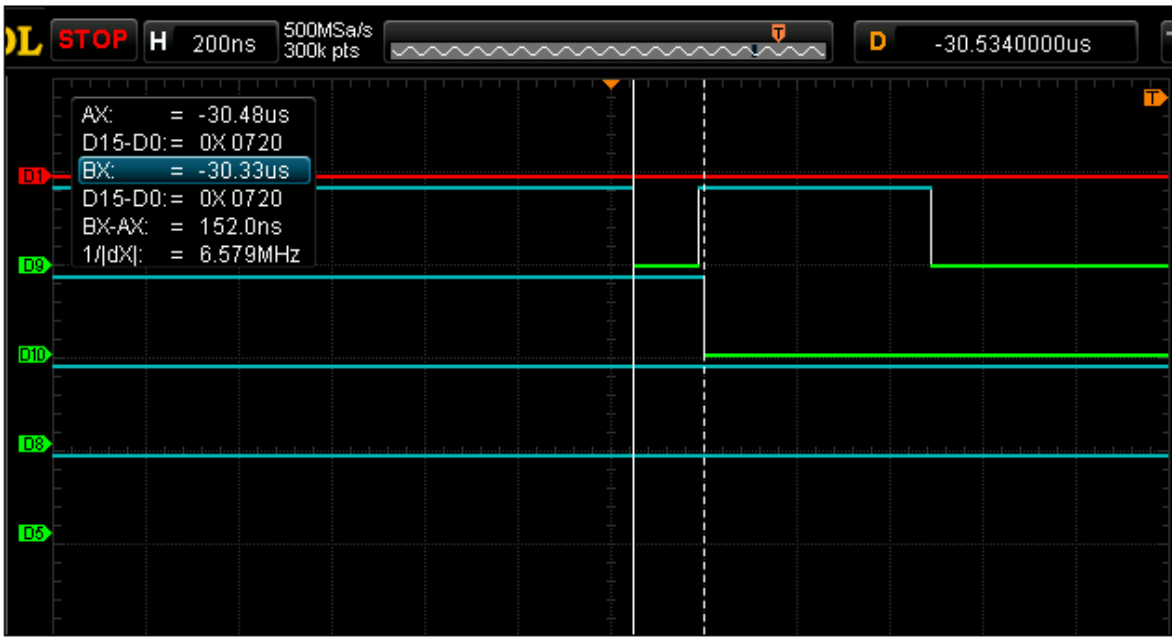


Figure 4: Errata Capture (Zoom In)

Workaround:

Any one of the following prevents the issue:

1. Use signal conditioning circuits to prevent glitch on DLY inputs < 200 ns. Examples:
   a. ACMP with Hysteresis
   b. External RC in front of Digital Input with Schmitt Trigger
   c. Filter cell.
2. Set OSC power mode to Force Power On mode instead of Auto Power On.
3. Use different oscillator, such as 25 MHz Ring OSC, which does not have Auto Power On issue.

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