Product part number: SLG46200

Active SLG46200 Errata List

1. Long delay time

Lot number: C839002FYY

If Delay1 or Delay2 is configured for time values above 100 – 400 ms (depending on process variations), a delayed output edge will be earlier than expected. Delay 0 is not affected by this issue.

Workaround:
Do not use delay times that are above 100 ms.
Or use the counter instead.

2. ADC PGA 0.5X gain accuracy

Lot numbers: C839002FYY
C839003FXX
C839004FXX

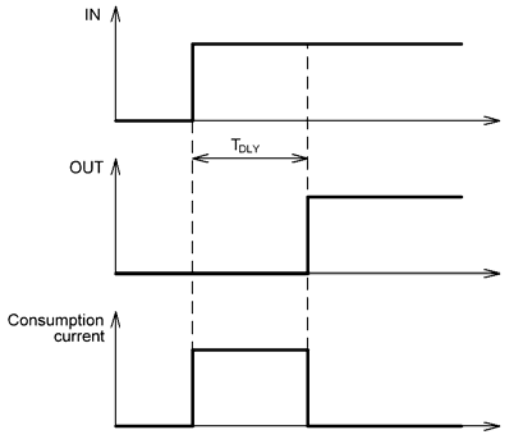
According to the datasheet and specifications ADC PGA has 0.5X gain. However, tested silicon has a measured value of 0.47X.

Workaround:
Use more accurate external voltage dividers.
If the ADC is used with DCMPs, error can be compensated by adjusting the DCMP register numbers.

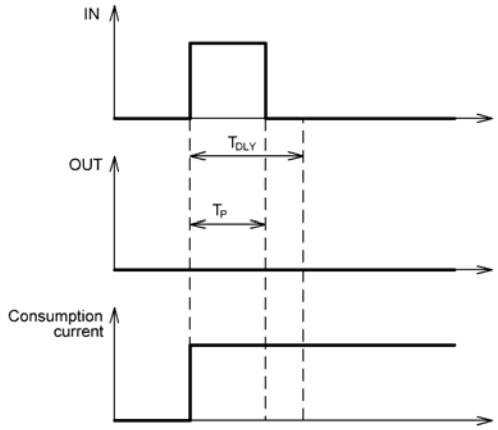
3. Delay blocks current consumption halt

Lot numbers: C839002FYY
C839003FXX
C839004FXX

Normal Delay block (rising edge) functionality



Incorrect Delay block (rising edge) functionality



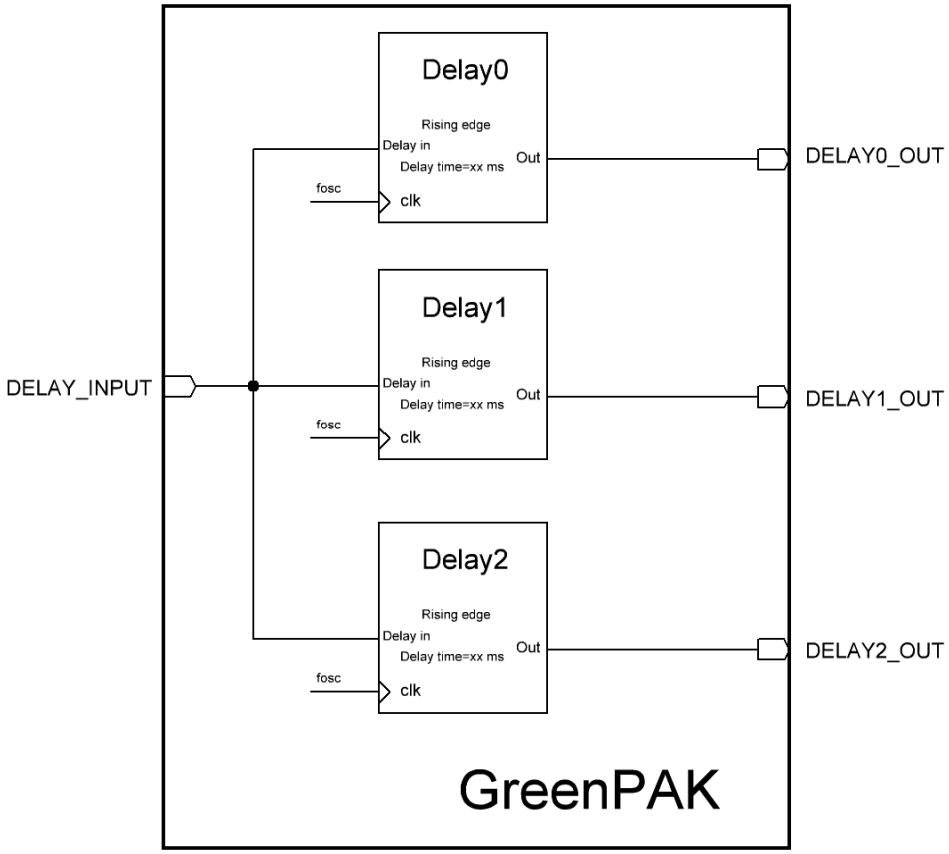
If the delay input pulse duration is less than the delay time (other blocks do not use internal RC oscillator), the output will be correct but the power consumption will stay high. This is due to the delay block that starts RC OSC work after detecting a corresponding edge and then shuts it down after the delay time has passed. If the input signal duration (T_P) is less than the delay time (T_{DLY}), then the RC OSC won't shut down (delay cell will not give the RC OSC shut down signal internally) and the power consumption will go on. If any other delay cell or other block that uses OSC gives a shut-down signal then current consumption will stop.

Workaround:
Either force the unused Counter/Delay (configured as Counter) block on and put 1 to its register.
Or make special internal protection circuits which will make the delay block count to the end.

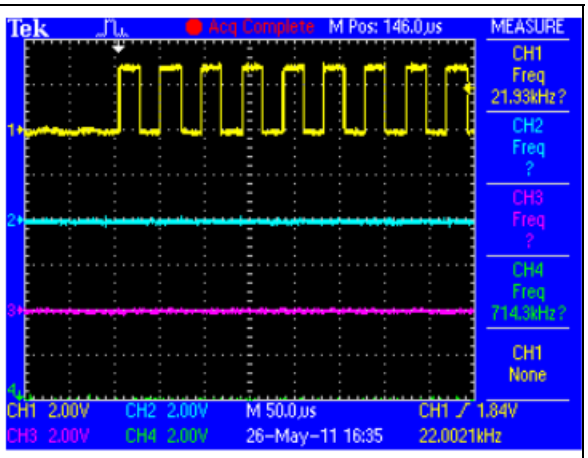
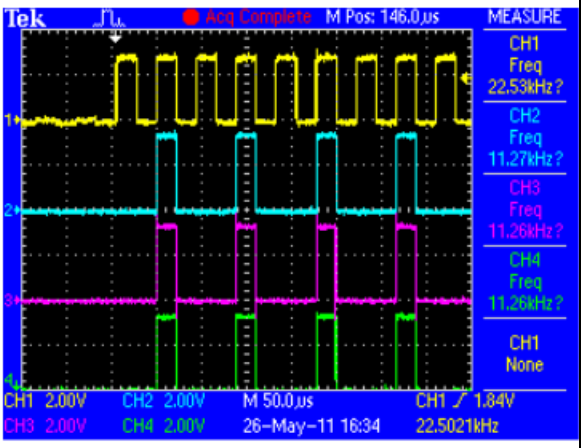
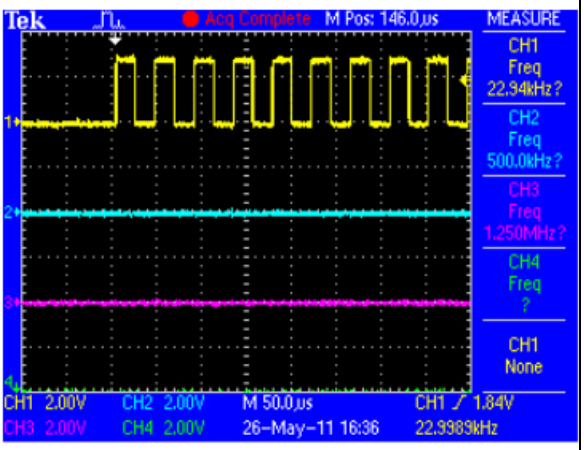
4. Delay blocks passing input signals to the output

Lot numbers: C839002FYY
C839003FXX
C839004FXX

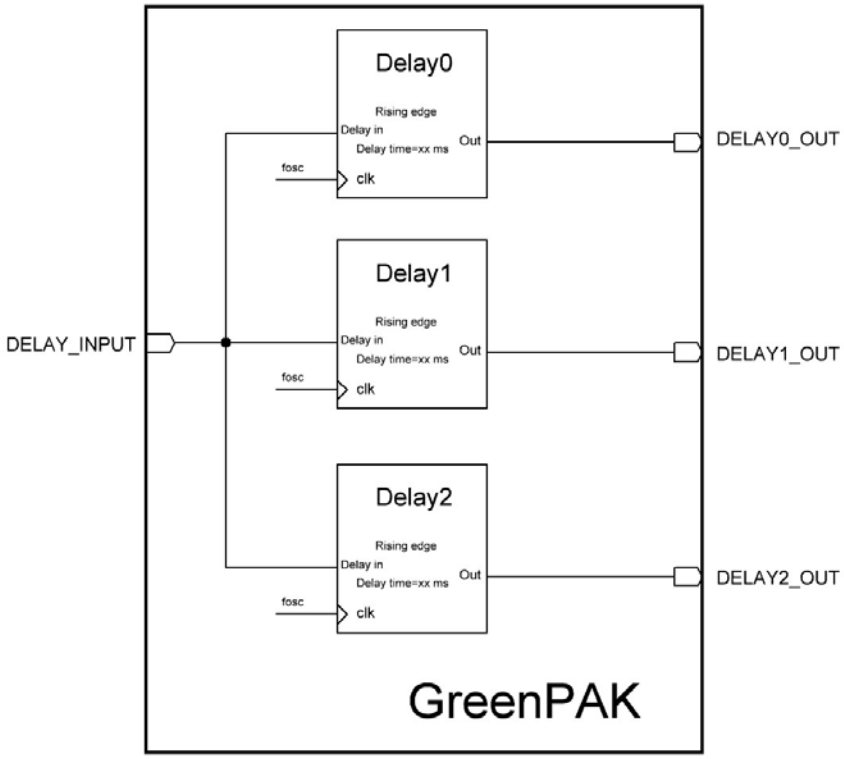
If time between two detected edges is approximately two times less than the delay clock period, then the input signal may pass to the delay output.

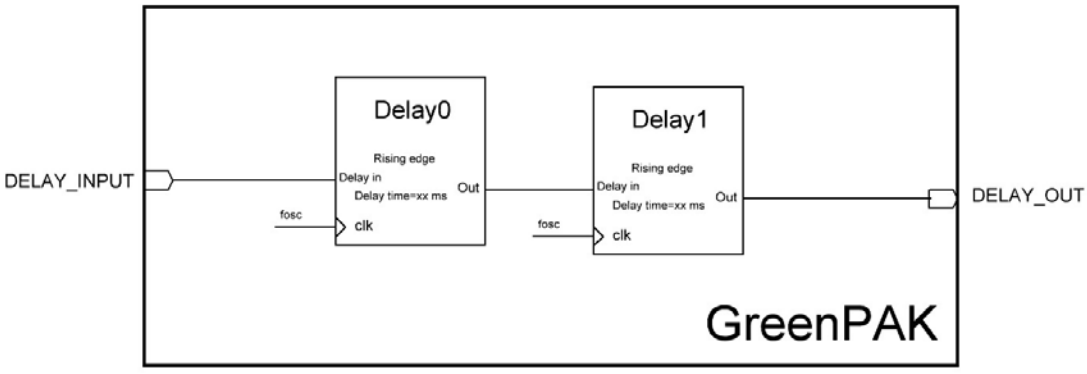


As an example the rising edge delay cell test results with internal RC oscillator frequency 43kHz are shown below.

ELAY_INPUT=22kHZ Delays function correctly	DELAY_INPUT DELAY0_OUT DELAY1_OUT DELAY2_OUT	 TDS 2014B - 16:35:42 26.05.2011
Delay_in=22.5kHZ (The input frequency value that causes incorrect functionality of delay blocks varies from chip to chip, duty cycle and delay clock value) Delays function incorrectly	DELAY_INPUT DELAY0_OUT DELAY1_OUT DELAY2_OUT	 TDS 2014B - 16:34:24 26.05.2011
Delay_in=23kHZ Delays function correctly	DELAY_INPUT DELAY0_OUT DELAY1_OUT DELAY2_OUT	 TDS 2014B - 16:36:18 26.05.2011

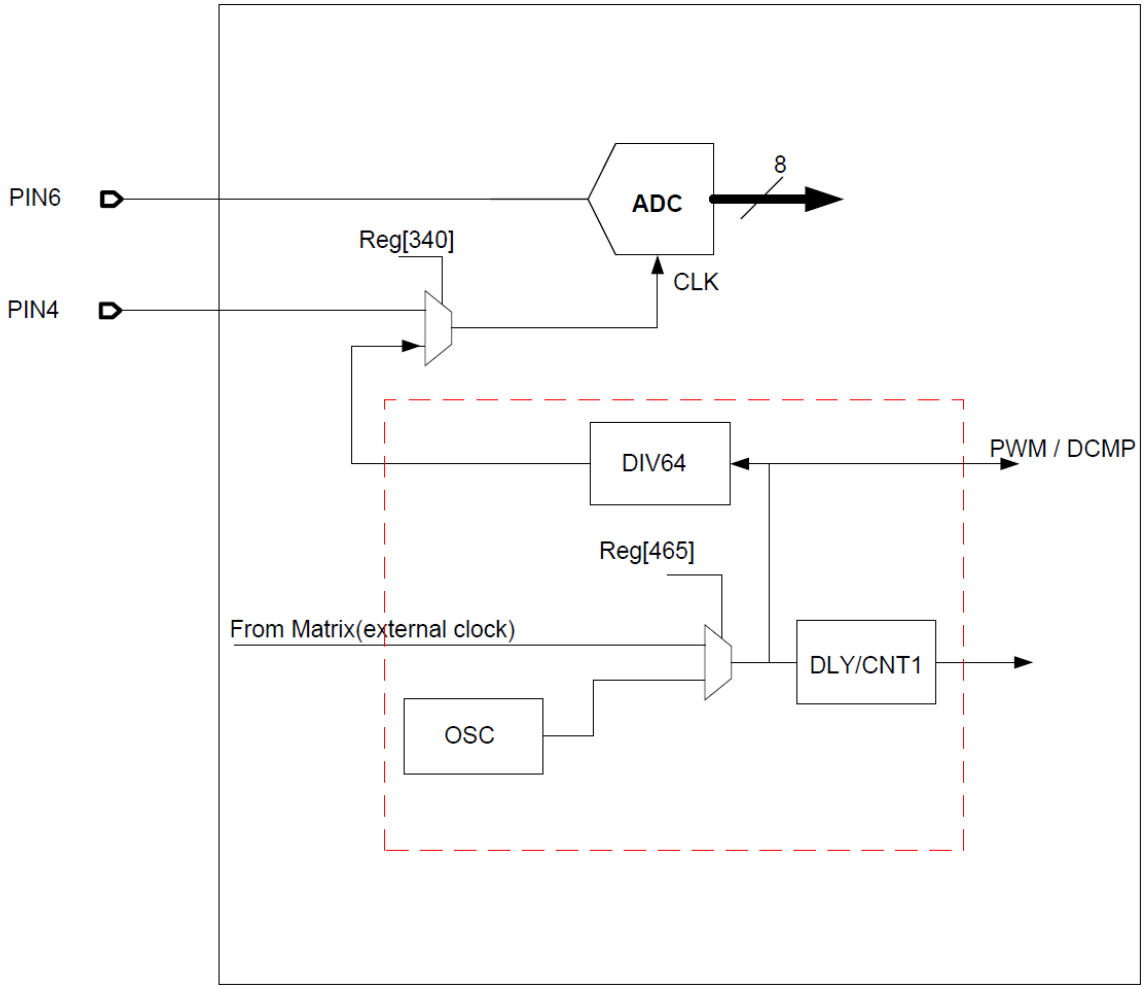
Workaround:
Use two Delay blocks in the series connection.





5. Analog-to-Digital Converter (ADC) using the Counter 1 clock.

Lot numbers: C839002FYY
C839003FXX
C839004FXX



The ADC uses Counter/Delay 1 clock source for sampling data. So if the Counter/Delay 1 clock is not connected, the ADC will not function at all.

Workaround:
Use the internal clock for Counter/Delay 1 for correct ADC functionality.

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