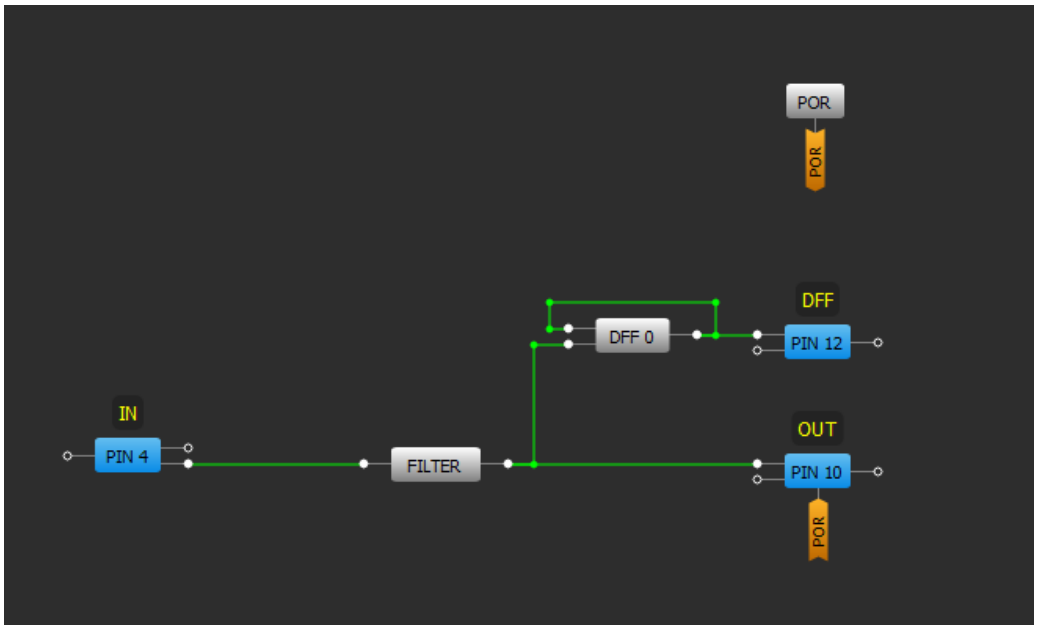
SLG46585

ISSUE 1: FILTER Cell does not Filter Out Repetitive Glitches
Functional Block Affected: FILTER

Description:

If the FILTER cell's input signal contains multiple consecutive pulses within short time intervals, the FILTER cell may not filter the input pulses as expected. The errant behavior applies only to repeated input pulses and depends on both their frequency and duty cycle.



Channel 1 (yellow/top line) – PIN#4 (IN).
Channel 2 (light blue/2nd line) – PIN#10 (OUT).
Channel 3 (magenta /3rd line) – PIN#12 (DFF).

1. Period is 60 ns. Pulse width is 10 ns, DC = 16.7 % (correct functionality).

2. Period is 60 ns. Pulse width is 20 ns, DC = 33.3 % (incorrect functionality).

3. Period is 60 ns. Pulse width is 30 ns, DC = 50 % (incorrect functionality).

4. Period is 60 ns. Pulse width is 40 ns, DC = 66.67 % (correct functionality).

Workaround:

Currently, there is no workaround for this issue. The FILTER block correctly filters isolated glitches, but it shouldn't be used to filter repetitive, high frequency input signals.

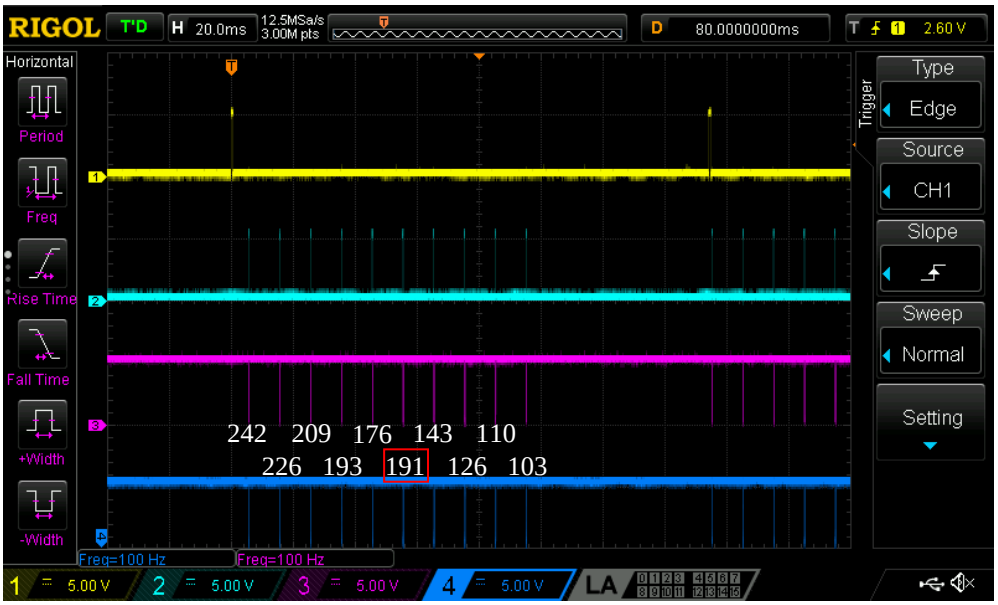
ISSUE 2: Incorrect I²C Reads of the 8-bit Counter Registers Functional Blocks Affected: CNT2/DLY2 and CNT4/DLY4

Description:

Asynchronous interaction between the CNT/DLY clock input and the I²C latch signal (generated by an I²C read command of the CNT/DLY block's count value) can result in an incorrect I²C data read. The CNT/DLY block will count accurately, but the count value transferred into the block's I²C read register might be loaded incompletely if the I²C latch signal and the clock input occur at about the same time.

The example data capture below shows ten periodic I²C reads of CNT2/DLY2 configured to count down at about 16 clocks per read. The sixth read sample erroneously shows a value greater than that of the fifth. The seventh sample reads as if the previous I²C error never occurred - the difference from the fifth sample (176) to the seventh (143) is 33 clocks or 16 clocks + 17 clocks as expected.

Channel 1 (yellow/top line) – PIN#2 (CNT2/DLY2 Out).
Channel 2 (light blue/2nd line) – PIN#1 (I²C Read Triggers).
Channel 3 (magenta /3rd line) – PIN#8 (I²C SCL).
Channel 3 (dark blue /4th line) – PIN#9 (I²C SDA).



Workaround:

If the possibility of incorrect I²C data reads can't be accommodated for by external software checks, one can guarantee proper operation by stopping the CNT/DLY block's clock during I²C reads through one of the following methods: by disabling the oscillator block, by reconfiguring the CNT/DLY block's clock source, or by gating an external clock using a LUT (Look-up Table) in the signal matrix. After disabling the CNT/DLY block's clock, the count registers can be read without error. Please note that this workaround will add the I²C read and processing time to the counter's overall clock period.

The best workaround depends on the resource constraints of the application. If the oscillator block doesn't clock other logic elements within the design, a matrix output can be used to manually power down the oscillators for the I²C read. When the CNT/DLY block's clock source is routed internally from the oscillator block, I²C commands can temporarily reconfigure the CNT/DLY block's clock source registers to select "Ext. CLK. (From Matrix)." This action will disable the clock by connecting it to ground. If the CNT/DLY block is clocked from the signal matrix, a LUT can be used to gate the clock during an I²C read.

ISSUE 3: Inaccurate Data Transfer between the RTC's Shadow Buffer and the RTC's Counter Registers

Functional Block Affected: RTC

Description:

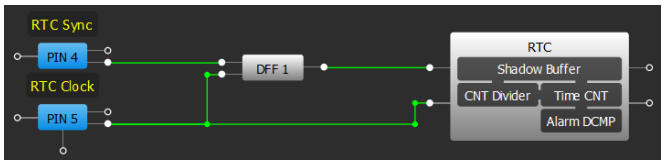
The SLG46585's I²C feature uses an internal shadow buffer to read from and write to the RTC's count registers. The data transfer between the count registers and the shadow buffer can be triggered through either the RTC block's Sync input or I²C.

Issue 2 describes an issue related to asynchronously clocking and latching data for I²C reading in various CNT/DLY blocks. Similar behavior affects the RTC block. When triggered by an I²C read, the data transfer from the counter registers to the shadow buffer will produce the correct results, but when the I²C block is used to write data to the counter registers or when the Sync input triggers the data transfer, a simultaneous rising edge of the Clock input might corrupt the data in the middle of a transfer.

Workaround:

As described in Issue 2, one can guarantee proper operation with I²C by disabling the clock of the RTC block during I²C reads and writes. This can be done by disabling the oscillator clocking the RTC or by gating the matrix clock using a LUT.

Alternatively, if the Sync input is used, one can synchronize the Clock and Sync inputs using a DFF as shown below. This method requires the RTC's Sync input to have an active high pulse width that exceeds 1.5 times the period of the Clock input.



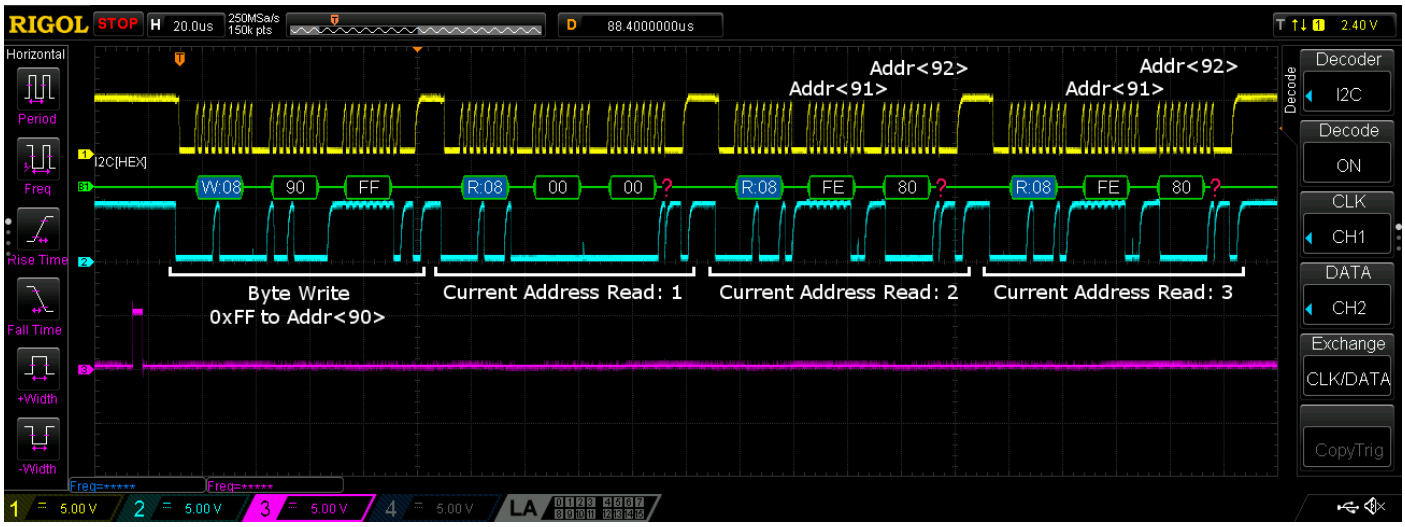
ISSUE 4: Invalid I²C Data Return for Initial "Current Address Read" or "Sequential Read" after an I²C Write

Functional Block Affected: I²C

Description:

The first "Current Address Read" or "Sequential Read" command following an I²C "Byte Write" or a "Sequential Write" command will produce incorrect data. Additional read commands will return the expected data. See the waveform below for more information.

Channel 1 (yellow/top line) – PIN#8 (SCL).
Channel 2 (light blue/2nd line) – PIN#9 (SDA).
Channel 3 (magenta /3rd line) – I²C Software Trigger.
Note: In the GreenPAK test design, Addr<91> and Addr<92> expect FE and 80 respectively.



Workaround:

If possible, use the “Random Read” command as described in the datasheet for SLG46585. This command will output the correct data.

If you expect consecutive reads of the same register, we recommend sending a “Random Read” command to the register preceding the register of interest. After the “Random Read” command finishes, the chip’s register pointer will increment to the desired register and the following “Current Address Read” or “Sequential Read” commands will produce the correct data. Note that the “Current Address Read” and “Sequential Read” commands don’t increment the GreenPAK’s register pointer.

ISSUE 5: DC_VOUT Glitch during Powerup if DC/DC ON/OFF is Enabled when the Maximum DC_VOUT to DC_VIN Duty Cycle Ratio is Exceeded. Applies only to DC_VOUT Selections 2.5 V, 3.0 V, and 3.3 V.

Functional Block Affected: DC/DC Step Down Converter

Description:

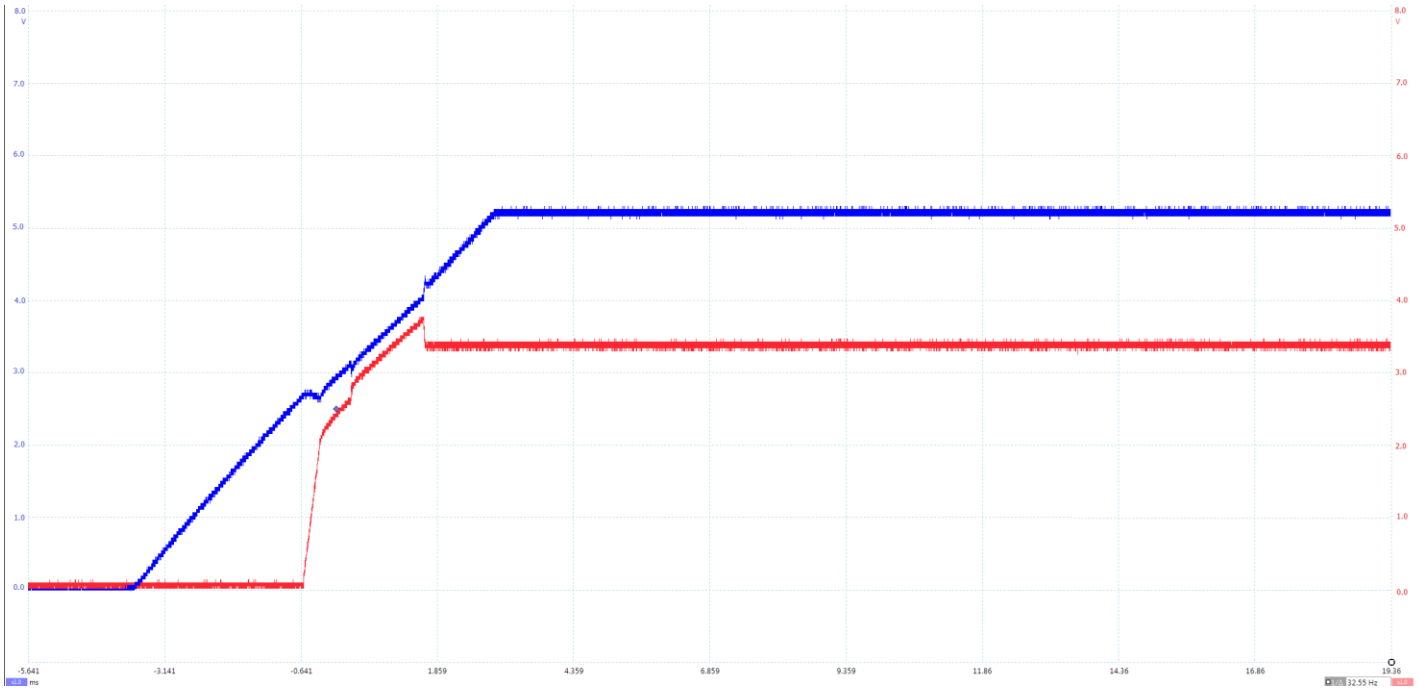
The maximum DC_VOUT to DC_VIN duty cycle ratio is 80 % for fsw=1.5 MHz and 75 % for fsw=2 MHz (See Table 20 in Datasheet section 5.11 parameter *Maximum Duty Cycle*). This voltage glitch issue only occurs if the DC_VOUT to DC_VIN ratio exceeds this maximum, meaning DC_VIN does not have enough headroom above DC_VOUT.

For DC_VOUT selections 1.2 V, 1.5 V, and 1.8 V, the UVLO can block the ON/OFF signal from enabling the DC/DC Buck Converter until DC_VIN is greater than 2.3 V. However, for selections 2.5 V, 3.0 V, and 3.3 V, which are greater than the UVLO threshold, there is no protection against enabling the DC/DC while the DC_VIN does not satisfy the Maximum Duty Cycle ratio specified above.

This glitch can be seen in an application where there is a slow DC_VIN/VDD ramp and the DC/DC’s enable signal is tied to DC_VIN/VDD, as shown in the example capture below.

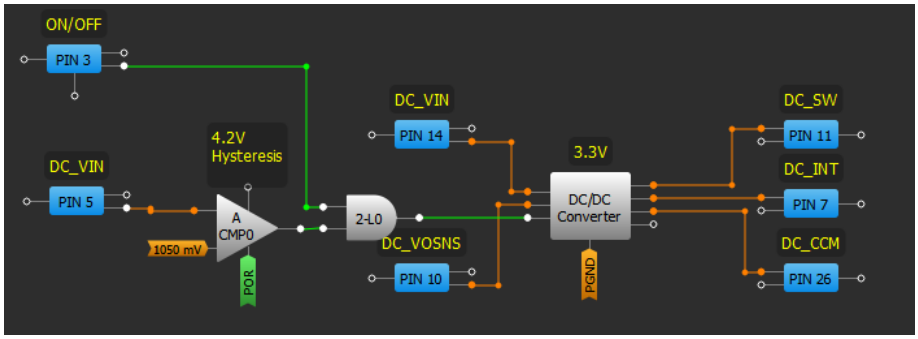
The example capture below shows DC_VIN/VDD ramping from 0 V to 5.5 V at 1 V/ms. The output voltage is set to 3.3 V.

Channel 1 (blue/top line) – PIN#14/PIN#16 (DC_VIN/VDD).
Channel 2 (red/2nd line) – PIN#10 (DC_VOSNS).



Workaround:

Use an ACMP to detect when DC_VIN is greater than DC_VOUT divided by Maximum Duty Cycle, and then AND the ACMP output with the ON/OFF signal.



ISSUE 6: ACMP Additional IN- Leakage Current

Functional Blocks Affected: ACMP, PIN

Description:

The SLG46585 has an additional leakage current through the PIN connected to the ACMP IN- input when all of the ACMPs are powered down. Typically, leakage through the PIN connected to IN- is much less than 1 µA. But when the ACMP is powered down and voltage is applied to the PIN, the leakage current may grow up to several µA (depending on the VDD and voltage applied).

Workaround:

Currently there is no workaround for this issue.

ISSUE 7: Input Glitch Pattern Combination into DLYs Fails to Trigger Auto Power On of 25 kHz or 2 MHz OSC

Functional Blocks Affected: 25 kHz/2 MHz OSC

Effect:

Specific combinations of DLY inputs can fail to trigger Auto Power On to enable 25 kHz or 2 MHz OSC. Other OSC generators (25 MHz) do not have issue with Auto Power On setting.

Conditions:

Auto Power On can potentially fail to enable OSC when all following conditions are present together:

1. 25 kHz or 2 MHz OSC is in Auto Power On mode.
2. DLYs are clocked by such OSC.
3. Input to one more such DLY have glitches < 200 ns.
4. OR of OSC trigger signals from all DLYs clocked by same OSC together form a long+short glitch pattern with precise (ns) timings as shown in Figure 1. The trigger signal generation per DLY is detailed in section Description.
5. During glitch period, no other DLY is active, meaning has already enabled OSC.

Description:

OSC generators have an Auto Power On mode which can be selected to automatically power on the OSC only when needed, such as when a DLY needs to count OSC cycles to time the delay output, thereby reducing quiescent power. Each individual DLY starts waiting in an inactive state, and when upon receiving an input edge (of polarity set by DLY configuration) then sets its individual trigger signal high. For example, in a rising-edge DLY, a rising edge input sets this trigger high. For a falling-edge, the situation is inverted. In either case (or both edge DLY), the individual DLY trigger is reset if either an opposite edge is detected (therefore, canceling the DLY function) or the DLY finishes timing its output upon reaching the desired count per its setting. Therefore, an input pulse shorter than the DLY time is filtered out. The global Auto Power On circuitry then takes the OR of all the individual DLY triggers and subsequently sends the master enable signal to activate the OSC.

For this chip, the Auto Power On circuitry of the 25 kHz/2 MHz generators contains a circuit errata, which can potentially fail to power on the OSC for a specific pattern and timing of the OR of all related DLY trigger signals. The pattern is shown in Figure 1 (boxed in red) and consists of a relatively longer pulse (~145 ns) followed by a shorter (~5 ns) glitch of opposite polarity.

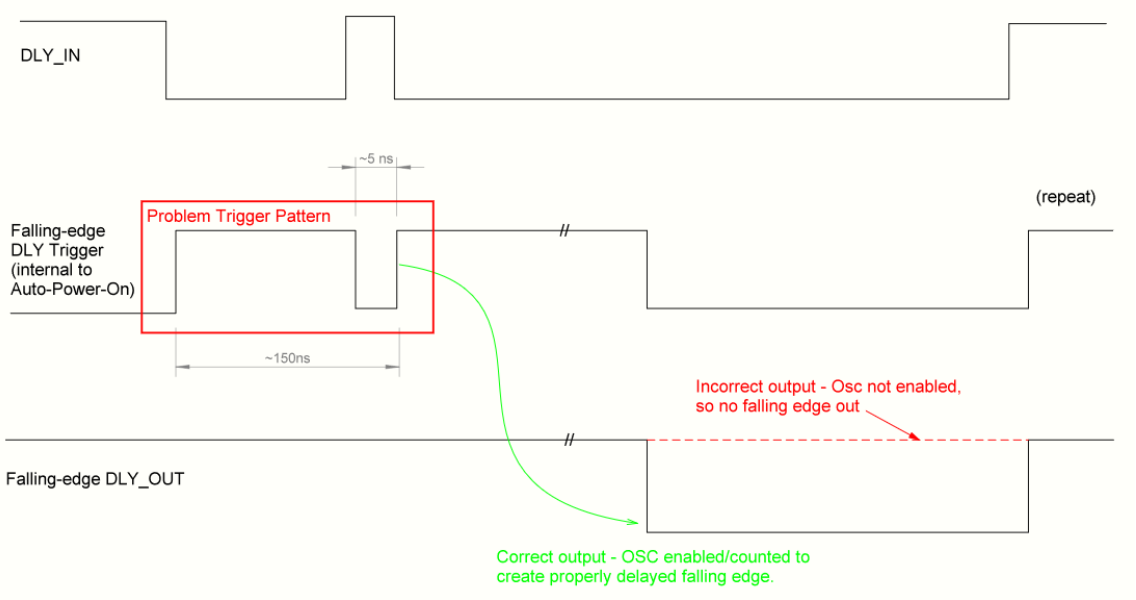


Figure 1: Problem Trigger Pattern

The error is difficult to capture as the timing must be exact within ns, and short (ns) pulses are difficult to generate glitch precise enough to induce the problem. GPIO naturally filter out ns pulses, so for purposes of errata capture, two simultaneous falling-edge DLY circuits (as shown in Figure 2) were used. By lining up two delays precisely at a particular timing relationship, we can use the internal Auto Power On (OR logic) to generate the glitch pattern necessary to cause the error.

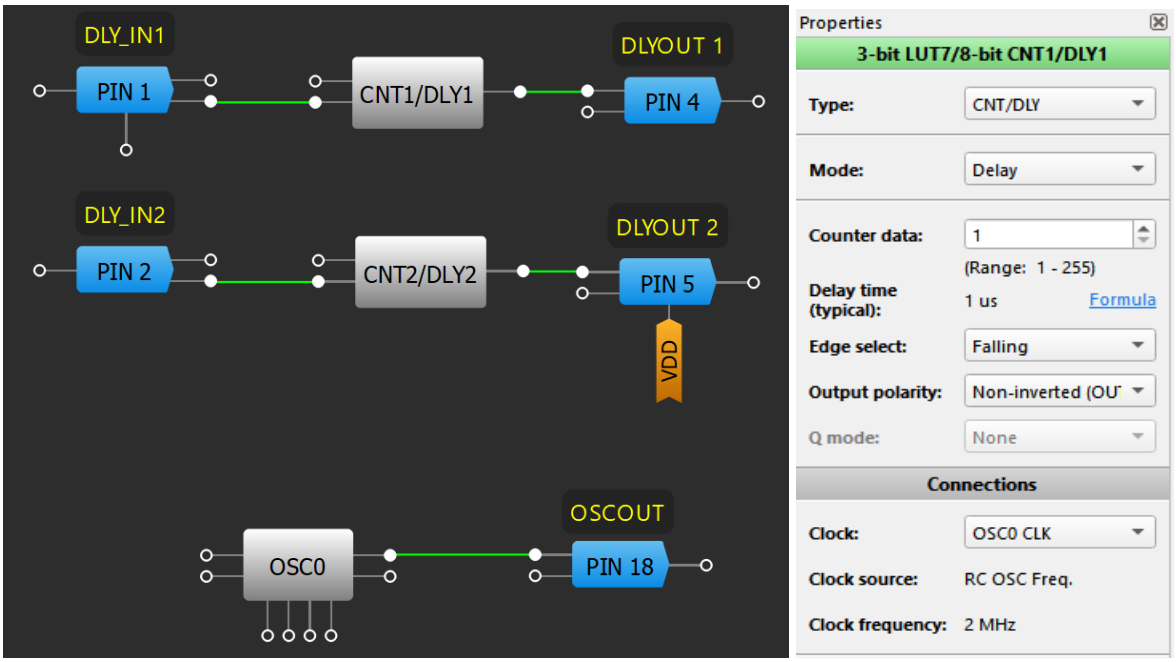


Figure 2: Test Circuit

Figure 3 shows a series of DLY output events are missing, where the OSC is correspondingly not triggering when it was supposed to. Figure 4 is a zoom in of the boxed region from Figure 3. The total glitch/chatter time was measured in this case at 152 ns. By using the composite OR of the two delay channels, we can asynchronously strobe with tiny frequency variations, and so tune the timing to induce this errata. Note that the error is not persistent – the system is recovered when all DLYs are returned to inactive state, such as when input of falling edge DLY goes high, thus canceling delay, or after DLY out finishes.

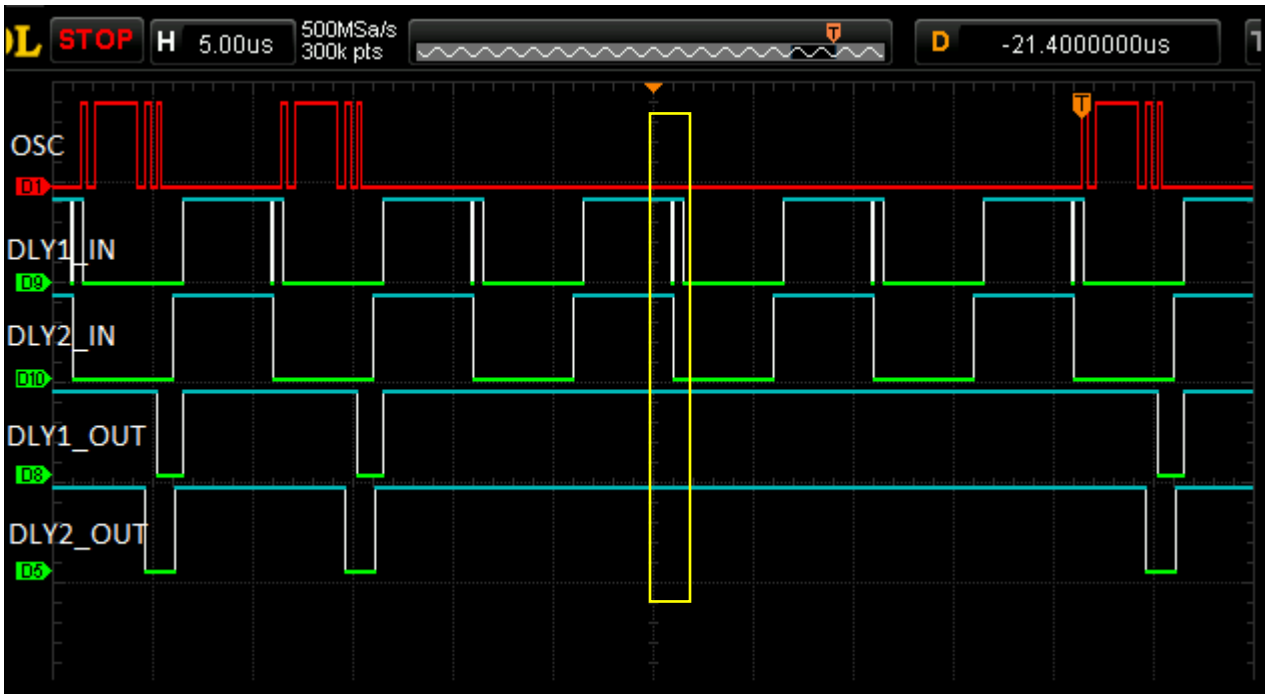


Figure 3: Errata Capture (Zoom Out)

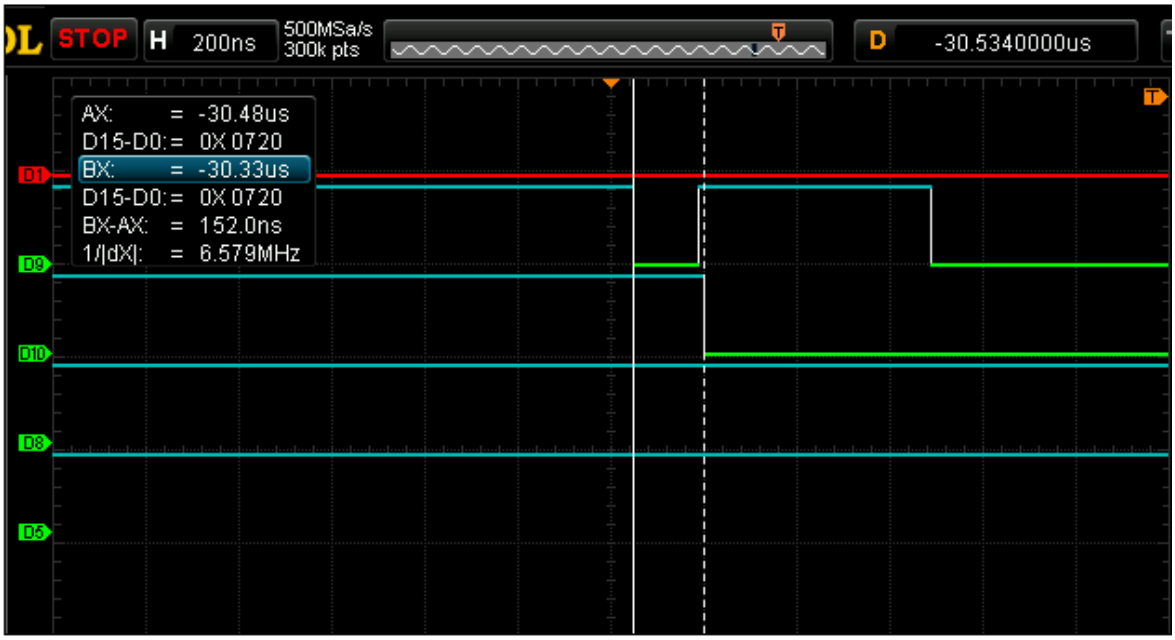


Figure 4: Errata Capture (Zoom In)

Workaround:

Any one of the following prevents the issue:

1. Use signal conditioning circuits to prevent glitch on DLY inputs < 200 ns. Examples:
   a. ACMP with Hysteresis
   b. External RC in front of Digital Input with Schmitt Trigger
   c. Filter cell.
2. Set OSC power mode to Force Power On mode instead of Auto Power On.
3. Use different oscillator, such as 25 MHz Ring OSC, which does not have Auto Power On issue.

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