Errata

SLG46811

CE-GP-008

Abstract

This document contains the known errata for SLG46811 and the recommended workarounds.

1 Information

Package(s)	12-pin STQFN: 1.6 mm x 1.6 mm X 0.55 mm, 0.4mm pitch

2 Errata Summary

Table 1: Errata Summary

Issue #	Issue Title
1	Incorrect 64 mV Hysteresis Operation while Using MS ACMP in Regular ACMP Mode

3 Errata Details

3.1 Incorrect 64 mV Hysteresis Operation while Using MS ACMP in Regular ACMP Mode

3.1.1 Effect

64 mV Hysteresis while Using MS ACMP in Regular ACMP Mode

3.1.2 Conditions

MS ACMP in Regular ACMP Mode with 64 mV hysteresis, V_{DD} = 4.0 V or higher, Vref = 1344 mV or higher.

3.1.3 Technical Description

If using MS ACMP in Regular ACMP mode with 64 mV hysteresis, MS ACMP output could be glitching when MS ACMP positive input (IN+) close to the negative input (IN-). It can happen when V_{DD} = 4.0 V or higher and Vref = 1344 mV or higher.

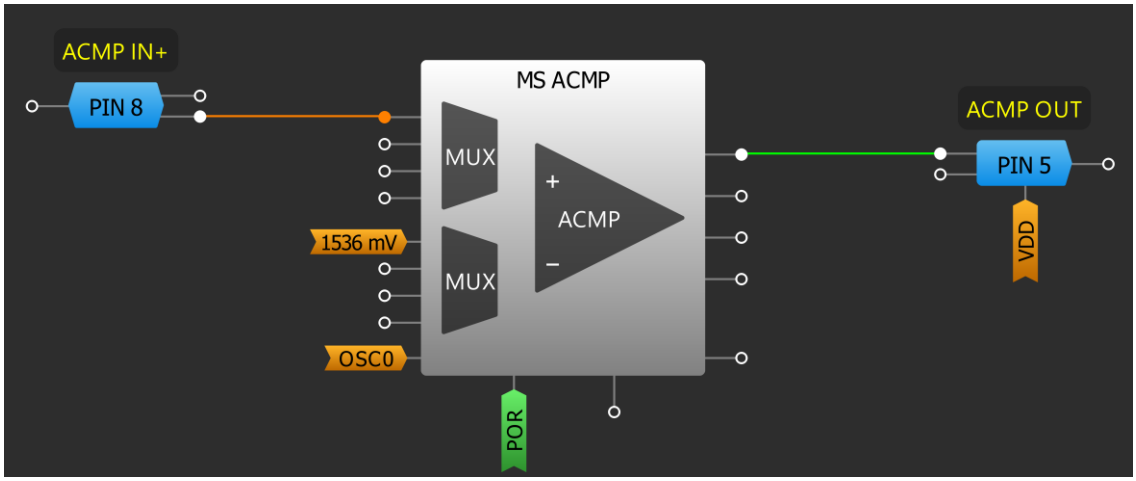

Figure 1: Testing Design

Channel (yellow/top line) - PIN#8 (ACMP IN+)

Channel (light blue/top line) - PIN#5 (ACMP OUT)

1. Waveform at Vref = 1536 mV, hysteresis is equal to 64 mV.

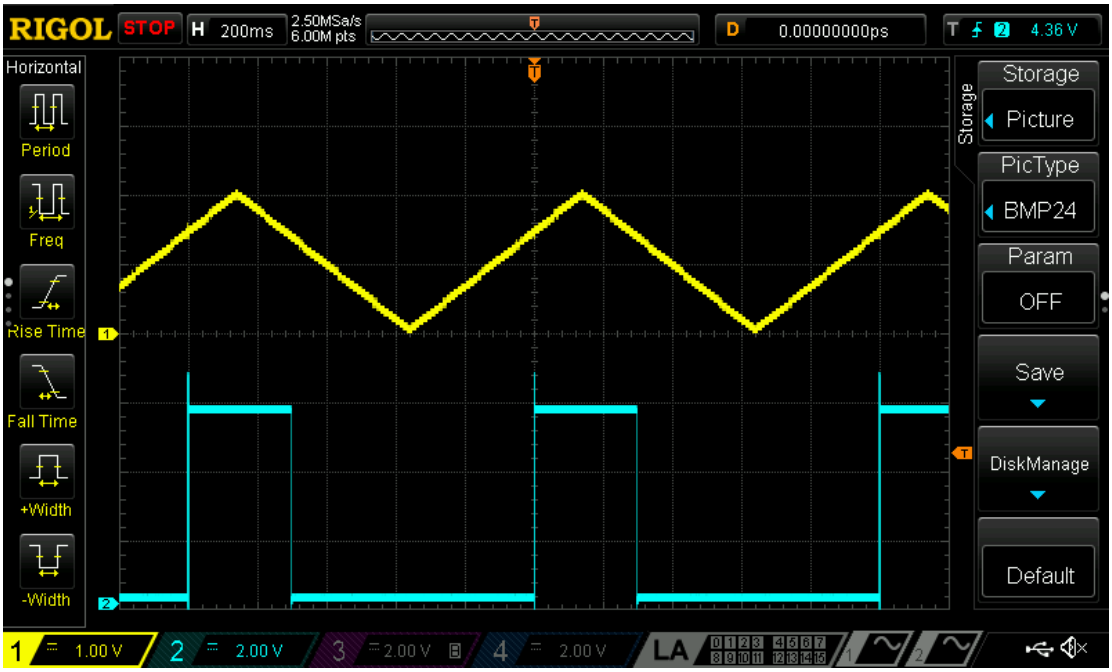

Figure 2: ACMP Output during Glitching

2. Waveform at Vref = 1536 mV, hysteresis is equal to 64 mV (zoomed rising edge).

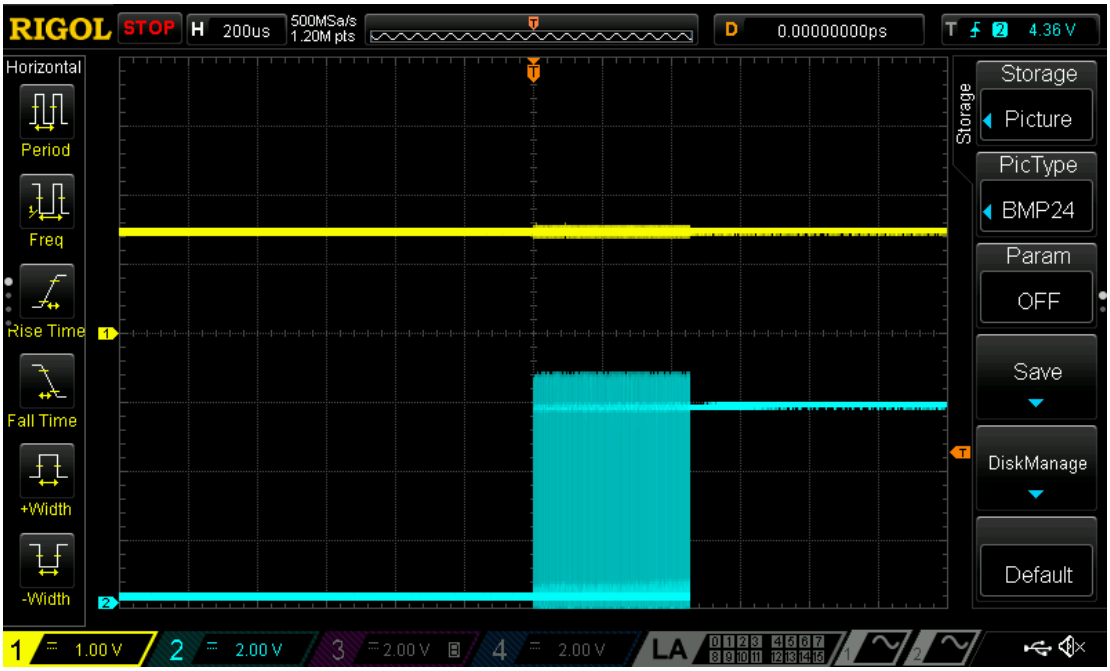

Figure 3: Zoomed ACMP Output during Glitching

3.1.4 Workaround

1. Use the deglitch filter connected to the MS ACMP output.

2. Decrease the reference (below 1344 mV) at IN- and add the IN+ gain to keep the needed threshold.

3. Use MS ACMP in multichannel mode.

Document Revision History

Revision	Date	Description
1.1	09-Mar-2022	Renesas rebranding
1.0	23-Mar-2021	Initial version

Status Definitions

Status	Definition
DRAFT	The content of this document is under review and subject to formal approval, which may result in modifications or additions.
APPROVED or unmarked	The content of this document has been approved for publication.