Errata

SLG46867

CE-GP-013

Abstract

This document contains the known errata for SLG46867 and the recommended workarounds.

1 Information

Package(s)	20-pin MSTQFN: 1.6 mm x 3.0 mm x 0.55 mm, 0.4 mm pitch

2 Errata Summary

Table 1: Errata Summary

Issue #	Issue Title
1	Incorrect I2C Reads of the 8-bit Counter Registers
2	Noise Coupling from Vref0 to Low-Power Bandgap
3	Unstable Vref Output Buffer
4	Incorrect Data Write
5	Extra 300 µA Current Consumption when Using SCL and SDA Pins as GPIO
6	Leakage from ACMP IN+ to Analog Input Pins
7	Incorrect 32 mV and 64 mV Hysteresis Operation with ACMPxH

3 Errata Details

3.1 Incorrect I²C Reads of the 8-bit Counter Registers

3.1.1 Effect

CNT2/DLY2 and CNT4/DLY4

3.1.2 Conditions

I²C latch signal and the clock input occur at about the same time.

3.1.3 Technical Description

Asynchronous interaction between the CNT/DLY clock input and the I²C latch signal (generated by an I²C read command of the CNT/DLY block's count value) can result in an incorrect I²C data read. The CNT/DLY block will count accurately, but the count value transferred into the block's I²C read register might be loaded incompletely if the I²C latch signal and the clock input occur at about the same time.

The example data capture below shows ten periodic I²C reads of CNT2/DLY2 configured to count down at about 16 clocks per read. The sixth read sample erroneously shows a value greater than that of the fifth. The seventh sample reads as if the previous I²C error never occurred - the difference from the fifth sample (176) to the seventh (143) is 33 clocks or 16 clocks + 17 clocks as expected.

Channel 1 (yellow/top line) – PIN#2 (CNT2/DLY2 Out)
Channel 2 (light blue/2nd line) – PIN#1 (I²C Read Triggers)
Channel 3 (magenta /3rd line) – PIN#8 (I²C SCL)
Channel 3 (dark blue /4th line) – PIN#9 (I²C SDA)

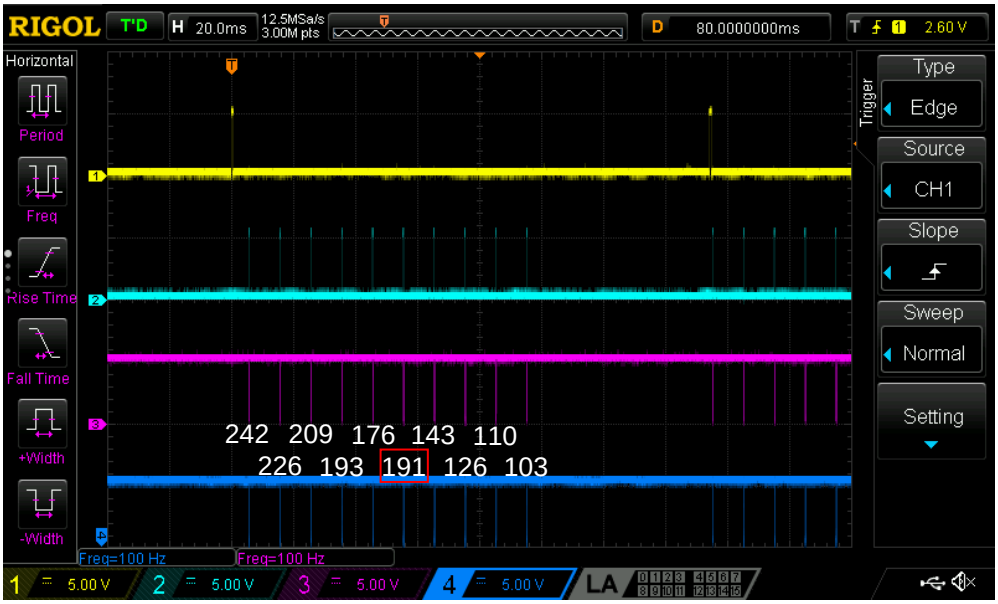

Figure 1: Example Data

3.1.4 Workaround

If the possibility of incorrect I²C data reads can't be accommodated for by external software checks, one can guarantee proper operation by stopping the CNT/DLY block's clock during I²C reads through one of the following methods: by disabling the oscillator block, by reconfiguring the CNT/DLY block's clock source, or by gating an external clock using a LUT (Look Up Table) in the signal matrix. After disabling the CNT/DLY block's clock, the count registers can be read without error. Please note that this workaround will add the I²C read and processing time to the counter's overall clock period.

The best workaround depends on the resource constraints of the application. If the oscillator block doesn't clock other logic elements within the design, a matrix output can be used to manually power down the oscillators for the I²C read. When the CNT/DLY block's clock source is routed internally from the oscillator block, I²C commands can temporarily reconfigure the CNT/DLY block's clock source registers to select "Ext. CLK. (From Matrix)." This action will disable the clock by connecting it to ground. If the CNT/DLY block is clocked from the signal matrix, the LUT can be used to gate the clock during the I²C read.

3.2 Noise Coupling from Vref0 to Low-Power Bandgap

3.2.1 Effect

All ACMPs

3.2.2 Conditions

Manual powering up the high-speed ACMPs via the "PWR UP" connector.

3.2.3 Technical Description

There is some noise coupling from the Vrefs of high-speed ACMPs to the low-power bandgap (BG) while the high-speed ACMPs Vref is turning on and off.

3.2.4 Workaround

There is no issue with manually powering up the low-speed ACMPs. If you are manually powering up the high-speed ACMPs via the "PWR UP" connector, you should add a 1 ms delay to the output of all of the ACMPs used in the design.

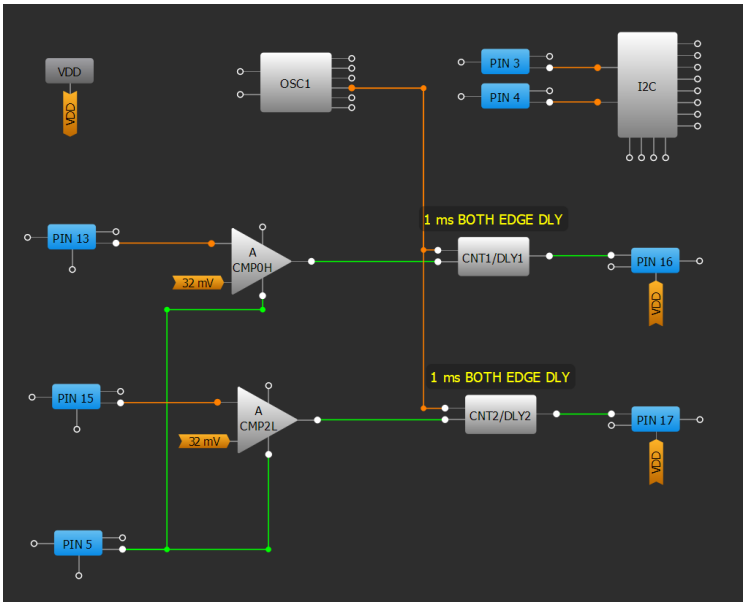

Figure 2: Testing Diagram

3.3 Unstable Vref Output Buffer

3.3.1 Effect

Both Vref Output

3.3.2 Conditions

V_{DD} = 2.5 V, Vref Out = (0.5xV_{DD}) ± 0.4 V.

3.3.3 Technical Description

For systems where V_{DD} = 2.5 V, the Vref output buffer will be unstable if the output voltage is around 0.5xV_{DD}.

3.3.4 Workaround

For a system where V_{DD} = 2.5 V, bypass the buffer if the output voltage of the Vref buffer is within (0.5xV_{DD}) ± 0.4. Check the Vref section of the device datasheet to see which registers need to be modified.

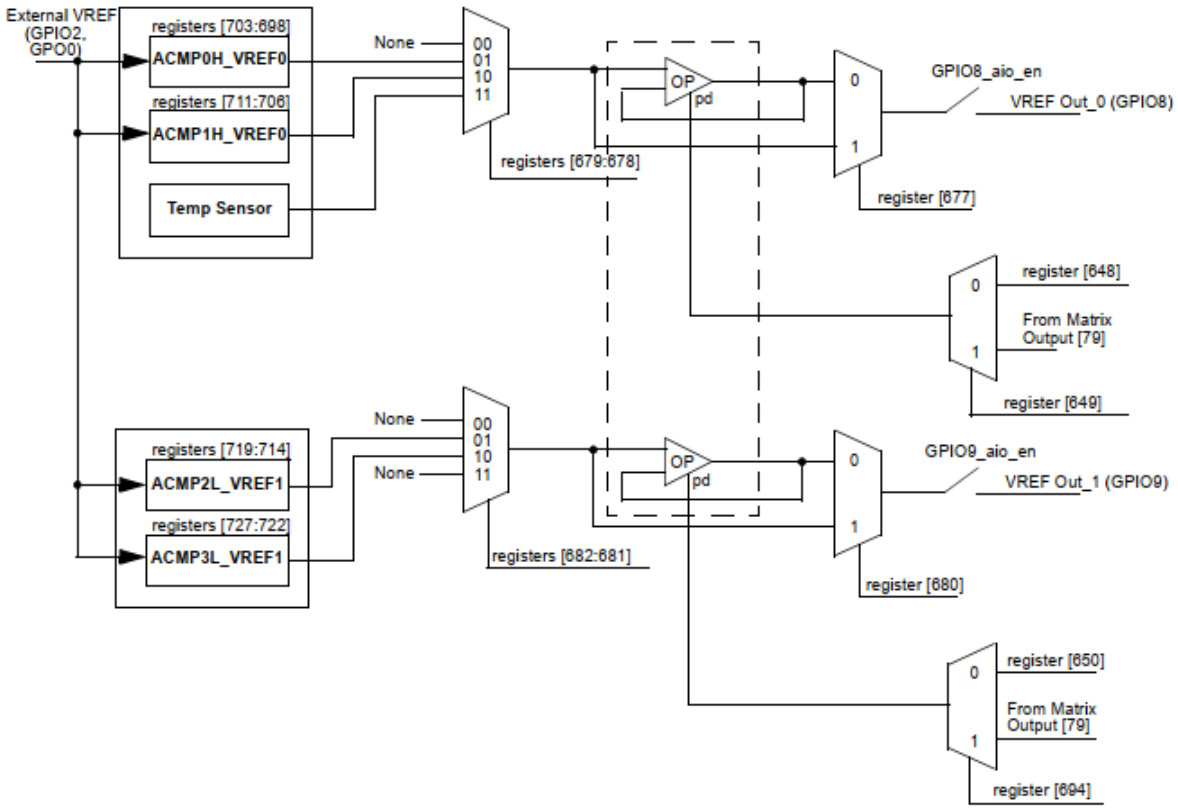

Figure 3: Voltage Reference Block Diagram

3.4 Incorrect Data Write

3.4.1 Effect

I²C

3.4.2 Conditions

Any.

3.4.3 Technical Description

When performing a masked I²C write, unchanged bits in the 8-bit I²C bus may be coupled to the changed bits due to the large coupling capacitor between the I²C bus bits, leading to incorrect data being written.

3.4.4 Workaround

There is no workaround, but this will be fixed in the next silicon revision.

3.5 Extra 300 µA Current Consumption when Using SCL and SDA Pins as GPIO

3.5.1 Effect

GPIO0, GPIO1

3.5.2 Conditions

SCL and SDA pins used as GPIO outputs.

3.5.3 Technical Description

When using the I^2C SCL and SDA pins as GPIO outputs, there is an internal block that causes about 300 µA of current consumption. This does not appear when the I^2C pins are used as either digital input pins or as I^2C pins.

3.5.4 Workaround

There is no workaround. It is not recommended to use these pins as Digital Outputs.

3.6 Leakage from ACMP IN+ to Analog Input Pins

3.6.1 Effect

GPIO4/5/6/7, ACMP0/1H, ACMP2/3L

3.6.2 Conditions

Multiple input sources connected to the ACMP IN+ port simultaneously.

3.6.3 Technical Description

When configured in “Analog IO” mode, GPIO4/5/6/7 can experience abnormal leakage behavior. This behavior occurs when multiple input sources are simultaneously connected to the ACMP IN+ port. Each of the 4 ACMPs has an input MUX which selects the IN+ source for the comparator. The MUX options are shown in the table below.

Table 2: ACMP Input Options

ACMP IN+ MUX Options	
ACMP0H	GPIO4 Buffered GPIO4 V_{DD}
ACMP1H	GPIO5 Buffered GPIO5 ACMP0H IN+ source
ACMP2L	GPIO6 ACMP0H IN+ source ACMP1H IN+ source
ACMP3L	GPIO7 ACMP2L IN+ source Vref0 output

In the GreenPAK Designer, the input source is selected by the IN+ source dropdown within the ACMP’s properties window. When an input source is selected and the ACMP is enabled, an analog

switch connects the source to the ACMP's IN+ port. If multiple sources are connected to the ACMP's IN+ port, there will be leakage between the sources.

The GPIOs shown above can be repurposed as Digital IOs if the ACMPs are disabled or if another input source is selected for the ACMP by the IN+ input MUX. Whenever a GPIO input mode is configured as an "Analog IO" in accordance with the register definition below, the GPIO will be connected to the ACMP's IN+ port through an internal switch. This can create a leakage scenario if the ACMP is enabled and connected to another input source.

Table 3: GPIO Input Mode Configurations

Byte	Register Bit	Signal Function	Register Bit Definition
GPIO4			
0x66	821 822	Input Mode Configuration	00: Digital without Schmitt Trigger 01: Digital with Schmitt Trigger 10: Low Voltage Digital In 11: Analog IO
GPIO5			
0x67	829 830	Input Mode Configuration	00: Digital without Schmitt Trigger 01: Digital with Schmitt Trigger 10: Low Voltage Digital In 11: Analog IO
GPIO6			
0x68	836 837	Input Mode Configuration	00: Digital without Schmitt Trigger 01: Digital with Schmitt Trigger 10: Low Voltage Digital In 11: Analog IO
GPIO7			
0x69	843 844	Input Mode Configuration	00: Digital without Schmitt Trigger 01: Digital with Schmitt Trigger 10: Low Voltage Digital In 11: Analog IO

There are 3 standard GPIO settings that use the "Analog IO" configuration: Analog input/output, Digital input/output (with "Input mode" set to Analog input), and Digital output (with "Output mode" set to 1/2/4x 3-State Output). The first setting is reserved for use with the ACMP, but the other two settings use the "Analog IO" configuration as a high-impedance input. It is important to note that these input modes won't be high impedance if the ACMP is enabled and connected to another input source. When two signals are connected to the ACMP's IN+ source, the voltage level at the ACMP's input depends upon the drive strength of the competing sources.

Figure 4 shows the GreenPAK configured with GPIO4 as a Digital IO with a 1 MΩ pull-down resistor. Since the OE pin is connected to 0 V, this pin is acting as an "Analog IO." As seen in **Error! Reference source not found.**Table 2, GPIO4 and V_{DD} are both input options for ACMP0H. In this example, GPI0 is being used as a digital input to enable and disable the ACMP.

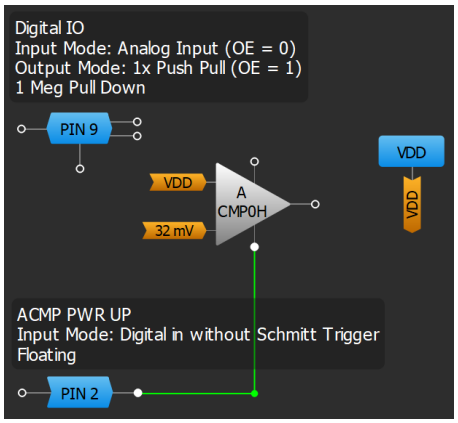

Figure 4: GreenPAK Input Structure Test Schematic

Figure 5 shows that GPIO4 in analog input mode is pulled HIGH by the V_{DD} signal whenever the ACMP is enabled despite having an internal pull-down resistor. This behavior is cause by an internal connection between V_{DD} and GPIO4. Similar behavior can be reproduced when one ACMP's IN+ port is connected to another ACMP's IN+ port.

CH1 (Yellow): ACMP PWR UP (GPI0)
CH3 (Light Blue): Digital IO w/ Analog Input Mode Configuration (GPIO4)

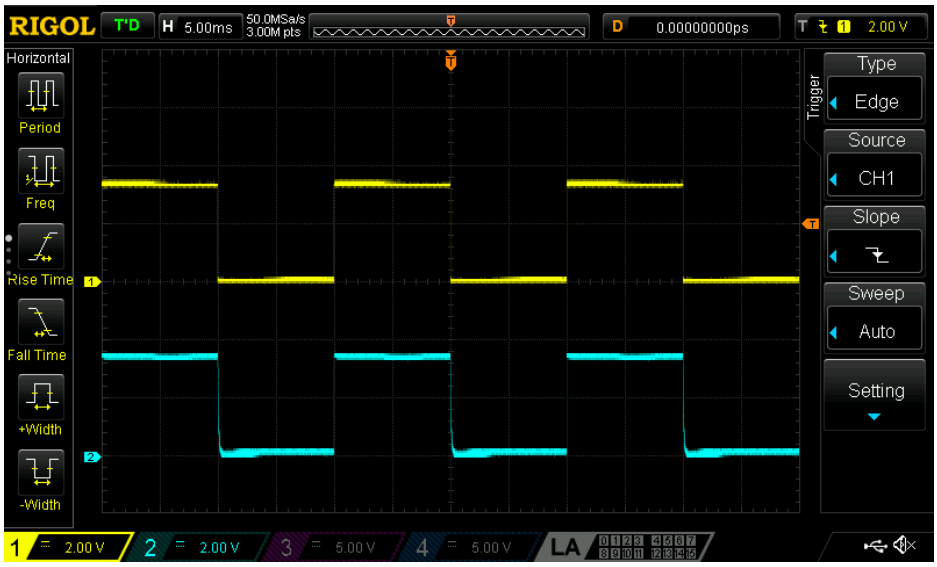

Figure 5: ACMP Input Structure Behavior

3.6.4 Workaround

If an ACMP is disabled, the GPIO associated with that ACMP will operate as expected under any configuration. Please reference Table 2 for more information regarding which GPIOs are associated with which ACMPs.

When the ACMPs are enabled, it is possible to inadvertently connect multiple ACMP sources together through the input structure. This is possible when the ACMP input is connected to a source other than its analog GPIO and that GPIO's input mode is set to "Analog IO".

There is no workaround for this behavior. With this in mind, the GPIOs should not be used as digital IOs (with "Input mode" set to Analog input) or as digital outputs (with "Output mode" set to 1/2/4x 3-State Output) if the respective ACMP is enabled and connected to another input source.

3.7 Incorrect 32 mV and 64 mV Hysteresis Operation with ACMPxH

3.7.1 Effect

ACMP0H and ACMP1H

3.7.2 Conditions

V_{DD} ≥ 4.6 V, with hysteresis 32 mV at Vref range 1.312 V to 2.016 V.
V_{DD} ≥ 4.6 V, with hysteresis 64 mV at Vref range 1.312 V to 1.696 V.

3.7.3 Technical Description

If using ACMPxH in with 32 mV or 64 mV hysteresis, ACMPxH output could be glitching when ACMPxH positive input (IN+) is close to the negative input (IN-). It can happen when V_{DD} = 4.6 V or higher and Vref is in a range from 1.312 V to 2.016 V for 32 mV hysteresis, and Vref is in a range from 1.312 V to 1.696 V for 64 mV hysteresis.

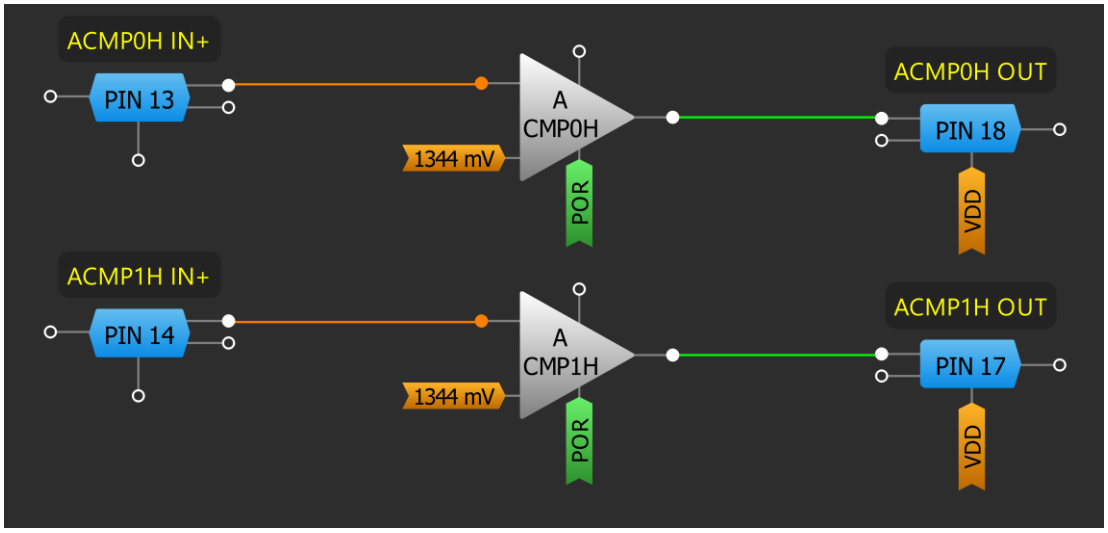

Figure 6: Testing Design

Channel (yellow/top line) - PIN#13 (ACMP0H IN+)

Channel (light blue/top line) - PIN#18 (ACMP0H OUT)

1. Waveform at Vref = 1344 mV, hysteresis is equal to 32 mV.

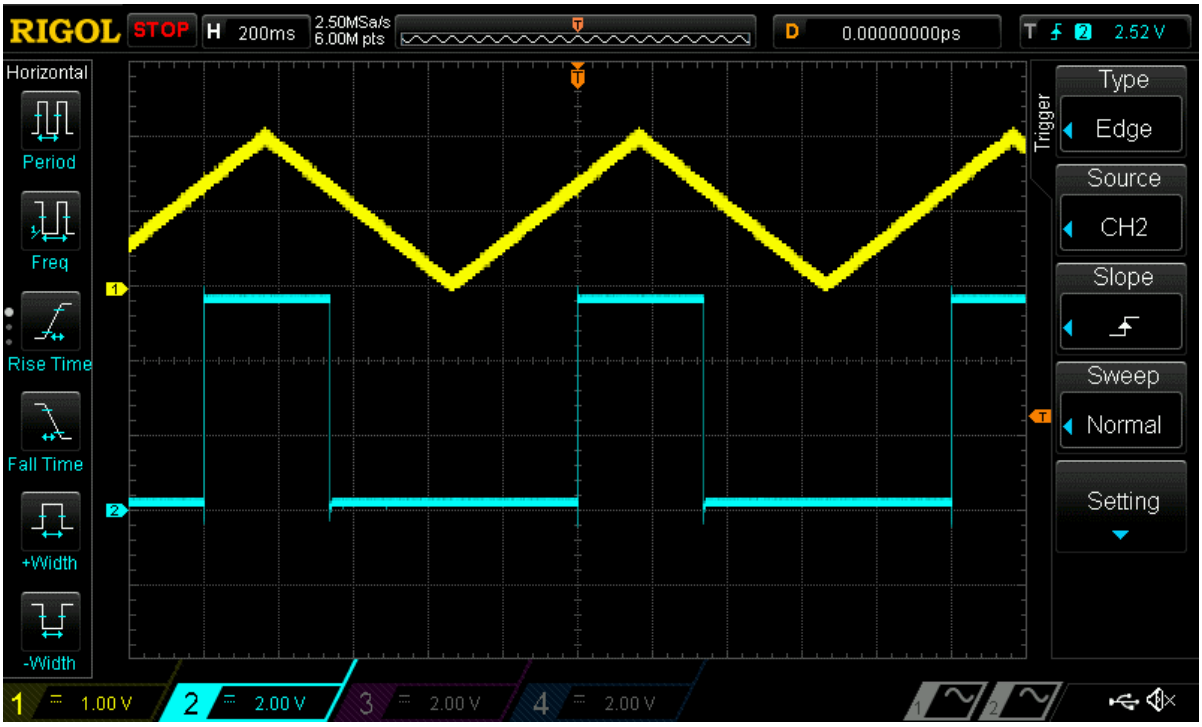

Figure 7: ACMP Output during Glitching

2. Waveform at Vref = 1344 mV, hysteresis is equal to 32 mV (zoomed rising edge).

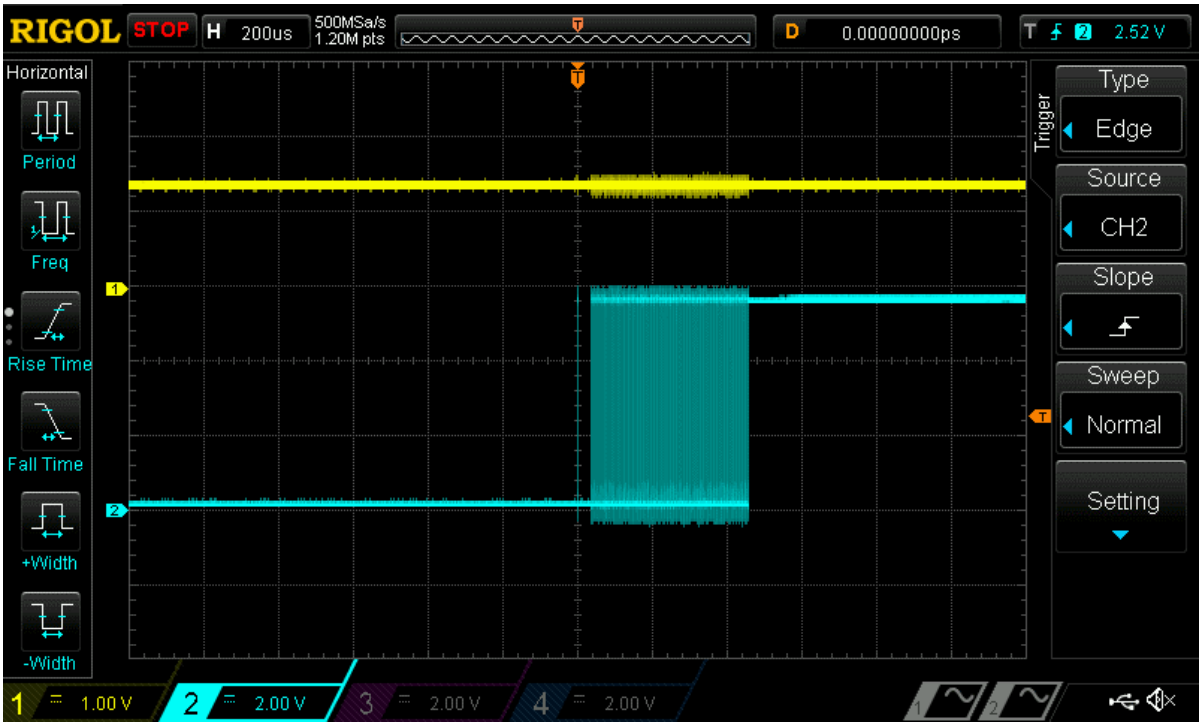

Figure 8: Zoomed ACMP Output during Glitching

3.7.4 Workaround

1. Use the deglitch filter connected to the ACMPxH output.

2. Avoid conditions described in paragraph 3.7.2.

Document Revision History

Revision	Date	Description
1.2	8-Mar-2022	Renesas rebranding
1.1	31-Mar-2021	Updated issue Incorrect 32 mV and 64 mV Hysteresis Operation with ACMPxH
1.0	25-Mar-2021	Added new issue - Incorrect 32 mV and 64 mV Hysteresis Operation with ACMP Updated according to new Dialog's format

SLG46867 Errata

Status Definitions

Status	Definition
DRAFT	The content of this document is under review and subject to formal approval, which may result in modifications or additions.
APPROVED or unmarked	The content of this document has been approved for publication.