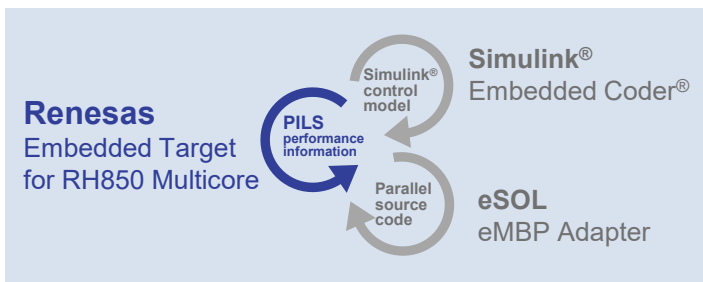


Simplifies complex driving control for the autonomous-driving era

RH850 Multicore Model-Based Environment

<https://www.renesas.com/mbd-rh850-multicore>

The model generates complex multi-core code automatically, which reduces the time required for design and allows for quick confirmation of performance.



Embedded Target for RH850 Multicore is a MATLAB® collaborative environment that automatically generates parallel codes and a Processor In the Loop Simulation (PILS) environment from a Simulink® model. This development environment also supports automatic multicore allocation in corporation with the model based parallelizer of eSOL Co., Ltd.

In an engine/vehicle body control system, Embedded Target for RH850 for single core is provided in addition to Embedded Target for RH850 Multicore + Multirate for the development of systems that have general multiple control cycles (multirate).

Five capabilities to accelerate model-based development

- ① Generates a scheduler of the type recommended by JMAAB./ Automatically generates code for multi-core processors. ● ● ●
 - ② Enables core-based execution in units of subsystems of a Simulink® model. ● ● ●
 - ③ Automatically searches core allocation best suited for control systems through collaboration with eMBP to enable parallelization. ● ● ●
 - ④ Automatically generates parallel codes and a PILS environment and visualizes multicore performance in the modeling process. ● ● ●
 - ⑤ Provides a cycle accuracy simulator that can measure time with an accuracy close to that of the actual machine. ● ● ●
- This enables evaluation of the operation of systems with multiple control periods, such as systems for controlling engines and bodies, and Electronic Control Units (ECUs) in which multiple systems for controlling various items in the vehicle as a whole are integrated.
 - The allowable margins for processing, for which the worst execution timespans during simulation are going to be the control periods, can be checked
 - This makes it possible to compare and examine which software structures make effective use of the capacity of the multiple cores directly on MATLAB® and Simulink models
 - Returning to earlier stages in design due to incorrect estimation of parallel performance before implementing software can be avoided, and the development times for multicore control software can be shortened
 - Enabling evaluation ahead of time in an environment without actual machine and emulator

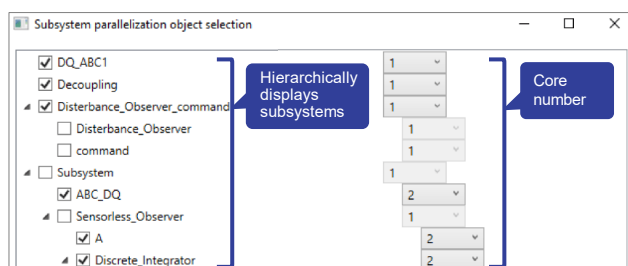
Function details

1. Generating sequential codes - Measuring execution time

The single-core PILS can measure the execution time of each subsystem of a Simulink® model by using the software trace function of the CS+ debugger.

3. Generate parallel codes

Synchronous processing is automatically allocated among the cores in accord with the core allocation plan from the model-based parallelization tool or an allocation plan specified by the user, and parallel source code for the RH850 is generated by the Embedded Coder® from The MathWorks, Inc.



2. Analyzing model structure and searching core allocation - Transform model automatically

Through interlinked operation with the optional product "eMBP Adaptor for Renesas PILS" of the eMBP Model Based Parallelizer of eSOL Co., Ltd., optimum core allocation is automatically searched and parallelization starts, based on the execution time obtained in step 1.

4. Displaying execution status

The CS+ debugger function acquires the execution time of each subsystem for which a core has been allocated, and then displays the execution status in graphs by core or rate (for the latter, when multirate is used).



Cycle-Accurate Simulator for RH850

The RH850 cycle precision simulator linked with an RH850 multi-core model-based development environment (Embedded Target for RH850 Multicore) can be used for verification of operation.

It can also be used to pre-evaluate the performance of the RH850 without actual equipment or an emulator.

www.renesas.com/rh850-cycle-accurate-sim

- ✓ Simulates CPU operation in consideration of access latency.
- ✓ Possible to simulate the executable files of the Renesas compiler CC-RH and Green Hills Software LLC (GHS) compiler.

Functions of the RH850 cycle precision simulator*

- The basic functions of some peripherals can also be simulated.
 - Dummy interrupts can be generated by using Python functions.
- * when used standalone

Comparison of functions by product

Select the license type applicable to the specifications of the microcontroller or model you use.

License Type/ Product name	Function					
	PIL Simulation on Single-Core Products (Supports multi-rate control)	PIL Simulation on Multicore Products		Load Module Generation by GHS Compiler	Performance Analysis in Blocks	Interlinking with eMBP
		One Core Used	Multiple Cores Used			
Embedded Target for RH850 Multicore + Multirate - RH850 multicore multirate version	✓	✓ ^{*1}	✓ ^{*1}	✓	✓	✓ ^{*2}
Embedded Target for RH850 Multicore - RH850 multicore version	✓	✓	✓	✓	✓	✓
Embedded Target for RH850 - RH850 single-core version	✓	-	-	✓	✓	-

*1 Supports multi-rate control

*2 Support for multi-rate control is in planning.

Supported MCUs

Supported MCUs	Cycle-Accurate Simulator
RH850/C1x RH850/C1H RH850/C1M-A1, RH850/C1M-A2	On sale
RH850/E1x RH850/E1M-S2*	Contact us.
RH850/E2x RH850/E2M, RH850/E2UH RH850/E2H	On sale
RH850/F1x RH850/F1L, RH850/F1H RH850/F1K RH850/F1KM, RH850/F1KH	Contact us. On sale
RH850/P1x RH850/P1H-C RH850/P1M, RH850/P1M-C RH850/P1M-E	On sale
RH850/U2x RH850/U2B	On sale

* Only the main CPU is used.

Video

www.renesas.com/mbd-rh850-multicore_videos

Applicable tools

MATLAB® R2016a - R2019b by MathWorks (64-bit edition only)
CS+ V8.05.00, V8.06.00

Operating environment

Windows® 10 (64-bit version)

Availability

For details on how to purchase the product and other information, contact the dealership or Renesas sales representative.

www.renesas.com/buy-sample/locations

FAQ

en-support.renesas.com/knowledgeBase



Community

community.renesas.com

renesas.com

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Contact information

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