

Interface IP

PCI Express 5.0 Controller

Overview

This IP is a Renesas-developed Controller IP for PCI Express® (PCIe®) 5.0. This IP is from AMBA® AXI interface to PIPE 5 interface. It has a Data Link Layer. It also has a Transaction Layer each for the Root Complex and Endpoint, and Type 0/1 Configuration Registers. It also has a DMA controller function. This IP is written in Verilog-RTL.

Key Features

- AMBA® AXI interface
 - Conforming to AMBA® AXI Protocol v1.0 Specification ARM IHI 0022B
 - Interface: Master/Slave
 - Endian: Little
 - Bus Width: 64 or 128 bits
 - DMAC functions are provided
- PCIe specification
 - Conforming to PCI Express Base Specification 5.0
 - Supports PCIe 1(2.5[GT/s]), 2(5.0[GT/s]), 3(8.0[GT/s]), 4(16.0[GT/s]) and 5[32GT/s]
 - Root Complex / Endpoint Applications, Type0/1 Configuration Register
 - Multiple lane implementations x1 / x2 / x4
 - Lane reversal and Polarity inversion
 - Maximum data payload size is 4096 bytes, Maximum read request size is 4096 bytes
 - Number of outstanding requests 1-8
- PIPE interface
 - Supports PIPE 5.2
 - Fixed Data-Path: 32bit
 - 1GHz(PCIe 5)/
 - 500MHz(PCIe 4)/
 - 250MHz(PCIe 3)/
 - 125MHz(PCIe 2)/
 - 62.5MHz(PCIe 1)
 - Message Bus I/F support
 - LPC interface support

