Interface IP

SATA PHY for TSMC 28nm HPC+

Overview

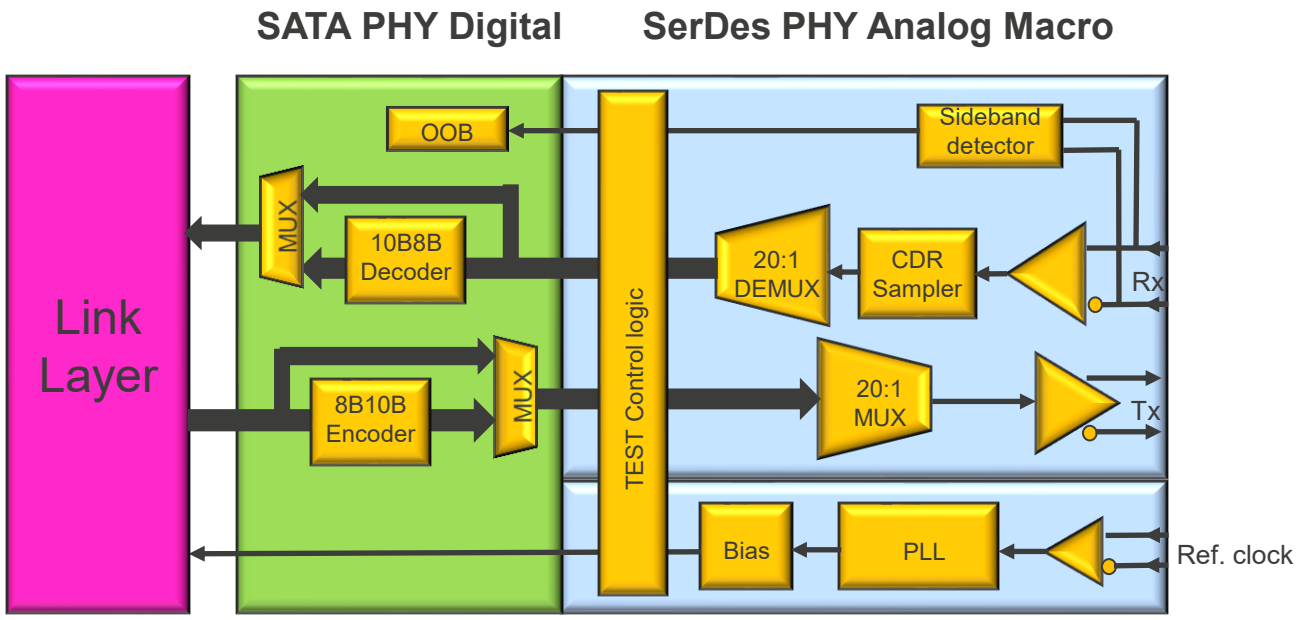
The Renesas SerDes PHY is useful analog transceiver hard macro for various high speed serial interface PHY layer of TSMC 28nm HPC+ process. This macro is designed for Serial ATA Revision 3.1.

Key Features

- Renesas SerDes PHY can be used for analog transceiver of following interface .
  - Serial ATA Revision 3.1 (compliant with “Serial ATA Revision 3.1”) *1
- Technology is TSMC 28nm HPC+ 1p10M.
- Supply voltage can be applied 0.90V for nominal and 1.0V for overdrive of core voltage, 1.8V for IO voltage.
- 2Tap FIR filter for Tx equalizer / Tunable peaking amplifier for Rx equalizer.
- Built-in differential input buffer for clean reference clock.

*1 There are some restrictions for use case of these standards. Please contact and consult to Renesas Electronics for detail information before purchasing product.

Block Diagram



This IP is contract design IP. Please contact for detail.

CTPD-24-114
R06PF0095EJ0100