8V19N850 Hardware Design

This document contains general board-level hardware design information for the 8V19N850. It provides recommendations for power rail handling, loop filter calculation, and input/output termination.

Contents

The simplified block diagram of 8V19N850 is shown in Figure 1. For a more detailed block diagram and in-depth descriptions about the device, see the *8V19N850 Datasheet*.

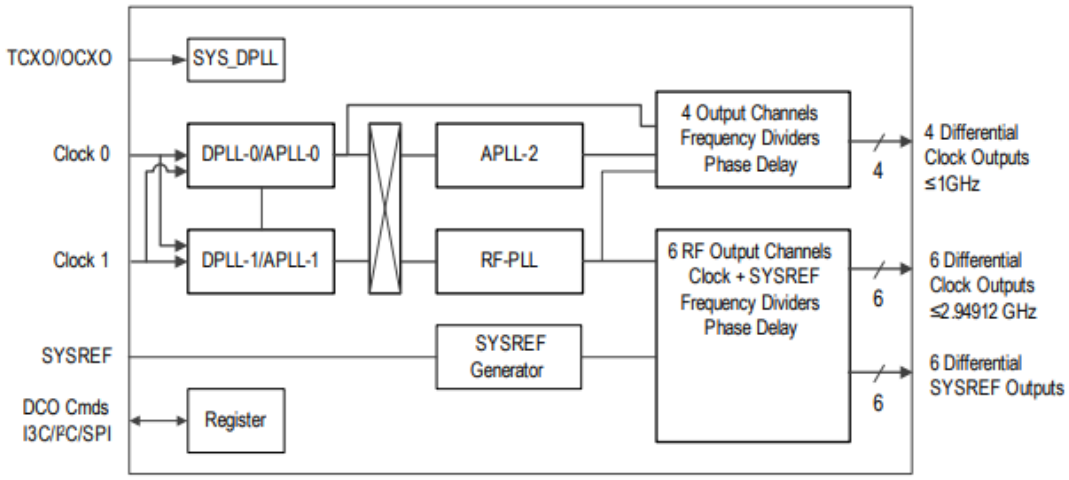

Figure 1. Simplified Block Diagram

A general reference schematic example is shown in Figure 2. A larger version can also be provided in a separate document. In this schematic, the input and output interfaces are shown for illustration purposes. For more examples, see the Input/Output Interface section. The input topology depends on the driver type, and the output driver termination depends on the receiver specification and structure.

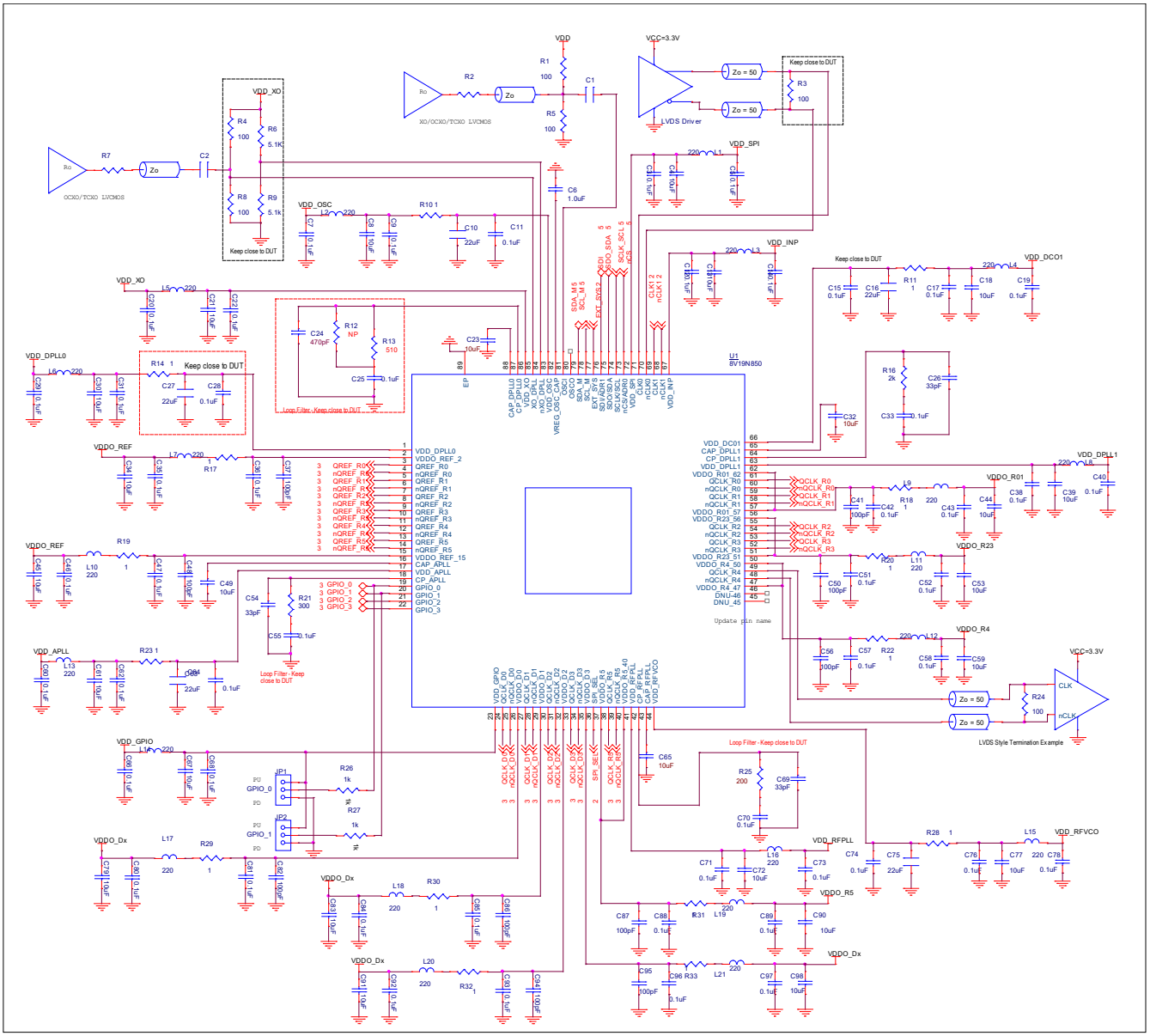

Figure 2. 8V19N850 Reference Schematic Example

1. Power Rails

1.1 Bypass Capacitors

To avoid signal interference, bypass capacitors are required to filter noise from switching power supplies and other devices in the system. Figure 2 shows examples of bypass capacitors on the schematic. The type of bypass capacitor will depend on the noise level and noise frequencies on the application board. The device output driver switching can also cause power rail noise and interference with noise signals from other devices on the board, resulting in unwanted spurious tones in output signals. The bypass capacitors minimize these noise sources.

The bypass capacitor values are usually in the range from 0.01µF to 0.1µF. Other values can also be used. Typical capacitor sizes are 0603, 0402, or 0201 with a low Equivalent Series Resistance (ESR). The dielectric types are typically X5R or X7R. A smaller size allows the capacitor to be placed closer to the power pin of the device with a reduced trace length.

To minimize ESR between power pins and the bypass capacitors, it is recommended to place at least one bypass capacitor at each VDD power pin, with a placement as near as possible to the respective power pin of the device. A thick trace width between the bypass capacitor and power pin helps to reduce ESR. It is recommended to combine multiple capacitors at different resonance frequencies to achieve band pass filter characteristics at the critical noise frequencies.

1.2 Power Supply Isolation

The power rails should be as noise-free as possible to support the low phase noise performance of the device PLLs. The 8V19N850 also integrates LDOs for additional noise filtering. An external ultra-low noise LDO may not be required but it is recommended for further reducing power supply noise. An LDO should have a noise level of less than 6.5µVrms from 10Hz to100kHz. The Renesas RAA214020 is a suitable LDO.

It is recommended to isolate the analog power rail from other high noise power rails, VDDO_x and VDD_INPUT. The isolation can be implemented through an RC low pass filter. The larger RC component values can further reduce the cutoff frequency and clean up lower frequency noise. For the output supplies VDDO_x, to reduce output frequency interference, the power rails between the output banks that operate at different output frequencies can be isolated using separate LDOs or using 1 to 2 ohm resistors if they share the same power source. Additional smaller value capacitors (for example, 100pF) in parallel with the existing 0.1µF near the power pins can provide additional higher frequency noise filtering.

1.3 Loop Filter

1.4 2nd Order Loop Filter

The 8V19N850 contains four Analog PLLs: APLL0, APLL1, APLL2, and RFPLL. These analog PLLs require board-level 2nd order loop filter. The approximate VCO frequency and VCO gains for each APLL is displayed in Table 1. The VCO gain Kvco depend on the operating region.

Table 1. 2nd Order Loop Filter

APLL	Approximate VCO Frequency (GHz)	Kvco (MHz/V)
APLL0	2.5	30
APLL1	3.93216	48
APLL2	3.75	52
RFPLL	2.94912	38

The following section provides a general design of a 2nd order loop filter for PLL. A typical 2nd order loop filter is shown in Figure 3. The design shows a step-by-step calculation to determine Rs, Cs, and Cp values. The required parameters for this part are also provided. A spreadsheet or software tool for calculating the loop filter values are also available.

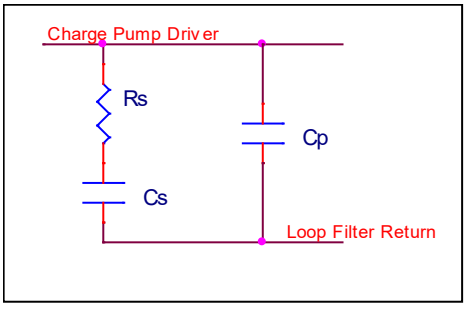

Figure 3. Typical 2nd Order Loop Filter

1. Determine desired loop bandwidth fc. The fc must satisfy the following condition:

$$\frac{Fpd}{fc} >> 20$$

where, Fpd is phase detector input frequency.

2. Calculate Rs

$$Rs = \frac{2 * \pi * \mathrm{fc} * \mathrm{N}}{\mathrm{Icp} * \mathrm{Kvco}}$$

where,

Icp is charge pump current.

Kvco is VCO gain.

N is effective feedback divider.

$$N = \frac{Fvco}{Fpd}$$

Fvco is vco frequency.

Fpd is the phase detector input frequency.

3. Calculate Cs

$$Cs = \frac{\alpha}{2 * \pi * fc * Rc}$$

where,

α is ratio between loop bandwidth and the zero frequency at zero, α = fc / fz, recommend α greater than 3.

fz is frequency at zero.

4. Calculate Cp

$$Cp = \frac{\mathrm{Cs}}{\alpha * \beta}$$

where,

β is ratio between frequency at pole and loop bandwidth, β = fp / fc, recommend β greater than 3.

fp is frequency at pole.

5. Verify maximum Phase Margin, PM

$$PM = \arctan\left(\frac{b-1}{2*\sqrt{b}}\right)$$

where,

$$\mathrm{b} = 1 + \frac{Cs}{Cp}$$

PM should be greater than 50 degrees.

1.5 Loop Filter Calculation Examples

This section provides calculation examples for APLL0 loop filter value for loop bandwidth of ~150kHz. In this example, the reference OCXO input frequency = 48MHz after multiplied by 2, the phase detector input frequency Fpd = 96MHz. This satisfies the condition of Fpd/Fc >> 20.

The APLL0 VCO frequency, Fvco = 2500MHz, the effective feedback divider.

N = Mv = Fvcxo / Fpd ~ 26

Rs can be calculated from the equation,

$$Rs = \frac{2 * \pi * \mathrm{fc} * \mathrm{N}}{\mathrm{Icp} * \mathrm{Kvco}}$$

The APLL0 VCO gain, Kvco ~30MHz/V.

The charge pump current is set as 1.7mA in this example.

Rs = 510 Ohm

Cs can be calculated from the following equation,

$$Cs = \frac{\alpha}{2 * \pi * fc * Rc}$$

For α = 10, Cs is calculated to be ~20 nF. Cs greater than this value can be used to assure that the α is greater than 10. For example, the actual chosen value can be 100 nF from a standard capacitor value to allow room for charge pump current adjustment.

Cp can be calculated from the equation,

$$Cp = \frac{\mathrm{Cs}}{\alpha * \beta}$$

For β = 3, Cp is calculated to be ~650pF. Less than this value can be used for Cp to assure that the β is greater than 3 (for example., the actual selected value Cp can be 470 nF).

Phase margin = 67 degrees

The following table shows Loop Filter Value Examples for APLL0, APLL1, APLL2, and RFPLL. The loop filter values will vary based on the application requirement. Other loop values can also be used as long as the PLLs operate at the stable region.

Table 2. 8V19N850 Analog PLLs Loop Filter Values Examples

	APLL0	APLL1	APLL2	RFPLL
Loop Bandwidth (Hz)	150k	600k	80k	80k
PDF	96MHz	96Mhz	78.125MHz	245.76MHz
Feedback Divider, N	26	40	48	24
Charge Pump Current Setting Can be set between 0.7mA to 2.2mA	1.7mA	1.7mA	1.7mA	1.7mA
Rs (Ohm)	510	2k	300	200
Cs	100nF	100nF	100nF	100nF
Cp	470pF	~33pF	~33pF	~33pF

2. Input/Output Interface

2.1 Input Termination for Reference Clock Input

The 8V19N850 reference clock input CLK/nCLK is a high impedance differential receiver. The inverting input nCLK has weak bias to ~1.65V. The input can accept a signal from a standard 3.3V LVPECL or an LVDS driver directly in DC coupling. The board-level termination at the CLK/nCLK input is determined by the driver type. Figure 4 and Figure 5 provide examples of input interface without AC coupling. Figure 6 and Figure 7 provide examples of input driven by a differential driver with AC coupling. This section provides only few examples. Other termination topologies can also be used. For single-ended driving the differential input, please refer to the example in the OX_DPLL Input (OCXO/TCXO) input section.

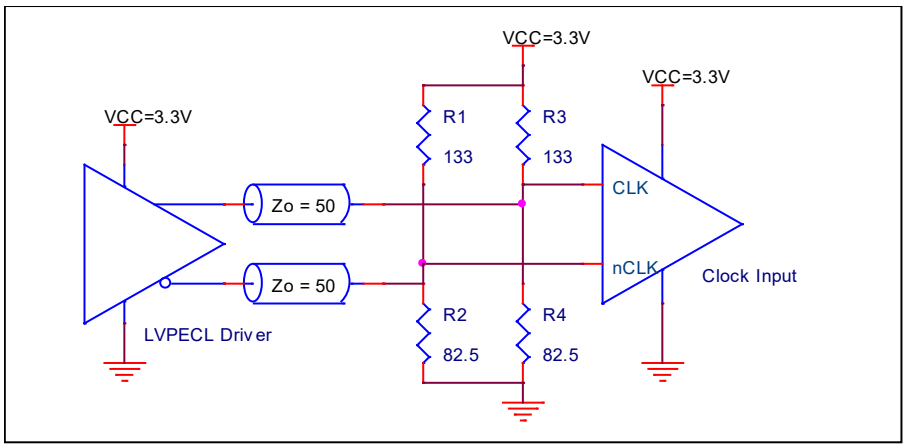

Figure 4. Input Termination Example – 8V19N850 Reference Clock Input CLK/nCLK, Driven by a 3.3V LVPECL Driver

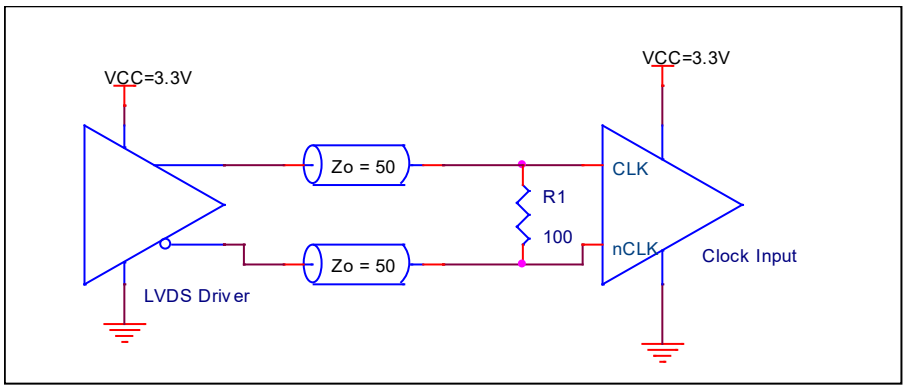

Figure 5. Input Termination Example – 8V19N850 Reference Clock Input CLK/nCLK Driven by a 3.3V LVDS Driver

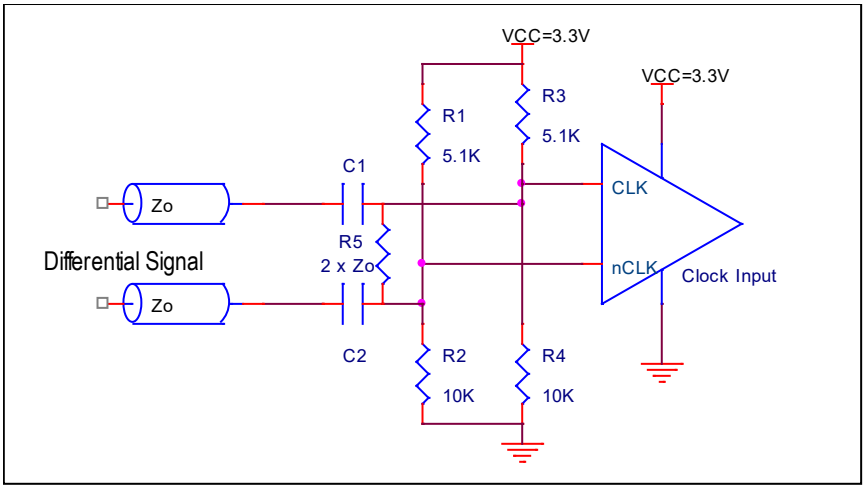

Figure 6. 8V19N850 Reference Clock Input CLK/nCLK AC Coupling Termination – Example 1

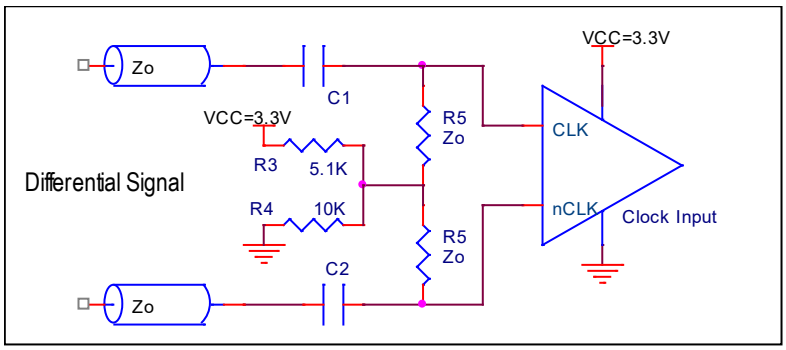

Figure 7. 8V19N850 Reference Clock Input CLK/nCLK AC Coupling Termination – Example 2

2.2 OX_DPLL Input (OCXO/TCXO)

The XO_DPLL input receives a stable frequency source from OCXO/TCXO mainly for SysAPLL and SysDPLL. This input can also be used for APLL0, APLL1, and APLL2 phase frequency detector input. The limitation of frequency range is provided in the 8V19N850 datasheet. When the XO_DPLL input is only used for SysAPLL or SysDPLL, a stable frequency TCXO/OCXO is required. Low frequency (for example, 10MHz to 20MHz) is fine. Phase noise performance is not critical. When the TCXO/OCXO is used for both SysAPLL/SysDPLL and APLL0, APLL1, both stable frequency and good phase noise performance are required. Higher frequency (for example, ~ 38MHz to 54MHz) is recommended for better phase noise performance.

XO_DPLL/nXO_DPLL is a differential high-impedance input with built-in weak pull-up and pull-down resistors. The input termination is dictated by the signal source driver type. If the driver is a differential driver, see the examples provided in “Input Termination for Reference Clock Input”. Since most OCXO/TCXO drivers are single-ended drivers, Figure 8 provides an example of single-ended to XO_DPLL input layout. Not all components in the footprint are required to be populated because of the varying strength of the driver and trace length in the layout.

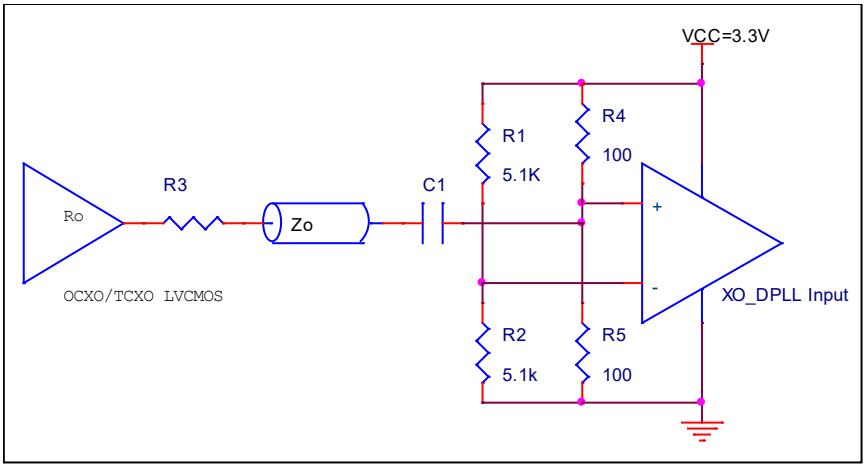

Figure 8. General Layout Example for Single-ended LVCMOS to XO_DPLL

2.3 OSCI/OSCO Input (XTAL, XO, OCXO/TCXO)

The OSCI input receives a signal from a crystal. It can be overdriven by oscillation sources like XO, OCXO, and TCXO. The limitation of the frequency range is provided in the datasheet. The OSCI input mainly provides a signal source for APLL0, APLL1, and APLL2. The OCSI source can also be used to SysAPLL. The OCSI source cannot be used for SysDPLL. The OCSI signal source phase noise needs to have good performance so that it provides a good close-end phase noise performance at the 8V19N850 output. The OCSI signal source can be XO, OCXO, or TCXO.

When an XO to OSCI is used in conjunction with an OCXO at the XO_DPLL input, the XO is used for APLL0, APLL1, or APLL2. This OCSI input must be a good phase noise performance and higher frequency (~38MHz to 54MHz). The OCXO to the XO_DPLL to the SysDPLL/SysDPLL must be frequency stable but it does not need to have as good phase noise performance as the XO to the OSCI. The OCXO can be lower frequency (for example, 10MHz to 20MHz).

The OCSI/OSCO input contains an oscillation circuit and can interface with a crystal. Figure 9 provides an example of a parallel resonant crystal to OCSI/OSCO input interface. The OCSI input can also be overdriven by an oscillator with a single-ended driver. Figure 10 shows an example of a single-ended oscillator overdrive OSCI input with AC coupling.

Note: The amplitude must be kept between 0.5V to 1.2V. The example in Figure 10 shows setting Ro + R3 ~ 100Ω results in an amplitude of ~1.1V, where Ro is output impedance of the 3.3V LVCMOS driver. The unused OSCO pin can be left floating.

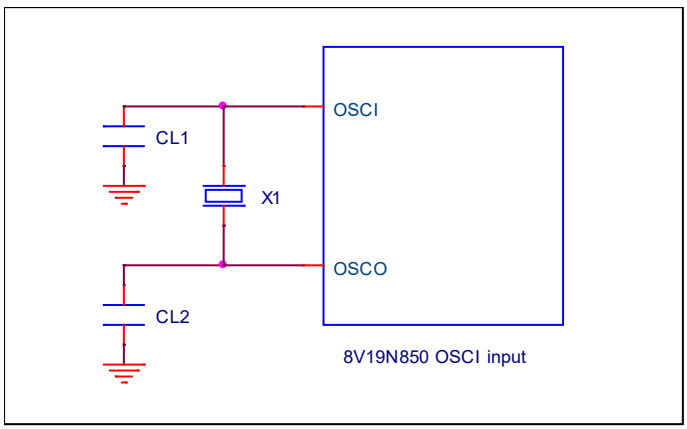

Figure 9. Crystal to OSCI Input Interface Example

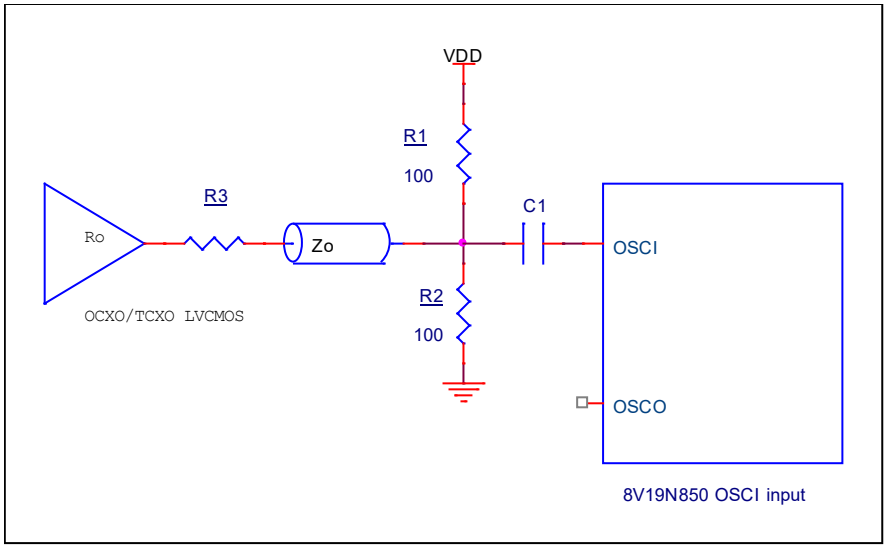

Figure 10. Single-ended Oscillator Overdrive OSCI Example

Notes:

1. When OSCI or XO_DPLL is used for input of APLL0 or APLL1 with DPLL0 or DPLL1 active, the selected frequency cannot cause the APLL0 or APLL1 feedback divider to set to an integer. For example, if APLL0 VCO = 2.5GHz, OSCI = 50MHz, the APLL0 PDF = 2x50MHz = 100MHz, the APLL0 feedback must be set to 25. The feedback divider = 25 is an integer. If DPLL0 is not active, there is no issue. If DPLL0 is active, this will create a problem and cause DPLL0 to be unstable; therefore, a 50MHz oscillator cannot be used under this condition.
2. When both XO_DPLL and OCSI are used, the two frequencies should not be close to each other.

The following list shows a few examples of OCXO:

- Rakon U7842 or different frequency in the same product family.
- TXC OG48070001 or different frequency in the same product family.
- CTS17 or different frequency in the same product family.

2.4 Output Terminations for QCLK and QREF Drivers

The output stage of the 8V19N850 QCLK drivers can be configured to be LVPECL style driver or LVDS style driver.

2.4.1. LVPECL Type Driver Terminations

When the 8V19N850 output is configured to LVPECL, the driver is an open emitter type that requires a DC current path to the termination voltage V_{TT} through the pull-down resistor. A standard LVPECL driver termination is shown in Figure 10, and Figure 12 to Figure 14 show alternative terminations. The LVPECL output driver is configurable and the applicable termination voltage V_{TT} depends on the output amplitude setting and output supply voltage V_{DDO_v}. Refer to the V_{TT} and termination resistor value tables below each diagram.

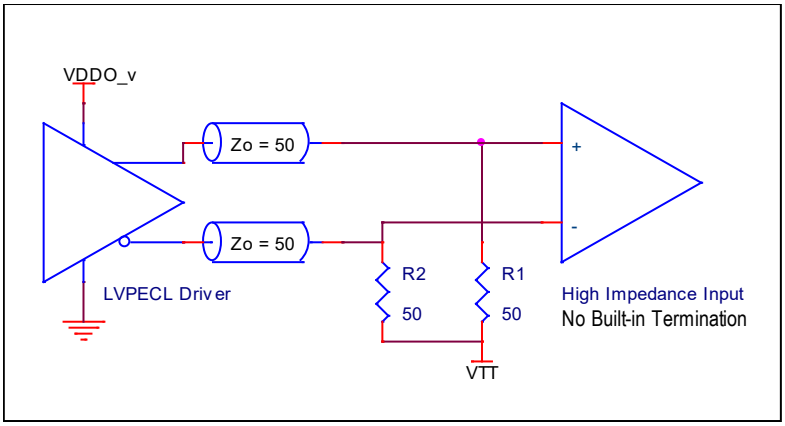

Figure 11. LVPECL Style Termination

Table 3. V_T Values for Output Termination in Figure 11

Output Supply Voltage	Output Amplitude	V_{TT}
V_{DDO_V} = 1.8V	350mV	V_{DDO_v} – 1.50V
	500mV	V_{DDO_v} – 1.75V
V_{DDO_V} = 2.5V	350mV	V_{DDO_v} – 1.50V
	500mV	V_{DDO_v} – 1.75V
V_{DDO_V} = 3.3V	350mV	V_{DDO_v} – 1.50V
	500mV	V_{DDO_v} – 1.75V
	750mV	V_{DDO_v} – 2.0V
	1000mV	V_{DDO_v} – 2.25V

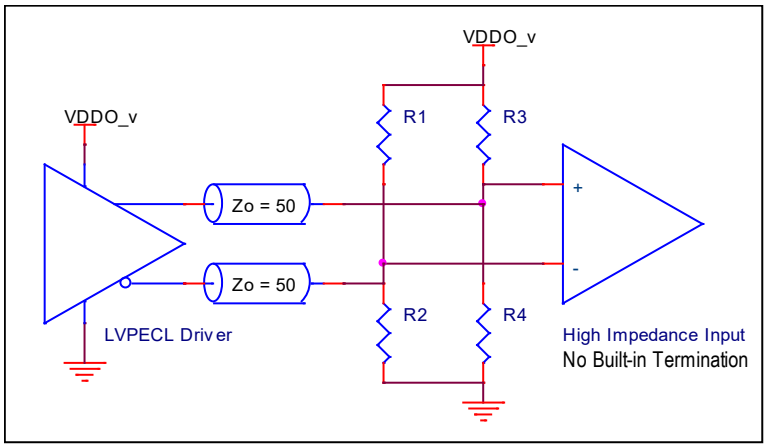

Figure 12. Alternative LVPECL Style Termination

Table 4. Resistor Values for Output Termination in Figure 12

Output Supply Voltage	Output Amplitude	R1, R3	R2, R4
V_{DDO_V} = 1.8V	350mV	350Ω	60Ω
	500mV	No-pop	50Ω
V_{DDO_V} = 2.5V	350mV	125Ω	83Ω
	500mV	166Ω	71Ω
V_{DDO_V} = 3.3V	350mV	92Ω	110Ω
	500mV	106Ω	94Ω
	750mV	127Ω	82.5Ω
	1000mV	157Ω	73Ω

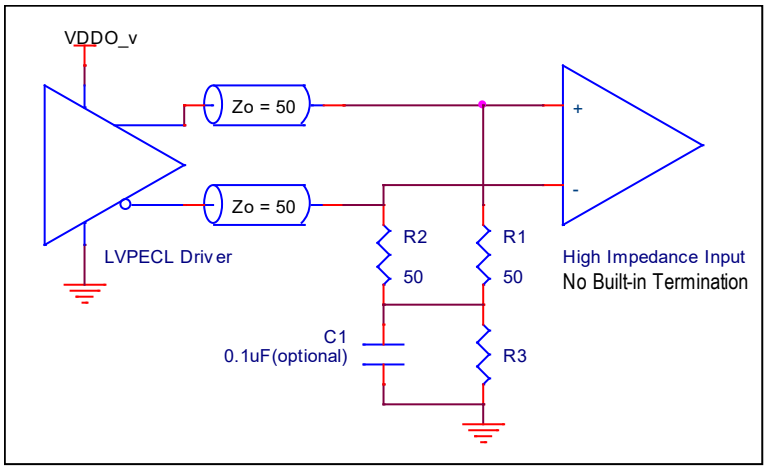

Figure 13. Alternative LVPECL Style Termination

Table 5. Resistor Values for Output Termination in Figure 13

Output Supply Voltage	Amplitude	R3
V_{DDO_V} = 1.8V	350mV	21.4Ω
	500mV	0Ω
V_{DDO_V} = 2.5V	350mV	71.4Ω
	500mV	41Ω
V_{DDO_V} = 3.3V	350mV	128Ω
	500mV	86Ω
	750mV	57Ω
	1000mV	40Ω

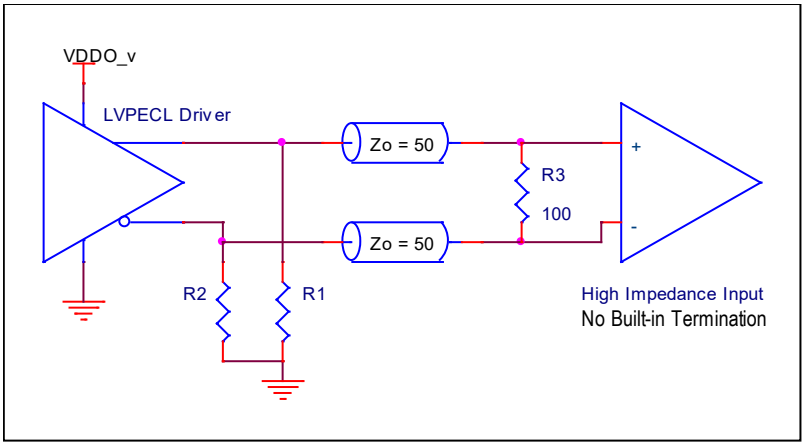

Figure 14. Alternative LVPECL Style Termination

Table 6. Resistor Values for Output Termination in Figure 14

Output Supply Voltage	Amplitude	R1, R2
V_{DDO_V} = 1.8V	350mV	93Ω
	500mV	55Ω
V_{DDO_V} = 2.5V	350mV	192Ω
	500mV	133Ω
V_{DDO_V} = 3.3V	350mV	300Ω
	500mV	222Ω
	750mV	165Ω
	1000mV	214Ω

2.4.2. LVDS Type Driver Terminations

Unlike the LVPECL style driver, the LVDS style driver does not require a board level pull-down resistor. Figure 15 and Figure 16 show typical termination examples with DC coupling for the LVDS style driver. A termination example with AC coupling is shown in Figure 17. All three figures are for LVDS receivers with a high-input impedance (no built-in 100Ω termination). For receivers with built-in 100Ω termination, see the note below Figure 17.

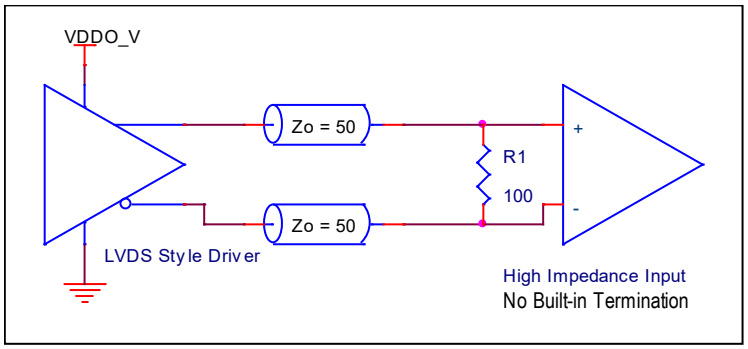

Figure 15. LVDS Style Driver Termination (DC Coupled)

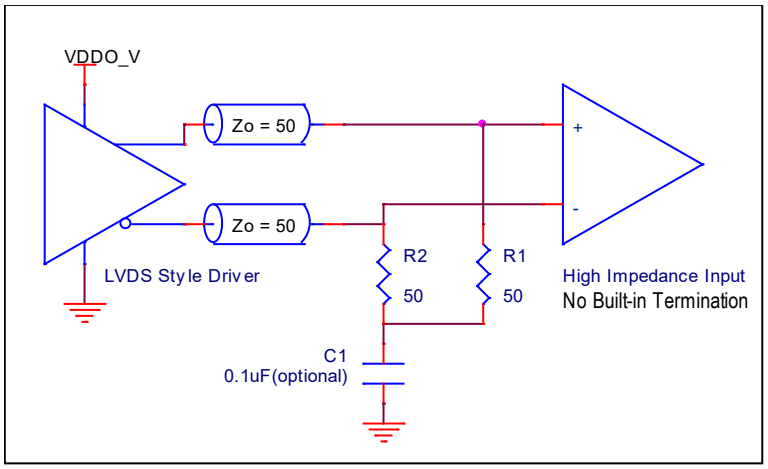

Figure 16. LVDS Style Alternative Driver Termination (DC Coupled)

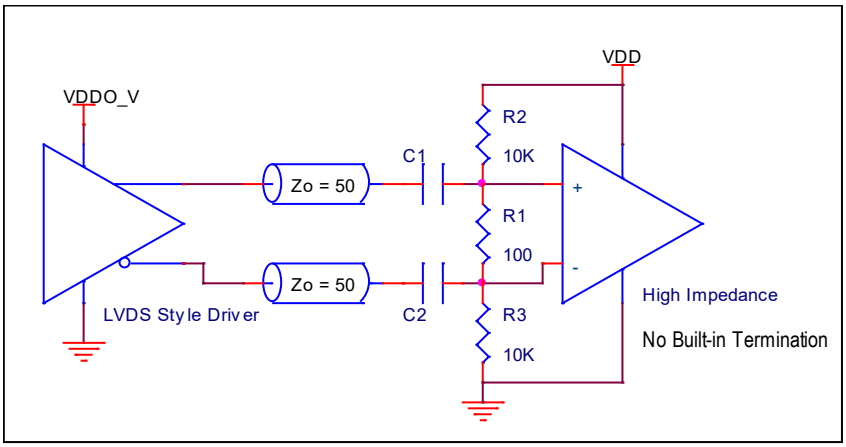

Figure 17. LVDS Style Alternative Driver Termination (AC Coupled)

Note: For receivers with built-in 100Ω termination that provides its own DC offset (self-bias), apply the AC-coupled termination shown in Figure 17 and do not populate the resistors R1, R2, and R3.

3. Schematic Example

A reference demonstration board schematic and the board layout are available upon request:

- 8V19N850 EVB schematic
- 8V19N850 EVB board layout

4. Revision History

Revision	Date	Description
1.01	Jan 5, 2024	Added the fourth paragraph descriptive text in section 2.3 OSCI/OSCO Input (XTAL, XO, OCXO/TCXO).
-	Mar 25, 2021	Initial release.

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