# RX FAMILY
# HARDWARE MANUAL GUIDANCE
# (ELECTRICAL CHARACTERISTICS)

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RENESAS ELECTRONICS



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# DC CHARACTERISTICS

# ABSOLUTE MAXIMUM RATINGS

## 60.1 Absolute Maximum Ratings

**Table 60.1 Absolute Maximum Rating**

Conditions: VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V

| Item | | Symbol | Value | Unit |
|---|---|---|---|---|
| Power supply voltage | | VCC, VCC_USB | –0.3 to +4.0 | V |
| $V_{BATT}$ power supply voltage | | $V_{BATT}$ | –0.3 to +4.0 | V |
| Input voltage (except for ports for 5 V tolerant*1) | | $V_{in}$ | –0.3 to VCC + 0.3 (up to 4.0) | V |
| Input voltage (ports for 5 V tolerant*1) | | $V_{in}$ | –0.3 to VCC + 4.0 (up to 5.8) | V |
| Reference power supply voltage | | VREFH0 | –0.3 to AVCC0 + 0.3 (up to 4.0) | V |
| Analog power supply voltage | | AVCC0, AVCC1*2 | –0.3 to +4.0 | V |
| Analog input voltage | | $V_{AN}$ | –0.3 to AVCC + 0.3 (up to 4.0) | V |
| Junction temperature | D version | $T_j$ | –40 to +105 | °C |
| | G version | $T_j$ | –40 to +125 | °C |
| Storage temperature | | $T_{stg}$ | –55 to +125 | °C |

Caution: Permanent damage to the LSI may result if absolute maximum ratings are exceeded.

Note 1. Ports 07, 11 to 17, 20, 21, 30 to 33, 67, and C0 to C3 are 5 V tolerant.

Note 2. Connect the AVCC0, AVCC1, and VCC_USB pins to VCC, and the AVSS0, AVSS1, and VSS_USB pins to VSS. When the A/D converter unit 0 is not to be used, connect the VREFH0 pin to VCC and the VREFL0 pin to VSS, respectively. Do not leave these pins open. Insert capacitors of high frequency characteristics between the AVCC0 and AVSS0 pins, or AVCC1 and AVSS1 pins. Place capacitors of about 0.1 µF as close as possible to every power supply pin and use the shortest and heaviest possible traces.

The range that does not cause "permanent damage" to the LSI. It doesn't mean the normal operation is guaranteed.

Requirements to guarantee the following electrical characteristics

The voltage ranges of power supply that don't cause permanent damage

The input voltage ranges that don't cause permanent damage to pins.

The value in the bracket is applied when VCC or AVCC is equal or greater than the minimum voltage described in the recommended operating voltage.

Junction temperature range that doesn't cause permanent damage

The storage temperature when the chip doesn't operate

Supplementary information for electrical property items.
Necessary conditions for use.

# RECOMMENDED OPERATING CONDITIONS

The USB power supply's specification differs between when USB is in use (3.3V) and when USB is not in use (5V). If VCC_USB is connected to 5V VCC since USB is not in use initially, the change to use USB later will cause incompliance to USB power supply's specification. Please make sure to comply with USB power supply's specification.

The temperature at which the operation is guaranteed. Equivalent to Ta unless otherwise specified.

This relationship should be maintained during power-up as well

Must follow the recommended value for the smoothing capacitor for internal power supply stabilization. Otherwise, the normal operation couldn't be guaranteed.

**Table 45.2 Recommended operating conditions (1)**

| Item | | | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| Power supply voltage | | | VCC*1 | 2.7 | — | 5.5 | V |
| | | | VSS | — | 0 | — | |
| USB power supply voltage*2 | | When USB in use | VCC_USB*1 | 3.0 | — | 3.6 | |
| | | | VSS_USB | — | 0 | — | |
| | | When USB not in use | VCC_USB | — | VCC | — | |
| | | | VSS_USB | — | VSS | — | |
| Analog power supply voltage*3 | | | AVCC0, AVCC1, AVCC2*1 | 3.0 | — | 5.5 | |
| | | | AVSS0, AVSS1, AVSS2 | — | 0 | — | |
| Input voltage | PB1, PB2, PC0*4, and PD2*4 | | $V_{in}$ | –0.3 | — | 5.8 | |
| | P40 to P42, and P44 to P46 | With negative input enabled*5 | | –1.0 | — | AVCC1 + 0.3 | |
| | | With negative input disabled | | –0.3 | — | | |
| | PH0, PH4 | With negative input enabled*5 | | –0.5 | — | AVCC1 + 0.3 | |
| | | With negative input disabled | | –0.3 | — | | |
| | P43, P47, PH1 to PH3, and PH5 to PH7 | | | –0.3 | — | AVCC1 + 0.3 | |
| | P50 to P55, and P60 to P65 | | | –0.3 | — | AVCC2 + 0.3 | |
| | USB0_DP, USB0_DM | | | –0.3 | — | VCC_USB + 0.3 | |
| | Other than above | | | –0.3 | — | VCC + 0.3 | |
| Operating temperature | D version | | $T_{opr}$ | –40 | — | 85 | °C |
| | G version | | | –40 | — | 105 | |

Note 1. Comply with the following voltage condition: VCC_USB ≤ VCC ≤ AVCC0 = AVCC1 = AVCC2
Note 2. When the USB interface is not to be used, connect VCC_USB to VCC and VSS_USB to VSS, and set VOLSR.USBVON=0.
Note 3. When not using any of the12-bit A/D converter (unit 0 to 2), 12-bit D/A converter, comparator C, or temperature sensor, connect AVCC0, AVCC1, and AVCC2 to VCC, and AVSS0, AVSS1, and AVSS2 to VSS, respectively. For details, refer to section 38.6.10, Voltage Range of Analog Power Supply Pins.
Note 4. This is only available for products with 128 Kbytes of RAM.
Note 5. When VOLSR.PGAVLS = 0 and ADPGADCR0.PxDEN = 1 (x = 000, 001, 002, 100, 101, 102).

**Table 45.3 Recommended operating conditions (2)**

| Item | Symbol | Value |
|---|---|---|
| Decoupling capacitance to stabilize the internal voltage | $C_{VCL}$ | 0.47 µF ± 30%*1 |

Note 1. Use a multilayer ceramic capacitor whose nominal capacitance is 0.47 µF and a capacitance tolerance is ±30% or better.

Conditions to guarantee AC specifications and normal operation

The reference voltage might be different between pins

Refer to the application note for precaution of high-temperature operation.

**Notes on High-Temperature Operation**

VCL should be connected only to VSS via a capacitor.(Do not connect to VCC)

Only multilayer ceramic capacitors should be used

# DC CHARACTERISTICS

**Table 45.4 DC Characteristics (1)**

Conditions: VCC = 2.7 to 5.5 V, VCC_USB = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5V,
VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V,
$T_a = T_{opr}$

| Item | | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| Schmitt trigger input voltage | CAN input pin<br>MTU input pin<br>GPTW input pin<br>POE input pin<br>POEG input pin<br>TMR input pin<br>SCI input pin<br>ADTRG# input pin<br>RES#, NMI | $V_{IH}$ | 0.8 × VCC | — | — | V | |
| | | $V_{IL}$ | — | — | 0.2 × VCC | | |
| | | $\Delta V_T$ | 0.06 × VCC | — | — | | |
| | IRQ input pin<br>(except for P52 to P55, and P60 to P65) | $V_{IH}$ | 0.8 × VCC | — | — | | |
| | | $V_{IL}$ | — | — | 0.2 × VCC | | |
| | | $\Delta V_T$ | 0.06 × VCC | — | — | | |
| | IRQ input pin<br>(P52 to P55, and P60 to P65) | $V_{IH}$ | 0.8 × AVCC2 | — | — | | |
| | | $V_{IL}$ | — | — | 0.2 × AVCC2 | | |
| | | $\Delta V_T$ | 0.06 × AVCC2 | — | — | | |
| | RIIC input pin<br>(except for SMBus) | $V_{IH}$ | 0.7 × VCC | — | — | | |
| | | $V_{IL}$ | — | — | 0.3 × VCC | | |
| | | $\Delta V_T$ | 0.06 × VCC | — | — | | |
| | Pins for 5 V tolerant<br>(PB1, PB2, PC0*1, and PD2*1) | $V_{IH}$ | 0.8 × VCC | — | — | | |
| | | $V_{IL}$ | — | — | 0.2 × VCC | | |
| | Analog input pins<br>(P40 to P47, and PH0 to PH7) | $V_{IH}$ | 0.8 × AVCC1 | — | — | | |
| | | $V_{IL}$ | — | — | 0.2 × AVCC1 | | |
| | Analog input pins<br>(P50 to P55, and P60 to P65) | $V_{IH}$ | 0.8 × AVCC2 | — | — | | |
| | | $V_{IL}$ | — | — | 0.2 × AVCC2 | | |
| | Other input pins<br>(pins other than those above) | $V_{IH}$ | 0.8 × VCC | — | — | | |
| | | $V_{IL}$ | — | — | 0.2 × VCC | | |
| High-level input voltage (except for Schmitt trigger input pin) | MD pin, EMLE | $V_{IH}$ | 0.9 × VCC | — | — | V | |
| | EXTAL, WAIT#, RSPI input pin | | 0.8 × VCC | — | — | | |
| | D0 to D15 | | 0.7 × VCC | — | — | | |
| | RIIC (SMBus) | | 2.1 | — | — | | |
| Low-level input voltage (except for Schmitt trigger input pin) | MD pin, EMLE | $V_{IL}$ | — | — | 0.1 × VCC | V | |
| | EXTAL, WAIT#, RSPI input pin | | — | — | 0.2 × VCC | | |
| | D0 to D15 | | — | — | 0.3 × VCC | | |
| | RIIC (SMBus) | | — | — | 0.8 | | |

Note 1. This is only available for products with 128 Kbytes of RAM.

Required conditions to guarantee the following specifications

The reference voltage might be different between pins

Terminals for which ΔVt is not specified are not guaranteed to have hysteresis width. It is only guaranteed to be recognized as High if it is above VIHmin and Low if it is below VILmax.

# DC CHARACTERISTICS

**Table 45.5 DC Characteristics (2)**

Conditions: VCC = 2.7 to 5.5 V, VCC_USB = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5V, VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V, $T_a = T_{opr}$

| Item | | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| High-level output voltage | P43, P47, PH1 to PH3, and PH5 to PH7 | $V_{OH}$ | AVCC1 – 0.5 | — | — | V | $I_{OH}$ = –1.0 mA |
| | P50 to P55, and P60 to P65 | | AVCC2 – 0.5 | — | — | | $I_{OH}$ = –1.0 mA |
| | P90 to P95, P71 to P76, P81, PB5, and PD3 | | VCC – 1.0 | — | — | | $I_{OH}$ = –5.0 mA (when the large current output is set) |
| | Other than above | | VCC – 0.5 | — | — | | $I_{OH}$ = –1.0 mA |
| Low-level output voltage | P43, P47, PH1 to PH3, and PH5 to PH7 | $V_{OL}$ | — | — | 0.5 | | $I_{OL}$ = 1.0 mA |
| | P50 to P55, and P60 to P65 | | — | — | 0.5 | | $I_{OL}$ = 1.0 mA |
| | P90 to P95, P71 to P76, P81, PB5, and PD3 | | — | — | 1.0 | | $I_{OL}$ = 15 mA (when the large current output is set) |
| | RIIC pins | | — | — | 0.4 | | $I_{OL}$ = 3.0 mA |
| | | | — | — | 0.6 | | $I_{OL}$ = 6.0 mA |
| | Other than above | | — | — | 0.5 | | $I_{OL}$ = 1.0 mA |
| Input leakage current | RES#, MD pin, PE2, and EMLE*1 | $\lvert I_{in} \rvert$ | — | — | 1.0 | μA | $V_{in}$ = 0 V<br>$V_{in}$ = VCC |
| | P40 to P42, and P44 to P46 | | — | — | 1.0 | | $V_{in}$ = 0 V<br>$V_{in}$ = AVCC1 |
| | PH0 and PH4 | | — | — | 1.0 | | $V_{in}$ = 0 V<br>$V_{in}$ = AVCC1<br>VOLSR.PGAVLS = 1 |
| Three-state leakage current (off state) | RIIC pins | $\lvert I_{TSI} \rvert$ | — | — | 5.0 | | $V_{in}$ = 0 V<br>$V_{in}$ = VCC |
| | Other than above | | — | — | 1.0 | | |
| Input pull-up resistors current | P43, P47, PH1 to PH3, PH5 to PH7, P50 to P55, and P60 to P65 | $I_p$ | –300 | — | –10 | | AVCC1 = AVCC2 = 3.0 to 5.5 V<br>$V_{in}$ = 0 V |
| | Pins other than those above and PE2 | | –300 | — | –10 | | VCC = 2.7 to 5.5 V<br>$V_{in}$ = 0 V |
| Input pull-down resistors current | EMLE | | 10 | — | 300 | | $V_{in}$ = VCC = AVCC |
| Input capacitance | RIIC pins, PH0, and PH4 | $C_{in}$ | — | — | 16 | pF | $V_{bias}$ = 0 V<br>$V_{amp}$ = 20 mV<br>f = 1 MHz<br>$T_a$ = 25°C |
| | USB0_DP, and USB0_DM pins | | — | — | 16 | | |
| | Other than above | | — | — | 8 | | |
| Output voltage of the VCL pin | | $V_{CL}$ | — | 1.25 | — | V | |

Note 1. The input leakage current value at the EMLE pin is only when $V_{in}$ = 0 V.

Required conditions to guarantee the following specifications

For information under the test conditions which are not listed here, refer to the IBIS model

Leakage current of terminals other than those described in the "Input Leakage Current" item.
The off state refer to the high impedance state

Built-in pull-up resistor value can be calculated by using this value

Pull-up resistor = voltage in use ÷ Ip

# DC CHARACTERISTICS

Current consumption when all functions except BGO are in operation.

Current consumption value when BGO is not working and the clock to modules described in Module Stop Control Registers is supplied/stopped

Current consumption value of each low power consumption mode. Refer to Low Power Consumption chapter for the peripheral state of each modes.

(Below is an example of RX66T)

**Table 11.2 Entering and Exiting Low Power Consumption Modes and Operating States in Each Mode**

| Entering and Exiting Low Power Consumption Modes and Operating States | Sleep Mode | All-Module Clock Stop Mode | Software Standby Mode | Deep Software Standby Mode |
|---|---|---|---|---|
| Transition condition | Control register + instruction | Control register + instruction | Control register + instruction | Control register + instruction |
| Method of release other than reset | Interrupt | Interrupt*1 | Interrupt*2 | Interrupt*3 |
| State after release*4 | Program execution state (interrupt processing) | Program execution state (interrupt processing) | Program execution state (interrupt processing) | Program execution state (reset processing) |
| Main clock oscillator | Operating possible | Operating possible | Stopped | Stopped |
| High-speed on-chip oscillator | Operating possible | Operating possible | Stopped | Stopped |
| Low-speed on-chip oscillator | Operating possible | Operating possible | Stopped | Stopped |
| IWDT-dedicated on-chip oscillator | Operating possible*5 | Operating possible*5 | Operating possible*5 | Stopped (Undefined)*5 |
| PLL | Operating possible | Operating possible | Stopped | Stopped |
| CPU | Stopped (Retained) | Stopped (Retained) | Stopped (Retained) | Stopped (Undefined) |
| RAM and ECCRAM | Operating possible (Retained) | Stopped (Retained) | Stopped (Retained) | Stopped (Undefined) |
| Flash memory | Operating | Stopped (Retained) | Stopped (Retained) | Stopped (Retained) |
| USBFS host/function module (USBb) | Operating possible | Stopped*6 | Stopped*6 | Stopped (Undefined) |
| Watchdog timer (WDTA) | Stopped (Retained) | Stopped (Retained) | Stopped (Retained) | Stopped (Undefined) |
| Independent watchdog timer (IWDT) | Operating possible*5 | Operating possible*5 | Operating possible*5 | Stopped (Undefined)*5 |
| Port output enable (POE) | Operating possible | Operating possible*7 | Stopped (Retained) | Stopped (Undefined) |
| 8-bit timer (unit 0, unit 1) (TMR) | Operating possible | Operating possible*8 | Stopped (Retained) | Stopped (Undefined) |
| Voltage detection circuit (LVDA) | Operating possible | Operating possible | Operating possible | Operating possible*9 |
| Power-on reset circuit | Operating | Operating | Operating | Operating |
| Peripheral modules | Operating possible | Stopped (Retained) | Stopped (Retained) | Stopped (Undefined) |
| I/O ports | Operating | Retained*10 | Retained*11 | Retained*11 |

Required conditions to guarantee the following specifications

**Table 45.6 DC Characteristics (3) (Products with 64 Kbytes of RAM, D version)**

Conditions: VCC = 2.7 to 5.5 V, VCC_USB = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5V,
VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V,
$T_a = T_{opr}$

| Item | | | Symbol | D version Min. | D version Typ. | D version Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|---|
| Supply current*1 | Normal operating mode | Full operation*2 | $I_{CC}$*3 | — | — | 75 | mA | ICLK = 160 MHz<br>PCLKA = 80 MHz<br>PCLKB = 40 MHz<br>PCLKC = 160 MHz<br>PCLKD = 40 MHz<br>FCLK = 40 MHz<br>BCLK = 40 MHz<br>BCLK pin = 40 MHz |
| | | Normal operation: Peripheral module clocks are supplied*4 | | — | 21 | — | | |
| | | Normal operation: Peripheral module clocks are stopped *4, *5 | | — | 12 | — | | |
| | | CoreMark: Peripheral module clocks are stopped *4, *5 | | — | 21 | — | | |
| | | Sleep mode: Peripheral module clocks are supplied*4 | | — | 18 | 37 | | |
| | | All module clock stop mode (reference value) | | — | 9.4 | 23 | | |
| | | Increase current by BGO operation*6 | | — | 13 | — | | |
| | | Increase current by operating Trusted Secure IP | | — | 3.9 | 5.0 | | |
| | Software standby mode | | | — | 0.9 | 7.0 | | VOLSR.PGAVLS = 1 |
| | Deep software standby mode | | | — | 14 | 20 | µA | VOLSR.PGAVLS = 1 |

Note 1. Supply current values are measured when all output pins are unloaded and all input pull-up resistors are disabled.
Note 2. Peripheral module clocks are supplied. This does not include operations as BGO (background operations).
Note 3. $I_{CC}$ depends on f (ICLK) as follows.
(when ICLK : PCLKA : PCLKB : PCLKC : PCLKD : BCLK : BCLK pin = 4 : 2 : 1 : 4 : 1 : 1 : 1 and EX
• D version product
$I_{CC}$ Max. = 0.375 × f + 15 (full operation in high-speed operating mode)
$I_{CC}$ Typ. = 0.099 × f + 5 (normal operation in high-speed operating mode)
$I_{CC}$ Max. = 0.135 × f + 15 (sleep mode)
Note 4. This does not include operations as BGO (background operations). Whether the peripheral module stopped is controlled only by the bit settings in the module stop control registers A to D.
Note 5. When peripheral module clocks are stopped, each clock frequency is set for division by 64, and the f PCLKA, PCLKB, PCLKC, PCLKD, and the BCLK pin are the same.
Note 6. This is an increase caused by program/erase operation to the code flash memory or data flash memory during executing the user program.

Differences in Typ/max are due to temperature, manufacturing variations, etc. (in particular due to temperature)

How to calculate the actual current consumption is described in “Precautions for high temperature operation of each group”. For details, please refer to the document below.

Useful Information for RX MCUs

# DC CHARACTERISTICS

Required conditions to guarantee the following specifications

**Table 45.11 DC Characteristics (5)**

Conditions: VCC = 2.7 to 5.5 V, VCC_USB = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5 V,
VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V,
$T_a = T_{opr}$

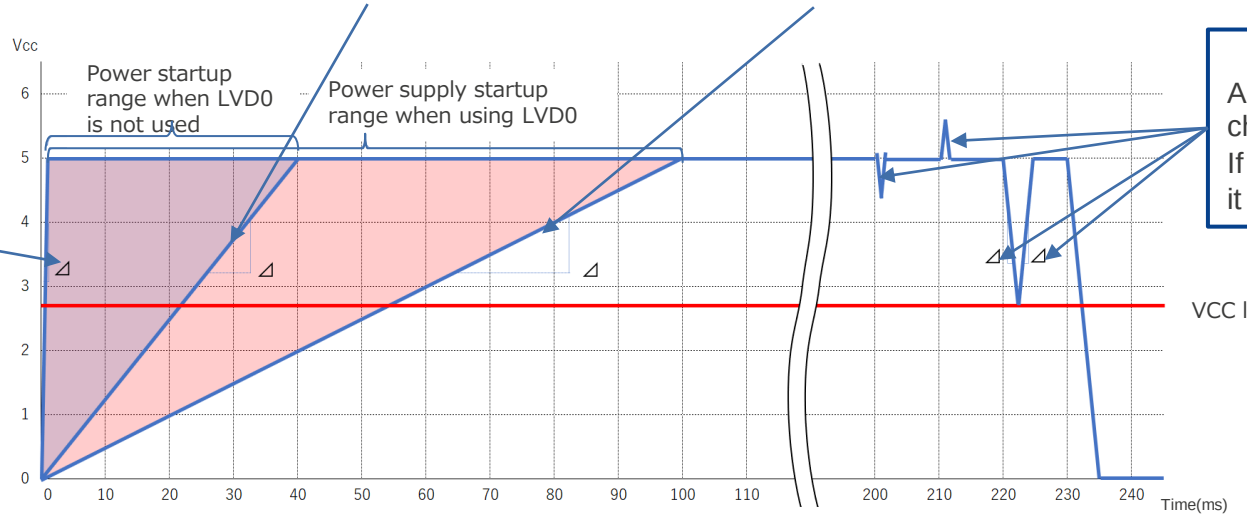
| Item | | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| VCC ramp rate at power-on | At normal startup | SrVCC | 0.02 | — | 8 | ms/V | |
| | Voltage monitoring 0 reset enabled at startup*1, *2 | | 0.02 | — | 20 | | |
| VCC ramp rate at power fluctuation | | dt/dVCC | 1.0 | — | — | | When VCC change exceeds VCC ±10% |

Note 1. When OFS1.LVDAS = 0.
Note 2. Settings of the OFS1 register are not read in boot mode or user boot mode, so turn on the power supply voltage with a ramp rate at normal startup.

Allowable slope of power supply variation when VCC variation exceeds ±10%.

SrVCC(MAX)
VCC ramp rate at power-on when LVD0 is not used. If the VCC ramp rate is slower than this, it is out of the guaranteed range (8ms/V)

SrVCC(MAX)
VCC ramp rate at power-on when LVD0 is used. If the VCC ramp rate is slower than this, it is out of the guaranteed range (20ms/V)




Example when VCC=5V

SrVCC(MIN)
if VCC ramp rate at power-on is more rapidly than this, it is out of the guaranteed range (0.02ms/V)

dt/dVCC
Allowable rising/falling slope of a voltage change (greater than ±10%).
If a voltage change is more rapid than this, it is out of the guaranteed range. (1ms/V)

# DC CHARACTERISTICS

Required conditions to guarantee the following specifications

The current value that flows in from external

Average current over MCU driving time.

(Example) If the values are 1mA, 2mA and 3mA, the average value is 6mA/3 = Average 2mA

The maximum allowable current value that can flow in per pin. If this value is exceeded, reliability cannot be ensured.

Total current value of all MCU output pins

The current value that flows out from MCU

Port driving ability set by Port Capacity Control register (DSCRx). The output impedance is as follows.

Normal drive > High drive > High speed interface high drive

**Table 61.8 Permissible Output Currents**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

| Item | | | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| Permissible output low current (average value per pin) | All output pins*1 | Normal drive | $I_{OL}$ | — | — | 2.0 | mA |
| | All output pins*2 | High drive | | — | — | 3.8 | |
| | All output pins*3 | High-speed interface high-drive | | — | — | 7.5 | |
| Permissible output low current (max. value per pin) | All output pins*1 | Normal drive | $I_{OL}$ | — | — | 4.0 | mA |
| | All output pins*2 | High drive | | — | — | 7.6 | |
| | All output pins*3 | High-speed interface high-drive | | — | — | 15 | |
| Permissible output low current (total) | Total of all output pins | | $\Sigma I_{OL}$ | — | — | 80 | mA |
| Permissible output high current (average value per pin) | All output pins*1 | Normal drive | $I_{OH}$ | — | — | –2.0 | mA |
| | All output pins*2 | High drive | | — | — | –3.8 | |
| | All output pins*3 | High-speed interface high-drive | | — | — | –7.5 | |
| Permissible output high current (max. value per pin) | All output pins*1 | Normal drive | $I_{OH}$ | — | — | –4.0 | mA |
| | All output pins*2 | High drive | | — | — | –7.6 | |
| | All output pins*3 | High-speed interface high-drive | | — | — | –15 | |
| Permissible output high current (total) | Total of all output pins | | $\Sigma I_{OH}$ | — | — | –80 | mA |

Caution: To protect the MCU's reliability, the output current values should not exceed the values in Table 61.8.

Note 1. This is the value when normal driving ability is set with a pin for which normal driving ability is selectable.

Note 2. This is the value when high driving ability is set with a pin for which normal driving ability is selectable or the value of the pin to which high driving ability is fixed.

Note 3. This is the value when high-speed interface high-driving ability is set with a pin for which high-speed interface high-driving ability is selectable.

# DC CHARACTERISTICS

**Table 45.13 Thermal Resistance Value (Reference)**

Conditions: VCC = 2.7 to 5.5 V, VCC_USB = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5V,
VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V,
$T_a = T_{opr}$

| Item | Package | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| Thermal resistance | 144-pin LFQFP (PLQP0144KA-B) | $\theta_{ja}$ | — | — | 32.4 | °C/W | JESD51-2 and JESD51-7 compliant |
| | 112-pin LQFP (PLQP0112JA-B) | | — | — | 33.8 | | |
| | 100-pin LFQFP (PLQP0100KB-B) | | — | — | 35.0 | | |
| | 80-pin LFQFP (PLQP0080KB-B) | | — | — | 36.3 | | |
| | 80-pin LQFP (PLQP0080JA-A) | | — | — | 35.7 | | |
| | 64-pin LFQFP (PLQP0064KB-C) | | — | — | 37.9 | | |
| | 144-pin LFQFP (PLQP0144KA-B) | $\Psi_{jt}$ | — | — | 0.6 | | |
| | 112-pin LQFP (PLQP0112JA-B) | | — | — | 0.6 | | |
| | 100-pin LFQFP (PLQP0100KB-B) | | — | — | 0.8 | | |
| | 80-pin LFQFP (PLQP0080KB-B) | | — | — | 0.8 | | |
| | 80-pin LQFP (PLQP0080JA-A) | | — | — | 0.8 | | |
| | 64-pin LFQFP (PLQP0064KB-C) | | — | — | 0.8 | | |

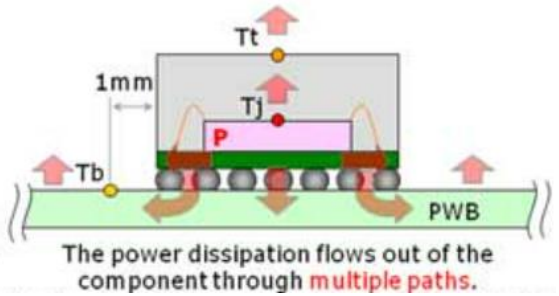
Note: The values are reference values when the 4-layer printed circuit board is used. Thermal resistance depends on the number of layers and size of the board. For details, refer to the JEDEC standards.

Thermal resistance according to JEDEC standard.
Please refer to below for details.

<Heat-dissipation Mechanism | Renesas>

Θja=(Tj-Ta)/P

Ψjt=(Tj-Tt)/P

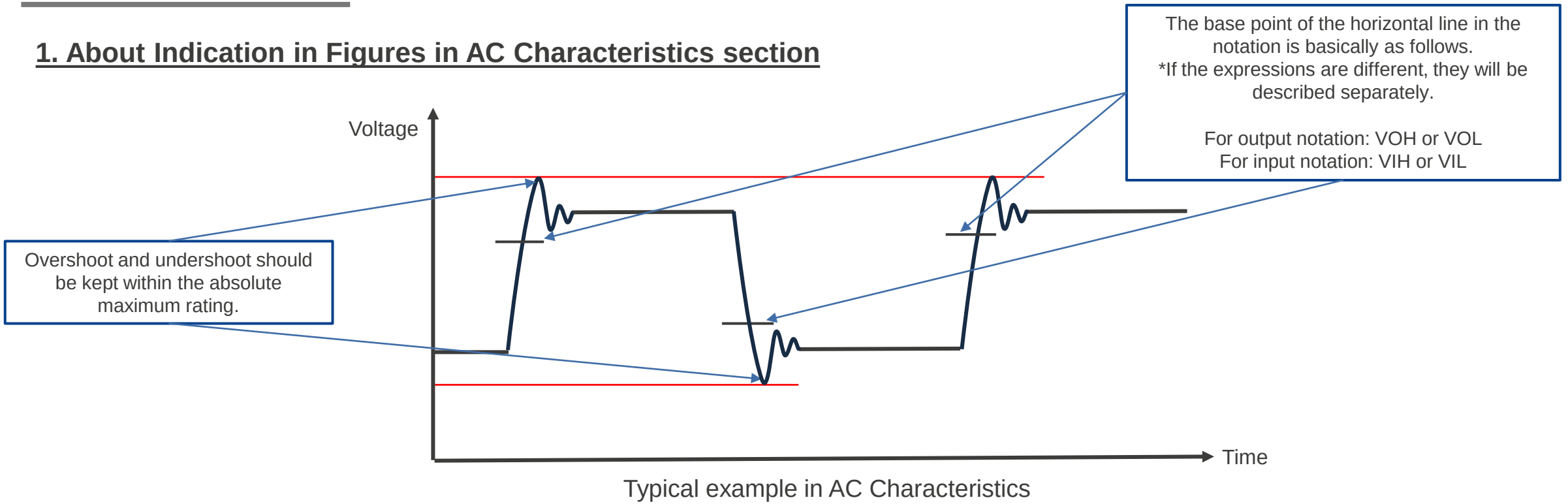



Ta: Temperature of a place not affected by a heat source

# AC CHARACTERISTICS AND OTHERS

# PREREQUISITES:

## 1. About Indication in Figures in AC Characteristics section




Typical example in AC Characteristics

## 2. Notation of clocks in AC Specification section

Depending on the product, there are places where the clock notation is omitted.
For the exact clock name, refer to the Clock section of the hardware manual.

Example : Notation in AC Characteristics section : PCLK,  notation in Clock section : PCLKB
Notation in AC Characteristics section : ADCLK, notation in Clock section : PCLKD

# AC CHARACTERISTICS : RESET TIMING

Required conditions to guarantee the following specifications.

45.4.1 Reset Timing

**Table 45.17 Reset Timing**

Conditions: VCC = 2.7 to 5.5 V, VCC_USB = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5V,
VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V,
$T_a = T_{opr}$

| Item | | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| RES# pulse width | Power-on | $t_{RESWP}$ | 2.0 | — | — | ms | Figure 45.2 |
| | Deep software standby mode | $t_{RESWD}$ | 0.6 | — | — | | Figure 45.3 |
| | Software standby mode | $t_{RESWS}$ | 0.3 | — | — | | |
| | Programming or erasure of the code flash memory, or programming, erasure or blank checking of the data flash memory | $t_{RESWF}$ | 200 | — | — | µs | |
| | Other than above | $t_{RESW}$ | 200 | — | — | | |
| Waiting time after release from the RES# pin reset | | $t_{RESWT}$ | 62 | — | 63 | $t_{Lcyc}$ | Figure 45.2 |
| Internal reset time (independent watchdog timer reset, watchdog timer reset, software reset) | | $t_{RESW2}$ | 108 | — | 116 | | |

This is the reset time required for internal initialization.
Be sure to input a reset that is greater than or equal to the value described in this manual. If the reset time is short, the MCU may not be initialized correctly and operation may not be possible.

After the reset pin is turned High, the reset process is required internally. After this time has elapsed, the reset is canceled and the user program is executed.

The starting point of tRESWP is the lower limit of the recommended line-voltage (in this case, 2.7V).

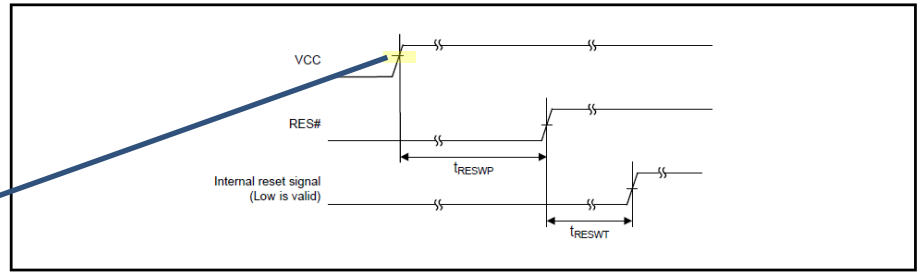



**Figure 45.2 Reset Input Timing at Power-On**

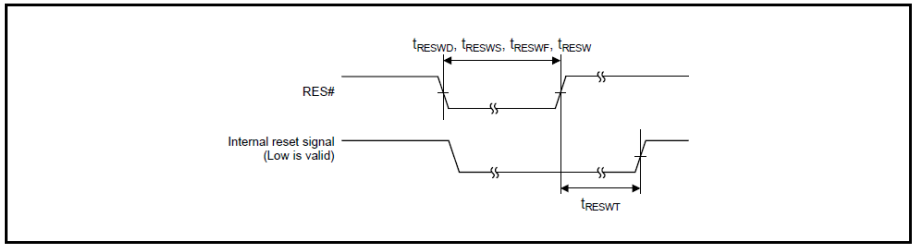



**Figure 45.3 Reset Input Timing**

# POWER-ON RESET CIRCUIT AND VOLTAGE DETECTION CIRCUIT CHARACTERISTICS

This is used to release the internal-reset state **at the time of power-on (when VCC rises)**. Internal-reset release is released after tdet+tPOR period has elapsed from VPOR. Increase VCC to the operating voltage before releasing.

Enable or disable can be selected by the voltage that generates the internal reset **when VCC drops**. When enabled, the voltage can be selected from n level (2 level in this example). The internal-reset release is released after the elapse of tdet+tLVD0 period from Vdet0. Increase VCC to the operating voltage before releasing.

These are the voltages that interrupt (You can choose from non-maskable and maskable. In addition, the timing of occurrence can be selected from both ascent and descent.) or cause an internal reset **when VCC rises and falls**. Enabled/Disabled can be selected. The voltage can be selected from n levels (5 levels in this example). When LVD1RN(LVD2RN) = "0", the internal-reset release is released after Vdet1 (2) rising voltage elapses for tdet+tLVD1 (2) time, and when LVD1RN(LVD2RN) = "1", the internal-reset release is released after tLVD1 (2) time elapses for Vdet1 (2) falling voltage. Increase VCC to the operating voltage before releasing.

45.11 Power-on Reset Circuit and Voltage Detection Circuit Characteristics

**Table 45.54 Power-on Reset Circuit and Voltage Detection Circuit Characteristics**

Conditions: VCC = 2.7 to 5.5 V, VCC_USB = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5V, VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V, $T_a = T_{opr}$

| | Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| Voltage detection level | Power-on reset (POR) | $V_{POR}$ | 2.46 | 2.58 | 2.70 | V | Figure 45.67 |
| | Voltage detection circuit (LVD0) | $V_{det0\_1}$ | 4.04 | 4.22 | 4.40 | | Figure 45.68 |
| | | $V_{det0\_2}$ | 2.71 | 2.83 | 2.95 | | |
| | Voltage detection circuit (LVD1) | $V_{det1\_0}$ | 4.39 | 4.57 | 4.75 | | Figure 45.69 |
| | | $V_{det1\_1}$ | 4.29 | 4.47 | 4.65 | | |
| | | $V_{det1\_2}$ | 4.14 | 4.32 | 4.50 | | |
| | | $V_{det1\_3}$ | 2.81 | 2.93 | 3.05 | | |
| | | $V_{det1\_4}$ | 2.76 | 2.88 | 3.00 | | |
| | Voltage detection circuit (LVD2) | $V_{det2\_0}$ | 4.39 | 4.57 | 4.75 | | Figure 45.70 |
| | | $V_{det2\_1}$ | 4.29 | 4.47 | 4.65 | | |
| | | $V_{det2\_2}$ | 4.14 | 4.32 | 4.50 | | |
| | | $V_{det2\_3}$ | 2.81 | 2.93 | 3.05 | | |
| | | $V_{det2\_4}$ | 2.76 | 2.88 | 3.00 | | |
| Internal reset time | Power-on reset time | $t_{POR}$ | — | 13.7 | — | ms | Figure 45.67 |
| | LVD0 reset time | $t_{LVD0}$ | — | 0.70 | — | | Figure 45.68 |
| | LVD1 reset time | $t_{LVD1}$ | — | 0.57 | — | | Figure 45.69 |
| | LVD2 reset time | $t_{LVD2}$ | — | 0.57 | — | | Figure 45.70 |
| Minimum VCC down time | | $t_{VOFF}$ | 200 | — | — | µs | Figure 45.67, Figure 45.68 |
| Response delay time | | $t_{det}$ | — | — | 200 | µs | Figure 45.67 to Figure 45.70 |
| LVD operation stabilization time (after LVD is enabled) | | $T_{d(E-A)}$ | — | — | 20 | µs | Figure 45.69, Figure 45.70 |
| Hysteresis width (LVD1 and LVD2) | | $V_{LVH}$ | — | 80 | — | mV | |

Note: The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels $V_{POR}$, $V_{det1}$, and $V_{det2}$ for the POR/ LVD.

Required conditions to guarantee the following specifications.

Internal-reset holding period of POR.

Internal-reset holding period of LVDn.

This is the time below the detect voltage (the time from detecting the voltage at VCC drop to detecting the voltage at VCC rise). If the period is not secured, the voltage cannot be detected correctly when VCC rises, and a power-on reset does not occur.

Voltage detection response delay time (delay time until it reacts after voltage detection).

Even if LVD is enabled, it will not function as an LVD immediately.
Td(E-A) Be sure to wait for the time before using the product.

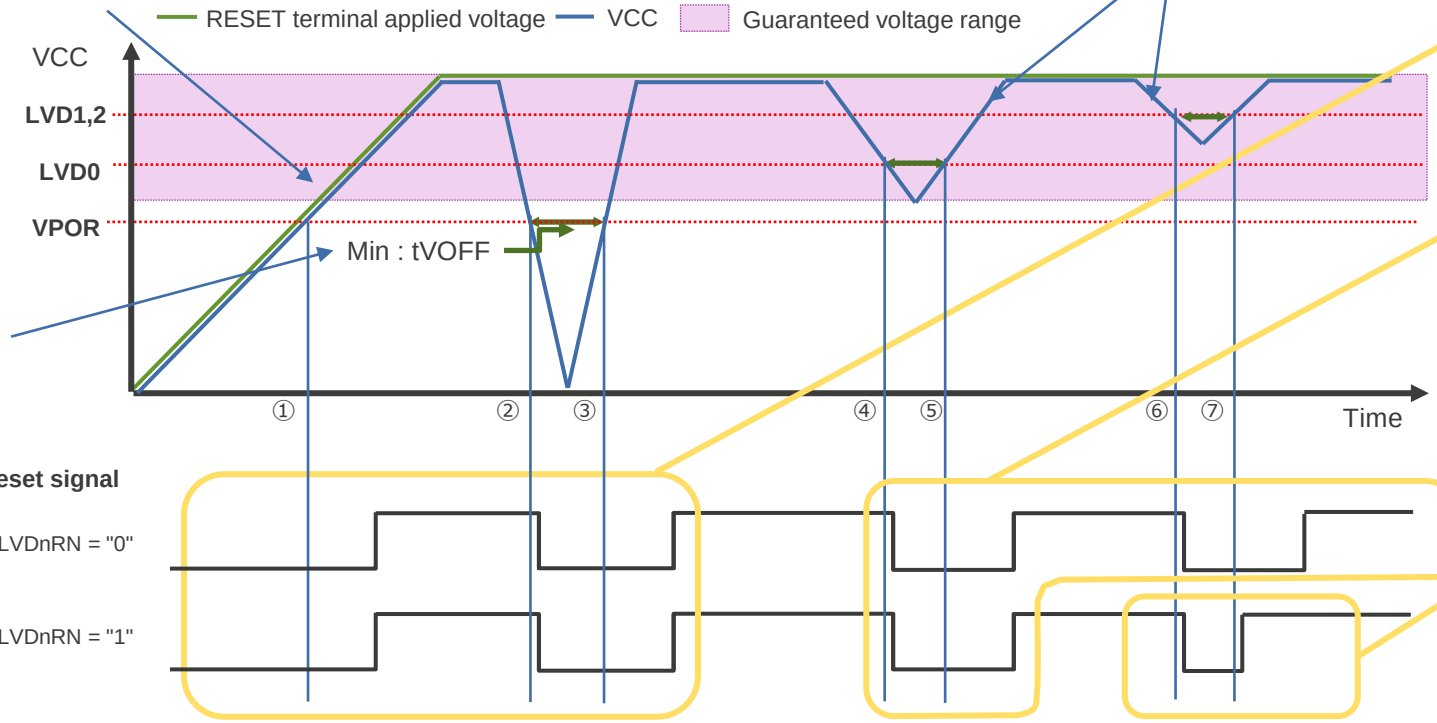
Voltage detection has hysteresis. Detecting deviation of TYP:80mV occurs.

# SUPPLEMENTARY INFORMATION : POWER-ON RESET CIRCUIT AND VOLTAGE DETECTION CIRCUIT CHARACTERISTICS

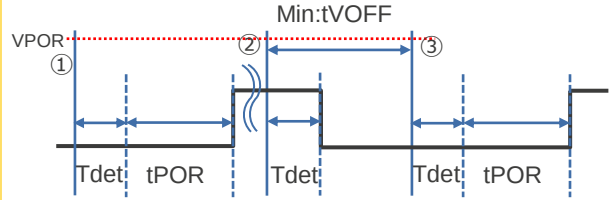
■ To enable POR, apply more than VCC*1 to RESET pin.
Note that if a capacitor is inserted to RESET pin to protect against noises, RESET pin rising potential will be slower than VCC rising potential, which means that the pin is judged to be a RESET pin reset, not a power-on reset.
*1 : VCC must comply with the following rising slope (SrVCC).
Example of RX66T case :
Power supply startup without LVD0 : (0.02ms/V) ≦ SrVCC ≦ (8ms/V)
Power supply startup with LVD0 : (0.02ms/V) ≦ SrVCC ≦ (20ms/V)

■ Dt/dVCC
Allowable rise/fall gradient for power supply fluctuation (fluctuation exceeding ±10%).
If the power supply suddenly **fluctuates more than 1ms/V**, it will not be covered by the warranty.
*The above is a sample RX66T. There are some products that have no default.

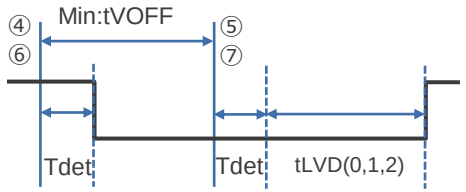
■ tVOFF
In order to reliably generate resetting, the potential must be lowered for more than tVOFF period.
If the VCC returns prior to tVOFF period, resetting cannot be issued correctly.



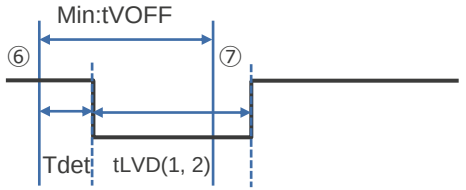

■ Internal-reset operation when POR is applied




■ Internal-reset operation by LVD0, 1, 2
(LVD1,2 is when LVDnCR0.LVDnRN = "0")




■ Internal-reset operation by LVD1, 2
(When LVDnCR0.LVDnRN = "1")




* LVD1 and 2 can be reset by setting LVDnCR0.LVDnRN = "1".

n : 1,2
NOTE :Various values in the statements and tables vary depending on the product. Refer to the electrical characteristics in the hardware manual of each product.

# AC CHARACTERISTICS : CLOCK TIMING

Since the BCLK pin is connected to the other device, please check the specifications of the other device before confirming this characteristic.

45.4.2 Clock Timing

**Table 45.18 BCLK Pin Output Clock Timing (1)**

Conditions: 4.5 V ≤ VCC ≤ 5.5 V, VCC_USB = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5V,
VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V,
$T_a = T_{opr}$

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| BCLK pin output cycle time | $t_{Bcyc}$ | 25 | — | — | ns | Figure 45.4 |
| BCLK pin output high pulse width | $t_{CH}$ | 7.5 | — | — | | |
| BCLK pin output low pulse width | $t_{CL}$ | 7.5 | — | — | | |
| BCLK pin output rising time | $t_{Cr}$ | — | — | 5 | | |
| BCLK pin output falling time | $t_{Cf}$ | — | — | 5 | | |

**Table 45.19 BCLK Pin Output Clock Timing (2)**

Conditions: 2.7 V ≤ VCC < 4.5 V, VCC_USB = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5V,
VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V,
$T_a = T_{opr}$

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| BCLK pin output cycle time | $t_{Bcyc}$ | 31.25 | — | — | ns | Figure 45.4 |
| BCLK pin output high pulse width | $t_{CH}$ | 10.625 | — | — | | |
| BCLK pin output low pulse width | $t_{CL}$ | 10.625 | — | — | | |
| BCLK pin output rising time | $t_{Cr}$ | — | — | 5 | | |
| BCLK pin output falling time | $t_{Cf}$ | — | — | 5 | | |

Required conditions to guarantee the following specifications.
In addition, there are cases where two types are listed for the same terminal output as shown in the two tables on the left. These are different conditions, so please confirm that you have met your usage conditions.

The $t_{CH}$ start and end points are VOH.

The $t_{Bcyc}$ start origin and end points are VCC median (0.5×VCC).

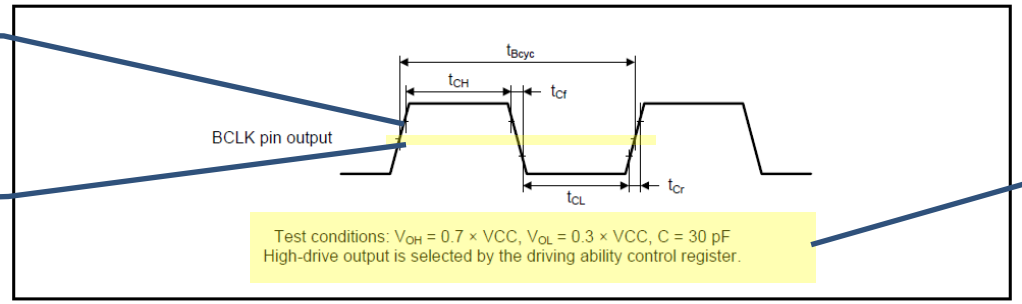



**Figure 45.4 BCLK Pin Output Timing**

The measurement conditions shown in the figure are also Required conditions to guarantee.

# AC CHARACTERISTICS : CLOCK TIMING

**Table 45.21 Main Clock Timing**

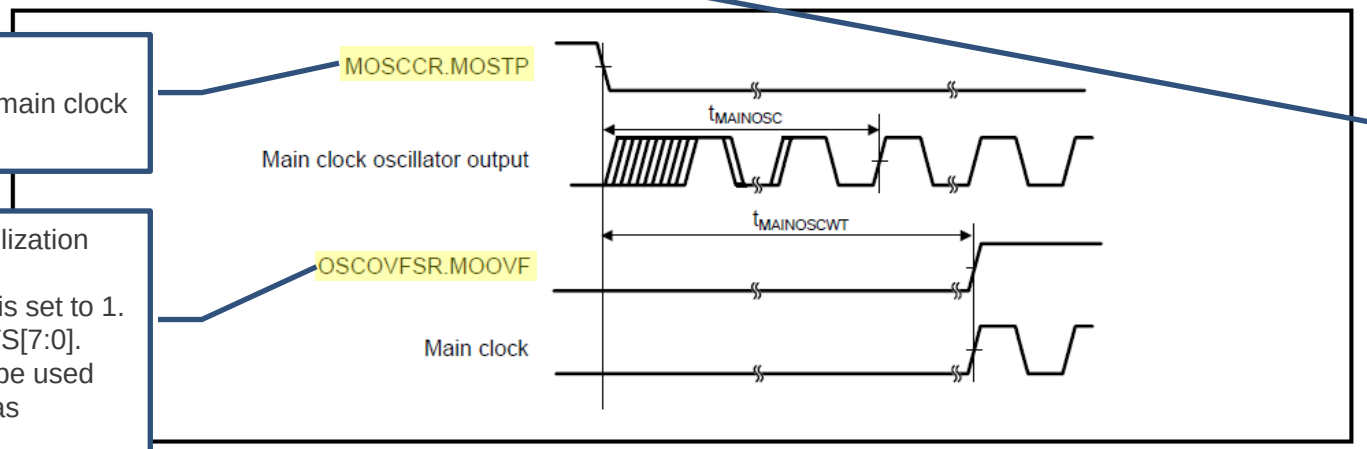
Conditions: VCC = 2.7 to 5.5 V, VCC_USB = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5V
VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V,
$T_a = T_{opr}$

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Main clock oscillation frequency | $f_{MAIN}$ | 8 | — | 24 | MHz | |
| Main clock oscillator stabilization time (crystal) | $t_{MAINOSC}$ | — | — | —*1 | ms | Figure 45.6 |
| Main clock oscillation stabilization wait time (crystal) | $t_{MAINOSCWT}$ | — | — | —*2 | | |

Note 1. When using a main clock, ask the manufacturer of the oscillator to evaluate its oscillation. Refer to the results of evaluation provided by the manufacturer for the oscillation stabilization time.

Note 2. The number of cycles selected by the value of the MOSCWTCR.MSTS[7:0] bits determines the main clock oscillation stabilization wait time in accord with the formula below.

$t_{MAINOSCWT}$ = [(MSTS[7:0] bits × 32) + 7] / $f_{LOCO}$




**Main Clock Oscillation Start Timing**

This is the time until the oscillation of the resonator stabilizes. This value follows the matching evaluation by the resonator manufacturer.

Time required to further stabilize the internal circuit after the external resonator has stabilized.

This bit stops the main clock oscillator.
Setting this bit to "0" starts output of the main clock oscillator.

This bit is the main clock oscillation stabilization flag.
After a lapse of $t_{MAINOSCWT}$ time, this flag is set to 1.
This flag depends on MOSCWTCR.MSTS[7:0].
When the setting value is correct, it can be used as a flag to indicate that the resonator has stabilized.

Required conditions to guarantee the following specifications.

The clock oscillation stabilization time and clock oscillation stabilization wait time are indicated by the microcontroller. These values are for reference only.

MOSCWTCR.MSTS[7:0] must be higher $t_{MAINOSC}$.
The formulas are described in MOSCWTCR section of the clock-generator.

Please consider the $f_{LOCO}$ in terms of specifications on the MAX side. For more information, see MOSCWTCR register section.

# AC CHARACTERISTICS : LOCO, IWDT CLOCK TIMING

**Table 45.22 LOCO and IWDT-Dedicated Low-Speed Clock Timing**

Conditions: VCC = 2.7 to 5.5 V, VCC_USB = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5V, VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V, $T_a = T_{opr}$

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| LOCO clock cycle time | $t_{Lcyc}$ | 3.78 | 4.16 | 4.63 | µs | |
| LOCO clock oscillation frequency | $f_{LOCO}$ | 216 | 240 | 264 | kHz | |
| LOCO clock oscillation stabilization time | $t_{LOCOWT}$ | — | — | 44 | µs | Figure 45.7 |
| IWDT-dedicated low-speed clock cycle time | $t_{ILcyc}$ | 7.57 | 8.33 | 9.26 | | |
| IWDT-dedicated low-speed clock oscillation frequency | $f_{ILOCO}$ | 108 | 120 | 132 | kHz | |
| IWDT-dedicated low-speed clock oscillation stabilization wait time | $t_{ILOCOWT}$ | — | 142 | 190 | µs | Figure 45.8 |

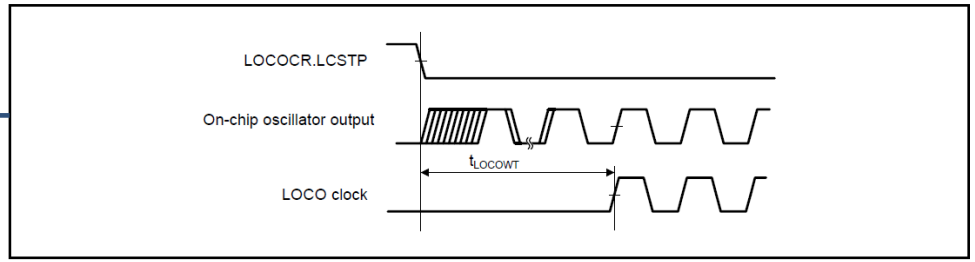



**Figure 45.7 LOCO Clock Oscillation Start Timing**

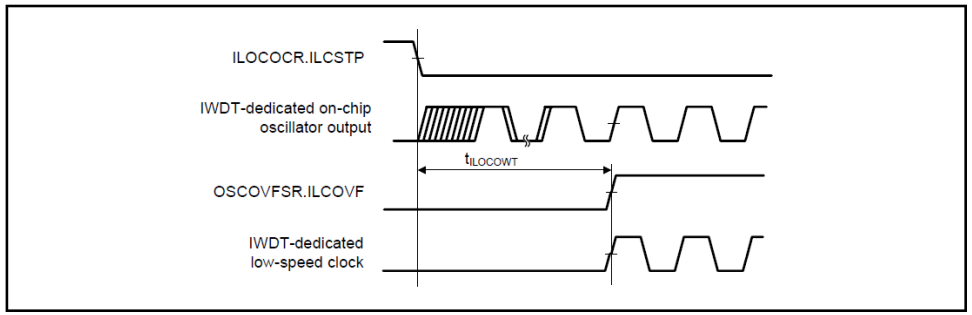



**Figure 45.8 IWDT-dedicated Low-Speed Clock Oscillation Start Timing**

Required conditions to guarantee the following specifications.

One-cycle period of LOCO. Calculated from the oscillator frequency of LOCO.
Ex.) TYP : 4.16us = 1/240KHz

Oscillating frequency error of LOCO is shown. Accuracy can be calculated from this value.
Negative side:-10%=(216-240)/240
Positive side: +10%=(264-240)/240

It takes time to stabilize the oscillation after LOCO is oscillated (LOCOCR.LCSTP=0).
Max. 44us is applied under the conditions in this table.

One-cycle time (cycle) of IWDT dedicated on-chip oscillator. Calculated from the oscillator frequency of IWDT dedicated on-chip oscillator.
Ex.) TYP : 8.33us = 1/140KHz

The oscillation frequency error of IWDT dedicated on-chip oscillator is shown. Accuracy can be calculated from this value.
Negative side:-10%=(108-120)/120
Positive side: +10%=(264-240)/240

It takes time for oscillation to stabilize after IWDT dedicated on-chip oscillator is oscillated (ILOCOCR.ILCSTP=0).
Max. 190us is applied under the conditions in this table.

# AC CHARACTERISTICS : HOCO CLOCK TIMING

HOCO oscillator frequency can be selected from several options. For this device, the oscillator frequency of 16/18/20MHz can be selected. This table also shows the errors at each oscillation frequency.
In addition, note that the measurement conditions have temperature characteristics. The accuracy according to this value is as follows.

| Oscillation frequency (MHz) | Error (Ta = -20~105℃) | Error (Ta = -40~-20℃) |
|---|---|---|
| 16 | ±2.4375% | ±3% |
| 18 | ±2.44% | ±3% |
| 20 | ±2.4 | ±3% |

It takes time for the operation to stabilize after power is supplied to HOCO. When changing HOCO power supply to OFF→ON, make sure that HOCO oscillates (HOCOCR.HCSTP=0) after the power supply stabilization period has elapsed. After resetting, the power is supplied (HOCOPCR.HOCOPCNT=0).

**Table 45.23 HOCO Clock Timing**

Conditions: VCC = 2.7 to 5.5 V, VCC_USB = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5V,
VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V,
$T_a = T_{opr}$

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| HOCO clock oscillation frequency | $f_{HOCO}$ | 15.61 | 16 | 16.39 | MHz | −20°C ≤ $T_a$ ≤ 105°C |
| | | 17.56 | 18 | 18.44 | | |
| | | 19.52 | 20 | 20.48 | | |
| | | 15.52 | 16 | 16.48 | | −40°C ≤ $T_a$ < −20°C |
| | | 17.46 | 18 | 18.54 | | |
| | | 19.40 | 20 | 20.60 | | |
| HOCO clock oscillation stabilization wait time | $t_{HOCOWT}$ | — | 105 | 149 | μs | Figure 45.9 |
| HOCO clock power supply stabilization time | $t_{HOCOP}$ | — | — | 150 | | Figure 45.10 |

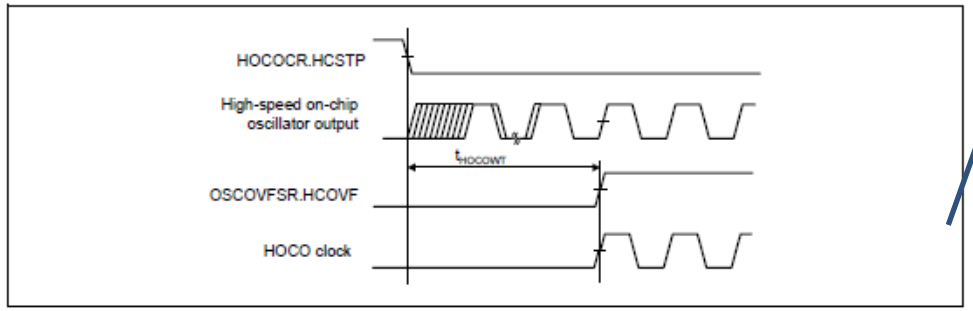



**Figure 45.9 HOCO Clock Oscillation Start Timing (Oscillation is Started by Setting the HOCOCR.HCSTP Bit)**

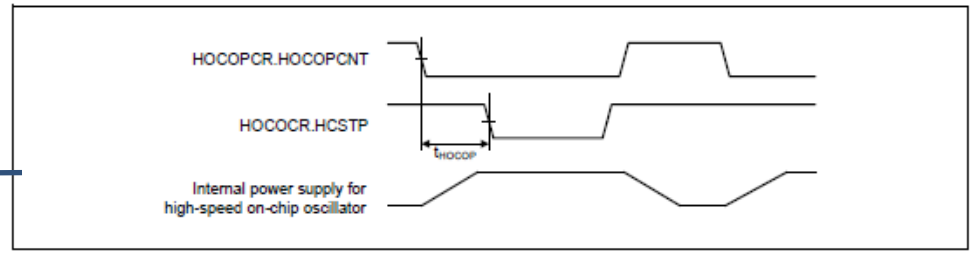



**Figure 45.10 High-Speed On-Chip Oscillator Power Supply Control Timing**

Required conditions to guarantee the following specifications.

It takes time to stabilize the oscillation after HOCO is oscillated (HOCOCR.HCSTP=0).
Max. 149us is applied under the conditions in this table.

# AC CHARACTERISTICS : PLL CLOCK TIMING

The output clock frequency range of the PLL frequency synthesizer.
Note that this is not the operation clock. In addition, please note that the input frequency range of the PLL frequency synthesizer is determined by the product[NOTE].

NOTE : Refer to the Clock Generation Circuit section in the User's Manual Hardware.

It takes time to stabilize the oscillation after PLL is oscillated (PLLCR2.PLLEN=0).
Max. 320us is applied under the conditions in this table.

**Table 45.24 PLL Clock Timing**

Conditions: VCC = 2.7 to 5.5 V, VCC_USB = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5V,
VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V,
$T_a = T_{opr}$

Required conditions to guarantee the following specifications.

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| PLL clock oscillation frequency | $f_{PLL}$ | 120 | — | 240 | MHz | |
| PLL clock oscillation stabilization wait time | $t_{PLLWT}$ | — | 259 | 320 | µs | Figure 45.11 |

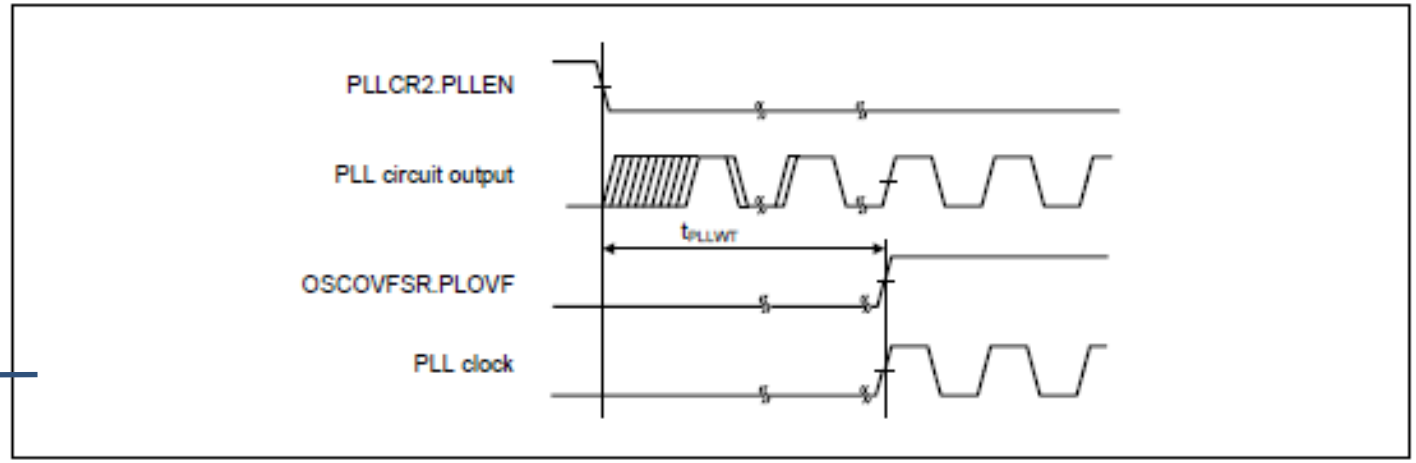



**Figure 45.11 PLL Clock Oscillation Start Timing**

# AC CHARACTERISTICS :
# TIMING OF RECOVERY FROM LOW POWER CONSUMPTION MODE

45.4.3 Timing of Recovery from Low Power Consumption Modes

**Table 45.25 Timing of Recovery from Low Power Consumption Modes (1)**

Conditions: VCC = 2.7 to 5.5 V, VCC_USB = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5 V
VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V,
$T_a = T_{opr}$

| Item | | | Symbol | Min. | Typ. | Max. $t_{SBYOSCWT}$*2 | Max. $t_{SBYSEQ}$*3 | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|---|---|
| Recovery time after cancellation of software standby mode*1 | Crystal resonator connected to main clock oscillator | Main clock oscillator operating | $t_{SBYMC}$ | — | — | {(MSTS[7:0] bits × 32) + 76} / 0.216 | 100 + 7 / $f_{ICLK}$ + 2n / $f_{MAIN}$ | μs | Figure 45.12 |
| | | Main clock oscillator and PLL circuit operating | $t_{SBYPC}$ | | | {(MSTS[7:0] bits × 32) + 138} / 0.216 | 100 + 7 / $f_{ICLK}$ + 2n / $f_{PLL}$ | | |
| | External clock input to main clock oscillator | Main clock oscillator operating | $t_{SBYEX}$ | | | 352 | 100 + 7 / $f_{ICLK}$ + 2n / $f_{EXMAIN}$ | | |
| | | Main clock oscillator and PLL circuit operating | $t_{SBYPE}$ | | | 639 | 100 + 7 / $f_{ICLK}$ + 2n / $f_{PLL}$ | | |
| | High-speed on-chip oscillator operating | High-speed on-chip oscillator operating | $t_{SBYHO}$ | | | 454 | 100 + 7 / $f_{ICLK}$ + 2n / $f_{HOCO}$ | | |
| | | High-speed on-chip oscillator operating and PLL circuit operating | $t_{SBYFH}$ | | | 741 | 100 + 7 / $f_{ICLK}$ + 2n / $f_{PLL}$ | | |
| | Low-speed on-chip oscillator operating*4 | | $t_{SBYLO}$ | | | 338 | 100 + 7 / $f_{ICLK}$ + 2n / $f_{LOCO}$ | | |

Note 1. The time for return after release from software standby is determined by the value obtained by adding the oscillation stabilization waiting time ($t_{SBYOSCWT}$) and the time required for operations by the software standby release sequencer ($t_{SBYSEQ}$).
Note 2. When several oscillators were running before the transition to software standby, the greatest value of the oscillation stabilization waiting time $t_{SBYOSCWT}$ is selected.
Note 3. For n, the greatest value is selected from among the internal clock division settings.
Note 4. This condition applies when $f_{ICLK} : f_{FCLK}$ = 1 : 1, 2 : 1, or 4 : 1.

Required conditions to guarantee the following specifications.

Please calculate the recovery time by entering the required parameter values according to your usage conditions.

# AC CHARACTERISTICS : CONTROL SIGNAL TIMING

## 45.4.4 Control Signal Timing

**Table 45.27 Control Signal Timing**

Conditions: VCC = 2.7 to 5.5 V, VCC_USB = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5V,
VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V,
$T_a = T_{opr}$

| Item | Symbol | Min.*1 | Typ. | Max. | Unit | Test Conditions*1 |
|---|---|---|---|---|---|---|
| NMI pulse width | $t_{NMIW}$ | 200 | — | — | ns | $2 \times t_{PBcyc} \leq 200$ ns, Figure 45.14 |
| | | $2 \times t_{PBcyc}$ | — | — | | $2 \times t_{PBcyc} > 200$ ns, Figure 45.14 |
| IRQ pulse width | $t_{IRQW}$ | 200 | — | — | | $2 \times t_{PBcyc} \leq 200$ ns, Figure 45.15 |
| | | $2 \times t_{PBcyc}$ | — | — | | $2 \times t_{PBcyc} > 200$ ns, Figure 45.15 |

Note 1. $t_{PBcyc}$: PCLKB cycle

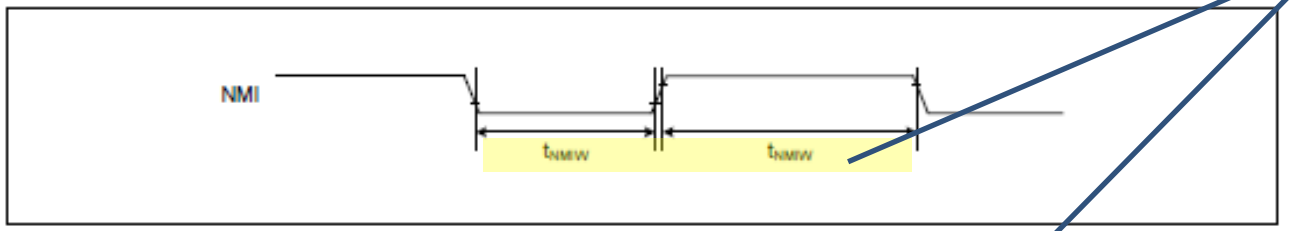



**Figure 45.14 NMI Interrupt Input Timing**

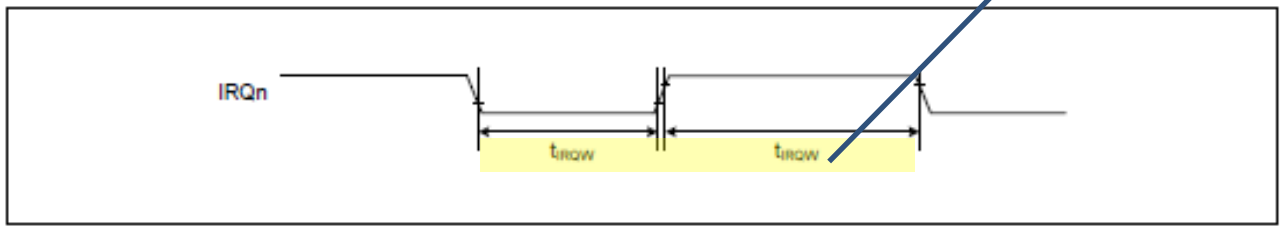



**Figure 45.15 IRQ Interrupt Input Timing**

Please note that depending on the clock frequency used, the min of the pulse width will change.

Both level detection and edge detection must satisfy this condition.

# AC CHARACTERISTICS : BUS TIMING

## 45.4.5 Bus Timing

Required conditions to guarantee the following specifications.
Pay special attention when selecting the output load conditions and drive capability. If the normal drive output is selected for bus driving, the timing may not be long enough and access may not be performed correctly.

**Table 45.28 Bus Timing (1)**

Conditions: 4.5 V ≤ VCC ≤ 5.5 V, VCC_USB = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5V,
VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V, $T_a = T_{opr}$,
ICLK = 8 to 160 MHz, PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, PCLKC = 8 to 160 MHz, BCLK = 8 to 60 MHz,
Output load conditions: $V_{OH}$ = 0.5 × VCC, $V_{OL}$ = 0.5 × VCC, C = 30 pF,
High-drive output is selected by the driving ability control register (other than for P53 to P55 and P60 to P65).

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Address delay time | $t_{AD}$ | — | — | 12.5 | ns | Figure 45.16 to Figure 45.21 |
| Byte control delay time | $t_{BCD}$ | — | — | 12.5 | | |
| CS# delay time | $t_{CSD}$ | — | — | 12.5 | | |
| ALE delay time | $t_{ALED}$ | — | — | 12.5 | | |
| RD# delay time | $t_{RSD}$ | — | — | 12.5 | | |
| Read data setup time | $t_{RDS}$ | 12.5 | — | — | | |
| Read data hold time | $t_{RDH}$ | 0 | — | — | | |
| WR# delay time | $t_{WRD}$ | — | — | 12.5 | | |
| Write data delay time | $t_{WDD}$ | — | — | 12.5 | | |
| Write data hold time | $t_{WDH}$ | 0 | — | — | | |
| WAIT# setup time | $t_{WTS}$ | 12.5 | — | — | | Figure 45.22 |
| WAIT# hold time | $t_{WTH}$ | 0 | — | — | | |

As for this value, it does not become 0 or less.

# AC CHARACTERISTICS : EXTERNAL BUS READ/WRITE TIMING

In 1-write strobe mode, the WR# signal is always asserted at the write timing, and the corresponding BCn# signal is asserted at the same time.
In the byte strobe mode, the BCn# signal is invalid.

In byte strobe mode, the corresponding WRn#(0~3) signal is asserted at the write timing.
In 1-write strobe mode, everything except WR0# is invalid.

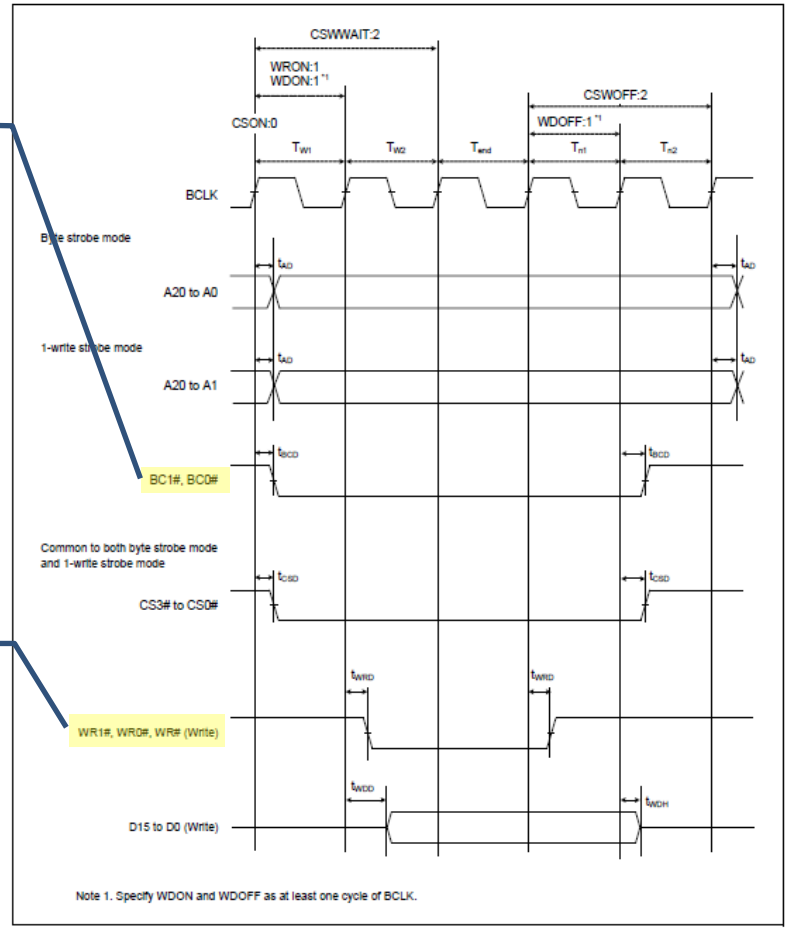



Figure 45.19 External Bus Timing/Normal Write Cycle (Bus Clock Synchronized)

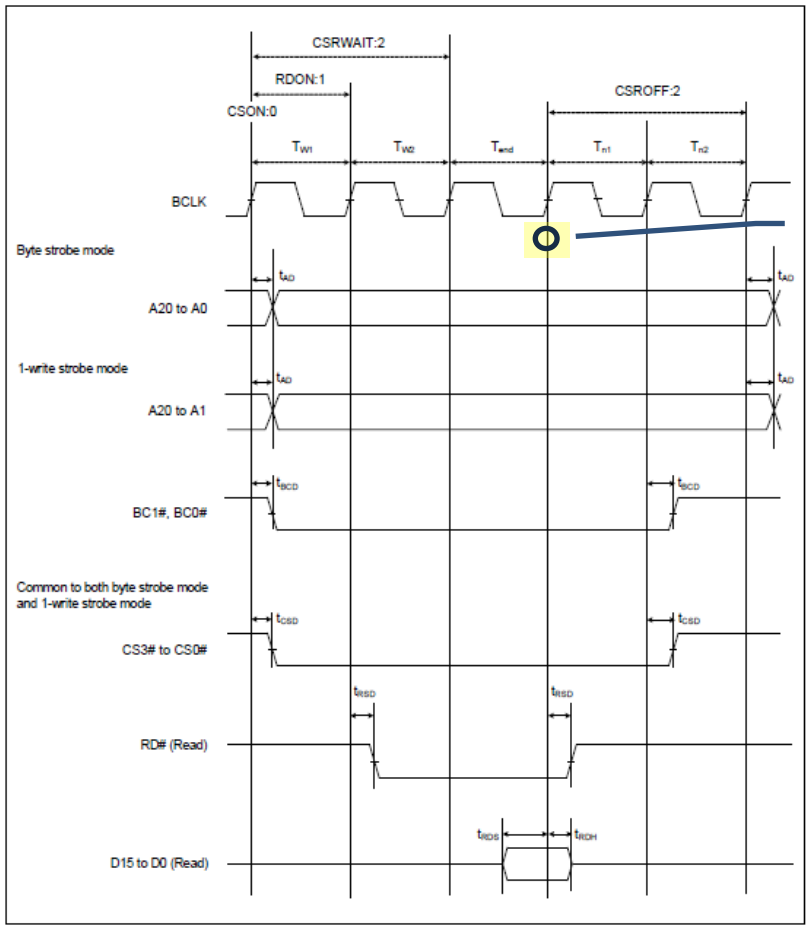



Figure 45.18 External Bus Timing/Normal Read Cycle (Bus Clock Synchronized)

Read timing is the rising edge of BCLK's Tend. (When BCLK terminal = Internal BCLK)

# AC CHARACTERISTICS : ADDRESS/DATA MULTIPLEX TIMING

A0~A15 is output from the address bus/data bus (A0/D0~A15/D15). After A16, it is output from the address bus of Axx.

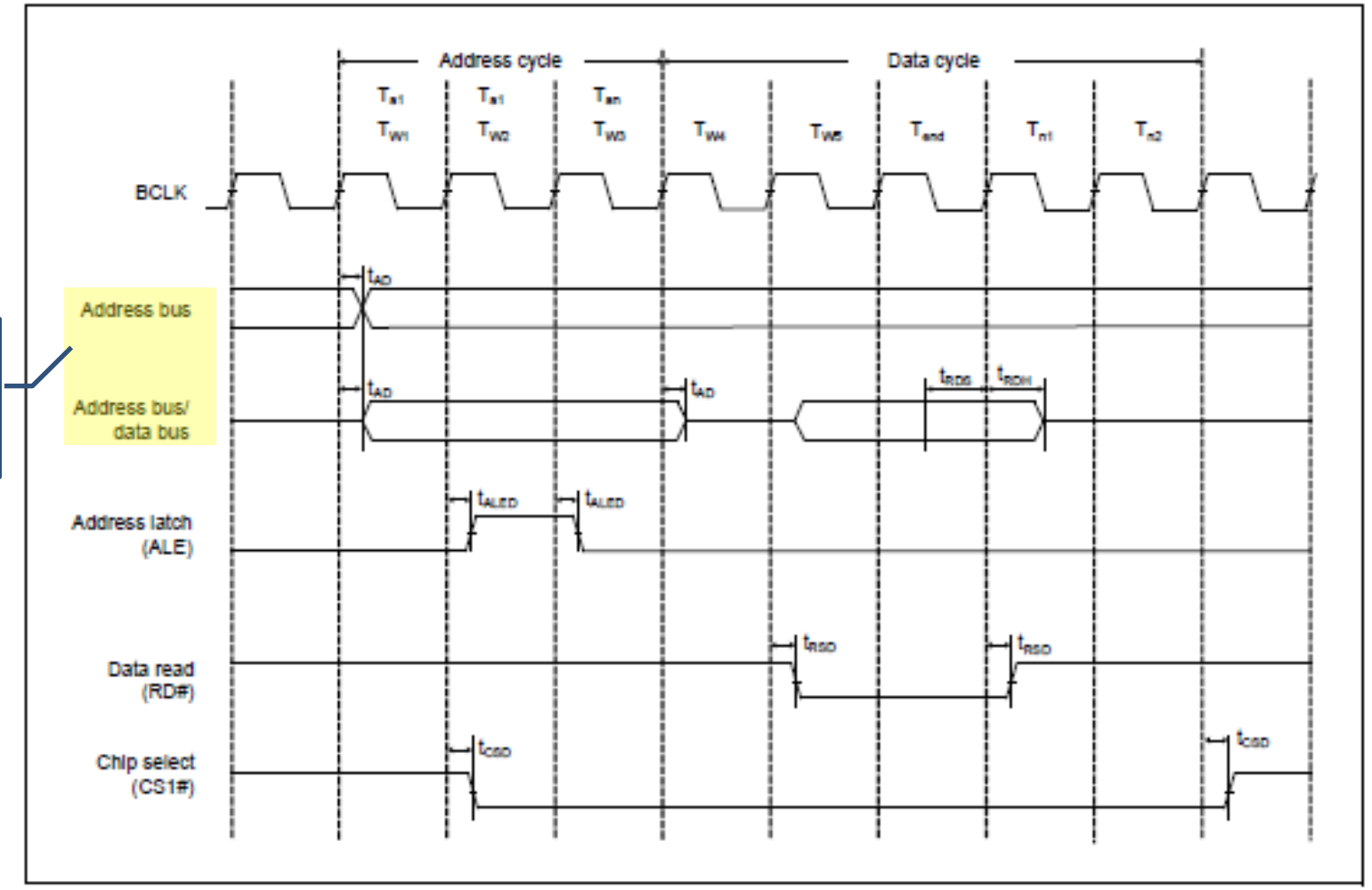



Figure 45.16 Address/Data Multiplexed Bus Read Access Timing

# AC CHARACTERISTICS :
# NOTE WHEN BCLK PIN IS SET TO 1/2 OF THE INTERNAL BCLK

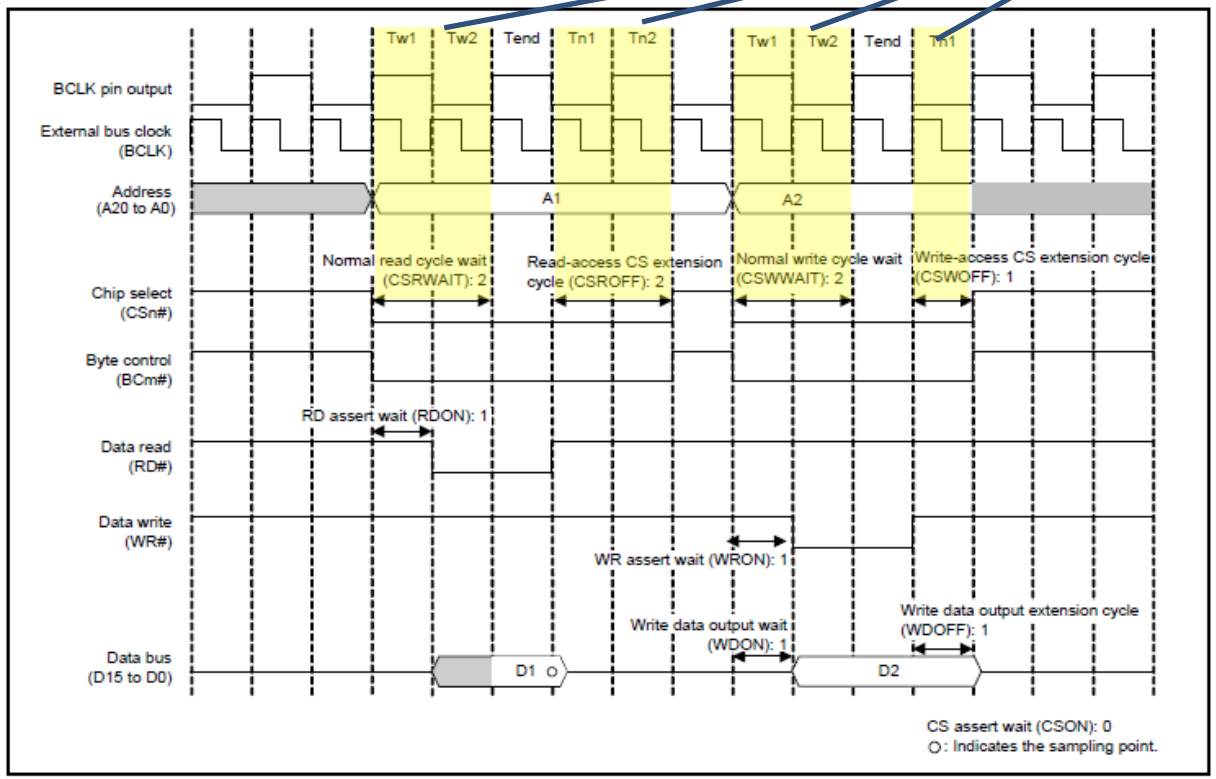



**Figure 15.15 Example of Normal Access (when 1/2 BCLK is Selected with the BCLK Pin Output Select Bit) (n = 0 to 3, m = 0, 1)**

WAIT cycling is inserted synchronously with the inner BCLK. When BCLK pin output is set to 1/2 of the internal BCLK clock, note that the assertion/negation timing of the control signals may change not only at the rising timing but also at the falling timing of the BCLK pin depending on the number of WAITs set.

# AC CHARACTERISTICS : I/O PORT TIMING

### 45.4.6.1 I/O Port

**Table 45.30 I/O Port Timing**

Conditions: VCC = 2.7 to 5.5 V, VCC_USB = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5V,
VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V, $T_a = T_{opr}$,
ICLK = 8 to 160 MHz, PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, PCLKC = 8 to 160 MHz, BCLK = 8 to 60 MHz,
Output load conditions: $V_{OH}$ = 0.5 × VCC, $V_{OL}$ = 0.5 × VCC, C = 30 pF,
High-drive output is selected by the driving ability control register (other than for P53 to P55 and P60 to P65).

| Item | | Symbol | Min. | Max. | Unit*1 | Test Conditions |
|---|---|---|---|---|---|---|
| I/O ports | Input data pulse width | $t_{PRW}$ | 1.5 | — | $t_{PBcyc}$ | Figure 45.23 |

Note 1. $t_{PBcyc}$: PCLKB cycle

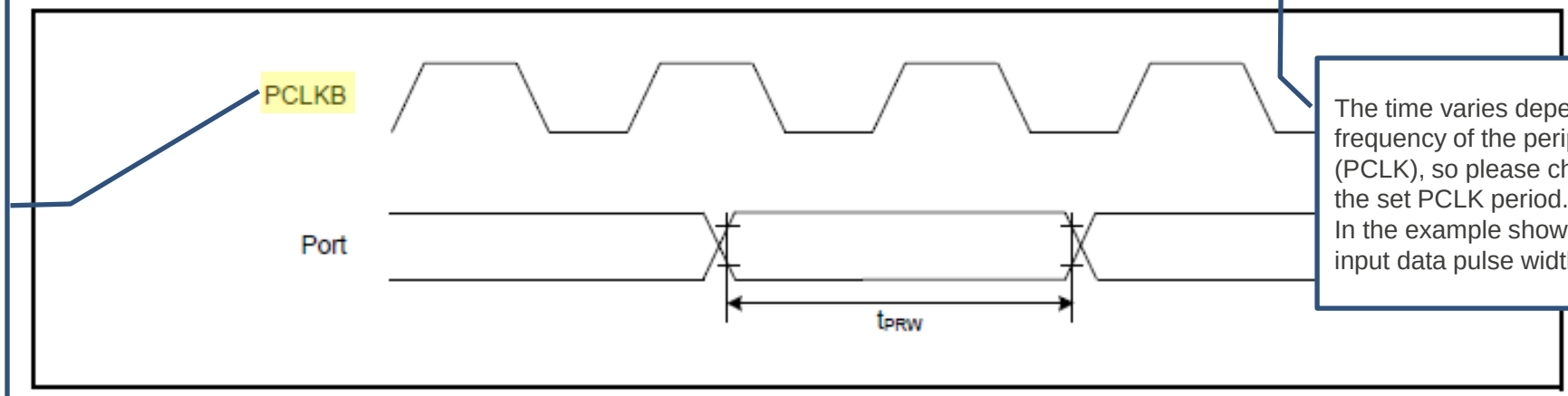
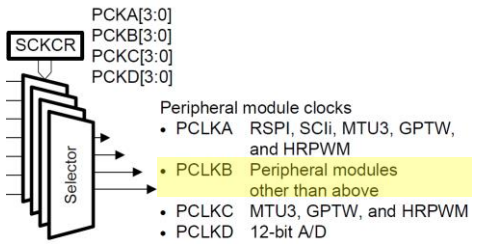



**Figure 45.23 I/O Port Input Timing**

The reference clock is the peripheral module clock supplied to I/O port. Check in the Clock Generation Circuit chapter.
In the following example, it is an PCLKB.




The time varies depending on the frequency of the peripheral module clock (PCLK), so please check it together with the set PCLK period.
In the example shown, $t_{PBcyc}$ x 1.5 is the input data pulse width.

# AC CHARACTERISTICS : MTU

The MTIOCnm pin (n=0~4,6,7,9, m=A~D) and the MTIC5m pin (m=U,V,W) and the internal clock of the input capture pin are asynchronous. Therefore, the input capture input pulse width must be at least 1.5 PCLKC wide on a single edge and 2.5 PCLKC on both edges.

Input timing of external clock pins and external clock pins in phase coefficient mode.
Note that High width /Low width is specified.

Required conditions to guarantee the following specifications.
Clock and output load conditions in particular are greatly affected by clock timing.

**Table 45.32 MTU Timing**

Conditions: VCC = 2.7 to 5.5 V, VCC_USB = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5V,
VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V, $T_a = T_{opr}$,
ICLK = 8 to 160 MHz, PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, PCLKC = 8 to 160 MHz, BCLK = 8 to 60 MHz,
Output load conditions: $V_{OH}$ = 0.5 × VCC, $V_{OL}$ = 0.5 × VCC, C = 30 pF,
High-drive output is selected by the driving ability control register (other than for P53 to P55 and P60 to P65).

| Item | | | Symbol | Min. | Max. | Unit*1 | Test Conditions |
|---|---|---|---|---|---|---|---|
| MTU | Input capture input pulse width | Single-edge setting | $t_{MTICW}$ | 1.5 | — | $t_{PCcyc}$ | Figure 45.25 |
| | | Both-edge setting | | 2.5 | — | | |
| | Timer clock pulse width | Single-edge setting | $t_{MTCKWH}$, $t_{MTCKWL}$ | 1.5 | — | $t_{PCcyc}$ | Figure 45.26 |
| | | Both-edge setting | | 2.5 | — | | |
| | | Phase counting mode | | 2.5 | — | | |

Note 1. $t_{PCcyc}$: PCLKC cycle

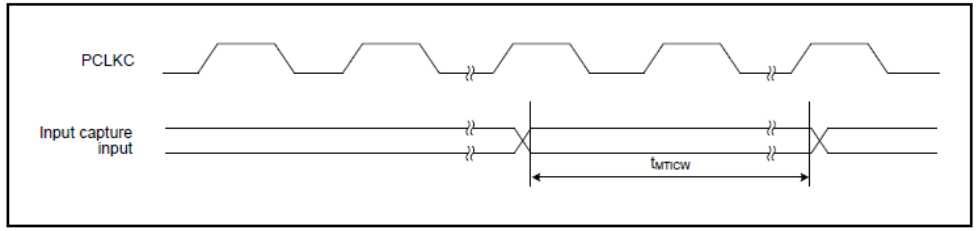



**Figure 45.25 MTU Input Capture Input Timing**

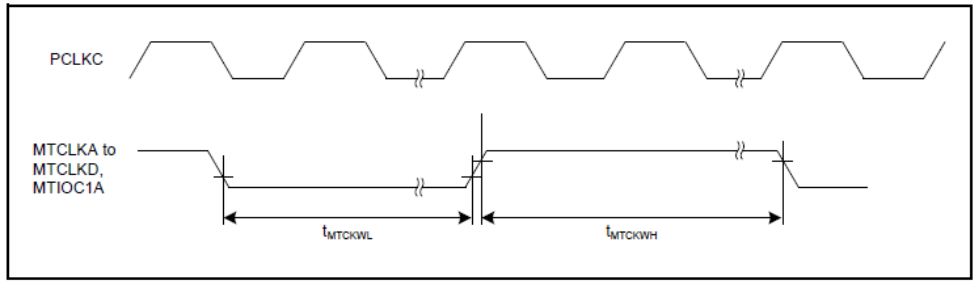



**Figure 45.26 MTU Clock Input Timing**

# AC CHARACTERISTICS : POE, POEG

**Table 45.33 POE Timing**

Conditions: VCC = 2.7 to 5.5 V, VCC_USB = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5V,
VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V, $T_a = T_{opr}$,
ICLK = 8 to 160 MHz, PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, PCLKC = 8 to 160 MHz, BCLK = 8 to 60 MHz,
Output load conditions: $V_{OH}$ = 0.5 × VCC, $V_{OL}$ = 0.5 × VCC, C = 30 pF,
High-drive output is selected by the driving ability control register (other than for P53 to P55 and P60 to P65).

| Item | | | Symbol | Min. | Typ. | Max. | Unit*1 | Test Conditions |
|---|---|---|---|---|---|---|---|---|
| POE | POEn# input pulse width (n = 0, 4, and 8 to 14) | | $t_{POEW}$ | 1.5 | — | — | $t_{PBcyc}$ | Figure 45.27 |
| | Output disable time | Transition of the POEn# signal level | $t_{POEDI}$ | — | — | 5 PCLKB + 0.24 | µs | Figure 45.28<br>When detecting falling edges (ICSRm.POEnM[3:0] = 0000b (m = 1 to 5, 7 to 9, n = 0, 4, 8 to 14)) |
| | | Simultaneous conduction of output pins | $t_{POEDO}$ | — | — | 3 PCLKB + 0.2 | µs | Figure 45.29 |
| | | Detection of comparator outputs | $t_{POEDC}$ | — | — | 5 PCLKB + 0.2 | µs | Figure 45.30<br>The time is that when the noise filter for comparator C is not in use (CMPCTL.CDFS[1:0] = 00b) and excludes the time for detection by comparator C. |
| | | Register setting | $t_{POEDS}$ | — | — | 1 PCLKB + 0.2 | µs | Figure 45.31<br>Time for access to the register is not included. |
| | | Oscillation stop detection | $t_{POEDOS}$ | — | — | 21 | µs | Figure 45.32 |
| POEG | GTETRGn input pulse width (n = A to D) | | $t_{POEGW}$ | 1.5 | — | — | $t_{PBcyc}$ | Figure 45.33 |
| | Output disable time | Input level detection of the GTETRGn pin (via flag) | $t_{POEGDI}$ | — | — | 3 PCLKB + 0.34 | µs | Figure 45.34<br>When the digital noise filter is not in use (POEGGn.NFEN = 0 (n = A to D)) |
| | | Detection of the output stopping signal from GPTW (deadtime error, simultaneous high output, or simultaneous low output) | $t_{POEGDE}$ | — | — | 0.5 | µs | Figure 45.35 |
| | | Edge detection signal from a comparator | $t_{POEGDC}$ | — | — | 4 PCLKB + 0.5 | µs | Figure 45.36<br>The time is that when the noise filter for comparator C is not in use (CMPCTL.CDFS[1:0] = 00b) and excludes the time for detection by comparator C. |
| | | Register setting | $t_{POEGDS}$ | — | — | 1 PCLKB + 0.3 | µs | Figure 45.37<br>Time for access to the register is not included. |
| | | Oscillation stop detection | $t_{POEGDOS}$ | — | — | 21 | µs | Figure 45.38 |
| | | Input level detection of the GTETRGn pin (direct path) | $t_{POEGDDI}$ | — | — | 2 PCLKB + 1 PCLKC + 0.34 | µs | Figure 45.39 |
| | | Level detection signal from a comparator | $t_{POEGDDC}$ | — | — | 3 PCLKB + 0.3 | µs | Figure 45.40<br>The time is that when the noise filter for comparator C is not in use (CMPCTL.CDFS[1:0] = 00b) and excludes the time for detection by comparator C. |

Note 1. $t_{PBcyc}$: PCLKB cycle

Required conditions to guarantee the following specifications.
Clock and output load conditions, in particular, are greatly affected by timing.

This is a rules for POE3 (Port Output Enable 3) module.
The control target pins of POE3 are PWM output pins of MTU3 and PWM output pins of GPTW.

This is a rules for POEG (GPTW Port Output Enable) modules.
POEG control target terminal is PWM output terminal of GPTW. Note that MTU3's PWM out terminal is not included.

Please note that POE(MTU3/GPTW port output enable and POEG(GPTW port output enable differ in their specifications. They differ according to the electrical characteristics. Therefore, the timing of reflection is different.

# AC CHARACTERISTICS : POE, POEG TIMING (TRIGGER PIN INPUT)

- External trigger pin input (Specified pulse width)

Trigger terminal input pulse width (POE3: POEn#, POEG:GTETRGn) of POE3, POEG module. Both are asynchronous to the internal clocks, so the input-pulse width requires a 1.5PCLKB width at a minimum.

POE3

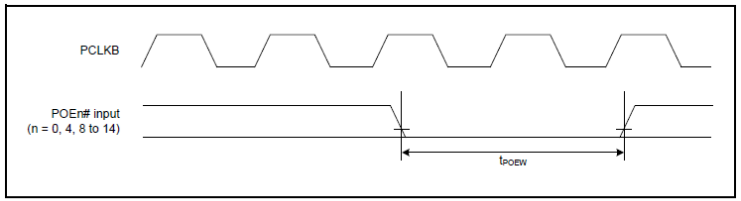



Figure 45.27 POE Input Timing

POEG

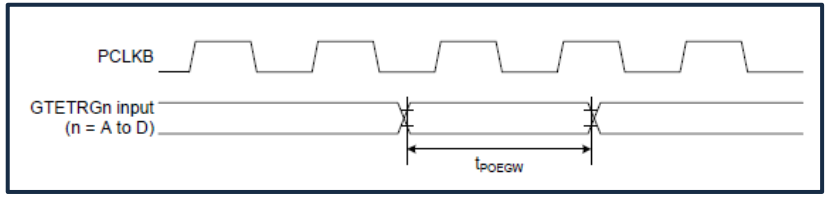



Figure 45.33 POEG Input Timing

- External trigger pin input (Stop time)

In the case of POE3, this is the time from the input of POE# to the time when the output stop of the following target PWM output pins.
In the case of POEG, this is the time from the input of GTETRGn to the time when the output stop of the following target PWM output pins.

- Target PWM Output port
  POE3 : PWM output port of MTU3/GPTW
  POEG : PWM output port of GPTW

The POE3 waveform on the right shows the timing diagram at the time of edge detection. The POEG waveform shows a timing diagram in case of the noise filter is not used and “via flag”/”direct path”.
In addition, the level detection stops the output of the target PWM output terminal after the sampling count set by ICSRm.POEnM2[3:0] for POE3 or OEGGn.NFCS[1:0] for POEG has been met and the time to stop output as shown in the right figure has elapsed.

POE3

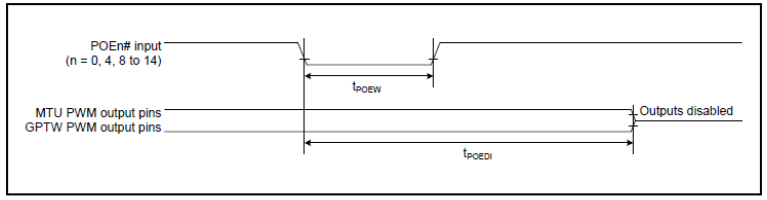



Figure 45.28 Output Disable Time for POE in Response to Transition of the POEn# Signal Level

POEG

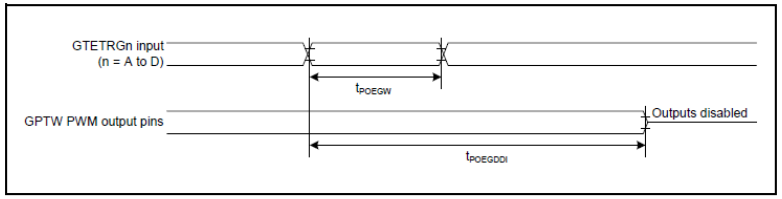



Figure 45.39 Output Disable Time for POEG in Direct Response to the Input Level Detection of the GTETRGn pin

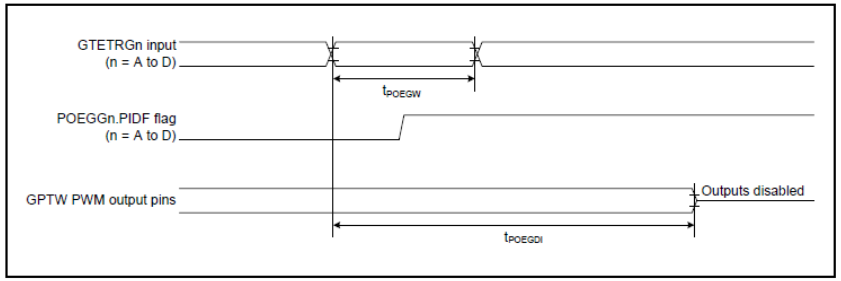



Figure 45.34 Output Disable Time for POEG via Detection Flag in Response to the Input Level Detection of the GTETRGn pin

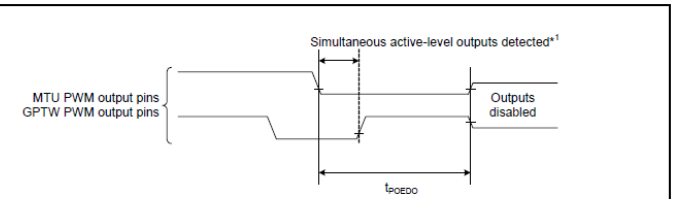
# AC CHARACTERISTICS : POE, POEG TIMING (PWM OUTPUT SHORT-CIRCUIT, OSCILLATION STOPPED)

## ■ PWM output-short circuit

When the short-circuit of PWM output signal (positive and negative phases are active at the same time) continues for longer than 1PCLK, the following target PWM output pins stop output.

- Target PWM Output port
  POE3 : PWM output port of MTU3/GPTW
  POEG : PWM output port of GPTW

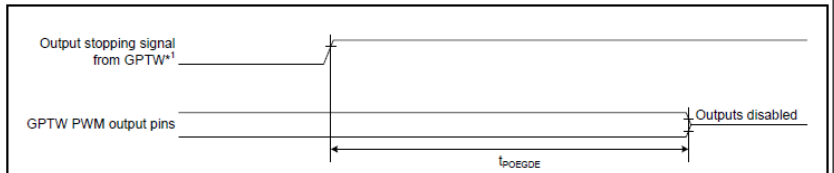
POE3




Note 1. When the active level is set to low.

Figure 45.29 Output Disable Time for POE in Response to the Simultaneous Conduction of Output Pins

POEG




Note 1. GPTWn.GTST.DTEF (dead time error flag), GPTWn.GTST.OABLF (simultaneous low output flag), or GPTWn.GTST.OABHF (simultaneous high output flag)

Figure 45.35 Output Disable Time for POEG in Response to Detection of the Output Stopping Signal from GPTW

## ■ Stop oscillation

This is the time until the target PWM output pins listed below stop outputting when an oscillation stop detection signal is input to the POE3 or POEG module.

- Target PWM Output port
  POE3 : PWM output port of MTU3/GPTW
  POEG : PWM output port of GPTW

POE3

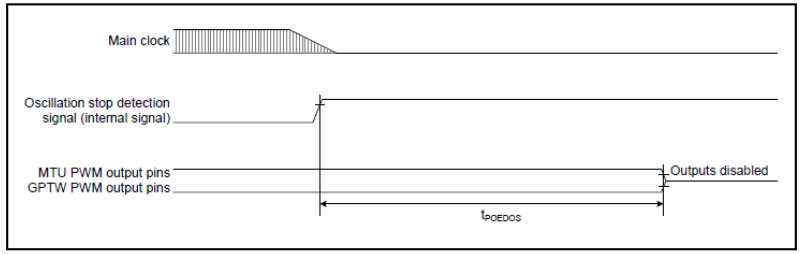



Figure 45.32 Output Disable Time for POE in Response to the Oscillation Stop Detection

POEG

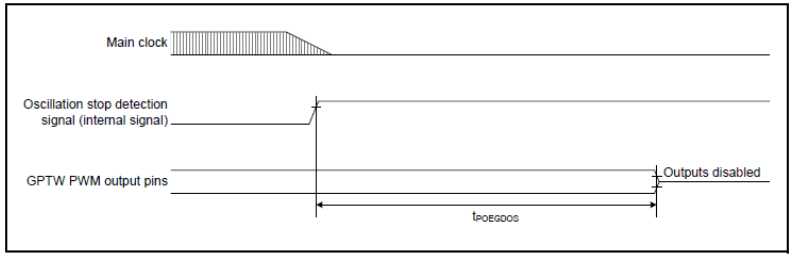



Figure 45.38 Output Disable Time of POEG in Response to the Oscillation Stop Detection

# AC CHARACTERISTICS : POE, POEG TIMING (COMPARATOR DETECT AND REGISTER SETTINGS)

## ■ Comparator output detection

This is the time until the target PWM output terminals listed below stop outputting when the COMPn level detection signal is input to the POE3 or POEG module.

- Target PWM Output port
  POE3 : PWM output port of MTU3/GPTW
  POEG : PWM output port of GPTW

POE3

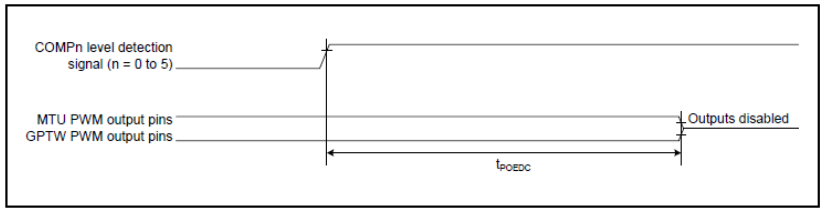



Figure 45.30 Output Disable Time for POE in Response to Detection of the Comparator Outputs

POEG

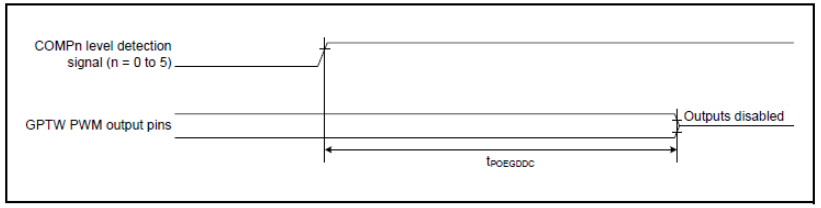



Figure 45.40 Output Disable Time for POEG in Response to Level Detection Signal from a Comparator

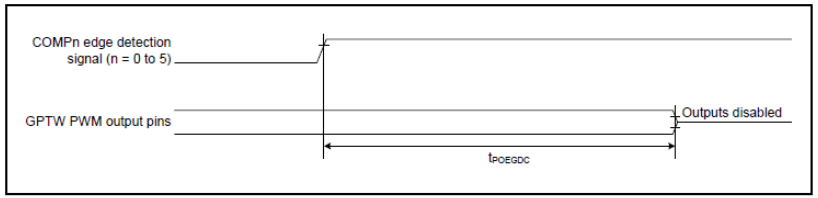



Figure 45.36 Output Disable Time for POEG in Response to Edge Detection Signal from a Comparator

## ■ Register setting

When output stop is set by software (register), it takes until the following target PWM output pins stop output.

- Stop setting register
  POE3 : SPOER register
  POEG : POEGGn.SSF bit
- Target PWM Output port
  POE3 : PWM output port of MTU3/GPTW
  POEG : PWM output port of GPTW

POE3

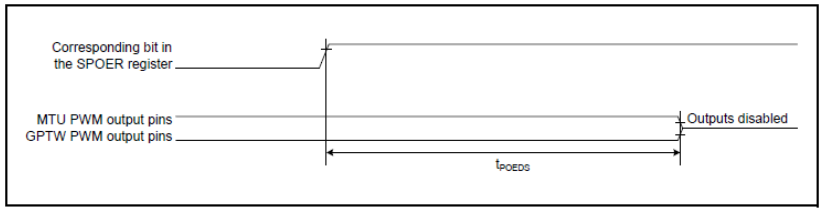



Figure 45.31 Output Disable Time for POE in Response to the Register Setting

POEG

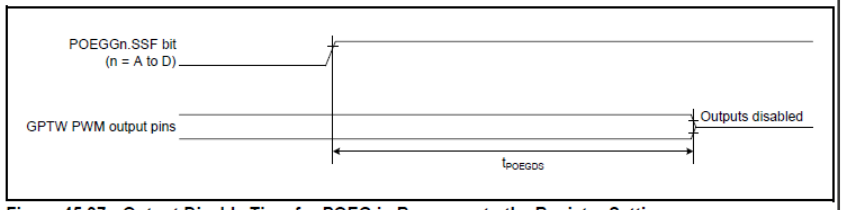



Figure 45.37 Output Disable Time for POEG in Response to the Register Setting

# AC CHARACTERISTICS : A/D CONVERTER TRIGGER TIMING

The timing clock for capturing A/D converter trigger pin level is captured not by the operation clock for A/D but by the operation clock for I/O.
*For this example, PCLKB is not A/D operation clock but I/O operation clock.

For VIH/VIL, refer to ADTGR# Input Terminal section of the Schmitt Trigger Input Voltage in DC Characteristics. ADTGR# pin has a hysteresis-width.

**Table 45.36 A/D Converter Trigger Timing**

Conditions: VCC = 2.7 to 5.5 V, VCC_USB = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5V,
VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V, $T_a = T_{opr}$,
ICLK = 8 to 160 MHz, PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, PCLKC = 8 to 160 MHz, BCLK = 8 to 60 MHz,
Output load conditions: $V_{OH}$ = 0.5 × VCC, $V_{OL}$ = 0.5 × VCC, C = 30 pF,
High-drive output is selected by the driving ability control register (other than for P53 to P55 and P60 to P65).

| Item | | Symbol | Min. | Max. | Unit*1 | Test Conditions |
|---|---|---|---|---|---|---|
| A/D converter | A/D converter trigger input pulse width | $t_{TRGW}$ | 1.5 | — | $t_{PBcyc}$ | Figure 45.44 |

Note 1. $t_{PBcyc}$: PCLKB cycle

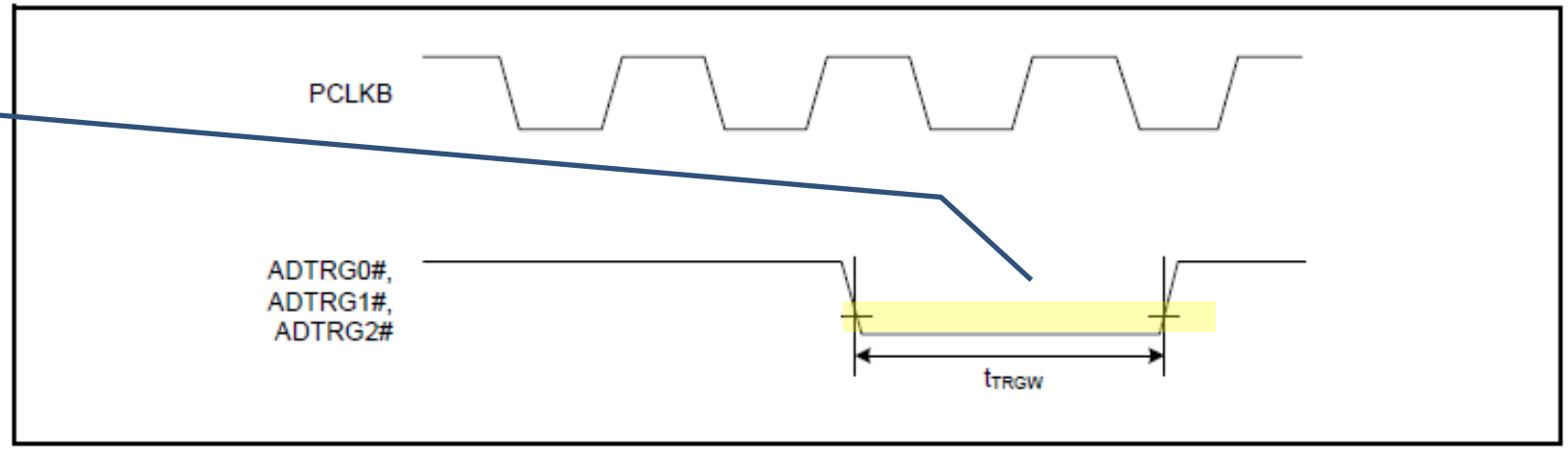



**Figure 45.44 A/D Converter Trigger Input Timing**

# AC CHARACTERISTICS : RSPI

Consider the max. bit rate considering the specifications of the communication-facing IC, such as setting up and holding, and the bus configuration (bus loading).

Required conditions to guarantee the following specifications.

**Table 45.41 RSPI Timing**

Conditions: VCC = 2.7 to 5.5 V, VCC_USB = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5V,
VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V, $T_a = T_{opr}$,
ICLK = 8 to 160 MHz, PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, PCLKC = 8 to 160 MHz, BCLK = 8 to 60 MHz,
Output load conditions: $V_{OH}$ = 0.5 × VCC, $V_{OL}$ = 0.5 × VCC, C = 30 pF,
High-drive output is selected by the driving ability control register (other than for P53 to P55 and P60 to P65).

| Item | | | Symbol | Min.*1 | Max.*1 | Unit*1 | Test Conditions | |
|---|---|---|---|---|---|---|---|---|
| RSPI | RSPCK clock cycle | Master | $t_{SPcyc}$ | 2 | 4096 | $t_{PAcyc}$ | Figure 45.53 | |
| | | Slave | | 4 | — | | | |
| | RSPCK clock high pulse width | Master | $t_{SPCKWH}$ | $(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3$ | — | ns | | |
| | | Slave | | $(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2$ | — | ns | | |
| | RSPCK clock low pulse width | Master | $t_{SPCKWL}$ | $(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3$ | — | ns | | |
| | | Slave | | $(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2$ | — | ns | | |
| | RSPCK clock rise/fall time | Output | $t_{SPCKr}$, $t_{SPCKf}$ | — | 5 | ns | | |
| | | Input | | — | 1 | μs | | |
| | Data input setup time | Master | $t_{SU}$ | 6 | — | ns | VCC ≥ 4.5 V | Figure 45.54 to Figure 45.59 |
| | | | | 11 | — | | VCC < 4.5 V | |
| | | Slave | | 8.3 | — | | Figure 45.54 to Figure 45.59 | |
| | Data input hold time | Master: PCLKA division ratio set to 1/2 | $t_{HF}$ | 0 | — | ns | | |
| | | Master: PCLKA division ratio set to a value other than 1/2 | $t_H$ | $t_{PAcyc}$ | — | | | |
| | | Slave | | 8.3 | — | | | |
| | SSL setup time | Master | $t_{LEAD}$ | 1 | 8 | $t_{SPcyc}$ | | |
| | | Slave | | 6 | — | $t_{PAcyc}$ | | |
| | SSL hold time | Master | $t_{LAG}$ | 1 | 8 | $t_{SPcyc}$ | | |
| | | Slave | | 6 | — | $t_{PAcyc}$ | | |
| | Data output delay time | Master | $t_{OD}$ | — | 6.3 | ns | VCC ≥ 4.5 V | Figure 45.54 to Figure 45.59 |
| | | Slave | | — | 28 | | | |
| | | Master | | — | 11.3 | ns | VCC < 4.5 V | |
| | | Slave | | — | 33 | | | |
| | Data output hold time | Master | $t_{OH}$ | 0 | — | ns | Figure 45.54 to Figure 45.59 | |
| | | Slave | | 0 | — | | | |
| | Successive transmission delay time | Master | $t_{TD}$ | $t_{SPcyc} + 2 \times t_{PAcyc}$ | $8 \times t_{SPcyc} + 2 \times t_{PAcyc}$ | ns | | |
| | | Slave | | $6 \times t_{PAcyc}$ | — | | | |
| | MOSI and MISO rise/fall time | Output | $t_{Dr}$, $t_{Df}$ | — | 5 | ns | | |
| | | Input | | — | 1 | μs | | |
| | SSL rise/fall time | Output | $t_{SSLr}$, $t_{SSLf}$ | — | 5 | ns | | |
| | | Input | | — | 1 | μs | | |
| | Slave access time | | $t_{SA}$ | — | $2 \times t_{PAcyc} + 28$ | ns | VCC ≥ 4.5 V | Figure 45.58, Figure 45.59 |
| | | | | — | $2 \times t_{PAcyc} + 33$ | | VCC < 4.5 V | |
| | Slave output release time | | $t_{REL}$ | — | $2 \times t_{PAcyc} + 28$ | ns | VCC ≥ 4.5 V | |
| | | | | — | $2 \times t_{PAcyc} + 33$ | | VCC < 4.5 V | |

Note 1. $t_{PAcyc}$: PCLKA cycle

# AC CHARACTERISTICS : SIMPLE SPI TIMING

Required conditions to guarantee the following specifications.

Consider the max. bit rate by considering the specifications of the communication destination IC, such as setting up and holding, and the bus configuration (bus loading).

**Table 45.40 Simple SPI Timing**

Conditions: VCC = 2.7 to 5.5 V, VCC_USB = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5V,
VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V, $T_a = T_{opr}$,
ICLK = 8 to 160 MHz, PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, PCLKC = 8 to 160 MHz, BCLK = 8 to 60 MHz,
Output load conditions: $V_{OH}$ = 0.5 × VCC, $V_{OL}$ = 0.5 × VCC, C = 30 pF,
High-drive output is selected by the driving ability control register (other than for P53 to P55 and P60 to P65).

| Item | | Symbol | Min. | Max. | Unit*1 | Test Conditions |
|---|---|---|---|---|---|---|
| Simple SPI (SCI11) | SCK clock cycle output (master) | $t_{SPcyc}$ | 4 | 65536 | $t_{PAcyc}$ | Figure 45.48 |
| | SCK clock cycle input (slave) | | 8 | — | | |
| | SCK clock high pulse width | $t_{SPCKWH}$ | 0.4 | 0.6 | $t_{SPcyc}$ | |
| | SCK clock low pulse width | $t_{SPCKWL}$ | 0.4 | 0.6 | $t_{SPcyc}$ | |
| | SCK clock rise/fall time | $t_{SPCKr}$, $t_{SPCKf}$ | — | 20 | ns | |
| | Data input setup time | $t_{SU}$ | 33.3 | — | ns | Figure 45.49 to Figure 45.52 |
| | Data input hold time | $t_H$ | 33.3 | — | ns | |
| | SS input setup time | $t_{LEAD}$ | 1 | — | $t_{SPcyc}$ | |
| | SS input hold time | $t_{LAG}$ | 1 | — | $t_{SPcyc}$ | |
| | Data output delay time | $t_{OD}$ | — | 33.3 | ns | |
| | Data output hold time | $t_{OH}$ | –10 | — | ns | |
| | Data rise/fall time | $t_{Dr}$, $t_{Df}$ | — | 16.6 | ns | |
| | SS input rise/fall time | $t_{SSLr}$, $t_{SSLf}$ | — | 16.6 | ns | |
| | Slave access time | $t_{SA}$ | — | 7 | $t_{PAcyc}$ | Figure 45.51, Figure 45.52 |
| | Slave output release time | $t_{REL}$ | — | 7 | $t_{PAcyc}$ | |
| Simple SPI (SCI1, SCI5, SCI6, SCI8, SCI9, SCI12) | SCK clock cycle output (master) | $t_{SPcyc}$ | 4 | 65536 | $t_{PBcyc}$ | Figure 45.48 |
| | SCK clock cycle input (slave) | | 8 | — | | |
| | SCK clock high pulse width | $t_{SPCKWH}$ | 0.4 | 0.6 | $t_{SPcyc}$ | |
| | SCK clock low pulse width | $t_{SPCKWL}$ | 0.4 | 0.6 | $t_{SPcyc}$ | |
| | SCK clock rise/fall time | $t_{SPCKr}$, $t_{SPCKf}$ | — | 20 | ns | |
| | Data input setup time | $t_{SU}$ | 33.3 | — | ns | Figure 45.49 to Figure 45.52 |
| | Data input hold time | $t_H$ | 33.3 | — | ns | |
| | SS input setup time | $t_{LEAD}$ | 1 | — | $t_{SPcyc}$ | |
| | SS input hold time | $t_{LAG}$ | 1 | — | $t_{SPcyc}$ | |
| | Data output delay time | $t_{OD}$ | — | 33.3 | ns | |
| | Data output hold time | $t_{OH}$ | –10 | — | ns | |
| | Data rise/fall time | $t_{Dr}$, $t_{Df}$ | — | 16.6 | ns | |
| | SS input rise/fall time | $t_{SSLr}$, $t_{SSLf}$ | — | 16.6 | ns | |
| | Slave access time | $t_{SA}$ | — | 7 | $t_{PBcyc}$ | Figure 45.51, Figure 45.52 |
| | Slave output release time | $t_{REL}$ | — | 7 | $t_{PBcyc}$ | |

Note 1. $t_{PAcyc}$: PCLKA cycle, $t_{PBcyc}$: PCLKB cycle

# AC CHARACTERISTICS (RSPI)

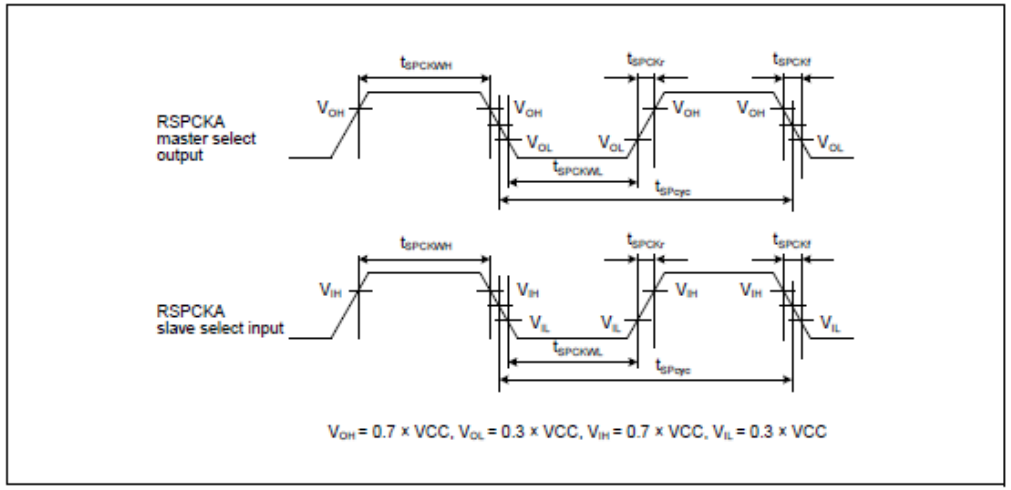



**Figure 45.53 RSPI Clock Timing**

When performing continuous communication, a wait time is required when one frame of data is transmitted.

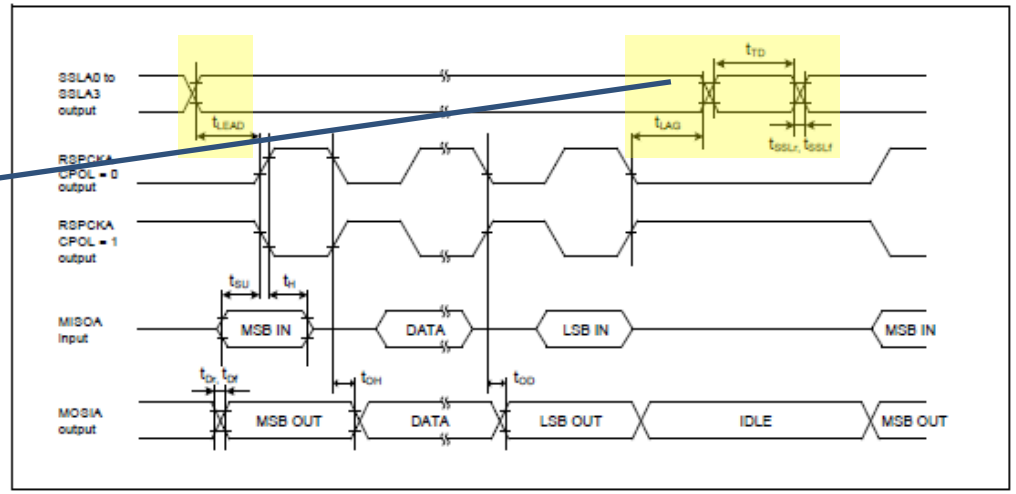



**Figure 45.54 RSPI Timing (Master, CPHA = 0) (Bit Rate: PCLKA Division Ratio Set to a Value Other Than 1/2)**

# RIIC BUS INTERFACE INPUT/OUTPUT TIMING

The upper/lower limit of tSCLH,tSCLL differs depending on the communication speed of IIC. For more information, please refer to the "IIC Bus Specifications" proposed by NXP.

As the rise time varies depending on the load conditions, observe the actual output waveform after mounting the board and check.

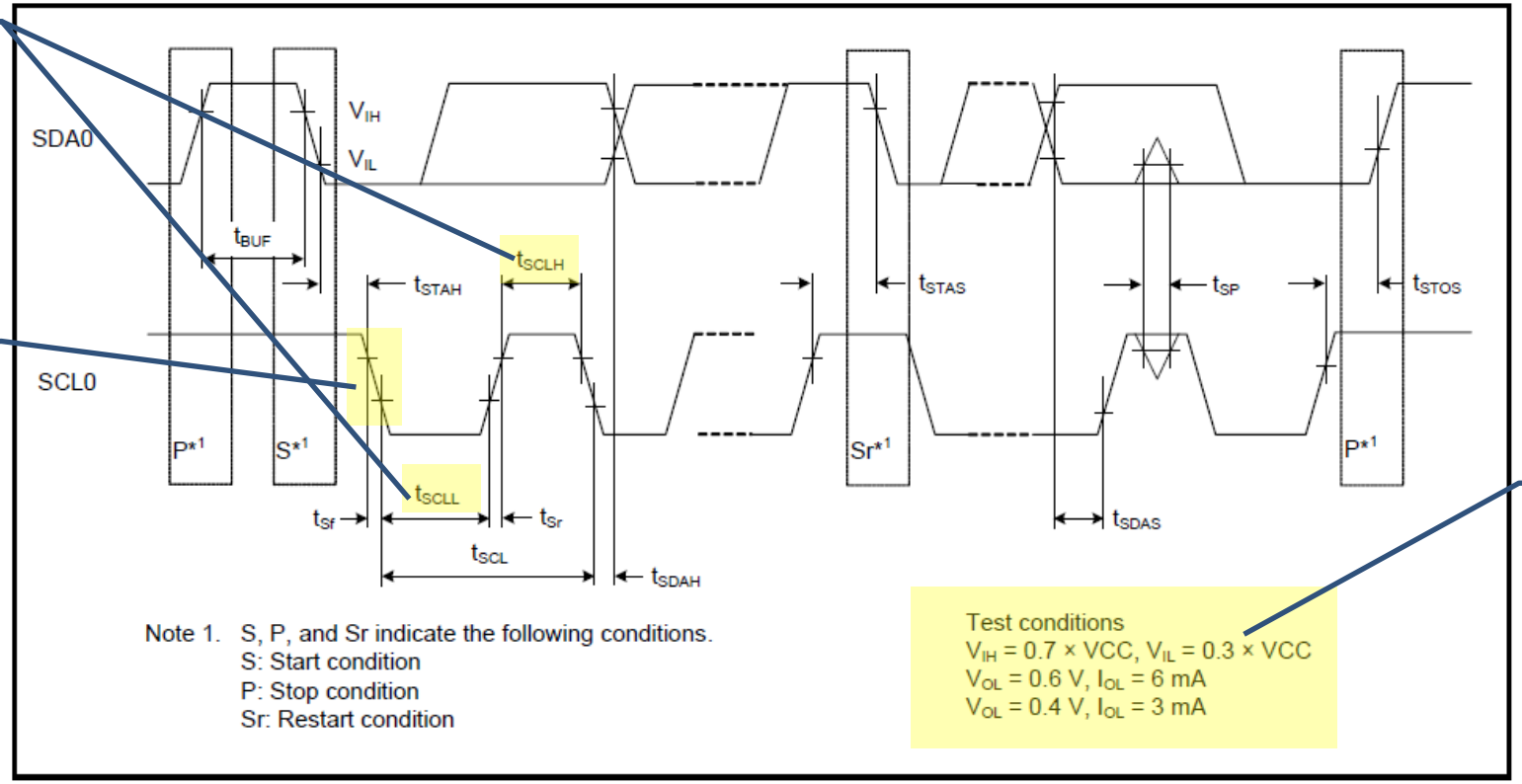



**Figure 45.60 RIIC Bus Interface Input/Output Timing**

The properties of IIC are based on the "IIC Bus Specification" proposed by NXP.

# A/D CONVERSION CHARACTERISTICS

Required conditions to guarantee the following specifications.

Refer to the next page for the terms of A/D conversion.

When a channel-dedicated sample-and-hold circuit is used
Indicates the input-range that can guarantee A/D transformation accuracy. In this situation, A/D conversion accuracy is not guaranteed for input-voltages outside the dynamic range.

Please also refer to the Hardware Manual "Analog input sampling time and scan conversion time (comparison time)".

45.6 A/D Conversion Characteristics

**Table 45.46 12-Bit A/D (Unit 0, 1, 2) Conversion Characteristics (1)**

Conditions: VCC = 2.7 to 5.5 V, VCC_USB = 2.7 to 5.5 V, 4.5 V ≤ AVCC0 = AVCC1 = AVCC2 ≤ 5.5V,
VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V, $T_a = T_{opr}$, PCLKB = PCLKD = 8 to 60 MHz*1,
Source impedance = 1.0 kΩ

| Item | | | | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|---|
| Resolution | | | | 12 | 12 | 12 | Bit | |
| Analog input capacitance | | | | — | — | 30 | pF | |
| Conversion time*2 (Operation at PCLKD = 60 MHz) | AN000 to AN002, AN100 to AN102 | Channel-dedicated sample-and-hold circuits in use | Constant sampling enabled | 1.00 | — | — | μs | • Sampling time: 24 PCLKD |
| | | | Constant sampling disabled | 1.40 | — | — | | • Sampling time of channel-dedicated sample-and-hold circuits: 24 PCLKD<br>• Sampling time: 24 PCLKD |
| | | Channel-dedicated sample-and-hold circuits not in use | | 0.90 | — | — | | • Sampling time: 30 PCLKD |
| | AN003 to AN006, AN103 to AN106 | | | 0.90 | — | — | | • Sampling time: 30 PCLKD |
| | AN007, AN107, AN200 to AN211 | | | 0.95 | — | — | | • Sampling time: 33 PCLKD |
| | AN216 to AN217 | | | 1.05 | — | — | | • Sampling time: 39 PCLKD |
| Offset error | | Channel-dedicated sample-and-hold circuits in use | | — | ±1.5 | ±6.0 | LSB | AN000 to AN002, AN100 to AN102 = 0.2 V |
| | | Channel-dedicated sample-and-hold circuits not in use | | — | ±1.5 | ±5.0 | | |
| Full-scale error | | Channel-dedicated sample-and-hold circuits in use | | — | ±1.5 | ±5.5 | | AN000 to AN002 = AVCC0 – 0.2 V<br>AN100 to AN102 = AVCC1 – 0.2 V |
| | | Channel-dedicated sample-and-hold circuits not in use | | — | ±1.5 | ±4.5 | | |
| Quantization error | | Channel-dedicated sample-and-hold circuits in use | | — | ±0.5 | — | | |
| | | Channel-dedicated sample-and-hold circuits not in use | | — | ±0.5 | — | | |
| Absolute accuracy | AN000 to AN002, AN100 to AN102 | Channel-dedicated sample-and-hold circuits in use | | — | ±3.0 | ±6.0 | | |
| | | Channel-dedicated sample-and-hold circuits not in use | | — | ±2.5 | ±5.5 | | |
| | AN003 to AN007, AN103 to AN107 | | | — | ±2.5 | ±5.5 | | |
| | AN200 to AN211 | | | — | ±2.5 | ±5.5 | | |
| | AN216 to AN217 | | | — | ±2.5 | ±6.5 | | |
| DNL differential nonlinearity error | | Channel-dedicated sample-and-hold circuits in use | | — | ±1.0 | ±2.5 | | |
| | | Channel-dedicated sample-and-hold circuits not in use | | — | ±1.0 | ±1.5 | | |
| INL integral nonlinearity error | | Channel-dedicated sample-and-hold circuits in use | | — | ±1.5 | ±4.0 | | |
| | | Channel-dedicated sample-and-hold circuits not in use | | — | ±1.5 | ±2.5 | | |
| Holding time of the channel-dedicated sample-and-hold circuit | | | | — | — | 20 | μs | |
| Dynamic range | AN000 to AN002 | Channel-dedicated sample-and-hold circuits in use | | 0.2 | — | AVCC0 – 0.2 | V | |
| | AN100 to AN102 | Channel-dedicated sample-and-hold circuits in use | | 0.2 | — | AVCC1 – 0.2 | | |

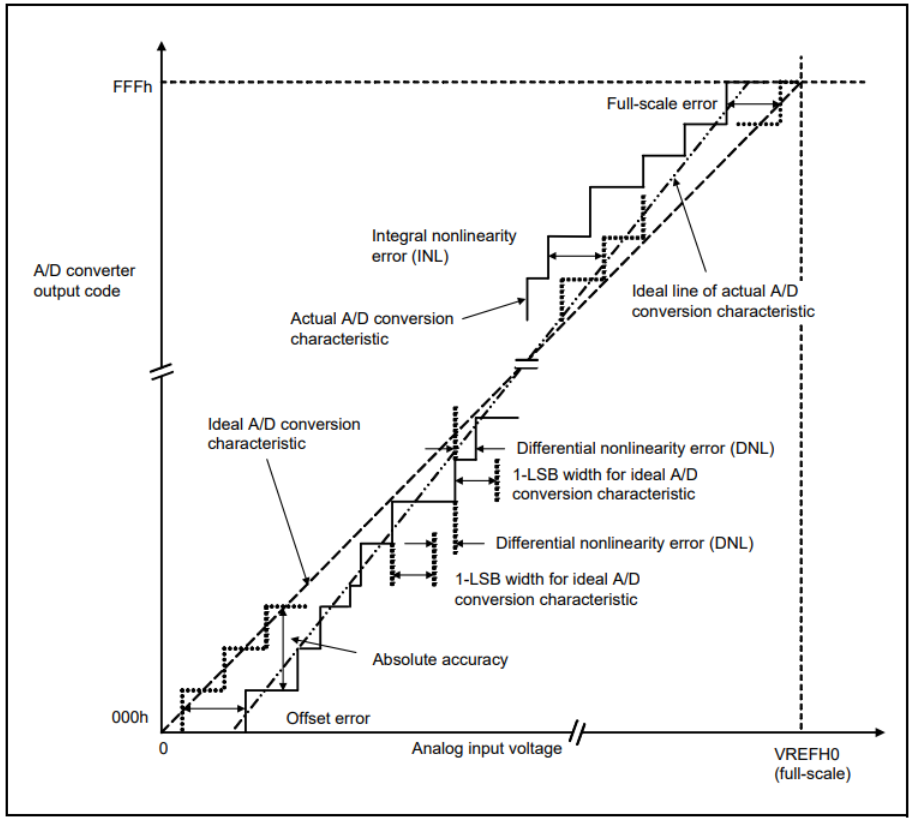
Note: The above specification values apply when there is no access to the external bus during A/D conversion. If access proceeds during A/D conversion, values may not fall within the above ranges.
Note 1. When PCLKD was higher than 40 MHz, capacitors with the following values were placed in parallel with the 0.1-μF capacitors between AVCC0 and AVSS0, AVCC1 and AVSS1, and AVCC2 and AVSS2 for measurement of the A/D conversion characteristics.
- Products with 64 Kbytes of RAM: 1000 pF
- Products with 128 Kbytes of RAM: 0.01 μF
Note 2. The conversion time is the sum of the sampling time and the comparison time. The numbers of sampling-clock cycles are indicated as the test conditions.

There is an upper/lower limit in PCLK of usage conditions. Please note that the settable frequency varies depending on the product.

Complete all channels A/D conversion of the channel-dedicated sample-and-hold circuitry (ANx00~ANx02) by this time.

# EXPLANATION OF A/D CONVERTER-CHARACTERISTIC TERMINOLOGY

- **Absolute accuracy**
  Absolute accuracy is the difference between output code based on the theoretical A/D conversion characteristics, and the actual A/D conversion result. When measuring absolute accuracy, the voltage at the midpoint of the width of analog input voltage (1-LSB width), that can meet the expectation of outputting an equal code based on the theoretical A/D conversion characteristics, is used as an analog input voltage. For example, if 12-bit resolution is used and if reference voltage (VREFH0 = 3.072 V), then 1-LSB width becomes 0.75 mV, and 0 mV, 0.75 mV, 1.5 mV, ... are used as analog input voltages.
  If analog input voltage is 6 mV, absolute accuracy = ±5 LSB means
  that the actual A/D conversion result is in the range of 003h to 00Dh though an output code, 008h, can be expected from the theoretical A/D conversion characteristics.
- **Integral nonlinearity error (INL)**
  Integral nonlinearity error is the maximum deviation between the ideal line
  when the measured offset and full-scale errors are zeroed, and the actual output code.
- **Differential nonlinearity error (DNL)**
  Differential nonlinearity error is the difference between 1-LSB width
  based on the ideal A/D conversion characteristics and the width of the actual output code.
- **Offset error**
  Offset error is the difference between a transition point of the ideal first output code
  and the actual first output code.
- **Full-scale error**
  Full-scale error is the difference between a transition point of the ideal last output code
  and the actual last output code.



# A/D INTERNAL REFERENCE VOLTAGE CHARACTERISTICS

**It is the reference voltage inside the chip, not the reference voltage of A/D converters.**
Measuring this value can be used to determine if AD modulehas failed.

This is a total consideration including voltage-fluctuation, temperature-fluctuation, secular change, and variation of individual MCU.

**Table 45.48 A/D Internal Reference Voltage Characteristics**

Conditions: VCC = 2.7 to 5.5 V, VCC_USB = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5V,
VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V, $T_a = T_{opr}$, PCLKB = PCLKD = 8 to 60 MHz

| Item | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|
| A/D internal reference voltage | 1.20 | 1.25 | 1.30 | V | |

Note: The above specification values apply during normal operations.

Required conditions to guarantee the following specifications.

Can be used to determine if a AD module is faulty or a reference voltage is faulty.

# PROGRAMMABLE GAIN AMPLIFIER CHARACTERISTICS

**Table 45.49 Programmable Gain Amplifier Characteristics (single-ended input)**

Conditions: VCC = 2.7 to 5.5 V, VCC_USB = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5V, VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V, $T_a = T_{opr}$

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Input offset voltage | $V_{IO}$ | — | 3 | 8 | mV | |
| Single-ended input voltage range | $V_{ISR}$ | $V_{OR}$ (min)/G | — | $V_{OR}$ (min)/G | V | |
| Output voltage range | $V_{OR}$ | 0.10 × AVCCn | — | 0.90 × AVCCn | | G = 2.000 to 3.636 |
| | | 0.15 × AVCCn | — | 0.85 × AVCCn | | G = 4.000 to 6.667 |
| | | 0.20 × AVCCn | — | 0.80 × AVCCn | | G = 8.000 to 20.000 |
| Gain | G | 2.000 | — | 20.000 | Linear gain | |
| Gain error | $E_G$ | — | ±0.5 | ±2.0 | % | G = 2.000 |
| | | — | ±0.5 | ±2.0 | | G = 2.500 |
| | | — | ±0.5 | ±2.0 | | G = 3.077 |
| | | — | ±0.5 | ±2.0 | | G = 3.636 |
| | | — | ±0.6 | ±2.0 | | G = 4.000 |
| | | — | ±0.6 | ±2.0 | | G = 4.444 |
| | | — | ±0.7 | ±2.0 | | G = 5.000 |
| | | — | ±0.7 | ±3.0 | | G = 6.667 |
| | | — | ±0.7 | ±3.0 | | G = 8.000 |
| | | — | ±0.7 | ±4.0 | | G = 10.000 |
| | | — | ±1.1 | ±4.0 | | G = 13.333 |
| | | — | ±1.3 | ±4.0 | | G = 20.000 |
| Slew rate | SR | 10 | — | — | V/µs | |
| Operation stabilization time | $t_{start}$ | — | — | 5 | µs | |

n = 0 and 1

**Table 45.50 Programmable Gain Amplifier Characteristics (pseudo-differential input)**

Conditions: VCC = 2.7 to 5.5 V, VCC_USB = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5V, VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V, $T_a = T_{opr}$

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions*1 |
|---|---|---|---|---|---|---|
| Input offset voltage | $V_{IO}$ | — | 10 | 20 | mV | |
| Differential input voltage range | $V_{IDR}$ | –0.28 × AVCCn / G | — | 0.28 × AVCCn / G | V | |
| Output voltage range | $V_{OR}$ | 0.22 × AVCCn | — | 0.78 × AVCCn | | |
| Input voltage range (PGAVSSn) | $V_{I(PGAVSS)}$ | –0.5 | — | 0.3 | | AVCCn < 4.3V |
| | | –0.5 | — | 0.6 | | AVCCn ≥ 4.3 V |
| Gain error | $E_G$ | — | ±0.5 | ±2.0 | % | G = 1.500 |
| | | — | ±0.5 | ±2.0 | | G = 4.000 |
| | | — | ±0.8 | ±3.0 | | G = 7.000 |
| | | — | ±1.2 | ±4.0 | | G = 12.333 |
| Slew rate | SR | 10 | — | — | V/µs | |
| Operation stabilization time | $t_{start}$ | — | — | 5 | µs | |

n = 0 and 1

Note 1. When AVCC0 = AVCC1 = AVCC2 ≥ 4.0 V, VOLSR.PGAVLS = 0
When AVCC0 = AVCC1 = AVCC2 < 4.0 V, VOLSR.PGAVLS = 1

This is the time until the operation stabilizes after PGA is enabled in S12ADx.ADPGACR.PxxxCR[3:0].

Voltages in the range of 0 to min, max ~ AVCC are output. However, you cannot guarantee these values.

# COMPARATOR CHARACTERISTICS

Required conditions to guarantee the following specifications.

This is the waiting time required to stabilize the operation after changing the setting of the comparator using the CMPSELx register.

This is the time it takes for the operation to stabilize after setting CMPCTL.HCMPON=1.

It is an electrical characteristic value at overdrive voltage (VOD) = 100 mV.

45.8 Comparator Characteristics

**Table 45.51 Comparator Characteristics**

Conditions: VCC = 2.7 to 5.5 V, VCC_USB = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5V, VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V, $T_a = T_{opr}$

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Input offset voltage | $V_{IO}$ | — | 8 | 40 | mV | |
| Reference input voltage range | $V_{ref}$ | 0 | — | AVCC1 | V | CMPSEL1.CVRS[3:0] = 0100b, 1000b |
| | | 0 | — | AVCC2 | | CMPSEL1.CVRS[3:0] = 0001b, 0010b |
| Response time | $t_{tot(r)}$ | — | — | 200 | ns | VOD = 100 mV CMPCTL.CDFS[1:0] = 00b |
| | $t_{tot(f)}$ | — | — | 200 | | |
| Waiting time for stabilization following switching of the input | $t_{cwait}$ | 300 | — | — | | |
| Operation stabilization time | $t_{cmp}$ | — | — | 1 | µs | |

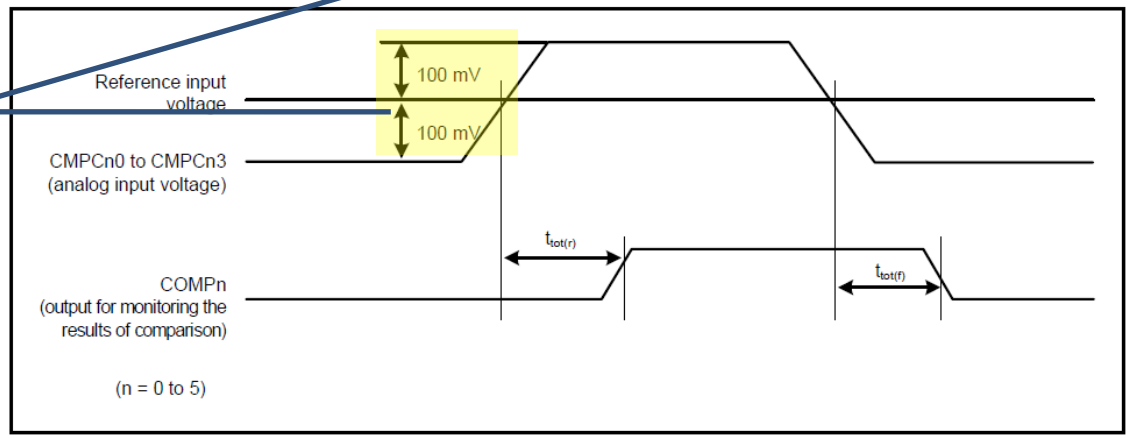



**Figure 45.66 Comparator Response Time**

# D/A CONVERSION CHARACTERISTICS

## 60.7 D/A Conversion Characteristics

Required conditions to guarantee the following specifications.

**Table 60.52 D/A Conversion Characteristics**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

| Item | | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| Resolution | | — | 12 | 12 | 12 | Bit | |
| Unbuffered output | Absolute accuracy | — | — | — | ±6.0 | LSB | 2-MΩ resistive load<br>10-bit conversion |
| | Differential nonlinearity error | DNL | — | ±1.0 | ±2.0 | LSB | 2-MΩ resistive load |
| | Output resistance | $R_O$ | — | 8.6 | — | kΩ | |
| | Setting time | $t_S$ | — | — | 3 | μs | 20-pF capacitive load |
| Buffered output | Load resistance | $R_L$ | 5 | — | — | kΩ | |
| | Load capacitance | $C_L$ | — | — | 50 | pF | |
| | Output voltage | $V_O$ | 0.2 | — | AVCC1 – 0.2 | V | |
| | Differential nonlinearity error | DNL | — | ±1.0 | ±2.0 | LSB | |
| | Integral nonlinearity error | INL | — | ±2.0 | ±4.0 | LSB | |
| | Setting time | $t_S$ | — | — | 4 | μs | |

This is the buffer characteristic when the low-capacitance impedance buffer is enabled.

Some products have no buffer.

If an output without buffer is used and a buffer is connected externally, it must be larger than RO resistor (for example, 100 times or more).
(Refer to the next page.)

0V~0.2V and AVCC1-0.2~AVCC are not guaranteed, although the voltage is output.

In the case of buffered output, DNL and INL characteristics are guaranteed rather than absolute accuracy.

# D/A CONVERSION CHARACTERISTICS

60.7 D/A Conversion Characteristics

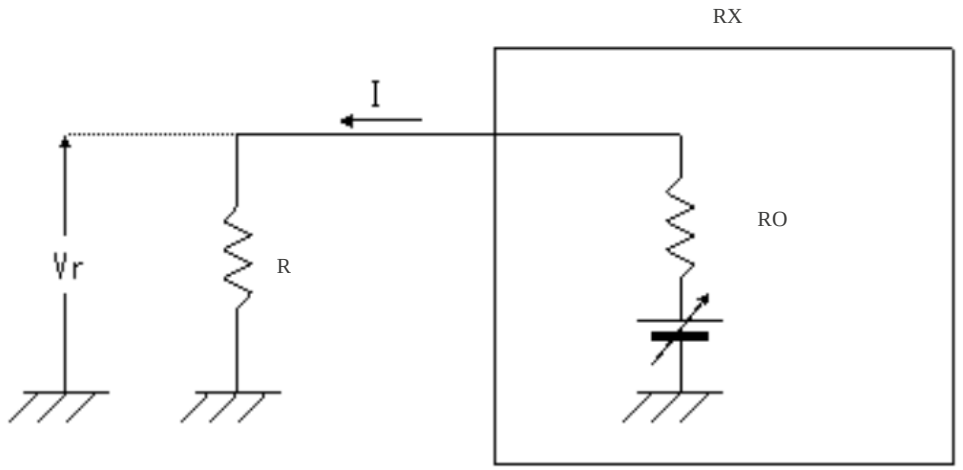
**Table 60.52 D/A Conversion Characteristics**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

| Item | | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| Resolution | | — | 12 | 12 | 12 | Bit | |
| Unbuffered output | Absolute accuracy | — | — | — | ±6.0 | LSB | 2-MΩ resistive load<br>10-bit conversion |
| | Differential nonlinearity error | DNL | — | ±1.0 | ±2.0 | LSB | 2-MΩ resistive load |
| | Output resistance | $R_O$ | — | 8.6 | — | kΩ | |
| | Setting time | $t_S$ | — | — | 3 | μs | 20-pF capacitive load |
| Buffered output | Load resistance | $R_L$ | 5 | — | — | kΩ | |
| | Load capacitance | $C_L$ | — | — | 50 | pF | |
| | Output voltage | $V_O$ | 0.2 | — | AVCC1 – 0.2 | V | |
| | Differential nonlinearity error | DNL | — | ±1.0 | ±2.0 | LSB | |
| | Integral nonlinearity error | INL | — | ±2.0 | ±4.0 | LSB | |
| | Setting time | $t_S$ | — | — | 4 | μs | |

Output resistor (RO) in D/A converters.
When external buffers are connected, a voltage-drop occurs due to the output-resistance inside D/A converter. The actual Vr are as follows.
Vr = Output voltage*R/ (R + RO)

Therefore, in order to bring Vr closer to the output voltage,
The external resistance (R) must be greater than RO (e.g., 100 times or more).



# TEMPERATURE SENSOR CHARACTERISTICS

The temperature can be calculated using this value. However, this value is only an average value, and there are individual differences.

If you wish to perform more accurate temperature measurement, we recommend that you perform two-point measurement for each chip and calculate the slope individually.

Average value of temperature sensor output potential when ambient temperature is 25°C. The temperature can be calculated using this value. However, this value is only an average value, and there are individual differences.

If you want to make more accurate temperature measurements, we recommend that you make actual measurements for each chip and use that value.

This temperature sensor can measure the temperature inside the chip.
Since there is a variation between individual values of this temperature sensor, the temperature slope and output potential of this temperature sensor characteristics are average (typical).
If you want to measure the temperature with higher accuracy, perform trial measurements of 1 and 2 points of temperature for each individual, and calculate the temperature slope and output potential.
For the calculation method, please refer to the How to use the temperature sensor in the Temperature Sensors chapter.

60.8 Temperature Sensor Characteristics

**Table 60.53 Temperature Sensor Characteristics**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

| Item | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|
| Relative accuracy | — | ±1 | — | °C | |
| Temperature slope | — | 4 | — | mV/°C | |
| Output voltage | — | 1.21 | — | V | $T_a$ = 25°C |
| Temperature sensor start time | — | — | 30 | µs | |
| Sampling time*1 | 4.15 | — | — | µs | |

Note 1. Set the S12AD1.ADSSTRT register such that the sampling time of the 12-bit A/D converter satisfies this specification.

This is the stable waiting time of the output (reference voltage) of the temperature sensor.
After starting up the temperature sensor, wait for the temperature sensor startup time before starting the A/D conversion.
The temperature sensor activation signal differs for each microcomputer. Check the temperature sensor chapter.

# FLASH MEMORY CHARACTERISTICS

45.13 Flash Memory Characteristics

**Table 45.56 Code Flash Memory Characteristics**

Conditions: VCC = 2.7 to 5.5 V, VCC_USB = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5V,
VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V,
Temperature range for program/erase: $T_a = T_{opr}$

| Item | | Symbol | FCLK = 4 MHz | | | 20 MHz ≤ FCLK ≤ 60 MHz | | | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | Min. | Typ. | Max. | | |
| Program time ($N_{PEC}$ ≤ 100 cycles) | 256 bytes | $t_{P256}$ | — | 0.9 | 13.2 | — | 0.4 | 6 | ms | |
| | 8 Kbytes | $t_{P8K}$ | — | 29 | 176 | — | 13 | 80 | | |
| | 32 Kbytes | $t_{P32K}$ | — | 116 | 704 | — | 52 | 320 | | |
| Program time ($N_{PEC}$ > 100 cycles) | 256 bytes | $t_{P256}$ | — | 1.1 | 15.8 | — | 0.5 | 7.2 | | |
| | 8 Kbytes | $t_{P8K}$ | — | 35 | 212 | — | 16 | 96 | | |
| | 32 Kbytes | $t_{P32K}$ | — | 140 | 848 | — | 64 | 384 | | |
| Erase time ($N_{PEC}$ ≤ 100 cycles) | 8 Kbytes | $t_{E8K}$ | — | 71 | 216 | — | 39 | 120 | | |
| | 32 Kbytes | $t_{E32K}$ | — | 254 | 864 | — | 141 | 480 | | |
| Erase time ($N_{PEC}$ > 100 cycles) | 8 Kbytes | $t_{E8K}$ | — | 85 | 260 | — | 47 | 144 | | |
| | 32 Kbytes | $t_{E32K}$ | — | 304 | 1040 | — | 169 | 576 | | |
| Program/erase cycles*1 | | $N_{PEC}$ | 1000*2 | — | — | 1000*2 | — | — | Cycles | |
| Program suspend latency | | $t_{SPD}$ | — | — | 264 | — | — | 120 | µs | |
| Primary erase suspend latency in suspend priority mode | | $t_{SESD1}$ | — | — | 216 | — | — | 120 | | |
| Secondary erase suspend latency in suspend priority mode | | $t_{SESD2}$ | — | — | 1.7 | — | — | 1.7 | ms | |
| Erase suspend latency in erase priority mode | | $t_{SEED}$ | — | — | 1.7 | — | — | 1.7 | | |
| Forced stop command | | $t_{FD}$ | — | — | 32 | — | — | 20 | µs | |
| Data retention*3, *4 | | $t_{DRP}$ | 20 | — | — | 20 | — | — | Year | $T_a$ ≤ 85°C |
| | | | 10 | — | — | 10 | — | — | | $T_a$ ≤ 105°C |

Note 1. Definition of program/erase cycle:
The program/erase cycle is the number of erasing for each block. When the number of program/erase cycles is n, each block can be erased n times. For instance, when 256-byte program is performed 32 times for different addresses in 8-Kbyte block and then the block is erased, the program/erase cycle is counted as one. However, the same address cannot be programmed more than once before the next erase cycle (overwriting is prohibited).
Note 2. Characteristics are degraded as the number of program/erase increases. This is the minimum value of program/erase cycles to guarantee all characteristics listed in this table.
Note 3. This shows the characteristic when the flash memory writer or self-programming library from Renesas Electronics is in use, and the number of times programming and erasure proceed does not exceed the specified value.
Note 4. These values are based on the results of reliability testing.

Required conditions to guarantee the following specifications.

The range of typ/max values depends on individual differences in the product, temperature, number of writes, etc.

The target area of the program/erase count is for each area of the program unit.
For example, if the program unit is 4B for a 32 KB area, it is possible to achieve more writes than described as a whole by staggering the areas instead of writing to the same area continuously.

# DATA FLASH CHARACTERISTICS

**Table 45.57 Data Flash Memory Characteristics**

Conditions: VCC = 2.7 to 5.5 V, VCC_USB = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5V,
VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V,
Temperature range for program/erase: $T_a = T_{opr}$

| Item | | Symbol | FCLK = 4 MHz | | | 20 MHz ≤ FCLK ≤ 60 MHz | | | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | Min. | Typ. | Max. | | |
| Program time | 4 bytes | $t_{DP4}$ | — | 0.36 | 3.8 | — | 0.46 | 1.7 | ms | |
| Erase time | 64 bytes | $t_{DE64}$ | — | 3.1 | 18 | — | 1.7 | 10 | | |
| Blank check time | 4 bytes | $t_{DBC4}$ | — | — | 84 | — | — | 30 | µs | |
| | 64 bytes | $t_{DBC64}$ | — | — | 280 | — | — | 100 | | |
| | 2 Kbytes | $t_{DBC2K}$ | — | — | 6160 | — | — | 2200 | | |
| Program/erase cycles*1 | | $N_{DPEC}$ | 100000 *2 | — | — | 100000 *2 | — | — | Cycles | |
| Program suspend latency | | $t_{DSPD}$ | — | — | 264 | — | — | 120 | µs | |
| Primary erase suspend latency in suspend priority mode | | $t_{DSESD1}$ | — | — | 216 | — | — | 120 | | |
| Secondary erase suspend latency in suspend priority mode | | $t_{DSESD2}$ | — | — | 300 | — | — | 300 | | |
| Erase suspend latency in erase priority mode | | $t_{DSEED}$ | — | — | 300 | — | — | 300 | | |
| Forced stop command | | $t_{FD}$ | — | — | 32 | — | — | 20 | | |
| Data retention*3, *4 | | $t_{DDRP}$ | 20 | — | — | 20 | — | — | Year | $T_a \leq 85°C$ |
| | | | 10 | — | — | 10 | — | — | | $T_a \leq 105°C$ |

Note 1. Definition of program/erase cycle:
The program/erase cycle is the number of erasing for each block. When the number of program/erase cycles is n, each block can be erased n times. For instance, when 4-byte program is performed 512 times for different addresses in 2-Kbyte block and then the block is erased, the program/erase cycle is counted as one. However, the same address cannot be programmed more than once before the next erase cycle (overwriting is prohibited).

Note 2. Characteristics are degraded as the number of program/erase increases. This is the minimum value of program/erase cycles to guarantee all characteristics listed in this table.

Note 3. This shows the characteristic when the flash memory writer or self-programming library from Renesas Electronics is in use, and the number of times programming and erasure proceed does not exceed the specified value.

Note 4. These values are based on the results of reliability testing.

Required conditions to guarantee the following specifications.

The range of typ/max values depends on individual differences in the product, temperature, number of writes, etc.

The target area of the program/erase count is for each area of the program unit.
For example, if the program unit is 4B for a 32 KB area, it is possible to achieve more writes than described as a whole by staggering the areas instead of writing to the same area continuously.

If the specified number of programs/erases is exceeded, the write/erase time will be longer and read errors will be more likely to occur.

# REVISION HISTORY

| Revision | Date | Page | Contents |
|---|---|---|---|
| 1.00 | 2022/11 | - | 1st version issued. |
| 2.00 | 2024/07 | P.6 | Updated the description regarding hysteresis width. |
| | | P.12 ~ 48 | Add the contents for “AC characteristics and others”. |