Verification Guide

RZ/T2H and RZ/N2H Groups

PCB Verification Guide for LPDDR4

RZ/T Series for Real-Time Control
RZ/N Series for Industrial Network
RZ Family
64-Bit & 32-Bit Arm®-Based High-End MPUs

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Rev.1.00 Sep 2024

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(Rev.5.0-1 October 2020)

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General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

Contents

1. Introduction

1.1 Overview

This document provides PCB verification guide on DDR-IF. The purpose of this guide is to help PCB design engineers to design signals and power supplies of DDR-IF in their PCB design. DDR-IF design needs to satisfy the waveform quality specification defined in JEDEC. To achieve this, intensive signal and power integrity verification are necessary with the use of LSI, PCB and DDR model (connected system level simulation of these models).

The chapters of this guide are organized as follows:

- Chapter 1 describes operating conditions, signal and power name list of DDR-IF, and verification method and items.
- Chapter 2 describes simulation setup for the signal and power integrity verification in the system level. Deliverables provided by Renesas are LSI model and information. System level simulation can be performed using PCB model to be prepared by user and DRAM model provided by DRAM vender.
- Chapter 3 describes recommended IO setting and PCB configuration for all DDR-IF signal and power.
- Chapter 4 describes verification items and method of signal line: verification item list, its target value, and measurement method for simulated waveform.
- Chapter 5 describes verification items and method of IO Power Distribution Network (PDN): verification item list, its target value (target impedance), and measurement method for PDN impedance.

1.2 Operating conditions

(1) Data transfer rate

- LPDDR4 : 3200Mbps

(2) DRAM and its connection

Table 1.1 DRAMs to be used and connections per X32 PHY

DRAM type	Bit count	Number of Rank	Number of connected DRAMs	DRAM grade
LPDDR4	X32	1 or 2	1	LPDDR4-3200, 3733, 4266

(3) DRAM specification

- JEDEC standard: JESD209-4D

(4) On die termination (ODT)

- Turn on ODT, to keep the signal quality.

(5) The function of LSI

- Use Write Leveling.
- Use Write Data timing training.
- Use Write Data Vref Training for LPDDR4.
- Use Read Data timing training.
- Use Read Data Vref Training for LPDDR4.
- Use WRITE/READ Data periodic timing training for LPDDR4.

- Use Command/Address timing training for LPDDR4.
- Use DBI in Write mode for LPDDR4. DBI is not used in Read mode.
- Use periodic calibration to the output drive strength and the termination resistance.

1.3 Signal and power name of DDR-IF

Descriptions and abbreviations of signal name are defined as Table 1.2, Table 1.3 and Table 1.4. DDR power supply pins are shown in Table 1.5. VREF for PHY is generated inside, so there are no terminals.

Table 1.2 Signal line (DQS/DQS#, DQ/DM)

LSI pin name	Description	Abbreviation
DDR_DQSA_T[1:0] / DDR_DQSA_C[1:0] DDR_DQSB_T[1:0] / DDR_DQSB_C[1:0]	Data strobe	DQS/DQS#
DDR_DQA[15:0], DDR_DQB[15:0]	Data	DQ
DDR_DMIA[1:0], DDR_DMIB[1:0]	Data Mask Inversion	DM

Table 1.3 Signal line (CK/CK#, CA/CTRL)

LSI pin name	Description	Abbreviation
DDR_CKA_T / DDR_CKA_C DDR_CKB_T / DDR_CKB_C	Clock	CK/CK#
DDR_CAA[5:0], DDR_CAB[5:0]	Command/Address	CA
DDR_CSA[1:0], DDR_CSB[1:0]	Chip select	CS
DDR_CKEA[1:0], DDR_CKEB[1:0]	Clock enable	CKE
DDR_RESET_N	Reset	RESET_N

Note: LSI has no terminal for driving ODT_CA at LPDDR4. Pull up the OCT_CA to VDDQ on PCB. Refer to 3.1.9.

Table 1.4 Other signal line

LSI pin name	Description	Abbreviation
DDR_ZN	Calibration reference	ZN
DDR_DTEST, DDR_ATEST	Open	-

Note: Pull-down ZN at LSI to GND via a chip resistor. Refer to 3.2.13.2.1.

Pull-up ZQ at LPDDR4 memory via a chip resistor. Refer to the datasheet of JEDEC and DRAM vendor.

Table 1.5 Power supply

LSI pin name	Description	Abbreviation
DDR_VDDQ	Power supply for DDR-IF IO	-
DDR_VAA	Power supply for DDR PLL	-
VSS	Ground pin	

1.4 Verification items and method

Figure 1.1 shows the interconnect between LSI and DRAM in DDR system. In transmitting and receiving data, drivers on LSI/DRAM transmit the data to DRAM/LSI via LSI PKG and PCB during Write/Read access (Figure 1.1 shows Write image).

Therefore, in designing PCB of DDR-IF, there are verification items on signal line and IO PDN shown in Table 1.6 and next page. Verification items are summarized from Table 4.1 to Table 4.14 and Table 5.1.

All restrictions must be satisfied in your PCB design. Please refer to chapter 4 and 5 about each verification items and method in detail.

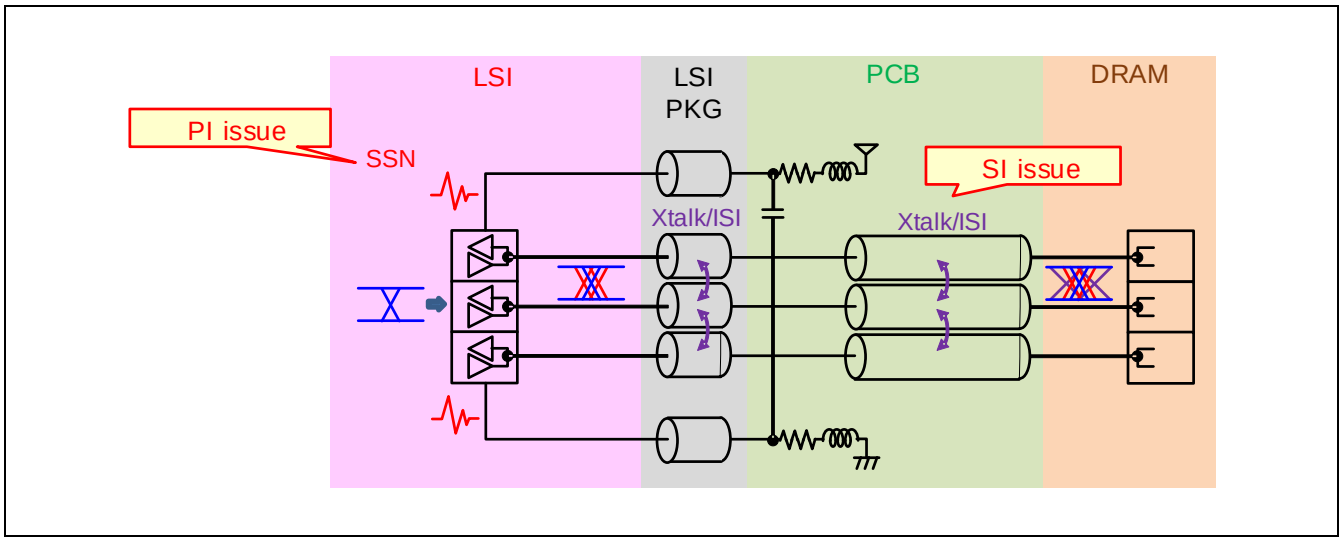

Figure 1.1 Interconnect in DDR System

Table 1.6 Verification items of DDR-IF

Verification target	Category	Verification items	reference
Signal line	Skew restrictions	Data-strobe skew, data-data skew and so on.	Section 4.1.1
	Flight-time restrictions	Flight-time	Section 4.1.2
	Timing restrictions	Eye, pulse width, jitter	Section 4.1.3
IO power distribution network	Waveform restrictions	Amplitude, slew rate, cross point, overshoot, undershoot and so on	Section 4.1.4
	IO power distribution network restrictions	Power supply impedance	Section 5.1

(1) Signal line restrictions

i) Skew restrictions

In DDR system, some kind of de-skew trainings need to be performed in order to realize high speed data transfer. It leads to the decrease of excessive serpentine routing and the relaxation of restrictions for PCB skew.

However, PCB skew and delay between DDR-IF signals must be managed within adjustable range for LSI because that range is finite.

In the verification of skew restrictions, only path mismatch which is not physical length, but electrical length should be measured.

ii) Flight-time restrictions

As well as skew restrictions, the flight-time restrictions must be satisfied in your PCB design.

iii) Timing restrictions

Timing at DRAM receiver is degraded because LSI PKG and PCB have some impedance mismatch, loss, inter-signal coupling and ground bounce which cause the reflection, Inter-Symbol Interference (ISI) and Cross talk (Xtalk). It's called Signal Integrity (SI) issue. In order to transmit the data correctly, these degradation components should be controlled so that all DDR signals satisfy JEDEC and LSI specification. In the verification of timing restrictions, signal timing should be verified taking these ISI and Xtalk into account.

iv) Waveform restrictions

Waveform (amplitude, slew rate and so on) at DRAM receiver is also degraded due to Xtalk, ISI and reflection.

In the verification of waveform restrictions, signal waveforms should be verified taking these ISI and Xtalk into account.

(2) IO power distribution network restrictions

In non-ideal power supply, Simultaneous Switching noise (SSN) causes degradation of LSI's output waveform. It's called Power Integrity (PI) issue. In the verification of IO power distribution network restrictions, target impedance for IO PDN must be satisfied.

For SI and PI issue, PCB design for DDR-IF need to satisfy the timing and waveform restrictions as SI verification and the target impedance of IO PDN as PI verification. Target values of timing and waveform restrictions in this guide are more severe than JEDEC standard because we need to consider the influence of power noise. Then, PI degradation for timing and waveform restriction is estimated by PI simulation based on the target impedance and is included in its target values.

2. Deliverables and simulation setup

This section shows necessary materials for DDR-IF verification. LSI models are provided by Renesas. User needs to prepare PCB models and get DRAM models from DRAM vender.

2.1 Information and models provided by Renesas

(1) BGA pin assignments

(2) IO buffer Model

IBIS IO buffer model (Ver.5.1):

Table 2.1 IBIS filename

Signal	IBIS filename
CA, CS	ca_nclp_lpd4_pc.ibs
CK	ck_nclp_lpd4_pc.ibs
CKE	cke_nclp_lpd4_pc.ibs
DQ, DM, DQS	dq_nclp_lpd4_pc.ibs
RESET	rst_nclp_lpd4_pc.ibs

(3) PKG model of DDR-IF signals (S-parameter)

Table 2.2 S-parameter filename

Signal	S-parameter filename	
	RZ/T2H	RZ/N2H
CA, CS, CK, CKE, RESET	RZT2H_LPDDR4_CA_RESET.s50p	RZN2H_LPDDR4_CA_RESET.s50p
DQA, DMIA, DQSA	RZT2H_LPDDR4_DQA.s44p	RZN2H_LPDDR4_DQA.s44p
DQB, DMIB, DQSB	RZT2H_LPDDR4_DQB.s44p	RZN2H_LPDDR4_DQB.s44p

(4) LSI IO PDN model for target impedance confirmation

Table 2.3 LSI IO PDN model filename

Component	Filename	
	RZ/T2H	RZ/N2H
Package Model	RZT2H_LPDDR4_DDR_VDDQ.s79p	RZN2H_LPDDR4_DDR_VDDQ.s79p
Die Model VDDQLP	die_model_VDDQLP.spi	die_model_VDDQLP.spi
Die Model VDDQ	die_model_VDDQ.spi	die_model_VDDQ.spi
Capacitance Model 1	GRM033D70J105ME01_25degC.mod	GRM033D70J105ME01_25degC.mod
Capacitance Model 2	GRM033R71E682KE14_DC0V_25degC.mod	GRM033R71C472KE14_DC0V_25degC.mod

Note: See readme.pdf included in the archive file for the connection of components.

(5) LSI User's Manual

2.2 Models to be prepared by user

(1) PCB model of DDR-IF signals between LSI and DRAM
(Xtalk and impedance mismatch of PCB trace should be included in this model.)

(2) PCB model of IO PDN for target impedance verification

2.3 Models provided by DRAM vendor

DRAM model (IO model, PKG model and so on)

2.4 Simulation setup

Figure 2.1 shows a circuit diagram image in verification of signal line. Renesas provides IO buffer model and PKG model. User needs to prepare PCB model. DRAM model is provided by DRAM vendor.

Figure 2.2 shows a circuit diagram image in verification of DDR IO PDN. User needs to prepare PCB model, connect it with LSI model provided by Renesas and verify the impedance of DDR IO power supply which is shown as ZPDN in Figure 2.2.

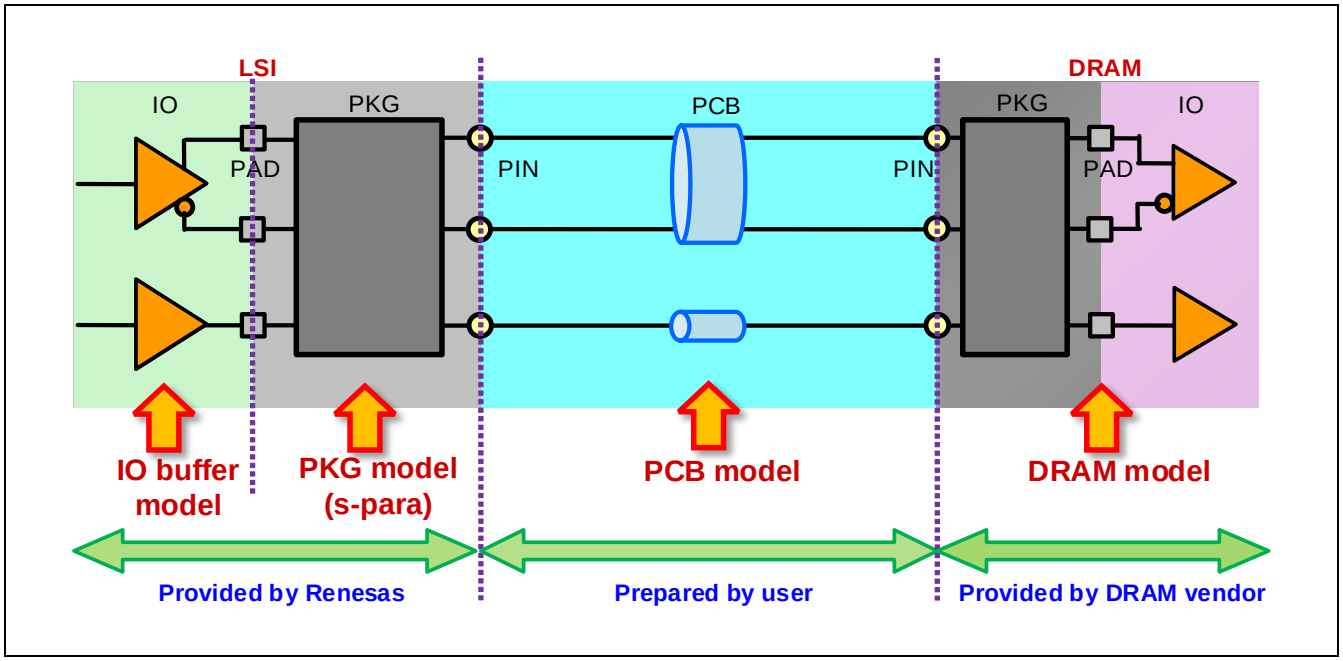

Figure 2.1 Measurement circuit connection image in verification of signal line

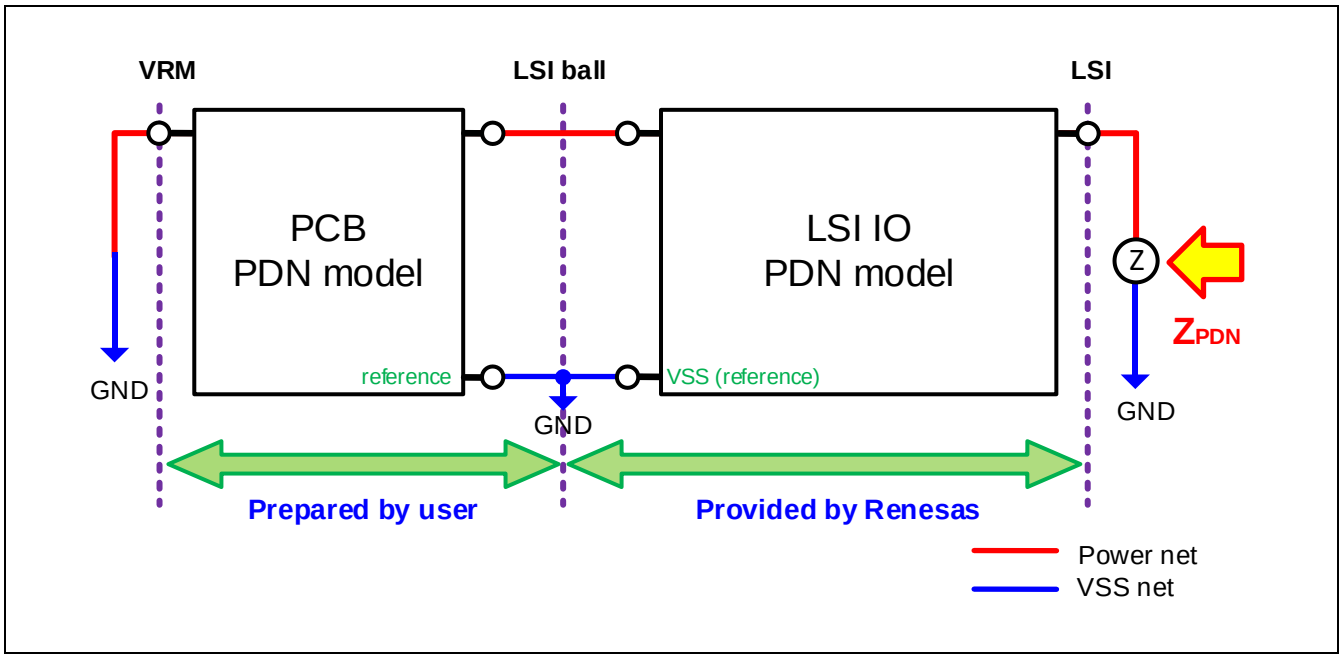

Figure 2.2 Measurement circuit connection image in verification of DDR IO PDN

3. Recommended IO setting and PCB configuration

3.1 Signal lines of high-speed DDR IF signals

PCB topology of each signal groups are shown in Section 3.1.1 to 3.1.9.

Transmission line impedance in each figure of topology shows target characteristic impedance which we recommend. IO setting and IBIS model to be used in each signal is summarized in section 3.1.1.

3.1.1 Summary of recommended IO settings

LSI IBIS models for recommended IO setting described before are listed in the following tables: Table 3.1, Table 3.2 and Table 3.3. Proper DRAM model must be selected based on materials provided by DRAM vender.

Table 3.1 Recommended setting of LSI IBIS and DRAM IO model in CA

Pin name	Recommended setting		
	LSI IBIS model	DRAM IO model setting	Rank
CK/CK#	ck_dl4_60	ODT = 60 ohm	1
		ODT = 60 ohm (Rank0 side) ODT = OFF (Rank1 side)	2
CA	mal4drv20_dl4_60	ODT = 60 ohm	1
		ODT = 60 ohm (Rank0 side) ODT= OFF (Rank1 side)	2
CS	mal4drv20_dl4_60	ODT = 60 ohm	1, 2
CKE	cke_dl4	input	1, 2
RESET_N	reset_dl4	input	1, 2

Table 3.2 Recommended setting of LSI IBIS and DRAM IO model in DQ Write mode

Pin name	Recommended setting		
	LSI IBIS model	DRAM IO model setting	Rank
DQS/DQS#	mal4drv27_dl4_40	ODT = 40 ohm	1
		ODT = 40 ohm (access side) ODT= OFF (non-access side)	2
DQ/DM	mal4drv27_dl4_40	ODT = 40 ohm	1
		ODT = 40 ohm (access side) ODT= OFF (non-access side)	2

Table 3.3 Recommended setting of LSI IBIS and DRAM IO model in DQ Read mode

Pin name	Recommended setting		
	LSI IBIS model	DRAM IO model setting*1	Rank
DQS/DQS#	mal4drv27_dl4_odt40	RONPD = 40 ohm, LSI ODT = 40 ohm, VOH = VDDQ / 3	1
		RONPD = 40ohm, VOH = VDDQ / 3 (access side) ODT = OFF (non-access side) LSI ODT = 40 ohm (both side)	2
DQ/DM	mal4drv27_dl4_odt40	RONPD = 40 ohm, LSI ODT = 40 ohm, VOH=VDDQ / 3	1
		RONPD = 40 ohm, VOH = VDDQ / 3 (access side) ODT = OFF (non-access side) LSI ODT = 40 ohm (both side)	2

Note 1. VOH is the setting of pull-up calibration point. LSI ODT is the setting of controller ODT value for VOH calibration of DRAM.

3.1.2 DQS/DQS#

Table 3.4 DQS/DQS# setting

Command	LSI		DRAM		Number of Rank	LSI IBIS model
	Driver setting	ODT	Driver setting	ODT		
Write	40 ohm	OFF	OFF	40 ohm	1	mal4drv27_dl4_40
				40 ohm (access side) OFF (non-access side)	2	
Read	OFF	40 ohm	RONPD = 40 ohm LSI ODT = 40 ohm VOH = VDDQ / 3	OFF	1	mal4drv27_dl4_40
				OFF (access side) OFF (non-access side)	2	

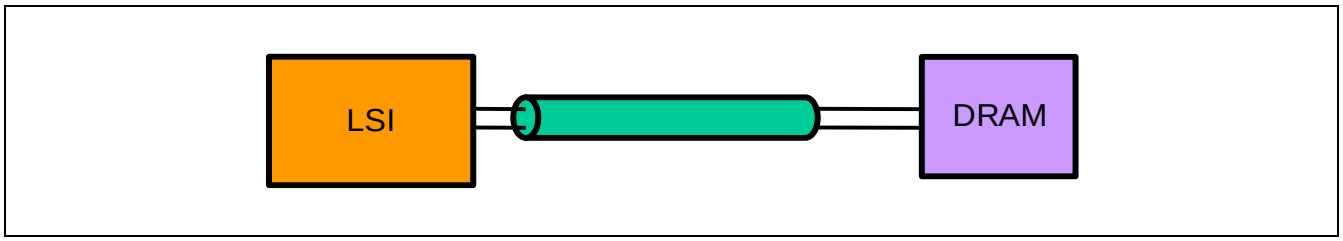

Figure 3.1 DQS/DQS# PCB topology

3.1.3 DQ/DM

Table 3.5 DQ/DM setting

Command	LSI		DRAM		Number of Rank	LSI IBIS model
	Driver setting	ODT	Driver setting	ODT		
Write	40 ohm	OFF	OFF	40 ohm	1	mal4drv27_dl4_40
				40 ohm (access side) OFF (non-access side)	2	
Read	OFF	40 ohm	RONPD = 40 ohm LSI ODT = 40 ohm VOH = VDDQ / 3	OFF	1	mal4drv27_dl4_odt40
				OFF (access side) OFF (non-access side)	2	

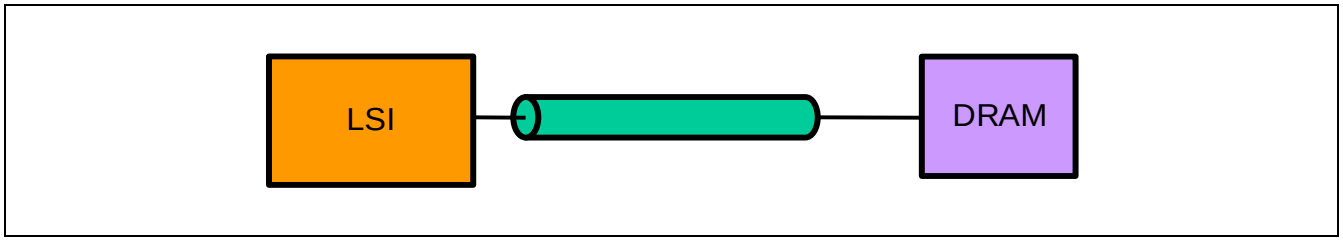

Figure 3.2 DQ/DM PCB topology

3.1.4 CK/CK#

Table 3.6 CK/CK# setting

Command	LSI	DRAM		LSI IBIS model

	Driver setting	ODT	Driver setting	ODT	Number of Rank	
Write / Read	60 ohm	–	–	60 ohm	1	ck_dl4_60
				60 ohm (Rank 0 side) OFF (Rank 1 side)	2	

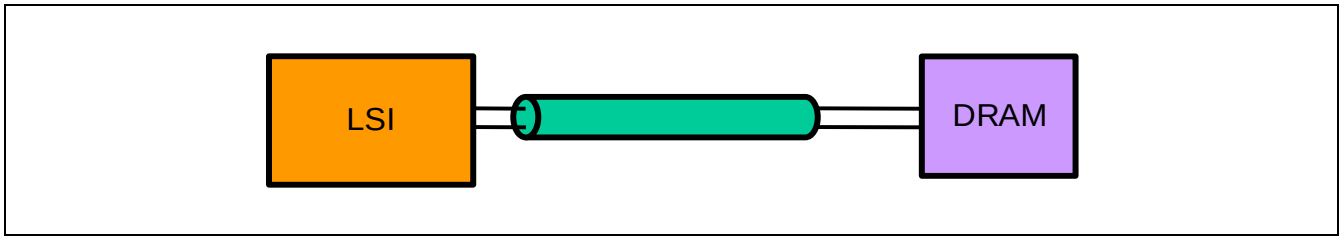

Figure 3.3 CK/CK# PCB topology

3.1.5 CA

Table 3.7 CA setting

Command	LSI		DRAM		Number of Rank	LSI IBIS model
	Driver setting	ODT	Driver setting	ODT		
Write / Read	60 ohm	–	–	60 ohm	1	mal4drv20_dl4_60
				60 ohm (Rank 0 side) OFF (Rank 1 side)	2	

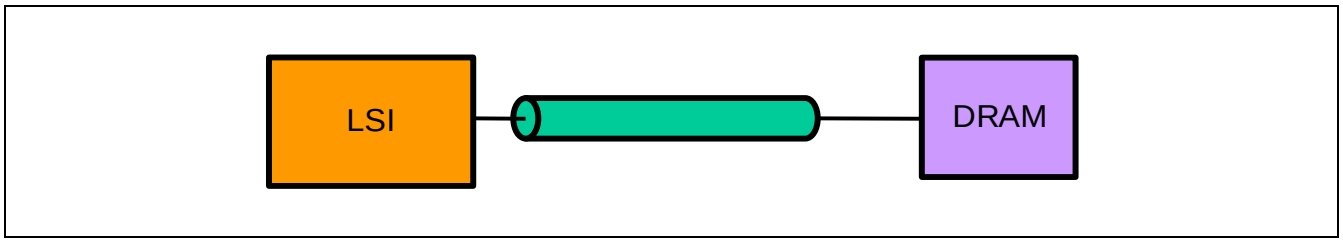

Figure 3.4 CA PCB topology

3.1.6 CS

Table 3.8 CS setting

Command	LSI		DRAM		Number of Rank	LSI IBIS model
	Driver setting	ODT	Driver setting	ODT		
Write / Read	60 ohm	–	–	60 ohm	1, 2	mal4drv20_dl4_60

Note: If the configuration is 2 ranks, the ODT for CS of rank 1 needs to be enabled.

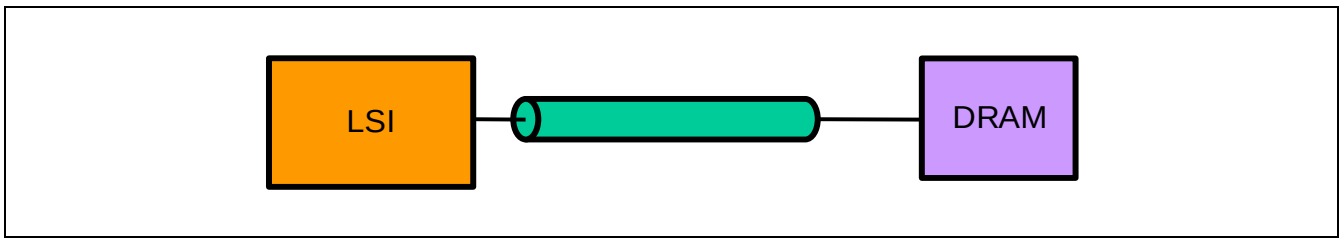

Figure 3.5 CS PCB topology

3.1.7 CKE

Table 3.9 CKE setting

Command	LSI		DRAM		Series resistor	Number of Rank	LSI IBIS model
	Driver setting	ODT	Driver setting	ODT			
Power Down	Fix	—	—	—	22 ohm	1, 2	cke_dl4

Note: Please confirm the DRAM vendor for IBIS model of DRAM.

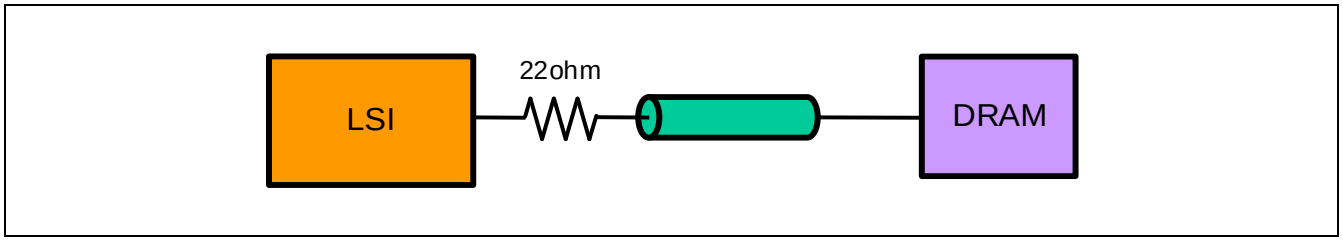

Figure 3.6 CKE PCB topology

3.1.8 RESET_N

Table 3.10 RESET_N setting

Command	LSI		DRAM		Series resistor	Number of Rank	LSI IBIS model
	Driver setting	ODT	Driver setting	ODT			
Reset	Fix	-	-	-	-	1, 2	reset_dl4

Note: Please confirm the DRAM vendor for IBIS model of DRAM.

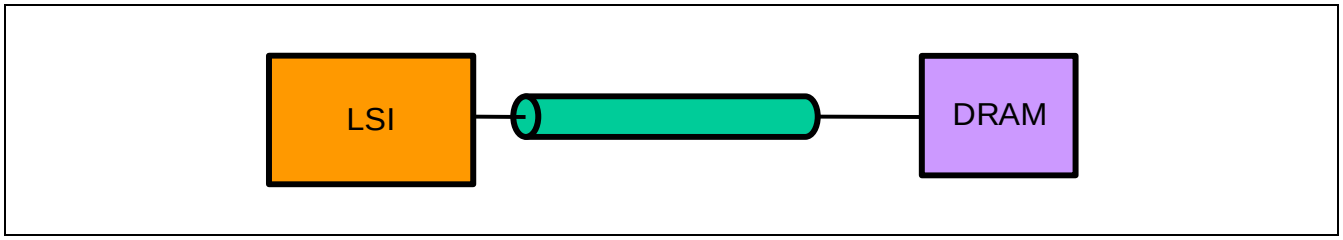

Figure 3.7 RESET_N PCB topology

3.1.9 ODT_CA_A/B of DRAM

Table 3.11 ODT_CA pins connection

Command	LSI		DRAM		LSI IBIS model
	Driver setting	ODT	Driver setting	ODT	
Any	None	None	—	—	No need. (Directly connected to VDDQ)

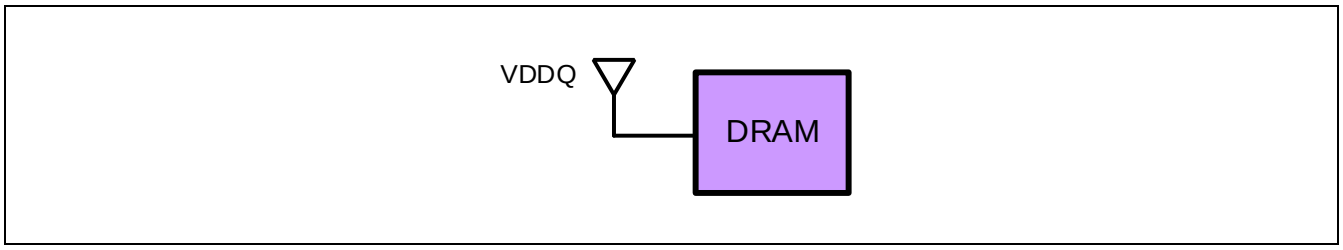

Figure 3.8 ODT_CA PCB topology

3.2 Other signal lines

3.2.1 ZN

Figure 3.9 shows a circuit diagram of external parts for ZN.

External resistor is connected between ZN and GND on LSI side. Please care of the difference between LSI and DRAM resistance connection of ZN.

Noise to ZN must be managed because ZN is analog signal.

Please follow the datasheet of JEDEC and DRAM vender about ZN resistance for DRAM.

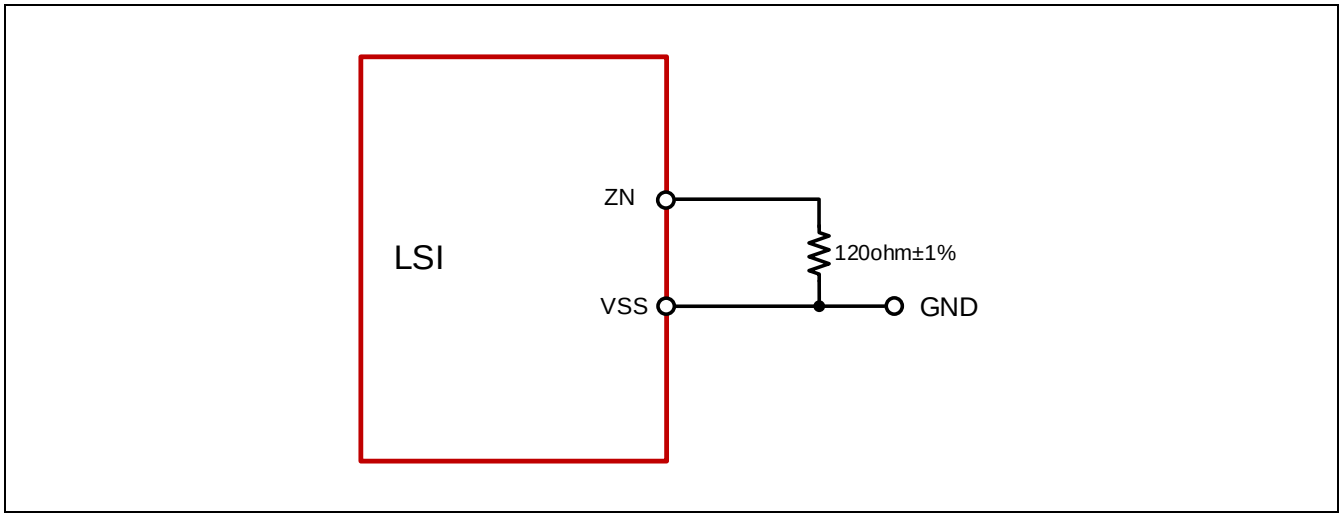

Figure 3.9 Circuit diagram of external parts for ZN

3.3 Power supply configuration

3.3.1 IO power supply (DDR_VDDQ)

Figure 3.10 shows a circuit diagram of IO power supply and external parts.

Power supply impedance of your PCB must be lower than target impedance for DDR IO power supply. Please refer to chapter 5 about target impedance and verification method.

Please confirm the DRAM vendor for circuit diagram and target impedance of DRAM power supply.

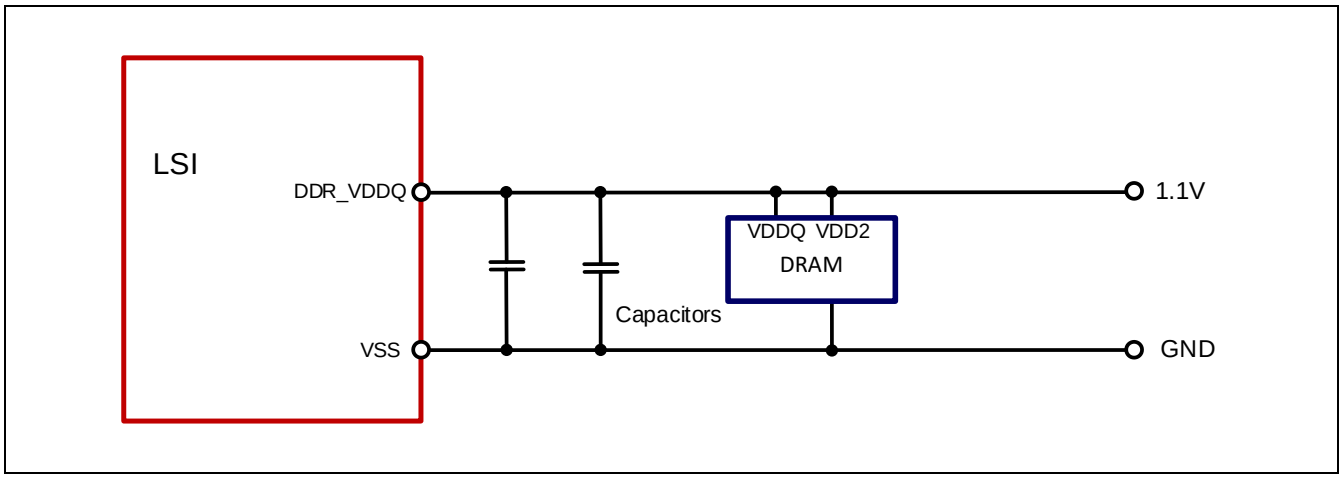

Figure 3.10 Circuit diagram of IO power supply and external parts

3.3.2 PLL power supply (DDR_VAA)

Figure 3.11 shows a circuit diagram image of PLL power supplies (DDR_VAA) and external parts that compose a low pass filter.

The external parts must be placed near LSI pin. Please refer to Table 3.12 to determine FB1,C1,C2 and C3 value. Filter is strongly recommended because PLL is very sensitive for power noise. Each PLL power supply consumes 7mA on maximum condition. The Ferrite bead FB1 must be able to flow this maximum current.

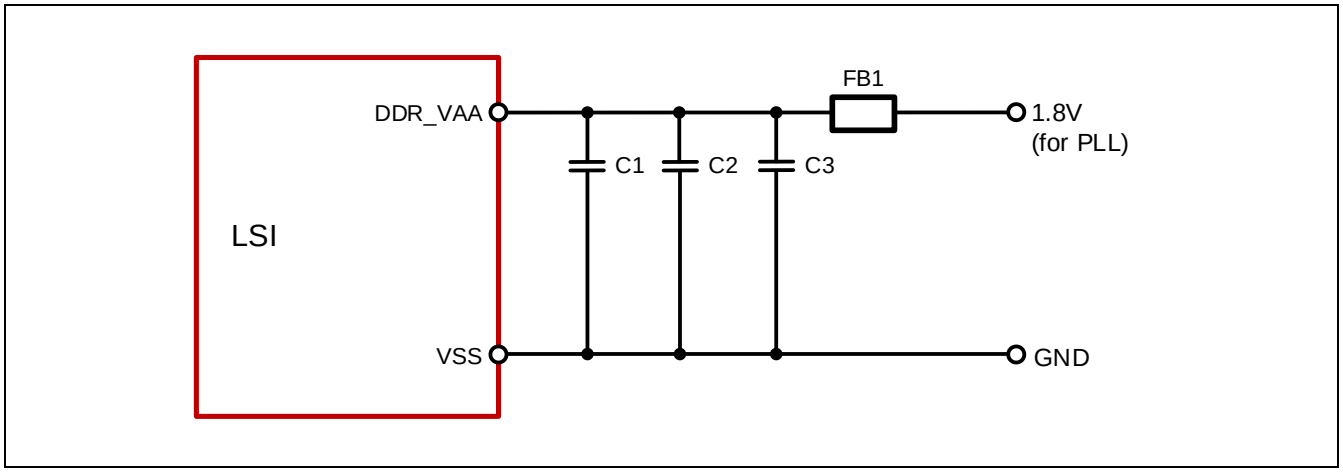

Figure 3.11 Circuit diagram of PLL power supply and external parts

Table 3.12 PLL power supply parts list

Item	Parts		Placement	Number	Value	Range	Size[*1]
DDR_VAA	C1	Ceramic capacitor	Less than 2mm from PKG edge	1	0.1uF	+-10%	1005
	C2	Ceramic capacitor	Less than 2mm from PKG edge	1	1.0uF	+-10%	1005
	C3	Ceramic capacitor	Less than 5mm from PKG edge	1	10uF	+-20%	2012
	FB1	Ferrite Bead	—	1	75ohm - 150ohm (@100MHz)	—	1005

Note 1. You can use the ones smaller than the size that has been described.

4. Verification items and method of signal lines

The verification of signal line includes restrictions of skew, flight-time, timing, and waveform. Items and method of these restrictions are described in this chapter.

Simulation condition for skew restriction and flight-time restriction are only in typical condition whereas the others are simulated in typical and corner conditions.

4.1 Verification items

4.1.1 Skew restrictions

Table 4.1 shows skew restrictions and Table 4.2 shows wiring length adjustment condition. Measurement method of each restriction is described in section 4.2.1. Each item in Table 4.1 and Table 4.2 needs to be verified in accordance with section 4.2.1.

Table 4.1 Skew restrictions

Mode	Target signal groups	Reference signal groups	Skew restriction value 3200 Mbps		Unit	Notes
			Min	Max		
Write	DQS/DQS#	CK/CK#	-125	62.5	ps	*1
Write/Read	CA	CK/CK#	-60	60	ps	*1, *6
Write/Read	CS	CK/CK#	-50	50	ps	*1, *6
Write/Read	CKE	CK/CK#	-312.5	312.5	ps	*1
Write/Read	same CA group		—	20	ps	*1, *2, *3
Write	DQ/DM	DQS/DQS#	-35	35	ps	*1
Write	DQx	DQy	—	35	ps	*1, *4
Read	DQ/DM	DQS/DQS#	-35	35	ps	*1
Read	DQx	DQy	—	35	ps	*1, *4

Table 4.2 Recommendation value of skew between differential signals

Mode	Target signal groups	Reference signal groups	Skew value 3200 Mbps		Unit	Notes
			Min	Max		
Write/Read	CK#	CK	-1	1	ps	*1, *5
Write	DQS#	DQS	-1	1	ps	*1, *5
Read	DQS#	DQS	-1	1	ps	*1, *5

Note 1. Skew restrictions value doesn't include ISI, Xtalk jitter.

Note 2. This restriction is applied in same CA group. Formula is Max delay – Min delay.

Note 3. Refer to Table 4.6 for CA group.

Note 4. This restriction is applied between two DQs in a byte. DM/DBI is included in these DQs.
Formula is Max delay – Min delay.

Note 5. These values are the recommended value to prevent from violating the VIX spec.
Differential signals are recommended the same wiring length as much as possible.

Note 6. Refer to Table 4.5.

4.1.1.1 Combination of measurement signals

Following tables show combination of measurement signals for skew restrictions.

Table 4.3 Skew between DQS and CK (tDQSS)

Target LSI pin names (DQS/DQS#)	Reference LSI pin names (CK/CK#)
DDR_DQSA_T0 / DDR_DQSA_C0 DDR_DQSA_T1 / DDR_DQSA_C1	DDR_CKA_T / DDR_CKA_C
DDR_DQSB_T0 / DDR_DQSB_C0 DDR_DQSB_T1 / DDR_DQSB_C1	DDR_CKB_T / DDR_CKB_C

Table 4.4 Skew between CK/CK#

Target LSI pin names (CK#)	Reference LSI pin names (CK)
DDR_CKA_C	DDR_CKA_T
DDR_CKB_C	DDR_CKB_T

Table 4.5 Skew between CA/CS and CK

Target LSI pin names (CA/CS)	Reference LSI pin names (CK/CK#)
DDR_CAA[5:0]	DDR_CKA_T / DDR_CKA_C
DDR_CSA[1:0]	
DDR_CAB[5:0]	DDR_CKB_T / DDR_CKB_C
DDR_CSB[1:0]	

Table 4.6 Skew in the same CA groups

Groups	LSI pin names
A	DDR_CAA[1:0]
B	DDR_CAA[5:2]
C	DDR_CAB[1:0]
D	DDR_CAB[5:2]

Table 4.7 Skew between CKE and CK

Target LSI pin names (CKE)	Reference LSI pin names (CK/CK#)
DDR_CKEA[1:0]	DDR_CKA_T / DDR_CKA_C
DDR_CKEB[1:0]	DDR_CKB_T / DDR_CKB_C

Table 4.8 Skew between DQS/DQS# (Write/Read)

Target LSI pin names	Reference LSI pin names
DDR_DQSA_C0	DDR_DQSA_T0
DDR_DQSA_C1	DDR_DQSA_T1
DDR_DQSB_C0	DDR_DQSB_T0
DDR_DQSB_C1	DDR_DQSB_T1

Table 4.9 Skew between DQ/DM and DQS (Write/Read)

Target LSI pin names	Reference LSI pin names
DDR_DQA[7:0], DDR_DMIA0	DDR_DQSA_T0 / DDR_DQSA_C0
DDR_DQA[15:8], DDR_DMIA1	DDR_DQSA_T1 / DDR_DQSA_C1
DDR_DQB[7:0], DDR_DMIB0	DDR_DQSB_T0 / DDR_DQSB_C0
DDR_DQB[15:8], DDR_DMIB1	DDR_DQSB_T1 / DDR_DQSB_C1

Table 4.10 Skew between DQx and DQy (Write/Read)

Target LSI pin names	Reference LSI pin names
DDR_DQA[7:0], DDR_DMIA0	DDR_DQA[7:0], DDR_DMIA0
DDR_DQA[15:8], DDR_DMIA1	DDR_DQA[15:8], DDR_DMIA1

DDR_DQB[7:0], DDR_DMIB0	DDR_DQB[7:0], DDR_DMIB0
DDR_DQB[15:8], DDR_DMIB1	DDR_DQB[15:8], DDR_DMIB1

4.1.2 Flight-time restrictions

Table 4.11 shows flight-time restrictions. Measurement method of the restriction is described in section 4.2.2. The item in Table 4.11 needs to be verified in accordance with section 4.2.2. This restriction is necessary to keep through put of DDR-IF.

Table 4.11 Flight-time restriction

Restriction item	Restriction value	Unit	Note
Flight-time	0 - 1.0	ns	*1

Note 1. Flight-time restrictions value doesn't include ISI, Xtalk jitter.

4.1.2.1 Combination of measurement signals

The following table shows combination of measurement LSI pin names for Flight-time.

Table 4.12 Flight-time

No.	CK_delay	DQS_delay
1	DDR_CKA_T / DDR_CKA_C	DDR_DQSA_T0 / DDR_DQSA_C0
2	DDR_CKA_T / DDR_CKA_C	DDR_DQSA_T1 / DDR_DQSA_C1
3	DDR_CKB_T / DDR_CKB_C	DDR_DQSB_T0 / DDR_DQSB_C0
4	DDR_CKB_T / DDR_CKB_C	DDR_DQSB_T1 / DDR_DQSB_C1

4.1.3 Timing restrictions

Table 4.13 shows timing restrictions based on LSI timing budgets. Measurement method of each item is described in section 0. Each item in Table 4.13 needs to be verified in accordance with section 00.

Table 4.13 Timing restrictions

Category	Verification Item	JEDEC Standard to be referred	JEDEC Spec. *1 LPDDR4-3200		Timing Restriction LPDDR4-3200		Unit
			Min	Max	Min	Max	
DQ/DM	Write DQ eye degradation	tdIVW_total	—	78.125	—	106	ps
	Read DQ eye degradation	tQW	—	93.75	—	126	ps
	DQ Input pulse width degradation (At Vcent_DQ) *4	tdIPW DQ	—	140.625	—	88.8	ps
DQS/DQS#	DQS input low/high pulse width degradation	tDQSL / tDQSH	-62.5	62.5	-6.25	6.25	ps
	Jitter of DQS referred to CK rise edge	tDQSS	468.75	781.25	-12.5	12.5	ps
CA	CA eye degradation	tcIVW	—	187.5	—	185	ps
	CA input pulse width degradation	TcIPW	—	375	—	130.5	ps
CS	CS eye degradation	tcIVW	—	187.5	—	185	ps
	CS input pulse width degradation	TcIPW	—	375	—	130.5	ps
CK/CK#	Average input clock period *2	tCK(avg)	0.625	100	0.625	1.25	ns
	Average High/Low pulse width degradation	tCH(avg)/ tCL(avg)	-25	25	-2.5	2.5	ps
	Clock High/Low pulse width degradation	tCH(abs)/ tCL(abs)	-43.75	43.75	-6.25	6.25	ps
	Clock period jitter *3	tJIT(per)	-40	40	-6.25	6.25	ps

Note 1. Please note that some of these names do not correspond to JEDEC standard because these are calculated as degradation of corresponding spec.

For example, tQW(min) is 0.70UI by JEDEC LPDDR4-3200, so degradation is 625*0.5*(1-0.70) = 93.75ps.

Note 2. This item shows the input data, trigger and clock period. Signaling rate in the verifications show in this table should be matched with actual data rate in your system.

Note 3. The restriction for tCK(abs) isn't specified in this table because tCK(abs) is calculated from tCK(avg)MIN and tJIT(per)MIN as described in JEDEC standard.

Note 4. If the timing restriction for tdIVW_tolal is satisfy, this restriction need not to satisfy.

4.1.4 Waveform restrictions

Table 4.14 shows waveform restrictions. Measurement method of these items are described in JEDEC standard. Each item in Table 4.14 needs to be verified in accordance with JEDEC standard. Only those of Rx Mask voltage p-p (for DQ and CA) is described in section 0. When violating it, please consult with RENESAS about the wave form restrictions. But when violating DRAM specifications, please consult with a DRAM vendor.

Table 4.14 Waveform restrictions

Category	Verification Item	JEDEC Standard to be referred	JEDEC Spec. LPDDR4-3200		Timing Restriction LPDDR4-3200		Unit
			Min	Max	Min	Max	
Write DQ/DM	DQ AC input pulse amplitude p-p	VIHL_AC	180	—	230	—	mV
	Rx Mask voltage p-p total	VdIVW_total	—	140	140	—	mV
	Input Slew Rate over VdIVW_total	SRIN_dIVW	1	7	2.0	6.6	V/ns
Write DQS/DQS#	DQS Differential input crosspoint voltage ratio	Vix_DQS_ratio	—	20	-9.0	9.0	%
	DQS differential input	Vindiff_DQS	360	—	460	—	mV
	DQS Differential Input Slew Rate	SRIdiff	2	14	2.6	13.4	V/ns
	DQS Single-Ended input voltage	Vinse_DQS	180	—	280	—	mV
	DQS Single-Ended input voltage High from VrefDQ	Vinse_DQS_High	90	—	140	—	mV
	DQS Single-Ended input voltage Low from VrefDQ	Vinse_DQS_Low	90	—	140	—	mV
Read DQ/DM	DQ AC input pulse amplitude p-p	VIHL_AC	—	—	230	—	mV
	Rx Mask voltage p-p total	VdIVW_total	—	—	140	—	mV
	Input Slew Rate over VdIVW_total *1	SRIN_dIVW	—	—	1.5	6.7	V/ns
Read DQS/DQS#	DQS Differential input crosspoint voltage ratio	Vix_DQS_ratio	—	—	-15	15	%
	DQS differential input	Vindiff_DQS	—	—	460	—	mV
	Differential Input High for slew rate	—	—	—	140	—	mV
	Differential Input Low for slew rate	—	—	—	—	-140	mV
	DQS Differential Input Slew Rate	SRIdiff	—	—	3.0	13.4	V/ns
CA/CS	CA/CS AC input pulse amplitude p-p	VIHL_AC	190	-	240	—	mV
	Rx Mask voltage p-p*2	VcIVW	—	155	155	—	mV
	Input Slew Rate over VcIVW_CA	SRIN_cIVW	1	7	2.0	6.4	V/ns
	Input Slew Rate over VcIVW_CS	SRIN_cIVW	1	7	2.0	6.4	V/ns
CK/CK#	CK Differential input crosspoint voltage ratio	Vix_CK_ratio	—	25	-9.6	13	%
	CK differential input voltage	Vindiff_CK	380	—	480	—	mV

	Differential Input Slew Rate for CK	SRIdiff_CK	2	14	2.6	13.4	V/ns
	CK Single-Ended input voltage	Vinse_CK	190	—	292	—	mV
	CK Single-Ended input voltage High from VrefCA	Vinse_CK_High	95	—	146	—	mV
	CK Single-Ended input voltage Low from VrefCA	Vinse_CK_Low	95	—	146	—	mV
DQ/DM, DQS/DQS#	Maximum peak amplitude allowed for overshoot area	Maximum peak amplitude for overshoot area	—	0.3	—	0.26	V
	Maximum peak amplitude allowed for undershoot area	Maximum peak amplitude for undershoot area	—	0.3	—	0.26	V
	Maximum overshoot area above VDD/VDDQ	Maximum overshoot area above VDD/VDDQ	—	0.1	—	0.087	V-ns
	Maximum undershoot area below VSS/VSSQ	Maximum undershoot area below VSS/VSSQ	—	0.1	—	0.087	V-ns
CA, CS, CK/CK#, CKE, RESET_N	Maximum peak Amplitude allowed for overshoot area	Maximum peak Amplitude allowed for overshoot area	—	0.35	—	0.31	V
	Maximum peak Amplitude allowed for undershoot area	Maximum peak Amplitude allowed for undershoot area	—	0.35	—	0.31	V
	Maximum overshoot area above VDD/VDDQ	Maximum overshoot area above VDD/VDDQ	—	0.8	—	0.787	V-ns
	Maximum undershoot area below VSS/VSSQ	Maximum undershoot area below VSS/VSSQ	—	0.8	—	0.787	V-ns
CKE, RESET_N	Input high level (AC) for CKE	VIH(AC)	0.75* VDDQ	VDDQ + 0.2	0.75* VDDQ	*3	V
	Input low level (AC) for CKE	VIL(AC)	-0.2	0.25*VDDQ	*4	0.25*VDDQ	V
	Input high level (DC) for CKE	VIH(DC)	0.65* VDDQ	VDDQ + 0.2	0.65* VDDQ	VDDQ + 0.2	V
	Input low level (DC) for CKE	VIL(DC)	-0.2	0.35*VDDQ	-0.2	0.35*VDDQ	V
	Input high level for RESET_N	VIH	0.80*VDDQ	VDDQ + 0.2	0.80*VDDQ	*3	V
	Input low level for RESET_N	VIL	-0.2	0.20*VDDQ	*4	0.20*VDDQ	V

p-p : Peak-to-Peak

Note 1. SRIN_dIVW = VdIVW_Total / (tr or tf), same as Write SRIN_dIVW.

Note 2. Refer to 4.2.4.1 Rx Mask voltage p-p (for DQ and CA).

Note 3. Refer Maximum peak Amplitude allowed for overshoot area.

Note 4. Refer Maximum peak Amplitude allowed for undershoot area.

4.2 Verification method

4.2.1 Method of skew restrictions

Skew restrictions shown in Table 4.1 are confirmed at DRAM PAD and LSI PAD. Delay from LSI PAD to DRAM PAD must be confirmed to satisfy skew restrictions described in Figure 4.1, which compensate the skew of PKG by adjusting PCB delay.

In verifying skew between differential and single-ended signals, it is necessary to remove IO buffer delay (named “basic delay”) to measure only interconnect skew.

Measurement method of basic delay is shown in Figure 4.2 and Figure 4.3.

Skew factors are assumed the following three items as described in section 1.4.

(1) Path mismatch

Delay time deviation caused by the LSI PKG and PCB trace length difference among signals.

(2) Inter-Symbol Interference (ISI)

(3) Xtalk jitter

Table 4.1 shows restrictions for (1) path mismatch. PCB design should be verified by using data pattern which causes no ISI and no Xtalk jitter. (2) and (3) are verified in timing restriction by using data pattern with ISI and Xtalk (refer to section 0). To eliminate the influence of ISI to the result of skew simulation, DQ/CA data frequency should be slow, for example 100MHz(10ns). On the other hand, the frequency for CK and DQS should be real operating frequency, for example the operating frequency 1.6GHz(625ps).

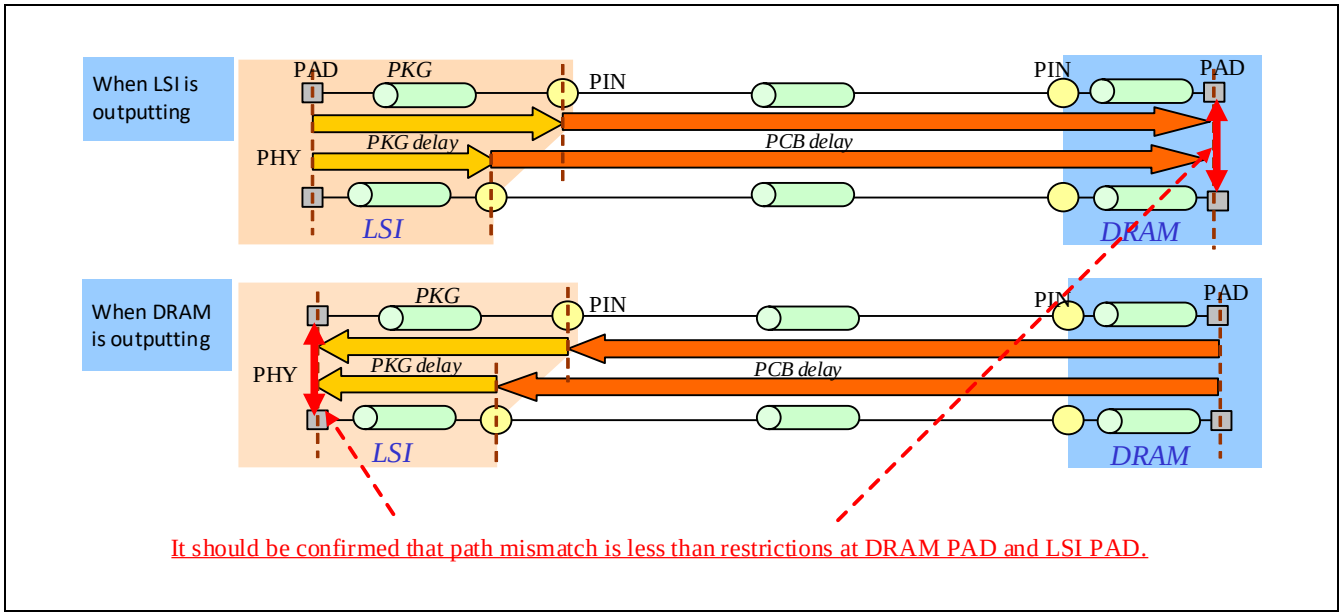

Figure 4.1 How to adjust path mismatch

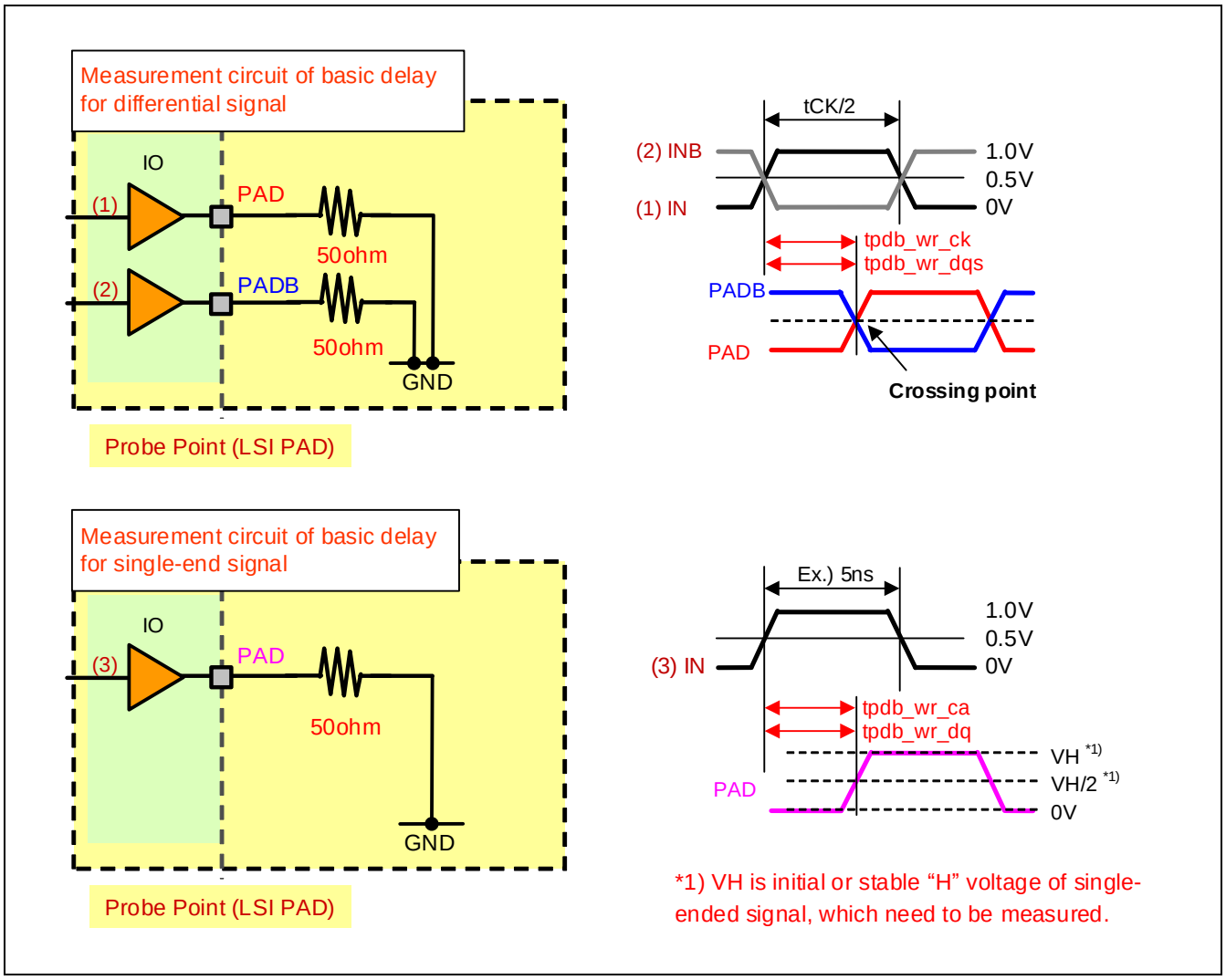

Figure 4.2 Measurement method of basic delay (Write)

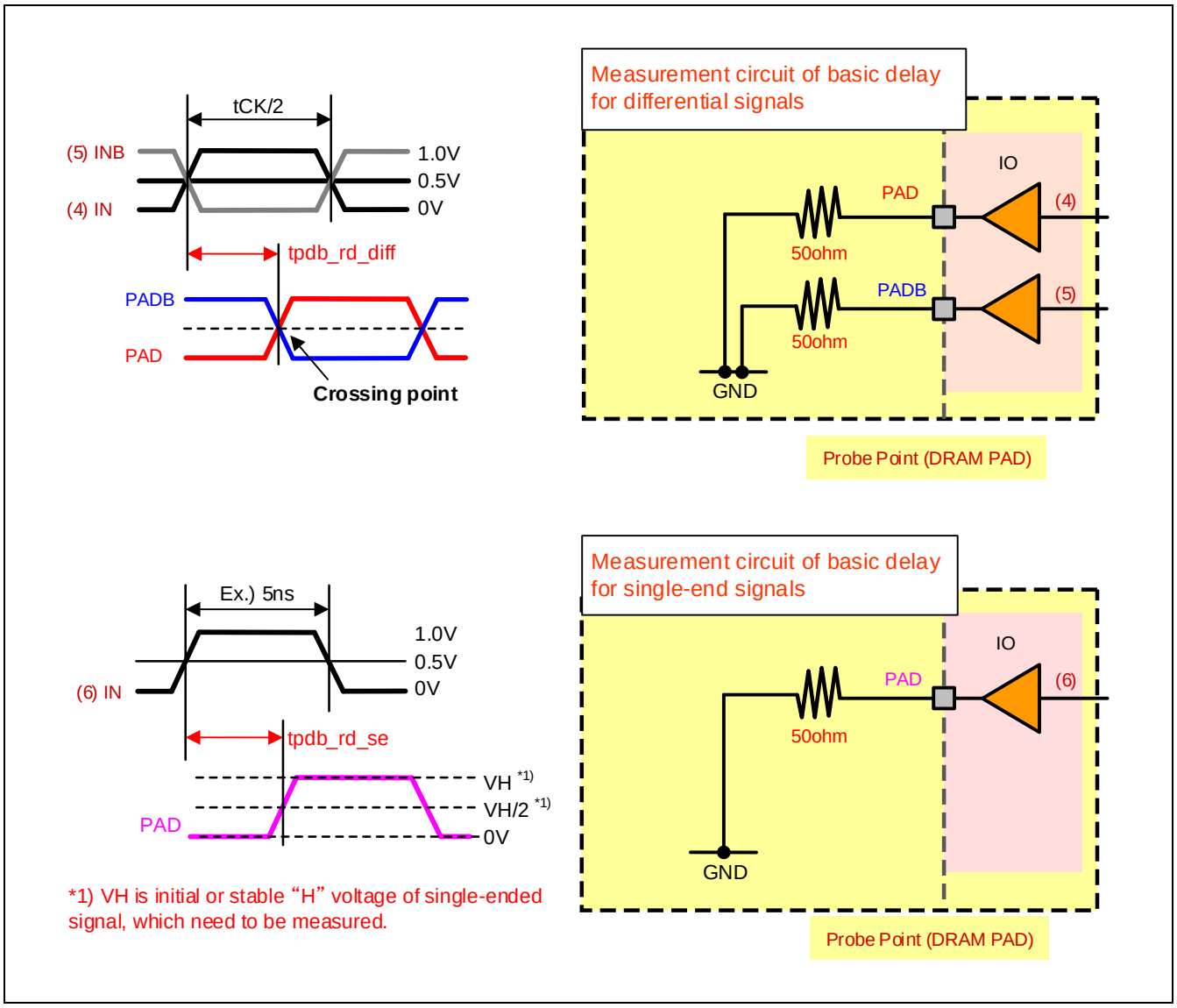

Figure 4.3 Measurement method of basic delay (Read)

4.2.1.1 Skew between DQS and CK (tDQSS)

Figure 4.4 shows the measurement circuit, input waveform to LSI IO buffer model, and measured waveform at DRAM PAD. DQS-CK skew should be smaller than the target specification shown in Table 4.1.

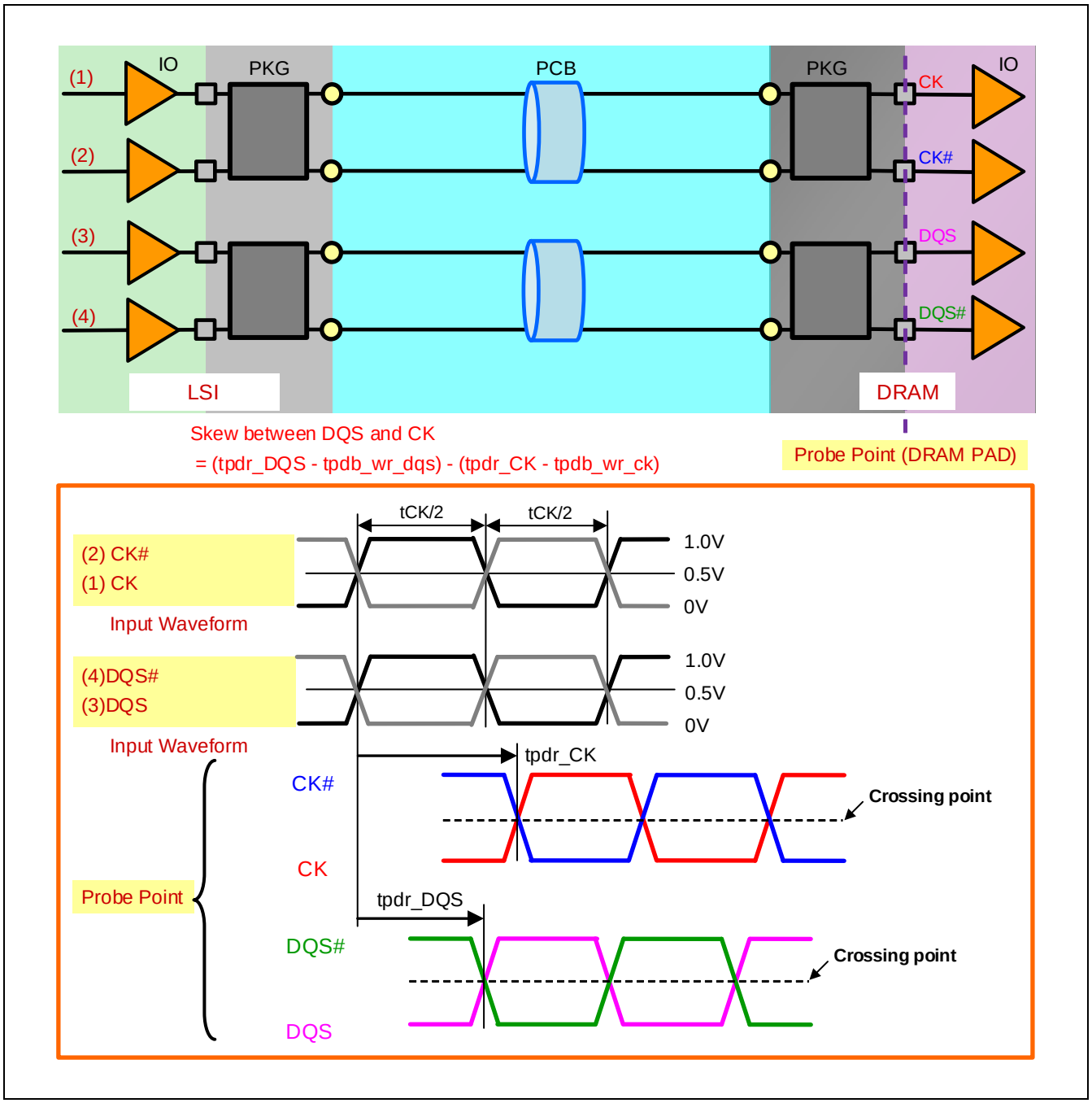

Figure 4.4 Measurement method of basic delay (Read)

4.2.1.2 Skew between CK/CK#

Figure 4.5 shows the measurement circuit, input waveform to LSI IO buffer model, and measured waveform at DRAM PAD. Skew between CK/CK# should be smaller than the target specification shown in Table 4.1.

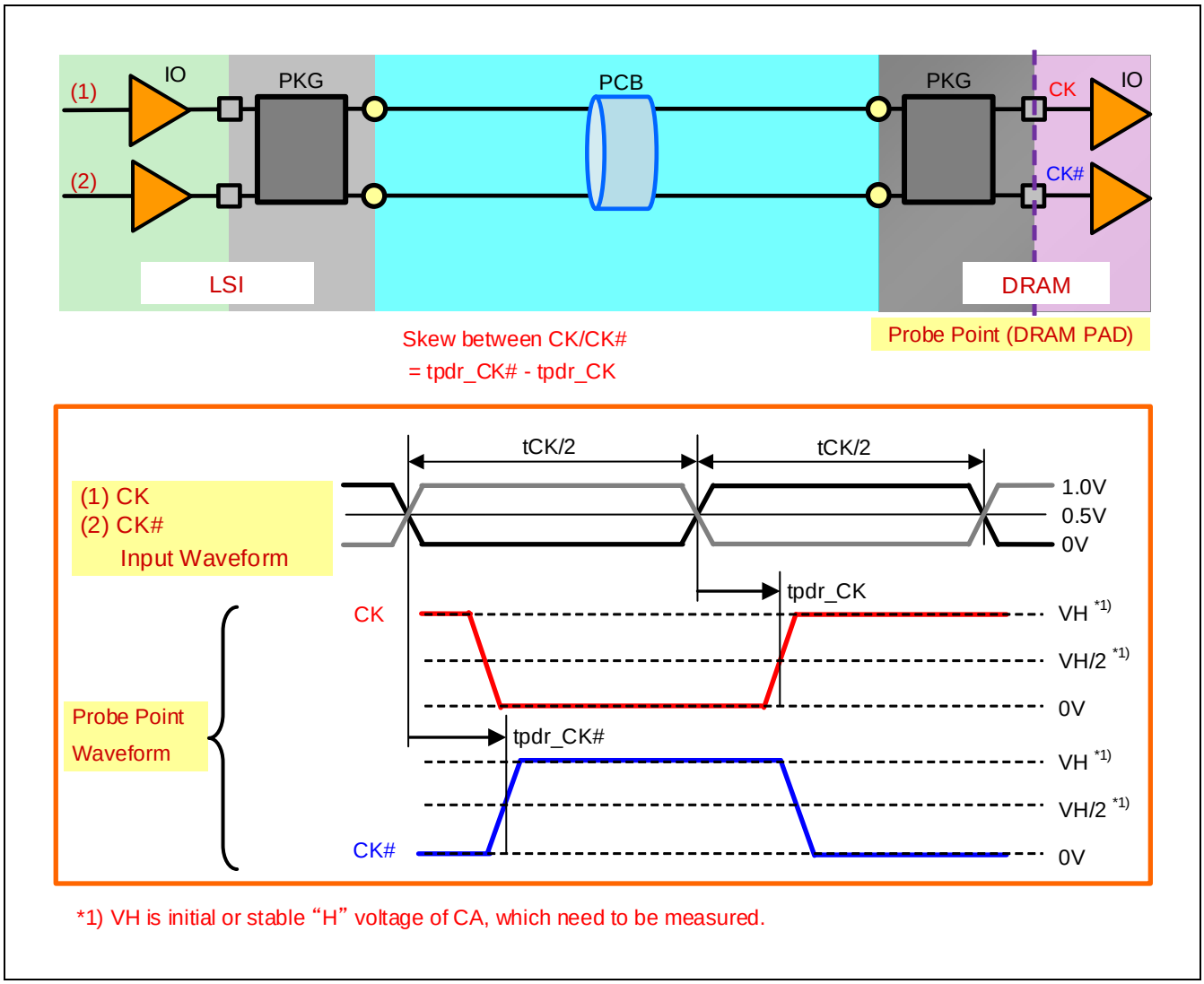

Figure 4.5 Measurement method of skew between CK/CK#

4.2.1.3 Skew between CA/CS and CK

Figure 4.6 shows the measurement circuit, input waveform to LSI IO model, and measured waveform at DRAM PAD. CA/CS-CK skew should be smaller than the target specification shown in Table 4.1. PCB design should be verified by using data pattern which causes no ISI and no Xtalk jitter.

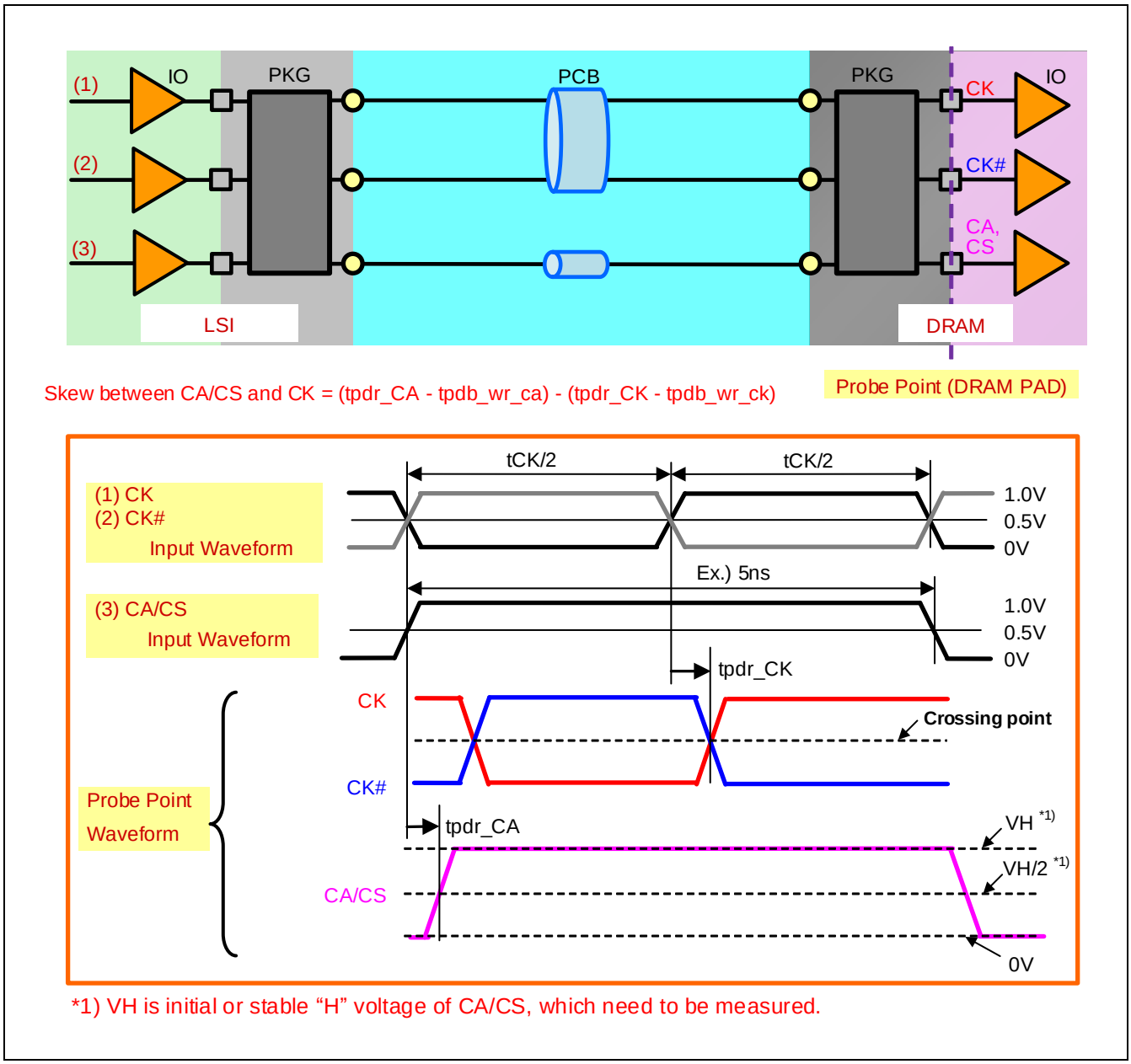

Figure 4.6 Measurement method of skew between CA/CS and CK

4.2.1.4 Skew in the same CA groups

Figure 4.7 shows the measurement circuit, input waveform to LSI IO buffer model, and measured waveform at DRAM PAD. CA skew should be smaller than the target specification shown in Table 4.1. When being different in a connected channel, it's necessary to keep the restrictions in the same group. PCB design should be verified by using data pattern which causes no ISI and no Xtalk jitter.

Note : Refer to Table 4.6 for CA groups.

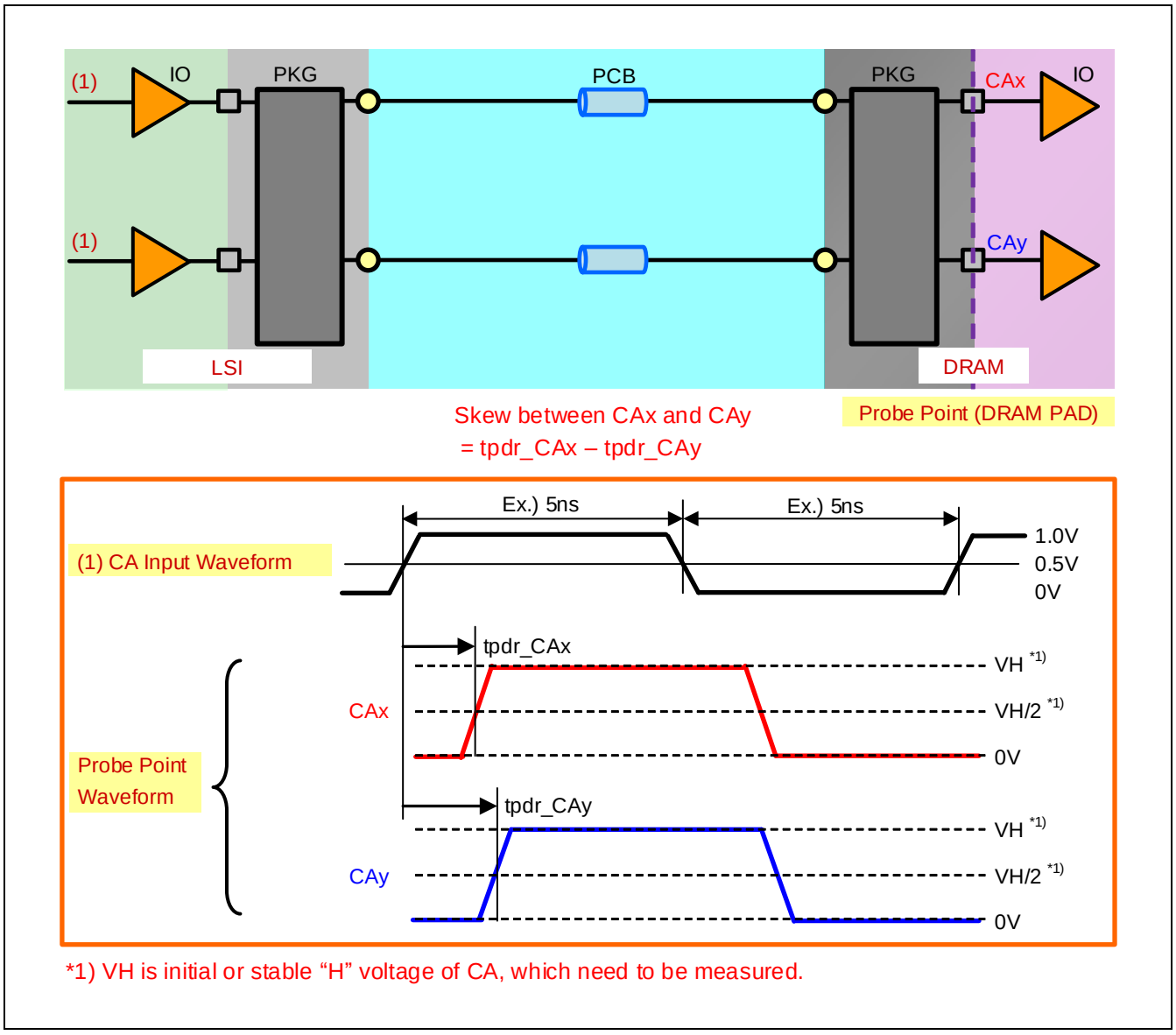

Figure 4.7 Measurement method of skew in the same CA groups

4.2.1.5 Skew between CKE and CK

Figure 4.8 shows the measurement circuit, input waveform to LSI IO buffer model, and measured waveform at DRAM PAD. CKE and CK skew should be smaller than the target specification shown in Table 4.1. PCB design should be verified by using data pattern which causes no ISI and no Xtalk jitter.

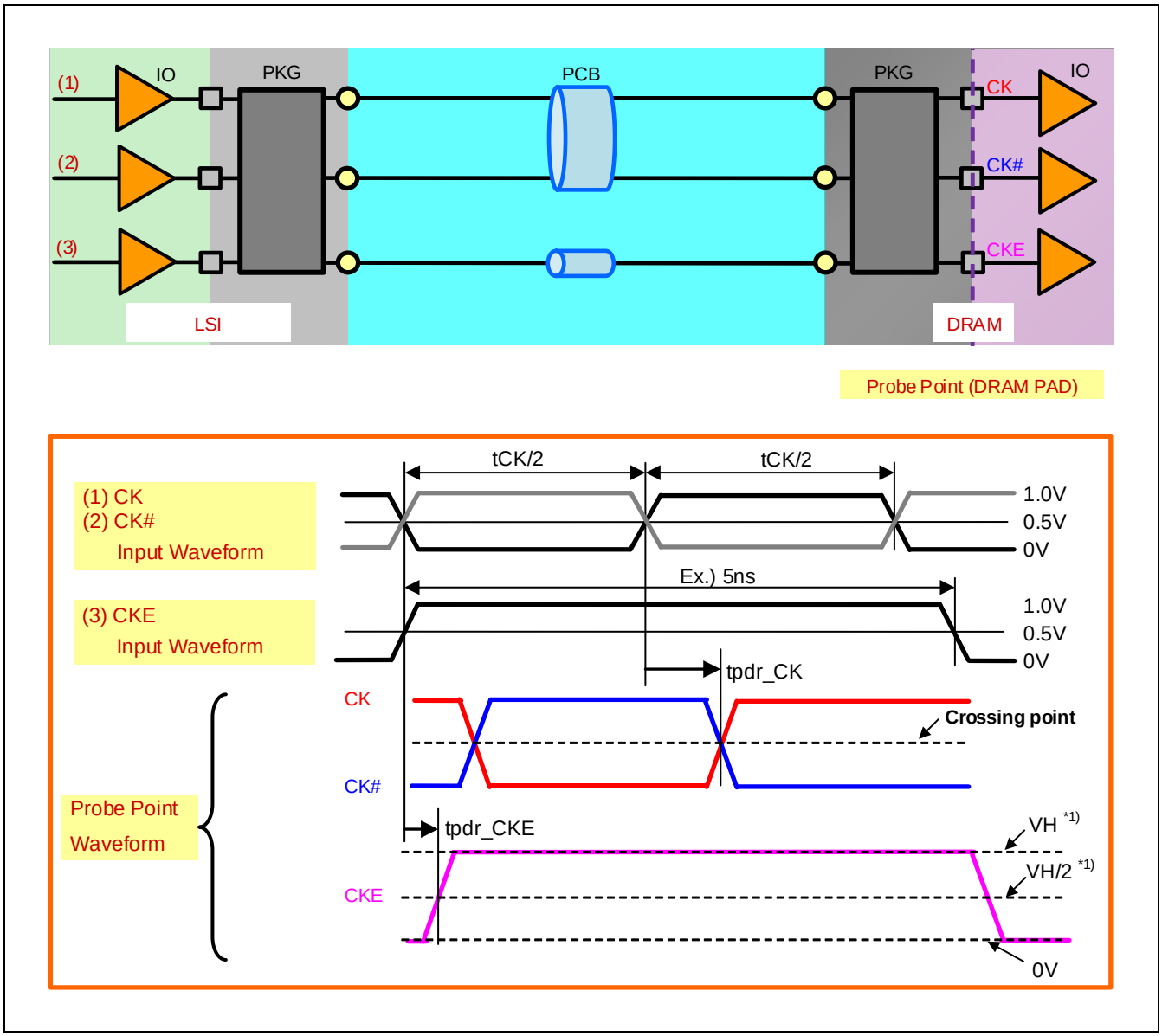

Figure 4.8 Measurement method of skew between CKE and CK

4.2.1.6 Skew between DQS/DQS# (Write)

Figure 4.9 shows the measurement circuit, input waveform to LSI IO buffer model, and measured waveform at DRAM PAD. Skew between DQS/DQS# in Write mode should be smaller than the target specification shown in Table 4.1.

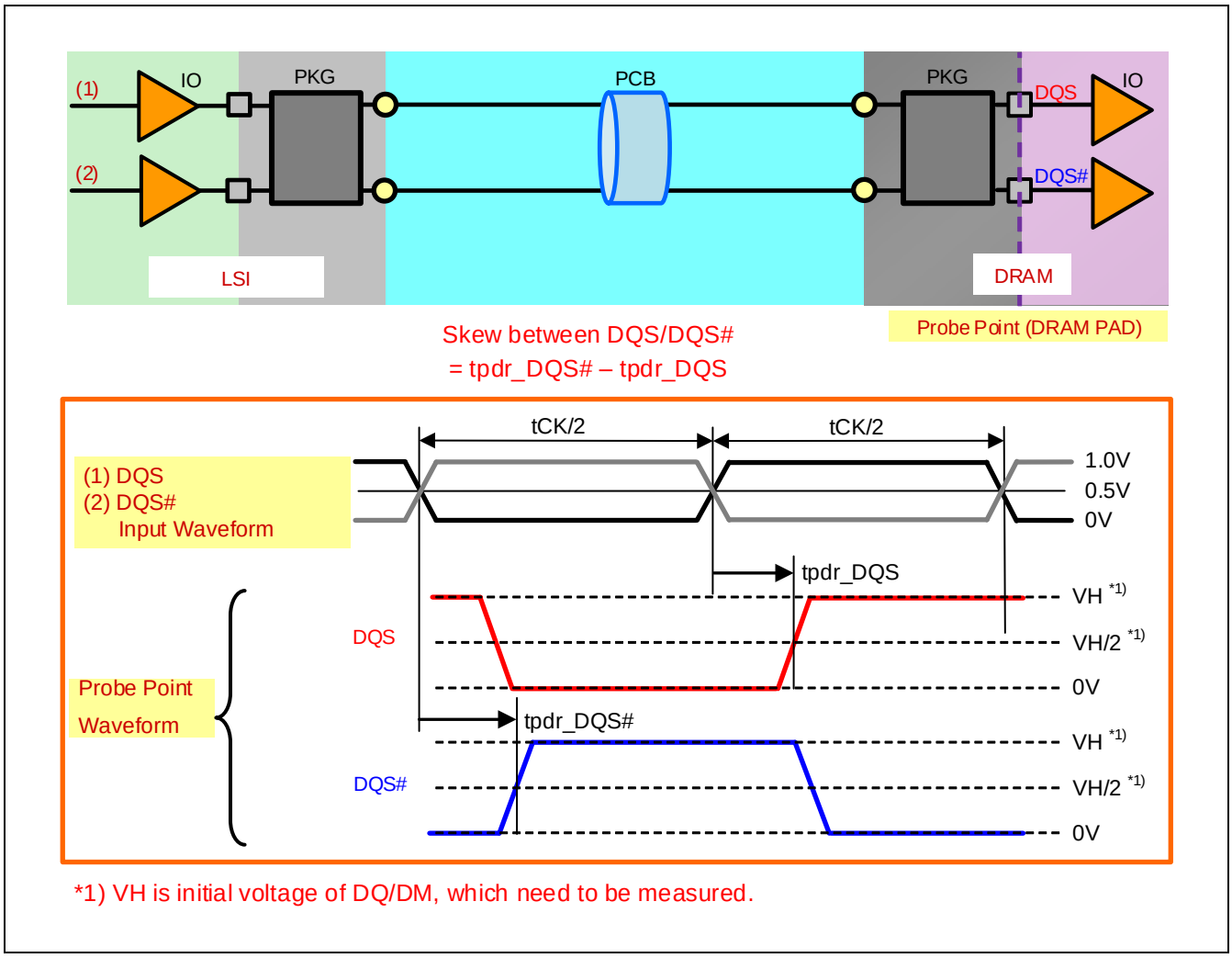

Figure 4.9 Measurement method of skew between DQS/DQS# (Write)

4.2.1.7 Skew between DQ/DM and DQS (Write)

Figure 4.10 shows the measurement circuit, input waveform to LSI IO model, and measured waveform at DRAM PAD in write mode. DQ/DM-DQS skew should be smaller than the target specification shown in Table 4.1. PCB design should be verified by using data pattern which causes no ISI and no Xtalk jitter.

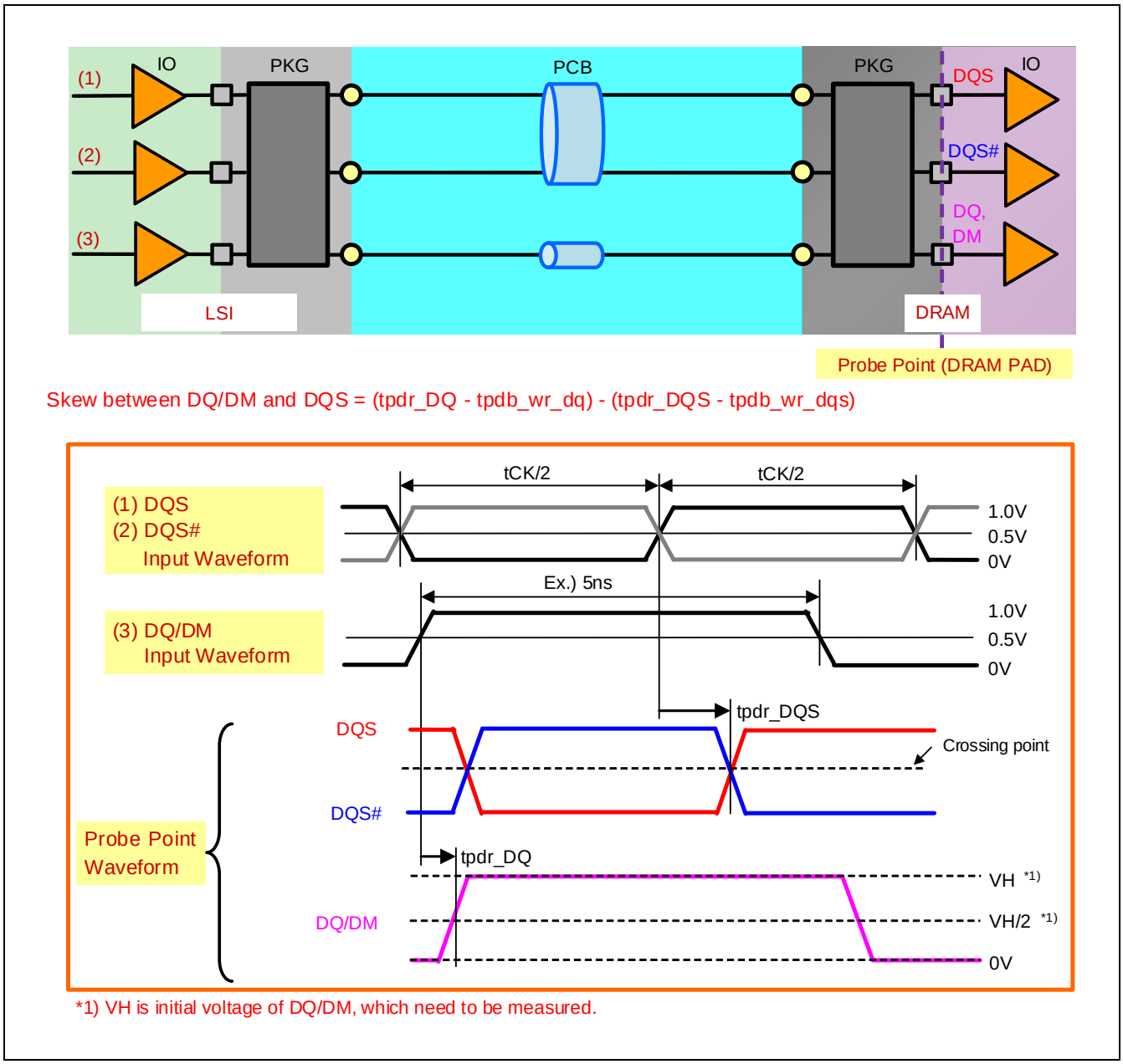

Figure 4.10 Measurement method of skew between DQ/DM and DQS (Write)

4.2.1.8 Skew between DQx and DQy (Write)

Figure 4.11 shows the measurement circuit, input waveform to LSI IO model and measured waveform at DRAM PAD in write mode. DQx/DQy skew should be smaller than the target specification shown in Table 4.1. PCB design should be verified by using data pattern which causes no ISI and no Xtalk jitter.

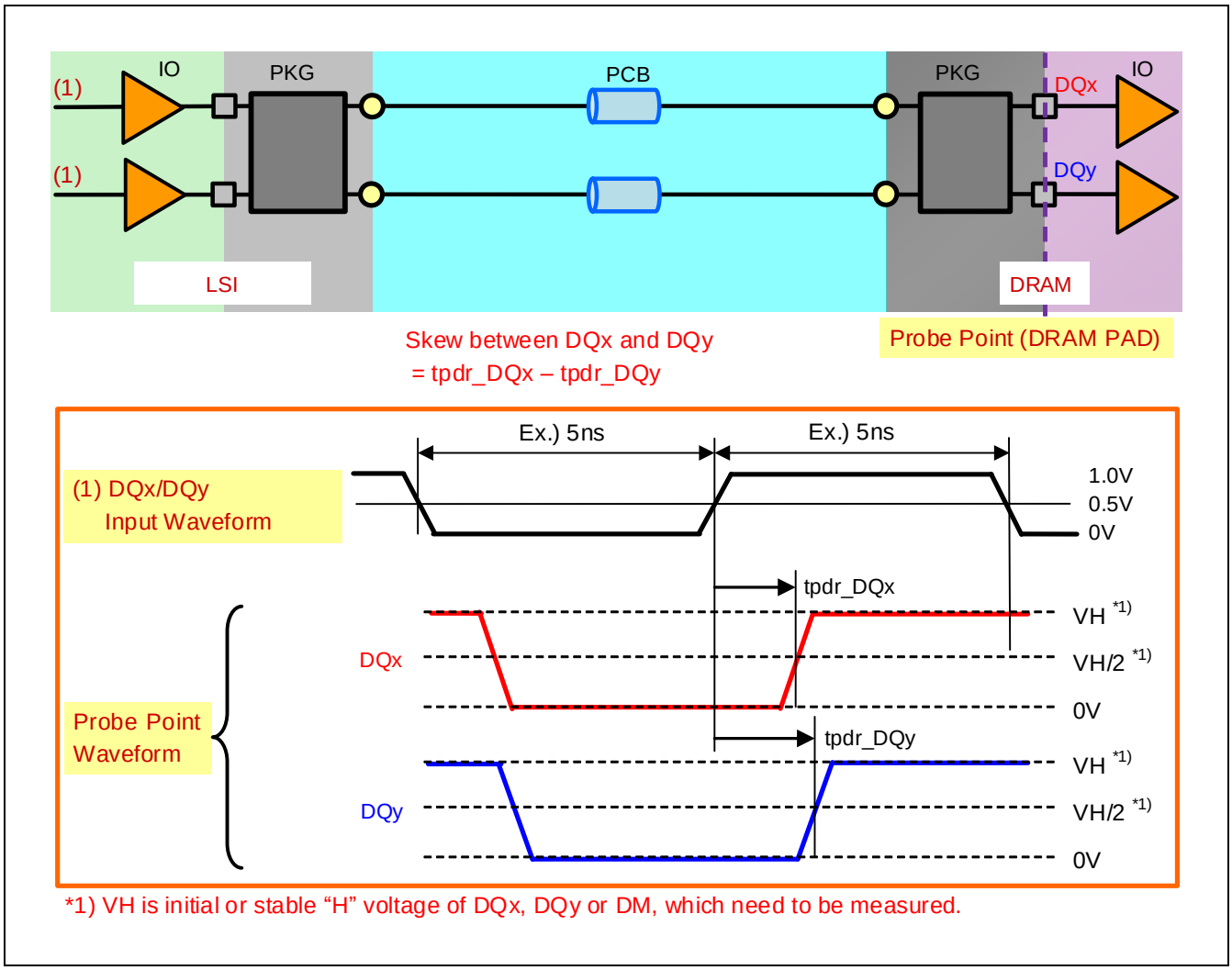

Figure 4.11 Measurement method of skew between DQx and DQy (Write)

4.2.1.9 Skew between DQS/DQS# (Read)

Figure 4.12 shows the measurement circuit, input waveform to DRAM IO model, and measured waveform at LSI PAD in read mode. DQS/DQS# skew should be smaller than the target specification shown in Table 4.1.

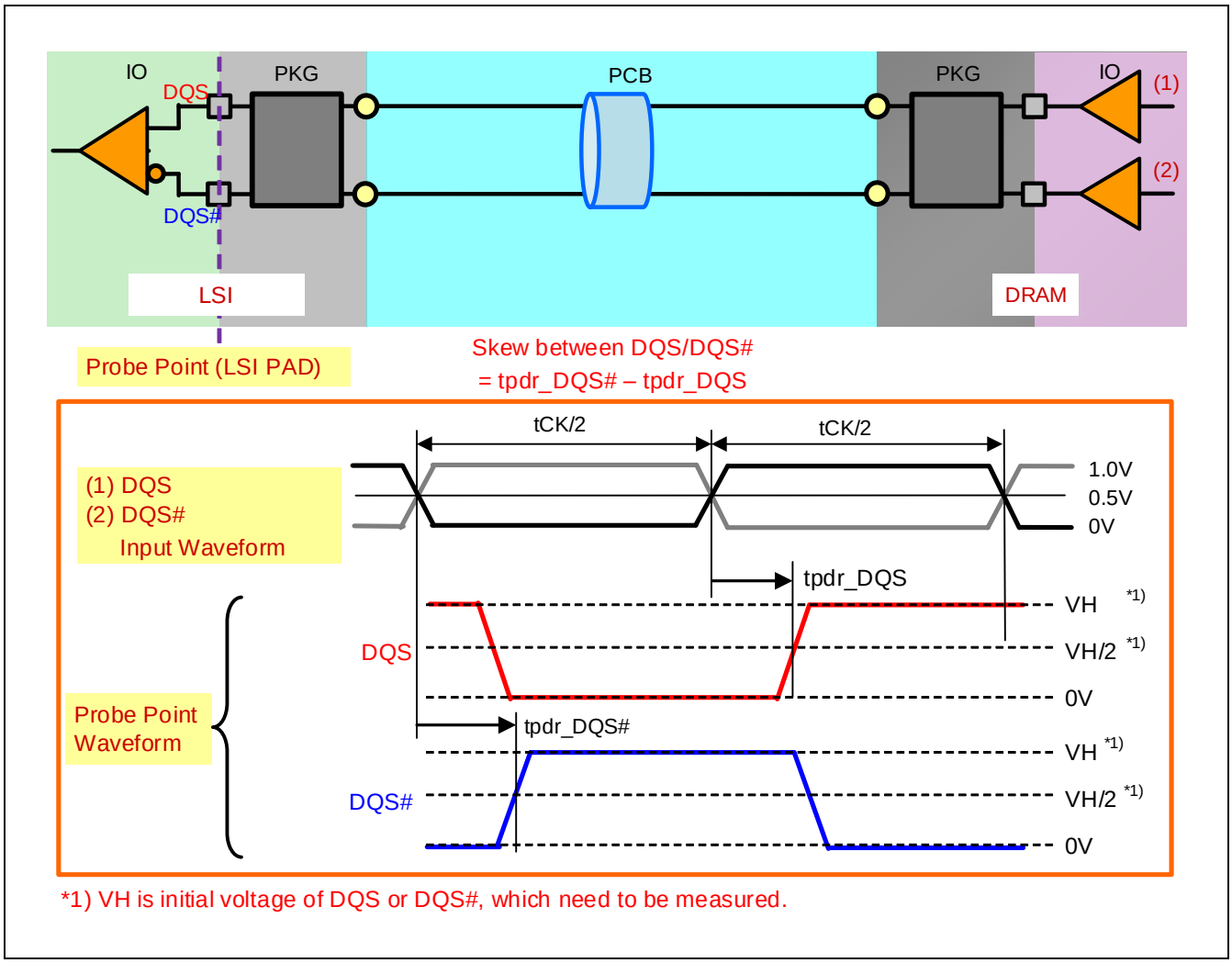

Figure 4.12 Measurement method of skew between DQS/DQS# (Read)

4.2.1.10 Skew between DQ/DM and DQS (Read)

Figure 4.13 shows the measurement circuit, input waveform of DRAM IO model and measured waveform at LSI PAD in read mode. DQ/DM-DQS skew should be smaller than the target specification shown in Table 4.1. PCB design should be verified by using data pattern which causes no ISI and no Xtalk jitter.

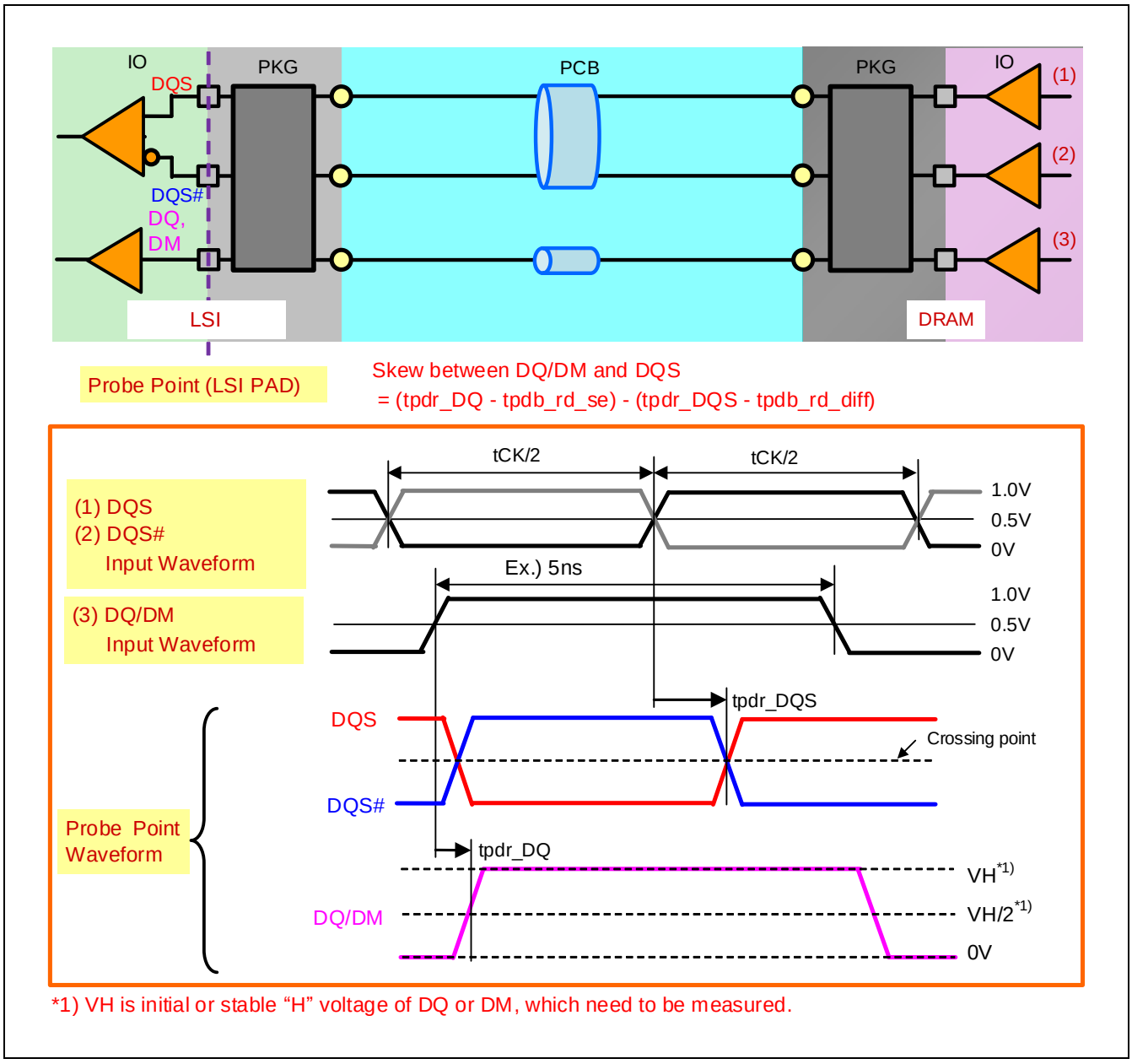

Figure 4.13 Measurement method of skew between DQ/DM and DQS (Read)

4.2.1.11 Skew between DQx and DQy (Read)

Figure 4.14 shows the measurement circuit, input waveform of DRAM IO model and measured waveform at LSI PAD in read mode. DQx/DQy skew should be smaller than the target specification shown in Table 4.1. PCB design should be verified by using data pattern which causes no ISI and no Xtalk jitter.

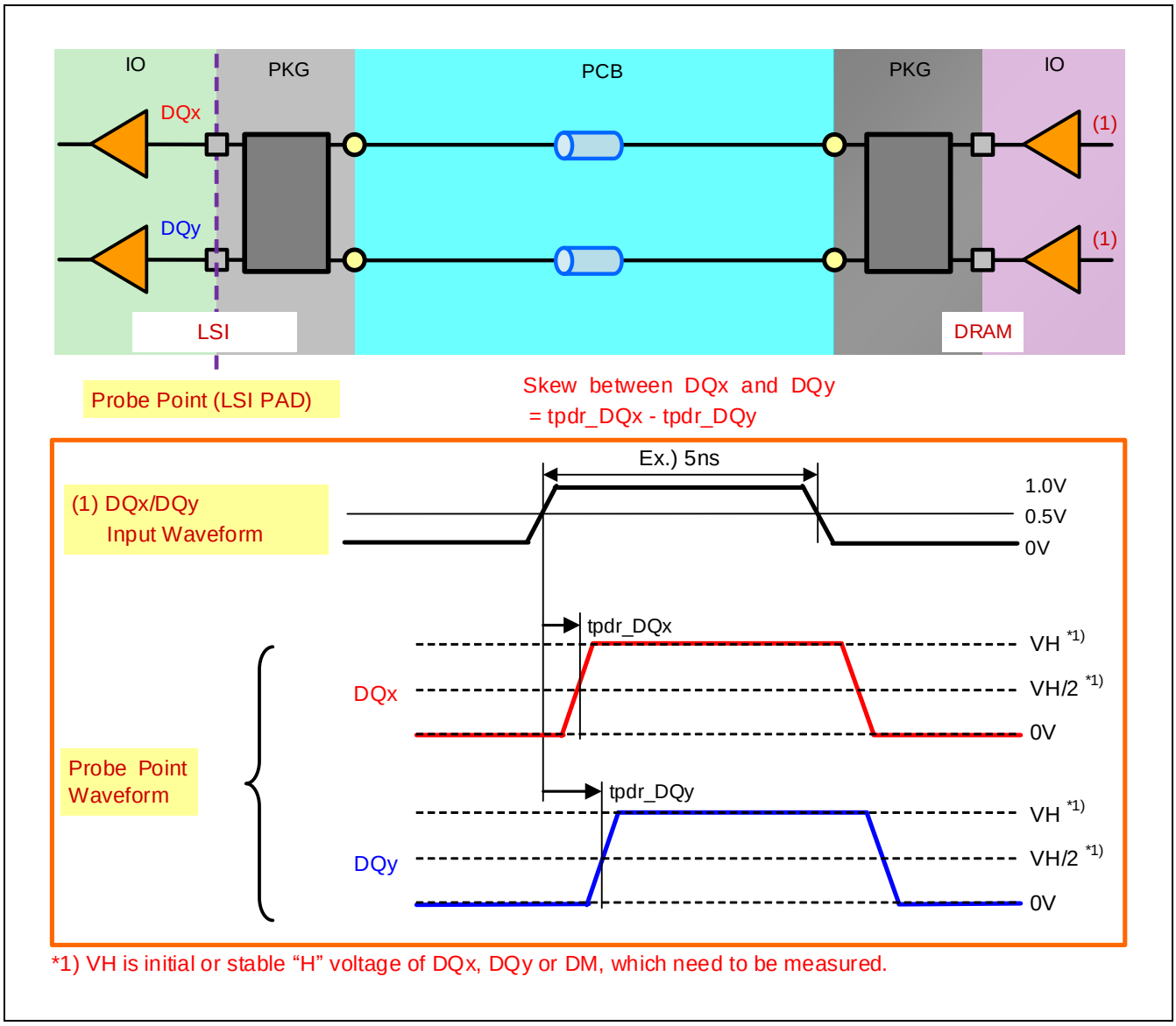

Figure 4.14 Measurement method of skew between DQx and DQy (Read)

4.2.2 Method of Flight-time restrictions

Flight-time is defined as sum of a) CK delay from LSI PAD to DRAM PIN (CK_delay) and b) DQS delay from DRAM pin to LSI PAD (DQS_delay), shown in below equation.

Flight-time = CK_delay + DQS_delay

4.2.2.1 Flight-time

Figure 4.15 and Figure 4.16 show measurement method of CK and DQS delay which compose the flight-time.

(1) Measurement method of CK_delay

Both delay “A” from PHY input to DRAM PIN and LSI IO delay “B” are measured in accordance with Figure 4.15. Then, CK_delay = A - B.

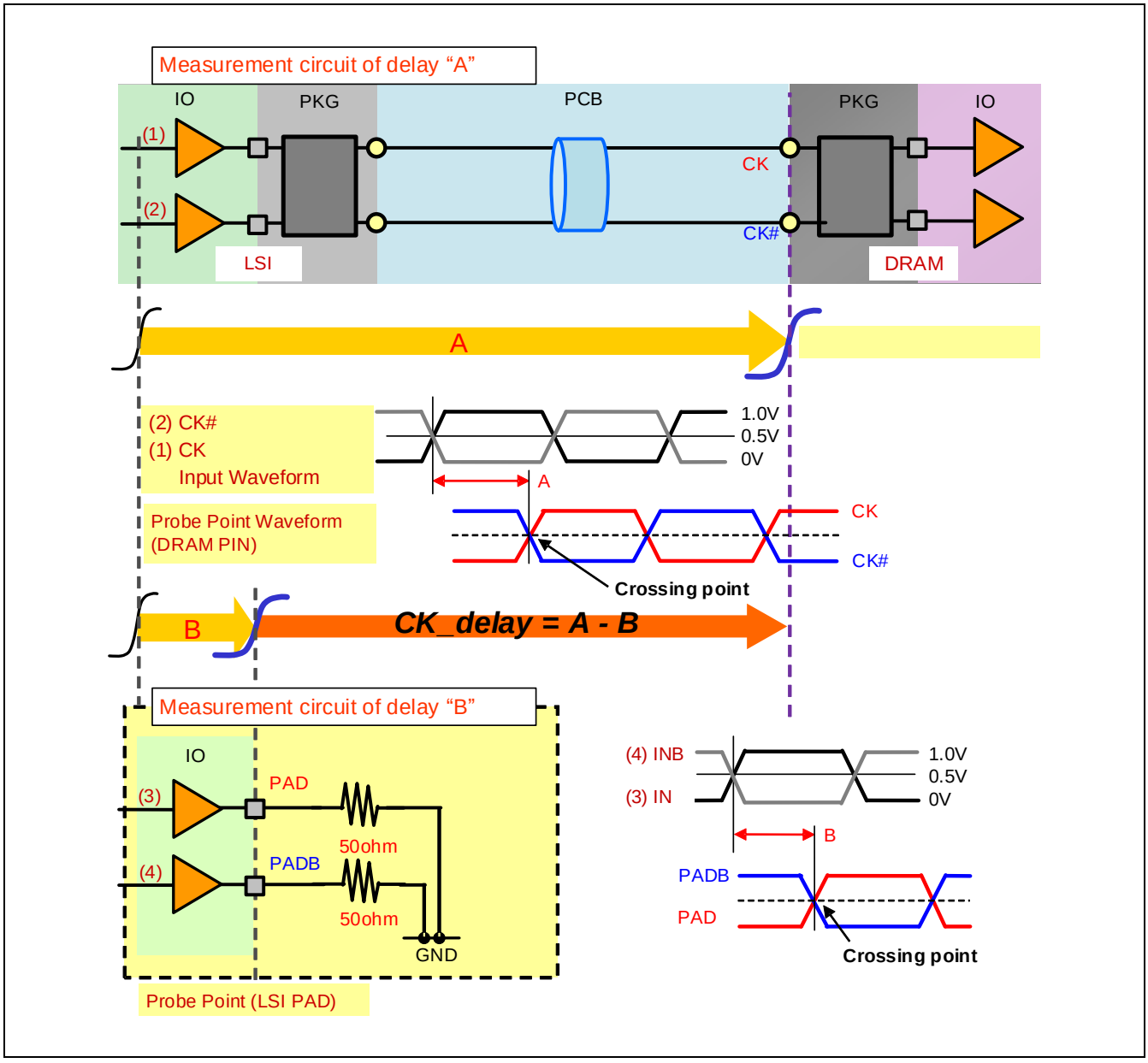

Figure 4.15 Measurement method of CK_delay

(2) Measurement method of DQS_delay

Both delay “C” from DRAM PIN to LSI PAD and DRAM delay “D” are measured in accordance with Figure 4.16. Then, DQS_delay = C - D.

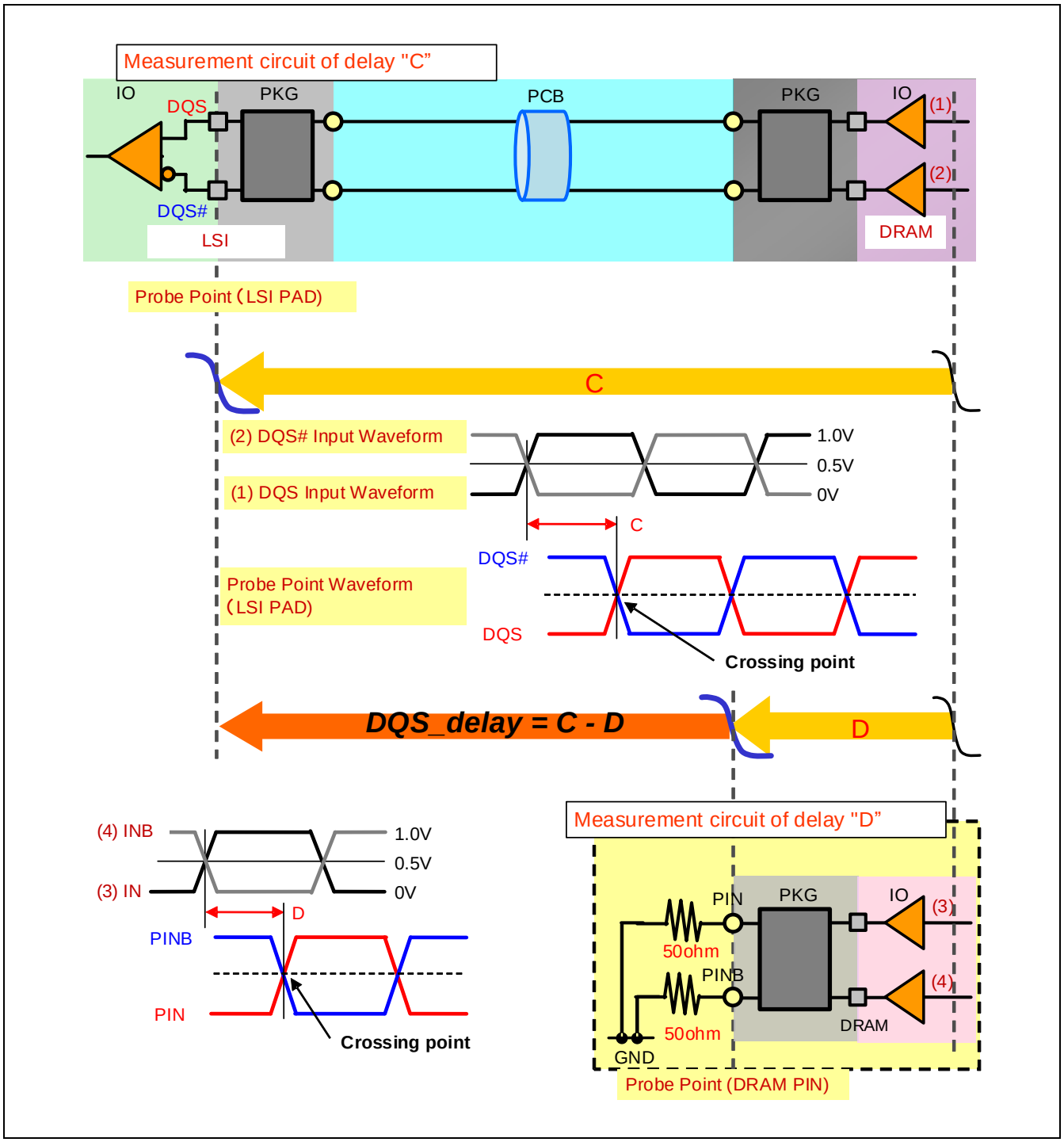

Figure 4.16 Measurement method of DQS_delay

4.2.3 Method of timing restrictions

Measurement methods for timing restriction are described in this section.

Timing restrictions shown in Table 4.13 must be confirmed at DRAM PAD / LSI PAD in Write/Read mode respectively. ISI and Xtalk effects of interconnect are evaluated in this measurement.

4.2.3.1 Write/Read DQ eye degradation (tdIVW_total)

Figure 4.17 shows a measurement example of DQ eye pattern. Vcent_DQ(pin_mid) is determined based on JEDEC standard. Maximum eye opening around Vcent_DQ(pin_mid) is measured as tdIVW_total(measured). The difference between UI and tdIVW_total(measured) is the degradation of Write (Read) DQ eye.

PCB design need to satisfy the target value of the DQ Eye degradation. Each target value is defined for both Write mode and Read mode. The all signals of DQ/DM need to be checked in both modes.

The trigger signal of DQ eye pattern is the differential signal of DQS/DQS#. Trigger level is differential zero volt.

The LSI has Write/Read DQ-DQS de-skew training function. This function aligns the rising and falling edge of DQS-DQS# to the center of DQ eye opening.

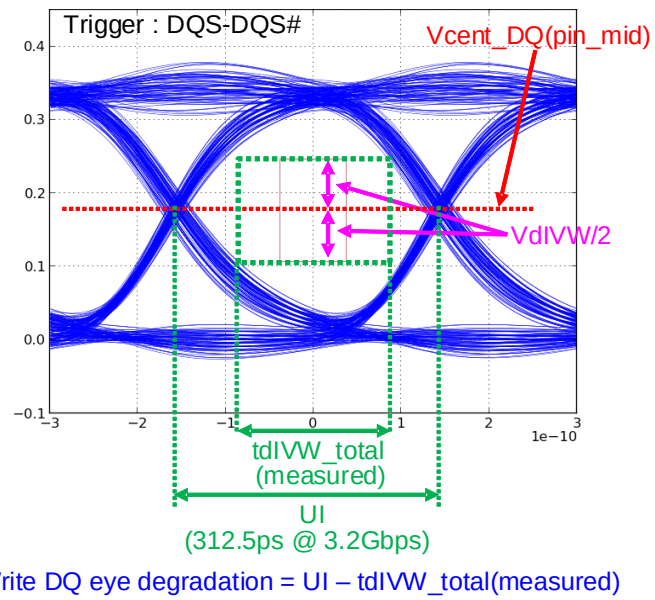

Figure 4.17 Measurement example of DQ Eye pattern

4.2.3.2 DQ Input pulse width degradation (At Vcent_DQ)

This is the restriction for the pulse width of DQ. Each pulse width of DQ should be measured for all DQs. Input pulse width degradation is calculated as the difference between tCK(avg)/2 and measured minimum DQ pulse width. DQ pulse width should be measured at Vcent_DQ(pin_mid) shown in JEDEC standard.

4.2.3.3 DQS input low/high pulse width degradation (tDQSL/tDQSH)

tDQSL/tDQSH should be checked in the same manner of clock low/high pulse width degradation (tCL/tCH). Please see section 4.2.3.6.

4.2.3.4 CA eye degradation (tcIVW)

Figure 4.18 shows a measurement example of CA eye pattern. Vcent_CA(pin_mid) is determined based on JEDEC standard. Maximum eye opening around Vcent_CA(pin_mid) is measured as tcIVW_total(measured). The difference between UI and tcIVW_total(measured) is the degradation of Write CA eye.

PCB design need to satisfy the target value of the CA Eye degradation. The all signals of CA/CS need to be checked.

The trigger signal of CA eye pattern is the differential signal of CK/CK#. Trigger level is differential zero volt.

The LSI has CA/CS-CK de-skew training function. This function aligns the rising edge of CK to the center of CA/CS eye opening.

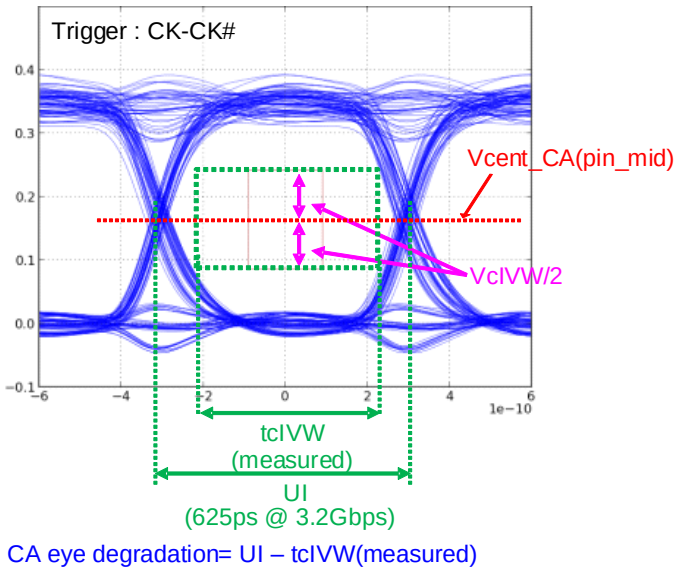

Figure 4.18 Measurement example of CA Eye pattern

4.2.3.5 CA input pulse width degradation

This is the restriction for the pulse width of CA. Each pulse width of CA should be measured for all CAs and CSs. Input pulse width degradation is calculated as the difference between tCK(avg) and measured minimum CA pulse width. CA pulse width should be measured at Vcent_CA(pin_mid) shown in JEDEC standard.

4.2.3.6 Clock High/Low pulse width degradation

Figure 4.19 shows a measurement example of tCH/tCL. tCH(min) and tCL(min) are determined based on JEDEC standard. The difference between tCK(avg) and each measured value is the tCH/tCL degradation. tCK(avg) means the average of CK period. tCH(max) and tCL(max) need to be checked in the same manner. PCB design need to satisfy the target value of the clock high/low pulse width degradation.

Average value of tCH and tCL degradation should also satisfy the restriction for tCH(avg) and tCK(avg).

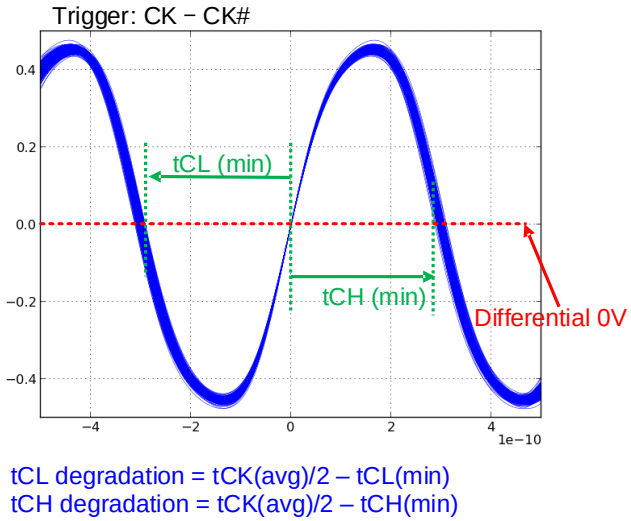

Figure 4.19 Measurement example of tCL/tCH

4.2.3.7 Clock period and cycle-cycle jitter (tJIT(per)/tJIT(cc))

Figure 4.20 shows a measurement example of tJIT(per). tCK(max) and tCK(min) are determined based on JEDEC standard. The difference between tCK(avg) and each measured value is the tJIT(per). tCK(avg) means the average of CK period.

PCB design need to satisfy the target value of the clock period jitter.

Similarly, tJIT(cc) need to be measured based on JEDEC standard and confirmed that the measured value satisfies the target value of the cycle-cycle jitter.

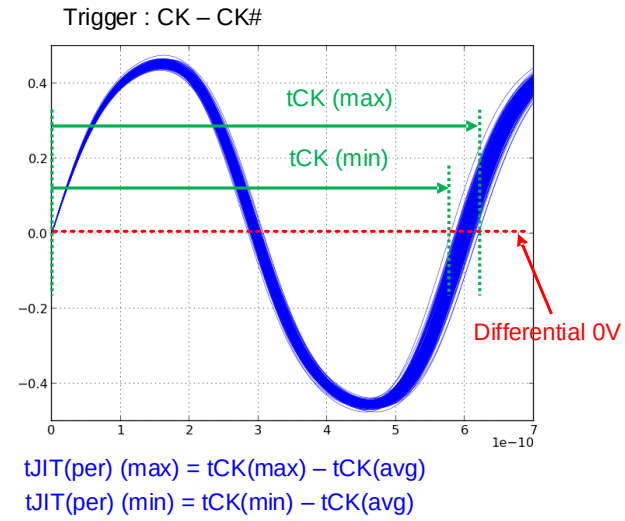

Figure 4.20 Measurement example of tJIT(per)

4.2.3.8 Jitter of DQS referred to CK rise edge (tDQSS)

Figure 4.21 shows the measurement method of DQS jitter referred to CK rise edge.

Please measure difference between minimum and maximum time from CK rise edge to next DQS rise edge (shown as tDQSS_fast and tDQSS_slow). The jitter of DQS referred to CK rise edge in Table 4.13 is half of this difference (= (tDQSS_slow - tDQSS_fast) / 2). PCB design need to satisfy the target value of the jitter.

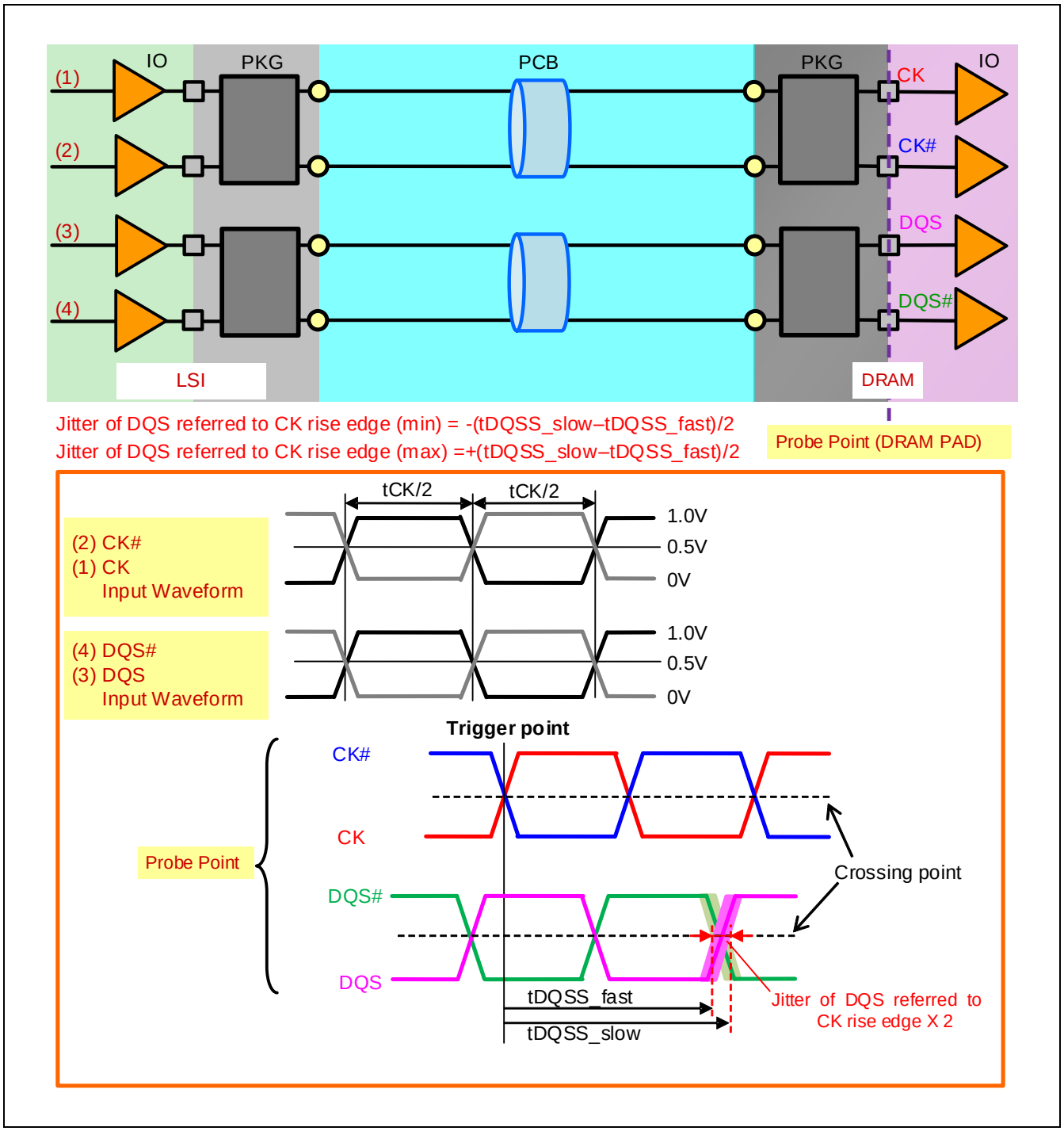

Figure 4.21 Measurement method of DQS jitter referred to CK rise edge

4.2.4 Method of waveform restrictions

Measurement method for waveform restrictions is described in JEDEC standard. Waveform restrictions shown in Table 4.14 must be confirmed at DRAM PAD / LSI PAD in Write/Read mode respectively. ISI and Xtalk effects of interconnect are evaluated in this measurement.

As an example of waveform restriction, Rx Mask voltage p-p is described in this section.

4.2.4.1 Rx Mask voltage p-p (for DQ and CA)

Figure 4.22 shows a measurement example of Rx Mask voltage p-p (for CA).

Minimum amplitude within the time range of eye mask (tcIVW in CA case) is measured as VcIVW_H(measured) and VcIVW_L(measured).

PCB design need to satisfy the target value of VcIVW/2.

The trigger signal of CA eye pattern is the differential signal of CK/CK#. Trigger level is differential zero volt.

Rx Mask voltage p-p (for DQ) need to be checked in the same manner.

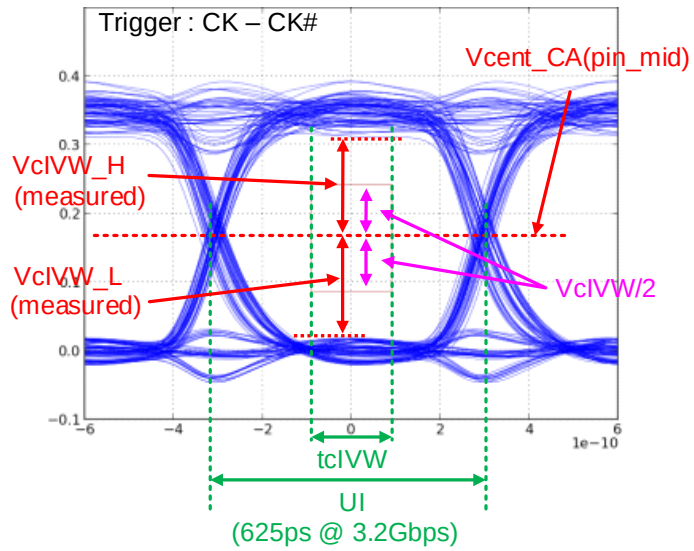

Figure 4.22 Measurement example of Rx Mask voltage p-p (for CA)

5. Verification items and method of IO Power Distribution Network (PDN)

5.1 Verification items

The target impedance Ztarget_ddr_vddq(f) is shown in Table 5.1, which is defined for the power domain of 32bit width. Frequency range for Ztarget_ddr_vddq(f) is defined higher than 100kHz. IO PDN must be designed so that the voltage is kept in the range specified by LSI specification.

Table 5.1 Target impedance for DDR_VDDQ

Frequency	Target impedance : Ztarget_ddr_vddq(f)		
	Min	Max	Unit
100kHz - 20MHz	–	0.05	ohm
20MHz <	–	0.20	ohm

5.2 Verification method

Renesas prepared LSI IO PDN model to confirm target impedance of LSI IO power supply for DDR-IF (DDR_VDDQ).

Please prepare PCB PDN model of your design.

Please connect these two models as in Figure 5.1, and confirm impedance in every frequency to meet the target impedance of Figure 5.2.

Power domain must be verified at 32bit width.

Renesas recommend that all impedances are less than target impedance in every frequency as in Figure 5.2.

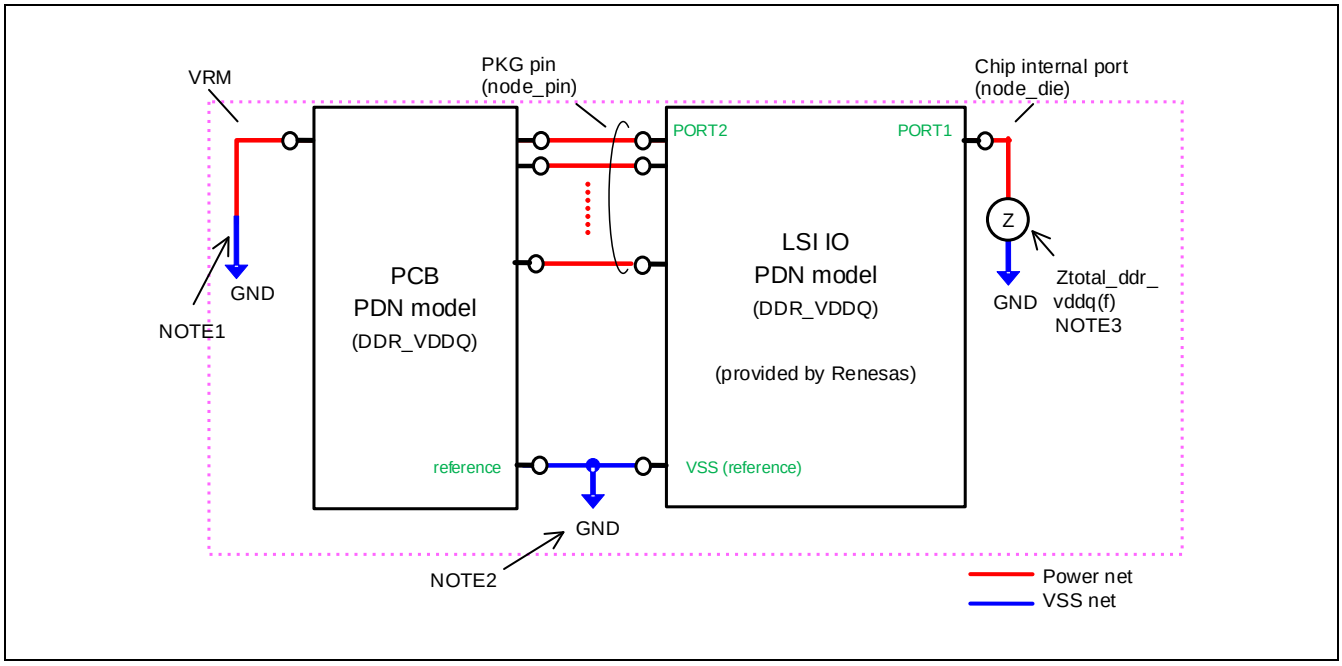

Figure 5.1 Connection for Ztotal_DDR_vddq(f) calculation

- NOTE1: Power node is shorted to VSS node on VRM side.

  Appropriate setting of GND is very important to simulate PDN impedance.
- NOTE2: Reference node on PCB PDN model (PKG pin side) is connected to the GND.

VSS (reference) node on LSI PKG PDN model (PKG pin side) is connected to the GND.

- NOTE3: Ztotal_ddr_vddq(f) is that loop impedance from chip internal port to the GND.

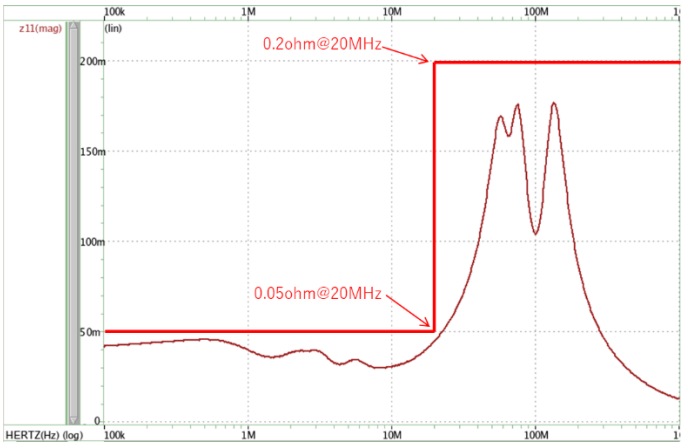

Figure 5.2 Target impedance of DDR_VDDQ for 32bit

REVISION HISTORY	RZ/T2H and RZ/N2H Groups PCB Verification Guide for LPDDR4

Rev.	Date	Description	
		Page	Summary
0.70	Feb 7, 2024	—	First Preliminary Edition issued
1.00	Sep 25, 2024	7	1.2 Operating conditions (3) DRAM specification: JESD209-4-1, deleted.
		9	Table 1.6 Verification items of DDR-IF: I/F column, deleted.
		11	Table 2.2 S-parameter filename and Table 2.3 LSI IO PDN model filename, added.
		13	Table 3.1 Recommended setting of LSI IBIS and DRAM IO model in CA: Note 1, deleted.
		13	Table 3.2 Recommended setting of LSI IBIS and DRAM IO model in DQ Write mode: Note 1, deleted.
		14, 15	Table 3.3 Recommended setting of LSI IBIS and DRAM IO model in DQ Read mode: description of Note 1, modified.
		17	Table 3.9 CKE setting: Command: Write / Read → Power Down, modified.
		17	Table 3.10 RESET_N setting: Command: Write / Read → Reset, modified.
		17	Table 3.11 ODT_CA pins connection: Command: Write / Read → Any, modified.
		18	3.3.1 IO power supply (DDR_VDDQ): DDR_VDDQLP, deleted.
		19	Table 3.12 PLL power supply parts list: Range of C3, modified.
		21, 22	Table 4.3 to 4.10: signals → LSI pin names, modified.
		22	4.1.2.1 Combination of measurement signals: “signals for skew restrictions” → “LSI pin names for Flight-time”, modified.
		22	Table 4.13 Timing restrictions: Category, modified.
		23, 24	Table 4.14 Waveform restrictions: Category and restrictions, modified. Note 2 to 4, added.
		24	4.2.1 Method of skew restrictions: title, modified.
		39	4.2.2 Method of Flight-time restrictions: title, modified.
		41	4.2.3 Method of timing restrictions: title, modified.
		45	4.2.4 Method of waveform restrictions: title, modified.
		46	5.1 Verification items: Ztarget_ vddq(f) → Ztarget_ddr_vddq(f), modified. Ztarget_ vddqlp(f), deleted.
		46, 47	5.2 Verification method: 64bit width → 32bit width, modified. Ztarget_ vddqlp(f), deleted.

RZ/T2H and RZ/N2H Groups PCB Verification Guide for LPDDR4

Publication Date: Rev.0.70 Feb 7, 2024
Rev.1.00 Sep 25, 2024

Published by: Renesas Electronics Corporation

RZ/T Series for Real-Time Control
RZ/N Series for Industrial Network
RZ/T2H and RZ/N2H Groups

Renesas Electronics Corporation

R01AN7260EJ0100