SLG51000/1 Development Software User Guide

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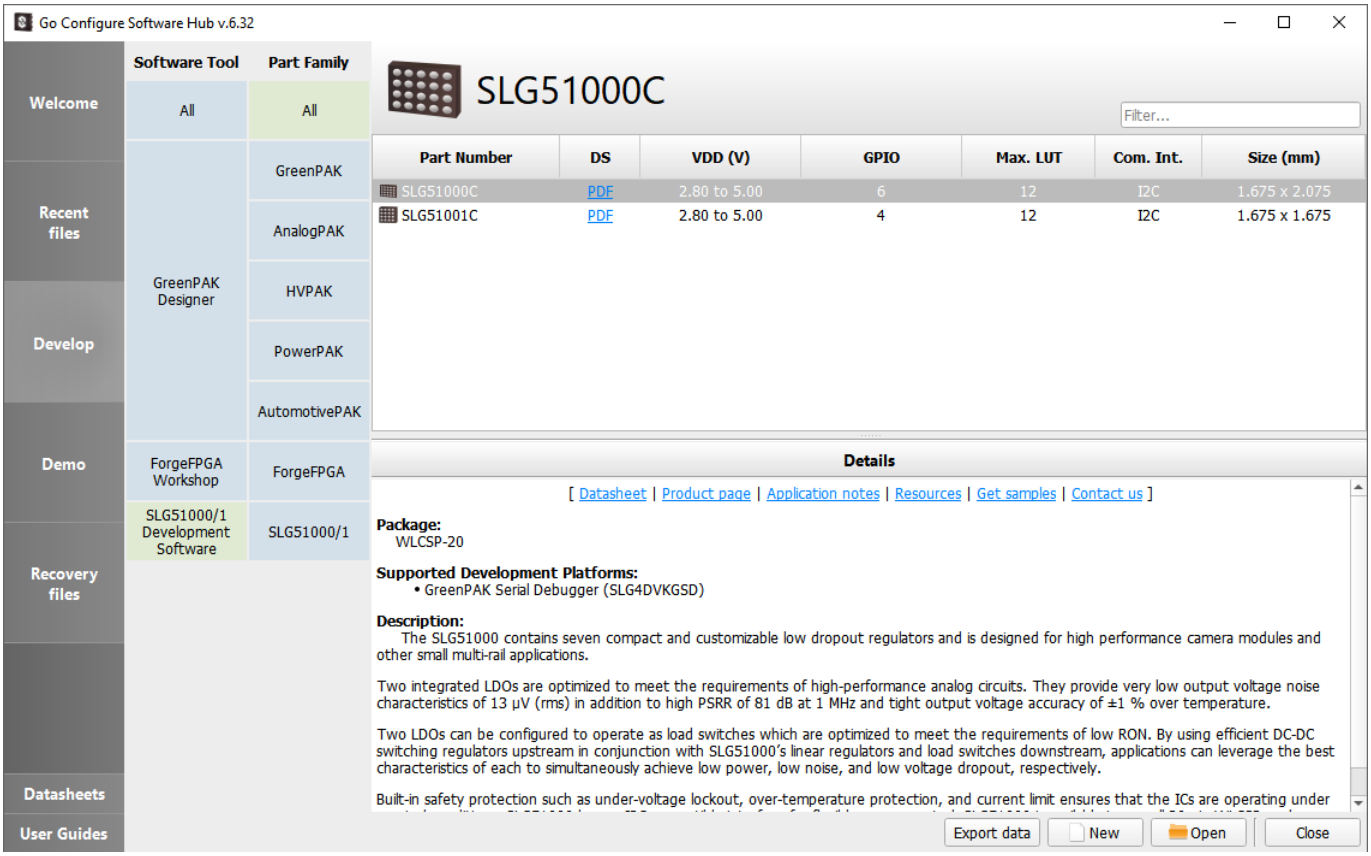
Contents

1. SLG51000/1 Development Software

This section describes SLG51000/1 Development Software application and its features.
Open Go Configure Software Hub application and select SLG51000/1 Development Software in Software Tools selector. Start new project for selected chip revision.

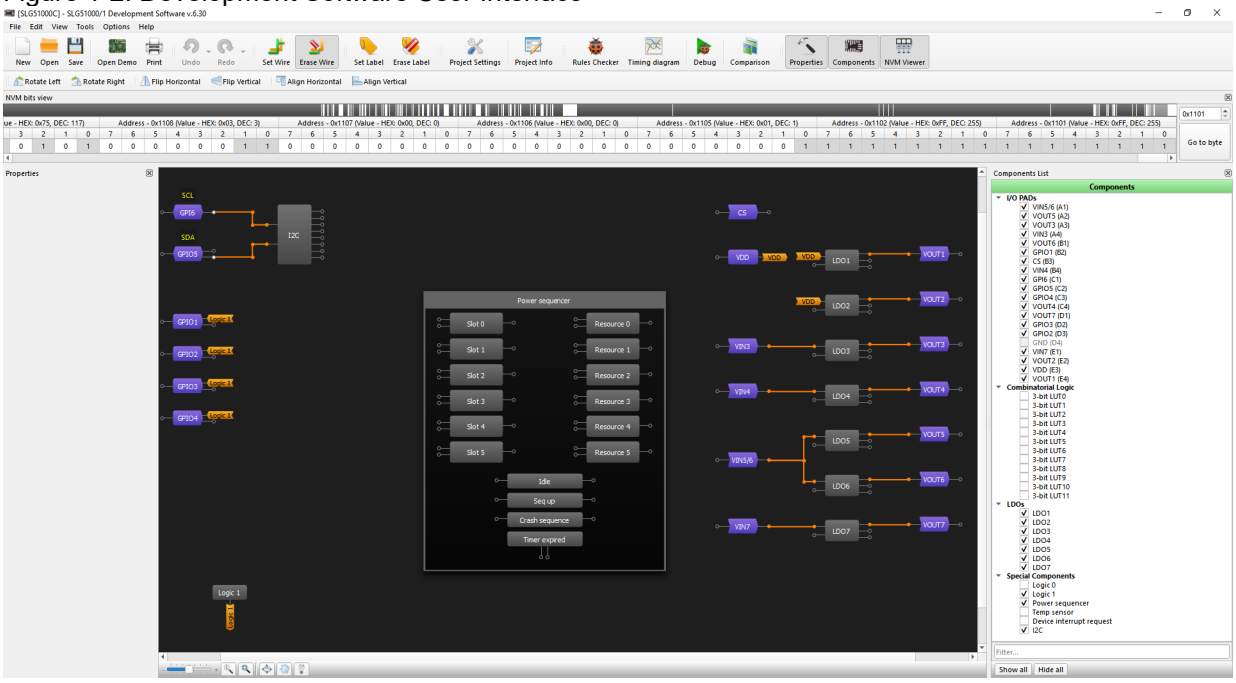
Figure 1-1. SLG51000/1 Development Software in Go Configure Software Hub User Interface



1.1. SLG51000/1 Development Software Interface Overview

Development Software consists of: main menu, toolbar, main work area, output window, properties panel and components list (see Figure 1-2).

Figure 1-2. Development Software User Interface



1.1.1. Main Menu

Main menu contains controls described below:

- **File**
  - New – start new project SLG51000/1 Development Software;
  - Open – open existing project in SLG51000/1 Development Software;
  - Save – save current project;
  - Save as – save current project in specified location;
  - Import (Import NVM) – load configuration bits from text file in specific format;
  - Export (Export NVM, Export registers) – save configuration bits to text file in specific format;
  - Print – starts simple print feature with block information;
  - Project Information;
  - Exit program – close Development Software;
- **Edit**
  - Rotate Left – rotate a selected block counterclockwise;
  - Rotate Right – rotate a selected block clockwise;
  - Flip Horizontal – horizontal reflection of a selected block
  - Flip Vertical – vertical reflection of a selected block
  - Align Horizontal – horizontal alignment of selected blocks
  - Align Vertical – vertical alignment of selected blocks
  - Set Label – creating a text label for selected blocks
  - Erase Label – erasing text labels near selected blocks
  - Set Wire – enable wire creating mode;
  - Erase Wire – enable wire erase mode;
- **View**
  - Zoom in – increase the work area scale;
  - Zoom out – decrease the work area scale;
  - Fit work area – tune scale to show all blocks visible in project;
  - Zoom 1:1 – set default scale;
  - Full-screen mode – switch to full-screen mode
  - Pan mode – enable/disable scene move in pan mode;
  - Show hints – enable/disable hints for blocks on the scene;
  - Properties – show/hide Properties panel;
  - Components – show/hide chip blocks list;
  - NVM Viewer – show/hide NVM bits viewer;
  - Rules Checker Output;
- **Tools**
  - Debug – this tool is included for convenient project testing with Demo Board;
  - Rules Checker – checks current design for correct settings;
  - Snipping tool – tool for copying or saving of the selected workarea;

- Comparison – compares bits of two projects;
- Timing diagram – shows window with state time configurator;

- **Options**
  - Settings – default projects folder, autosave, toolbars position, recovery, shortcuts and update options;
- **Help**
  - Help – show help window;
  - User Guides – open User guides folder or web page;
  - Legend box – show the color legend box;
  - Renesas web site – open Renesas official web site;
  - Software and documentation – open Software & Doc web page;
  - Renesas web store – open Renesas chip store;
  - Design support – web page with training courses and videos;
  - Contact Us – web form with request;
  - Social – Renesas in social networks;
  - Datasheet – open documentation web page;
  - Updater – open SLG51000/1 Development Software update tool;
  - About Go Configure Software Hub – show information about Development Software versions modification.

1.1.2. Toolbars

Toolbar provides a quick access to frequently used functions. There are 8 toolbars:

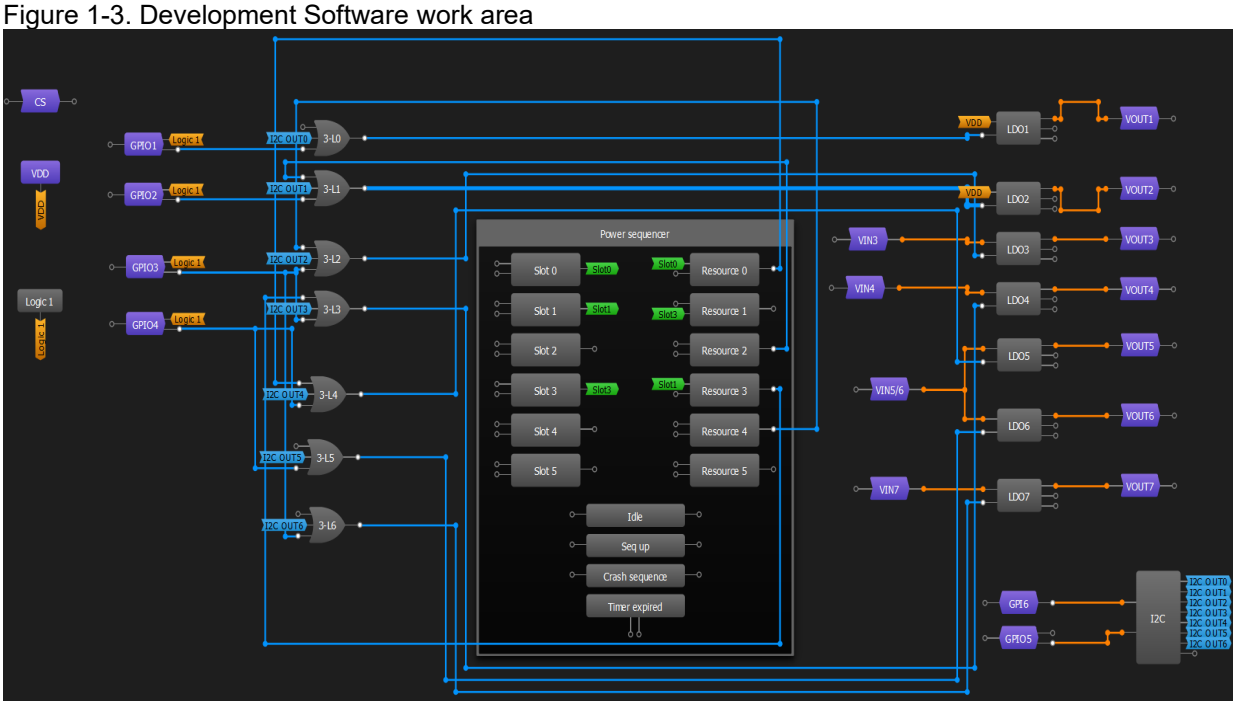
- **File**
  - New;
  - Open;
  - Save;
  - Demo;
  - Print;
- **Undo**
  - Undo;
  - Redo;
- **Wire**
  - Set wire;
  - Erase Wire;
- **Label**
  - Set Label;
  - Erase Label;
- **Item editor**
  - Rotate Left;
  - Rotate Right;
  - Flip Horizontal;

    - Flip Vertical;
    - Align Horizontal;
    - Align Vertical;
- **Tools**
    - Rules Checker;
    - Timing diagram;
    - Debug;
    - Comparison;
- **Panel switcher**
    - Properties;
    - Components;
    - NVM Viewer;
- **Navigation**
    - Zoom slider – adjust scale;
    - Zoom 1:1;
    - Fit work area;
    - Full screen mode;
    - Pan mode;
    - Show item hint;

1.1.3. Work Area

Work area contains all macrocells available in SLG51000/1 chip and their connections.

Figure 1-3. Development Software work area



Three types of components connection:

- Connectivity matrix connections (blue) – user can connect any output to any input through wiring tool;
- Settings defined connections (orange) – these connections are predefined and depend on block settings;
- Power sequencer connection between (green labeled) – these connections are inside Power sequencer area between slots and resources;

All macrocells can be moved using mouse or keyboard (Ctrl+Arrow Keys or Alt+Arrow Keys) and rotated. You can move a few blocks at the same time by using multiple select option. Rotation, flipping and alignment is also available for more than one block at a time.

1.1.4. Properties Panel

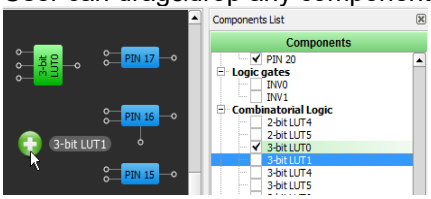
Properties panel contains all settings available for selected chip component. The panel is divided in two partitions: **Properties** and **Connections**. Properties division contains settings and parameters that could be specified for a selected block. Connection division contains settings which control the predefined connections to the selected block. Last division could not be present in some blocks. Some parameters and settings are common for a few blocks. After finishing all configurations press **Apply** button to confirm changes. If you want to discard changes you can press **Reset** button with options: reset settings to default or reset connections to default.

1.1.5. Components List

The Components list is an instrument that contains all blocks available in chip. It provides user with the possibility to show/hide unused blocks. You cannot hide blocks that are connected by any type of lines. In the SLG51000/1 chip there are connections which are beyond the connectivity matrix. They are controlled by settings of proper components and cannot be fully disconnected. That's why there are some blocks that cannot be hidden. Hidden blocks retain their configuration. For this reason, be sure to configure hidden components properly. You can show/ hide selected blocks by using the checkbox on the list. In order to show a group of blocks, double-click on the checkbox of the desired group. In order to hide a group use a single click.

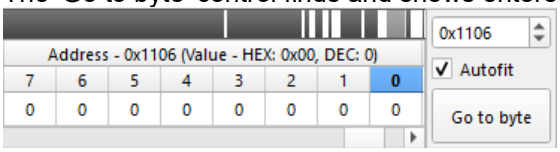
There are two buttons at the bottom of the components list – Show all (shows all blocks) and Hide all (hides all blocks which are not connected to a circuit). Also user can use filter to find required components.

User can drag&drop any component from Component List to the workarea to the right place:



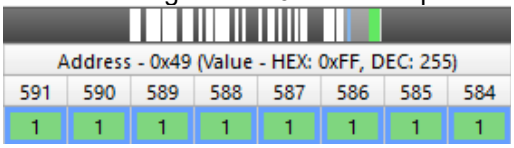
1.1.6. NVM Viewer

NVM Viewer contains all chip bits in the table, divided into bytes. All bytes have their address and 8-bit sequence. The 'Go to byte' control finds and shows entered byte in hex format from 0 to 7 bit:

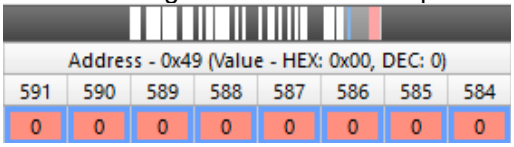


It is easy to see which bits are set to 0 or 1 with the NVM viewer highlight bits tool. Bits, set to 1 denoted by grey color. The slider on the top of NVM Viewer shows position in the NVM table, selected bytes are shown on the bottom. All bits are highlighted in blue color for the selected block.

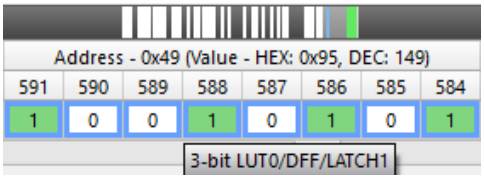
Bits that changed from 0 to 1 are represented by green color



Bits that changed from 1 to 0 are represented by red color



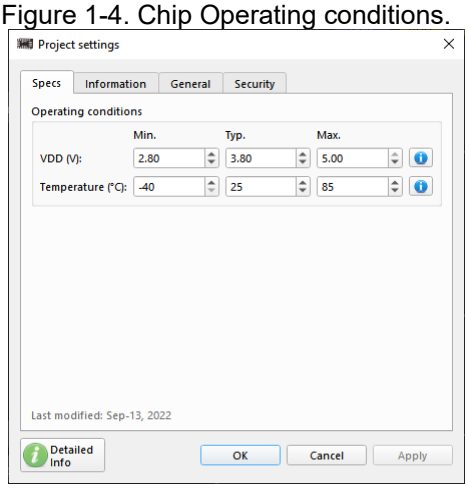
Hover the mouse cursor over the table to see the macrocell name hint



1.2. Creating a Project

To create a new SLG51000/1 chip project start SLG51000/1 Development Software or go to **File->New** or click the "New" icon on the toolbar. While creating new project in SLG51000/1 Development Software please specify operating conditions – VDD and Temperature.

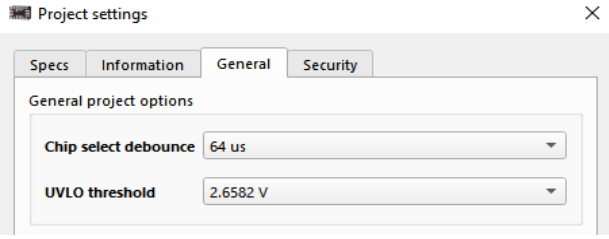
Figure 1-4. Chip Operating conditions.



A new project will be created in current window and all unsaved changes will be lost. By default the project is configured for minimal power consumption and some components are disabled. All disabled components are darker and colored in red after selection. SLG51000/1 Development Software projects use [.can] file extension. It contains information about position, rotation/flipping and configuration of chip blocks, all wire connections, and bit file sequence settings, etc. Interface settings will not be saved in the Project file.

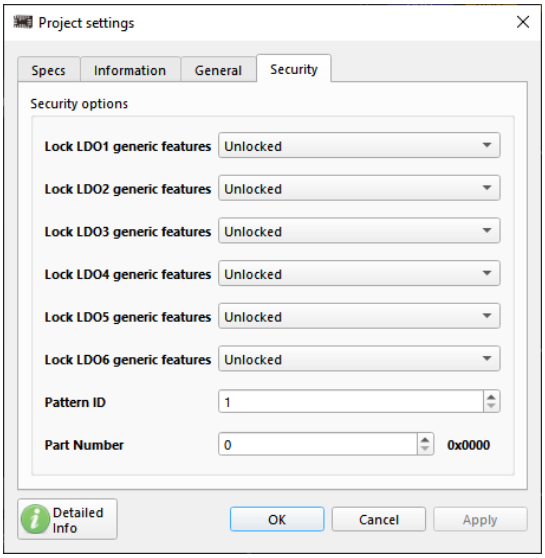
1.2.1. Project Settings Window

Figure 1-5. Project Settings General tab



Chip select debounce – this option will set programmable shutdown debounce time (from 0 to 256us);
UVL0 threshold – safety protection under-voltage lockout;

Figure 1-6. Project Settings Security tab



Lock LDOx generic features – this options control locks on LDOx.

Pattern ID – gives an ID (1-255) to the project. The ID will be put in the chip after programming, and also will be read while “chip reading” operates.

Part Number – unique number (16-bit) used to identify the device.

1.3. Configuring Chip Components

1.3.1. Placing Components

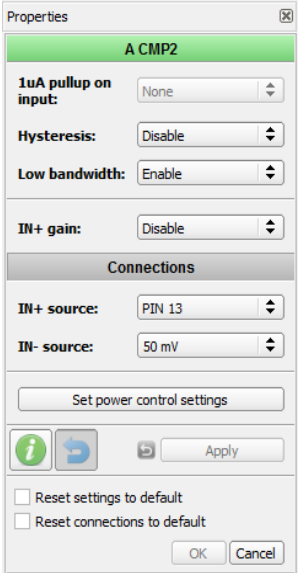
When you open SLG51000/1 Development Software it will start with a blank project. A blank project contains pins and blocks which cannot be hidden. Components can be moved, rotated, flipped and aligned. In order to move a component, simply drag it where you want by clicking the left mouse button. To rotate/flip/align component select it and press the “Rotate/Flip/Align” buttons 

on the toolbar or select Rotate/Flip/Align in the main menu.

1.3.2. Setting Chip Components Parameters

Each chip component has different parameters. Some components have parameters that are shared with other components. Changes in one block cause changes in other blocks. Component settings are available at component **Properties** panel (Figure 1-6) which appears after double-clicking on the component. **Properties** panel consists of three parts: Properties, Connections, and Information. Properties section contains all settings of a selected component. Connections section allows you to configure connections that couldn’t be made using wiring tool. Information section contains short information about parameters of selected component. After making changes in **Properties** panel click the **“Apply”** button to save changes. If you do not click the **“Apply”** button and select another block, a save changes message box will appear.

Figure 1-7. Properties Panel

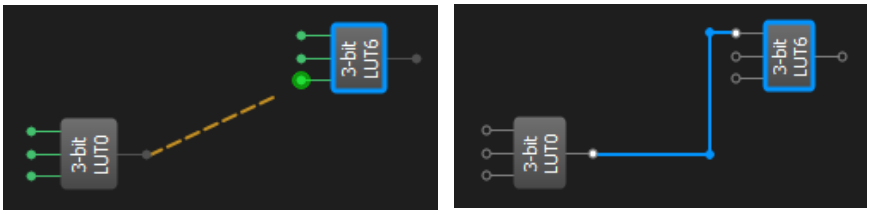


Reset connections and/or settings to default: this option allows to reset NVM bits, components properties, wire connections from/to component.

1.4. Specifying Interconnections

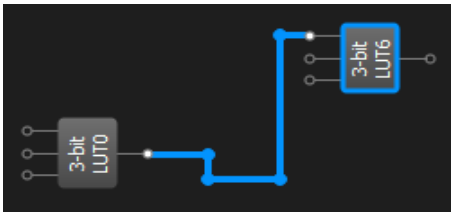
You can interconnect chip components to achieve the necessary functionality. To make a connection please select **Set wire** on the **Wire** toolbar or from the main menu. Next, click the first and second pins that you want to connect (Figure 1-8). After selecting the first pin, software highlights allowed connections in some color (see Legend box). If you click the first pin and then decide to exit line creating mode press **Esc** or the right mouse button.

Figure 1-8.



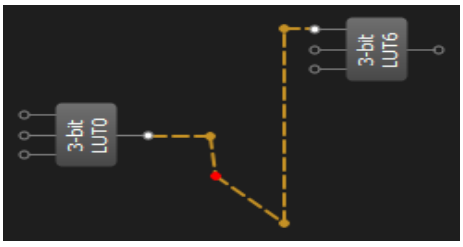
Also you can manually correct the created wires.
You can move horizontal lines up and down, vertical lines left and right (Figure 1-9).

Figure 1-9.



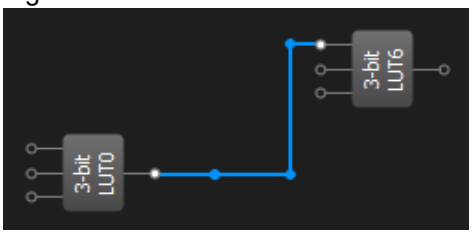
You can move points on the wire (Figure 1-10).

Figure 1-10.



In order to create additional points on the line use the double click (Figure 1-11).

Figure 1-11.



Only the blue color pins can be connected Using Wire Creating tool. Some components have pins that are not allowed to be connected using wiring tool. Connections between such pins (orange line and violet pin color) can be made only by changing settings in **Connections** section of the **Properties** panel of proper components. In this case violet pins can change color to green and user can connect them using wiring tool. Orange wires will be automatically generated. Orange wires also can be modified by user. Input pins without connections are considered to be tied to ground.

In order to delete wire please select **Erase wire** 

at the **Wire** tool-bar and click on the selected wire. Only blue and green labeled wires can be deleted.

Additional controls for add/remove wires:
Hold button to force wire mode:

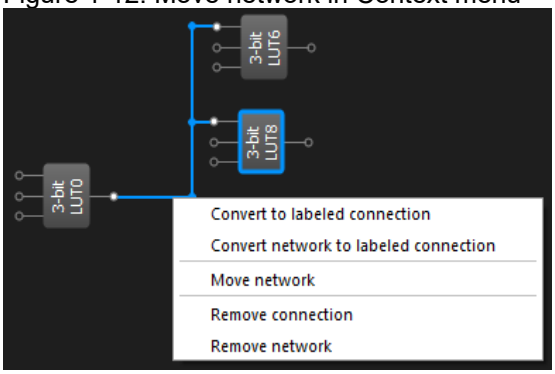
- Shift: for Set Wire;
- Alt: for Erase Wire;

Action with multiple wires:

- Hold Ctrl+Shift and click on pin: add multiple wires from the same source pin;
- Hold Ctrl+Alt and click on wire: remove all wires from source pin;
- Hold Ctrl: works as Ctrl+Shift or Ctrl+Alt based on current wire mode;

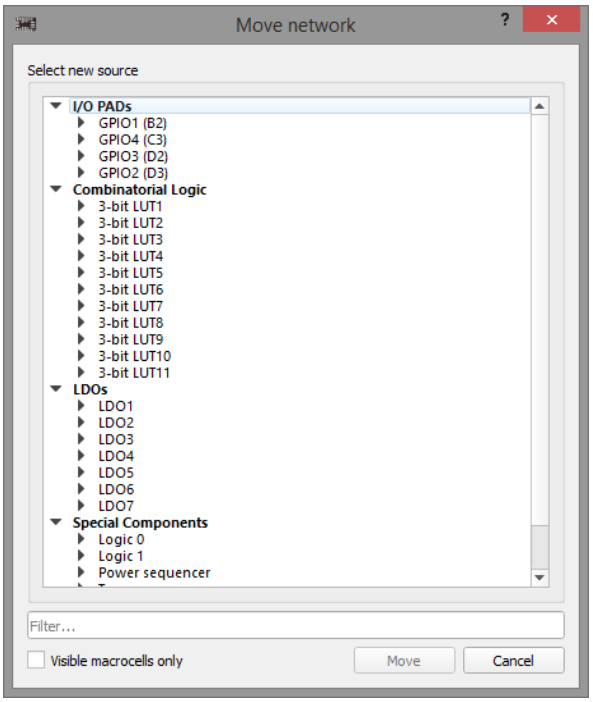
Move network
Move network feature provides the fastest way to reconnect all matrix wires from any pin to another. Simply click on wire with right mouse button and select Move network in Context menu

Figure 1-12. Move network in Context menu



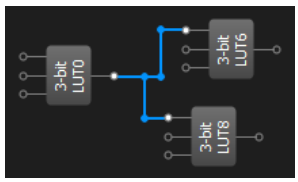
Select new source from list in Move network window. User can select new source only from list of visible blocks or from list of all blocks.

Figure 1-13. Move network window



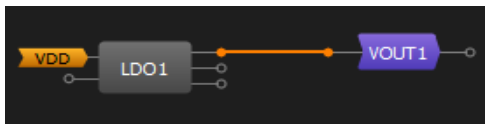
1.4.1. Wire Types

Figure 1-14. Blue Line



Blue lines in SLG51000/1 Development Software tools are used to mark manual wires. Using them you can manually connect necessary blocks to operate in the desired way. You can connect block output to multiple inputs, but wiring of different outputs to one input is impossible.

Figure 1-15. Orange Line



Orange lines are used to mark the internal functional bounds of the chip blocks. They do not have the impact on chip operation until the proper function is used. These lines can't be erased.

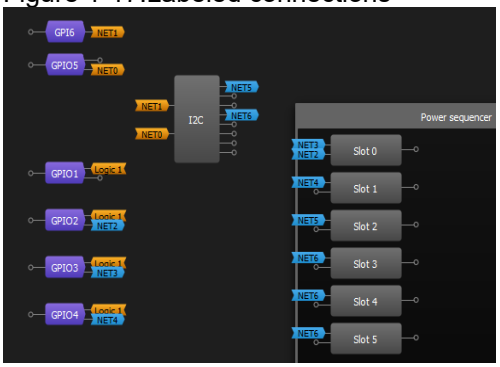
Figure 1-16. Green labels

Green labels are used to mark the connections between Slot and Resources in Power sequencer area. Their behavior is the same as the blue lines.

Replacing wires by labels

This option converts wired connection to 2 labels (for output and input pins) and back (Figure 1-17). Name of the label will be generated automatically: NETx, where x – random number. If output was connected to few inputs all of them should have the same name. For changing the connection type use the context menu of the block, line or label(NET).

Figure 1-17.Labeled connections



Available options for wire (context menu):

- Convert to labeled connection;

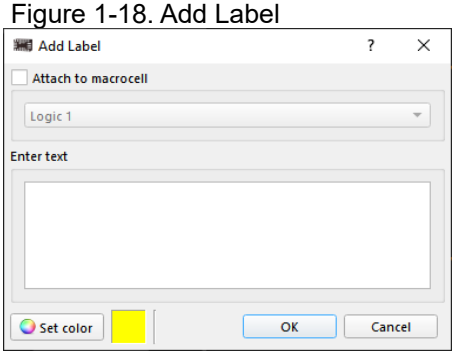
Available options for label (context menu):

- Convert to wired connection;
- Rename network;
- Remove connection.

1.4.2. Set/Erase Label

Using Set/Erase Label the user can add/delete text label. The Set Label tool adds a text label to the selected component or without connecting them to the specific component. The user can Attach label to component or Detach label(s) from component(s). If no component is selected, then the user can select a component from the list offered by the Set Label tool. The user can also choose text color. If the selected component already has a label, Set Label tool can edit label text. If the user selects more than one component, it is possible to change the text color without changing text in all components at once. If the user changes the text while more than one component is selected, it will be changed on all selected components at once as well. Erase Label deletes text label.

Figure 1-18. Add Label



1.5. Navigation

To navigate through project workspace use the **View** menu or toolbar. Use **Zoom In** , **Zoom Out** buttons or slider to zoom workspace. If you want to see all project components click on **Fit work area** or **Zoom 1:1** . To navigate through work area you can use **Pan mode** . Pan mode also activates by using middle mouse button.

To enable block's hint, press **Show item hints** button. A hint box pops up next to the item when the mouse moves over the block.

1.6. Keyboard commands

To navigate through SLG51000/1 Development Software use specific keyboard commands or shortcuts. List of commands specified in the table:

Table 1-1. Keyboard commands

Keyboard command	***Action***
Block moving on the scene	
Alt+Arrow Keys	Moves selected block on 1 pixel
Ctrl+Arrow Keys	Moves selected block on 10 pixels
Connecting/Erasing wires	
Hold *Shift*	Forces Set wire while using Erase Wire
Hold *Alt*	Forces Erase wire while using Set Wire
Hold *Ctrl+mouse cursor*	Adds multiple wires from the same source
Hold *Ctrl+Shift+mouse cursor*	Forces add of multiple wires from the same source while using Erase Wire
Hold *Ctrl+Alt+mouse cursor*	Forces remove of all wires from the network while using Set Wire
Standard hotkeys	
Ctrl+Z	Undo
Ctrl+Y	Redo
Ctrl+N	New project
Ctrl+O	Open project
Ctrl+S	Save project
Ctrl+P	Print Editor
Ctrl+Q	Exit program
Ctrl+L	Rotate component Left
Ctrl+R	Rotate component Right
Ctrl+H	Flip component Horizontal
Ctrl+V	Flip component Vertical
Ctrl+W	Set Wire
Ctrl+E	Erase Wire
Ctrl+F	Filter on Components List
H	Hide component
+	Zoom in

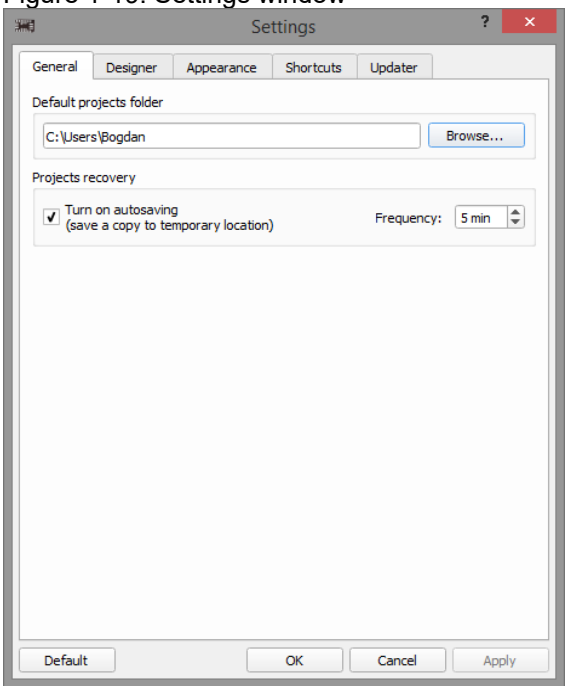
-	Zoom out
F1	Help
F2	NVM Viewer
F3	Properties of component
F4	Components List
F5	Rules Checker
F9	Debug
F11	Fullscreen Mode

All other SLG51000/1 Development Software main window actions can be configured by entering specific key sequence in Settings window on Shortcuts tab.

1.7. SLG51000/1 Development Software Settings

SLG51000/1 Development Software settings configure all basic options of program in several tabs (Figure 1-19). To open settings select Options-> Settings in main menu.

Figure 1-19. Settings window



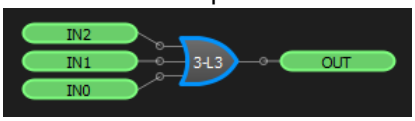
SLG51000/1 Development Software settings window contains of tabs:

General:

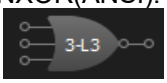
- Default projects folder – defines path to users SLG51000/1 project files;
- Projects recovery – activates autosave function, which allows to reduce the risk or impact of data loss in case of a crash or freeze. Autosave function in predetermined time intervals will save your files and after a critical problem will save files to default projects folder.

Designer:

- Pin hints – shows pin hints while block is selected or properties panel of component is visible:



- Look-Up Table (LUT) – allow usage of regular shape by default. For example, regular shape of NXOR(ANSI):



Appearance:

- Window appearance – saves positions of toolbars/dock widgets and window geometry of Development Software work area;
- High DPI displays – enables SLG51000/1 Development Software scalling on high DPI displays;

Shortcuts:

- On Shortcuts tab all SLG51000/1 Development Software actions can be configured by entering specific key sequence.

Updater:

- Scheduler – determines check for updates time: after Development Software starts or Once per 1-7 days;
- Path – defines server for update and destination to download updates;
- Proxy – allow user to configure proxy for updates;
- Check configuration button – checks connection to server.

Default button:

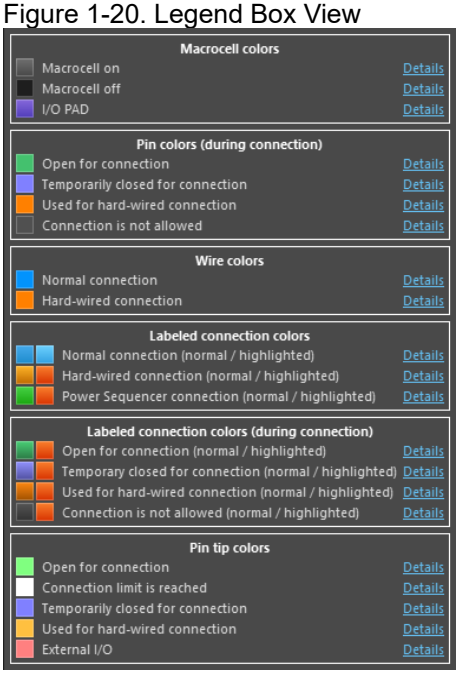
- Resets settings to default parameters by categories or all at once.

1.8. Legend Box

Legend box shows the color scheme of SLG51000/1 Development Software.
The user can open this window by clicking 'Legend box' button in 'Help' menu.

Legend box show colors of macrocells, pins, wires, labeled connections and pin tips on the work area.

Figure 1-20. Legend Box View

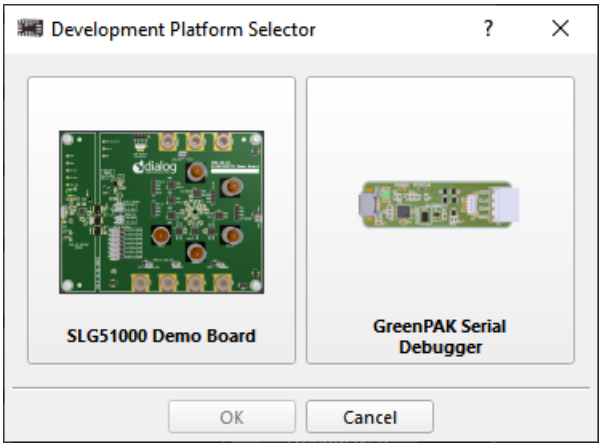


2. Debug mode

Type of hardware platform

After start of Debugging tools select type of hardware platform with supported features (Figure 2-0):

Figure 2-0. Platform selector window



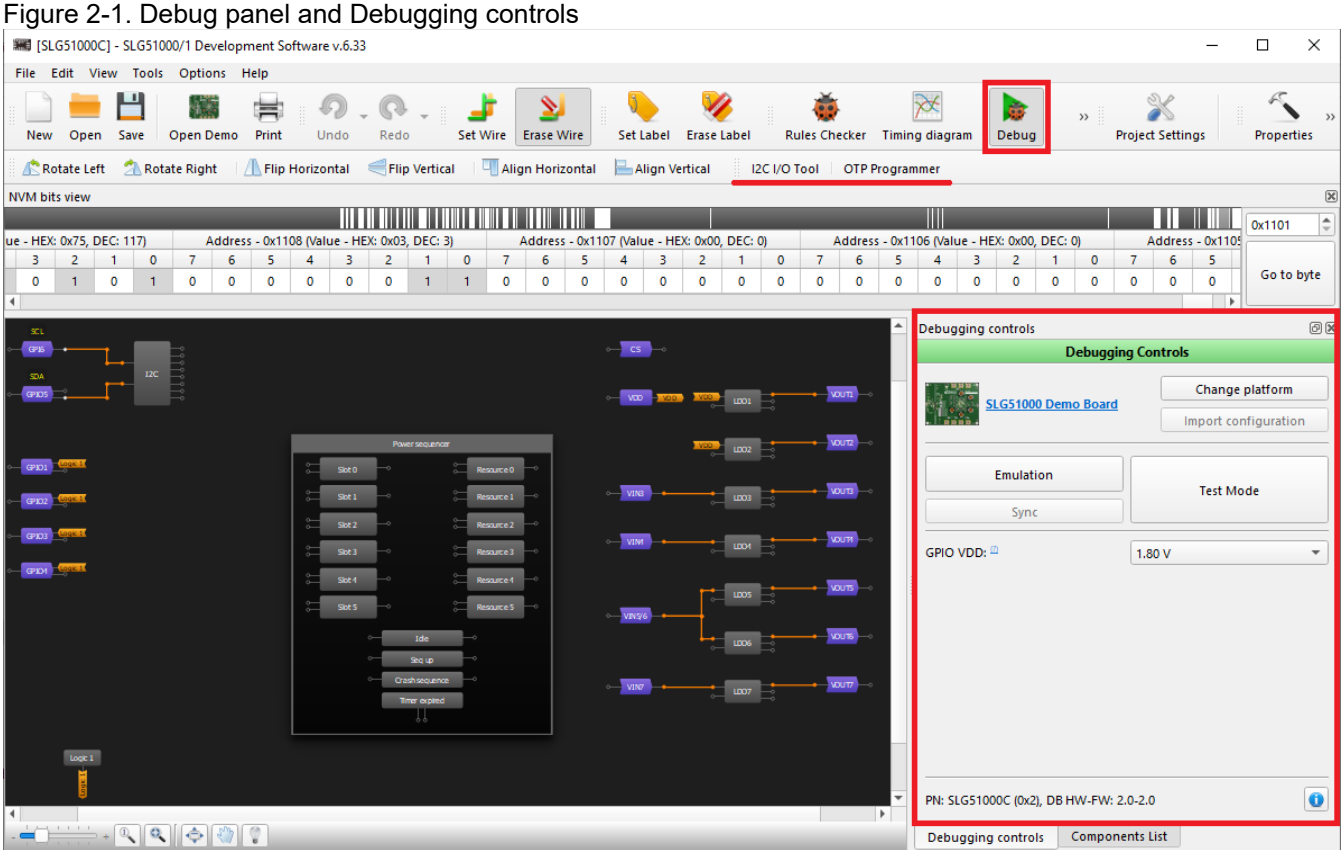
SLG51000/1 Demo boards

Demo board is a special hardware with a mission to demonstrate some specific application of SLG51000/1 chip. It has SLG51000/1 chip soldered on the board. It also supports I2C transferring that allows SLG51000/1 Development Software to communicate with SLG51000/1 chip and temporarily change its NVM in Emulation. Emulation starts communication with SLG51000/1 chip from software. User can load any project data to chip by clicking Sync button and test configuration on hardware Demo board.

Demo board connection

After starting of Debug, the SLG51000/1 Development Software waits for connection of Demo Board. All Debugging controls become available after the connection of the Demo board.

Figure 2-1. Debug panel and Debugging controls



Debug

Debug button starts Debug tool in the SLG51000/1 Development Software (Figure 2-1). The Debug tool enables electronic circuit emulation and chip programming, which uses a specific hardware platform to replicate the behavior of chip components. Before starting the emulation process, add test points controls to configure the emulation process.

After proper Demo board detected (Figure 2-1), simple Debug tool activated:

- Emulation – starts communication with a chip, sends current project data to chip;
- Sync – sends current project's NVM to device;
- Test mode – turns on the power supply on the chip, uses chip project, programmed on the chip;
- GPIO SW Control – adds buttons for software control of GPIO1, GPIO2, GPIO3(SDA), GPI4(SCL) and CS I/O pads (Figure 2-2). This functionality is available only for the SLG51001 Demo board. **Attention:** Please plug in all 'SWCTRL' jumpers to be able to control GPIO from the software.

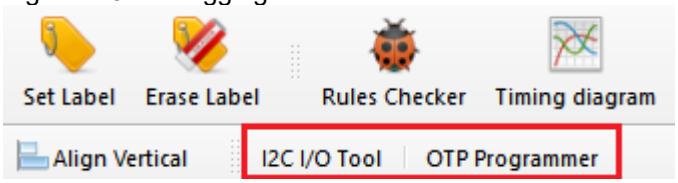
  Figure 2-2. Configurable Button

  The default connection can be set to Upper or Bottom connection. Click your mouse over the key U or B to change the value. The user can configure each connection to High-Z or GND. The button has 2 modes: Latched or Not latched, which can be configured by clicking over the key LATCH.
- GPIO Vdd – selects operational GPIO Vdd for Emulation;
- Close – exits Debug mode;
- Info button – shows all system and hardware information;
- I2C I/O Tool, OTP Programmer – appear on Debugging tool toolbar (Figure 2-3).

Attention: Start Emulation to begin work with SLG51000/1 chip

Figure 2-3. Debugging Tool toolbar

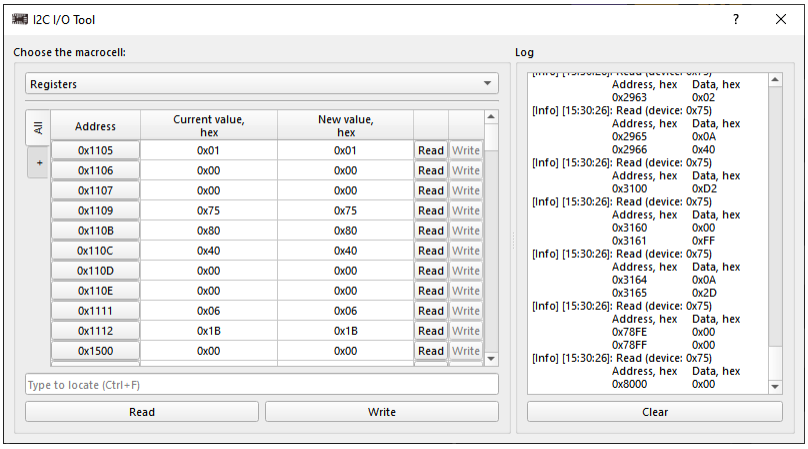


Debugging Tool toolbar contains (Figure 2-3):

- I2C I/O Tool;
- OTP Programmer;

I2C I/O Tool:

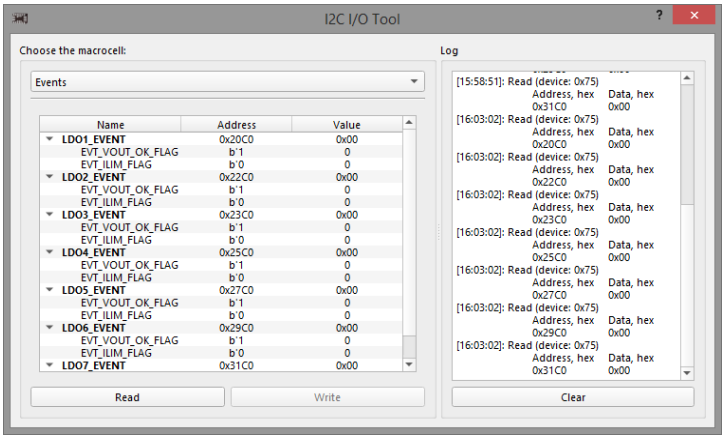
Figure 2-4. I2C I/O Tool window



Choose the macrocell:

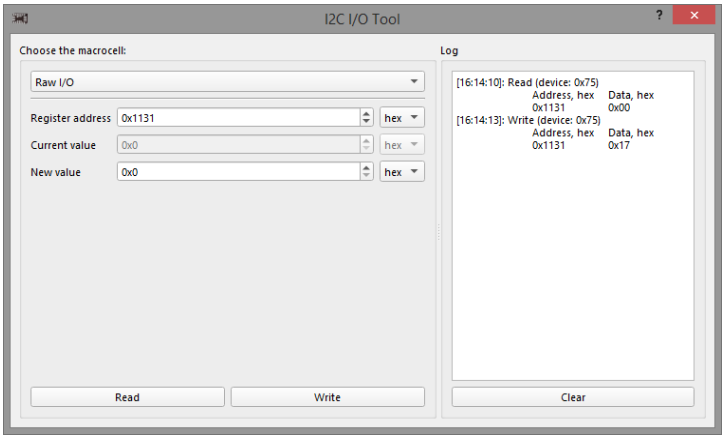
- Registers – the current value of all chip registers can be read and write via I2C. Click on any Register byte Address to change it value;
- Events – shows the list of LDO events: name, address and value;

Figure 2-5. I2C I/O Tool window with events



- Raw I/O – reads and writes any data from/to registers via I2C(Figure 2-6);

Figure 2-6. I2C I/O Tool window with Raw I/O



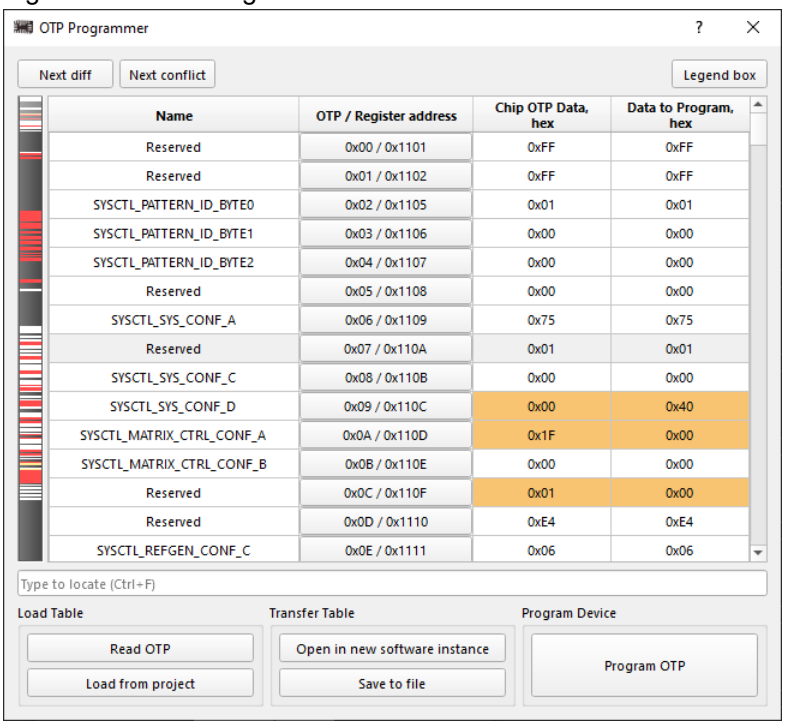
- Log – shows log of read/write operations;
- Clear – clears all Log information;

OTP Programmer:

OTP Programmer reads OTP memory from chip and programs chip with the current project data. Tool shows diffs and conflicts between chip and project data.

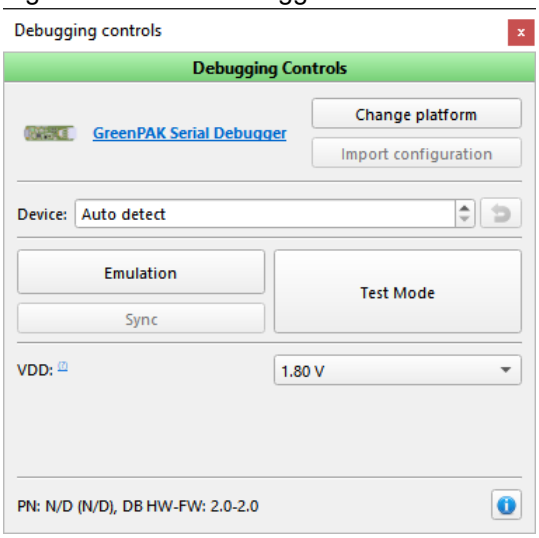
Attention: Users have opportunity to reprogram bits changed from 0 to 1.

Figure 2-7. OTP Programmer



Serial Debugger

Figure 2-8. Serial Debugger tools



After Serial Debugger board detected, simple Debug tool activated (Figure 2-8):

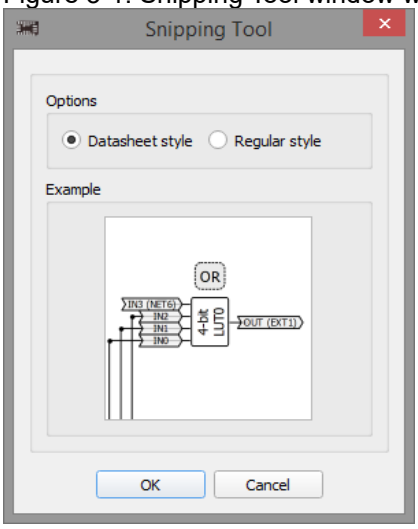
- Device – slave address selector for I2C communication;
- Emulation – starts communication with a chip, sends current project data to chip;
- Sync – sends current project's NVM to device;
- Test mode – turns on the power supply on the chip, uses chip project, programmed on the chip;
- VDD – the voltage level on I2C bus;
- Info button – shows all system and hardware information;

3. Snipping Tool

Snipping Tool is screenshot tool for SLG51000/1 Development Software workarea. It allows scene selection, copying or saving as a file.

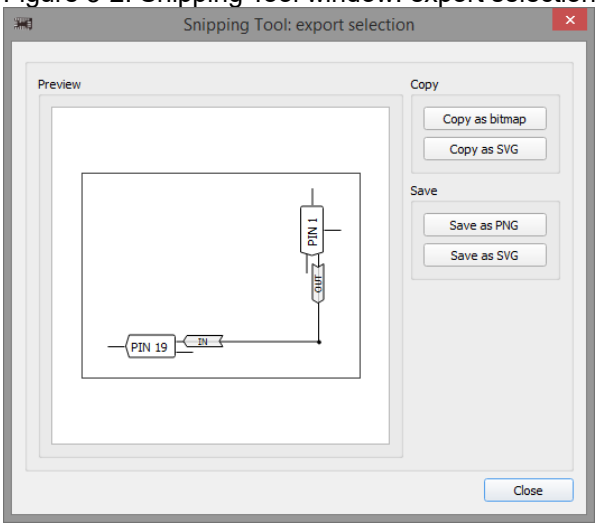
Click Tools → Snipping Tool, select style of screenshot area (Figure 3-1)

Figure 3-1. Snipping Tool window with style selection



Select area and copy to clipboard or save image in Bitmap/PNG/SVG format (Figure 3-2)

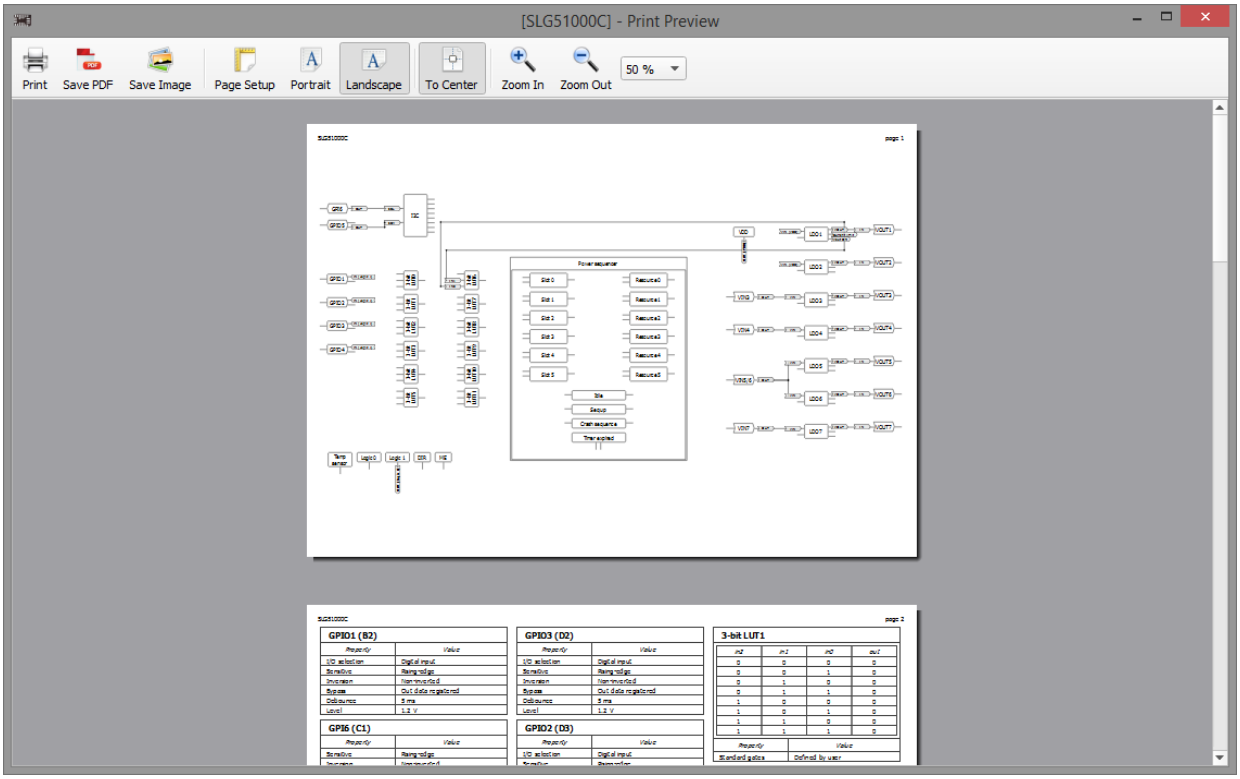
Figure 3-2. Snipping Tool window: export selection



4. Print Function

Print window shows the composed and ready-to-print diagram with block properties and its values. In this window, the user cannot change the position of the components or the other elements in the diagram. The user can only choose the advanced settings for printing or saving to the file.

Figure 4-1. Print window with block properties and values



Print options:

- Choose orientation of the diagram on a paper (landscape or portrait)
- Fit diagram to center
- Zoom in or zoom out
- Choose the size or type of paper
- Save the finished diagram into a PDF/Image file
- Print diagram and block properties

5. Rules Checker

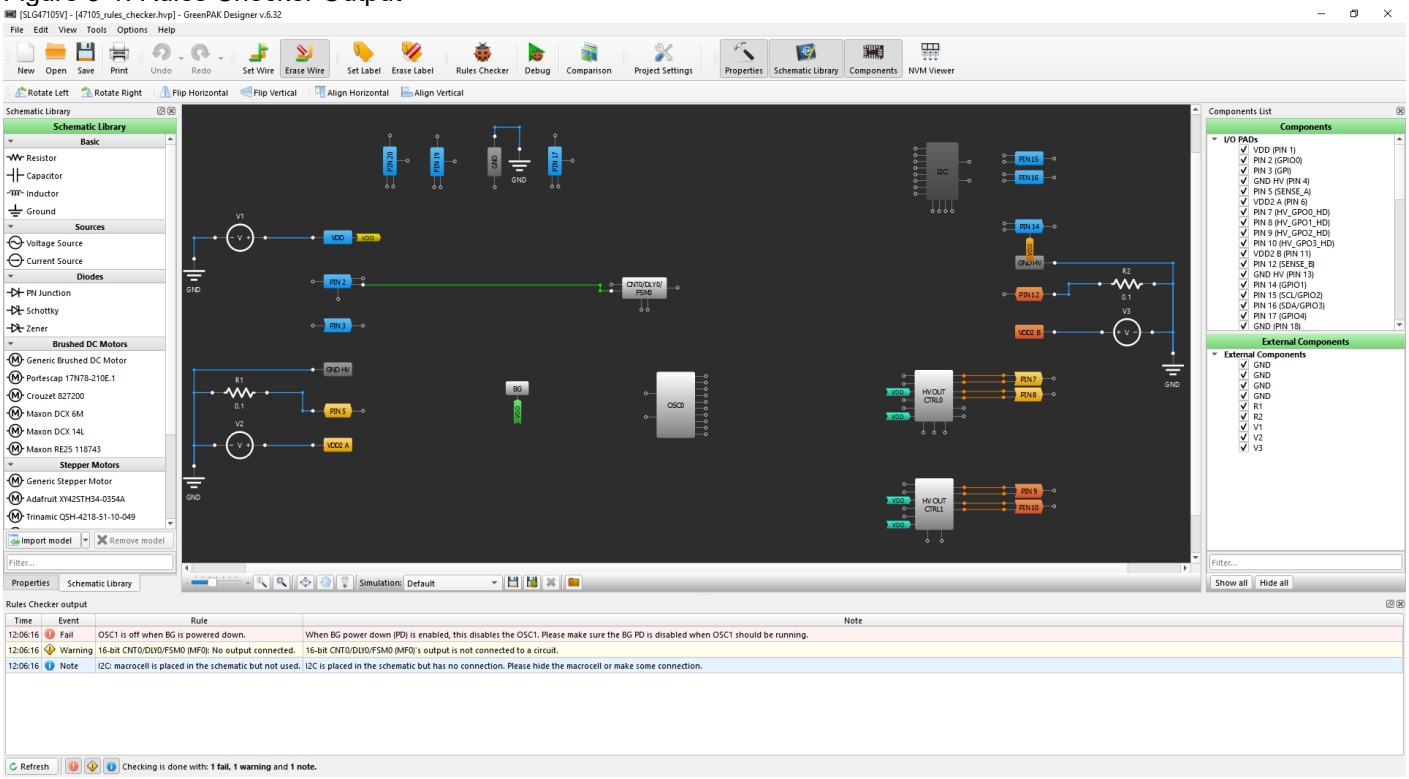
This tool allows checking current project errors, for example, incorrect block connections or settings. Rules Checker has three types of messages:

Fail - this message is generated when there is a significant error in design that will not work under any conditions.

Warning - this message is generated when one or more blocks may contain incorrect connections or settings in the design. This does not mean that there is an error. It only notifies the user to check the connections or settings of the blocks.

Note - this message is generated to remind the user to check for correct settings.

Figure 5-1. Rules Checker Output



In order to check the design, click the Rules Checker button on the tool bar in Tools menu. Rules Checker Window can be called by clicking Rules checker output in View menu. Rules checker output consists of three parts:

1. Event – shows message type (Fail, Warning, Note).
2. Rule – information about the message.
3. Note – recommendations on how to correct the error or error explanation.

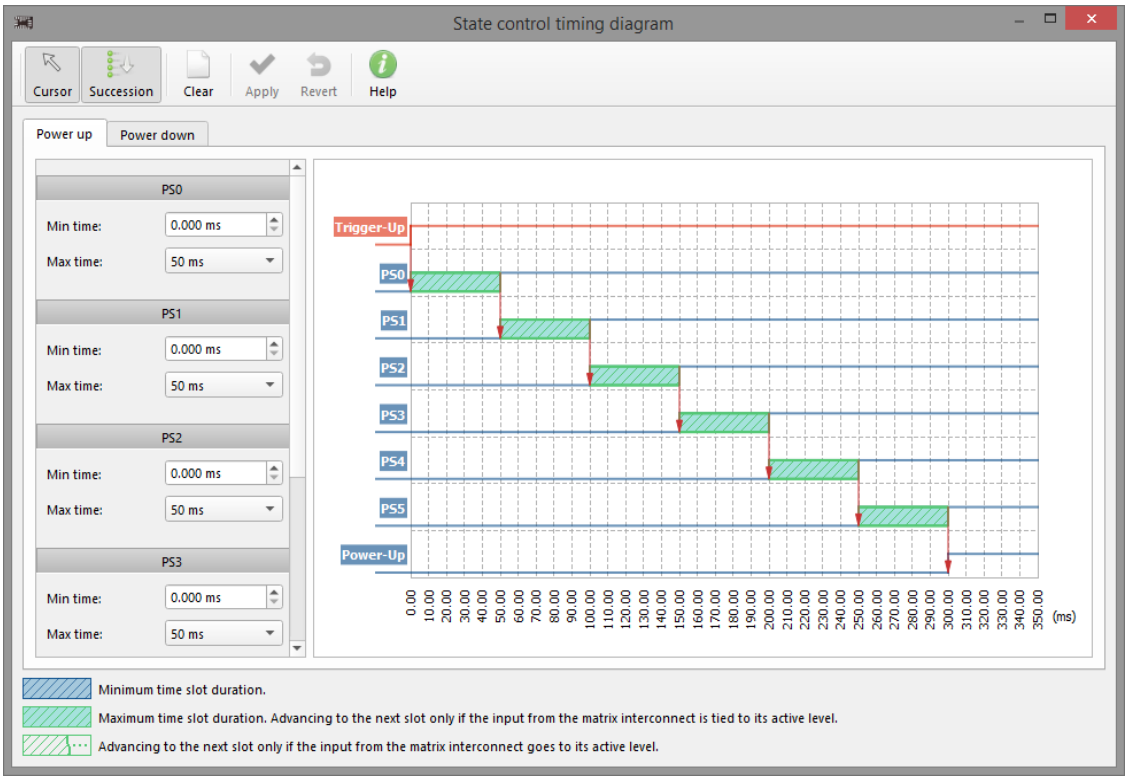
6. Timing diagram

The supply controller provides a flexible power sequencer that controls the power-up and power-down timings for the six resource enable outputs feeding the matrix interconnect. The timing sequence is divided into six slots or discrete periods of time between events. There are two dedicated configurable sequences (up and down). Initiation of a sequence is performed with the trigger-up and trigger-down control signals from the matrix interconnect.

The Power sequencer supports, One-Time Programmable (OTP) configurable, minimum and maximum slot duration limits for each slot in each of the power sequences.

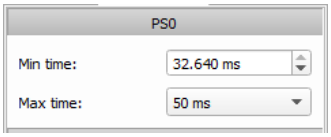
Timing diagram state control allows to configure the Power sequencer minimum and maximum slot durations provided for each slot and for both the up and down sequences (Figure 6-1).

Figure 6-1. Timing diagram window



The time duration in a given slot is limited to the minimum duration regardless of the state of the power-up and power-down signals from the matrix interconnect. The time duration in a given slot is limited to the maximum slot duration, when maximum duration control is configured as enabled in OTP.
Slot duration minimum timers support a range of 0 ms to 32.64 ms with a resolution of 128 µs.
Slot duration maximum timers support options of (0, 10, 30, or 50) ms (Figure 6-2).

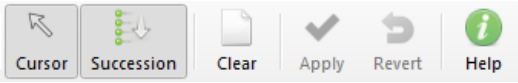
Figure 6-2. State minimum and maximum time



Timing diagram options (Figure 6-3):

- Cursor – shows time label when cursor is placed over the timing diagram;
- Succession – shows Power sequencer state transitions on timing diagram;
- Clear – clears all PS time settings to default;
- Apply – saves all min and max time parameters of PS, changed by user;
- Revert – discards all min and max time parameters of PS, changed by user;
- Help – shows help.

Figure 6-3. Timing diagram options



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