

User Manual DA913X-30 Customer EVB UM-PM-64

Abstract

This document is a user manual for the DA913x-30 Customer EVB for the DA9130, DA9131 and DA9132 PMICs. This board is referred through the document as "EVB". It provides the basic information for configuring and using the EVB.



Contents

| Ab | strac | : | | |
|-----|--------|-----------|------------------------------------|---|
| Со | ntent | s | | 1 |
| Fig | jures. | | | 2 |
| Tal | bles | | | 2 |
| 1 | Term | ns and D | Pefinitions | 3 |
| 2 | Refe | rences | | 3 |
| 3 | Intro | duction. | | 4 |
| 4 | Eval | uation B | oard Hardware | 4 |
| | 4.1 | Quick S | Start | 5 |
| | 4.2 | | he Evaluation board | |
| | | 4.2.1 | Efficiency measurements | 6 |
| | | 4.2.2 | Load transient measurements | 6 |
| | | 4.2.3 | Output voltage ripple measurements | 7 |
| | 4.3 | Jumper | r configuration | 7 |
| | 4.4 | OTP sp | pecific configuration | 8 |
| Re | visior | n History | / | 9 |
| | | | | |
| | | | | |
| Fi | gure | es | | |
| Fig | ure 1: | DA913x | c-30 Evaluation Board | ∠ |
| Fig | ure 2: | DA913x | c-30 Jumpers and headers location | 5 |
| | | | | |
| | | | | |
| Ta | able | S | | |
| | | | and headers overview | |
| Tal | ble 2: | Jumpers | and headers complete list | 7 |
| | | | OTP configuration | |
| Γal | ble 4: | DA9131 | OTP configuration | 8 |

© 2022 Dialog Semiconductor



1 Terms and Definitions

EVB Evaluation board

PMIC Power management integrated circuit

PWM mode Fixed frequency mode using Pulse Width Modulation
PFM mode Variable frequency mode improving efficiency at low loads

Auto mode Automatic mode switching from PFM to PWM depending on load

2 References

- [1] DA9130 Datasheet, Dialog Semiconductor.
- [2] DA9131 Datasheet, Dialog Semiconductor.
- [3] DA9132 Datasheet, Dialog Semiconductor
- [4] DA913x-30-A1_sch Schematics, Dialog Semiconductor

Note 1 References are for the latest published version, unless otherwise indicated.



3 Introduction

Dialog Semiconductor's DA9130, DA9131 and DA9132 devices are power management ICs with integrated power FETs, see datasheets [1][2][3]. The DA9130 is configured as a single-channel dual-phase buck converter, while the DA9131/DA9132 are configured as a two channel, one-phase buck converters.

4 Evaluation Board Hardware

The DA913x-30-A Customer Evaluation board referred below as "EVB" enables the measurement and evaluation of the DA9130/DA9131/DA9132 PMIC.



Figure 1: DA913x-30 Evaluation Board



4.1 Quick Start

The EVB allows to use the DA9130 dual-phase 10A buck or DA9131-DA9132 dual-channel 5A bucks.

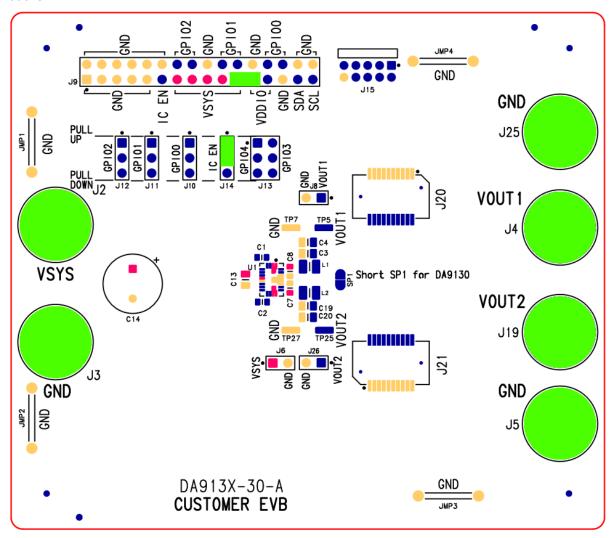


Figure 2: DA913x-30 Jumpers and headers location

Connections from the table below are highlighted in green.

Table 1: Jumpers and headers overview

| Connection | on | Description | | Default | Location | |
|------------|----------------|------------------------------|--------------------------------------|--------------------------------------|---|--|
| J14 | | IC_EN | | Jumper fitted to pull-up position | Top-left, 4th jumper from the left | |
| J9 | | GPIO header | | Jumper between VSYS and VDDIO | TOP left, jumper on positions 21 and 23 | |
| J2 | J2 J3 VSYS GND | | Supply from PSU, 4V - 5A recommended | Left of EVB | | |
| J4 | J25 | VOUT1 | GND | Channel 1 output | Top right of EVB | |
| J5 | J19 | VOUT2 ^{[Note} 2] | GND | Channel 2 ^[Note 2] output | Bottom right of EVB | |

Note 2 VOUT2 is connected to VOUT1 on DA9130 boards.



4.2 Using the Evaluation board

Before going any further, it is recommended to make sure the 4mm banana connectors are properly tightened (150N.cm maximum recommended), as can come loose after shipping and reflow cycles.

The default use case is to connect a PSU to Vsys, with the positive on J2 and the negative/GND on J3. The PSU should be capable of supplying at least 6 A at 3-5.5V and should be capable of remote sensing.

Once the jumpers are set and the PSU is connected, you can switch on the PSU and probe the voltage on the output rails (J4 - J25 and J5 - J19) in order to make sure the setup functions correctly.

4.2.1 Efficiency measurements

It is necessary to use a reliable PSU and load, to use remote sensing as much as possible and to keep the wiring short and tidy to minimize parasitics.

The PSU should supply *Vsys* between J2 and J3 (4mm banana jacks), and its remote sense and input voltage measurement should be connected to J6.

The load can be connected to the output across J4 - J25 (4mm banana jacks), or to J20 (board edge/blade connector), and its remote sense and output voltage measurement should be connected to J8.

For DA9131 and DA9132, the load can also be connected on the second channel across J5 - J19 or J21. Remote sense and output voltage measurement should be connected to J26.

lin can be measured using an ammeter placed in series between J2 and the PSU.

lload can be measured using an ammeter placed in series between J4 or J20 and the load (J5 or J21 and the load for the second channel).

Vsys can be measured across J6, which is connected close to the input capacitors.

Vout can be measured across J8 (or J26 for the second channel), which is connected close to the output capacitors.

The efficiency is obtained through this formula for various voltages and loads:

$$Pin = Vsys * Iin$$
 $Pout = Vout * Iload$
 $\eta = \frac{Pout}{Pin}$

- **Note 3** In case of the DA9131 and DA9132 chips, make sure that the load and the load sense are connected to the same channel.
- **Note 4** In case of the DA9130 chip, it is possible to use the connections from both channels since they are connected in parallel.

4.2.2 Load transient measurements

Just as for the efficiency measurements. it is necessary to use a reliable PSU, to use remote sensing where possible and to keep the wiring short and tidy to minimize parasitics.

The PSU should supply *Vsys* between J2 and J3 (4mm banana jacks), and its remote sense and input voltage measurement should be connected to J6.

The pulse load should be connected to J20 (board edge/blade connector). The wiring impedance is critical here.

For DA9131 and DA9132, the load can also be connected on the second channel on J21.

lload should be monitored on the pulse load, and *Vout* can be measured across J8 (or J26 for the second channel), which is connected close to the output capacitors. The probes and the oscilloscope should have a bandwidth greater than 20MHz.

© 2022 Dialog Semiconductor



4.2.3 Output voltage ripple measurements

It is possible to measure the output voltage ripple using a similar setup as the efficiency, and by measuring the AC voltage across the output capacitors using an oscilloscope. It is recommended to use a differential voltage probe with a bandwidth greater than 20MHz.

The voltage probe can be connected across J8 or TP5 and TP7 depending on the convenience. Those pins and pads are connected to C3 and C4 using kelvin connections.

For the second channel, the voltage probe can be connected across J26 or TP25 and TP27 depending on the convenience. Those pins and pads are connected to C19 or C20 using kelvin connections.

4.3 Jumper configuration

Table 2: Jumpers and headers complete list

| Connection | | Description | | Default | | |
|--------------|---------|--|--------|--|------------------------------------|--|
| JMP1 to JMP4 | | GND points | | Available for grounding scope probes | Each corner of board | |
| J2 | J3 | VSYS | GND | Supply from PSU, 5V recommended | Left of EVB | |
| J4 | J25 | VOUT1 | GND | Channel 1 output | Top right of EVB | |
| J5 | J19 | VOUT2 ^{[Note} 5] | GND | Channel 2 ^[Note 5] output | Bottom right of EVB | |
| J9 | • | GPIO heade | r | Available for probing or using GPIOs | Top left of EVB | |
| J15 | | I2C dongle h | neader | Internal use | Top of EVB | |
| J10 - J1 | 1 - J12 | GPIO0, 1, 2 pull-up pull-down jumpers | | Can be used to pull up or low each individual GPIO | Below J9 | |
| J13 | | GPIO3 and 4 pull-up pull-down jumpers | | Can be used to pull up or low each individual GPIO | Below J9 | |
| J14 | | IC_EN | | Jumper fitted to pull-up position, can be pulled low to disable the chip | Top-left, 4th jumper from the left | |
| J6 | | VSYS sense | | Available for probing or PSU remote sense | Left of J21 | |
| J8 | | VOUT1 sense | | Available for probing or load remote sense | Left of J20 | |
| J26 | | VOUT2* sense | | Available for probing or load remote sense | Left of J21 | |
| J20 | | VOUT1 | | Channel 1 output | Top right of EVB | |
| J21 | | VOUT2 ^[Note 5] | | Channel 2 ^[Note 5] output | Top right of EVB | |
| SP1 | | Single-dual phase | | Shorted on DA9130, open on DA9131/DA9132 | Center of EVB | |
| TP5 | TP7 | VOUT1 | GND | Unused, available for probing | Center of EVB | |
| TP25 TP27 | | VOUT2* | GND | Unused, available for probing | Center of EVB | |

Note 5 VOUT2 is connected to VOUT1 on DA9130 boards.



4.4 OTP specific configuration

Table 3: DA9130 OTP configuration

| ОТР | Voltage A | Voltage B | GPIO0 | GPIO1 ^[Note 6] GPIO2 [Note 6] | | GPIO3 | GPIO4 | I2C addr. |
|-----|--------------|--------------|------------------|--|-------------------------|-------|-------|--------------|
| 02 | 0.72 | 0.72V | Output enable | Power Good output | NC | SCL | SDA | 0x64 |
| 07 | 0.7V | 0.75V | Output enable | DVC Pull-up: Vout=0.75V Pull-down: Vout=0.7V | Power Good output | SCL | SDA | 0xD0 |
| 08 | 0.8V | 0.85V | Output enable | DVC Pull-up: Vout=0.85V Pull-down: Vout=0.8V | Power Good output | SCL | SDA | 0xD0 |
| 09 | 0.9V | 0.95V | Output enable | DVC Pull-up: Vout=0.95V Pull-down: Vout=0.9V | Power Good output | SCL | SDA | 0xD0 |
| 10 | 1.0V | 1.05V | Output enable | DVC Pull-up: Vout=1.05V Pull-down: Vout=1.0V | Power Good output | SCL | SDA | 0xD0 |

Table 4: DA9131 OTP configuration

| ОТР | Vout1 A | Vout1 B | Vout2 A | Vout2 B | GPIO0 | GPIO1 | GPIO2 [Note 6] | GPI O3 | GPIO 4 | I2C addr. |
|-----|------------|------------|------------|------------|--|--|--|-----------|-----------|--------------|
| 41 | 0.85V | 0.85V | 0.9V | 0.9V | Channel 1 output enable, pull-up to enable | Channel 2 output enable, pull-up to enable | Power Good 1 output | SCL | SDA | 0x66 |
| 42 | 0.8V | 0.8V | 0.8V | 0.8V | Unused | Channel 1 output enable, pull-up to enable | Channel 2 output enable, pull-up to enable | SCL | SDA | 0xD0 |
| 43 | 0.8V | 1 | 1.65V | 1.65V | Channel 1 DVC Pull-up: Vout=0.8 V Pull- down: Vout=1.0 V | Channel 1 output enable, pull-up to enable | Channel 2 output enable, pull-up to enable | SCL | SDA | 0xD2 |

Note 6 Items in **bold** are output only.



Revision History

| Revision | Date | Description |
|----------|-------------|------------------|
| 1.1 | 04-Feb-2022 | Update |
| 1 | 26-Nov-2021 | Initial version. |

Status Definitions

| Status | Definition |
|----------------------|--|
| DRAFT | The content of this document is under review and subject to formal approval, which may result in modifications or additions. |
| APPROVED or unmarked | The content of this document has been approved for publication. |

Disclaimer

Unless otherwise agreed in writing, the Dialog Semiconductor products (and any associated software) referred to in this document are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of a Dialog Semiconductor product (or associated software) can reasonably be expected to result in personal injury, death or severe property or environmental damage. Dialog Semiconductor and its suppliers accept no liability for inclusion and/or use of Dialog Semiconductor products (and any associated software) in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Information in this document is believed to be accurate and reliable. However, Dialog Semiconductor does not give any representations or warranties, express or implied, as to the accuracy or completeness of such information. Dialog Semiconductor furthermore takes no responsibility whatsoever for the content in this document if provided by any information source outside of Dialog Semiconductor.

Dialog Semiconductor reserves the right to change without notice the information published in this document, including, without limitation, the specification and the design of the related semiconductor products, software and applications. Notwithstanding the foregoing, for any automotive grade version of the device, Dialog Semiconductor reserves the right to change the information published in this document, including, without limitation, the specification and the design of the related semiconductor products, software and applications, in accordance with its standard automotive change notification process.

Applications, software, and semiconductor products described in this document are for illustrative purposes only. Dialog Semiconductor makes no representation or warranty that such applications, software and semiconductor products will be suitable for the specified use without further testing or modification. Unless otherwise agreed in writing, such testing or modification is the sole responsibility of the customer and Dialog Semiconductor excludes all liability in this respect.

Nothing in this document may be construed as a license for customer to use the Dialog Semiconductor products, software and applications referred to in this document. Such license must be separately sought by customer with Dialog Semiconductor.

All use of Dialog Semiconductor products, software and applications referred to in this document is subject to Dialog Semiconductor's Standard Terms and Conditions of Sale, available on the company website (www.dialog-semiconductor.com) unless otherwise stated.

Dialog, Dialog Semiconductor and the Dialog logo are trademarks of Dialog Semiconductor Plc or its subsidiaries. All other product or service names and marks are the property of their respective owners.

© 2022 Dialog Semiconductor. All rights reserved.

RoHS Compliance

Enquiry Form

Dialog Semiconductor's suppliers certify that its products are in compliance with the requirements of Directive 2011/65/EU of the European Parliament on the restriction of the use of certain hazardous substances in electrical and electronic equipment. RoHS certificates from our suppliers are available on request.

Contact Dialog Semiconductor

General Enquiry:

Local Offices:

https://www.dialog-semiconductor.com/contact/sales-offices

Application Note Revision 1.1 01-Feb-2022

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES ("RENESAS") PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu, Koto-ku, Tokyo 135-0061, Japan www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.