USB3.0 Board Layout Guideline

Document No ISG-ED1-010033
Date Published Dec.3. 2012

Renesas Electronics
www.renesas.com
Printed in Japan

[MEMO]

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation of these circuits, software, and information in the design of your equipment. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from the use of these circuits, software, or information.
2. Renesas Electronics has used reasonable care in preparing the information included in this document, but Renesas Electronics does not warrant that such information is error free. Renesas Electronics assumes no liability whatsoever for any damages incurred by you resulting from errors in or omissions from the information included herein.
3. Renesas Electronics does not assume any liability for infringement of patents, copyrights, or other intellectual property rights of third parties by or arising from the use of Renesas Electronics products or technical information described in this document. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
4. You should not alter, modify, copy, or otherwise misappropriate any Renesas Electronics product, whether in whole or in part. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from such alteration, modification, copy or otherwise misappropriation of Renesas Electronics product.
5. Renesas Electronics products are classified according to the following two quality grades: "Standard" and "High Quality". The recommended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below.

   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; and industrial robots etc.

   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control systems; anti-disaster systems; anti-crime systems; and safety equipment etc.

   Renesas Electronics products are neither intended nor authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems, surgical implantations etc.), or may cause serious property damages (nuclear reactor control systems, military equipment etc.). You must check the quality grade of each Renesas Electronics product before using it in a particular application. You may not use any Renesas Electronics product for any application for which it is not intended. Renesas Electronics shall not be in any way liable for any damages or losses incurred by you or third parties arising from the use of any Renesas Electronics product for which the product is not intended by Renesas Electronics.
6. You should use the Renesas Electronics products described in this document within the range specified by Renesas Electronics, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas Electronics shall have no liability for malfunctions or damages arising out of the use of Renesas Electronics products beyond such specified ranges.
7. Although Renesas Electronics endeavors to improve the quality and reliability of its products, semiconductor products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Further, Renesas Electronics products are not subject to radiation resistance design. Please be sure to implement safety measures to guard them against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas Electronics product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or systems manufactured by you.
8. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. Please use Renesas Electronics products in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Renesas Electronics assumes no liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
9. Renesas Electronics products and technology may not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You should not use Renesas Electronics products or technology described in this document for any purpose relating to military applications or use by the military, including but not limited to the development of weapons of mass destruction. When exporting the Renesas Electronics products or technology described in this document, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations.
10. It is the responsibility of the buyer or distributor of Renesas Electronics products, who distributes, disposes of, or otherwise places the product with a third party, to notify such third party in advance of the contents and conditions set forth in this document, Renesas Electronics assumes no responsibility for any losses incurred by you or third parties as a result of unauthorized use of Renesas Electronics products.
11. This document may not be reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products, or if you have any other inquiries.

(Note 1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its majority-owned subsidiaries.

(Note 2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

Contents

1. Introduction

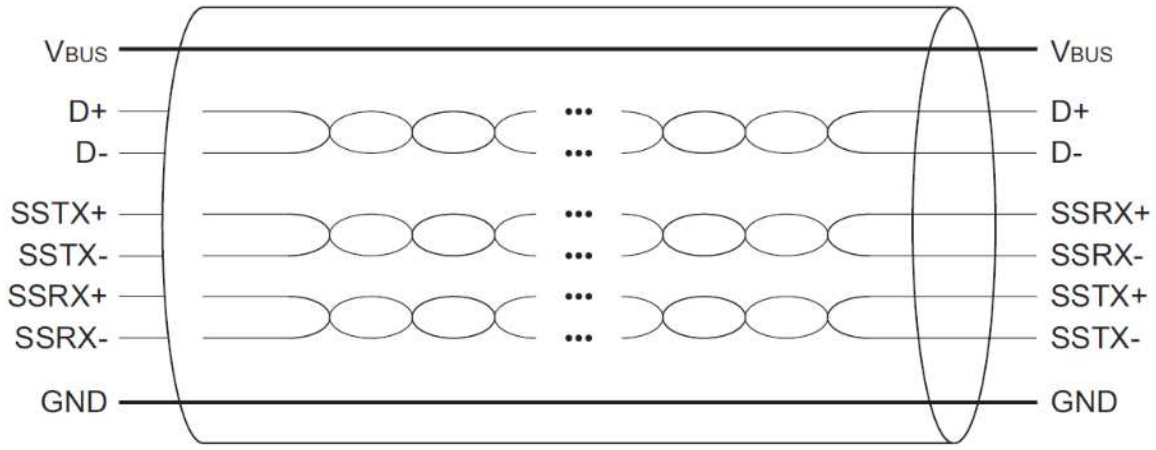
This document describes guidelines for designing boards using Renesas Electronics USB3.0 devices. These guidelines offer Renesas Electronics' recommendations with no guarantee of results.

2. Overview on USB 3.0

USB 3.0 is one of the state-of-the-art interconnecting technologies for both PCs and CE equipment, with performance up to 5 Gbps PHY rate, enabling nearly 300MB/s data transfer. That is only one tenth of the time consumption of USB 2.0 Hi-Speed. In the USB 3.0 standard, the expected distance is up to 3m via a dedicated cable compliant with USB IF requirements.

The difference between USB 3.0 and USB 2.0 is tabulated below. On the other hand, the policy for ease of use is inherited from USB 2.0, and there is well-considered backward compatibility in USB 3.0.

Standard	USB 2.0	USB 3.0
Name for maximum speed	Hi-Speed USB (HS)	SuperSpeed USB (SS)
Maximum PHY rate	480Mbps	5.0Gbps
Maximum range	5m	3m nominal
Coding	NRZI	8B/10B
Use of SSC(Spectrum spread clock)	Not mandatory	Mandatory
Transfer mode	Half duplex	Dual simplex
Cable signal count	Two (D+, D-)	Six (SSTX+, SSTX-, SSRX+, SSRX-, D+, D-)
Ability of power supply by every VBUS	5V/100mA in low-power device 5V/500mA in high-power device	5V/150mA in low-power device 5V/900mA in high-power device



(Topology of USB 3.0 wiring)

To achieve the 5 Gbps speed, all of the Renesas Electronics USB 3.0 devices are carefully designed to implement functions that allow all the customers to realize the USB 3.0 solution easily. However, inevitable difficulties arise during every design because USB 3.0 is based on an extremely high-speed data transfer technique as well as very high frequency circuits, or RF techniques that extremely few engineers understand. As a USB pioneer, Renesas Electronics provides this board design guide as the customers' reference based on good knowledge of RF and high-speed techniques.

3. USB 3.0 Board Design Guidelines

The guidelines are the reference for any designer to realize any USB 3.0 solution that is embedded on a motherboard or main board or subsidiary board in PCs or CE devices, as well as add-in cards or Expresscards. **Please note: all recommendations in this chapter follow the assumption that the material for any board or card is FR-4. Other PCB materials that may be better for high-speed transmission lines are out of scope.**

These guidelines include the following topics:

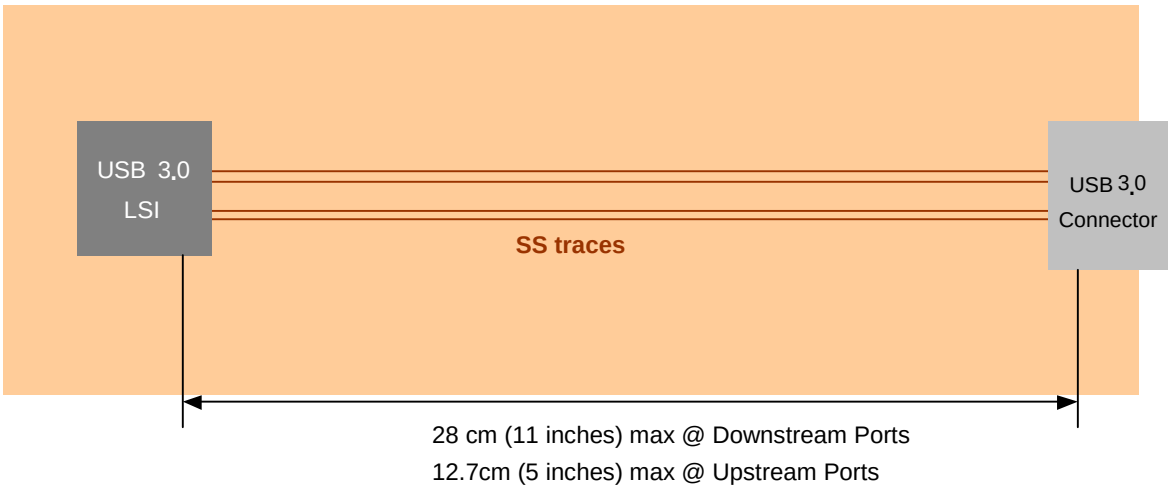
- The SuperSpeed(SS) trace length between data ports on USB 3.0 LSI and connectors at the edge of a card or module
- Placing AC series coupling capacitors for the SS transmission traces
- Trace crossing
- Number of layers
- Ground plane
- Impedance for signal traces
- Routing differential pairs
- Trace bends
- Routing close to USB 3.0 LSI or connector
- Guidelines related to Renesas Electronics USB 3.0 LSI

3.1. The SS trace length

Recommended maximum length of SS trace line on PCB (FR-4)

Downstream ports: Length up to 28 cm (11 inches).

Upstream ports: Length up to 12.7 cm (5 inches).



Note: For designing USB SS trace on PCB, if long run of SS trace over 10cm (4inches) to 28cm (11inches) are needed on the PCB, it's necessary to pay attention to the signal integrity. So it's recommended to keep design rule by this guideline strictly in order to ensure good SS performance.
By carefully designed SS line of good performance, it's possible to drive USB3.0 cable of the long length. Please refer to the example of the attached figures in section 8.Appendix.

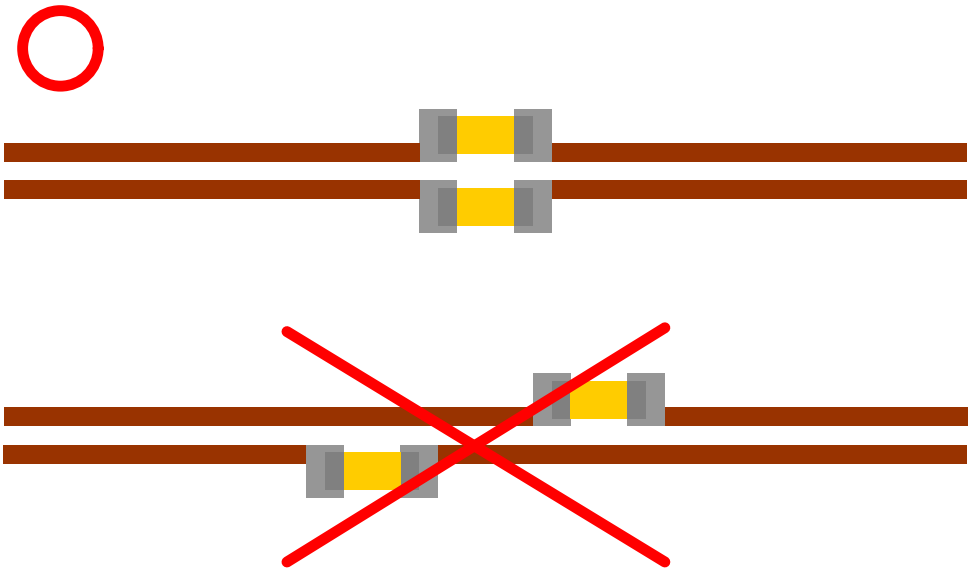
Note: For designing SS trace over 10cm (4inches) on PCB, it's recommended to check the SS compliance test beforehand by following steps.
(1) Making a test channel by PCB of expected to use and checking the differential impedance 90 ohm +/- 10% by TDR method.
(2) Checking this test channel of Differential signal attenuation (SDD21) up to 7.5GHz by network analyzer.
(3) Connecting this test channel to USB3.0 LSI such as an Add-in card and testing the SS compliance test. This test method was defined by USB Implementers Forum (USB-IF).
Then it's possible to judge this PCB test channel trace by this result.

Note: For PCI Express 2.0, length up to 12.5cm (6 inches) on mother board or up to 10cm (4 inches) on any type of daughter card is recommended.

Note: For a board which acts as USB host and has data transfer via PCI Express bus, it is acceptable for the traces for PCI Express signals to be longer than for USB SS. This is because USB traces usually suffer degradation which doesn't apply to on-board systems like PCI Express. If long runs of SS traces are needed on the board, it is better to consider replacing the traces on board with cable wiring having low loss per a unit length. A similar case will happen when using SATA, and a similar option with the help of cable is likely to be effective.

3.2. AC coupling capacitor on the SS signal trace pair

TX trace only, not RX. Place close to the receptacle symmetrically. 0.1uF(100000pF) on each trace is recommended, using a chip ceramic capacitor. See diagram ("O" means ok or good.)



Note: In general, a chip capacitor has intrinsic inductance and so impedance for high frequency signals may be more than the usual expectation. It may cause failure of USB data transfer. If possible choose capacitors having 0.2nH or lower inductance in order to ensure good SS performance.

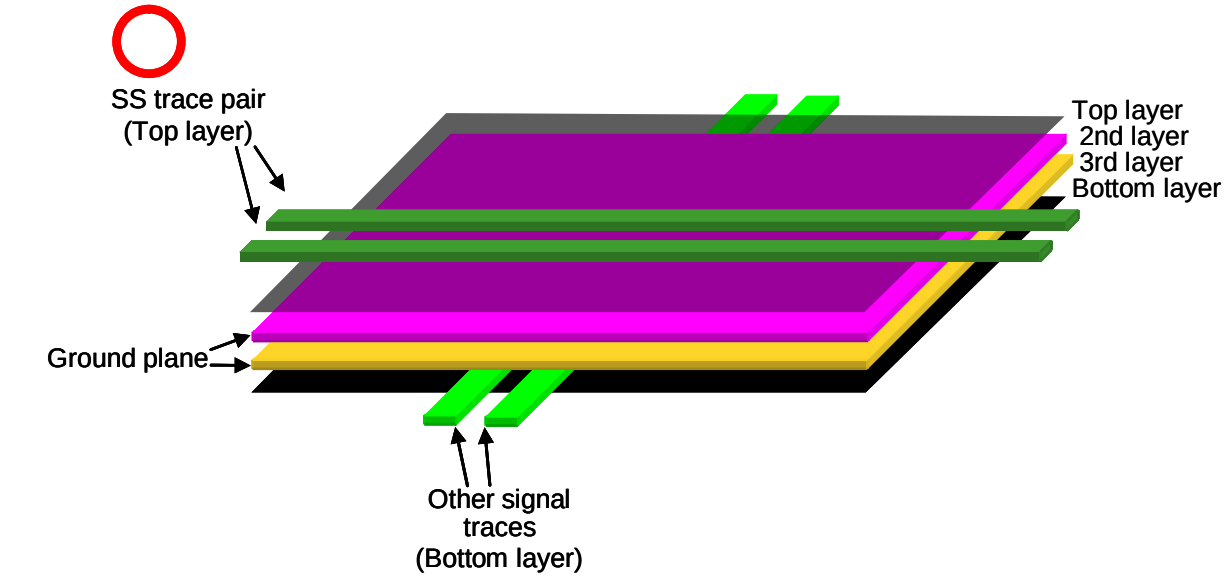
Note: For PCI express signals, this recommendation also applies.

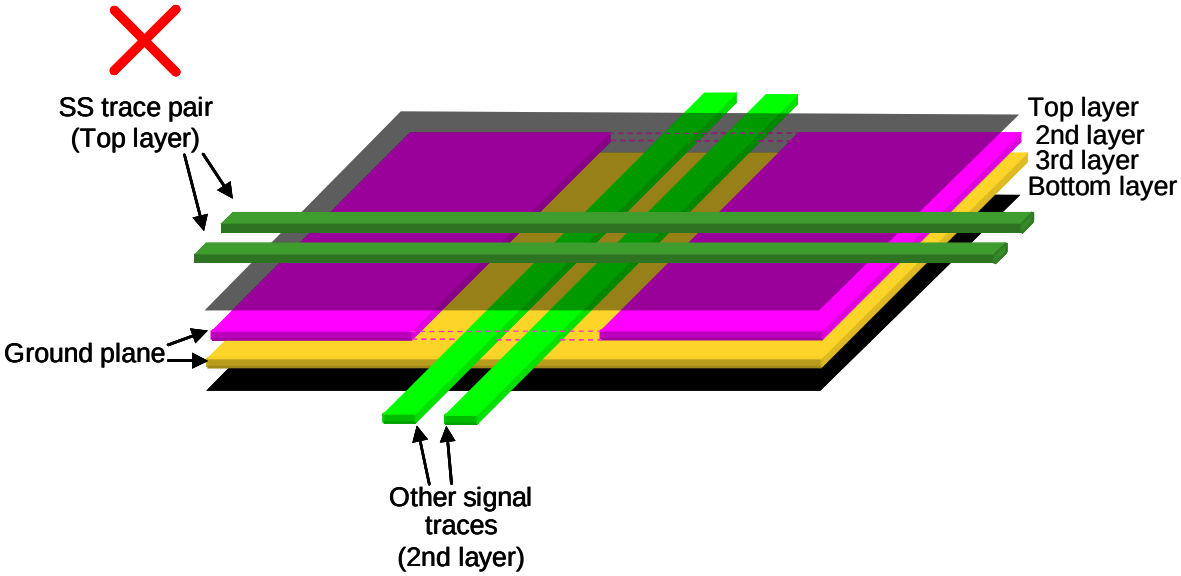
Note: For each differential pair, using capacitors from the same lot is greatly preferred over using capacitors from different lots. Using capacitors from different lots may result in additional common mode noise.

3.3. Trace crossing

At least one layer of ground plane is needed at any crossing of signal traces and any other signal trace or power traces.

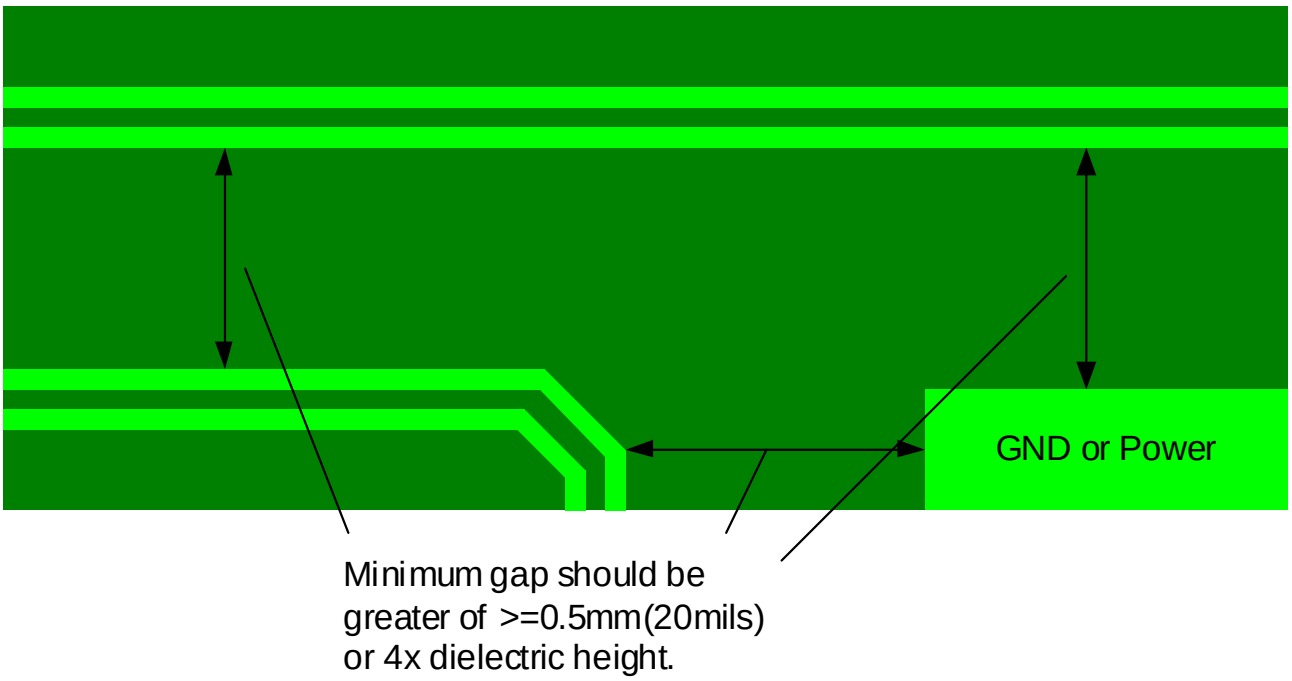
Any crossing on the same layer causes serious problems for system performance.





3.4. Adjacent trace

To avoid crosstalk, maintain an appropriate gap between any different trace. See also section 3.7.



Note: Long side-by-side routing of different signals may allow excessive crosstalk.

3.5. Number of PCB layers

At least four layers are necessary in any case.

Note: Recommended setting is as follows when using a four-layer PCB:

Layer	Method 1	Method 2
Top	Data signal, clock	Power, control signal
2nd	GND	Power, GND
3rd	Power, GND	GND
Bottom	Power, control signal	Data signal, clock

Assure that every data signal trace is routed entirely over the ground plane on an adjacent layer.

3.6. Ground plane

From this section (3.6) to section 3.9 the basic guidelines for routing the differential trace pair are described.

Among these sections there are several factors or restrictions in order to get better performance of USB SS; however, it may be very difficult to achieve all of the layout goals in a limited area.

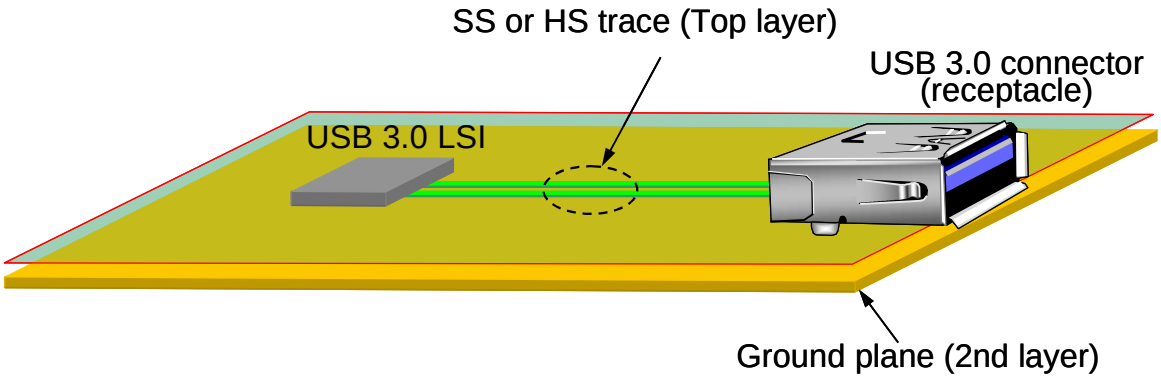
Before explaining detailed guides on individual items, the recommended priority is introduced as shown below.

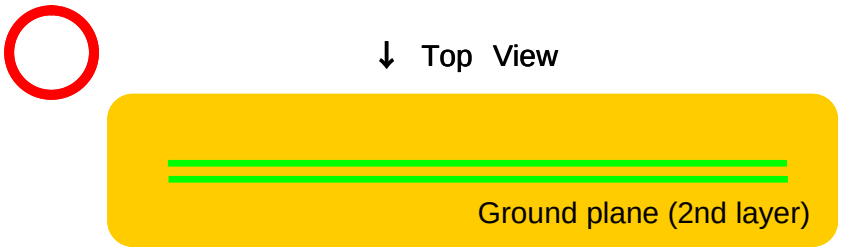
Priority	Item	Related section No.
1 (top priority)	Enough grounding	3.6
2	Keeping differential impedance within 10%	3.7
3	Keeping same length	3.8
4	Symmetrical routing	3.8
5	Routing on one layer, no layer change	3.8
6	No stub	3.9

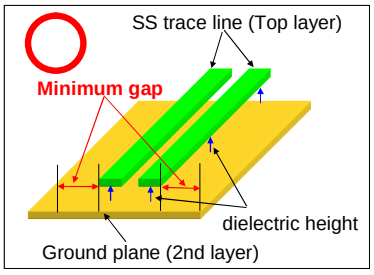
To maintain good performance, there should be huge area of ground plane on the layer next to that on any signal trace.

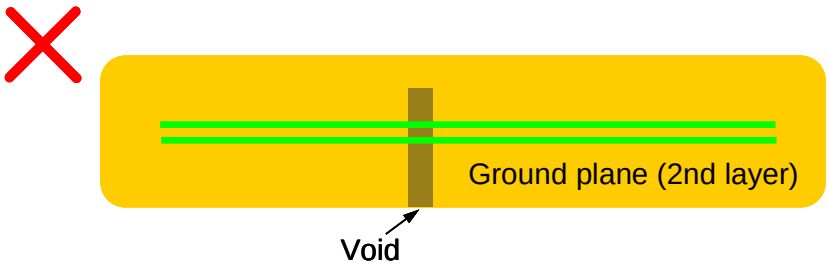
Route every trace entirely over the ground plane.

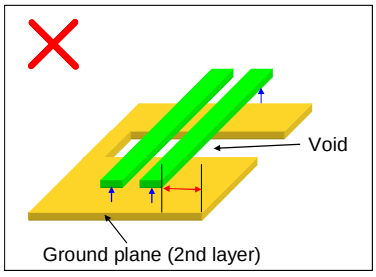
No void, no power plane, or no other signal trace should be allowed in the ground plane under USB-related signal traces.

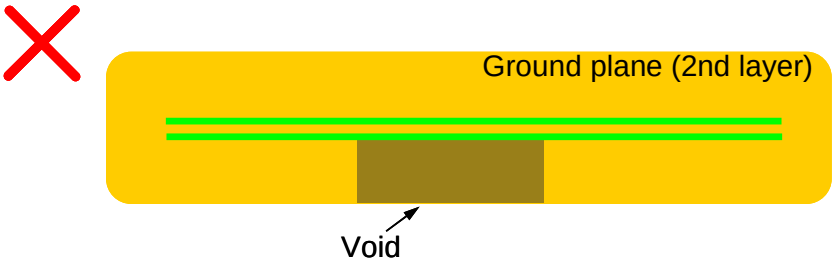


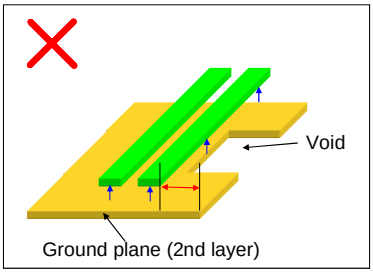


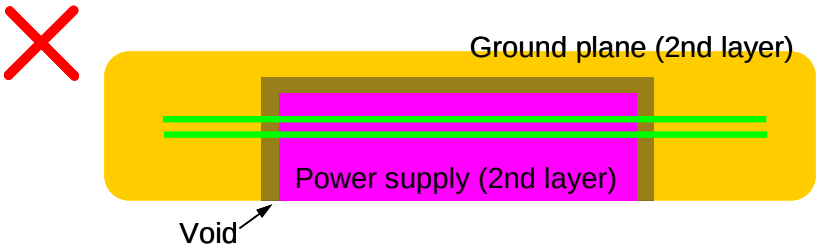


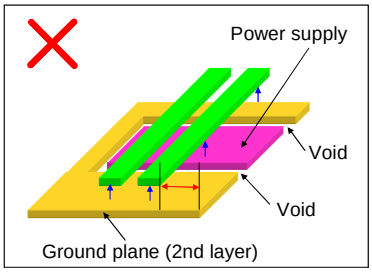





Ground plane (2nd layer)
Void


Void
Ground plane (2nd layer)


Ground plane (2nd layer)
Power supply (2nd layer)
Void


Power supply
Void
Void
Ground plane (2nd layer)

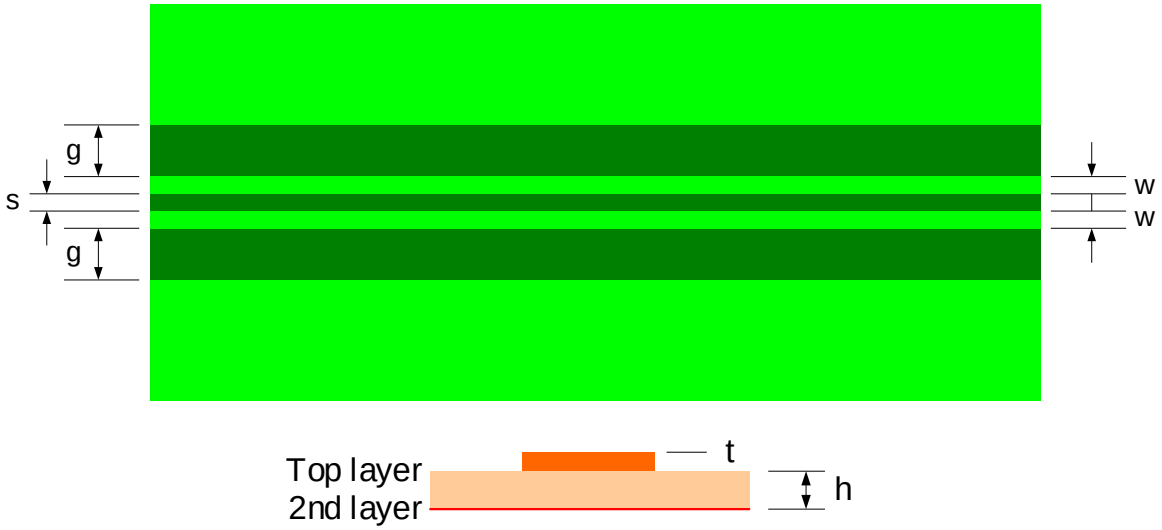
3.7. Line impedance

Signal line impedance of USB is typically 90 Ohms differential. +/-10% accuracy may be allowed.

Fixed width and fixed spacing between traces in a pair should be maintained to avoid impedance mismatch.

Proper gaps are required if any other trace goes nearby.

If the routing layer for a signal trace has to be changed, maintain continuous grounding by putting in an appropriate number of vias.



Dimension example of 90Ohm-differential pair (possible case)

εr	dielectric constant	4.1 (FR4)
h	height of 2nd layer to top layer	0.1mm (4 mils)
t	metal thickness	38 μm (1.5 mils)
w	trace width	0.15 mm (6 mils)
s	intra-pair spacing (within pair)	0.1 mm (4 mils)
g	gap between edges from signal trace and other neighbor plane, trace, or via	0.5 mm (20 mils)

Note: Dielectric of constant for FR-4 varies per material vendor. In addition there is some variation with location on the board.

Note: Differential impedance isn't always twice as much as single-ended impedance due to edge-to-edge coupling of the differential pair.

Note: To reduce unwanted emissions (EMI), it is desirable for the spacing within pair not to exceed trace width.

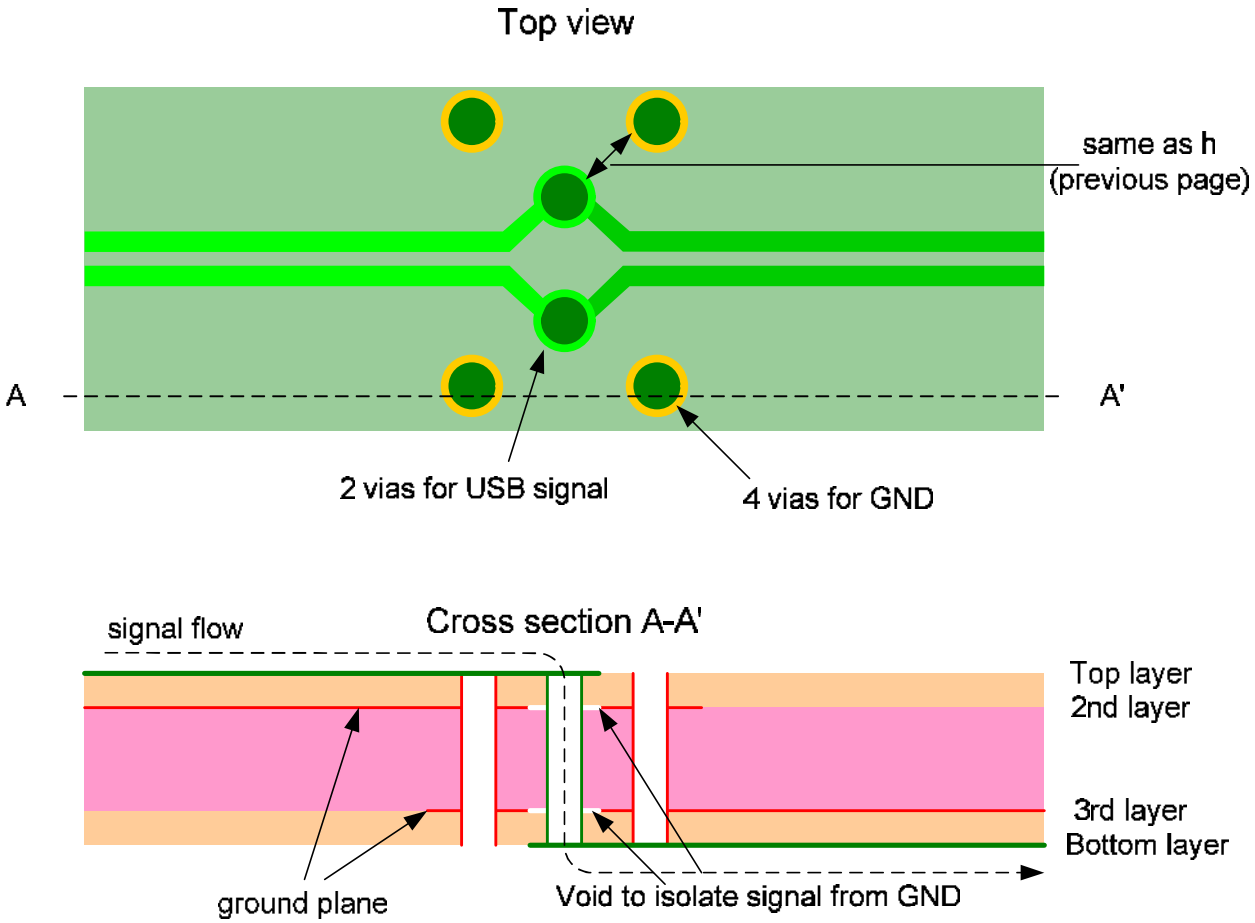
Note: For the metal both on the top and the bottom layer, nickel plating isn't recommended due to low conductivity.

Note: For PCI Express 1.1, differential impedance is 100Ohms nominal, and PCI Express 2.0, differential impedance is 85 Ohms nominal.

Note: When PCI Express 2.0 differential impedance can't be set to 85 Ω by restriction of PCB design rule, it is possible to set at 90 Ω. (max 120 Ω)

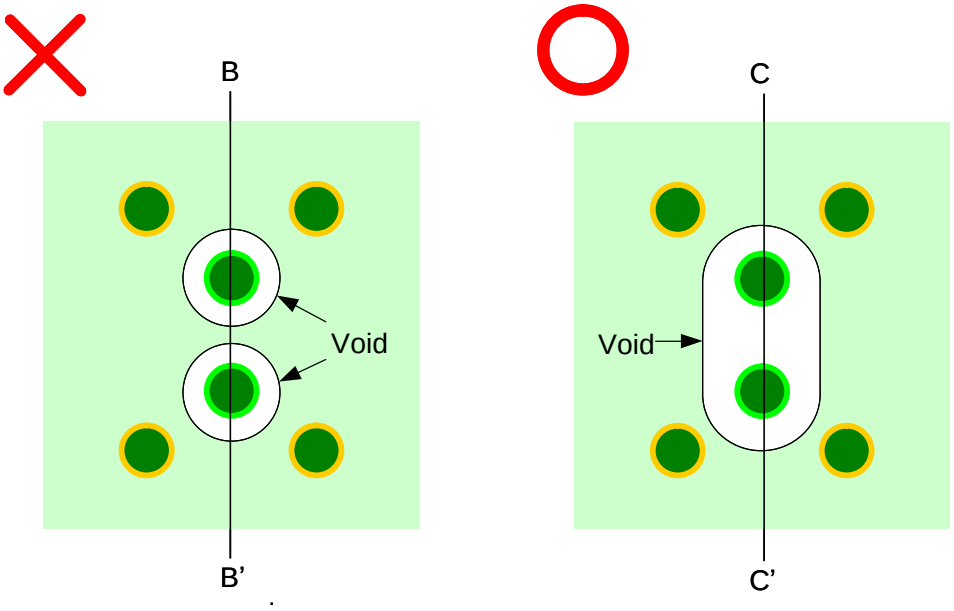
Note: TDR method is suitable for checking the impedance.

Example of layer change



Note: Diameter of the vias in the figures above is almost equal to the trace width w.

Example of layer change



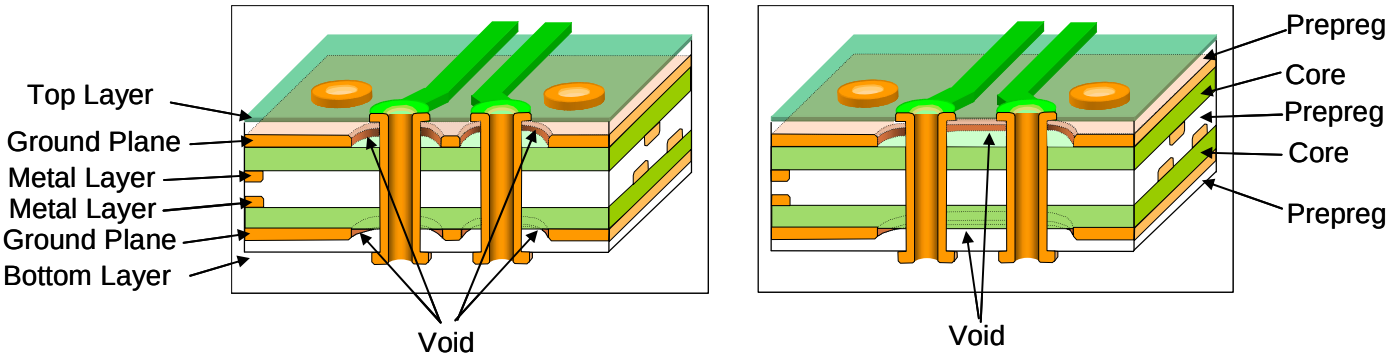
This layout may cause discontinuity of the differential impedance

This layout contains less discontinuity and enables maintaining the differential impedance

Consideration for the inner layers

Cross section B-B'

Cross section C-C'



Example of layer change

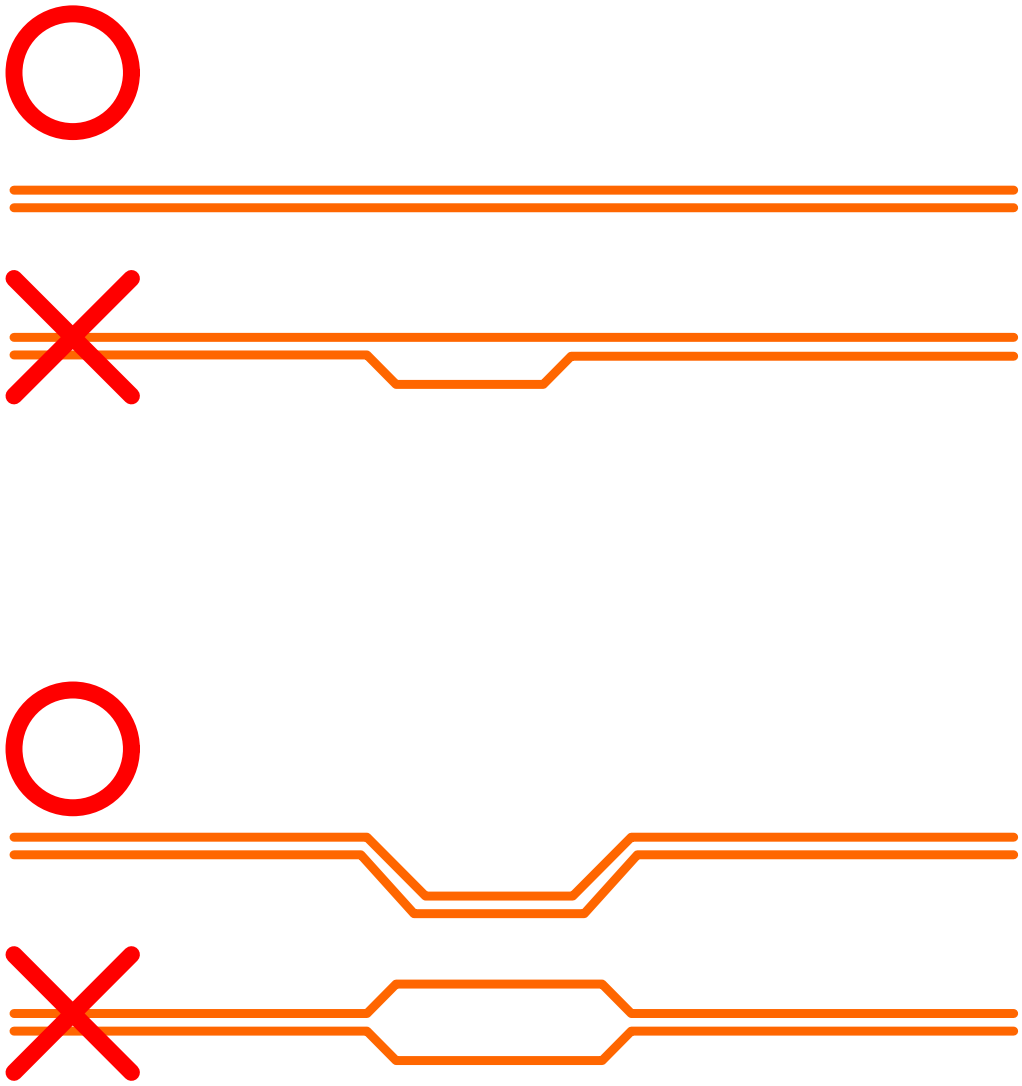
（Cross Section of 6 layer PCB）

3.8. Symmetrical routing

Same length, same width, same layer, fixed spacing are keys to symmetrical routing for any differential data signal of a USB system, keeping fixed impedance.

Length should be matched within 0.12mm (5mils) delta. Adjustment near the connector(receptacle) is desirable if needed (see also section 3.12).

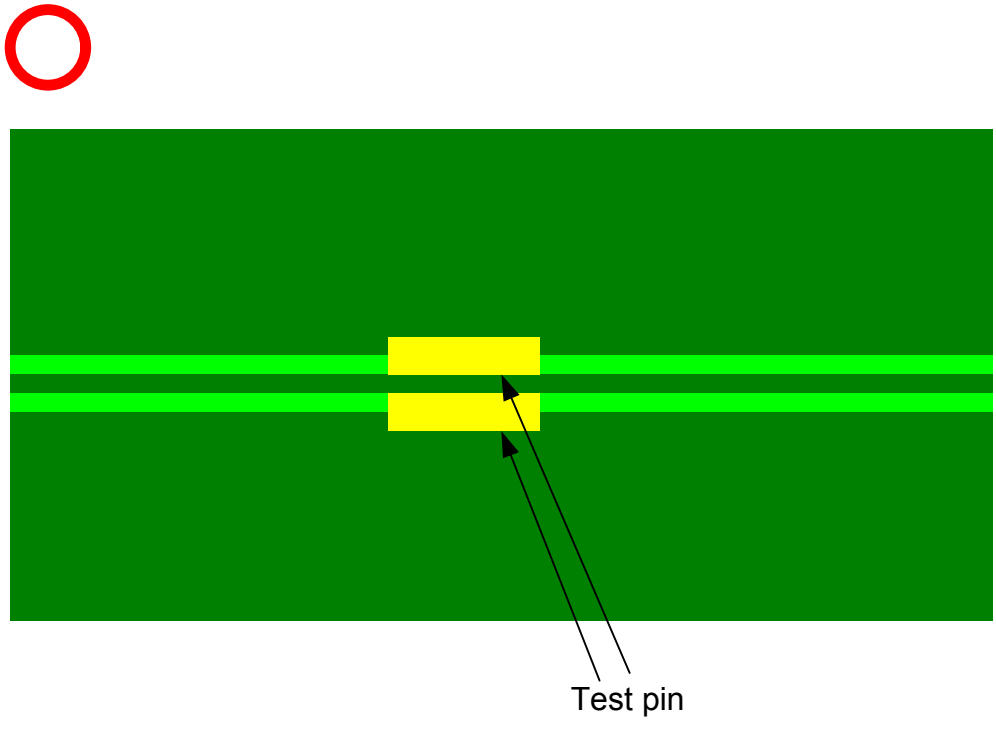
No need to route symmetrically between different pairs, e.g. SSTX and SSRX.

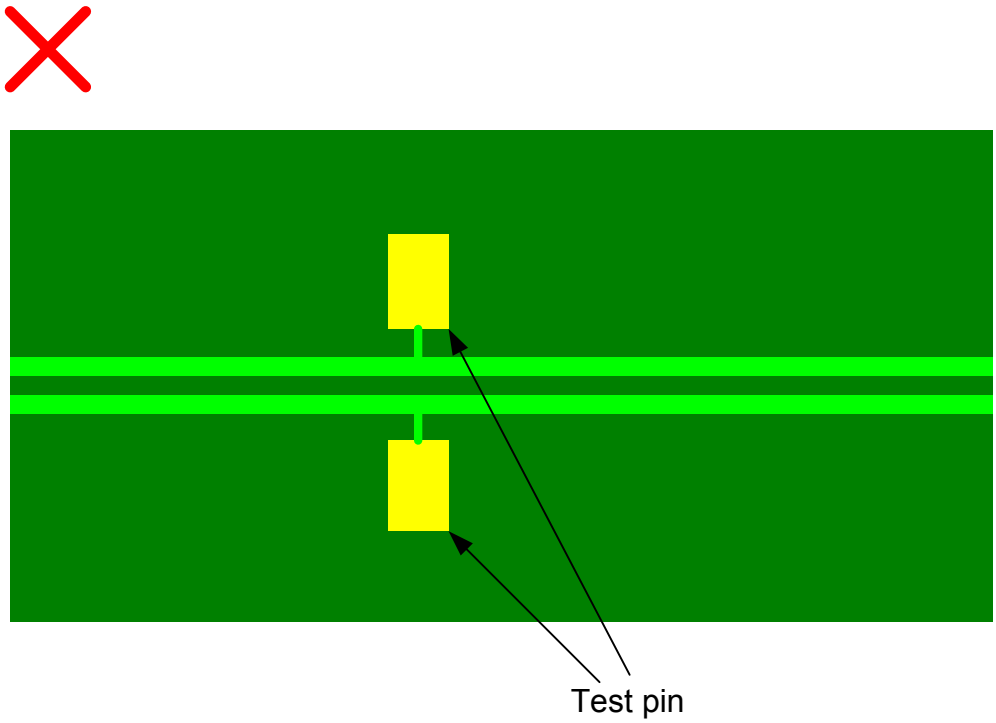


Note; In the case of the lower figure, bottom tracing is more symmetrical geometrically, however the upper one is better to keep a single value of impedance throughout the route by keeping the same spacing between traces.

3.9. Stub on signal traces

No stub on any signal trace.
Also avoid unexpected stubs.





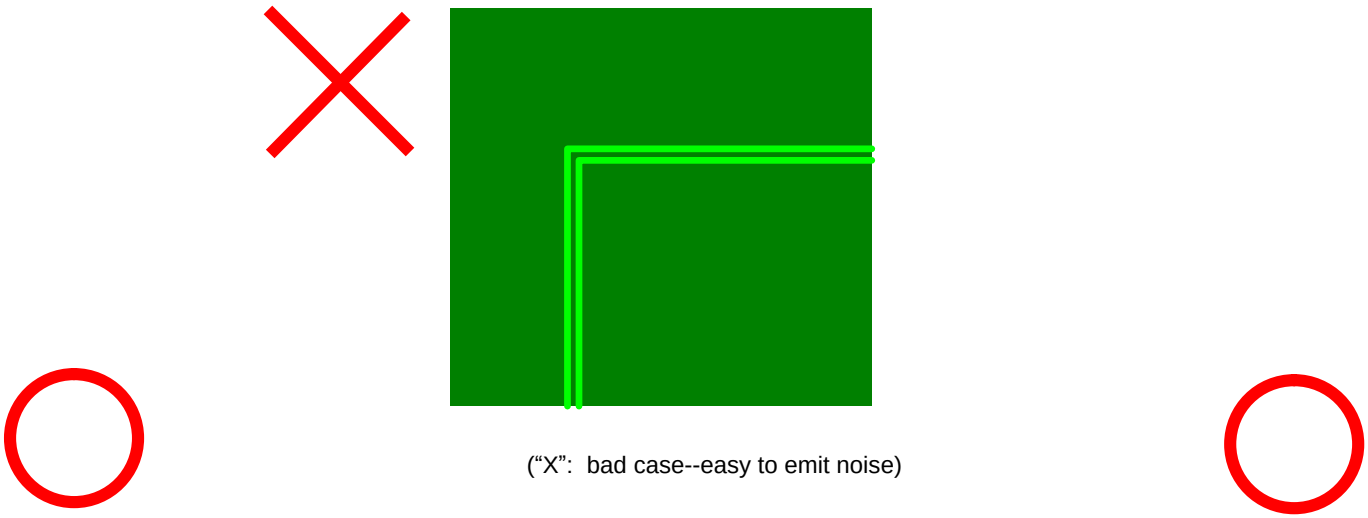
Note: The “X” figure above shows an example of unexpected stubs. For more examples regarding stubs, please see section 3.11. The “O” figure shows avoiding the stubs by placing the test pads in a row with the signal traces.

3.10. Trace Bending

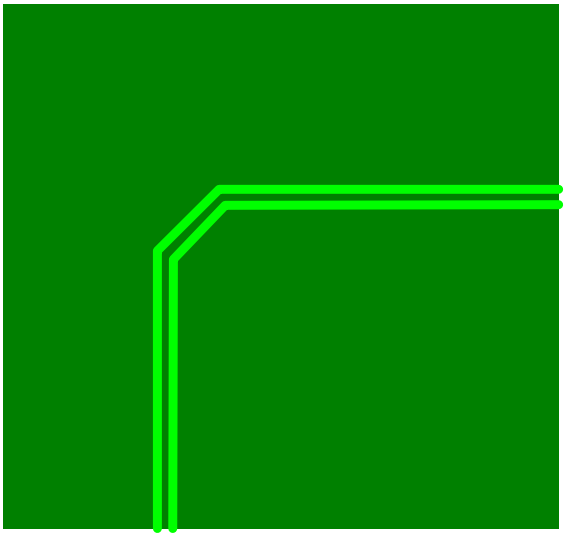
Use as few bends as possible, preferably not more than two bends except for the area close to USB connector or USB LSI, or necessary at a via to change the routing layer.

If necessary, a 45-deg bend or rounded bend is desirable.

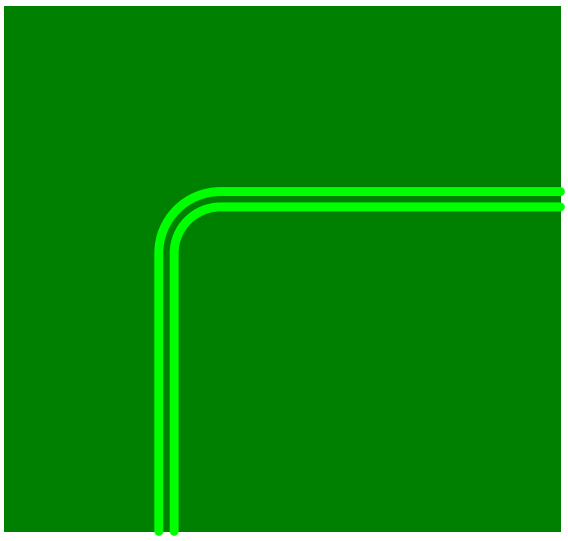
Allow for the length mismatch occurring at any bend, and maintain trace spacing within a differential pair.



("X": bad case--easy to emit noise)



(Good case--45deg. bend)



(Good case--round bend)

3.11. Routing around USB receptacle

Be sure to maintain the impedance of signal traces, avoiding any stubs and removing any routing that causes severe EMC noise problems.

Also be sure not to put any metal between all SS-pair pins on every layer when using receptacles with pins stabbing the PCB.

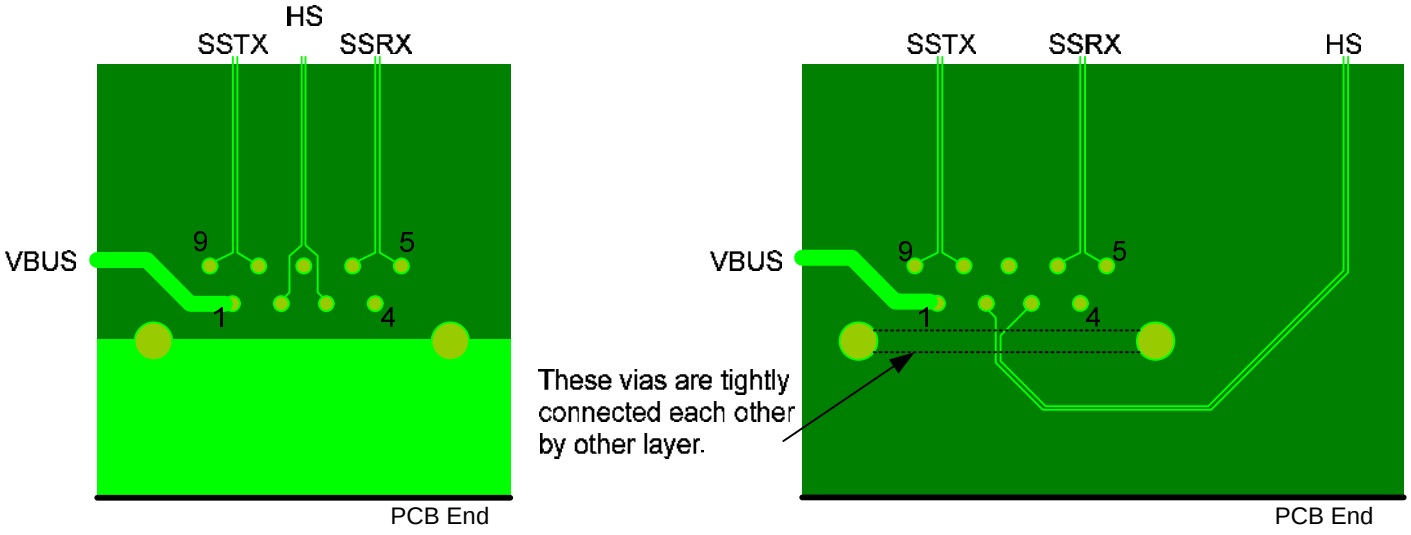
Be careful to avoid any possible crosstalk within

As for VBUS traces, it is necessary to insert a ferrite bead.

As for shielding of USB cables, AC isolation to the ground of the PCB is desired (i.e., proper value of inductor, instead of connecting the cable shield directly to the PCB ground plane).

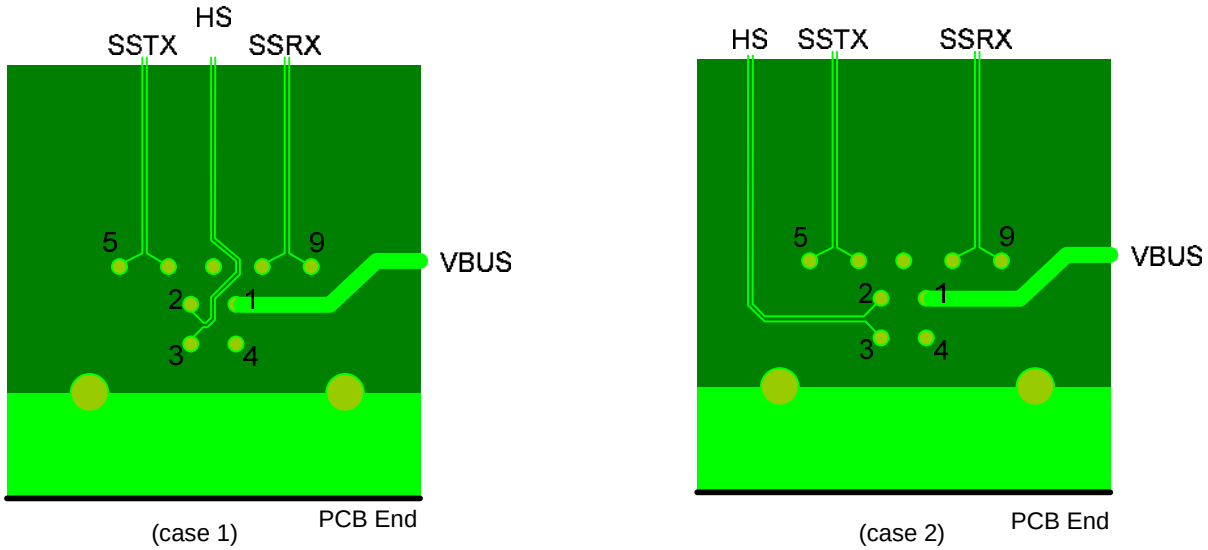
Example of routing on the top layer

(Standard-A receptacle)

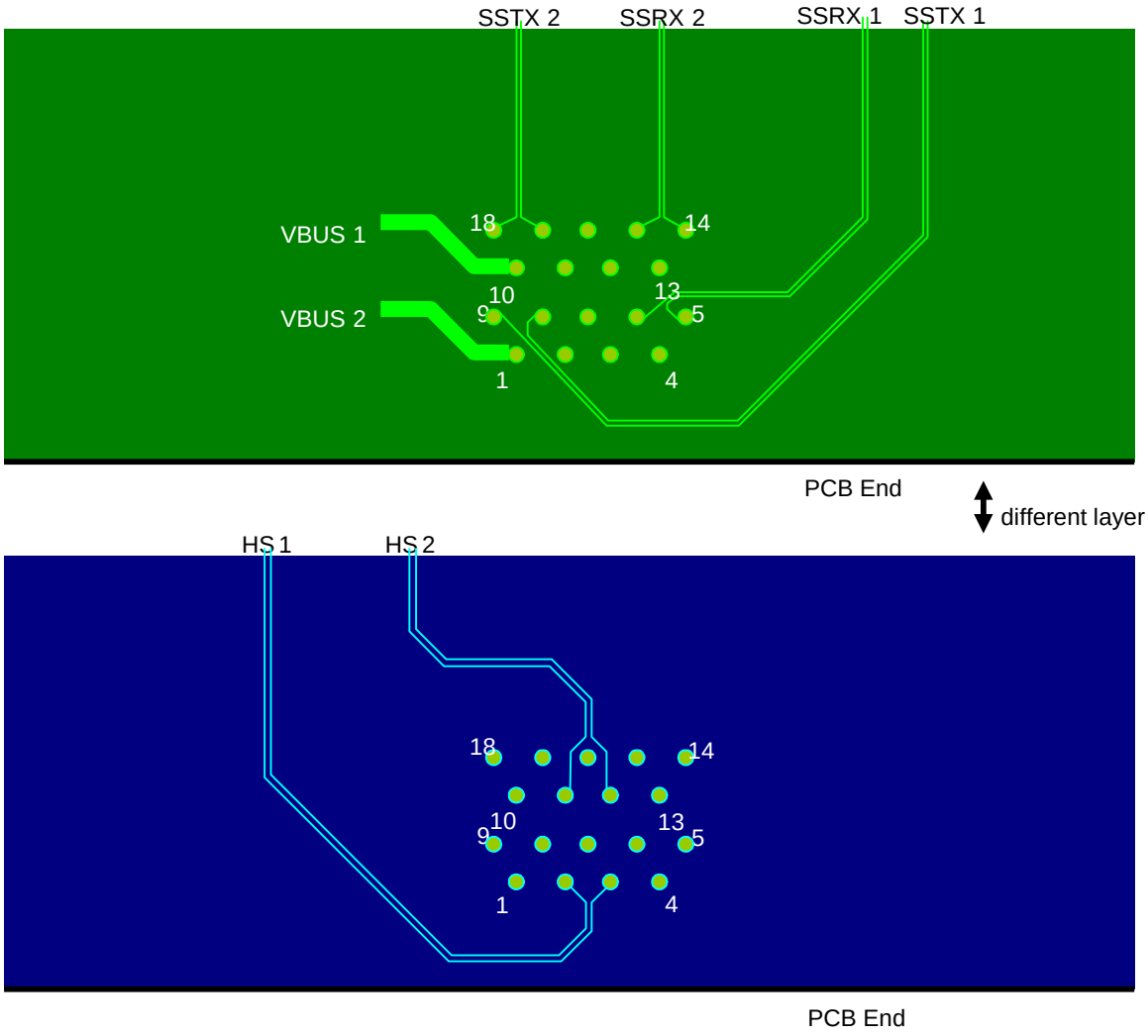


Note: If a double-stacked receptacle is used, consider possible crosstalk caused by the mechanical structure.

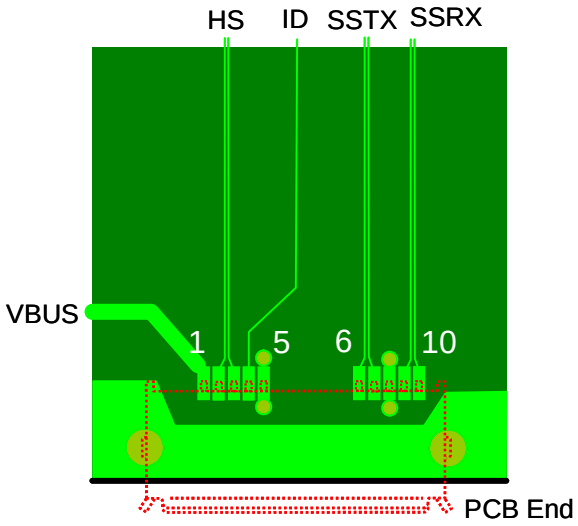
(Standard-B receptacle)



(Standard-A double-stack receptacle)

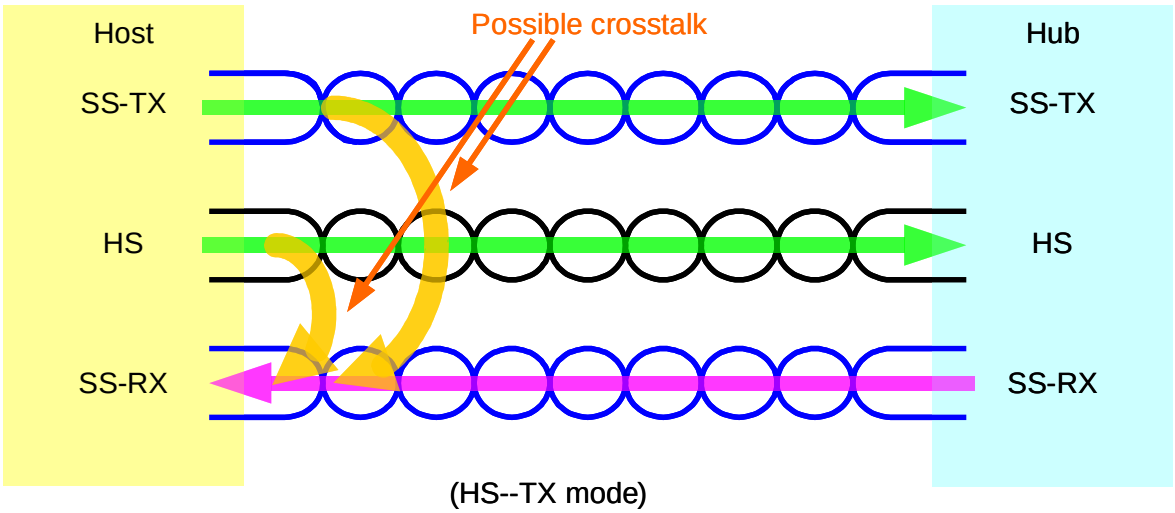


(Micro-B receptacle)

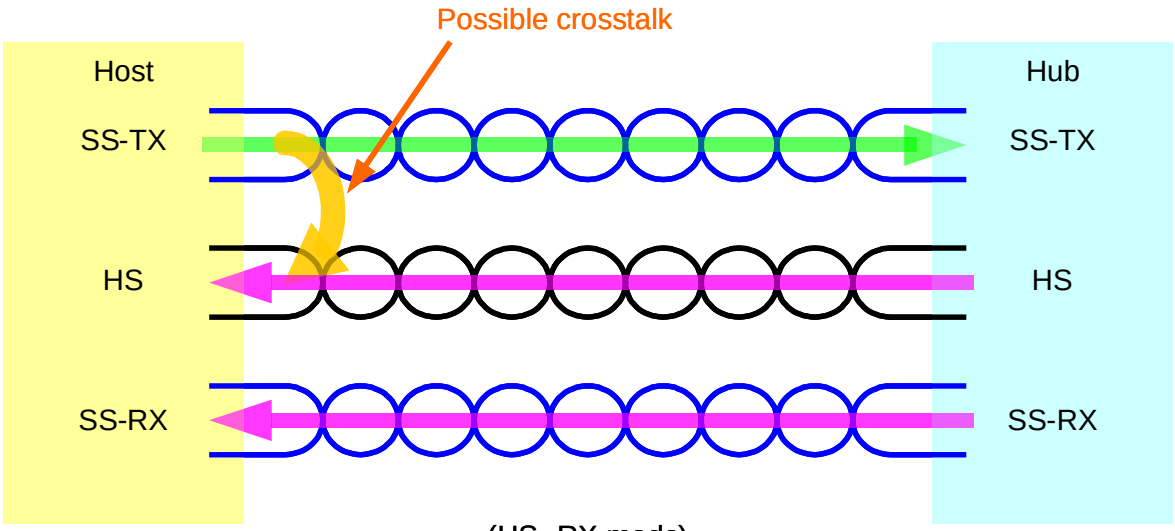


Consideration on crosstalk

As for USB3.0 there are three typical cases in terms of near-end crosstalk: (a) SSTX->HS in RX mode; (b) SSTX->SSRX; (c) HS in TX mode->SSRX. Therefore, please take care SSTX, SSRX, and HS traces aren't closely located each other. It should be taken into account that the moment that all communication modes in the system--SSTX, SSRX, and HS are active exists when connecting to USB3.0 HUB.

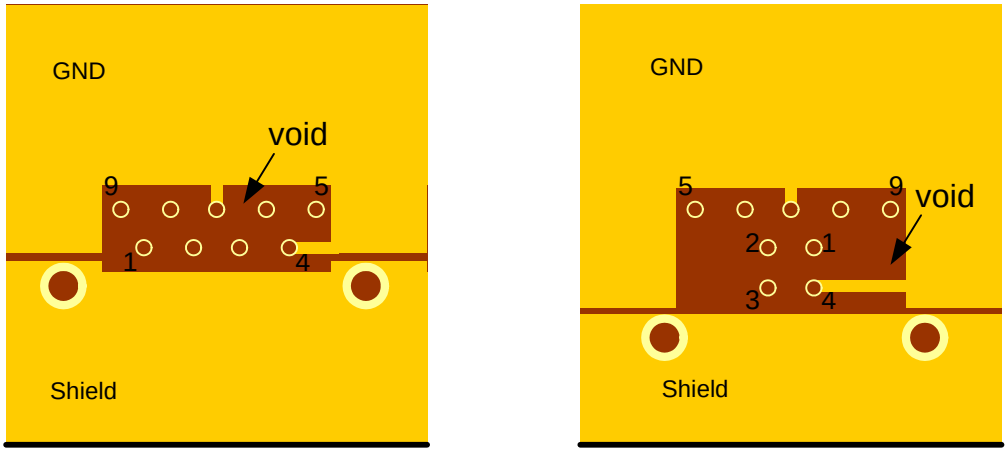


(HS--TX mode)

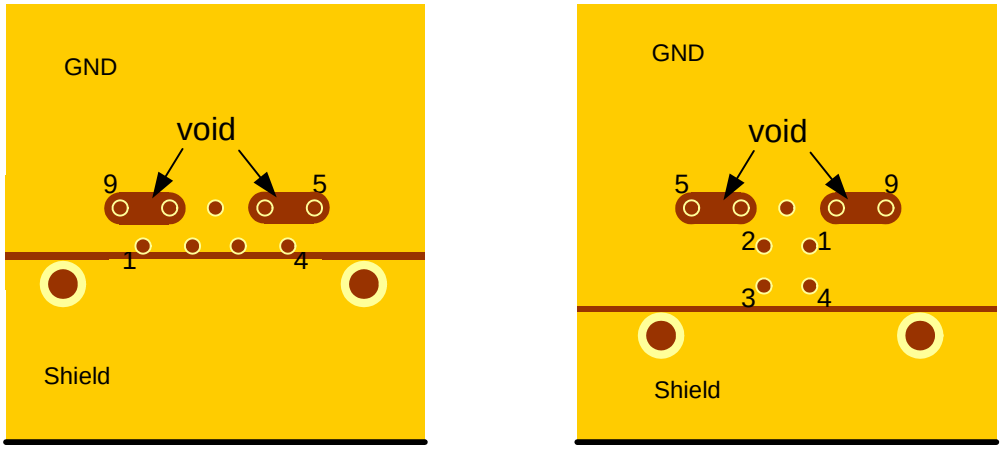


(HS--RX mode)

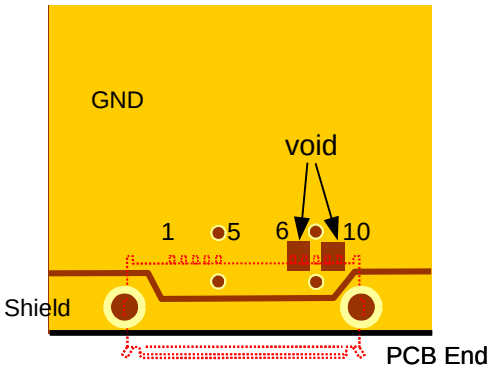
As for the layout around USB 3.0 receptacle where there are one or more large planes like GND in a specific layer, please be sure there is no metal between pins for any differential pair in order to maintain differential impedance of any SS trace. A couple of examples are shown as follows for a reference. Each of them has the two planes that one is the ground and the other is the shielding for the USB3.0 cable which belongs to the same dc level as the ground. Putting any trace between pins for any differential pair may not be allowed as well.



(One case -- void at whole area around pins)

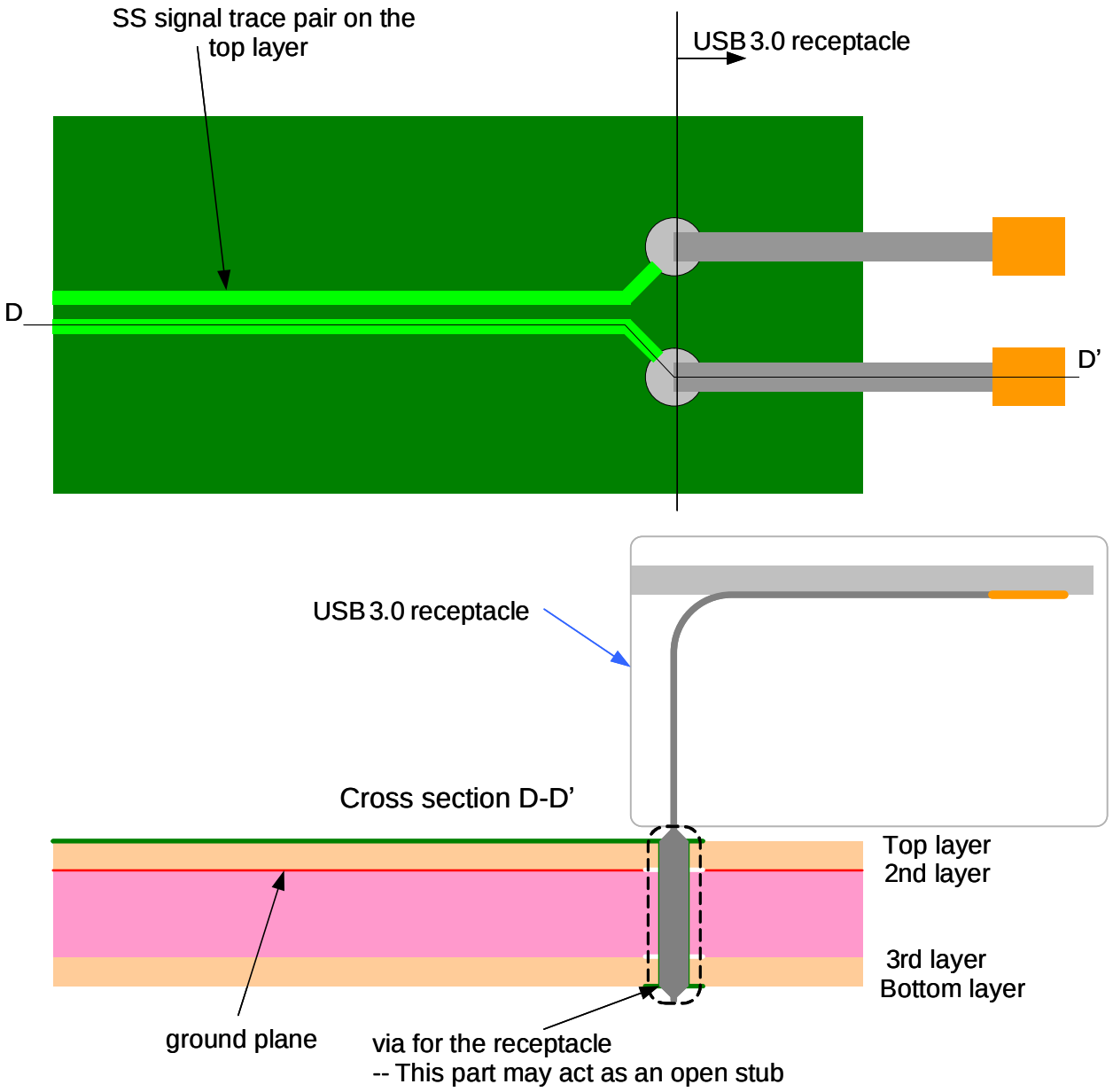


(Another case -- void around SS-related pins)

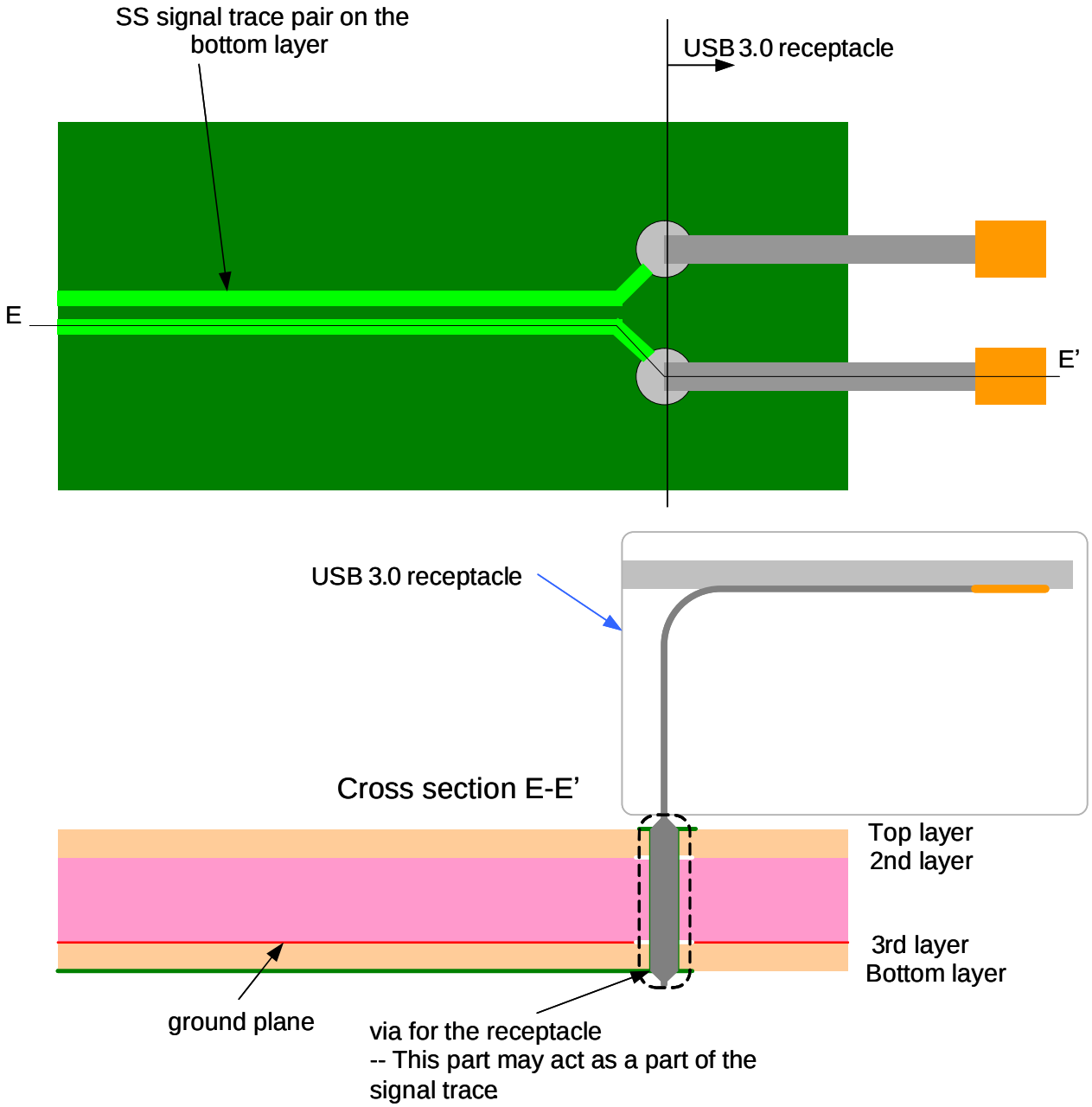


(Micro-B receptacle case -- void around SS-related pins)

SS trace routing example for connecting to USB 3.0 receptacle



(One case -- straightforward)

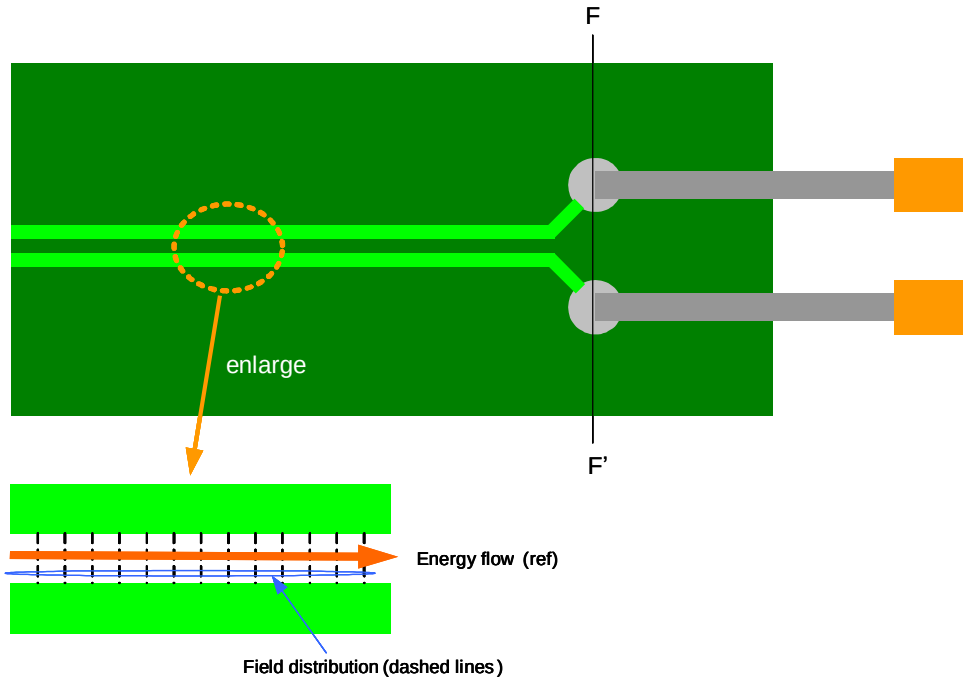


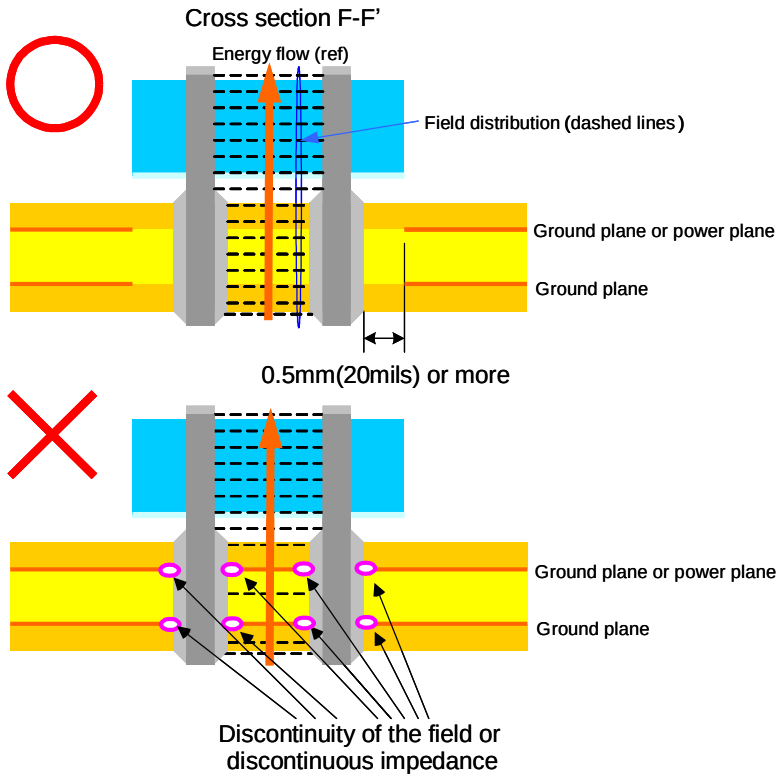
(Another case)

Note: In this case at least one layer change is required if USB3.0 LSI is on the top layer.

(On maintaining differential data transfer mode in realistic electric circuit)

For high speed data transfer system like USB3.0, data signal is transferred along the differential pair by electromagnetic field generated in the pair electrically. The electromagnetic field that varies in time produces power transition which is similar to a radio propagation in a RF cable or an infrared beam in a optical fiber. Since this field goes from/to one of the differential pair, metal object in the pair may cause discontinuous field distribution and affect degradation for transfer performances especially over 3Gbps. It also can be applied that the discontinuous field leads the discontinuous line impedance. It is strongly recommended that there is no metal between the differential pair for any high speed signal such as USB3.0 to maintain the continuity.





3.12. Routing around USB LSI

Consider the same issues as in section 3.11 in the case of signal traces.

As for every power plane or every ground plane, avoid narrow traces that produce unexpected parasitic inductance.

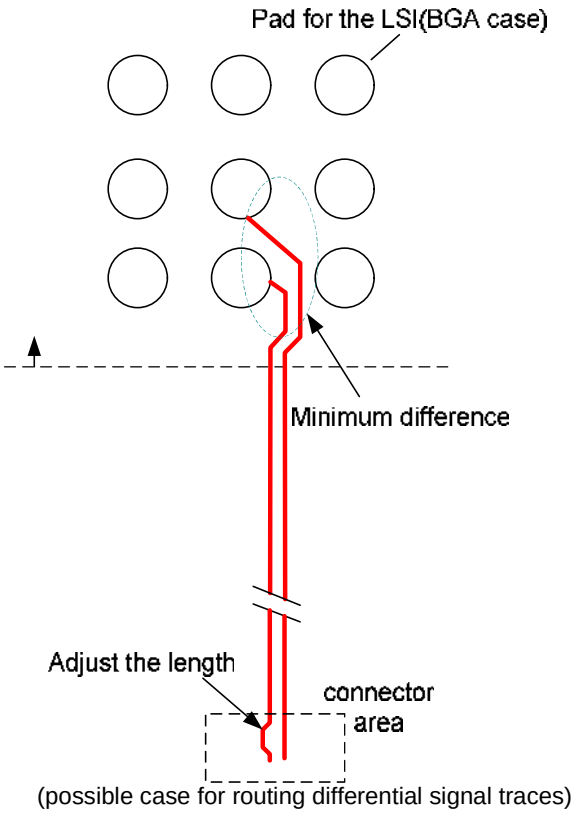
Since a large number of voids may be placed around vias for ground underneath the LSI, assure adequate power flow to each power pin.

In the case of high speed data transfer, a module dividing analog ground and digital ground may cause an unexpected level of bounce potentially causing electrical damage to the LSI. Only one category of ground plane with huge area is recommended. A sufficient number of vias are necessary for stabilizing the ground if it is on multiple layers.

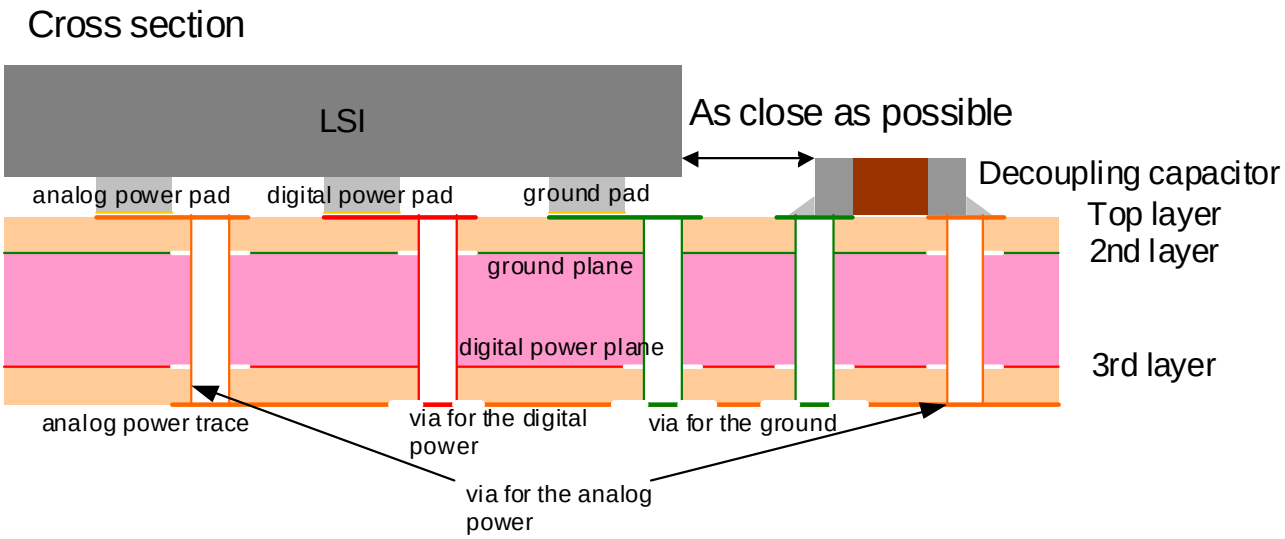
On the other hand, power should be divided according to voltage level, keeping a large area or “island” for each power voltage. It is also necessary to insert a ferrite bead between digital power and analog power, both of which have the same voltage, for a noise filtering.

Routing of analog power should keep it far away from any digital traces including signal traces, to avoid possible malfunctions on the embedded analog circuit.

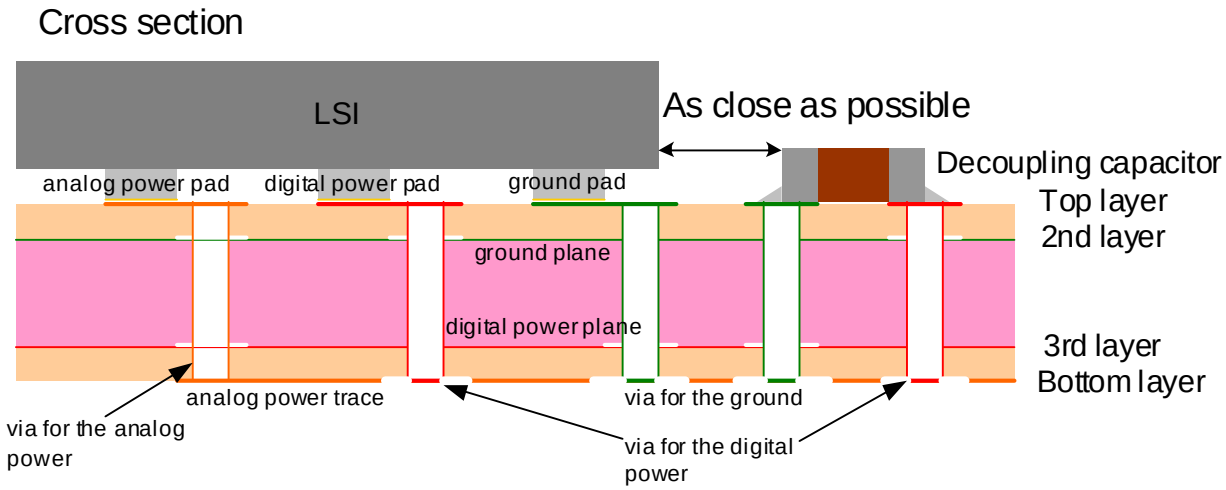
Decoupling capacitors should be put close to the LSI's power area and tightly connected to the ground (this is the very basic for any IC).



(possible case for routing differential signal traces)



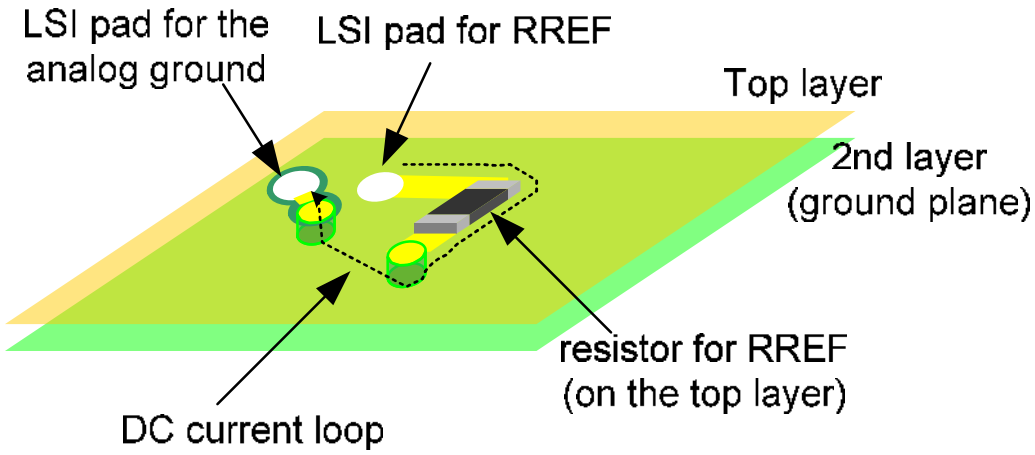
(recommended decoupling capacitor placement for analog power)



(recommended decoupling capacitor placement for digital power)

Example for placing the resistor for RREF

In most of Resas Electronics USB LSI devices, there is a pin named RREF. An external resistor of good accuracy (e.g., 1%) should be connected to RREF, with the opposite side of the resistor connected to ground, in order to realize optimal performance of USB system. Make sure the DC current path routing is kept as short as possible and the circuit is protected from any digital noise. Placing RREF resistor on the same layer as the USB LSI is mounted is strongly recommended.

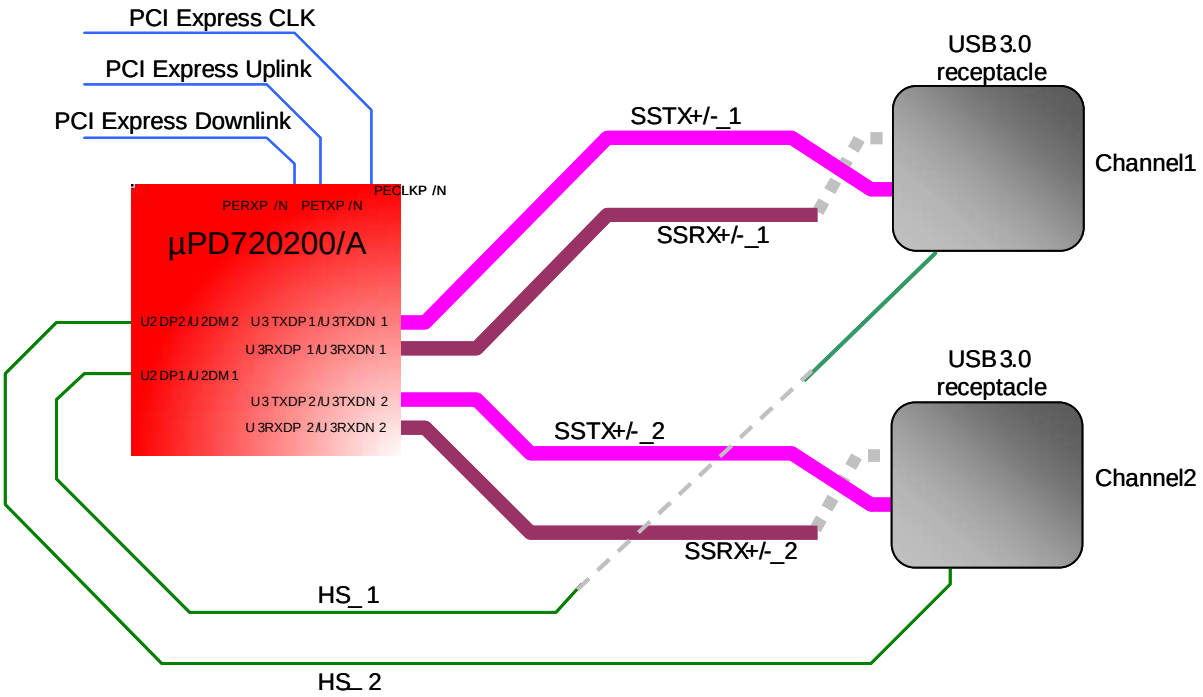


To shorten the DC current loop resistor should be put as close to the LSI as possible.

4. Example for signal routing for µPD720200/A Host controller

µPD720200/A is a USB 3.0 host controller LSI which includes an interface using PCI Express® 2.0. It has three types of major high-speed data transfer protocol. Care should be taken to avoid interference between the three high-speed sections.

One topological example is shown below. Route shorter traces for SS signals first.



For dashed lines tracing on opposite side -- solder side of the PCB for 4 - layer case is better. For more layer it depends on how designer defines of each layer, keeping in mind there is at least one ground plane between the traces

5. References

(1) "Universal Serial Bus 3.0 Specification, Revision 1.0", USB-IF, November, 2008
(2) "USB2.0 Board Layout Guideline", NEC Electronics, May, 2006
(3) "PCI Express® Card Electromechanical Specification Revision 2.0", PCI SIG, April, 2007
(4) “PCI Express® Base Specification Revision 2.0”, PCI SIG, December 20, 2006
(5) "USB3.0 Electrical Test Fixture Topologies", USB-IF
http://www.usb.org/developers/estoreinfo/USB30_ElectricalTestFixture_Topologies.pdf

A. High-speed data transmission line/USB3.0

	Question	Answer
1	What is the important point when the signal pair changes its layer?	Please check if there is a ground plane next to the trace after changing the layer, then there is at least one ground via per the trace near the layer change in order to maintain continuous impedance.
2	How big is the allowable difference between the intra-pair -- one trace to another trace in one pair?	0.13mm (5 mils).
3	Estimated length exceeds 8 inches from the LSI to the associated connector in a board. Is there any better idea to maintain the performance?	Use of the material which has less attenuation than FR4 is one solution, such as polyimide-made flat flexible cable. Please take care maintaining signal impedance and proper dimension for the ground and VBUS in applying the idea like this.
4	What is the important point when the signal pair crosses another trace?	Please pay attention to place the ground plane between the different traces.
5	Is it permitted to use the power plane as a reference plane?	No. Because the power plane doesn't work as the reference of the USB3.0 signal traces even if the power plane has enough AC by-pass capacitors to the ground.
6	Is it necessary to keep symmetry in the differential signal pair even at the decoupling capacitor?	Yes. To avoid any common mode noise please keeps symmetry.
7	What is the important point when the signal pair is on an inner layer?	Please take care that the dimension varies when the signal trace is routed on any inner layer, compared to the case on the surface. Moreover, it is necessary to consider to protect any crosstalk.
8	Why is the restriction of the length to route every high speed signal trace recommended?	In general, PCB made from FR4 isn't suitable with respect to high frequency circuit such as high-speed data transmission lines. For giga-bit data transfer like USB3.0, attenuation by the traces on the FR4-made PCB becomes remarkable and then the system may fail to accomplish desired performance. For these reasons a certain number of the restricted trace length is presented.

B. Power/Ground

	Question	Answer
1	How big is the proper width for the power supply?	It depends on the structure of the PCB. It is needed to keep the allowable I-R drop and the low AC impedance to the ground. The thicker, the better is the basic.
2	Which has the priority, the power or the ground?	The ground. Insufficient grounding affects the system performance.
3	Is it necessary to divide analog ground and digital ground?	No. For the PCB installed in PCs, PC peripherals, CEs, or CE peripherals there are more technical disadvantages than advantages in case of dividing the grounding in high-speed data transfer over 3Gbps.

C. 'RREF'

	Question	Answer
1	What is the important point for the placing of the 'RREF'?	Please take care the entire circuit path including the RREF pin, the AVSS pin of USB LSI, and the external resistor is highly isolated from any power trace or plane as well as any signal trace. And it is also important that the path length is as short as possible. The resistor should be placed on the same layer as USB LSI is on. Surrounding by the ground trace may be effective in order to prevent from the low-frequency noise.

D. Others

	Question	Answer
1	How many layers are the PCB appropriate to have?	Four or more layers are recommended.
2	Is it available to apply another material than FR4 for the PCB?	It depends on customers' decisions.

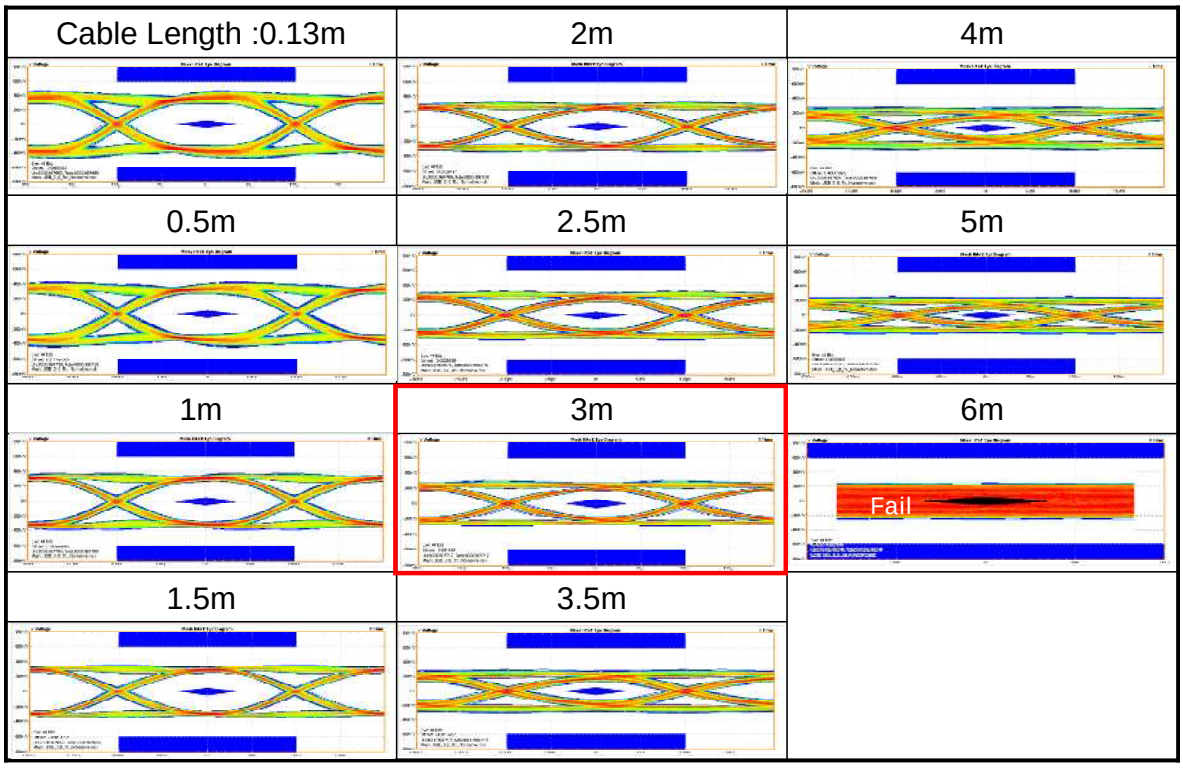
7. USB3.0 Board Layout check list

	Item	Description
☐	1	**The SS trace length is arranged on PCB (FR-4);** **Downstream ports: Length up to 28 cm (11 inches).** **Upstream ports: Length up to 12.7 cm (5 inches).**
☐	2	**AC coupling capacitors are placed symmetrically only in SS Tx line and the capacity of 0.1uF.**
☐	3	**SS trace crossing; At least one layer of ground plane is needed at any crossing of signal traces and any other signal or power line.**
☐	4	**To avoid crosstalk, maintain an appropriate gap between any differential trace. Minimum gap should be greater of >= 0.5mm (20mil) or 4x dielectric height.**
☐	5	**PCB should be FR-4 material and at least four layers.**
☐	6	**2nd layer just beneath the USB3.0 LSI should be GND plane.**
☐	7	**Make the ground wide enough to keep low impedance.**
☐	8	**Make many grand vias and connect ground pad of USB LSI to 2nd layers as many as possible.**
☐	9	**Make the impedance of VDD10 power plane low following a ground.**
☐	10	**All of the decoupling capacitors should be located as close as possible from USB3.0 LSI.**
☐	11	**SS/HS trace line should be route entirely over the ground plane.** **No void, no power plane, or no other signal trace should be allowed in the ground plane under USB-related signal traces.**
☐	12	**SS/HS trace differential impedance should be 90 ohm +/-10%**
☐	13	**If the routing layer for SS signal trace has to be changed, maintain continuous grounding by putting in an appropriate number of vias.**
☐	14	**No stub on any SS signal trace.**
☐	15	**When it becomes necessary to turn 90 degrees, use as few bends as possible.**
☐	16	**Be sure not to put any metal between all SS-pair pins on every layer when using receptacles with pins stabbing the PCB.**

8. **Appendix**

This is the example of SS eye pattern from USB3.0 LSI Tx signal on the appropriate designed PCB (ex. ET-D720200-0011 Add-in card), driving the 0.13m ~ 6m USB3.0 Standard-A to Standard-B cables.
These figures show the enough Eye Height and Eye Width margin of this 3m cable.

SS Eye pattern by USB3.0 Cable (0.13m~6m)



Note: USB Implementers Forum (USB-IF) has defined 3m for the maximum length of the USB3.0 cable.

9. History

Sep. 12. 2012 Release Rev 1.0

- Add upstream SS trace length in section 3.1 and section 7.

Feb. 28 2011 Release Rev.04

- Renewal for Renesas Electronics format.
- The recommended Max SS trace length is extended to 28cm (11inches) in section 3.1
- Add sample figures in section 3.6.
- Add cross section figures in section 3.7.
- Add example figures of Micro-B receptacle in section 3.11
- Add USB3.0 board layout checklist in section 7.
- Add appendix in section 8.

Oct. 15, 2009 Release Rev.03

- Add supplementary notifications in section 3.7
- Add a reference specification in section 5

May. 15, 2009 officially first released, Rev.02