Handbook

Semiconductor Reliability Handbook

Renesas Electronics
www.renesas.com

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Using this Semiconductor Reliability Handbook

- This document shows mainly three topics. Firstly, in Section 1, it shows Renesas' efforts at achieving reliability in its semiconductor products. Secondly, in Sections 2, 3, and 4, it shows fundamental information relating to reliability that supplements the reliability documentation Renesas provides for its semiconductor products. Finally, in Section 5, it presents some common precaution or instruction for using semiconductor products that our customers should understand and follow.

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1. Quality Assurance for Semiconductor Devices

1.1 Basic Policy for Quality

In accordance with the quality policy stated in Figure 1.1, Renesas Electronics has established a quality assurance system based on the ISO 9001 and ISO/TS 16949 standards. Renesas is developing consistent quality assurance and quality control across all stages from product planning to after-sales services, based on “built-in quality” that is backed up with reliability technologies.

Renesas has always placed great emphasis on maintaining and improving levels of quality and reliability. From the development to the delivery of a products, Renesas implements quality control and reliability verification from the three standpoints of “quality control and reliability verification in design”, “quality control in production”, and “quality assurance of product”. All Renesas parties uphold the basic principle that quality comes first. To this end, they are concerned the achievement of quality levels that satisfy customer expectations.

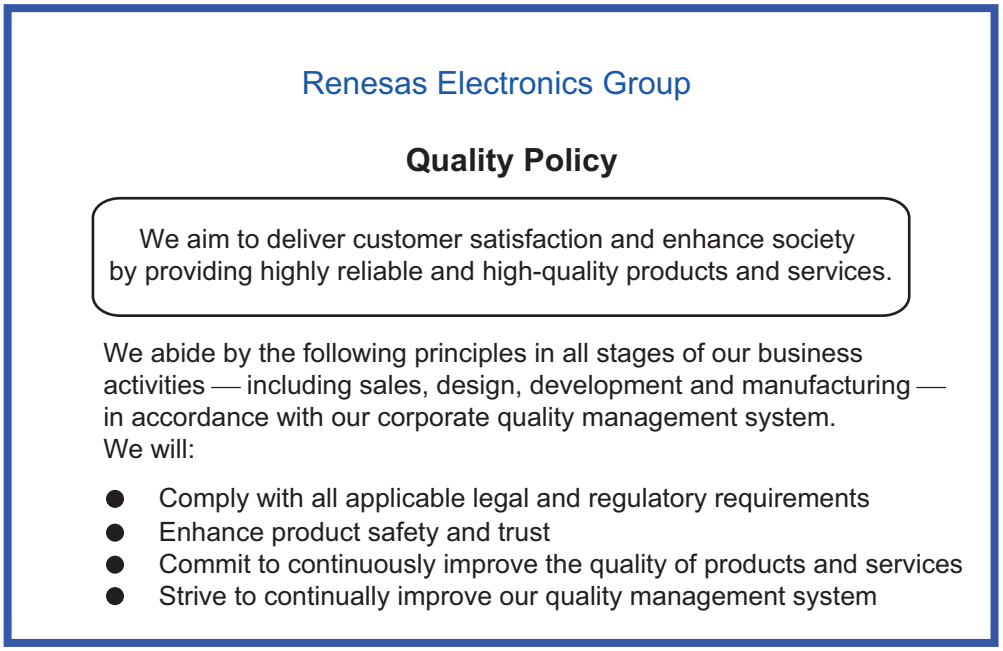

Figure 1.1 Renesas Electronics Quality Policy

1.2 Quality Assurance System for Semiconductor Devices

Figure 1.2 outlines our quality assurance system which covers all stages from product development to field use.

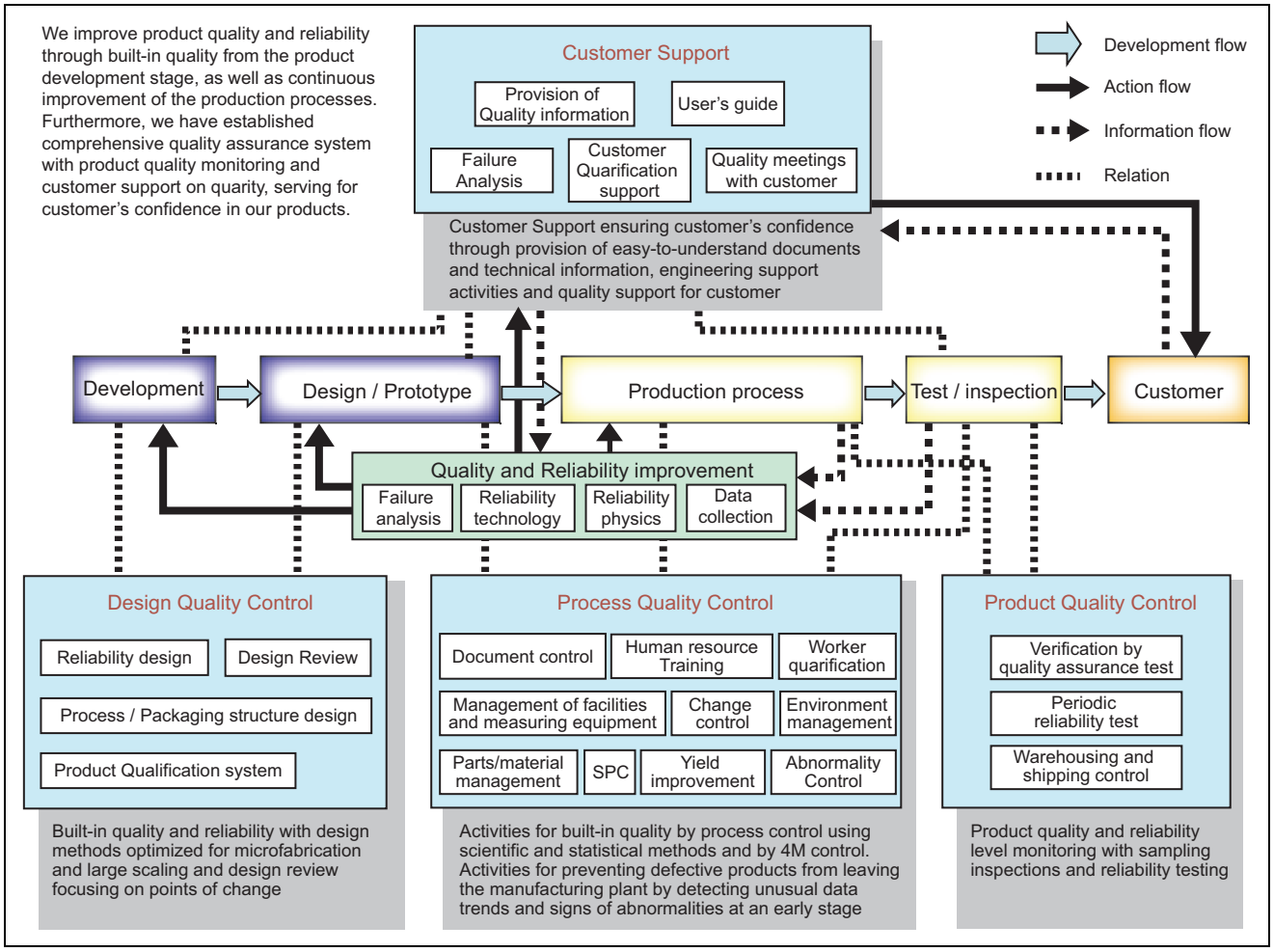

Figure 1.2 Renesas Quality Assurance System for Semiconductor Devices

Quality control in the design stage is the activity of built-in quality and reliability during design, and it concentrates on design review and the optimization of device structure, applicable materials, circuit design, packages, production process and so on. After verifying the electrical characteristics and reliability of prototypes for each product type, it moves to mass-production stage.

Quality control in mass-production stage is the activity of built-in quality during production process. This quality control is for equipment, tools, D.I. water, gasses and production conditions, and quality control of product performance. Using the EDP (Electronic Data Processing) system to control these quality control information, it is established the total quality control system.

Quality control in the finished product stage has two activities. The first activity is to check the completed products meet prescribed functionality and reliability target. These checks include the inspection of each device lot, or periodic in-house inspections and examinations. The second activity is to involve the customer support such as quality information service.

In this way, the quality information is fed backwards and forwards between all stages from the development and design to mass-production, shipping, and actual product operation. This system enable the implementation of more efficient product quality.

Figure 1.3 shows a flowchart of the quality assurance program.

Our quality control system has been built based on the ISO 9001 and ISO/TS 16949 standards.

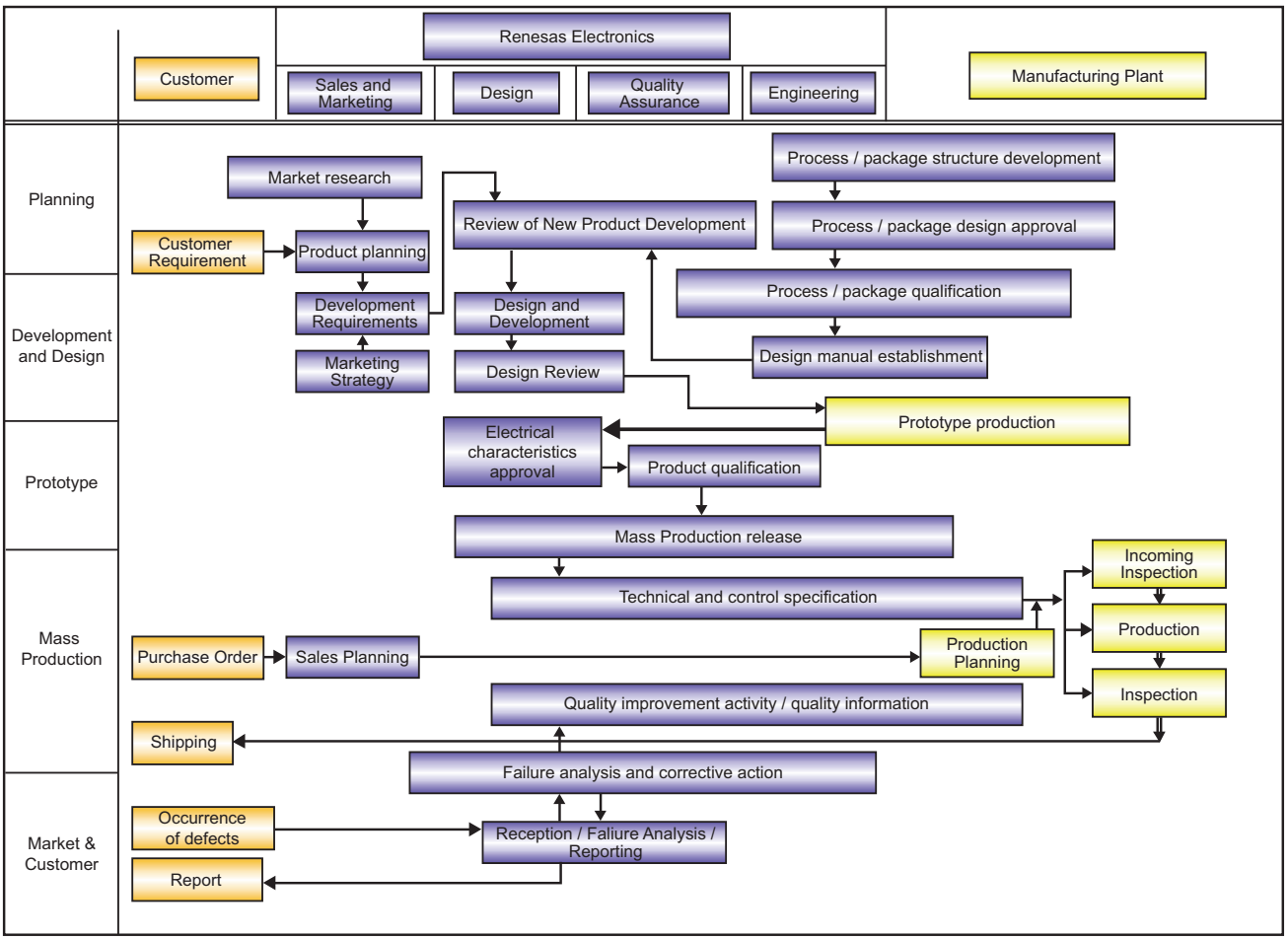

Figure 1.3 Quality Assurance Program Flowchart

Not only have Renesas products been manufactured with high reliability and then improved for higher reliability by the quality assurance system illustrated in Figure 1.3, but they also have been specified from the product development stage for an appropriate degree of reliability based on the classification in Table 1.1.

Table 1.1 Quality Grades for Renesas Semiconductor Devices

Quality Grades	Representative Examples of Use Application
High Quality	Transportation equipment (automobiles, trains, ships, etc.), traffic control (signals) , large-scale communication equipment, key financial terminal systems, safety control equipment, etc.
Standard	Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment, industrial robots, etc.

1.3 Quality Assurance at Development Stage

The following procedure is used in product development to ensure the target quality and reliability. Using demand estimates for new products based on market research, we study to plan product development by investigating, at the product planning stage, first the required quality grade, functionality, and reliability of the new product, then issues related to product manufacture, and then issues related to cost. Based on the development plan, new theories, technologies, and concepts are actively adopted for design and technology development during the development of the new product.

The design is reviewed and then prototype is fabricated. Then the prototype undergoes a qualification test that checks whether their electrical characteristics, maximum ratings, and reliability meet the quality target.

Also at this stage, we provide the drawings and specifications required for mass production and at the same time as implementing education and training for the workers, we create a system for procuring the required materials and parts and provide the equipment and jigs required for manufacturing.

When the prototype has passed characteristics evaluation and reliability testing, we study issues related to design, manufacture, and quality, and once we have verified that there are no problems, we move on to the next step, the mass production stage.

These processes are set up for the various development levels and, to assure the desired quality and reliability, we implement quality approval at the device prototype period based on reliability design.

Product Quality Certification at Renesas is based on the following approach.

1. Use an objective viewpoint of the customers' stand point.
2. Incorporate examples of past failures and field use information.
3. Certify design modifications and operation alterations.
4. Certify parts, materials, and processes using stringent criteria.
5. Investigate the process capability and causes of deviation and verify the control items and points during mass-production.

The process of certification is divided into three steps:

a. Certification of Parts and Materials
b. Electrical Characteristics Approval
c. Product Quality Certification

Design verification for parts and materials is performed during the Certification of Parts and Materials. Product design verification is covered in Electrical Characteristics Approval. Design validation is checked through the Product Quality Certification.

Renesas implements early warning system to verify the quality of the product at the initial stages of mass production. In early warning system, we set up a special management system for a fixed period after mass production starts, and under that system, we collect increased amounts of quality control information, quickly implement corrective measures for any problems found, and verify the results.

1.4 Quality Assurance at Mass Production Stage

At the mass production stage, the device is put into production based on the production plan. The materials, parts, production processes, environments and equipment conditions, and products in plant are carefully controlled. In addition, in-process inspections and final inspection are carried out on both semi-manufactured and manufactured products to check quality levels.

Built-in-quality at this stage is very important for manufacturing to keep high quality and reliable products. To do this, the Manufacturing Department establishes production specifications and determines the items to be controlled for the main manufacturing conditions. Production is performed based on these production specifications, and, for manufacturing conditions that have a large effect on quality, quality is maintained and improved by implementing checklist based inspections and characteristics management.

Periodical maintenance and accuracy adjustments are regularly performed for early detection of abnormalities and for establishing/monitoring preventive maintenance schedules.

In the production process, Statistical Process Control, SPC, with continuous data and workmanship control are performed as in-process control.

To build in quality, SPC techniques are used at each stage. In particular, in the mass production stage, control chart is applied to critical work steps to monitor whether process variations are within acceptable ranges. Here, we have everyone involved with the manufacturing itself strive to minimize these process variations as much as possible by monitoring and managing various process parameters, such as the process capability index, Cp and Cpk, and the process performance index, Pp and Ppk.

The process capability index is used to obtain stability with respect to the process specifications from process data acquired over a fixed period and the values in the process control specification and are defined by the formulas shown below. We determine these process capability index and the process performance index periodically and use them to improve any dispersion in the process.

$$Cp = \frac{(Upper\ specification\ limit - Lower\ specification\ limit)}{6\,\sigma}$$

$$Cpk = \frac{|Specification\ limit\ close\ to\ the\ average|}{3\,\sigma}$$

At the final inspection, all products undergo electrical characteristic testing. Screening is also performed to detect and reject defective products that do not meet the quality specifications that were determined in advance. The data collected here is used to improve product quality.

Quality related information that is seen as necessary from the purchasing of materials and parts, through manufacturing and inspection, shipment, to actual use by the customer is collected in a quality management system and analyzed using statistical quality control methods. The results are provided to Manufacturing Department and all other related departments as feedback and used both to maintain and improve quality and to improve yields. If a problem is found in either the manufacturing process or the product, the department where the problem was found issues a process non-conforming report and the relevant departments investigate the cause of failure and take corrective actions. Figure 1.4 shows the relationships between process abnormalities and their corrective actions.

When the design, materials and parts, production methods, equipment, and such can be changed, prototype is made to check for quality levels and evaluate the reliability. If no problem is detected, the change will be implemented after the customer gives their approval.

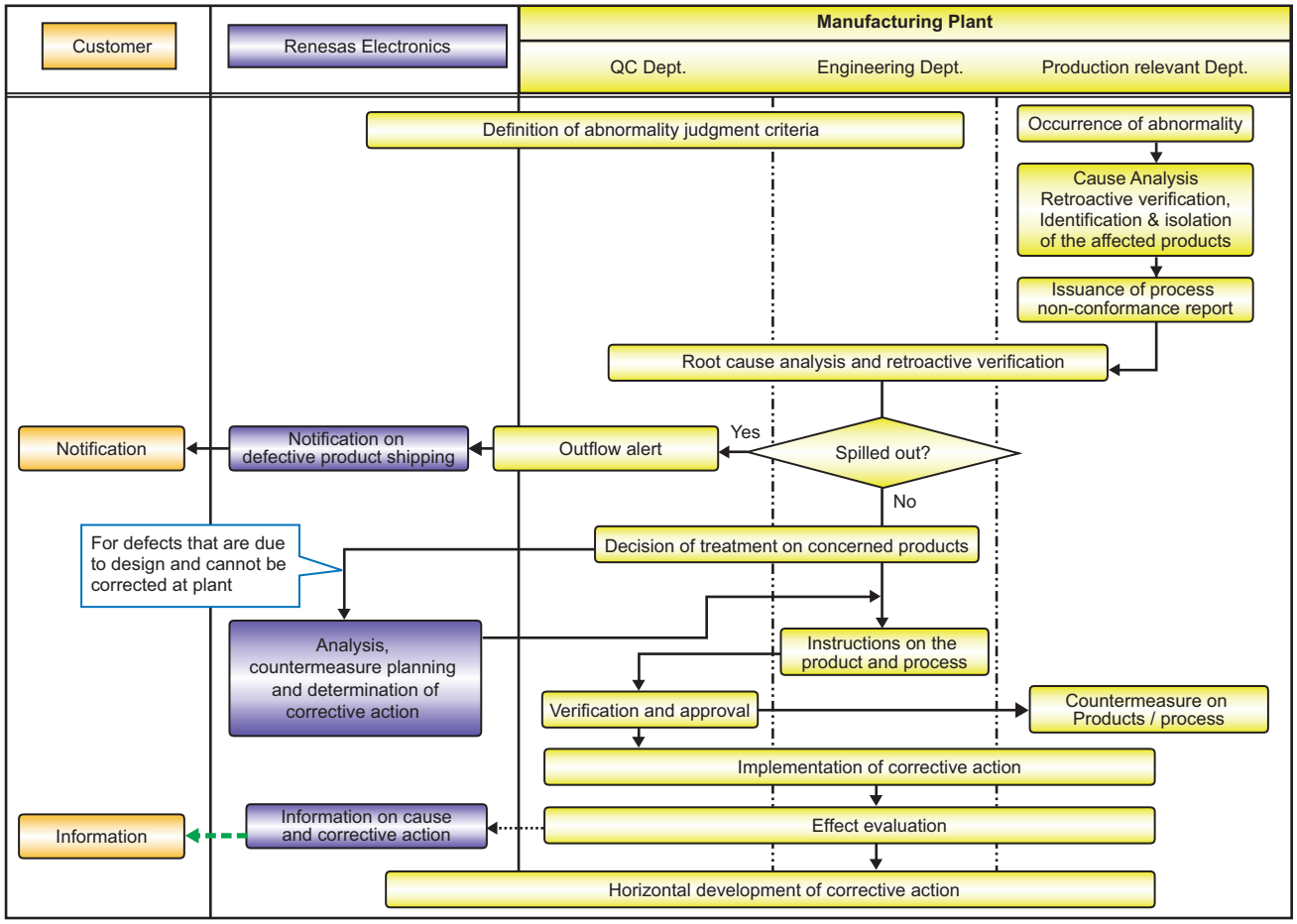

Figure 1.4 Flowchart of Corrective Action

1.5 Change Control

We have attempted stabilization of manufacturing process to optimize our equipment and processes by adjusting to external factors. To minimize the risks from changes we have set up and are operating the change management system shown in Figure 1.5. This system manages not only changes involving manufacturing equipment, manufacturing conditions, and manufacturing plants, but also changes at the detail items. For changes that affect product quality or characteristics, we have adopted a system that applies those changes to mass production only after informing our customers.

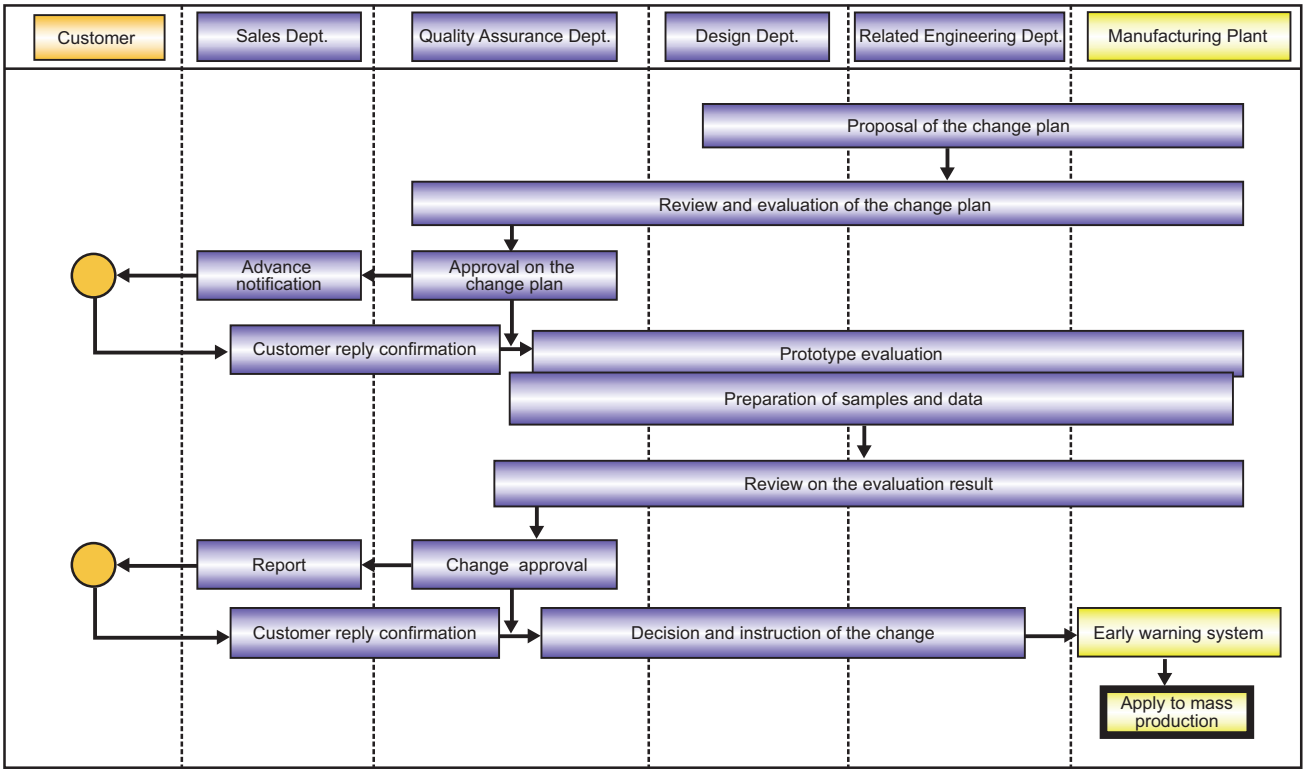

Figure 1.5 Change Control System

1.6 Failure After Shipping and Corrective Actions

When a failure is found at the acceptance inspection, assembly, or field operation stage in the customer, the Quality Assurance Department plays the major role in identifying the cause of failure and implementing corrective actions. Based on the analysis request issued by the Sales Department, the Quality Assurance Department investigates the failure and analyzes it using various testing equipment, and analysis tools and methods.

Based on the analysis result, Design and Engineering, Manufacturing, and other related departments hold a meeting. Then corrective action is taken as required, and a report is issued to the customer. Figure 1.6 shows the flowchart of returned product control.

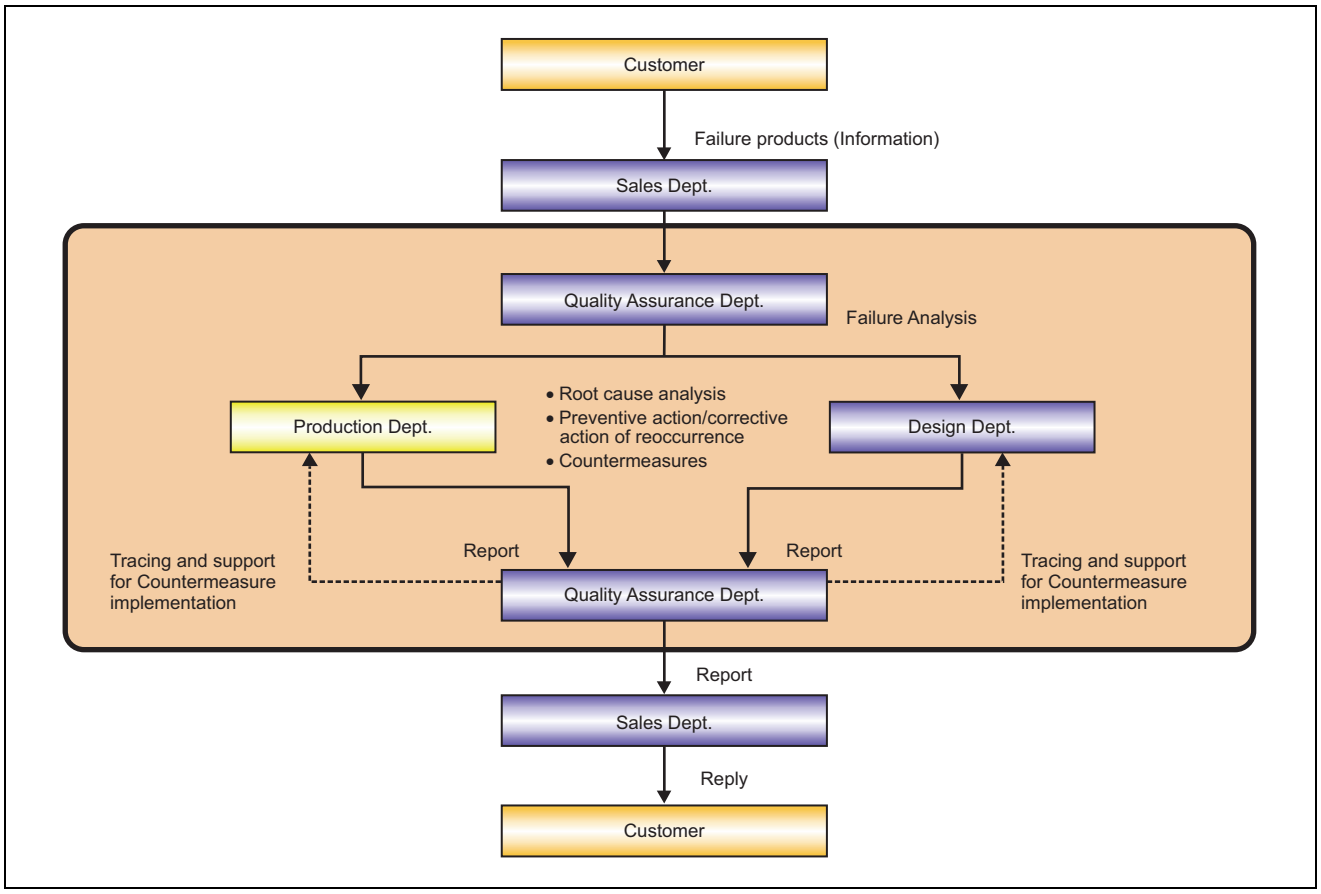

Figure 1.6 Flowchart of Customer Complaint Management

2. Reliability

2.1 Concept of Semiconductor Device Reliability

The reliability of semiconductor devices is represented by the failure rate curve (called the “bathtub curve”), which is illustrated in Figure 2.1. The curve can be divided into the three following regions: (1) early failures, which occur within a relatively short time after a device starts to be used, (2) random failures, which occur over a long period of time, and (3) wear-out failures, which increase as the device nears the end of its life.

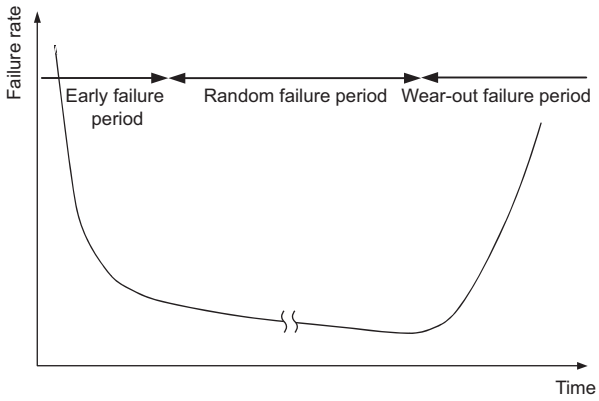

Figure 2.1 Failure Rate Curve (Bathtub Curve)

Early failure is defined as a failure that occurs at an early stage after operation of semiconductor devices is initiated. In addition, the early failure rate tends to decrease with the passage of time. Latent failures that were not removed in the screening process are included in early failures and become manifest within a short time under stresses such as temperature and voltage after operation starts. In the case of semiconductor devices, most early failures are due to defects that form during the production process (for example, microdust adhering to wafers) and defective materials.

“Random failures” occur once devices having latent defects have already failed and been removed. In this period, the remaining high-quality devices operate stably. The failures that occur during this period can usually be attributed to randomly occurring excessive stress, such as power surges, and software errors. This group also includes devices susceptible to remains of early failures.

“Wear-out failures” occur due to the inherent lifetime of the device due to wear and fatigue. When a device enters the wear-out period, the failure rate tends to increase rapidly. This is influenced by the usage conditions.

Accordingly, for the production of highly reliable semiconductor devices, it is important to reduce the early failure rate and to ensure the long life, or durability against wear-out failures.

To reduce the early failure rate and thereby improve reliability, Renesas has implemented both product quality assurance based on improving quality control procedures and quality improvement activities as well as a variety of screening procedures, including electrical characteristics testing and burn-in tests. Furthermore, to provide the necessary product durability for the service life of products, the company has been building in reliability starting with the design and development stages. In addition, it carries out design review and other activities to ensure reliability, and also conducts reliability testing.

2.2 Dependencies of Failure Rate Function (Bathtub Curve)

As shown in Figure 2.2, the ideas discussed in the previous subsection can be illustrated if they are expressed in terms of the changes that occur with device failures. In Figure 2.2, individual semiconductors are represented as sets (circles). At the start of device operation, there may be semiconductors with latent defects included in the set. These will fail under operating stress and are removed from the set. The early failure period can therefore be defined as the period during which devices having latent defects fail. The failure rate can be defined as a decreasing function, since the number of devices having latent defects decreases as they are removed.

In the next several years, devices with latent defects are removed and the reliability goes up. Although there are no more failures resulting from latent defects in this period, semiconductors can still fail due to some excessive external stress. This period is considered as the period of random failures, and the failure rate accordingly becomes random (the failure rate is nearly constant).

Finally, the basic device structure wears out due to stress over its long period of use, and failures due to the inherent lifetime of the semiconductor device itself begin to occur. The failure rate at that time can be expressed as a function that increases with time.

As this discussion should make clear, early failures and wear-out failures have different causes, even though they appear to be the same. A means of illustrating the causes of failure is the bathtub curve, shown in Figure 2.3.

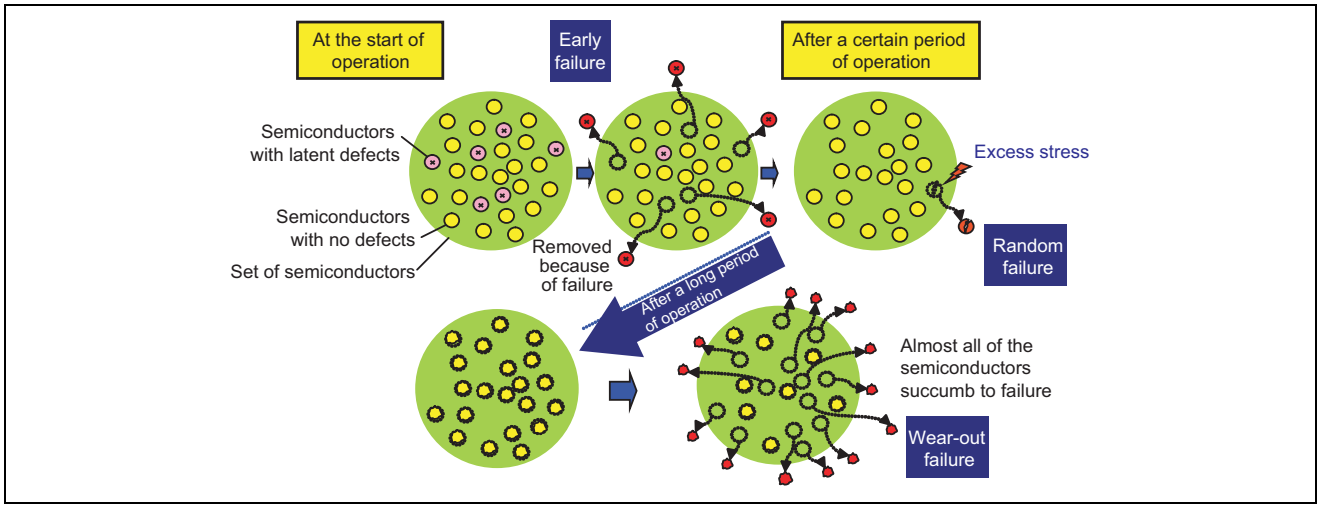

Figure 2.2 Image Showing Changes in the Semiconductor Failure Rate Results in a Bathtub Curve

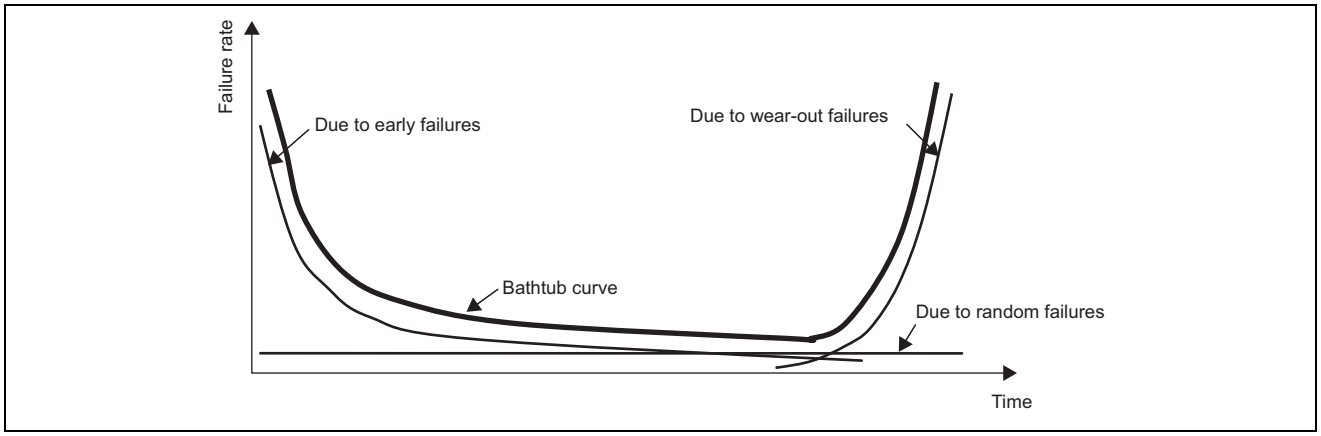

Figure 2.3 Factors Creating the Bathtub Curve

2.2.1 Early Failures

In the production process, semiconductor devices may contain defects due to the presence of tiny particles, as well as variations in manufacturing equipment and variations in dimensions. This fact is known as the initial defect density. Products with the desired characteristics and reliability in the classification and inspection processes are classified and obtained within the range of variations and distinguished between good and bad ones. The rate of good products obtained is called as the yield. Products with a higher yield have a lower defect density, while products with a lower yield have a higher defect density. Generally, the period of early failures is defined as the first year of a product life cycle. To reduce the failure rate in this period, semiconductor manufacturers are attempting to improve quality by introducing a screening process that can include stress, burn-in, and other types of tests. Since the failure rate in the early failure period decreases with time, once the products with defects are screened out, only the products with low probability of failure are left (See Figure 2.2), which allows manufactures to bring high-quality products to the market. However, because the screening process itself entails a trade-off between quality and cost, it is desirable to set screening conditions by considering the usage of products and the quality requirements. Screening is nevertheless an after-the-fact measure for products that have already been manufactured. If you take such measures as reducing the defect rate initially incorporated in the production stage and designing a layout that helps to prevent defects, you can achieve stable quality from a reduction of early defects as well as obtaining a higher yield (more efficient production). Note that, in the early failure period, the Weibull distribution has a shape parameter (m) smaller than 1.

2.2.2 Random Failures

Failures resulting from production defects will attenuate with time. Even though early failures are screened out, products having minor defects will still remain. Strictly speaking, therefore, the region of random failures can be considered to be a continuation of the early failure region, which is a type of region in which the failure rate is falling.

The mode in which the failure rate is constant (exponential function) in the true sense covers soft errors, electrical noise, electrostatic discharge, and other problems. All of these problems will occur at random under the stress of external factors. Accordingly, the magnitude of durability can be determined from the specifications used in the design stage. Note that, in the random failure period, the Weibull distribution has a shape parameter (m) approximately equal to 1. The failure rate function therefore approximates an exponential distribution.

2.2.3 Wear-out Failures

Semiconductors fail when they reach the limits of their basic durability. This period is called the region of wear-out failures, and indicates the life of different failure modes of semiconductors, such as HC, EM, and TDDB. Wear-out failures differ with differences in the stresses applied to the device while it is being used. During the wear-out period, the Weibull distribution shape parameter m is greater than 1.

2.3 Screening

Generally, semiconductor devices have a high early failure rate immediately after they are manufactured. Thereafter, the failure rate begins to decrease. Renesas sets reliability targets (early failure rate (ppm/year or FIT)) based on the customer's quality needs and intended use of the product. Devices whose failure rate exceeds the set values undergo screening so that the target values can be achieved.

Screening is implemented to exclude devices in which early failures would occur. There are two screening methods. In the first, an appropriate stress, which will not degrade or damage non-defective devices other than those with latent defects, is applied intentionally to the products and after those latent defects are exposed, excludes defective products with appropriate tests. In the second, products that have defects are selected and excluded without applying stresses in the manufacturing process.

When applying screening, it is necessary both to investigate fully the applications, required quality grade, design, structure, and fabrication methods of the product being screened and also to consider carefully how not to adversely influence non-defective products.

Table 2.1 lists a variety of typical screening methods.

Table 2.1 Typical Screening Methods

Type	Screening method	Faults to be excluded
Non-stress methods	Pre-packaging visual inspection	Die surface defects, missing bonding wires
	Post-packaging visual inspection	Chips in or damage to the package surface
	X-ray transmission inspection	Deformed bonding wires, defects in the bonding eutectic alloy
Thermal stress methods	Temperature cycling	Defects in the die bonding or package, insufficient hermetic sealing
	Thermal shock	As above
	Low-temperature testing	Influence of hot carriers, changes in the electrical characteristics
Mechanical stress methods	Drop testing	Defects in the bonding, bonding wires, or package
	Constant acceleration testing	As above
	PIND	Foreign matter in the package cavity
Electrical stress methods	Burn in	Die internal defects such as a minutes foreign particles and defects, and contaminations in thin films.
	High-voltage application	Insufficient withstand voltage in insulating films or circuits

2.4 Characteristics of Semiconductor Reliability

Reliability of semiconductor devices can be summarized as follows:

1. Semiconductor devices (Figure 2.4) have a configuration, which is fundamentally very sensitive to impurities and particles, and the stability status of the surface state is extremely important. Consequently, to manufacture these devices it is necessary to manage many processes while completely controlling the level of impurities and particles. Furthermore, the quality of the finished product depends upon the complex relationship of each interacting substance in the semiconductor, including chip material, metallization and package.
2. The problems of thin films and micro-processes must be fully understood as they apply to metallization and bonding. It is also necessary to analyze surface phenomena from the aspect of thin films.
3. Due to the rapid advances in technology, many new products are developed using new processes and materials, and there is a high demand for product development in a short time period. Consequently, it is sometimes not possible to refer to the reliability achievements of existing devices.
4. Semiconductor products are manufactured in high volume. In addition, repair of finished semiconductor products is impractical. Therefore incorporation of reliability at the design stage and reduction of variation in the production stage have become essential.
5. Reliability of semiconductor devices may depend on assembly, use, and environmental conditions. Stress factors effecting device reliability include voltage, current density, temperature, humidity, gas, dust, contamination, mechanical stress, vibration, shock, radiation, and intensity of electrical and magnetic fields.

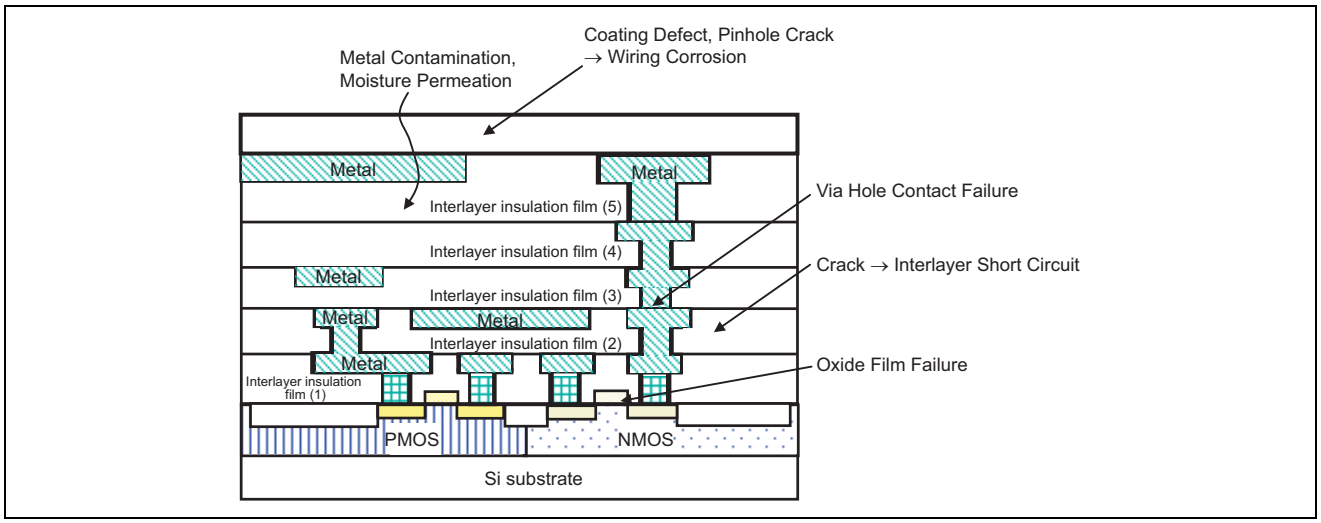

Figure 2.4 Semiconductor Device Cross-Section

In recent years high-level functions, systemization, and large scale integration have advanced rapidly, therefore ensuring reliability has become extremely important. Reliability is usually expressed as the “Failure Rate.”

Generally, the failure rate of electronic parts and devices, including semiconductor devices, follow the ‘bathtub’ curve as shown in Figure 2.1. The manner in which failures occur can be divided into three periods, i. e. — an early failure period, a random failure period and a wearout failure period.

Failures during the “early failure period” most commonly result from deficiencies in production. During this period the failure rate falls with time and finally becomes stable. The “random failure period” is the useful lifetime of semiconductor devices and the failure rate in this period is generally constant. The “wear-out failure period” (aging period) is a period of concentrated incidence of failures of specific defects that result into the end of the component life. The semiconductor component will not exhibit wear-out failures in its predefined lifetime if environmental stresses in the field use do not exceed those of the intended application profile, therefore early failure period and random failure period are more related to the reliability and maintainability.

Almost all semiconductor devices with latent defects, which may fail in the early failure period, can be screened out by using a testing method such as a burn-in test.

2.5 Reliability Criteria

Reliability is defined by JIS Z 8115 “Glossary of Terms Used in Reliability” as;

“The features of an item which enables it to fulfill its required functions for the specific period under the given conditions.” In this definition, reliability includes the concept of time. Therefore, reliability has to be differentiated from initial product quality which does not include the time parameter. But in practice reliability is often expressed as the fraction defective irrespective of time parameter during this “early failure period.”

2.5.1 Early Failure Period Criteria

In the early failure period, rate of a number of defects or failures against the total number of samples, irrespective of the time parameter, is generally expressed in (%) or ppm. Where ppm is the abbreviation for “parts per million,” 1 ppm means 1 defective component out of 1,000,000 semiconductor devices. Therefore, if the fraction defective is 100 ppm then there are 100 defective components out of 1,000,000 or 1 component out of 10,000.

2.5.2 Random Failure Period Criteria

In the random failure period it is necessary to consider the time parameter. The following criteria are used:

- Reliability Function
- Unreliability Function
- Probability Density Function
- Conditional Failure Rate Function (Failure Rate Function)

These criteria have constant relation each other. In particular the unit of FIT (Failure in Time) is widely used.

(1) Reliability Function and Unreliability Function

The Reliability Function is the proportion of components (devices, parts and elements) which keep to perform their designed functions normally after time (t). This can be expressed by the equation:

$$R(t) = (n - c(t))/n \qquad (2\text{-}1)$$

where $R(t)$ = *Reliability Function*

n = *The total number of tested components*

$c(t)$ = *The total number of failures to develop up to time (t)*

On the other hand, the complement of the Reliability Function is the Unreliability Function.

The Unreliability Function, also known as the Cumulative Failure Distribution Function, is defined as the Distribution Function when the failure time is considered as the Probability Function. That is the total number of failures (the cumulative number of failures) which lose their designed functions after any particular device, part, or component is being used for a period of time expressed as “t”.

This can be expressed by the equation:

$$F(t) = c(t)/n \qquad (2\text{-}2)$$

where $F(t)$ = *Unreliability Function*

n = *The total number of tested components*

$c(t)$ = *The number of failures to develop up to time (t)*

In addition, the following relation is true:

$$R(t) + F(t) = 1 \qquad (2\text{-}3)$$

Further, as shown in Figure 2.5, the Reliability Function $R(t)$ is a monotonically decreasing function and the Unreliability Function $F(t)$ is a monotonically increasing function.

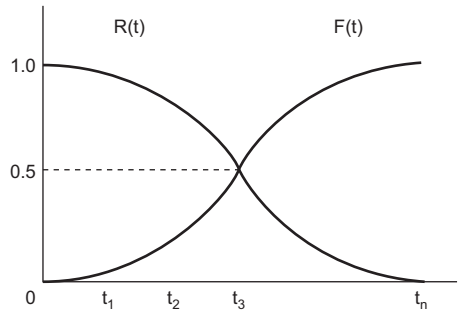

Figure 2.5 Relation of *R*(*t*) and *F*(*t*)

(2) Probability Density Function

The Probability Density Function (of failures) is defined as the probability of failure of any particular device or component after being used for a period of time (t). From this definition Probability Density Function can be expressed by the equation:

$$f(t) = dF(t)/dt = -dR(t)/dt \qquad (2\text{-}4)$$

As can be seen from the above equation, the Reliability Function $R(t)$ and the Unreliability Function $F(t)$ can be calculated by taking the integral of the Probability Density Function, as below:

$$F(t) = \int_0^t f(t)dt \qquad (2\text{-}5)$$

$$R(t) = 1 - F(t) = 1 - \int_0^t f(t)dt = \int_t^\infty f(t)dt \qquad (2\text{-}6)$$

Figure 2.6 shows a schematic of $f(t)$, $R(t)$, $F(t)$.

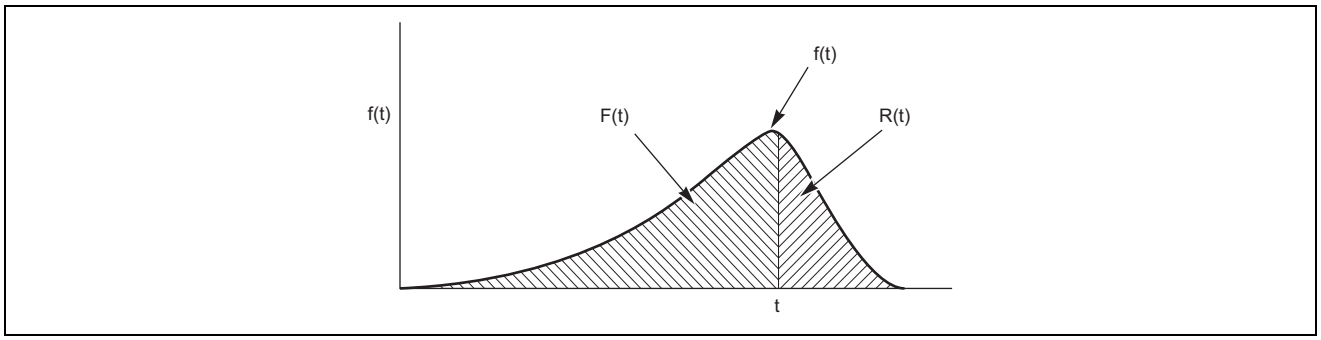

Figure 2.6 Schematic of $f(t)$, $R(t)$, $F(t)$

(3) Failure Rate Function

The Failure Rate Function (also known as "hazard function") is defined as the rate of failures, that occur per time (t) given below, out of all sample performing normally until the time (t) passes after particular device, part, or component is being used. The Failure Rate Function, $\lambda(t)$, is given by

$$\lambda(t) = f(t)/R(t) \qquad (2\text{-}7)$$

Each information that f(t),R(t), or $\lambda(t)$ possesses is equivalent. Using previously described information and by expanding equations (2-4), (2-5), (2-6) and (2-7), we can calculate $R(t)$ and $f(t)$ and $\lambda(t)$.

The Failure Rate Function is also known as the Instantaneous Failure Rate. This is often used to express reliability of semiconductor devices and other components. Instantaneous Failure Rate is theoretically very accurate, but in practice it is impractical to calculate failure rate at a point of time in a short period. Therefore, one time period of 1000 hours, one month or one year, is selected and the Mean Failure Rate is used.

Mean Failure Rate = Total failures in the period / Total operating time in the period

The values of Mean Failure Rates are expressed in unit of % per 1000 hours or ppm/1000 hours. The more common term Failure in Time (FIT) is widely used as a unit to express the failure rate:

$1\ FIT = 1 \times 10^{-9}\ 1/h = 1ppm/1000h$

Number of failures / (actual number of devices tested × actual operation time)

However, if the failure rate is 100 FIT the probability of a failure developing is 1 in 10^7 of operating hours, but this does not mean that the life of an individual component is 10^7 operating hours.

It is important to understand that the total operating hours (= actual number of devices tested × actual operation time) are not obtained by focusing on one single component.

(4) Cumulative Hazard Function

The Reliability Function $R(t)$ and Failure Rate Function $\lambda(t)$ can be determined by expanding (2-7) from equation (2-4) to produce the following relation shown in equation (2-8).

$$R(t) = exp\left[-\int_0^t \lambda(t)dt\right] \quad (2\text{-}8)$$

Further if the cumulative hazard function $H(t)$ is defined by the expression (2-9), then

$$H(t) = \int_0^t \lambda(t)dt \quad (2\text{-}9)$$

where $\lambda(t)$ expresses a Weibull distribution, the following relation applies.

$$R(t) = e^{-(\frac{t}{\eta})^m} \quad (2\text{-}10)$$

Therefore,

$$H(t) = (\frac{t}{\eta})^m \quad (2\text{-}11)$$

Further

$$R(t) = exp\,[-H(t)] \quad (2\text{-}12)$$

This relation will be applied later to hazard analysis.

(5) Criteria to Express Lifetime

Like the failure rate, “Time to Failure” is widely used. Time to Failure is defined as the time until failures occur in components (devices, parts, and elements) from when they commence to be used.

Generally semiconductor devices cannot be repaired, maintained and reused once a component fails. Therefore, they can be referred to as non-repairable (non-maintainable) products. The average time for non-repairable components (devices, parts, elements) to fail is defined as the Mean Time to Failure (MTTF) and can be expressed by the equation:

$$MTTF = \int_0^t tf(t)dt \quad (2\text{-}13)$$

or as the exponential distribution,

where

$f(t) = \lambda\, exp\,(-\lambda t)$
$R(t) = exp\,(-\lambda t)$
$\lambda(t) = \lambda\ (constant)$

then from equation (2-13) MTTF can be expressed as

$$MTTF = \int_0^\infty t\lambda e^{-\lambda t}dt = 1/\lambda \quad (2\text{-}14)$$

becoming the reciprocal of the failure rate.

2.6 Probability Distribution Used for Reliability Analysis

(1) Exponential Distribution

Exponential distribution is random failure-type distribution. Many results obtained through reliability tests of semiconductor devices are Decreasing Failure Rate (DFR) type and is not well adapted to the exponential distribution. However, the exponential distribution is sometimes used because it is the most fundamental distribution of reliability life, and random failures are found in the stable phase, which excludes early failures.

The Probability Density Function f(t) and the Reliability Function R(t) of exponential distribution are expressed by the equations:

$$f(t) = \lambda exp(-\lambda t) \quad (t \geq 0)$$
$$R(t) = exp(-\lambda t)$$

These are shown in Figure 2.7. Only parameter λ features the exponential distribution. The Mean Time to Failure (MTTF) becomes the reciprocal of λ.

$$MTTF = 1/\lambda$$

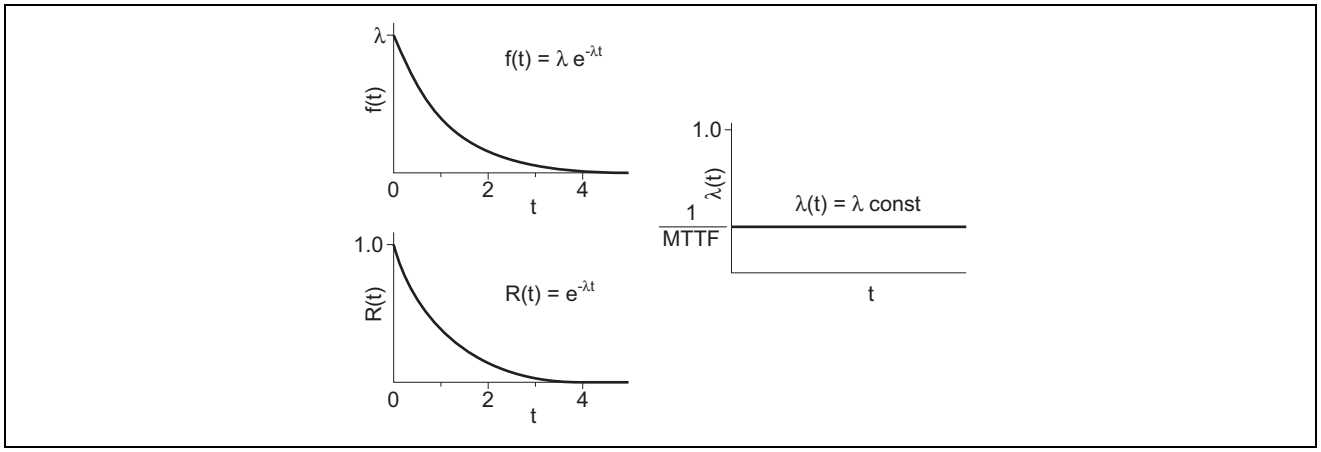

Figure 2.7 Exponential Distribution

(2) Normal Distribution

The normal distribution is widely used for general data analysis, the distribution of controlled characteristic values and errors, quality control, and other purposes. It is also used as a time to failure distribution. Examples to which this distribution applies can be seen especially in the case wear-out failures. The Probability Density Function f(t) and the Reliability Function R(t) of the normal distribution are expressed by the equations shown below.

As shown in Figure 2.8, the normal distribution has a symmetrical hanging bell shape, where μ = mean and σ = standard deviation.

$$f(t) = \frac{1}{\sqrt{2\pi}\cdot\sigma} e^{-\frac{(t-\mu)^2}{2\sigma^2}}$$
$$R(t) = 1 - \frac{1}{\sqrt{2\pi}\cdot\sigma} \int_{-\infty}^{t} e^{-\frac{(t-\mu)^2}{2\sigma^2}} dt \qquad (-\infty < t < +\infty)$$

In general, the normal distribution is abbreviated with mean μ and standard deviation σ, and is indicated by N (μ, σ^2). 68.3% of the total distribution falls within the range of μ ±σ, 95.54% within μ ±2σ, and 99.73% within μ ±3σ. 90% and 95% of the total distribution fall within the range of μ ±1.645σ and μ ±1.96σ, respectively.

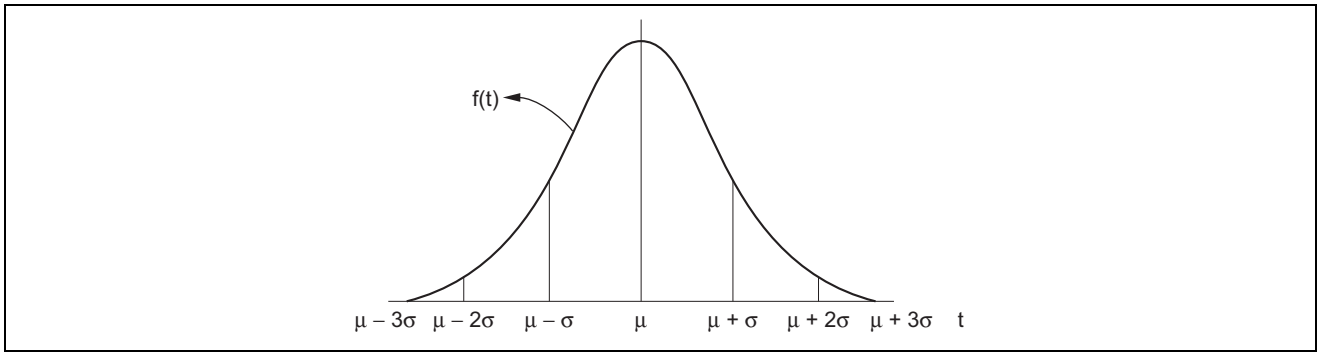

Figure 2.8 Normal Distribution

(3) Logarithmic Normal Distribution

When the logarithm of lifetime t conforms to the normal distribution, the distribution of lifetime is called the logarithmic normal distribution. The Probability Density Function f(t) and the Reliability Function R(t) are expressed by the equations:

$$f(t) = \frac{1}{\sqrt{2\pi}\cdot\sigma t} e^{-\frac{(\ln t-\mu)^2}{2\sigma^2}} \qquad (t \geq 0)$$

$$R(t) = 1 - \frac{1}{\sqrt{2\pi}\cdot\sigma}\int_0^t \frac{1}{t}\cdot e^{-\frac{(\ln t-\mu)^2}{2\sigma^2}} dt$$

(4) Weibull Distribution

The Weibull distribution was invented by W. Weibull in Sweden as an extension of exponential distribution in his research on metal fatigue. The Probability Density Function f(t) and the Reliability Function R(t) are expressed by the following equations, where m is the shape parameter and η is the scale parameter.

$$f(t) = \frac{mt^{m-1}}{\eta^m}\cdot e^{-(\frac{t}{\eta})^m} \qquad (t \geq 0,\ \eta > 0, m > 0)$$

$$R(t) = e^{-(\frac{t}{\eta})^m}$$

Failure rate λ (t) and its time derivative can be expressed by the following equations from the definition given by equation (2.7).

$$\lambda(t) = \frac{mt^{m-1}}{\eta^m}$$

and

$$\frac{d\lambda(t)}{dt} = \frac{m(m-1)t^{m-2}}{\eta^m}$$

Thus, the failure rate decreases while m < 1, remains constant when m = 1, and increases while m > 1 with the passage of time.

As already described, in life tests of semiconductor devices, the “m > 1” distribution form appears normally.

For shape parameter “m” of the Weibull distribution is correlated with the temporal change of the failure rate, it is helpful for elucidating degradation phenomena from reliability test data. In general, lifetime distribution vary with the difference of failure mechanism or degradation phenomenon. Accordingly, parameters m and η of the Weibull distribution vary with the change of failure mode or failure mechanism or with stress change. The following consideration is possible by Weibull plot analysis in comparison between two lifetime data sets from reliability tests with different test condition.

(1) If only η changes while m remains comparable, the physical failure cause remains unchanged and only the speed of degradation has changed.

(2) If only m changes, the physical failure cause has also changed.

Weibull distribution is widely used as a means of lifetime analysis acquired by reliability tests. Parameters m and η of the Weibull distribution can be estimated easily by using a Weibull probability paper.

2.7 Reliability Testing

Reliability testing is a series of laboratory tests carried out under known stress conditions to evaluate the lifetime of a device or system.

Reliability tests are performed to ensure that semiconductor devices maintain the performance and functions throughout their life. These reliability tests aim to simulate or accelerate by the stresses that the semiconductor device may encounter during all phases of its life, including mounting, aging, field installation and operation. The typical stress conditions are defined in the testing procedure described later in this document.

Reliability tests are performed at various stages from development to mass-production. The purpose and contents differ in each stage. When testing semiconductor devices, (1) the subject and purpose of each test, (2) the test conditions, and (3) the judgement based on test results must be considered. Table 2.2 shows the phase, purposes, and contents of some reliability tests carried out at our laboratories.

Table 2.2 Examples of Reliability Testing Conducted When New Products are Developed

Phase	Purpose	Contents
Development of new device	To verify that the reliability target and the customer's reliability requirements are satisfied	The following and other tests are carried out as required: 1. Accelerated tests 2. Marginal checks 3. Physical structural analysis
Development or change of design, processes and materials	To verify that the reliability target and the customer's reliability requirements are satisfied with regard to the materials and processes. To understand the quality characteristics and limits as influenced by materials and processes	TEGs or products are used to perform acceleration tests and other analyses as required with focusing on the characteristics and changes of materials and processes.
Trial run before mass production	To verify that the production quality is at the specified level	1. Early warning system is performed focusing on the device parameters and characteristics. 2. Reliability tests are carried out to confirm the fluctuations and stability of the device parameters and characteristics in the initial stage of mass-production.

Note: TEG: Test element group. The devices for evaluation that are extracted from the structural elements of the semiconductor device.

2.8 Reliability Test Methods

Reliability tests are performed under known stress conditions. A number of semiconductor related standards have been established including Japan Electronics and Information Technology Industries Association (JEITA) standards, U.S. Military (MIL) standards, International Electrotechnical Commission (IEC) standards, and Joint Electron Device Engineering Council Solid State Technology Association (JEDEC). The testing procedures and conditions differ slightly from one another, their purpose is the same.

The test period and condition are determined in the same manner as the number of samples, by the quality grade of design and the quality grade required by the customer. However, mounting conditions, actual operating lifetimes, as well as the acceleration of tests are considered to select the most effective condition.

Reliability tests must be reproducible. It is preferable to select a standardized testing method. For this reason, tests are carried out according to publicly available testing standards.

The definition of a device failure is important in designing reliability tests. It is necessary to clarify the characteristics of the device being tested and set failure criteria. This failure criteria must be used in determining whether or not any variations in the device characteristics before and after the test is in an allowable range.

The reliability test is usually conducted by sampling from a population within the range that the design rule and manufacturing process are the same. The sampling criteria for semiconductor devices is determined by both the products reliability target and the customer's reliability requirements to achieve the required grade of lot tolerance percent defective (LTPD). The reliability tests for materials and processes are performed with the number of samples determined independently.

For newly developed processes and packages, however, there are cases in which the existing processes and packages cannot use acceleration factor within the maximum rating of the products or in which new failures cannot be detected within a short period of time. In these cases, it is important to perform reliability testing based on the failure mechanism by using Test Element Groups (TEGs). To ensure reliability during product design stage, we conduct testing according to the failure mechanism in the same process as the products, clarify the acceleration factor for temperature, electric field, and other factors, and reflect this in the design rules used in designing the product.

2.9 Accelerated Lifetime Test Methods

The reliability of semiconductors varies greatly an actual operating with an actual operating environmental factors such as ambient temperature, humidity, voltage and current.

The accelerated lifetime test is a method to estimate the failure rate of a component during actual use. The lifetime test focuses on the specific stresses of the environment in which the component is used, and this test is performed using the conditions of these stresses as parameters. This method is widely used, when developing the new products which adopted a new processes.

Following is an explanation of failure models, which form the basis for accelerated lifetime models, and statistical analysis methods.

2.9.1 Fundamental Failure Model

(1) Reaction Theory Model

The reaction theory model is the most commonly used failure model for accelerated lifetime tests of semiconductor devices. Generally, deterioration and destruction of substances are due to changes at the atomic and molecular level. The mechanisms of such changes include diffusion, oxidation, adsorption, dislocation (displacement), electrolysis, and development of corrosion cracks. The progression of these changes promotes deterioration of material and parts, then surpasses a certain threshold and finally leads to failure. This is called the reaction theory model. At one point in the process, from normal conditions to deteriorated conditions, there is an energy threshold. The energy needed to surpass

this threshold must be drawn from the environment. This threshold energy is called the activation energy. Figure 2.9 shows a schematic of the energy condition before and after the reaction.

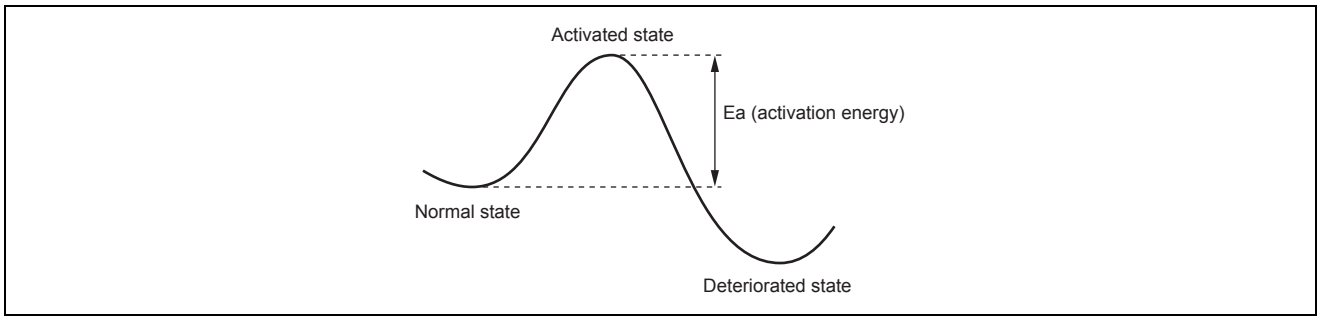

Figure 2.9 Activation Energy

The dependence of reaction rates on temperature was discovered by Arrhenius and the Arrhenius equation is widely used.

If the reaction rate is K, then this equation can be expressed as

$K = \Lambda \exp(-Ea/kT)$

where Λ: Reaction rate constant
Ea: Activation Energy (eV)
k: Boltzmann Constant [8.617×10^{-5} (eV/K)]
T: Absolute Temperature (K)

If the time to failure is L, then

$L = A \exp(Ea/kT)$

and by taking the logarithm of both sides, it gives the equation;

$\ln L = \ln A + Ea/kT$

This equation shows the logarithm of lifetime (L) plotted against the reciprocal of temperature is linear, and the gradient of the straight line produced represents the activation energy. Then, based on this, the acceleration coefficient between two given temperatures can be derived.

For example, if L_1 and L_2 represent the lifetimes at T_1 and T_2 respectively, then

$\ln(L_1/L_2) = 1/k\,(1/T_1 - 1/T_2)\,Ea$

This equation provides an acceleration factor to determine the activation energy of a reaction. Figure 2.10 shows a schematic of this model.

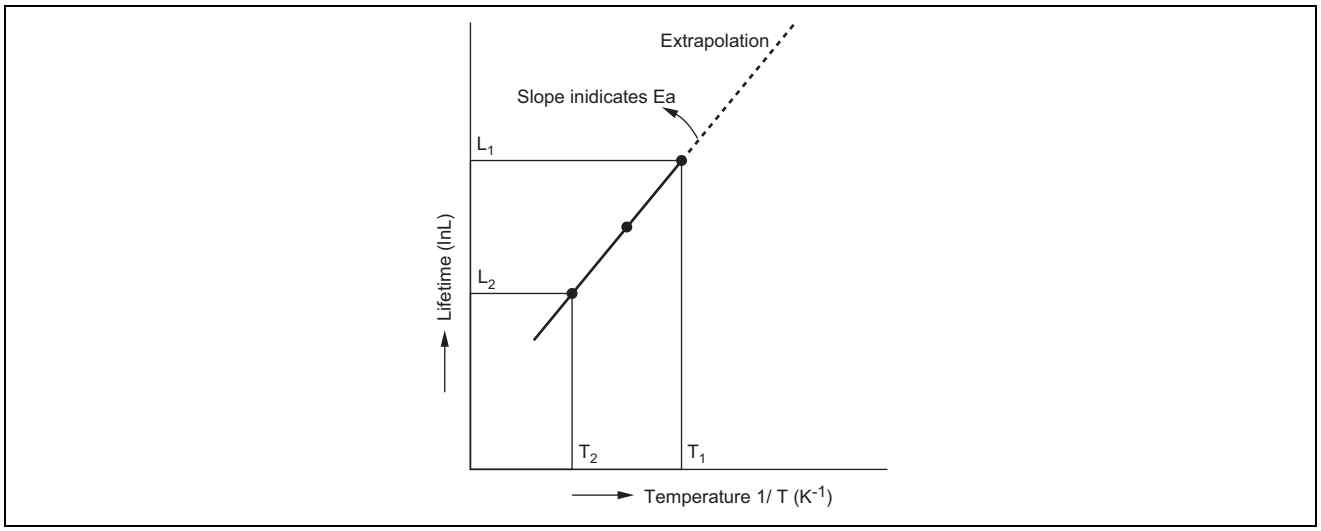

Figure 2.10 Schematic of the Arrhenius Model

(2) Eyring Model

While the Arrhenius model emphasizes the dependency of reactions on temperature, the Eyring model is commonly used for demonstrating the dependency of reactions on stress factors other than temperature, such as mechanical stress, humidity and voltage.

The standard equation for the Eyring model is as follows

$$K = a(kT/h) \cdot exp\ (-Ea/kT) \cdot S^{\alpha}$$

where a, α: Constants
h: Planck Constant
S: Stress Factors other than Temperature
k: Boltzmann Constant
T: Absolute Temperature (K)

If the temperature range T is small, then this equation can be approximated as

$$K = A\ exp\ (-Ea/kT) \cdot S^{\alpha}$$

Further, if we focus on stress factors other than temperature then lifetime (L) is proportional to 1/K and then taking the logarithm gives the equation

$$ln\ L = A - \alpha\ ln\ S$$

where A: Constant

The Eyring equation is often applied when conducting accelerated stress tests.

For example consider heat fatigue of plastics. If a stress is set to S and a life is set to N, the life in the stress S_1 and S_2 is set to N_1 and N_2, respectively, It can be expressed by the equation:

$$ln\ (N_1/N_2) = -\alpha\ ln\ (S_1/S_2)$$

Further in the example of temperature cycle tests by substituting the change in temperature ΔT for stress and let N be the number of temperature cycles to failure, then the above equation can be expressed as

$$ln\ (N_1/N_2) = -\alpha\ ln\ (\Delta T_1/\Delta T_2)$$

Figure 2.11 shows a graph of the Eyring Model.

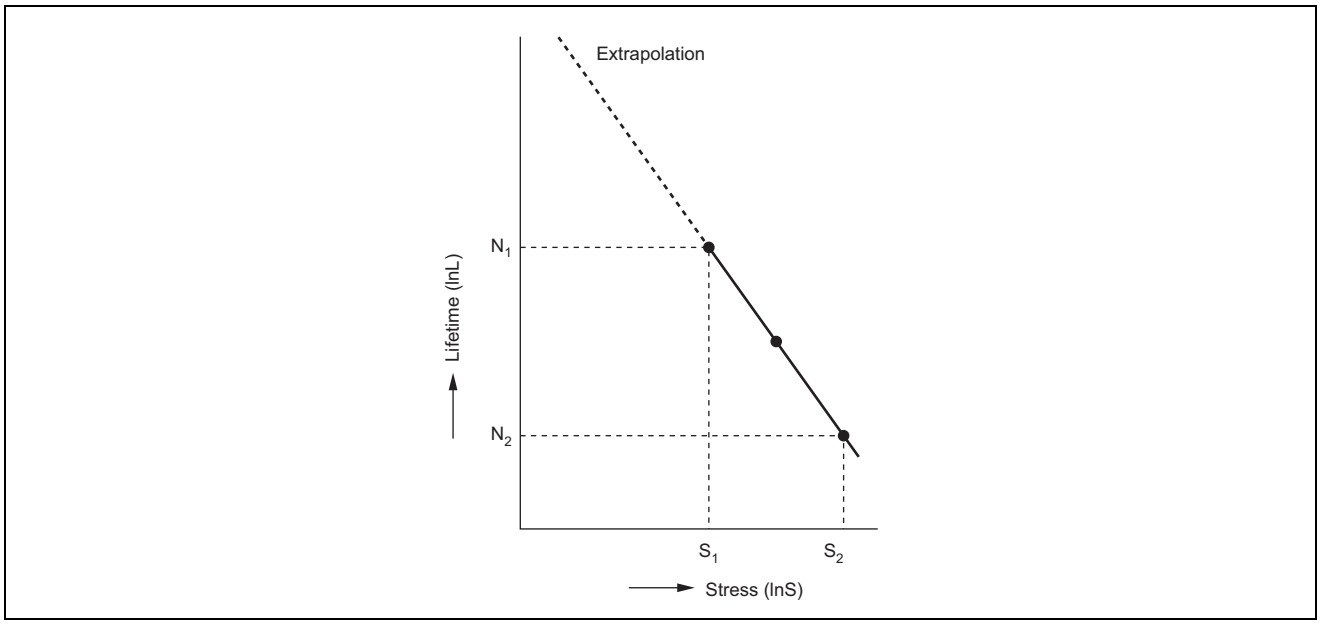

Figure 2.11 Schematic of the Eyring Model

(3) Stress Strength Model

As shown in Figure 2.12, in spite of having safe margin between material strength and stress, it is the model of resulting in failure because material strength decreases by degradation of material strength due to stress.

As shown by stress strength distribution, failure includes an element of probability.

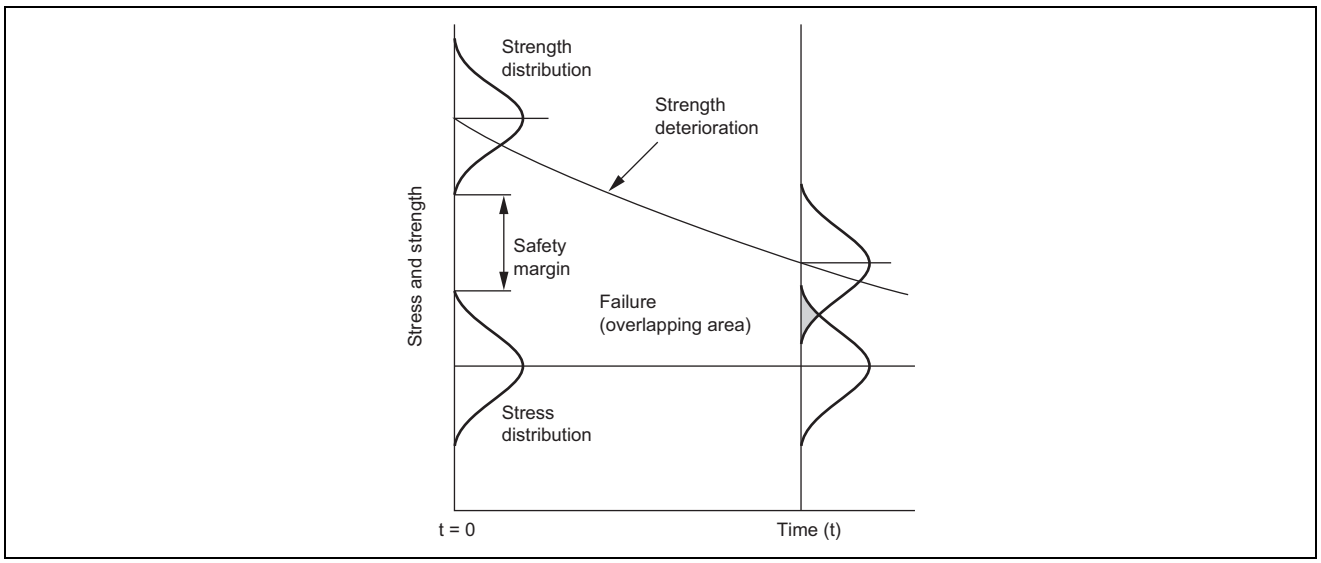

Figure 2.12 Stress Strength Model

2.9.2 Method of Accelerated Life Testing

(1) Means of Acceleration

Accelerated lifetime tests are conducted under stress conditions more severe than actual conditions of use. They are the methods of promoting a failure mechanism physically and chemically and presuming the life time and failure rate in an actual use condition for a short time.

The means of acceleration are:

- Increase the stress of stressors (e.g. temperature, voltage)
- Increase the frequency of the applied stress.
- Use tighter failure criteria.
- Use test vehicles/structures specific to the failure mode

(2) Stress Applying Method

Examples of how stress is applied in accelerated lifetime tests are constant stress, and step stress methods. The constant stress method is a lifetime test where stress, such as temperature or voltage, is held constant and the degree of deterioration of properties and time to failure lifetime distribution are evaluated. In the step stress method, contrary to the constant stress method, the stress applied to the sample is periodically increased in stepped manner and note is taken of which increase in stress causes failure to occur. This relation is shown in Figure 2.13. In the Figure, the continuously increasing stress test can be considered as a step stress test the stress applied time in each step is extremely short.

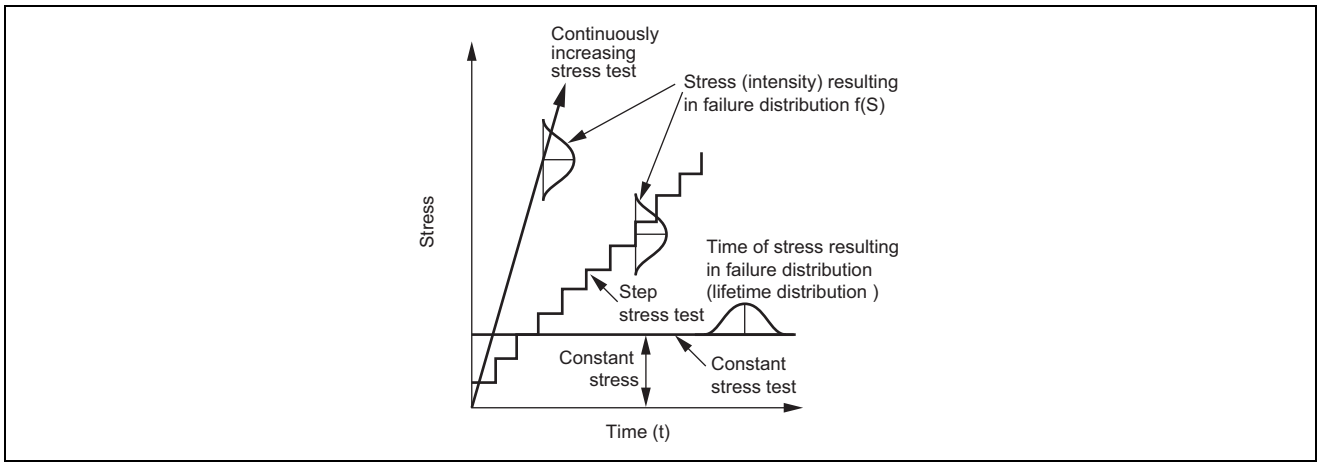

Figure 2.13 The Outline of Each Stress Tests

The constant stress method determines the lifetime distribution for a given stress when time is constant. Assuming the failure mechanism does not change, the results obtained from these two methods can be expected on the same straight line in a graph of the Arrhenius model or the Eyring model.

Representative examples of tests using the constant stress method, the step stress method, and the cyclic stress method, a variation of the constant stress method, are shown in Table 2.3.

Table 2.3 Distribution of Representative Accelerated Lifetime Tests

Stress Applying Method	Purpose	Accelerated Test	Main Stressor	Failure Mechanism
Constant stress method	Investigation of the effects of constant stress on a device	High-temperature storage test	Temperature	Junction degradation, impurities deposit, ohmic contact, inter-metallic chemical compounds
		Operating lifetime test	Temperature Voltage Current	Surface contamination, junction degradation, mobile ions, Electromigration (EM)
		High temperature high-humidity storage	Temperature Humidity	Corrosion, surface contamination, pinhole
		High temperature high-humidity bias	Temperature Humidity Voltage	Corrosion, surface contamination, junction degradation, mobile Ions
Cyclic stress method	Investigation of the effects of repeated stress	Temperature cycle	Temperature difference Duty cycle	Cracks, thermal fatigue, broken wires and metallization
		Power cycle	Temperature difference Duty cycle	Insufficient adhesive strength of ohmic contact
		Temperature-humidity cycle	Temperature difference Humidity difference	Corrosion, pinhole, surface contamination
Step stress method	Investigation of the stress limit that a device can withstand	Operating test	Temperature Voltage Current	Surface contamination, junction degradation, mobile ions, EM
		High-temperature reverse bias	Temperature Voltage	Surface contamination, junction degradation, mobile ions, TDDB

2.10 Reliability Prediction Based on the Failure Mechanism

The prediction of a failure rate for semiconductor devices when used in electronic systems is also important for system reliability and integrity design.

The reliability of semiconductor devices is considered using three major failure periods: initial failures, random failures, and wear-out failures. Of these, wear-out failures have a well-defined distribution, implying that you need only a small number of samples to recognize their distribution.

The failure mechanisms related to the wafer process will be explained in section 3. Typical examples such as TDDB, EM, HC, and NBTI are well-known.

Meanwhile, the trend in product development is toward increasingly shorter development periods, and the meeting of user requirements has become a critical task. To effectively build in quality in the development and design phases for new products within the allotted time, we use the Failure Mode and Effects Analysis (FMEA) method and the Design Review Based on Failure Mode (DRBFM) method in the design review (DR) conducted at the beginning of development. To meet the requirements for the product use condition and for quality, we strive to identify reliability related failure modes and mechanisms so that we can build in quality in the design phase. In the first DR phase, we plan on accelerated tests that conform to the failure modes and mechanisms. Prior to product development, we conduct the accelerated tests using the TEGs and use the results to build in both quality and reliability and to create design manuals (design rules). This allows us to build in quality in the design phase.

A variety of typical failure mechanisms are illustrated in section 3. For information about how to test reliability based on these failure mechanisms, refer to the Japan Electronics and Information Technology Industries Association (JEITA) standard (JEITA ED-4704A) and other related standards.

2.10.1 Example of Predicting the Early Failure Rate (Early Failures from Dielectric Breakdown)

The typical early failure mechanism, mainly for MOS devices, is the degradation of oxide films over time. The results of reliability testing based on this failure mechanism provide us with data about electric field and temperature acceleration. After converting the data to an actual use time, we use the following method to predict reliability.

Based on data of failure rate (voltage stress, aging, etc.) in the screening process, we make predictions from the calculations by assuming that the early failures occurring after screening according to the Weibull distribution. Renesas defines early failures as the fraction defective (ppm) assumed as one year after a product is launched on the market. Figure 2.14 presents a conceptual overview of lifetime prediction based on Weibull plotting of data acquired through screening.

A major characteristic of early failures is that the shape parameter (m) is small. Identifying this with a test requires a large amount of data. Reliability prediction based on the Weibull distribution refers to the process of predicting the reliability of products on the market both from screening conditions (at the wafer and package levels) through burn-in and other tests and from the number of defectives produced under those conditions. For example, you can estimate the shape parameter (m) by plotting burn-in defectives on the Weibull graph. You can also predict the market failure rate by obtaining the scale parameter (η) as setting the aging time. The following is an example application using this method.

Let the screening time be “ta”, the reliability function after screening be “R(ta)”, and the time during which a product has been available in the marketplace be “t”. Assuming that the reliability measured at the time (ta + t) is R(ta + t), the cumulative failure rate measured from “ta” to “ta + t” will be equal to “R(ta) – R(ta+t),” where the time “ta” is equivalent to the value converted to the actual working time. If R(ta) and F(ta) are the reliability function and unreliability function, respectively, immediately after screening and R'(t), and F'(t) are the reliability function and unreliability function, respectively, for the time from “ta”, then

$$R(ta) = \exp\{-(ta/\eta)^m\} \quad (2\text{-}15)$$

$$F'(t) = 1\text{-}R'(t) \quad (2\text{-}16)$$

$$R'(t) = R(ta + t)/R(ta) = \exp\left[-\{(ta + t)/\eta\}^m + (ta/\eta)^m\right] \quad (2\text{-}17)$$

substitute the shape parameter (m) and the reliability obtained from the result of screening into equation (2-15) to calculate the scale parameter (η).

$$\eta = ta/\{-\ln R(ta)\}^{1/m}$$

Substitute the scale parameter (η) into equation (2-17). From this and the relation with equation (2-16), you can obtain the F'(t) unreliability function from the time “ta” used as the starting point. This is the cumulative failure rate.

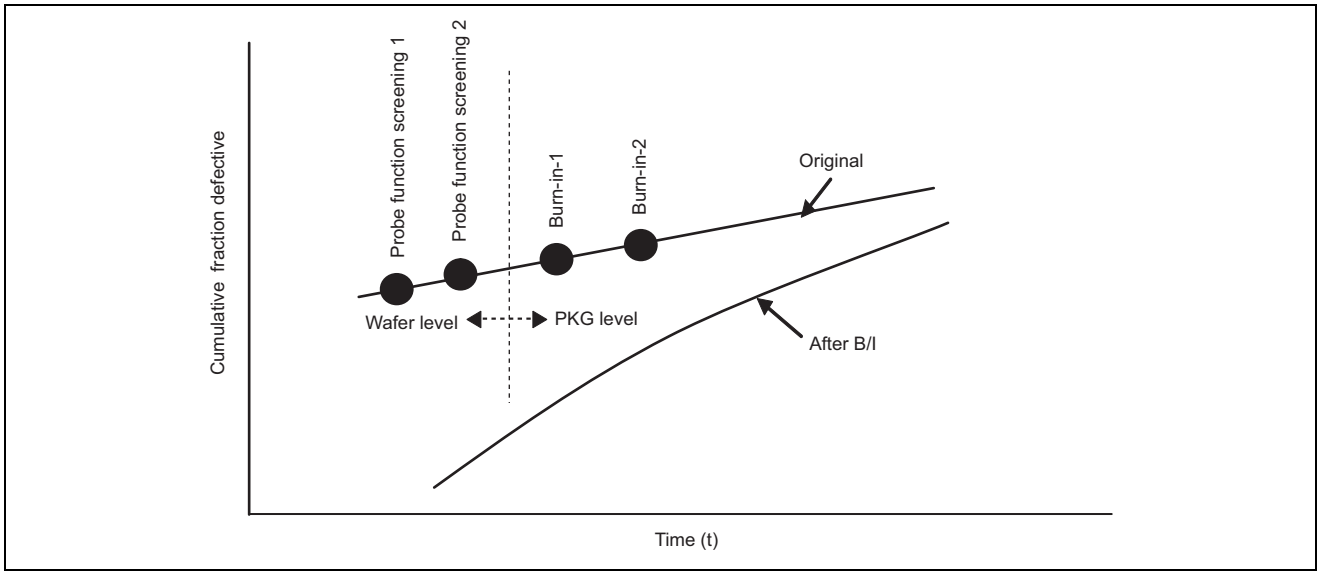

Figure 2.14 Life Prediction through Weibull Plotting

2.10.2 Example of Predicting the Random Failure Rate (Method of Estimating a Failure Rate at a 60% Confidence Level)

The internal quality certification conducted by Renesas during the development stage of semiconductor devices is an overall evaluation of quality and reliability, not just an evaluation of electrical properties and functionality. During reliability evaluation, we perform a variety of reliability tests involving such factors as operating lifetime, moisture resistance, thermal resistance, mechanical resistance, and environmental resistance, and judge pass or fail using criteria for each product according to whether the product meets market requirements.

The reliability data which Renesas publishes summarize the reliability test results.

Note that the format of reliability data differs slightly according to device type. Table 2.4 shows an example of a specific microcontroller product (function: single-chip microcontroller, wafer process: 0.8 µm, CMOS, package: PLCC).

The reliability tests include a lifetime test (endurance test), environment test, and mechanical test. The lifetime test evaluates device elements such as the metallization, the oxide films and so on formed on the chip, as well as the moisture resistance of the plastic packages. The environment test mainly evaluates resistance to the thermal stress exerted during use.

Test results are presented as the number of samples and the number of failures. You can check these results to see the failure rate for the product. For example, solderability in Table 2.4 has a lot tolerance percent defective (LTPD) of 10% pass standard, and high-temperature unbiased storage has a lot tolerance failure rate (LTFR) of 10%/1000 h.

Furthermore, failure rates can be estimated using the test results in the reliability data. The examples given here use the methods described in JIS C5003, “General Test Procedures for Failure Rate in Electronic Components”. Using the operation lifetime test results in Table 2.4, you can determine failure rates as follows.

$$\frac{\textit{Number of failures (r)} \times \textit{Coefficient (a)}}{\textit{Total test time (T)}} = \frac{0.92}{45 \times 1000}$$

$$= 2 \textit{ (\%/1000 hours)}$$

$$= 2 \times 10^{-5} \textit{ (1/hour)}$$

Assuming a confidence level of 60%, the calculation uses a = 0.92 (corresponds to the 60% confidence level), since the test resulted in no failures (r = 0) (See the JIS-C5003 standard.).

The value calculated here is the failure rate obtained under accelerated test conditions. When obtaining the failure rate under actual working conditions, however, the above value must be divided by the acceleration coefficient obtained from the test conditions and actual working conditions.

$$\textit{Failure rate} = \frac{\textit{(Cumulative number of samples failed)} \times \textit{60\% confidence level}}{\textit{(Total number of test samples from process family} \times \textit{test time} \times \textit{acceleration factor)}}$$

Temperature and apply voltage are the acceleration factors for accelerated tests. Activation energy is used for temperature acceleration, and has own value for each failure mechanism.

The above example for calculating a failure rate is based on microcontroller module design, layout design, wafer process design, structure design and package design, as well as design for components and materials.

Renesas conducts reliability tests on standardized TEGs and qualify each device element and process design. Products quality and reliability are maintained at the same level in the products because each product is composed of these standardized elements. Even if no failures at the test, the estimated failure rate will be relatively large because the total device hours (sample size × test time) is small due to the limited sample size. However the actual data on other products show much smaller failure rate.

Renesas is committed to realize reliability design and promotes the standardization in design. Standardization in design activity makes the quality and reliability for products as the same level even if the functional design or characteristics design are different. So the analysis on the reliability test results in the family products is important for the study on product reliability. For example CMOS 1.3 μm, 0.8 μm, 0.5 μm, 0.35 μm for wafer design and DIP, QFP, PLCC for package design are standardized. Products applying the same wafer design or package design are categorized as the product family.

Custom logic ICs or microcontroller ICs support various option for characteristics and function design from the same wafer process and the same package design. While memory products provide single functional design from each wafer process and package design. Table 2.4 shows the example of reliability test results.

Table 2.4 Reliability Test Results for Microcontroller A

Test Category	Test Item	Test Conditions	Results (Failure count/sample size)
Life test	High temperature operation life	Ta = 125°C, V_{CC} = 5.5 V, t = 1000 h	0/45
	High temperature storage life	Ta = 150°C, t = 1000 h	0/22
	Low temperature storage life	Ta = –55°C, t = 1000 h	0/22
	Temperature humidity storage	Ta = 65°C RH = 95%, t = 1000 h	0/77
	Temperature humidity bias	Ta = 85°C, RH = 85%, V_{CC} = 5.0 V, t = 1000 h	0/22
Environment test	Temperature cycle	–55°C to 150°C, 200 cycles	0/45
	Thermal shock	0°C to 150°C, 15 cycles	0/22
	Solderability	230°C, 5 s, rosin type flux	0/22
	Resistance to soldering heat	Infrared reflow 260°C, 10 s	0/22
	Pressure cooker (Autoclave)	Ta = 121°C, RH = 100%, t = 100 h	0/22
Mechanical test	Terminal strength (Pull test)	2.5 N, 10 s, 1 time	0/22

Next we will explain the general procedure for failure rate prediction of Renesas semiconductor devices, based on reliability test data.

(1) Failure Rate Prediction Based on Temperature Accelerated Tests

Temperature accelerated tests induce failures in a shorter period of time than occurrence at actual operating environment. These tests are thermal stress tests that accelerate the failure reaction inside semiconductor devices. In other words, thermal stress induces chemical and physical reactions and devices will fail when exceeding their withstanding threshold against thermal stress. For example, breakdown of junction, gate dielectrics and interlayer dielectrics, and breaks in metallization or contacts, are the failure mechanism. The reaction kinetics model discussed earlier can explain these kinds of phenomena.

High temperature operating life and high-temperature storage life are representative test methods for temperature acceleration. The temperature acceleration factor is expressed by a unit of energy called as activation energy (*Ea*). Activation energy shows a peculiar value for every failure mechanism. If the *Ea* value is large, the temperature acceleration is high. If it is small, the temperature acceleration is also low. *Ea* is indispensable information when predicting a failure rate from a reliability test results.

The failure rate under actual-use conditions can be predicted from the high-temperature operating test (125°C, 5.5-V operating test) in Table 2.4, “Microcontroller A Reliability Test Results,” as explained below.

The estimated condition of actual use are

$Ta = 40°C,\ V_{CC} = 5.0\ V$

assuming $Tj = Ta$, calculated as follows. (Where *Tj* is the junction temperature.)

Generally activation energy (*Ea*) can be determined from the evaluations of the various thermal conditions, if it assumes as follows based on the previous experience

$Ea = 0.80\ eV$

then, the procedure for prediction of the failure rate for conditions of actual use is as follows.

First, calculate the acceleration rate (temperature acceleration factor γr) for accelerated tests compared to actual use. Multiplication of test time for accelerated tests and the temperature acceleration rate is equivalent to operating time for the actual use. In other words, if temperature accelerated test time is L(*Tb*), the operation time under conditions of actual use is L(*Ta*), then

$L(Ta) = \gamma r \times L(Tb)$

From the Arrhenius model, the relation between L(Ta) and L(Tb) can be expressed by

$L(Ta) = C \bullet e^{Ea/kTa},\ L(Tb) = C \bullet e^{Ea/kTb}$

where

Ta: Temperature at actual use conditions (40°C)
Tb: Temperature at accelerated conditions (125°C)
Ea: Activation Energy (0.80 eV)
k: Boltzmann Constant $(8.617 \times 10^{-5}\ eV/K)$
C: Constant

Therefore, the acceleration factor γr is

$$\gamma r = \frac{L(Ta)}{L(Tb)} = \frac{e^{Ea/kTa}}{e^{Ea/kTb}}$$

This shows that compared to conditions of actual use, the temperature accelerated test has an equivalent acceleration of approximately 560 times and time to device failure at accelerated tests is reduced by a factor of 1/560 times. Consequently, the operating time L(*Ta*) under actual use conditions is equivalent to

$$L(Ta) = 560 \times 1{,}000 \text{ (h)}$$
$$= 560{,}000 \text{ (h)}$$

If we consider the case where four individual product reliability test data available from the same wafer process in microcontroller A device family,

$$\text{Failure rate} = 5.1 \times 10^{-6} \text{ (1/h)}$$

The failure rate for actual use conditions can be provided so as to divide γr into temperature accelerated failure rate.

$$\text{Failure rate} = 5.1 \times 10^{-6}/560$$
$$= 9.1 \times 10^{-9} \text{(1/h)} \approx 9 \text{ (FIT)}$$

Therefore, 9 (FIT) becomes the expected value for the microcontroller A.

If the temperature accelerated test is 1,000 hours of continuous operation, this is equivalent to 560,000 hours (roughly 64 years) of continuous operation for actual use conditions. However, very few systems, equipment, or devices are used continuously for 560,000 hours. When the stress in operating conditions is larger than that in standby, multiplication of stress reduction factor makes failure rate close to real failure rate.

In temperature accelerated tests, the higher the temperature within a certain range, the shorter the time to failure. However excessive temperature may cause unexpected failure in actual use (in other words, failure may be caused by a completely different failure mechanism than what will be found in actual use). Therefore certain precautions must be taken. Generally, 125°C is used operating life tests to minimize probability of inducing different failure mechanisms.

(2) Failure Rate Prediction Based on Temperature Cycle Tests

Temperature cycle tests use rapid temperature changes as an acceleration factor. The alternating temperature changes between high and low generate stress in semiconductor devices. This stress can activate failure factors that subsequently induce failures in a shorter time when compared to failure under “actual use” conditions. In other words, temperature cycles repeatedly cause heat stress inside semiconductor devices or other materials composing semiconductor devices. Consequently physical and mechanical reactions are accelerated and finally devices fail rapidly when exceeding their withstanding level against stress.

For examples, temperature cycle tests cause package cracks, wire open or short, and hermetically failure in package.

Various combination of high and low temperatures are prescribed; for example,

–65°C to 150°C
–55°C to 150°C
–55°C to 125°C
–45°C to 125°C
0°C to 125°C

Acceleration rate results in failures by temperature cycle depends on the difference between exposed temperatures and transition time from high to low or low to high, and also the storage time at high and low.

Stress S is proportional to temperature difference ΔT. The Eyring model between S and N is well known from the former experience, where N is the number of temperature cycles.

$ln\ N = ln\ C + (-n) \bullet ln\ \Delta T$

C: Constant

n: Temperature Difference Coefficient

The lifetime N (the number of temperature cycles) is proportional to the temperature difference ΔT to the minus nth power.

$N = C \times \Delta T^{-n}$

The n value for each failure mechanism varies; large n value means the higher acceleration, small n shows lower acceleration. The value n is indispensable information for the prediction of failure rate from the temperature cycle test results.

The failure rate under actual use conditions is predicted from the temperature cycle test results (temperature cycle –55°C to 150°C test) shown in Table 2.4, Microcontroller A Reliability Test Results.

The temperature difference ΔTb under test conditions is

$\Delta Tb = 150 - (-55) = 205$

The temperature difference ΔTa under actual use conditions is determined by the heat radiation from devices or systems when the power supply is on. It is also essential to consider the ambient temperature differences where the system is installed. If the system is set at in the room, temperature changes between on and off of air conditioning should be considered. Temperature difference a day should be cared for the case of outdoor use.

Assume

$\Delta Ta = 40°C$

Also, if we assume n to be 6, the acceleration coefficient $\gamma\sigma$ for actual use compared with the test condition is

$$\gamma\sigma = \frac{Na}{Nb} = \frac{C \times \Delta Ta^{-n}}{C \times \Delta Tb^{-n}} = \frac{\Delta Ta^{-n}}{\Delta Tb^{-n}}$$

$$= \left(\frac{40}{205}\right)^{-6} = 18{,}120$$

Consequently, the accelerated test can reduce the cycle time necessary that the device arrive at its life for actual use.

In case for microcontroller A, the test results are

–55°C to 150°C

200 cycles 0/45

The equivalent temperature cycle numbers for the actual working environment is

$Cycle\ count = 200 \times 18{,}120 = 3{,}624{,}000$

If, in the actual operating environment, 10 cycles of thermal stress are applied per day, the failure rate for a 60% confidence level can be predicted by

$$Failure\ rate = \frac{0.92}{45 \times (3{,}624{,}000/10) \times 24}$$

$$= 2.4 \times 10^{-9}\ (1/h)$$

$$= 2.4\ (FIT)$$

Therefore, failure rate for the microcontroller A can be predicted as approximately 3 FIT.

To expand the temperature range at higher and lower side is considered effective for the reduction of cycle time for failures. However excessive temperatures that exceed the device withstand level may cause unexpected failure in actual use (failures due to completely different failure mechanisms), therefore precautions must be taken. Generally, the temperature range between the maximum and minimum of storage temperature should be applied.

(3) Failure Rate Prediction Based on Moisture Resistance Tests

In moisture resistance tests, humidity stress is applied as an acceleration factor. Humidity stress test enhances the destructive chemical and physical reactions inside devices and accelerates the failure as a function of humidity. These phenomena can be described using the Arrhenius model.

For example, Temperature Humidity Bias and Temperature Humidity Storage are used for humidity acceleration tests. Typical test conditions for the former are the 85°C-85% RH bias test, and HAST (Highly Accelerated Temperature and Humidity Stress Test) where the temperature is 100°C or greater and the pressure is 1 atmosphere or greater. The latter are 65°C-95% RH unbiased test. The pressure cooker test (PCT) is also unbiased, where the temperature is 100°C or greater and the pressure is 1 atmosphere or greater.

Acceleration factors for moisture resistance tests are humidity, temperature and voltage. Then the lifetime for moisture resistance is expressed by a function of temperature (the Arrhenius model), humidity and voltage. This can be expressed by the following equation:

$$L(Tb) = C \cdot e^{Ea/kTb} \cdot (RH)^{-n} \cdot V^{-\alpha}$$

where, generally

L(*Tb*): Lifetime
C: Constant
RH: Relative Humidity
n: Relative Humidity Coefficient
V: Applied Voltage
α: Applied Voltage Coefficient

The *Ea*, *n* and α values are indispensable in the prediction of failure rate estimation under actual use from moisture resistance test results. These values, of course, differ according to the failure mode. Using Table 2.4, Microcontroller A Reliability Test Results as an example, following is an explanation of the procedure of predicting failure rate under actual use from Temperature Humidity Bias test results. Assuming conditions for actual uses are

$Ta = 30°C,\ V_{CC} = 5.0\ V,\ RH = 85\%$

The moisture resistance test conditions are

$Ta = 85°C,\ V_{CC} = 5.0\ V,\ RH = 85\%$

The test results are

1000 hours 0/22

Following is the procedure for predicting the failure rate under actual use. As we set the humidity and voltage values under tests the same as those in actual use, the relative humidity coefficient n and voltage coefficient α are not necessary for the calculation. Temperature acceleration should be examined for the above case. Activation Energy (Ea) is not possible to estimate directly from the test results due to no failure in the test, so we set Ea from the previous data as follows:

$$Ea = 1.0\ eV$$

From the Arrhenius model, L(Ta) and L(Tb) are

$$L(Ta) = C \bullet e^{Ea/kTa}$$
$$L(Tb) = C \bullet e^{Ea/kTb}$$

where

Ta: Actual use temperature conditions (30°C)
Tb: Accelerated temperature conditions (85°C)
Ea: Activation energy (1.0 eV)
k: Boltzmann constant ($8.6157 \times 10^{-5}\ eV/K$)
C: Constant

Therefore the coefficient γH under accelerated test is

$$\gamma H = \frac{L(Ta)}{L(Tb)} = \frac{e^{Ea/kTa}}{e^{Ea/kTb}}$$
$$= \frac{e^{[1.0/\{8.6157 \times 10^{-5}\ (273+30)\}]}}{e^{[1.0/\{8.6157 \times 10^{-5}\ (273+85)\}]}}$$
$$= 359.6$$

So the test conditions accelerate the speed results in failure by 360 times compared to that for actual use. Consequently, the operation time $L(Ta)$ under actual use conditions is equivalent to

$$L(Ta) = 360 \times 1000\ (h)$$
$$= 360{,}000\ (h)$$

Therefore, the microcontroller A failure rate for actual use can be predicted as

$$\text{Failure rate} = 0.92/(22 \times 360{,}000)$$
$$= 1.2 \times 10^{-7}(1/h)$$
$$= 120(FIT)$$

In moisture resistance tests, the higher the temperature and relative humidity within a certain range, the shorter the time to failure. However, when temperature and relative humidity exceed the device withstanding level, failures that would not occur in actual use sometimes happen (failures due to completely different failure mechanism), therefore precautions are deemed necessary. In tests like the PCT, where relative humidity is close to 100%, with a temperature of 100°C or greater, failure mechanisms sometimes change. For this reason individual failure analysis is essential. Furthermore, the sample calculations shown here are examples of single (isolated) stress conditions, and with these calculations very long expectant lifetime values can be obtained. However, under conditions of actual use, it is necessary that other factors also be considered.

(4) Failure Rate Prediction by Failure Data Collection

Collecting and analyzing actual failure data enables us to predict failure rate in the future. However complete data collection is almost impossible. Therefore, Hazard Function Analysis is effective on such a case because some hazard appears in the collected series data. The following is an example using the Hazard Function Analysis.

- Example

For the application of an electronic device, failure occurred by a specific failure mode. Note that two devices are mounted on each PCB and both devices on PCB are removed when the failure happened even if the failure is only one device on PCB.

Table 2.5 Failure Data

Time to Failure (*h*)	No. of Failures (*ri*)	Remarks
3,600	0	Total 200 electronic devices
6,000	1	2 samples taken
8,640	2	4 samples taken
13,140	5	10 samples taken
17,520	10	20 samples taken
26,280	17	

We can explain this using Weibull hazard probability paper.

First, the Weibull probability paper has the following format.

Right Vertical Axis: $ln\ ln\ \{1/[R(t)]\} = ln\ ln\ \{1/[1 - F(t)]\} = m\ ln\ t - m\ ln\ \eta$
Top Horizontal Axis: ln (t)
Left Vertical Axis: Unreliability Function $F(t)$ on a percentage (%) scale
Bottom Horizontal Axis: Time t

Therefore

Vertical Axis: $Y = ln\ ln\ \{1/[1 - F(t)]\}$

If Gradient: m
Horizontal Axis: $X = ln\ (t)$
Intercept: $b = -m\ ln\ \eta$

Then $Y = mX + b$

From the Cumulative Hazard Function expressed as $H(t) = (t/\eta)^m$
and taking the logarithm of both sides of the equation produces

$lnH(t) = m\ (lnt - ln\ \eta)$

Next by plotting t and $H(t)$ on the Weibull probability paper which has log-log scales, both produce a linear relationship and thereby obtaining m and η. From this relationship m and η, the Weibull parameter can be derived easily using spreadsheet software.

Table 2.6 Cumulative Hazard Table

Time to Failure (h)	X: ln (t)	No. of Failures	Hazard Value: (hi)	Cumulative Hazard Value: H(t)	y: ln H(t)
6,000	8.7	1	0.005 (1/200)	0.005	–5.298
8,640	9.06	2	0.010 (2/198)	0.015	–4.12
13,140	9.48	5	0.026 (5/194)	0.041	–3.194
17,520	9.77	10	0.054 (10/184)	0.095	–2.354
26,280	10.18	17	0.104 (17/164)	0.199	–1.614

Figure 2.15 shows this cumulative hazard Table plotted on Weibull probability paper. From this graph the respective values can be obtained.

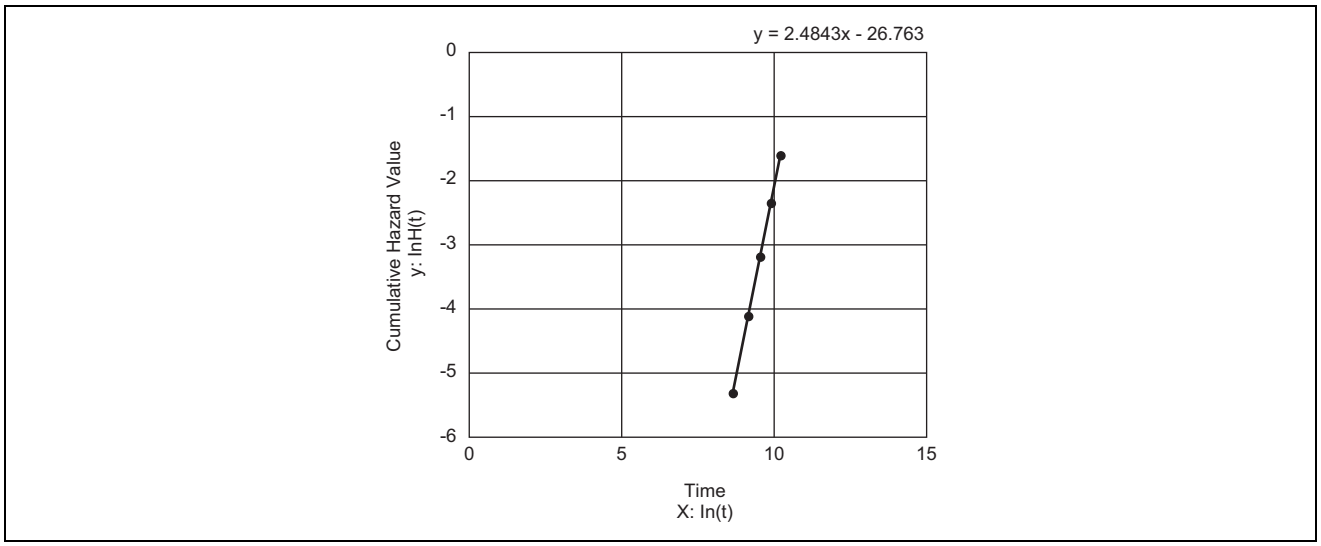

Figure 2.15 Lifetime Distribution Plot on Weibull Cumulative Hazard Paper

From the relationship shown between the equations y = 2.4843X – 26.763 and ln $H(t)$ = m(ln t – ln η), the following values can be determined:

Shape Parameter (m): 2.5
Scale Parameter (η): 47,700

2.10.3 Predicting Wear-Out Failures

Weibull shape parameter (m) for wear-out failures is greater than 1. Predicting service life, the time cumulative failures come to the specific value, is preferable rather than predicting failure rate when we discuss wear-out failure. For example, we define the service life as the time of 0.1% cumulative failures reached, then demonstrate the service life for each product. Accordingly, the useful life (as defined here) of individual product is checked. As for the known failure mechanism we demonstrate the service life of 0.1% cumulative failures for real application at product design stage using the suitable equation for the failure mechanism.

2.10.4 Post Screening (Future) Lifetime

The time (the lifetime) results in a certain cumulative failures is estimated below using the probability density function (PDF) for infant mortality failures following the fixed time(t) screening prior to product shipment. If we take the probability density function after the screening time (t_0) to be $f(t_0:t)$, this can be expressed by equation (2-18). (See Figure 2.16.)

$$f(t_0 : t) = \frac{f(t_0 + t)}{R(t_0)} \tag{2-18}$$

Note that $R(t_0)$ is the reliability function available until the time (t_0).

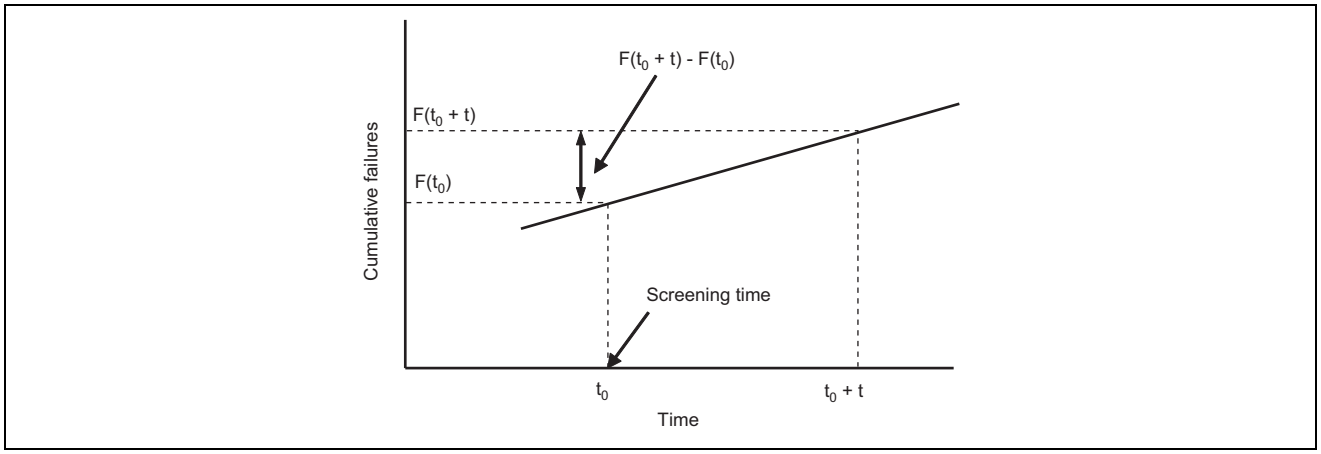

Figure 2.16 Post Screening (Future) Lifetime

If the probability density function, $f(t_0)$, has the Weibull distribution, the function can be expressed as

$$f(t_0) = \frac{m t_0^{m-1}}{\eta^m} e^{-\frac{t_0^m}{\eta^m}} \tag{2-19}$$

Substituting equation (2-19) into equation (2-18) gives the following probability density function:

$$f(t_0 : t) = \frac{m(t_0 + t)^{m-1}}{\eta^m} \bullet exp\left(-\frac{(t_0 + t)^m - t_0^m}{\eta^m}\right) \tag{2-20}$$

Therefore, the post screening unreliability function $F(t:t_0)$ will have the form of equation (2-21) below, and the estimated post screening (future) lifetime can be calculated.

$$F(t_0 : t) = 1 - exp\left(-\frac{(t_0 + t)^m - t_0^m}{\eta^m}\right) \tag{2-21}$$

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3. Failure Mechanisms

Reliability tests are designed to reproduce failures of a product which can occur in actual use. Understanding failure mechanisms from the results of reliability testing is extremely important to know the product is reliable in actual use. The effect of stresses (temperature, humidity, voltage, current, etc.) on the occurrence of failures can be identified by understanding the failure mechanisms. The product reliability in actual use can be predicted from the results of the reliability tests, which are conducted under accelerated conditions. Reliability-affecting problems of the product can also be identified by clarifying the failure mechanisms. Such information is useful in improving the product design and manufacturing processes to enhance the product reliability and quality, as well as in determining precautions for use which must be made clear to the customers. Reliability testing also provides useful information for the manufacturer to screen products using an optimal method selected according to the identified failure mechanisms. Furthermore, in the event of a failure reported in the market, understanding of the failure mechanisms enables the manufacturer to take prompt and proper measures for correcting the design and/or manufacturing processes, so that the recurrence of the failure can be prevented.

This chapter introduces typical failure mechanisms of semiconductor devices that can be encountered.

3.1 Failure Classification

Statistical methods and methods for treating failure from a physical standpoint are used to analyze semiconductor device reliability. This approach is called the physics of failure. Its objective is to make failure mechanisms clear by understanding the physical characteristics of failure down to the atomic and molecular levels.

Semiconductor device failure modes are generally divided into open circuits, short circuits, degradation, and others. The relationship between these failure modes and their failure mechanisms is detailed in Table 3.1.

Table 3.1 Failure Factors, Mechanisms, and Modes

Failure Factors		Failure Mechanisms	Failure Modes	Example
Diffusion Junction	Substrate Diffused junction Isolation	Crystal defect Impurity precipitation Photoresist mask misalignment Surface contamination	Decreased breakdown voltage Short circuit Increased leakage current	
Oxide film	Gate oxide film Field oxide film	Mobile ion Pinhole Interface state TDDB Hot carrier	Decreased breakdown voltage Short circuit Increased leakage current h_{FE} and/or Vth drift	Figure 3.1
Metallization	Interconnection Contact hole Via hole	Scratch or void damage Mechanical damage Non-ohmic contact Step coverage Weak adhesion strength Improper thickness Corrosion Electromigration Stress migration	Open circuit Short circuit Increased resistance	Figure 3.2
Passivation	Surface protection film Interlayer dielectric film	Pinhole or crack Thickness variation Contamination Surface inversion	Decreased breakdown voltage Short circuit Increased leakage current h_{FE} and/or Vth drift Noise deterioration	
Die bonding	Chip-frame connection	Die detachment Die crack	Open circuit Short circuit Unstable/intermittent operation Increased thermal resistance	Figure 3.3
Wire bonding	Wire bonding connection Wire lead	Wire bonding deviation Off-center wire bonding Damage under wire bonding contact Disconnection Loose wire Contact between wires	Open circuit Short circuit Increased resistance	Figure 3.4 Figure 3.5

Failure Factors		Failure Mechanisms	Failure Modes	Example
Sealing	Resin Sealing gas	Void No resin filling Water penetration Peeling Surface contamination Insufficient airtightness Impure sealing gas Particles	Open circuit Short circuit Increased leakage current	Figures 3.6 and 3.7 Figure 3.8
Input/output pin	Static electricity Surge Over voltage Over current	Diffusion junction breakdown Oxide film damage Metallization defect/destruction	Open circuit Short circuit Increased leakage current	Figure 3.9
Others	Alpha particles High electric-field Noise	Electron-hole pair generation Surface inversion	Soft error Increased leakage current	

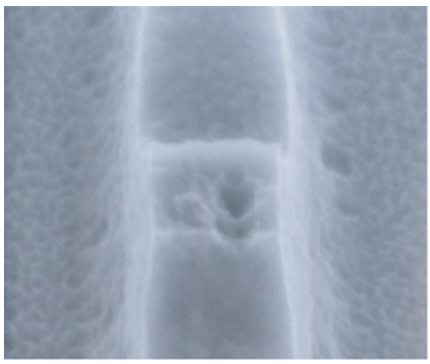


Figure 3.1 Gate Pinhole

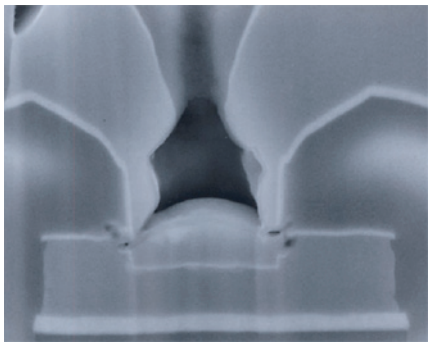


Figure 3.2 Al Wiring Coverage Disconnection

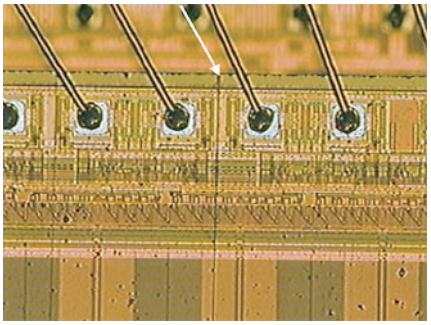


Figure 3.3 Crack

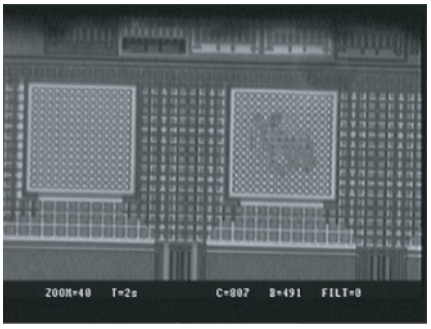


Figure 3.4 Damage under Bonding (Bottom View)

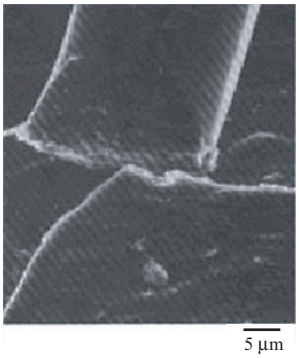


Figure 3.5 Damage on Wire Due to Ultrasonic Fatigue

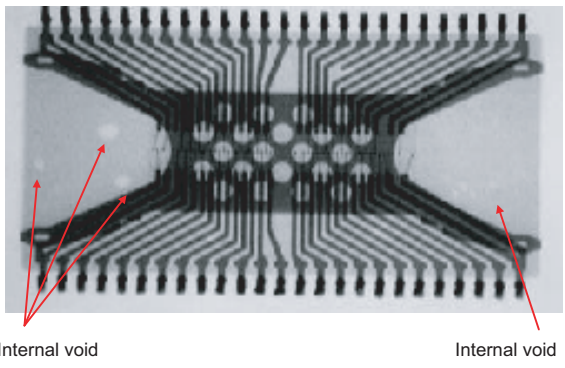


Figure 3.6 Internal Voids in Package

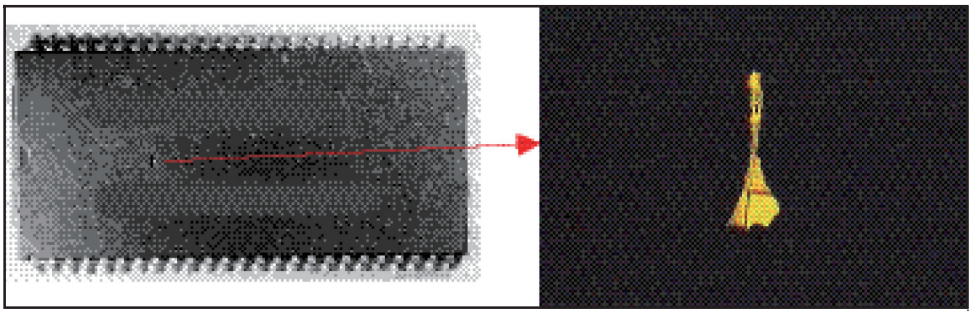


Figure 3.7 No Molding Resin Injected

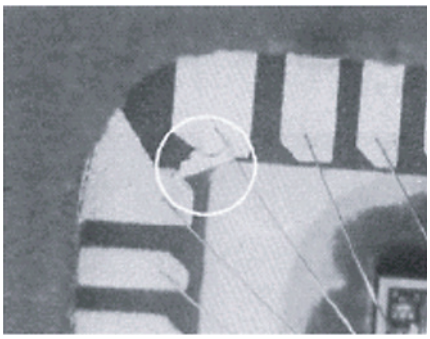


Figure 3.8 Short Circuit Due to Conductive Particles in Package

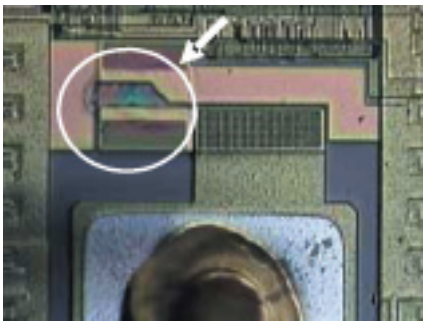


Figure 3.9 Terminal Breakdown Due to Overvoltage

3.2 Failure Mechanisms Related to the Wafer Process

3.2.1 Time Dependent Dielectric Breakdown [1] [2]

As the degree of integration increases, MOS gate oxide films become thinner. Supply voltages have also decreased, but the trend of miniaturization and improvement in performance resulted in higher electric fields across gate oxide films. Electric field intensity increases in sub-micron processes. Therefore, oxide film reliability becomes ever more important.

Good quality thermal oxide films have dielectric breakdown strength of 10 MV/cm or more. However, oxide film failure over time even in lower electric-field intensity (conditions of practical use) is a major cause of failure. Destruction occurring over time is called TDDB (time dependent dielectric breakdown). The time-dependent destruction of the oxide film (dielectric film) is one of major causes of failure.

(1) Failure Phenomena

Because stressing an actual product under accelerating conditions to evaluate its TDDB phenomena is difficult, a specially designed TEG (test element group) is used for this purpose.

Figures 3.10 and 3.11 show the results of a TDDB evaluation. The time-to-failure decreases with increased electric field or temperature.

Empirically, the following equation is often used as the TDDB failure model equation:

$$MTTF = A \times \exp(-\beta E) \times \exp(Ea/kT) \quad (3\text{-}2\text{-}1)$$

where

MTTF: Mean time to failure (h)
A: Constant
Ea: Activation energy (eV)
E: Electric field intensity (MV/cm)
ß: Electric field intensity coefficient (cm/MV)
k: Boltzmann constant
T: Absolute temperature (K)

For TDDB acceleration, it has been reported that, in reality, the less the electric field, the higher the activation energy (Ea), as shown in Figure 3.12.[3] [4]

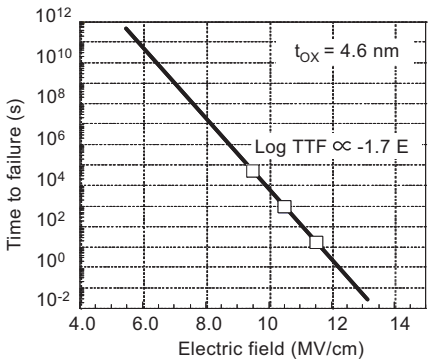


Figure 3.10 Electric Field Dependency of TDDB

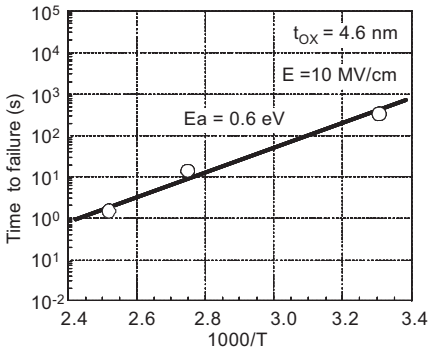


Figure 3.11 Temperature Dependency of TDDB

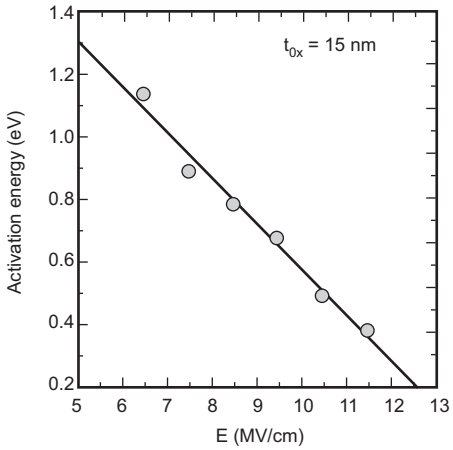


Figure 3.12 Electric-Field Dependency of Activation Energy [4]

(2) Failure Mechanism

Although a variety of models have been examined for the TDDB failure mechanism, recently the percolation model has gained favor as the qualitative mechanism.

Traps are generated in the oxide film by thermal and voltage stress. Current that passes though these traps due to hopping or tunneling can be measured as SILC (stress induced leakage current). It is thought that if the number of these traps increases and the gate electrode connects to the Si substrate, a large current can flow and the gate oxide film can be destroyed. (Figure 3.13[5])

Because the level of the traps (i.e. defect) in an oxide film strongly influences TDDB, it is necessary to characterize the oxide film quality with accelerated tests and feed the results into design rules. From the standpoint of the process, it is important to use SiO_2 film, which does not easily produce defects, and to develop a method of forming an oxide film thereby.

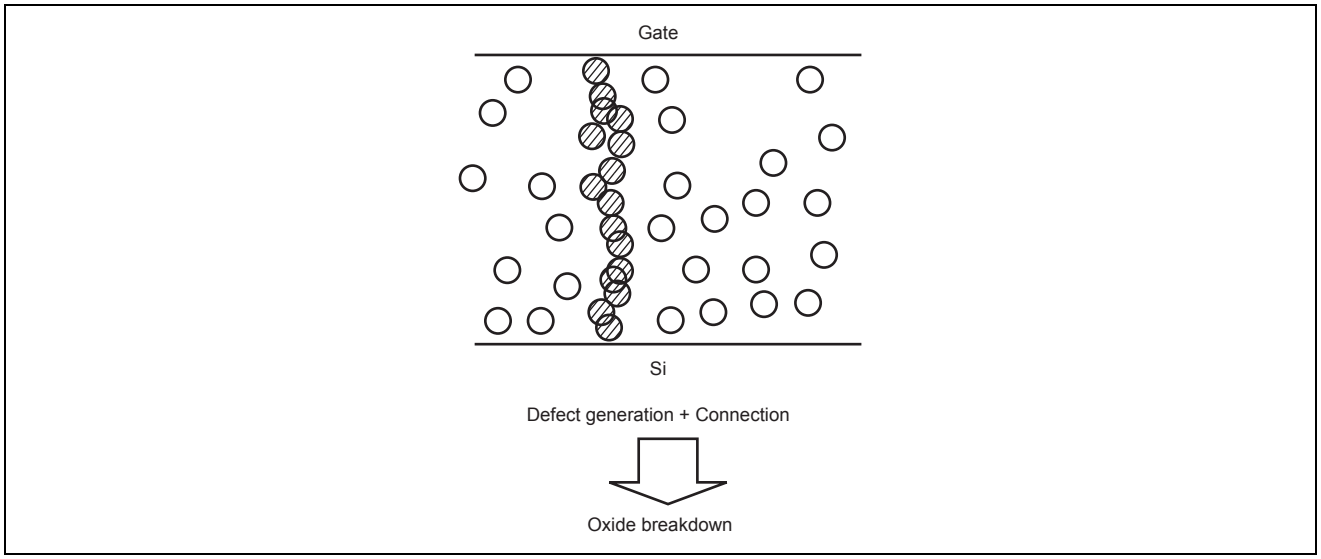


Figure 3.13 Dielectric Breakdown Mechanism [5]

3.2.2 Hot Carrier

While the integration density in semiconductor devices is increasing due to advances in microfabrication technology, it is also becoming more difficult to reduce voltages proportionally to those advances due to requirements from the systems side and due to the resultant reduced internal signal levels.

In MOS FET devices especially, the field strength near the drain increases and the hot carrier phenomenon occurs. Carriers (electrons or holes) that flow into this high-field region are accelerated by the field and acquire high energies. Some of these become “hot carriers”, which have a high enough energy to exceed the potential barrier that exists between the substrate and the gate oxide film. If the hot carriers injected into the gate oxide film are trapped in the film, they form a space charge, and, over time, degrade the characteristics of the MOS FET device, such as the threshold voltage (V_{th}) and the transconductance (gm). Also, any hot carriers injected here that are not trapped become gate current and can be measured as carrier substrate current that flows in the direction of the substrate.

Following are the typical mechanisms of hot carrier injection. Figure 3.14 illustrates two major mechanisms: drain avalanche hot carrier injection and channel hot electron injection.

(a) Drain avalanche hot carrier (DAHC) injection [6] [7]
(b) Channel hot electron (CHE) injection [8]
(c) Secondary generated hot electron (SGHE) injection [8] [9] [10]
(d) Substrate hot electron (SHE) injection [11]

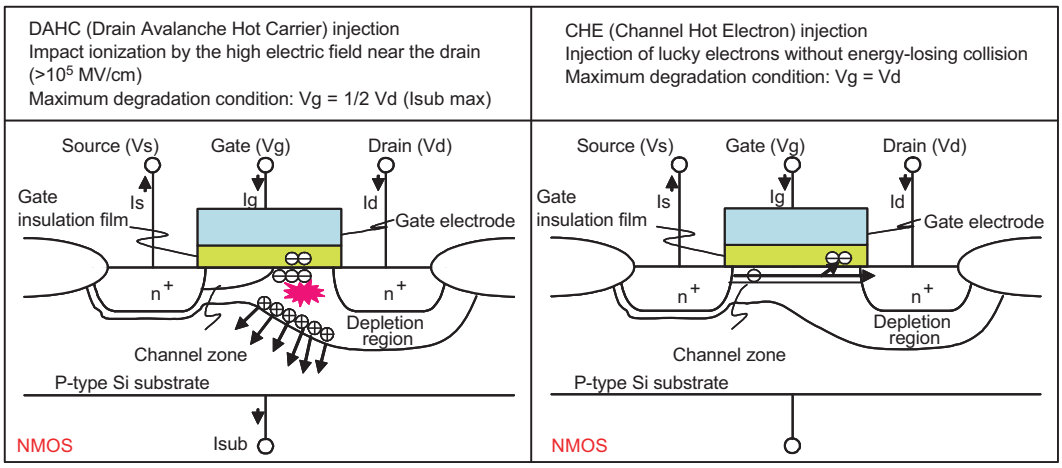


Figure 3.14 Major Mechanisms of Hot Carrier Injection

The hot carrier phenomenon will be explained using DAHC as an example. Assume a sample case in which a high voltage is applied to a MOS FET drain with $V_G<V_D$ (equivalent to the case in which the channel does not extend to the drain edge and the gate voltage is less than the drain voltage), as shown in Figure 3.14.

A high electric field area is formed near the drain when a high voltage is applied to the drain. Electrons flowing out of the source cause impact ionization by the high electric field near the drain and generate electron-hole pairs. Although most of the holes flow towards the substrate and become substrate current, electrons that have acquired a high energy level are injected into the gate oxide film and trapped. This results in a degradation of the characteristics of the MOS FET device, such as the threshold voltage (V_{th}) and the transconductance (gm), and also causes degradation of the product's VCC lower limit operating voltage. As shown in Figure 3.15, the higher the drain voltage, the greater the deterioration.

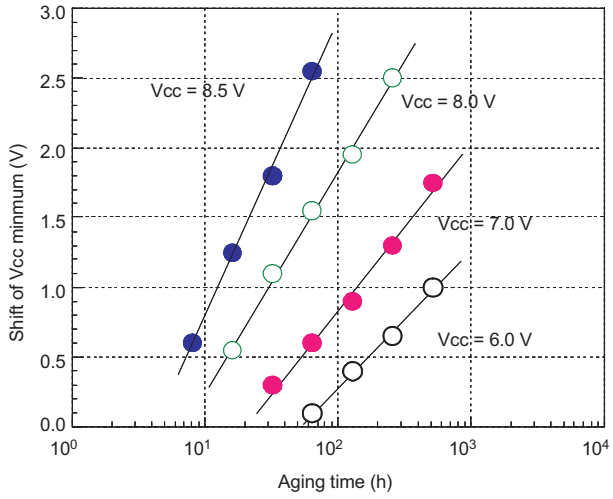


Figure 3.15 Supply Voltage (Drain Voltage) Dependency of Degradation

Typical equations for the life t of the degradation due to the hot carriers are as shown below. Values often reported are 3 or so for m and 100 to 200 for B.

$$t = C \times Isub^{-m} \quad (3\text{-}2\text{-}2)$$

$$t = A \times exp\ (-B/Vds) \quad (3\text{-}2\text{-}3)$$

where

A, B, C, and m: Constants
Isub: Substrate Current
Vds: Drain Voltage

In addition to the factors that influence hot carrier degradation, such as supply voltage and channel length, the ambient temperature and the presence of hydrogen in the protective films must also be considered.

Most semiconductor failure factors accelerate as temperature increases. However, hot carrier degradation tends to increase as temperature decreases. This is thought to be because the electron mean free path is longer and these electrons have even higher energy due to the fact that the probability of collision with Si atoms in the lattice is reduced at low temperatures due to the reduced thermal vibration of the Si atoms. However, due to the reduced power supply voltage in leading-edge devices, the impact ionization mode has changed and thus lower temperatures do not necessarily lead to accelerated degradation. [12] [13]

In advanced LSI chips, MOS FETs with the LDD (Lightly Doped Drain) structure shown in Figure 3.16 have been used as a way to improve hot carrier degradation. This structure can reduce the field concentration at the drain edge of the MOS FET. Furthermore, a variety of design stage measures have been adopted, including increasing the channel length of MOS FETs for circuits with high field strengths and reducing the number of hot carriers generated by optimizing the IC's internal timing.

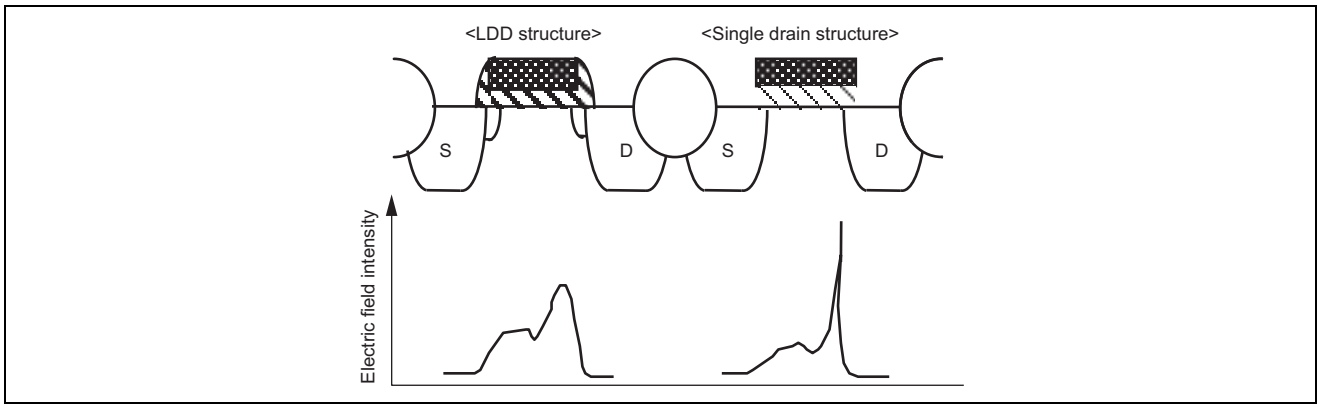


Figure 3.16 LDD Structure

3.2.3 NBTI (Negative Bias Temperature Instability)

Degradation (Ids/Vth shift) occurring due to negative biased BT (bias temperature) stress in P-MOS FETs is called the NBTI phenomenon. This phenomenon has become more obvious as the electric field intensity of internal MOS FETs has increased with the progress of miniaturization. It now counts as an important reliability factor.

(1) Failure Phenomenon

It has been reported that degradation due to the P-MOS FET NBTI phenomenon (Ids/Vth shift) is the result of an increase of the interface state and an increase of the positive charge in the gate oxide film.[14] [15] [16] [17]

The Vth degradation life τ in the NBTI phenomenon has a strong dependence on the gate electric field, and, in general, the following failure model equation is often used:

$$MTTF = A \times exp(-\beta E) \times exp\ (Ea/kT) \quad (3\text{-}2\text{-}4)$$

where

MTTF: Mean time to failure in hours (h)

A: Constant
E: Electric field intensity (MV/cm)
k: Boltzmann constant
Ea: Activation energy (eV)
β: Electric field intensity coefficient (cm/MV)
T: Absolute temperature (K)

In reality, however, the smaller the electric field, the higher the electric field dependence, as shown in Figure 3.17, with the dependence proportional to the exponentiation of the electric field (the power law model).[18] Using β, obtained under a high stress in equation (3-2-4) results in a difficult market forecast.

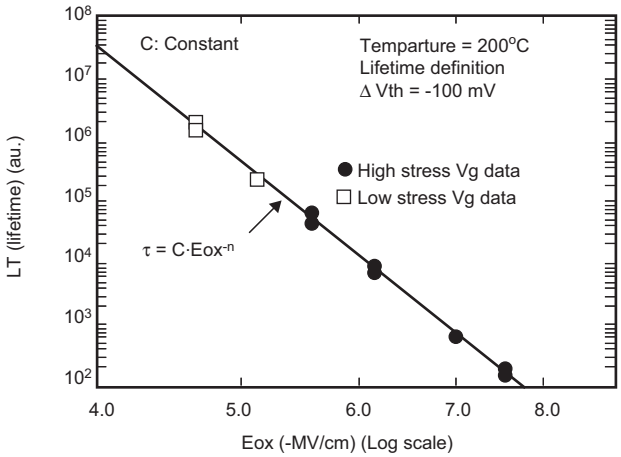


Figure 3.17 Electric field Dependency of Device Life[13]

(2) Failure Mechanism

The mechanism of the P-MOS FET NBTI phenomenon is thought to be as described below.[19]

The Si dangling bond (Si•) on the SiO_2-Si interface is inactivated by hydrogen and exists as Si-H, but stress from a high temperature and a high bias and the existence of holes give rise to an electrochemical-reaction that frees the hydrogen. In this sequence, the Si dangling bond becomes an interface state and the hydrogen diffuses into the oxide film. Some of the diffusing hydrogen in the oxide film joins with defects in the oxide film to form traps. This increase of the interface state and the charge resulting from the traps in the oxide film are considered to be the factors that lead to Ids/Vth degradation.

Recovery from the Ids/Vth degradation caused by the NBTI phenomenon can be accomplished by removing the stress bias and applying a reverse bias.[20] [21] [22]

Accordingly, the NBTI phenomenon is particularly important in circuits in which DC stress is applied.

3.2.4 Electromigration

Most semiconductor integrated circuits use Aluminum (Al) metallization wires for their interconnects. Electromigration is a design concern for semiconductor integrated circuits because Al metallization films have a polycrystalline configuration with many grain boundaries. In addition, advances in function, speed, and processing on the sub-micron level have caused the current density in the Al metallization to increase to as much as 10^4 to 10^5 A/cm^2.

Electromigration is a phenomenon of the movement of metal atom due to the current flow in a metallization wire. In Al metallization wire, Al atoms move in the direction of electron flow. A void occurs near the negative electrode, and an open failure results. Near the positive electrode, hillocks are created, which lead to a short-circuit failure. Figure 3.18 shows a failure mechanism and Figure 3.19 shows a photographic example.

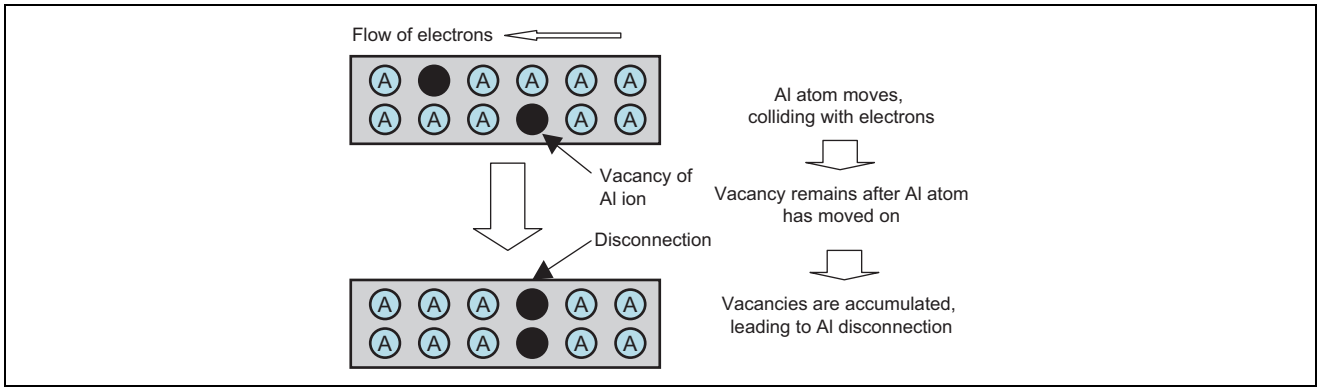


Figure 3.18 Failure Mechanism

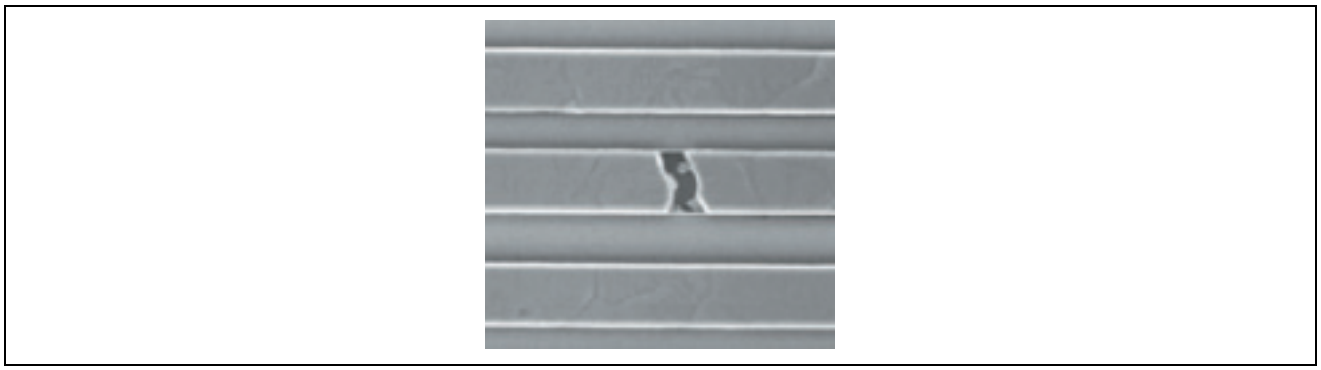


Figure 3.19 Electromigration of Al Wire

Al metallization wire has polycrystalline structure and diffusion of metal atoms is of three different types: lattice, grain boundary, and surface diffusion. See Figure 3.20. In polycrystalline films there are many grain boundaries with possible defects and the metal atoms move easily on grain boundaries. Therefore, grain boundary diffusion is a primary factor of the electromigration in Al metallization wire. The thinner the films are, the greater the ratio of surface to volume of the conductor becomes, thus increasing the importance of surface diffusion.

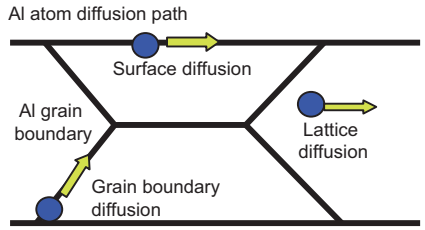


Figure 3.20 Lattice Diffusion, Grain Boundary Diffusion, and Surface Diffusion of Polycrystalline Al

The electromigration failure model equation is expressed (3-2-5) as

$$MTTF = A \times J^{-n} \times exp\ (Ea/kT) \quad (3\text{-}2\text{-}5)$$

MTTF: Mean Time to Failure (h)

A: Constant Determined by Metallization Material and Structure
J: Current density (A/cm²)
n: Constant (n = 2: refer to J. R. Black [23] [24])
Ea: Activation Energy (eV)
k: Boltzmann Constant
T: Absolute Temperature of Metallization (K)

The Ea value of temperature 0.6 to 1.0 eV has been confirmed.[25] [26] [27]

Tolerance of electromigration, which has seemed to have reached the limits of miniaturization, is being improved by laminating layers of refractory metals like tungsten (W) and titanium (Ti) as barrier metals on the lower layer or upper layer, or on both layers of Al wiring, adding Cu to Al wiring (suppression of grain boundary diffusion), and using tungsten plugs or the like in via-holes.

3.2.5 Stress Migration

Stress migration is the phenomenon in which metal atoms migrate in the presence of thermal stress alone, with no electric current applied.[28] [29] Stress migration is caused by stress that occurs from a difference of the thermal expansion coefficients between the passivation film or interlayer dielectric film and Al wiring. Figure 3.21 shows the mechanism. The passivation film on the wiring causes tensile stress on the wiring, resulting in the movement of A1 atoms, the formation of voids, and eventually a disconnection. The lower the temperature, the greater the stress; the higher the temperature, the easier it is for the metal atoms to move. Consequently, long-term storage at a moderate temperature between 150°C to 200°C results in stress migration. This mode is referred to as the low-temperature long-term mode, which usually creates a slit-shaped disconnection. The thinner the wiring width, the more frequently the phenomenon occurs.[30] [31] There is also a high-temperature short-term mode that causes a wedge-shaped void in the heating process in semiconductor device production. Figures 3.22 and 3.23 show failure examples.

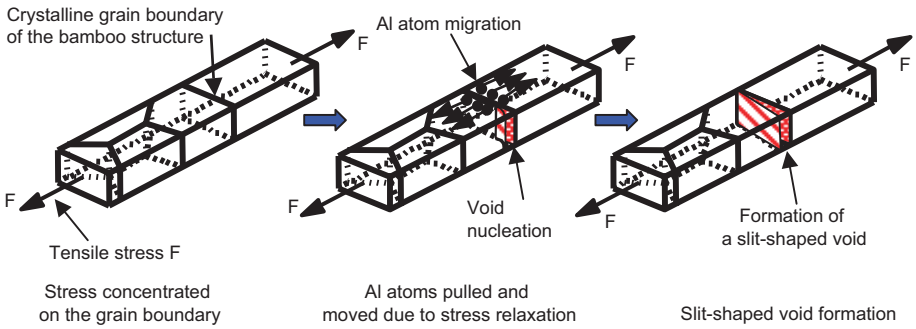


Figure 3.21 Mechanism of Slit-Shaped Void Formation

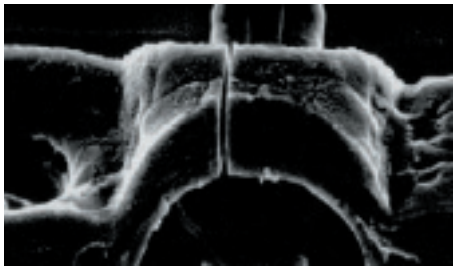


Figure 3.22 Slit-Shaped Void

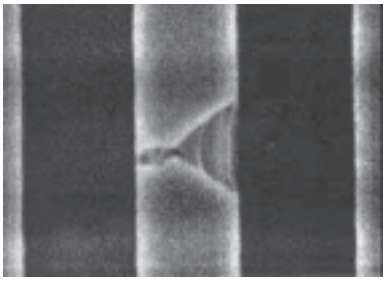


Figure 3.23 Wedge-Shaped Void

As with electromigration, stress migration tolerance is improving by the application of barrier metals, the addition of Cu to Al wiring (suppression of grain boundary diffusion), and the use tungsten plugs or the like for via-holes.

3.2.6 Soft Error

(1) Soft Error Caused by Alpha Particles

One of the problems which hinder development of larger memory sizes or the miniaturization of memory cells is the occurrence of soft errors that cause temporary malfunction due to alpha particles. This phenomenon was first described by T. C. May.[32]

U (uranium) and Th (thorium) are contained in very low concentrations in package and wiring materials and emit alpha particles that inverse memory data. When alpha particles impinge on the memory chip, a large concentration of electron-hole pairs is generated in the silicon substrate and these electron-hole pairs are separated by the electric filed as shown in Figure 3.24. If a PN-junction is present close to this place, the electrons move to the N-layer and the holes move to the P-layer. Finally, the memory information is reversed and a malfunction occurs. This error is not a permanent breakdown but recovered to normal operation by writing again.

The generated holes are pulled towards the substrate to which a negative potential is applied. Conversely, electrons are pulled to the data storage node to which a positive potential is applied. A dynamic RAM filled with charge has a data

value of 0. An empty or discharged cell has a value of 1. Therefore, a data change of 1 → 0 occurs when electrons are accumulated in the data storage node. Such a malfunction is called the “memory cell model” of a soft error.

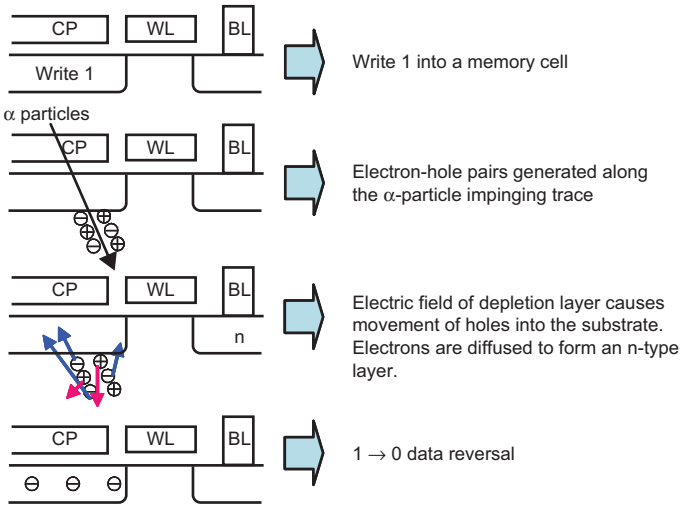


Figure 3.24 Incorrect Operation in Memory Cell

The “bit line model” occurs due to a change of the bit line electric potential.

The bit line’s electric potential varies with the data of the memory cell during readout, and is compared with the reference potential, resulting in a data value of 1 or 0. A sense amplifier is used to amplify the minute amount of change.

If α-particles impinge on the area near the bit line during the extremely short time between memory read-out and sense amplification, the bit line potential changes. An information 1 → 0 operation error results when the bit line potential falls below the reference potential. Conversely, if the reference potential side drops, an information 0 → 1 operation error results.

The memory cell model applies only to information 1 → 0 reversal, while the bit line model covers both information 1 → 0 and 0 → 1 reversals. The generation rate of the memory cell model is independent of memory cycle time because memory cell data turns over. Since the bit line model describes problems that occur only when the bit line is active at data read-out, increased frequency of data read-out increases the potential for soft errors, i.e. the bit line model occurrence rate is inversely proportional to the cycle time.

(2) Soft Error Evaluation Methods

Evaluating soft errors due to α-particles is an important element of memory reliability.

Field tests using actual memory devices are the best source for evaluating memory soft error failure rates, but they require large sample sizes and long monitoring times. Specifically, a minimum of 20,000 hours and a sample size of 500 are required to evaluate the soft error rate of a product with a reliability performance of several hundred FITs.

For that reason, soft error rates are evaluated with two methods. One is the field test with a representative product for a manufacturing process. The other is accelerated test method with an α-particle source for quick evaluation. Figure 3.25 shows a test system. An α-particle source is placed over the test chip and evaluated.

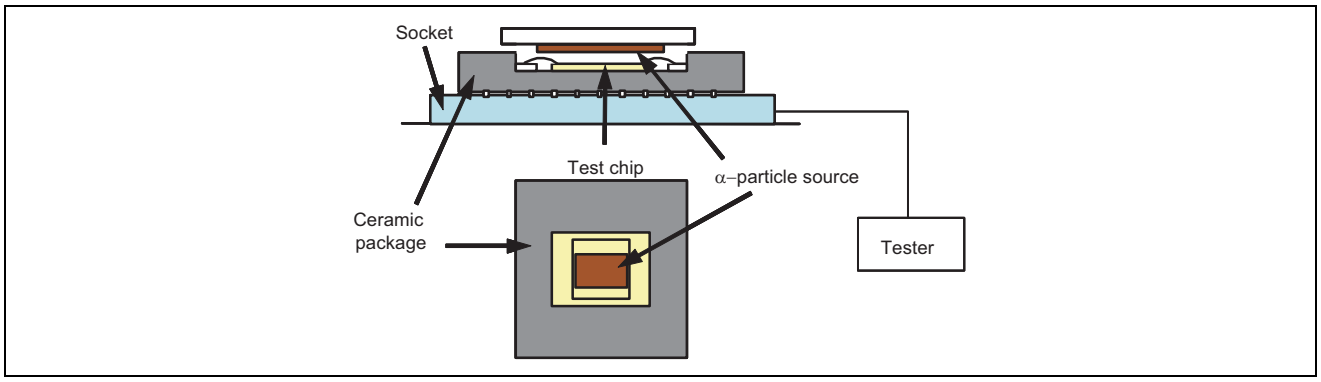


Figure 3.25 Accelerated Soft Error Evaluation System

(3) Countermeasures for Soft Errors

Methods for reducing memory soft errors due to α-particles include:

1. Reduction of α-particles emitted from the highly pure materials for a package or wiring
2. Coating the chip surface with a material to block α-particle radiation from the package material
3. Reduction of the memory device's sensitivity to α-particles

The objective is to reduce α-particle emission, so chip coat technology is becoming indispensable in large memory sizes. In order to prevent radiation from the package material from reaching the chip, the chip surface is coated with a material that does not contain radioactive elements such as U or Th.

Renesas uses a polyimide coating as a countermeasure to α-particles. Figure 3.26 shows the effectiveness of polyimide film for prevention of soft errors. The failure rate decreases as polyimide film thickness increases.

In addition, the amount of accumulated charges that are used as memory cell data should sufficiently be assured to improve the resistivity to α-particles.

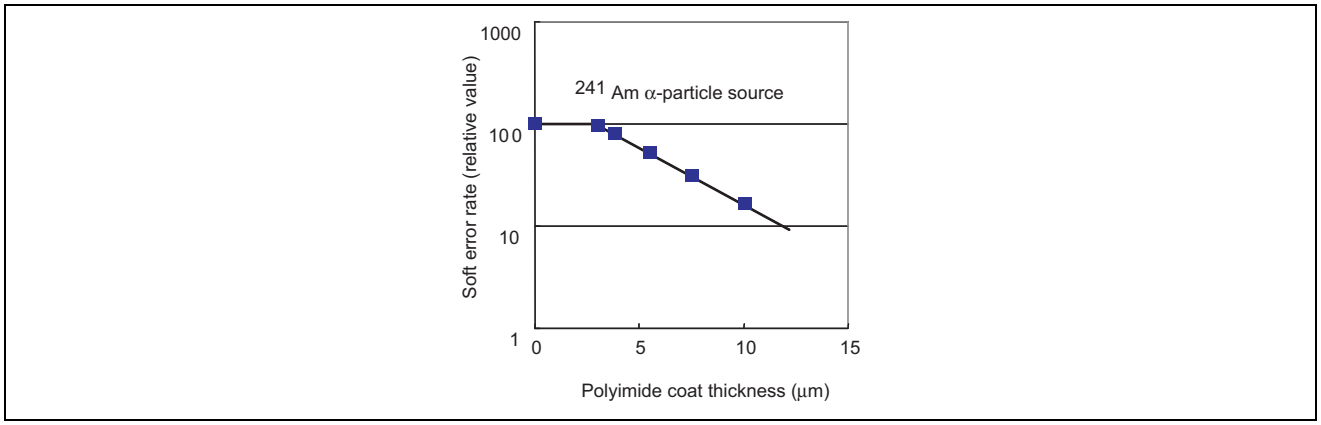


Figure 3.26 Soft Error Prevention Effect of Polyimide Coating

The main point of strengthening memory devices against α-particles is to maintain sufficient charge per bit.

However, the area occupied by one memory cell decreases as memory capacity increases, so it becomes ever more difficult to maintain sufficient charge per bit.

New memory cell configurations with trench and/or stack structures and improved dielectric films, instead of oxide films, are being used to maintain the charge and reduce sensitivity to α-particles.

More recently, other cosmic rays (mainly neutrons) and their effects on memory devices have become a matter of concern due to device miniaturization and low-voltage operation.[33] Evaluation methods for soft errors have been published in various standards, including JEDEC (JESD89) and JEITA (EDR-4705).

3.2.7 Reliability of Non-Volatile Memory

Non-volatile memories retain their data mainly by accumulating electrons in a floating gate within the memory cell, such as stack-type gate memory of Figure 3.27, or by accumulating electrons/holes in an MNOS/MONOS gate, such as MNOS-type gate memory of Figure 3.28.

In recent years, FRAM with the polarization characteristics of ferroelectric materials, phase-change memory, and magnetic memory (MRAM) have been developed as non-volatile memories of the next generation.

The principle of programming into flash memory (stack type gate) is described in the next paragraph. Generally electron injection into the floating gate of a flash memory is accomplished by supplying high voltages to the drain (V_D) and control gate (V_G), while the source is at ground potential (Figure 3.27). Electrons flowing from the source gain sufficient energy in the high electric-field area near the drain to generate electron-hole pairs by impact ionization.

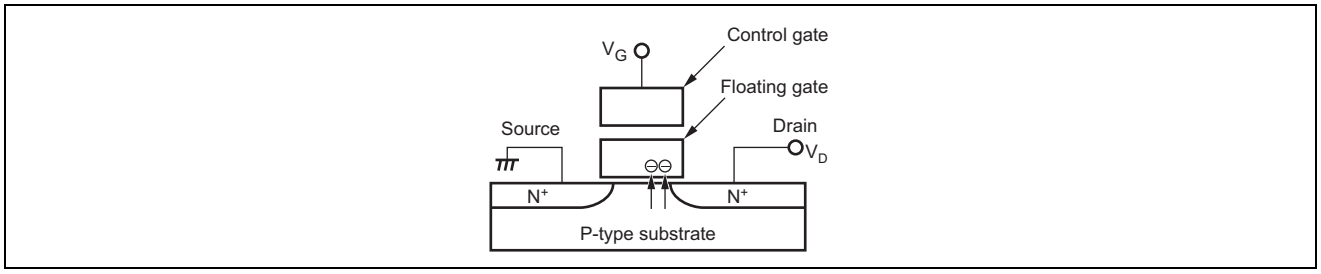


Figure 3.27 Stack Type Memory Cell Cross-section

The generated electrons are injected into the floating gate due to the high voltage on the control gate. Since the floating gate is insulated from its surroundings, the electrons become isolated.

The condition under which electrons were injected (program) is defined as data 0. A data 1 condition exists when electrons are not injected (erase).

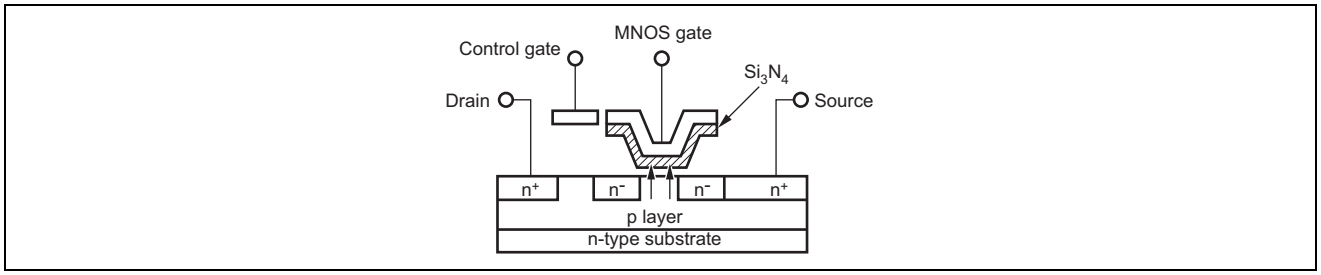


Figure 3.28 MNOS Memory Cell Cross-section

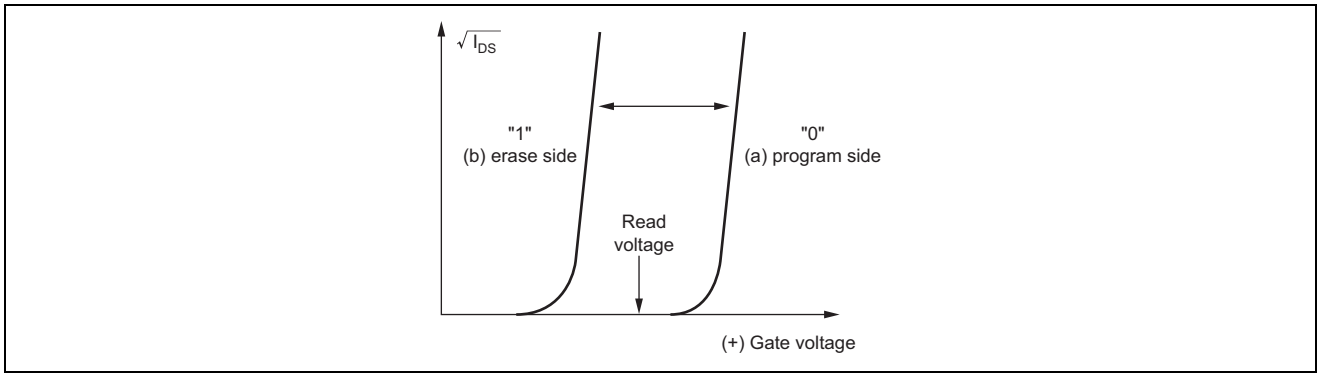


Figure 3.29 Stack-Type Memory Cell Vth Change

The program and erase conditions are shown with relation to memory threshold value (V_{th}) in Figure 3.29. The threshold voltage V_{th} of a memory cell is high for programmed state, and low for the erased state.

(1) Data Retention Characteristics

Programming to stack-type gate memory is accomplished with hot electrons (or FN tunneling).

Although the ability to retain the programmed condition (electrons isolated in the floating gate) for long periods of time is expected, there is a finite probability that electrons stimulated by heat will be lost because the programmed condition is essentially non-equilibrium. Electrons isolated in the floating gate gain sufficient thermal energy to overcome the energy barrier of the surrounding oxide film. Consequently, the higher the energy barrier between the floating gate and the surrounding oxide film, the better the ability of the cell to retain data.

The thermionic excitation model expresses the loss of electrons from the floating gate due to thermal excitation (3-2-6):

$$V_{CC}(t)/V_{CC}(0) = N(t)/N(0) = exp\ [-v \bullet t \bullet exp\ (-Ea/kT)] \quad (3\text{-}2\text{-}6)$$

where

V_{CC}: Maximum operating voltage
N: Amount of charge on the floating gate
v: Relaxation frequency (10^{12} cycles per second)
Ea: Activation energy (eV)
k: Boltzmann constant
T: Absolute temperature (K)

The time in this data retention model has a strong correlation with temperature. In general, the Ea (activation energy) related to data retention characteristics is estimated to be 1 eV or greater.

(2) Failure Mechanisms

If there are defects near the floating gate, the memory may not be able to retain data as mentioned above and a failure may occur due to charge loss or gain within a relatively short time period.

Causes of degradation in data retention characteristic can be divided into four broad categories:

1. Charge loss/gain due to an initial defect in the oxide film
2. Data retention degradation due to ionic contamination
3. Data retention degradation due to excessive electrical stress
4. Data retention degradation due to stress from too many program/erase cycles

A defect (leakage path, particles, etc.) within the gate oxide film (Figure 3.30) leads to gain or loss of charge because electrons are attracted from the substrate to the floating gate when a bias voltage is applied to the control gate.

If the defect is in the interlayer film, (Figure 3.31), no failure occurs in the erased state, but failure is possible in the programmed state due to the loss of electrons from the floating gate through the defect.

Failure for both modes can occur in a short time at high temperatures. It is possible to eliminate initial data retention failures by the use of high-temperature baking (screening) at the manufacturing process.

Loss of electrons from the floating gate can also be caused by ionic contamination in the oxide film. The high-temperature baking (data 1 and 0 mixed pattern) is an effective screen for this failure mode also.

Another type of data retention degradation occurs in stack-type gate memory.

During each program/erase cycle, high-energy electrons or holes pass through the oxide film. If this program/erase cycle is repeated often enough (typically 1,000 times or more), it is probable that electrons or holes will become trapped in the oxide film, reducing the difference between the threshold values of the 1 and 0 states. This causes an intrinsic degradation of data retention characteristics.

Furthermore, because the difference between the threshold values is reduced as the number of program/erase cycles increases, there is a natural limit on the number of program/erase cycles performed for stack-type gate memory. Accordingly, it is more effective for better reliability if program counts are suppressed during use.

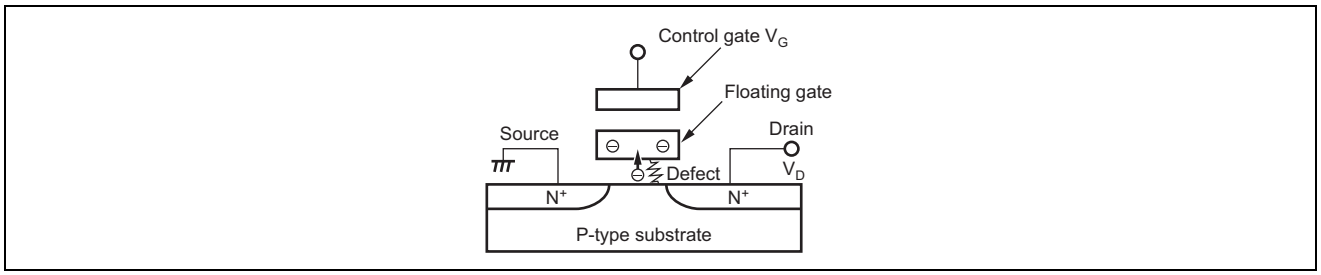


Figure 3.30 Gate Oxide Defect Mode (Charge Gain)

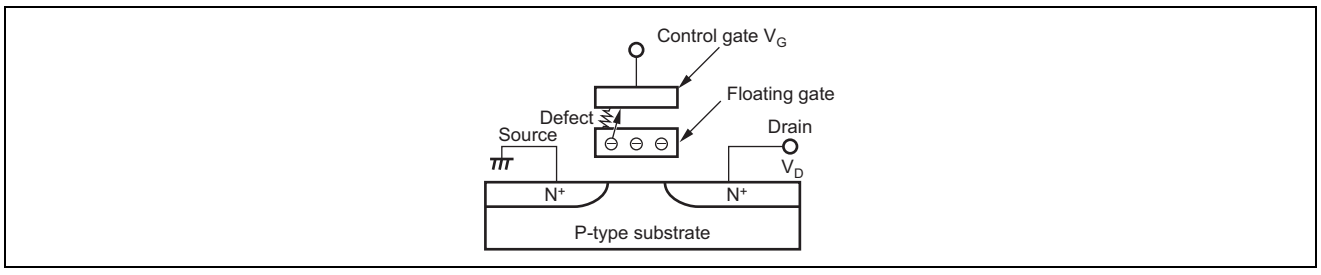


Figure 3.31 Interlayer Film Defect Mode (Charge Loss)

3.3 Failure Mechanisms Related to the Assembly Process

3.3.1 Wire Bonding Reliability (Au-Al Joint Reliability)

(1) Introduction

To assemble a semiconductor device, a semiconductor chip is first die bonded on the die pad of a package, and then a surface electrode (Al pad) of the semiconductor chip and an inner lead (Ag or Au plated) of the package are bonded and connected with each other by using a fine metal wire (Au or Al). In the past, most of the semiconductor failures were attributed to the wire bonding process; however, recent technological progress in wire bonding is remarkable, with improvement in accuracy of the manufacturing equipment and automation of the manufacturing processes dramatically increasing the reliability of wire bonding.

Automated wire bonding removes dispersion in quality by worker, reducing the initial joint failures during manufacturing significantly. It is known, however, that in the joint made of an Au-Al binary system, the formation of an intermetallic compound causes a structurally unavoidable long-term life degradation phenomenon to occur; the intermetallic compound is generally known as purple plague.

This section explains the reliability of wire bonding in relation with the progress of diffusion of the Au-Al alloy.

(2) Theory

In the Au wire method, the joint between the Al electrode on a semiconductor chip and the Au wire forms an Au-Al joint. For such an Au-Al joint, it is known that long-term storage of a semiconductor device at a high temperature causes the contact resistance of the joint to increase, eventually resulting in breaks in the joint. Many instances of such failures have been reported because the breaks have led to fatal failures in the equipment in which a joint has been used.

In an Au-Al alloy joint, it is known that several intermetallic compounds are formed, as shown in Figure 3.32. Table 3.2 shows the characteristics of intermetallic compounds, Au, and Al.

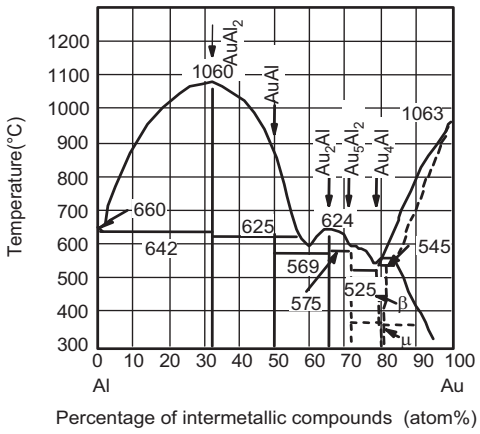


Figure 3.32 Phase Diagram for Au-Al Alloy

Table 3.2 Au-Al Alloy Characteristics

Chemical Compound	Crystal Structure	Expansion Coefficient	Hardness (Hv)	Color
Al	f.c.c.	2.3×10^{-5}	20 to 50	Silver
$AuAl_2$	CaF_2 structure	0.94×10^{-5}	263	Purple
AuAl	ZnS structure	1.20×10^{-5}	249	Gray
Au_2Al	Unknown	1.26×10^{-5}	130	Yellowish golden
Au_5Al_2	γ-brass structure	1.40×10^{-5}	271	Ditto
Au_4Al	β-Mn structure	1.20×10^{-5}	334	Ditto
Au	f.c.c.	1.42×10^{-5}	60 to 90	Gold

(3) Failure Mechanism

The following are considered to be causes that lead to degradation of Au-Al alloy joints:

- Several intermetallic compounds are produced in the diffusion layer as a result of the Au-Al diffusion; the difference in the expansion coefficient between the Au_5Al_2 and the Au_4Al layer causes the joint strength to lower;
- The difference in the diffusion coefficient between Au and Al causes voids to be produced around the joint (Kirkendall effect); this in turn weakens the joint strength; and
- The Au_4Al alloy layer is turned into a high resistance layer by the oxidization taking place with the bromine (Br), contained in the flame retardant in the resin material, as the catalyst

The diffusion processes are described below by using Figure 3.33:

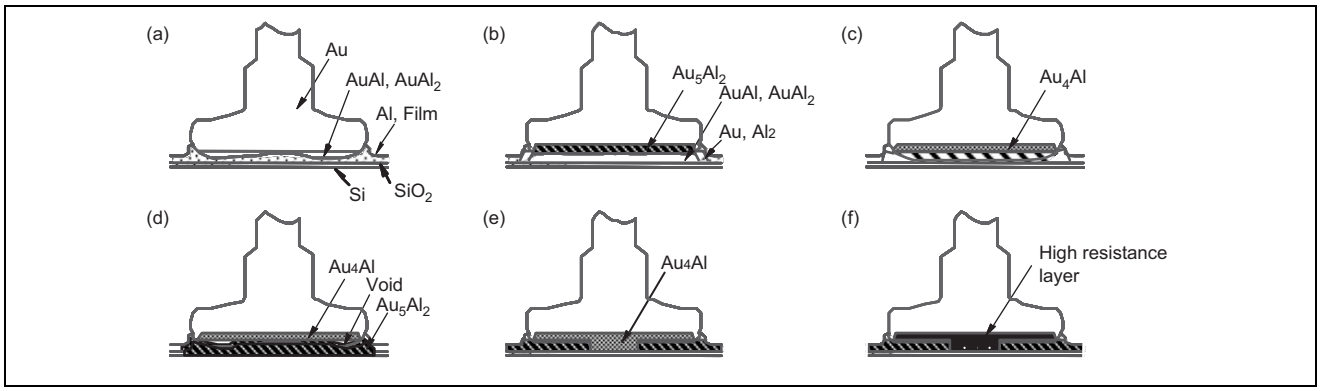


Figure 3.33 Au-Al Alloy State Chart

(a) At the early stage of bonding, a thin diffusion layer is formed between the Au portion and the Al film; the diffusion layer is purple-colored and estimated to consist of $AuAl_2$;

(b) Further heating causes the Au-Al diffusion to proceed, with Au diffusing into the Al thin film and thereby causing the pure Al layer to disappear. At the same time, an alloy layer distinguishable from the Au-Al alloy is formed on the Au ball side; this is estimated to consist of Au_5Al_2;

(c) The layer resulting from diffusion does not exceed a certain thickness; this is thought to be due to the limited supply of Al and the difference of the diffusion velocity between the direction toward Au and that toward Al. With D denoting the diffusion velocity, the following relation exists: $D_{Au \rightarrow Al} > D_{Al \rightarrow Au}$. With the initial thickness of Al evaporated film assumed to be 1 μm, the total thickness of the diffusion-formed portion is about 4-5 μm. Further heating causes Au to diffuse into the diffusion layer to form Au_4Al on the Au ball side, which grows into the semiconductor chip side;

(d) Further heating causes the Au diffusion into the diffusion layer to proceed and thereby the entire diffusion layer to be formed of Au_5Al_2 and Au_4Al. In addition, voids are created around the diffusion layer as a result of the Kirkendall effect caused by the difference in the diffusion velocity between $D_{Au \rightarrow Al}$ and $D_{Al \rightarrow Au}$.

(e) With the heating still continued, the Au diffusion into the diffusion layer is intensified except where voids are created, leading to formation of an Au_4Al layer in the central portion.

(f) With resin molded IC's, it is known that Br contained in flame retardant agents in resin materials acts as a catalyst to oxidize Al in the Au_4Al layer. Br penetrates from voids into the joint and oxidizes Al in the Au_4Al layer, causing a high resistance layer to be formed at the interface between the center of the Au ball and the alloy layer; this leads to a disconnection failure ($Au_4Al+3Br \rightarrow 4Au+AlBr_3$). Figure 3.34 shows the section of a joint under such condition.

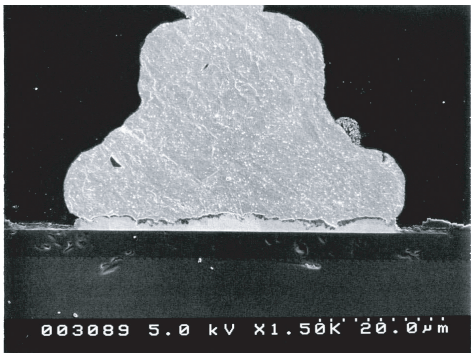


Figure 3.34 Cross-section of Au-ball Joint (SEM Image)

The following Arrhenius equation holds between the thickness X of the diffusion layer, the storage temperature T, and the storage time t:

$$X^2=D \cdot t,\ D=D_0 \cdot exp\ (-Ea/kT) \qquad (3\text{-}3\text{-}1)$$

where

D: Diffusion coefficient
Ea: Activation energy (eV)
D_0: Frequency factor
k: Boltzmann's constant
T: Storage temperature (K)

The following three points must be taken into consideration to improve the reliability of the Au ball bonding:

1. An initial bonding joint should be processed in a time as short as possible and at a temperature as low as possible to minimize the Au-Al mutual diffusion;
2. Mechanical shocks should be avoided where possible during the bonding process and prior to the resin sealing; and
3. After package sealing, heating an element should be avoided where possible.

(4) Summary

The Au-Al wire bonding is subject to structural life limits imposed by the alloy used. To improve the reliability of bonding, it is more important and effective that the control of manufacturing equipment and selection of materials be properly conducted to secure the initial joint properties and that unnecessary heating on semiconductor devices after the bonding process be avoided.

3.3.2 Ag Ion Migration

(1) Introduction

Ag ion migration is a phenomenon in which metal ions move under an electrochemical effect. It is referred to as electrochemical migration (in this section, “ion migration”) in order to distinguish it from the electro/stress migration that takes place in Al wiring on semiconductor chips. Ion migration can occur with electrode materials other than Ag, such as Cu, solder materials, and Au, if conditions are adverse. However, since it is Ag and Cu that trigger the migration most easily, these tend to pose problems.

This section describes Ag ion migration.

(2) Phenomenon

When Ag, in the form of foil, plating, or paste, is subjected to a voltage under high humidity and temperature, the electrolytic action causes Ag to migrate and grow like an ink blot or dendrite on the surface of the insulator as is shown in Figure 3.35. This may cause the electrical insulation resistance between the electrodes to decrease or be short-circuited.

In a typical case of migration, the ink blot growth starts in the anode side while the dendritic crystal growth starts in the cathode side. In reality, however, due to the effects of difference in the types of insulator, environmental conditions, and the like, the Ag ions eluted from the anode side may be reduced halfway to precipitate as metallic Ag and the material precipitated from the cathode side may grow not dendritically but in blot. Furthermore, because Ag reacts easily with sulfur (S) and chlorine (Cl) in the atmosphere, these elements are simultaneously detected on analysis by the EPMA or other means in many cases.

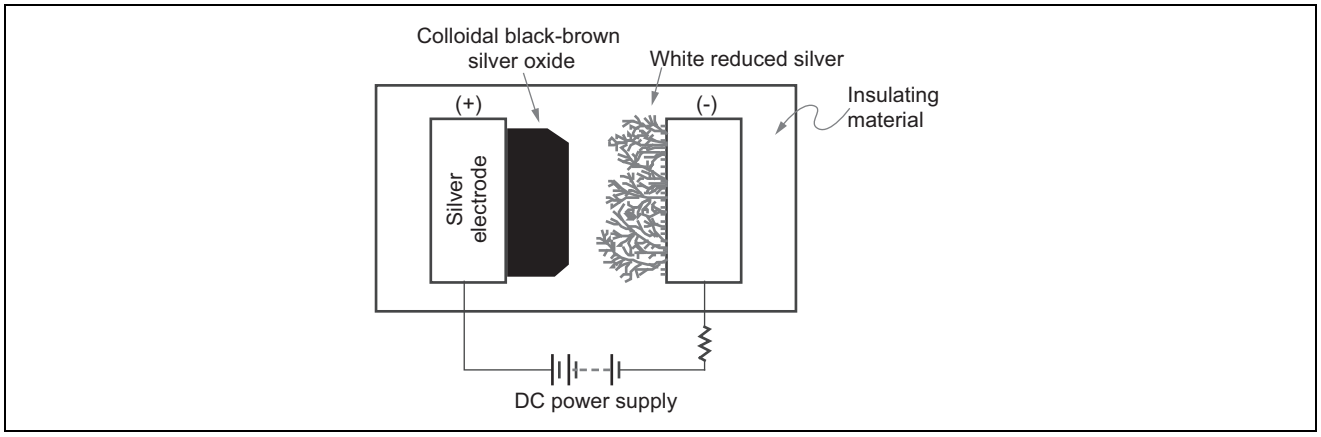


Figure 3.35 Generation of Silver Ion Migration

(3) Generation Mechanism

Initially, when moisture settles between Ag electrodes under voltage application, the chemical reaction given by Equation 3-3-2 takes place on the anode:

$$Ag+OH^- \rightarrow AgOH+e^- \quad (3\text{-}3\text{-}2)$$

Since the silver hydroxide (AgOH) generated in this reaction is very instable, the decomposition as given by Equation 3-3-3 takes place:

$$2AgOH \rightarrow Ag_2O+H_2O \quad (3\text{-}3\text{-}3)$$

The colloidal silver oxide (Ag_2O) generated in turn reacts as given by Equation 3-3-4:

$$Ag_2O+H_2O \Leftrightarrow 2AgOH \Leftrightarrow 2Ag^+ + 2OH^- \quad (3\text{-}3\text{-}4)$$

The colloidal Ag_2O generated and the Ag ions move slowly (Ag ions, in particular, are pulled by the electric field), until they reach the cathode to be reduced there to silver metal:

$$Ag^{+}+e^{-} \rightarrow Ag \quad (3\text{-}3\text{-}5)$$

The silver precipitated exhibits white dendritic growth as shown in Figure 3.35. The electric-field intensity at the tip of a dendrite increases with the growth; therefore, the growth, once initiated, proceeds with acceleration.

(4) Acceleration Factors and Countermeasures

Listed below are the factors that accelerate the occurrence of ion migration. These factors must be studied if they are to be addressed, and those having greatest influence must be removed.

(a) Potential Difference and Electrode Distance

As a type of electrolytic reaction, ion migration poses problems only when DC voltage is applied between electrodes. In addition, the time to short-circuit between electrodes is roughly inversely proportional to the potential difference and proportional to the distance.

(b) Temperature

Although temperature is less of a factor than humidity, a higher temperature accelerates the chemical reaction and hence the migration of ions.

(c) Humidity (Specifically, Condensation)

Humidity greatly affects ion migration. In general, ions do not migrate when the relative humidity is 50% or less, but when the relative humidity is 70% or more, migration accelerates rapidly.

(d) Types of Insulating Material

Like moisture, the properties of insulation materials greatly affect ion migration. In general, ion migration occurs in highly hygroscopic phenolic resin laminated materials and nylon materials, but does not often occur in poorly hygroscopic materials such as glass epoxy substrates.

(e) Dust and Water Properties

Because dust, in addition to being a retainer of moisture, also itself contains water-soluble matter, it accelerates ion migration. A higher concentration of electrolytes in water also accelerates ion migration.

(5) Summary

Measures against Ag migration should be examined and put into practice in consideration of the working conditions (the environment and voltage, in particular), the scope of the areas affected, and the quality requirements to reduce its potential. Some of the measures already known or reported include reduction of ionic impurities, control of the amount of Pd in Ag, and the addition of ion traps.

3.3.3 Al Sliding

(1) Introduction

In a temperature cycle environment, failure phenomenon due to a shear force directed towards the center of the chip. These phenomena, of which Al sliding is one, are due to the contraction stress of the mold resin at a low temperature. Metallic wiring materials such as Al are deformed easily by an external force and do not tolerate external stresses. If a horizontal stress is applied to the center of the chip surface and to the wiring around it, it is not the Al wiring that withstands the stress, but the passivation film on the surface. Therefore, when the Al wiring is wide, a protective film with structurally low strength is destroyed and the Al wiring slides. This failure phenomenon is known as Al sliding and causes cracks in the passivation film. These cracks can lead to circuit damage and subsequently device malfunction. This section describes the Al sliding phenomenon caused by a stress from the mold resin.[34]

(2) Phenomenon

Because the semiconductor chip, passivation film, and molding resin have different coefficients of thermal expansion, external thermal stress causes stress to occur between the different layers. When a chip is stored at a lower temperature, the contraction stress from the resin acts on the chip, causing the Al wiring to slide toward the center of the chip. In the chip corner in particular, where the stress on the chip coming from the resin becomes large, the Al sliding phenomenon is more remarkable than at the center of the chip. Furthermore, this phenomenon is more remarkable on a wide Al conductor on which stress is concentrated. The Al sliding and the cracks in the passivation film are closely related. Because Al wiring deforms easily, if a stress from the resin due to a temperature change is put on the passivation film, causing cracks on the passivation film, the Al wiring deforms and can no longer be restored to its original state (elastic deformation). As a result, the Al sliding phenomenon takes place. Figure 3.36 shows an example of Al sliding. Figure 3.37 shows the failure mechanism. This phenomenon is accelerated by the temperature cycle test.

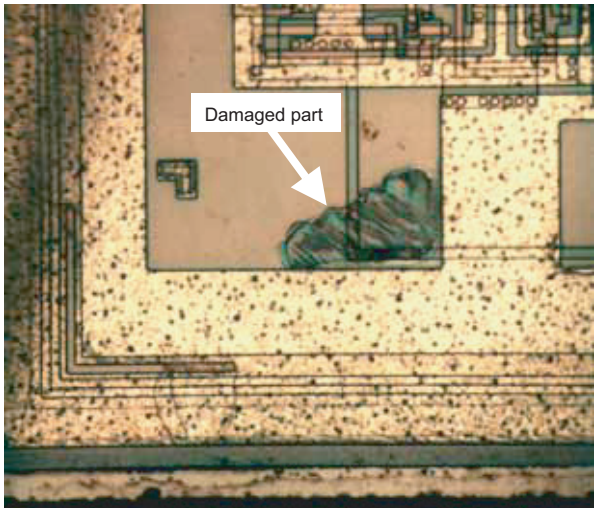


Figure 3.36 Example of Al Sliding

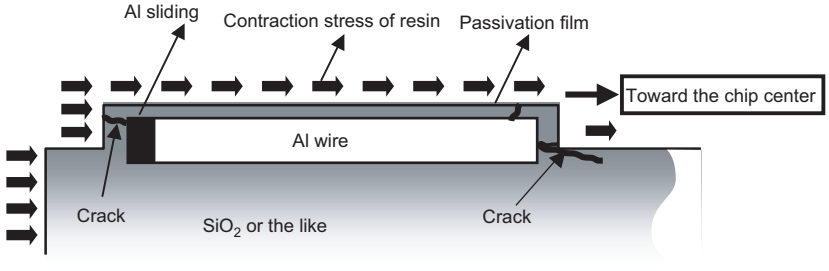


Figure 3.37 Chip Corner Al Wiring Cross Section

(3) Failure Mechanism

Since Al sliding is affected only by a temperature change, its failure model is based on the Eyring model equation.

$$\text{Life (L)} \propto (\Delta T)^{-n} \qquad (3\text{-}3\text{-}6)$$

For the acceleration coefficient n, n = 4.4 to 8.1 has been reported.[35]

(4) Summary

The Al sliding phenomenon is caused by the difference in the coefficient of thermal expansion between materials forming a semiconductor device, giving rise to passivation cracks from the resulting stress. The following methods can be used to address these problems:

1. Set the coefficient of thermal expansion of the mold resin as close as possible to that of the chip.
2. Set a limit on the Al wire width at the chip corners to prevent wide Al wires from being placed there.

3.3.4 Mechanism of Filler-Induced Failure

(1) Introduction

Mold resins include a filler that secures strength and has a thermal expansion coefficient close to that of the chip. When a filler of approximately 100 μm is located on the chip surface by molding, the filler presses the chip surface due to the temperature cycle and other factors, damaging the chip surface and possibly causing a failure.

(2) Phenomenon

When a mold resin includes large and pointed filler elements, and if the filler elements contact the surface of the chip during molding at a high temperature (while the mold resin is melting), the filler elements cannot damage the chip.

Thereafter, the resin around the filler shrinks gradually as it hardens. If the tip of a pointed filler element is facing the chip surface, as shown in Figure 3.38, the pointed tip moves (is displaced) closer to the chip surface as the resin shrinks. Thereafter, when the temperature falls, the resin shrinks more (the coefficient of thermal expansion of the resin is several times larger than that of the filler). Moreover, when the temperature drops in the temperature cycle, the resin shrinks more and the pointed tip of the filler element is pressed out over the chip surface. If the amount of displacement exceeds the thickness of the protective layer on the chip surface, the circuits on the chip surface are damaged and fail. Because the amount of displacement of a filler element tip correlates with the size of the filler element, the smaller the filler element, the less the displacement. Filler elements with a round tip can never be displaced by breaking through the resin. To avoid this problem, it is usually effective to make large filler elements round and to remove filler elements that exceed a certain size.

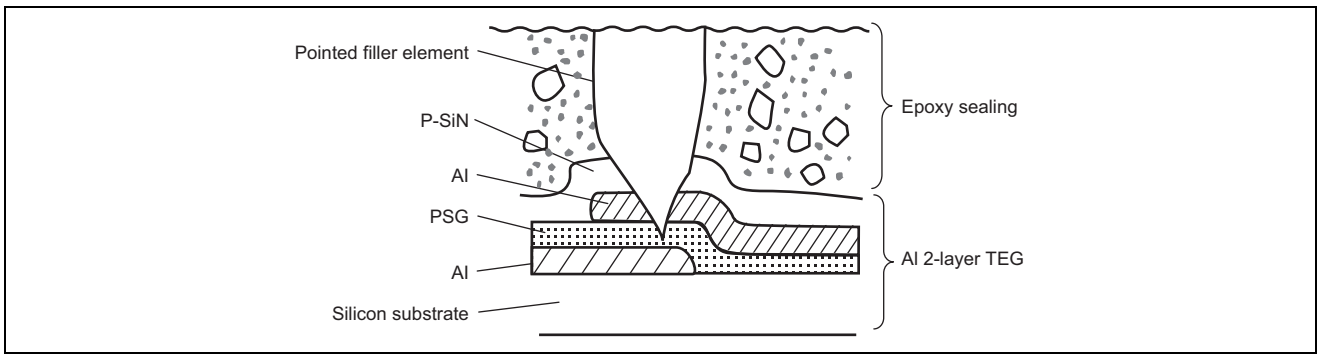


Figure 3.38 Cross Section of a Semiconductor Device in the Vicinity of the Chip Surface

(3) Summary

Failures arising from the filler have the potential of occurring in resin mold semiconductor devices. To cope with this problem, it is important to mitigate the stress which semiconductor chips undergo by implementing the measures described above.

3.3.5 Whiskers

Use of lead-free solders for mounting electronic components on boards has increased due to environmental considerations. From the standpoint of plating reliability, however, since Pb provides a significant benefit related to tin whiskers, a Pb-free policy requires that measures be taken for tin whiskers that satisfy values, conditions, and other factors existing in the marketplace. Although the mechanism of tin whisker generation has not been clearly determined yet, it has been demonstrated experimentally that the environmental factors in accelerated whisker growth (see Figure 3.39) are temperature, humidity, and stress. The most popular whisker generation mechanism is the one described below.

When the lead base material is Sn-plated Cu, Cu diffusion grows two kinds of intermetallic compounds: Cu_6Sn_5 and Cu_3Sn. At room temperature, Cu_6Sn_5, which has a lower density than Cu, is mainly formed and due to the increase in volume, compression stress is applied to the Sn layer. This compression stress causes whiskers to form through the growth of needle-shaped structures in the Sn. In contrast, at higher temperatures, since growth of the higher density Cu_3Sn increases, this compression stress due to increased volume is suppressed.[36]

The following are the principal measures for preventing whiskers:

1. Addition of atoms that can replace Pb (Bi, Cu, Ag, etc.)
2. Thicker plated film
3. Heating after plating
4. Underplating

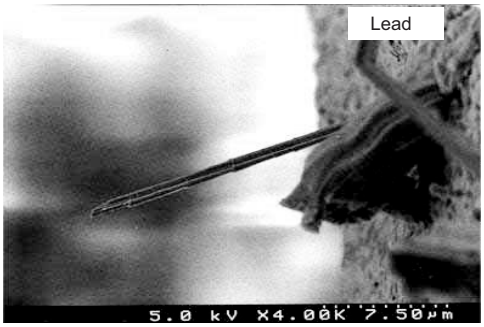


Figure 3.39 Example of Whisker Generation

3.3.6 Moisture Resistance of Resin Mold Semiconductor Devices

(1) Introduction

Semiconductor devices are generally put in resin mold type packages. At an early stage in the development of packages, resin mold devices were subject to such moisture resistance related problems as corrosion of Al electrode wiring corrosion and increased leakage current, but these problems have been largely solved.

This section describes the moisture resistance of a resin mold device in terms of mechanisms of its failures, the acceleration of failures under actual conditions of use, and the effects of bias application.

(2) Failure Mechanism

(a) Water Penetration Path

As described below, two water penetration paths are possible in a resin mold device: one of them passes straightforward through the resin and leads to the chip surface (moisture absorption/permeation of resin, or the moisture diffusion effect). The other is a path from the interface between the resin and leadframe to the chip surface via the interface between the resin and metal wire (Figure 3.40). In the latter case, the moisture becomes a caustic solution containing impurities (such as flux and cleaning fluid) that adhere to the package surface. The solution corrodes the bare Al electrodes and wires on the chip surface.

Reports so far[44] [47] on the relative significance of these two paths indicate that the resin and frame materials used and the package structure affect the relative significance. Recent data shows that a greater role is played by the path passing through the resin than the path passing the frame interface because adhesion between the frame material and the resin has improved.

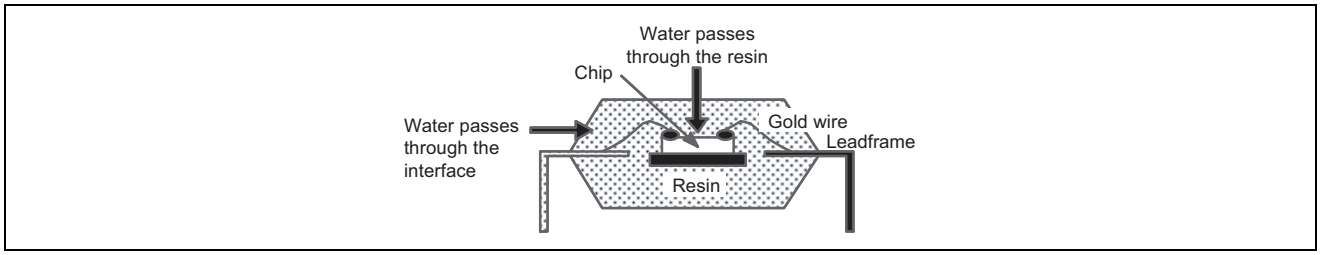


Figure 3.40 Water Penetration Path in a Plastic Mold Device

(b) Al Corrosion

During storage in high-humidity and high-temperature conditions, moisture that reaches the chip surface may cause corrosion (sometimes referred to as pitting) of Al on the bonding pads and internal wiring patterns exposed by passivation defects with pinholes and cracks. This type of corrosion does not cause a rapid increase in failures even after extended hours of storage, and the cause of any failures found is considered to be an initial defect on package/chip due to fluctuations occurring in production. It has been confirmed that delamination of the adhering interface between the chip surface and the resin sealing or an impurity on the chip surface might result in a similar failure pattern.

The two Al corrosion modes are moth-eaten corrosion and beltlike-shape corrosion, and are shown in Figure 3.41. It is assumed that these corrosion modes are due to the penetration of water containing chlorine and other impurities that has a pH 4 or lower from the Al crystal grain boundary.

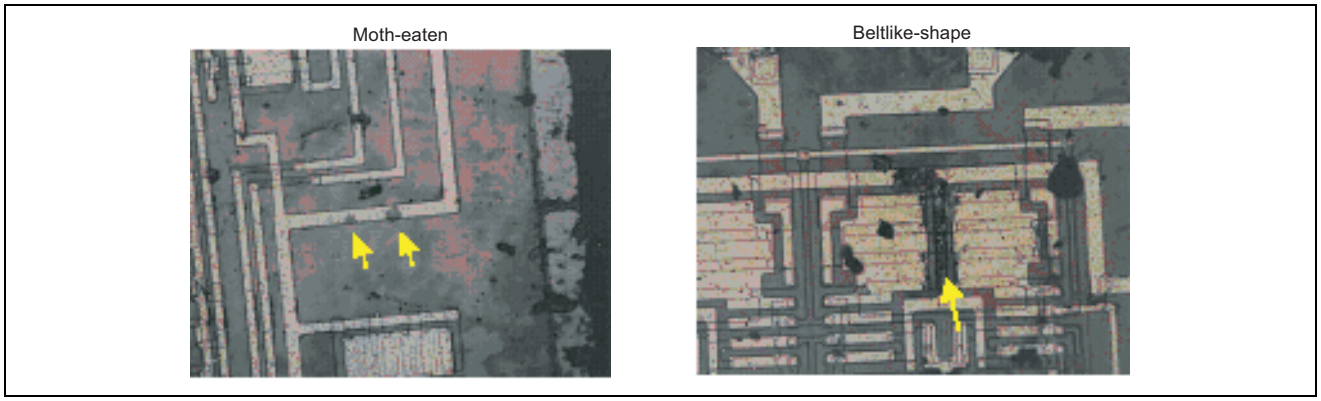


Figure 3.41 Al Corrosion During Storage with High Humidity and High Temperature

Aluminum is chemically a very active metal; left in dry air, it causes alumina (Al_2O_3) to be formed on its surface. Since this Al_2O_3 acts as a surface protection film, the reaction no longer proceeds. In the presence of sufficient water, on the other hand, aluminum hydroxide ($Al(OH)_3$) is formed. The $Al(OH)_3$ thus formed is amphoteric, dissolving both in acids and in alkalis; therefore, it dissolves easily into water containing impurities. The following are typical corrosive reactions involving aluminum [37]:

$$2Al+6HCl \rightarrow 2AlCl_3+3H_2\uparrow$$
$$Al+3Cl^- \Leftrightarrow AlCl_3+3e^-$$
$$AlCl_3+3H_2O \rightarrow Al(OH)_3+3HCl$$
$$2Al+2NaOH+2H_2O \rightarrow 2NaAlO_2+3H_2\uparrow$$
$$Al+3OH^- \rightarrow Al(OH)_3+3e^-$$
$$2Al(OH)_3 \rightarrow Al_2O_3+3H_2O$$
$$2AlO_2^-+2H^+ \rightarrow Al_2O_3+H_2O$$

High temperature and high humidity bias tests induce simultaneous Al corrosion on the anode and cathode sides, often leaving a metallic luster in places on the Al wiring. This corrosion mode consists of Al wiring corrosion (pitting) on the anode side and corrosion on the cathode side that progresses from the crystal grain boundary (intergranular corrosion, or imbricate corrosion). Figure 3.42 shows these two modes of corrosion. Once failure begins by pitting corrosion, almost every device suffers a wear-out failure in a comparatively short time. It has been confirmed that the time to failure correlates with the volume resistivity of the resin to the absorption of moisture. Note that intergranular corrosion (imbricate corrosion) tends to occur on the cathode side. Note that the following reaction formula has been proposed as a model for the formation of grain boundary corrosion at the cathode. [40]

Anode side: $2H_2O \rightarrow 4H^+ + 4e^- + O_2$

Cathode side: $2Al+6H^+ \rightarrow 2Al^{3+}+3H_2$

$$2Al^{3+}+6H_2O \rightarrow Al(OH)_3+6H^+$$
$$6H^++6e^- \rightarrow 3H_2$$

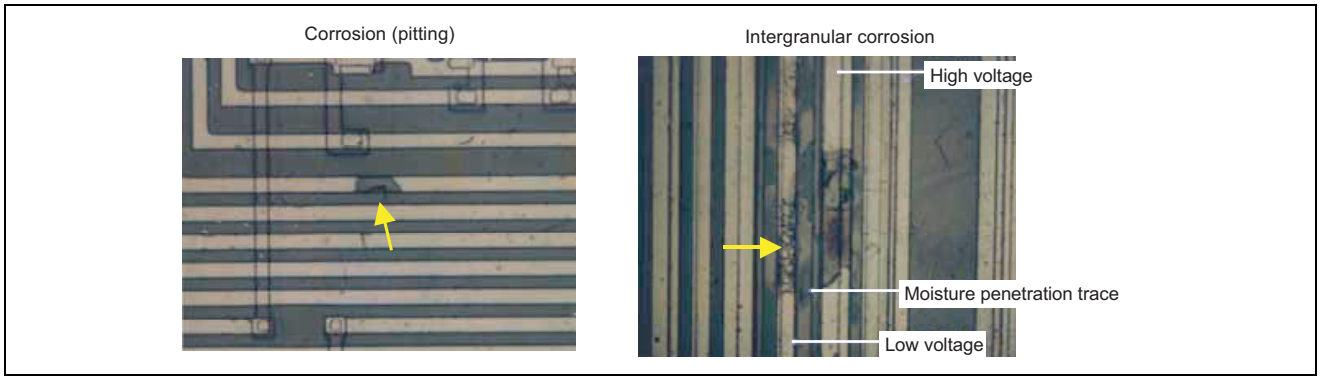


Figure 3.42 Al Corrosion on High Humidity and High Temperature Bias

(c) Chip Surface Leakage Due to Moisture Absorption of The Resin

Chip surface leakage current due to moisture absorption of the resin

- Insulation resistance degradation of resin
- Formation of a water film in the gap between chip surface and the resin

Leakage currents include the following two types: leakage current due to degradation of the resin's insulation resistance due to the absorption of water by the resin and leakage current that occurs when a water film forms in the gap between the chip and the resin surface and there is a potential difference between electrode wiring on the chip surface. In particular, for MOS and other devices that have surface activity, the surface potential can set up an inversion layer on the surface of the Si substrate under the oxide film, causing current to flow between the source and drain of the parasitic MOS FET and thus increasing the leakage current. The mechanism is shown in Figure 3.43.

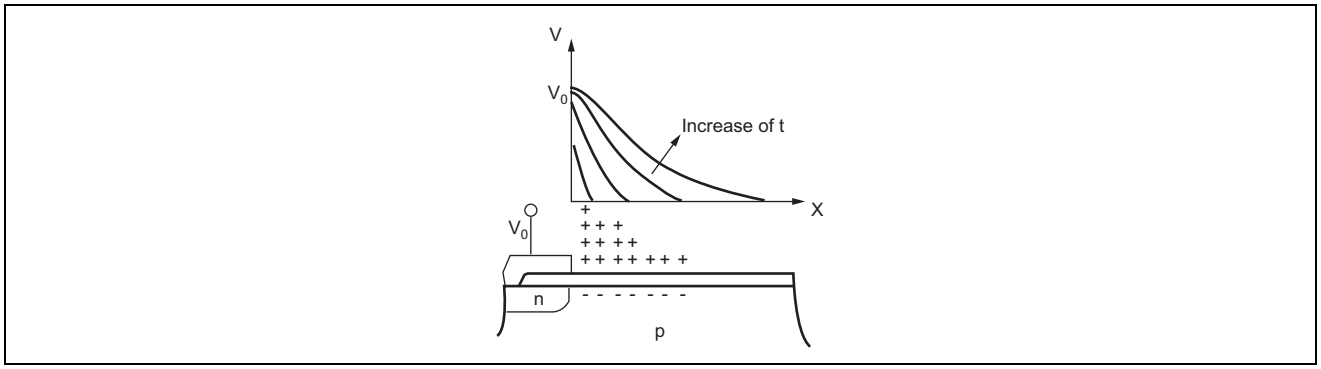


Figure 3.43 Surface Charge Expansion Phenomenon

(3) Conditions for Practical Use and Acceleration

Several acceleration models for predicting the reliability of resin mold semiconductor devices have been introduced on the basis of moisture-resistance test data, as follows:

(a) The mean time to failure, MTTF, is affected separately by the junction temperature Tj (K) and the relative humidity RH (%).[41]

Relationship between MTTF and Tj: Based on Arrhenius model (Ea≈0.8eV).

Relationship between MTTF and RH: The values of logMTTF and logRH are in a linear relation.

These are called relative humidity models and are expressed by the following equation:

$$MTTF \propto exp\,(Ea/kT) \cdot RH^{-n}$$

where k is Boltzmann constant, T is the absolute temperature, and n is a constant between 4 and 6.

(b) The time to a given cumulative failure rate t relates to the vapor pressure V_P.[42] [43] [44] This is called an absolute vapor pressure model and is expressed by the following equation, where m is a constant for which m ≅ 2 is used:

$$t \propto V_P^{-m}$$

Figure 3.44 shows the relationship of relative lifetimes at respective humidity/temperature points as an example of acceleration in a case where m = 2.

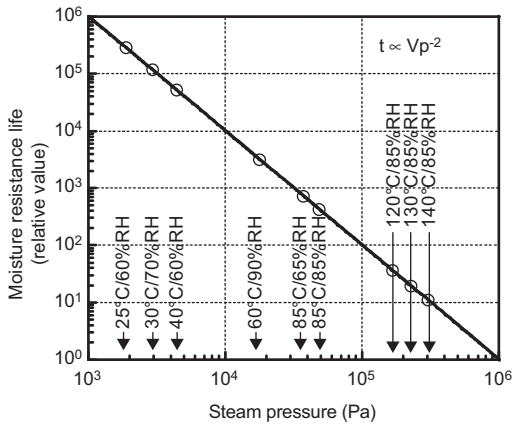


Figure 3.44 Example of Acceleration

Although various acceleration models including those described above have been proposed, the acceleration in each of them depends on the particular resin material, package structure, conditions of metallization and passivation, etc., which makes it difficult to determine a generalized acceleration coefficient.

(4) Methods for Evaluating the Moisture Resistance

Since various methods for evaluating the moisture resistance are available, the appropriate method for the intended purpose has been used. Table 3.3 shows the major test methods. The methods generally used are the pressure cooker storage test, the pressure cooker bias test (primarily for the unsaturated condition, sometimes called HAST (Highly Accelerated Temperature and Humidity Stress Test)), the high temperature and high humidity storage test, the high temperature and high humidity bias test, and, very rarely, varying combinations of these tests.

Furthermore, in response to widespread use of surface mount devices (SMD), an evaluation method has been proposed in which the moisture resistance tests listed above are preceded by a pretreatment consisting of a sequence of moisture absorption and thermal stress tests. When SMDs are mounted on a circuit board, an IR reflow or other method is used. This type of mounting method results in heat stress to the entire device as well as delamination of the leadframe interface to the resin or the adhesive interface between the chip surface and mold resin. The result is degradation of the moisture resistance life. To check the SMD moisture resistance level, an evaluation method in which moisture absorption and heat stress tests are performed as a preprocess has been used.

Table 3.3 Major Methods for Evaluating the Moisture Resistance

Evaluation Method	Example of Test Conditions	Features
High temperature and high humidity storage test	85°C/85%RH	Has substantial correlation with actual conditions of use. Requires a long time for the evaluation.
High temperature and high humidity bias test	85°C/85%RH/ with bias applied	Has substantial correlation with actual conditions of use. Requires a long time for the evaluation.
Pressure cooker storage test	130°C/85%RH 121°C/100%RH	Has substantial correlation with actual conditions of use.
Pressure cooker bias test (HAST)	110°C/85%RH/ with bias applied 120°C/85%RH/ with bias applied 130°C/85%RH/ with bias applied	Has substantial correlation with actual conditions of use. Allows the effects of the biasing to be evaluated.

(5) Summary

Various acceleration tests have been used to check the moisture resistance of resin mold devices under conditions of practical use. Recently, moisture resistance levels have improved so remarkably that they are sufficient for practical use without any critical problems.

3.4 Failure Mechanisms Related to the Mounting Process and During Practical Use

3.4.1 Cracks of the Surface-Mounted Packages in Reflow or Flow Soldering

(1) Introduction

As electronic devices become thinner, smaller, lighter, and multi-functional, surface-mounting techniques have become essential techniques for increasing the density of mounted parts. Most semiconductors now use surface-mount packages.

Soldering methods for surface-mounted packages are roughly classified as partial heating and full heating. Partial heating applies heat only to sections to be soldered whereas full heating applies heat to both the printed circuit board and packages. Full heating methods consist of reflow soldering methods and the flow soldering method.[45] [46]

- Reflow soldering methods

  The reflow methods consist of the infrared reflow method, the hot-air reflow method (air reflow method), and a method that combines the infrared reflow method and hot-air reflow method.

  In the infrared reflow method, devices to be mounted are soldered by directing infrared rays over the entire printed circuit board with devices installed. This method is suitable for mass production because separate parts can be soldered at one time. The disadvantage of the infrared reflow method is temperature differences when only infrared sources are used. To address this problem, infrared reflow machines that also use a hot air heater have come into widespread use.

  In the hot air reflow method (air reflow method), solder reflows by the circulation of hot air in a furnace. The advantages of this method are little difference in temperature of printed circuit board and parts and the ability to control the temperature deviation between components within a specified degree.
- Flow soldering method

  The flow soldering method is a low-cost soldering method. The parts to be soldered are temporarily fastened to a printed circuit board with an adhesive, the parts side is turned face down, and the printed circuit board is passed through molten solder (flow solder). However, since the flow soldering method cannot handle certain device sizes or dimensions, it is not suitable for high-density mounting of devices.

These full heating methods apply high temperatures to the packages as well as to the points to be soldered. Because the temperature actually applied exceeds 210°C, the surface mount devices can be subjected to severe stress. The following three reliability problems can therefore arise in the production of surface mount devices:

- Resin cracks in the package
- Lowering of moisture resistance
- Adverse effects on the wire bonding strength

(2) Package Cracks

These cracks arise from the combination of the moisture that the package has absorbed and heat applied during soldering.[47] [48] As shown in Figure 3.45, ambient moisture diffuses into the resin during storage in a warehouse, etc. and moisture reaches to the interfaces such as between resin and die pad. When packages with absorbed moisture pass through the reflow oven and are heated, the resin-die adhesive strength drops, differences in thermal expansion coefficients of the different materials give rise to a shear stress, and microscopic area separation or delamination results. Since the speed of moisture diffusion increases at high temperatures, moisture is forced out of the resin into the delamination, and with a rise in pressure there, the delamination region expands and the molding compound becomes increasingly swollen. The swelling stress is concentrated at the periphery of the die pad and eventually a crack in the resin results. The stress varies greatly with the amount of moisture content in the resin near the rear surface the die pad, the die pad size, and the temperature and heating time.

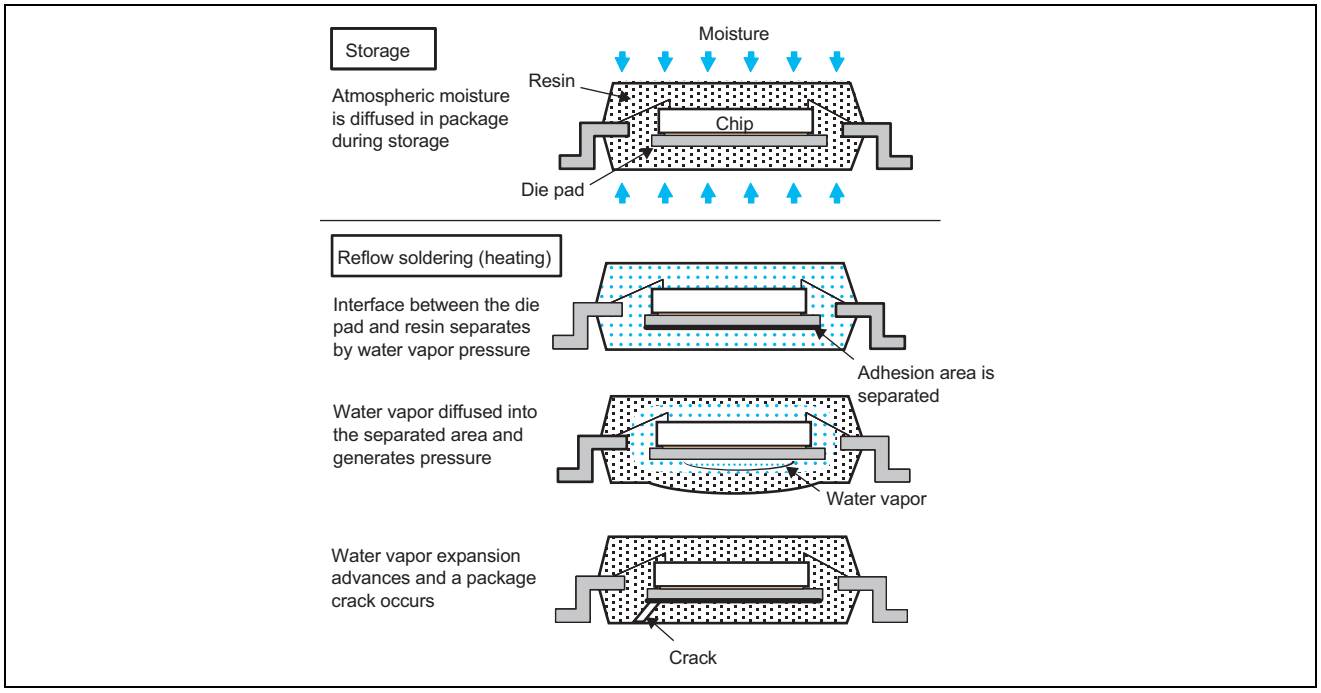


Figure 3.45 Model of Crack Generation in Reflow Soldering [49]

Although the model above shows an example of a crack on the backside of a package, cracks can occur on the front surface of a package due to expansion of the chip surface in the same sequence.

(3) Problems Caused by Package Cracks

Various types of package cracks are considered and are listed in Table 3.4. Quality problems differ, depending on the type of package crack. Package cracks confined to the rear surface occur most frequently. As the swollen unit pushes against the printed circuit board, it is displaced from the optimum assembly location and cannot be soldered correctly. The possibility of degradation of moisture resistivity with rear surface cracks is small, so this type causes the least damage.

Table 3.4 Package Cracking Types and Problems [50]

No.	Package Crack Type	Shape	Problems
1	Package rear-surface crack		Moisture resistivity degradation (least degradation)
2	Package side crack		Moisture resistivity degradation (small degradation)
3	Crack intersecting a bonding wire		Wire damage, open Moisture resistivity degradation
4	Package top-surface crack		Wire damage, open Wire bond peeled off Moisture resistivity degradation

(4) Measures for Improvement in Mounting

As described earlier, handling and storage after fabrication are very important for surface mount devices. However, controlling the environment alone is not sufficient. Because the packages absorb moisture during storage and cracks develop in the resin, the control of the storage time and baking prior to mounting are also necessary. Figure 3.46 shows the dehumidification characteristics of baked packages. As the Figure shows, a baking process at 125°C lasting for 20 to 24 hours results in sufficient dehumidification. The dehumidification at 125°C depends on the resin thickness. Moisture-proof packing for protection from exposure to moisture during transportation and storage period is also effective. In addition, moisture-proof packing has the capability of satisfactorily preventing the external effect shown in Figure 3.47.

In order to ensure quality (reliability), it is important to mount devices at as low a temperature as possible and in as short a time as possible while controlling the moisture absorption in the manner described above.

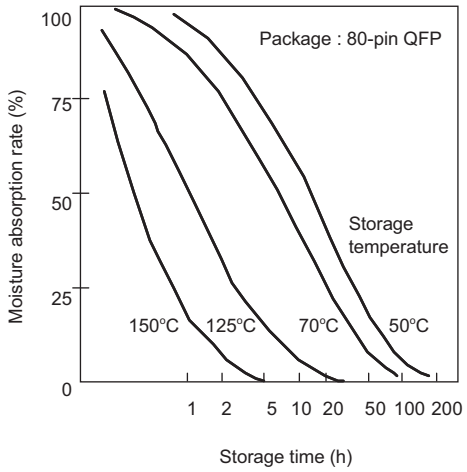


Figure 3.46 Dehumidification of Plastic Packages

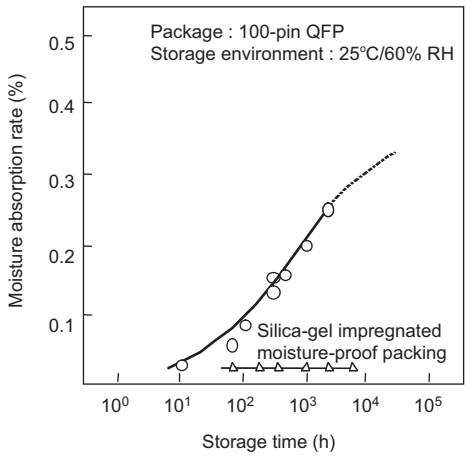


Figure 3.47 Effect of the Moisture-proof Pack

(5) Summary

In ensuring the quality (reliability) of surface mount devices, the following points are very important:

1. Control of moisture absorption of packages (after opening moisture-proof packs); and
2. Minute adjustment of mounting conditions.

To ensure the reliability of all our moisture-sensitive surface mount devices, the stress associated with the mounting process is mitigated by packaging them in moisture-proof packing cases containing a desiccant to protect from moisture. However, the following precautions should be taken:

- To control the temperature and humidity of the place where semiconductor devices are stored and the duration of storage, and to use them within the stipulated time limit.
- After opening the moisture-proof packing, devices should be used promptly within the specified time.
- To mount devices at allowable heat conditions.

3.5 Failure Mechanisms Related to Electrostatic Breakdown, Electrical Overstress Breakdown, Latchup, and Power Devices

3.5.1 Electrostatic Breakdown and Electrical Overstress Breakdown

Semiconductor devices are known for their fine feature sizes. It is because of these fine feature sizes that it is possible to create these high-speed, multifunctional devices. However, because of these fine features, they can be easily destroyed by commonly occurring levels of ESD (electrostatic discharge) or EOS (electrical overstress). Although the main materials, Si and SiO_2, from which these devices are manufactured have superlative resistance to heat and electricity in nature, when devices with fine feature sizes are fabricated, they can be melted or subject to dielectric breakdown if subject to high current levels.

ESD is due to electrical discharge from a charged conductor. Although ESD is a large current with peak levels from a few amperes to a few tens of amperes and a pulse width on the order of a few nanoseconds, it has the feature that although the current is large, the total energy is relatively small. In contrast, EOS refers to all other electrical stresses and thus a wide range of causes are possible. EOS has the feature that although the currents are less than those in ESD, the total energy dissipated is much larger since the pulses are several orders of magnitude longer. Note that long term stresses at the DC level due to, for example, conductive foreign matter or solder bridges on the circuit board, are possible causes for EOS. Figure 3.48 shows the differences between the regions occupied by ESD and EOS.

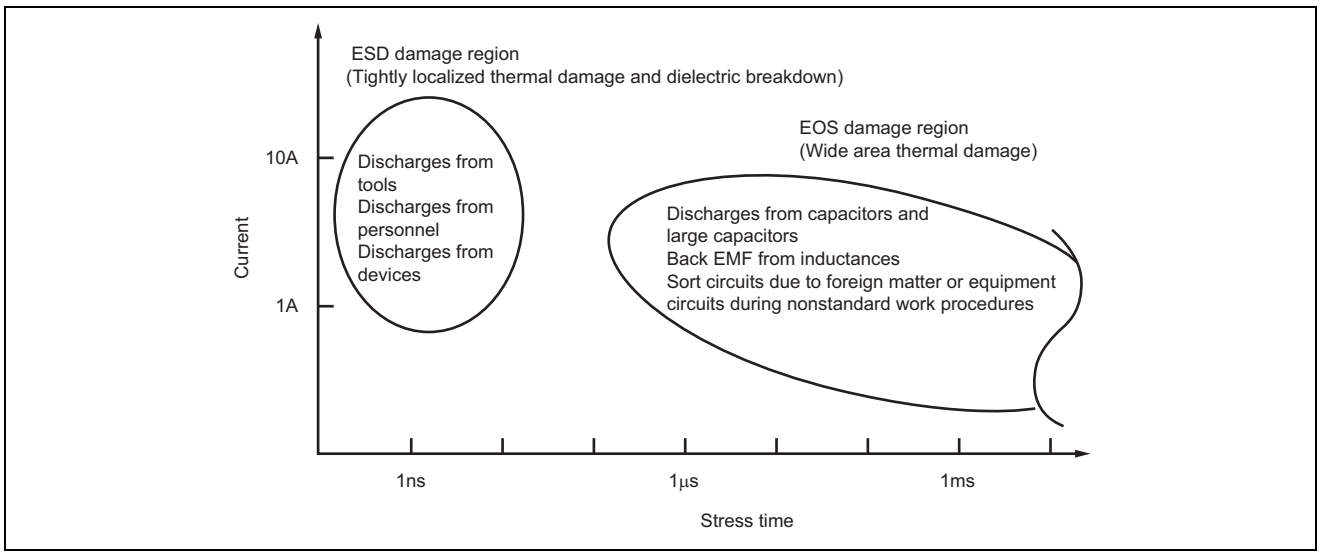


Figure 3.48 Differences Between the ESD and EOS Stress Regions

Since a large current flows momentarily in ESD, the temperature of the heated section rises rapidly and material fusing may occur. However, since the discharge terminates before the heat can be transmitted to the surrounding areas, ESD is observed as damage to small areas. Also, since large currents occur during ESD, high voltages occur within devices and dielectric breakdown also occurs.

In contrast, in EOS, since the currents are smaller and the pulse widths longer than in ESD, the heat is dissipated (transmitted) to surrounding areas and the temperature in the surrounding areas can also rise gradually and reach high temperatures. Thus damage that covers a wide area can occur. When the pulse continues for an extended period, there are cases where electromigration in wiring or deposition of charred resin can be observed. Since the voltage is lower, dielectric breakdown occurs only rarely.

In medium and large-scale ICs formed from parallel circuits with complicated device structures, the location, range, and appearance of the damage due to the same thermal damage may all differ depending on the peak current and the pulse width.

Recently there has been a reduction in the occurrence of ESD damage due to the wider adoption of static management measures in manufacturing processes that handle these devices. In contrast, EOS damage is occurring with greater frequency. EOS damage is not necessarily caused by surge-like electrical stresses, but rather a wide range of causes are possible. These include connection with a connector with a voltage of a few volts remaining, inadvertent shorting or voltage application during non-standard work operations, and circuit shorting due to conductive foreign materials or solder bridges. For EOS, it is extremely difficult to infer the cause of the damage from only the results of a failure analysis.

Furthermore, it is impossible to reproduce EOS damage in an ESD test. It is necessary to lower the current value and lengthen the pulse width to match those that actually occur to reproduce EOS damage, and to reproduce cases where damage occurs with power applied, it is necessary to perform testing after investigating the actual operating state, including the pulses applied.

(1) Damage Due to Electrostatic Discharge and Electrical Overstress

As shown in Table 3.5, there are similarities between ESD and EOS damage and it can be difficult to avoid confusion occur during fault analysis.

Table 3.5 MOS Device Failure Types from the Standpoint of Electric Stress Factors

Failure Mechanism	Stress Factors	Failure Modes
Bonding wire disconnection due to melting	EOS	Occurs due to a large current flowing for an extended period. The broken ends of wire are rounded.
Open circuits in metal lines due to melting	EOS	Occurs due to a large current flowing for a comparatively long time. In the state where heat generation and dissipation occur in equilibrium, places where the temperature rise melt. This failure is almost never seen in ESD, where the pulse width is narrow.
Open circuits in polysilicon due to melting	Mainly EOS	For polysilicon, as resistance values are large, power concentrates and melting occurs easily.
Contact section damage	Mainly EOS	Due to reverse bias current in junction, heat is transferred to contact section and metal interconnects melts.
Heat degradation of oxide film	Mainly EOS	Junction reverse bias current heat is transferred to oxide film, resulting in degradation.
Junction degradation	EOS or ESD	Occurred by junction reverse bias current heat and the like.
Hot electron, Trapping	EOS or ESD	Carriers accelerated by high electric fields are trapped in MOS transistor oxide films.
Oxide film degradation due to electric field	Mainly ESD	Occurred by application of voltage to gate oxide film.

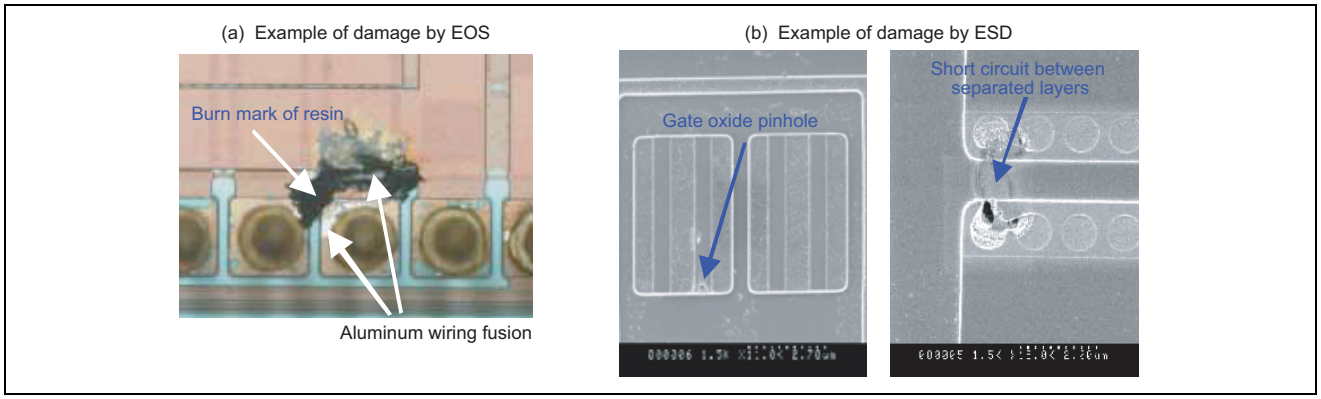


Figure 3.49 Example of Comparison between EOS Damage and ESD Damage

For example, we can say that the interconnect fusion and charred resin contamination such as that shown in Figure 3.49(a) was due to damage by EOS with a large amount of energy dissipated and a long period during which that stress continued. However, if the region where damage occurred is more limited, there are cases where there are common visual features between ESD and EOS damage and it will not be possible to differentiate the cause. In such cases, it is reasonable to consider EOS damage if the damage can be easily found with an optical microscope.

Damage due to ESD can be classified into damage to junctions and dielectric film and characteristics degradation due to charge injection into oxide films. Since the energy dissipated is relatively small, in many cases it will be not be possible to observe the traces of the damage with an optical microscope, as shown in Figure 3.49(b).

Damage such as the melting of interconnects and junction breakdown can be assumed to be due to the heat generated by the application of pulses. For example, the well-known Wunsch & Bell model explains that junction breakdown is caused by the melting of silicon at a junction when the local temperature exceeds the melting point of Si, which is 1415°C. The temperature rise is due to the heating caused by the reverse bias pulse current. The allowable applied power per unit area of the junction (P/A) is expressed in the following equation (3-5-1).[53] [54] [55]

$$\frac{P}{A} = \sqrt{\pi \cdot K \cdot \rho \cdot Cp}\ (Tm-Ti) \cdot t^{-1/2} \qquad (3\text{-}5\text{-}1)$$

where

P: Applied Power (W)
A: Junction Area (cm^2)
K: Thermal Conductivity near the Junction (Si: 0.306 W/cm • K)
ρ: Junction Density (Si: 2.33 g/cm)
Cp: Specific Heat of the Junction (Si: 0.7566 J/g • K)
Tm: Junction Melting Temperature (Si: 1688 K)
Ti: Junction Initial Temperature (Room temperature = 298 K)
t: Pulse Width (ESD duration)

All values with the exception of the pulse width (t) are constant in equation (3-5-1), so power tolerance per unit area at the junction is proportional to $t^{-1/2}$.

Figure 3.50 shows a plot of experimental values, which fall between those calculated from the equation above and 1/10 of those values.

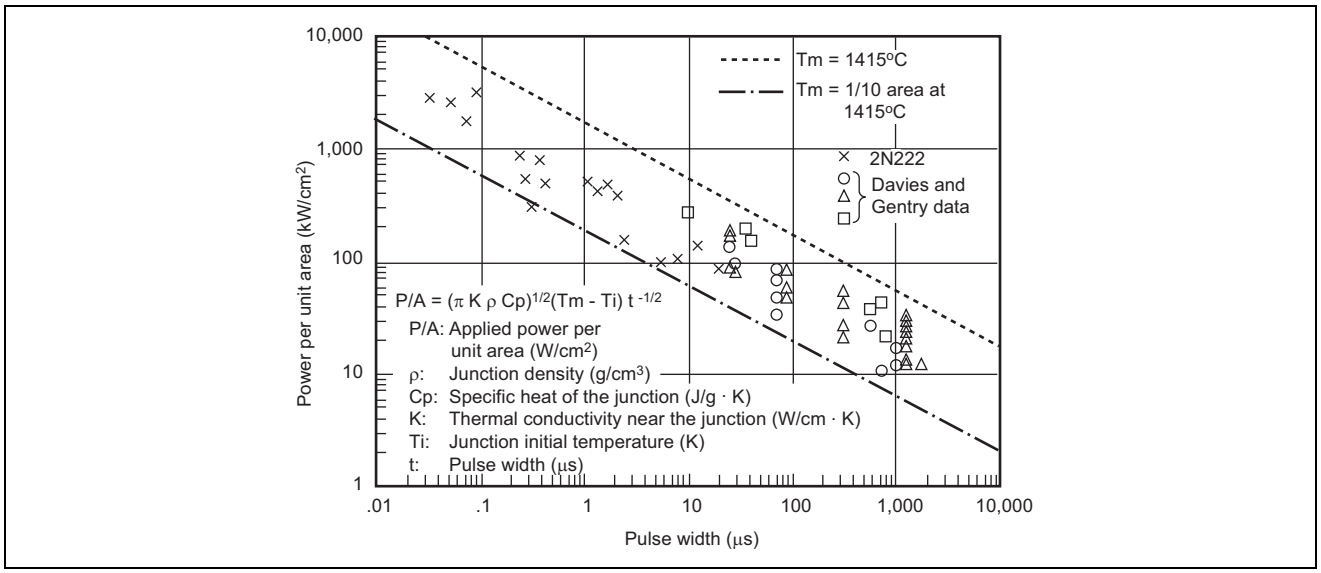


Figure 3.50 Wunsch & Bell Plot

As just described, damage due to heat depends on the amount of heat generated, specific heat, heat conductibility, and allowable temperature limit. These factors indicate that damage is fundamentally avoidable only by diffusion at heat-generated locations. However, when it is understood that most actual electrostatic discharges have pulse widths shorter than those indicated in Figure 3.49 and that their energy is small, measures other than those dealing only with heat, such as protective elements, need to be considered.

By contrast, the cause of damage to a dielectric film is thought to be due to eventual destruction by Joule heat after the current leakage in the dielectric film increases over time in a high electric field. Because the gate oxide films of most MOS devices have a breakdown voltage of 10 to 20 V, which results in damage when an excessive voltage is applied, protective elements are required to prevent damage.

Variation in device characteristics due to charge injection refers to the phenomenon of changes in characteristics due to the acceleration of carriers by locally generated potential differences so that the carriers become trapped in the oxide film. Such changes may recover or anneal out at elevated temperatures. Failure analysis is difficult since there are no visual indications for this failure mode.

(2) Charging Phenomena Requiring Caution When Handling Devices

From the standpoint of handling devices, the causes of charging are classified as types (a) to (c) below. The figures in this section (Figures 3.51 to 3.53) illustrate charging on a device. Charging on a printed circuit board, tool, human body, or any other conductive substance can be substituted.

(a) Charging by Friction or Delamination

Figure 3.51 illustrates the well-known charging by friction/delamination phenomenon. A charged conductor discharges when it comes close to another conductor. In addition, it sometimes charges the other conductor by electrostatic induction or contact charging. On the other hand, a charged insulator does not discharge, but it may charge a conductor by electrostatic induction.

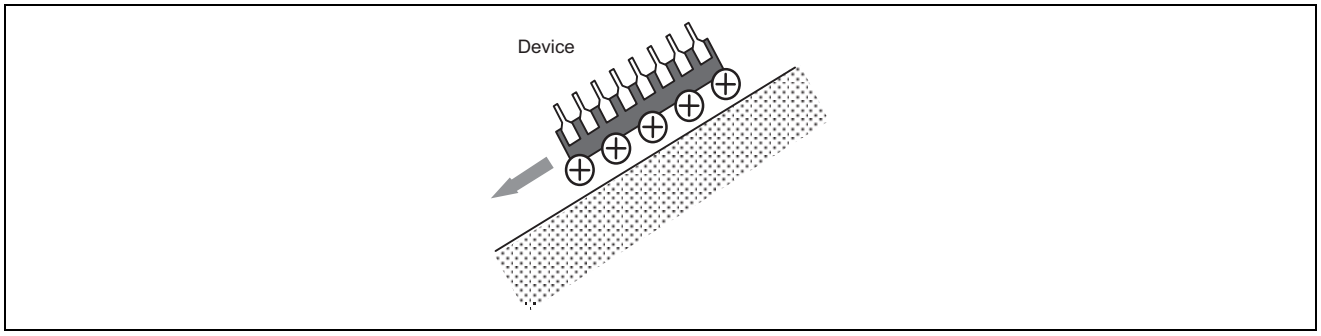


Figure 3.51 Triboelectric Charging

(b) Electrostatic Induction Phenomena

Electrostatic induction is a frequent phenomenon whenever devices are handled, but because it is not generally understood, attention needs to be paid to its causes. As shown in Figure 3.52, when a device, human body, tool, or other conductor in the floating state comes close to a charged conductor, electrostatic induction occurs in the conductor even though its total amount of electric charge is zero. If the conductor then contacts another conductor, it induces a discharge equivalent to that which would occur if it were charged. As a result, the discharge charges the device, and the device is in danger of discharging.

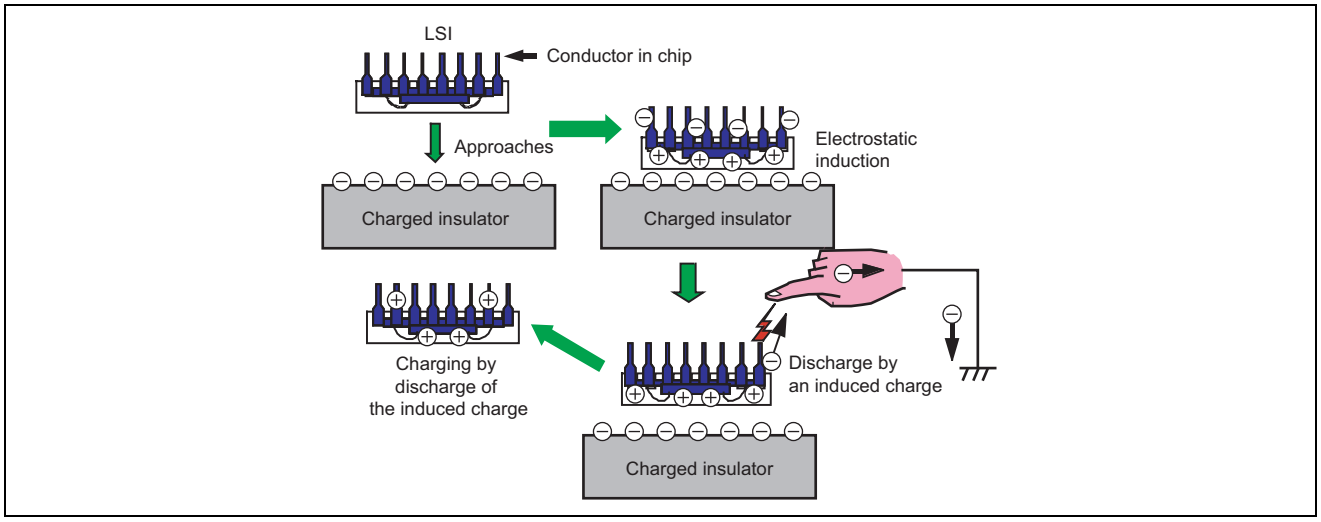


Figure 3.52 Discharge by Electrostatic Induction and Charging

(c) Contact Charging

When an uncharged conductor contacts a charged conductor, the conductor becomes charged. Figure 3.53 illustrates an example of a case where a charged human body charges a device when the device is grasped.

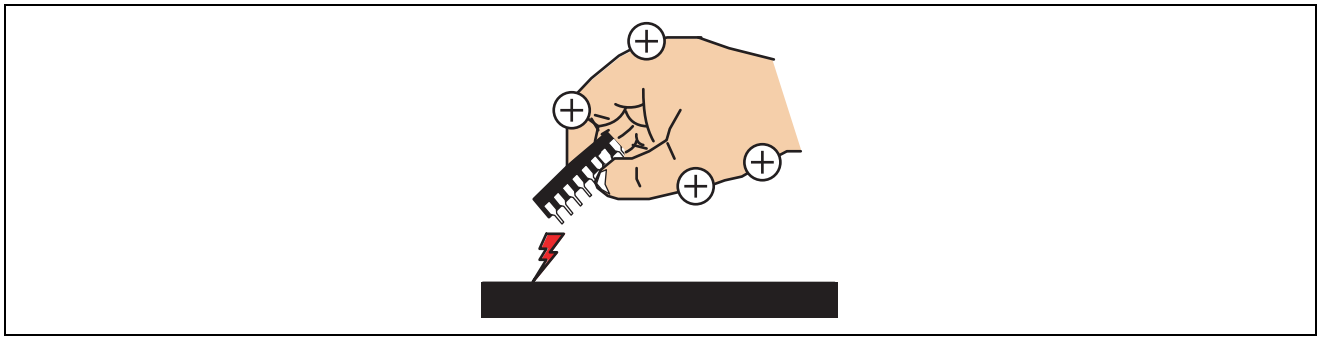


Figure 3.53 Contact Charging and Discharging

(3) ESD Phenomena that Can Damage a Device

An electrostatic discharge of a device occurs when a discharged current flows in the device. The higher the electric current, the easier it is for damage to occur. In the environments in which semiconductors are handled, since there are various conditions under which large currents flow, it is likely that, in most cases, good conductors (metal conductors in general) may be involved.

Two models exist for the types of discharge paths in devices. Figure 3.54 shows a model in which a conduction current flows between device pins, and Figure 3.55 shows a model in which a conduction current flows between pins and a displacement current flows in the device capacitor. The model in Figure 3.55 has a long discharge path and the capacitance and inductance are distributed on the path, so the model has a slower discharge than the model in Figure 3.54.

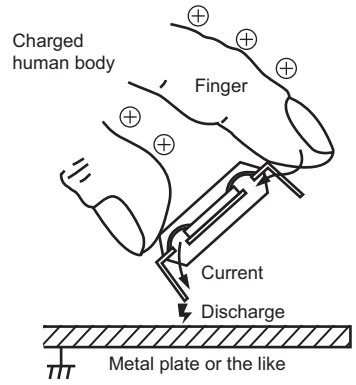


Figure 3.54 Discharge Model based on Human Body Model (Model in which a Conduction Current Flows between Device Pins)

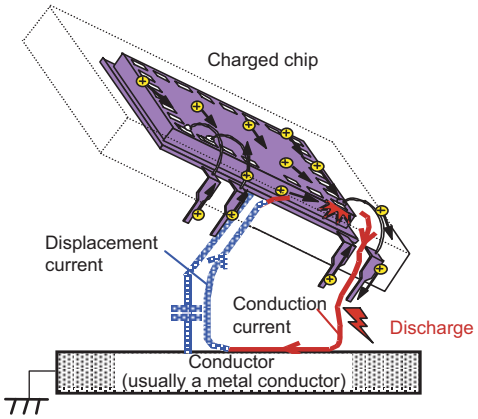


Figure 3.55 Discharge Model based on Changed Device Model (Model in which an Conduction Current Flows to the Discharging Pin and a Displacement Current Flows to the Device Capacitance)

Figure 3.54 illustrates an example of a discharge current between a human body and a device pin. Figure 3.55 illustrates an example of a discharge between a device and a conductor (usually a metal conductor). As shown in the example, when a low-resistance substance such as a metal is involved, a discharge current flows easily and damage occurs easily. In addition, for the case in Figure 3.54, when GND to which the current flows is a metal, damage occurs easily. Therefore, in environments in which devices are handled, it is necessary to pay attention not only to charged objects but also to objects to which the device comes into contact.

(4) Actual Discharge and Test Methods

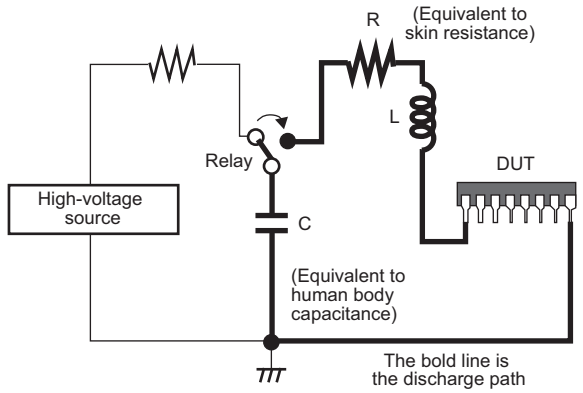
Three major types of applicable test methods are currently available as practical electrostatic discharge models [56] [57]:

- Human body model: HBM
- Machine model: MM (replaces HBM)
- Charged device model: CDM

(a) Human Body Model Test Method

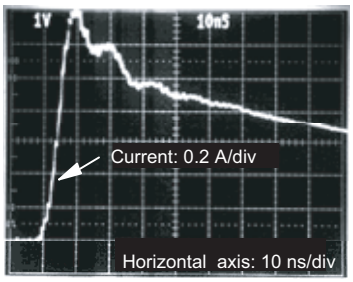
Figure 3.54 shows the Human Body Model (HBM): A human body charged with static electricity touching a device and discharging to a device pin. If any of the other pins are grounded or connected to a potential, a discharge current passes through the device and the device can be destroyed.

The ESD test circuit for the HBM is illustrated in Figure 3.56. The charge on capacitor C represents the amount of charge on a typical human body. The resistor R simulates the skin resistance. JEITA, JEDEC and MIL standard specify 100 pF and 1,500 Ω.

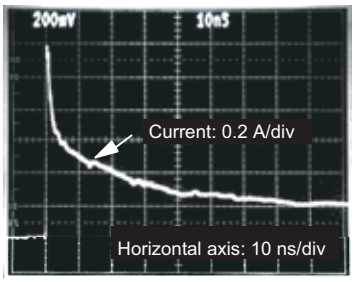


C	R	L
100 pF	1.5 kΩ	No value specified

Figure 3.56 Test Circuit for Human Body Model



(a) Example of HBM tester discharge current (conditions: 2000 V, short circuit)



(b) Example of discharge current from a fingertip (charge voltage of human body: 2000 V)

Figure 3.57 Comparison of Human Body and HBM Tester Discharge Currents [72]

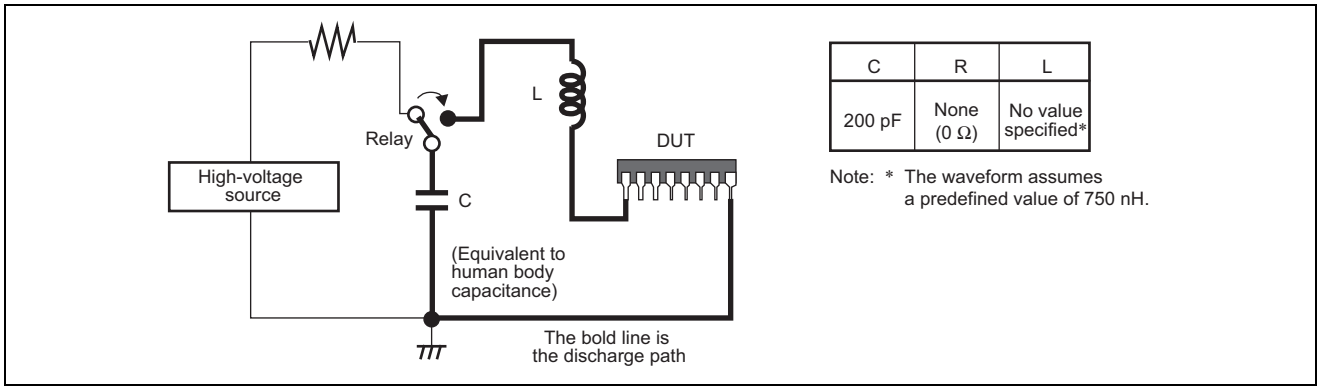
Figure 3.57 shows an example of the waveforms of discharges from the human body and the electrostatic discharge tester. The capacitance of the human body was about 300 pF (DC measurement method), but analysis of the discharge waveform reveals that the capacitance in the period during which a device-destroying high current is generated is effectively about several pF to several tens of pF. Since a full discharge takes several seconds, it is thought that the discharge proceeds through peripheral high-resistance elements. By contrast, since the tester has a single 1.5-kΩ resistor, the example shows a simple attenuating waveform, and its energy aspect is several times to 10 times severer than the human body discharge. Due to the wiring configuration, the example also shows a delayed rising edge by the inductance and other factors.[62]

Because the peak current influences the voltage generated in the device, and the peak current period influences the electrical power generated in the device, the HBM test method tends to emphasize destruction by electric power rather than actual device destruction.

(b) Machine Model Test Method

The machine model test method is a human body test method that has been long used in Japan (Figure 3.58). We have records indicating that Machine Model (MM) test methods were applied in our in-house tests in the latter half of 1960s as a test method that could reproduce a discharge from the human body or the like with a low voltage. Later, in 1981, it was standardized by EIAJ (present JEITA).

In countries other than Japan, the test method was named the MM method in the latter half of 1980s because the 200 pF and 0 Ω conditions did not take into account the skin resistance (0 Ω was assumed). The name "Machine Model," which implies a metal discharge, was therefore applied through a misunderstanding. You need to make sure that you understand this method is not related to a metal discharge. In 1996, JEDEC standardized this type of test method in the U.S. The background of the JEDEC's MM test method standardization was that the various types of MM test methods existing at the time needed be unified in response to many requests for test data from Japanese semiconductor users. Other certification test standards attach importance to CDM and HBM and do not recommend this machine model for electrostatic discharge testing.



C	R	L
200 pF	None (0 Ω)	No value specified*

Note: * The waveform assumes a predefined value of 750 nH.

Figure 3.58 Machine Model Test Circuit

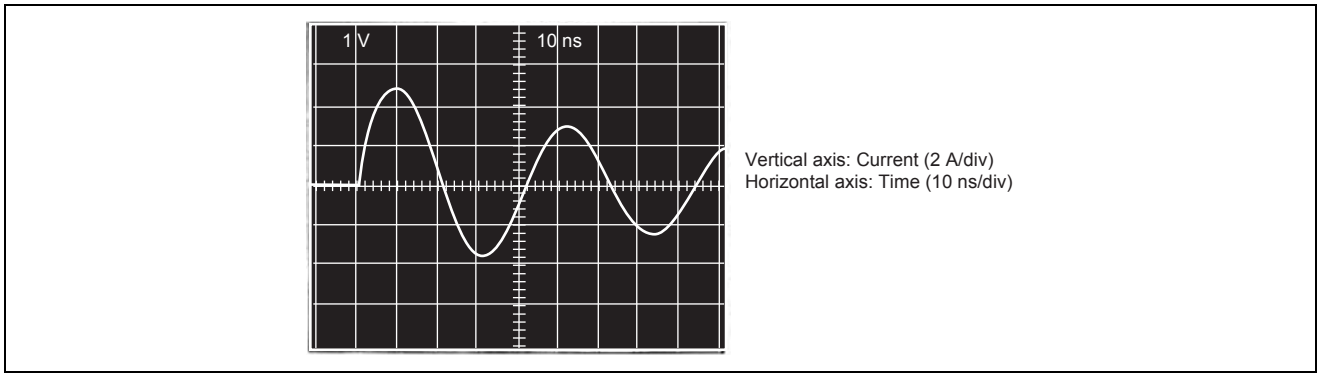


Figure 3.59 Discharge Waveform for Machine Model Test (Example with a Low Inductance L)

Output waveforms of the machine model test form a damped oscillation due to the influence of the test circuit inductance. Figure 3.59 shows an example of a waveform on a tester with shorter wiring than that specified by JEDEC and with a rapidly rising edge.

In semiconductor handling processes, however, it is thought that the metal objects easily picking up a charge are tools and implements. Since large components are grounded, they never pick up a charge as long as their grounding is not disconnected or otherwise compromised. Figure 3.60 shows an example of a discharge waveform of charged metal tweezers. A feature of the waveform is an extremely short rise time of about 100 ps, which is very close to the limit that a 3.5-GHz oscilloscope can measure. Other small metal tools produced a similar waveform. Discharges of metal

substances are very rapid like this and similar to the CDM discharge described later. The reason is that charged metals have very little inductance.[60] [61]

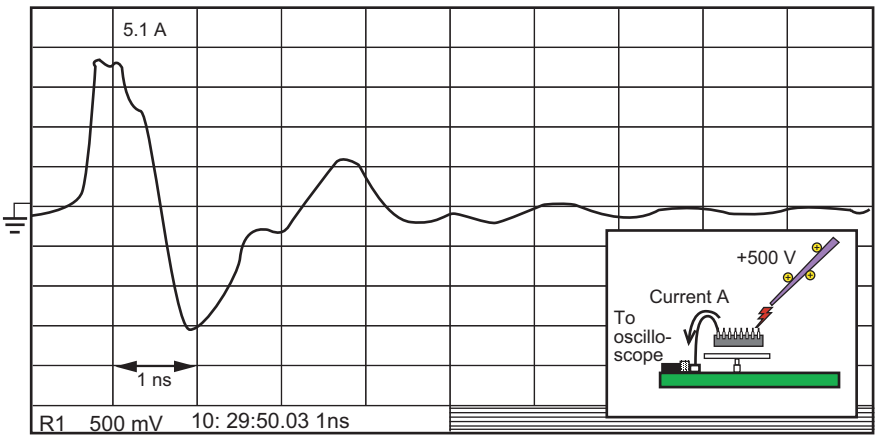


Figure 3.60 Discharge Waveform of Charged Metal Tweezers (Completely Different from That of the Machine Model)

As described earlier, the machine model test method indicates discharge characteristics completely different from those of a metal discharge that the method's name implies. It produces waveforms that are unusual in ordinary semiconductor handling processes, and provides no observable correlation between test and field. For these reasons, it has been demoted to a reference test model in the JEITA specifications. JEDEC also does not recommend this.

(c) Charged Device Model Test Method

As the automation of assembly increases, there are fewer operations in which humans touch devices and ESD damage due to HBM has been declining. Conversely, however, the occasions on which devices encounter friction and/or electrostatic induction and come into contact with metal substances has increased.[58] [59] [63]

In view of this increase in CDM discharge from contact between a charged device and a metal substance as the trend toward process automation continues, the CDM is a discharge model that needs to be treated with caution.

As shown in Figure 3.61, a CDM discharge is caused by a charged device that makes contact with a machine, tool, or other metal object. The discharge is very rapid, and an oscilloscope that supports bands over 1 GHz is required to observe it. Figure 3.62 shows the measurement result of the waveform of the CDM discharge example shown in Figure 3.55. The rise time of the waveform is less than 100 ps, which is the limit the oscilloscope can measure. This indicates that the rise time is faster by two or more orders of magnitude than the rise time of the human body model or machine model.

However, as already mentioned, the CDM discharge is similar to the metal discharge shown in Figure 3.60.

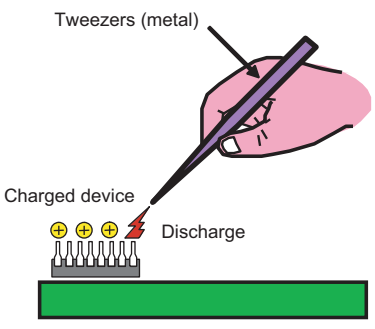


Figure 3.61 Discharge Example of the Charged Device Model (Example of a Discharge to a Metal Tool or the Like)

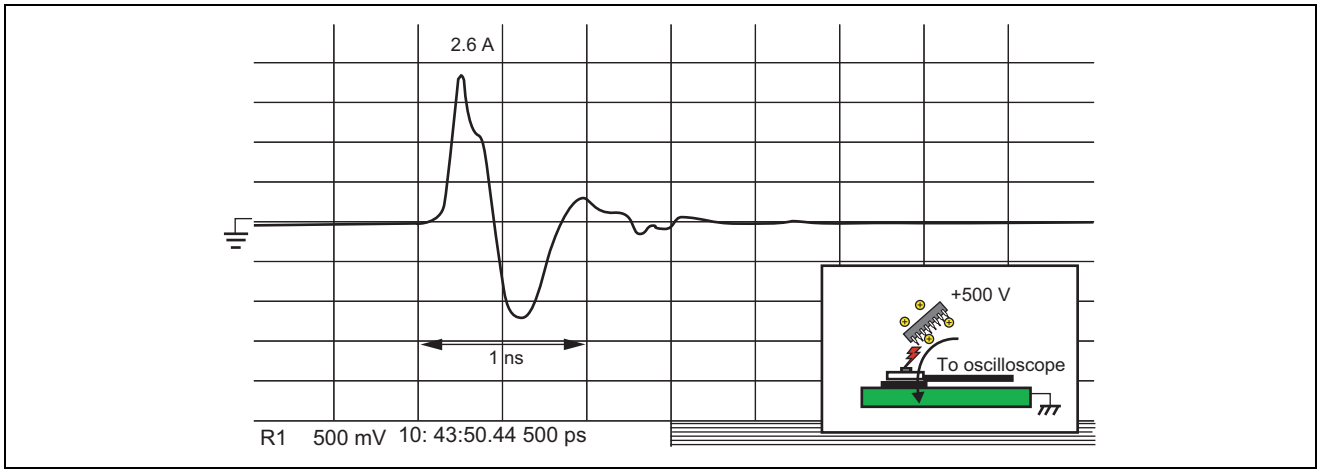


Figure 3.62 Discharge Waveform for Charged Device Model (Measured with a 3.5-GHz Oscilloscope)

ESD damage due to CDM discharge is caused by the current concentration discharging all of the stored charge through the pad of the discharge pin. The discharge current waveform shows high-speed oscillations, and is accompanied by severe transients within the device. Dielectric breakdown of oxide films results in most cases due to excessive voltage spikes, but thermal damage sometimes occurs due to energy concentration. Figure 3.63 shows an example of a CDM test circuit that we developed. In this test circuit, the ground bar corresponds to the tweezers or tool assumed in Figure 3.61 for simulation of a realistic form of discharge. Figure 3.64 shows the relationship between a fraction defective and a JEITA-standardized CDM test result. The fraction defective is based on one of our device package assembly processes that was a problem in the 1980s, when CDM problems had not been clearly identified and adequate measures had not been taken for them. As the figure shows, the CDM test clearly correlates with the process fraction defective, and the corner pins of the device have the potential to easily touch another substance and discharge.[70]

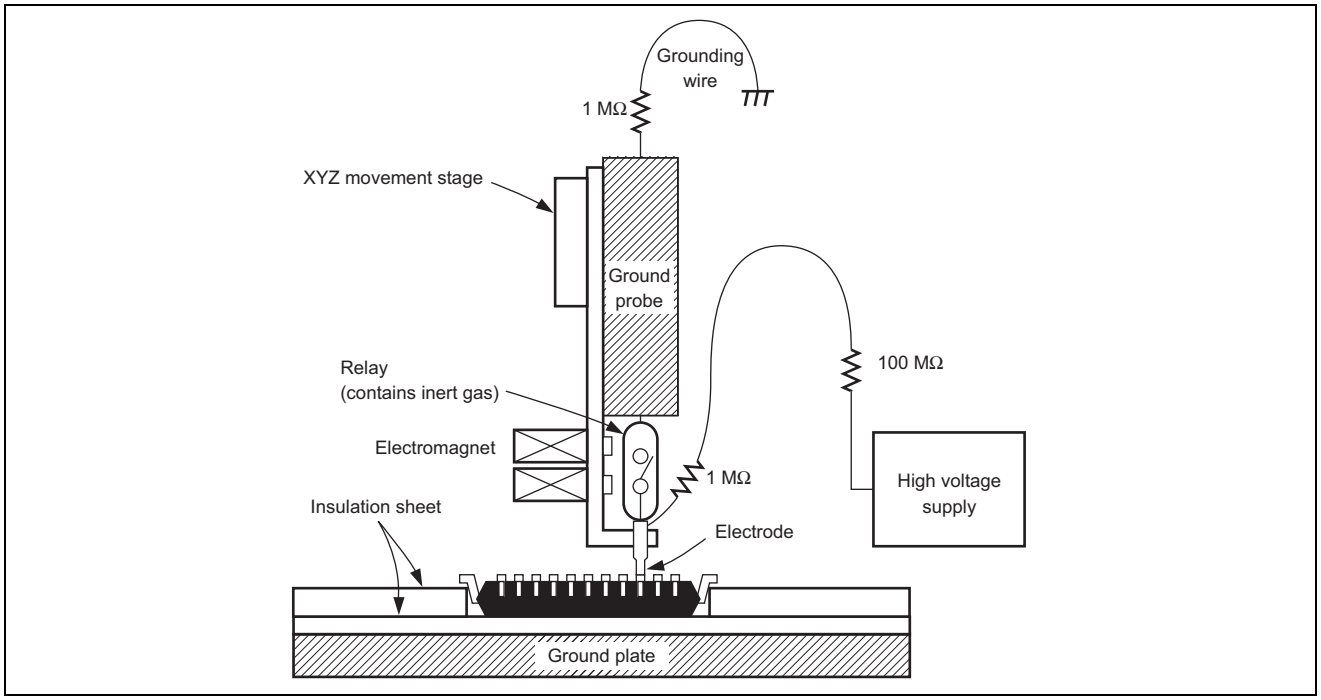


Figure 3.63 Example of CDM Test Circuit
(Device is Charged from High-Voltage Source, Relay is Closed, and Device is Discharged to a Ground Bar)

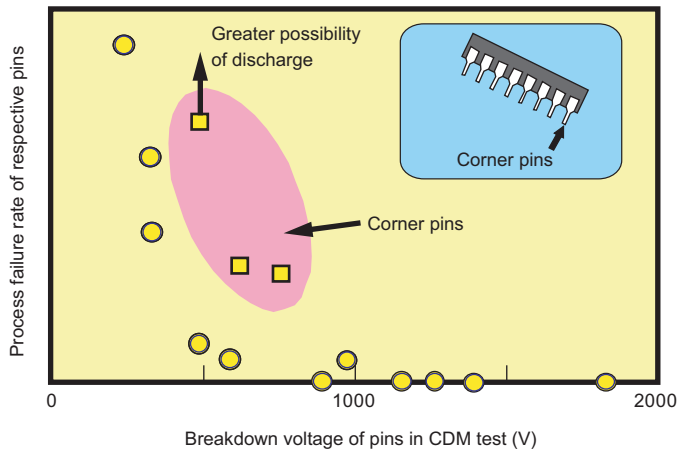


Figure 3.64 Relationship between Fraction Defective in Package Assembly Process and CDM Test Intensity

(d) Complex Discharge, Including CDM Discharge

It is natural to suppose that, as shown in Figure 3.65, the discharge resulting from a charged person touching a pin of the device in his hand to a metal object is purely an HBM type of discharge. Close investigation reveals that it contains, in fact, components equivalent to both HBM and CDM discharges. The following describes the complex discharge process.

When the metal plate and device pins come into contact, the electric field is propagated to the device, and the charge accumulated by the device begins to be discharged through the pins. This portion is equivalent to CDM discharge. Then, after the device charge has been transferred to the person, the charge on the person flows through the device and out the pin to the metal object. Figure 3.66 shows an example of a measured waveform. Due to skin resistance, the discharge current from the human body is small and the discharge time is longer. Accordingly, the CDM discharge current shows a higher value.

In cases other than the example above where a conductor touches another conductor with a different electric potential, a discharge equivalent to a CDM discharge is also observable. This may be one of the reasons why the CDM failure rate is high compared with other rates of failures in the market.[60] [61] [62]

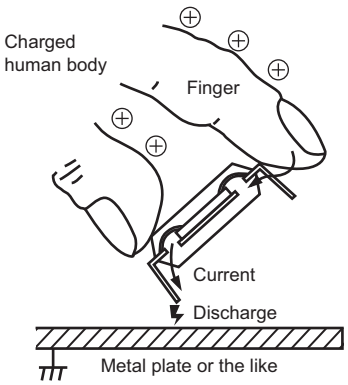


Figure 3.65 Example of Complex Discharge on HBM and CDM

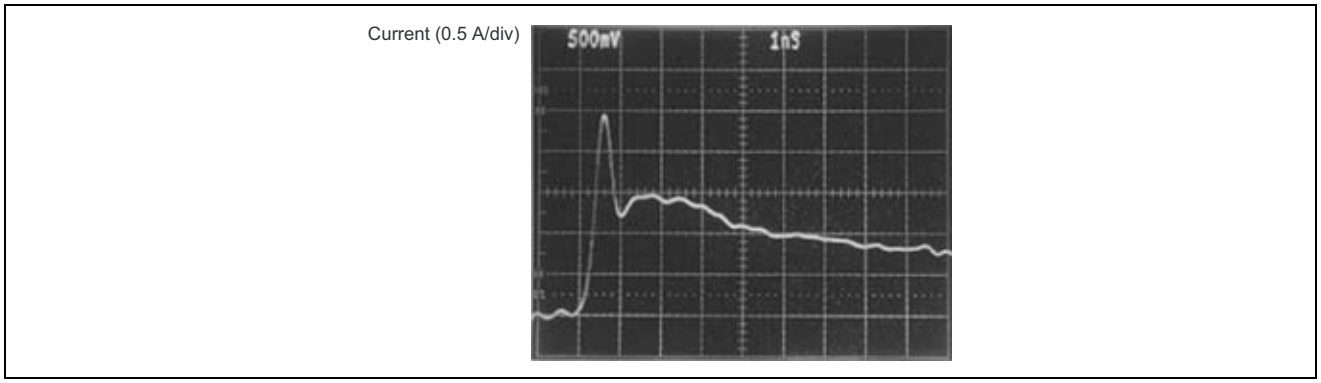


Figure 3.66 Example of Complex Discharge Current Waveform

3.5.2 Latchup

(1) Introduction

Due to their low power consumption and wide noise margin, CMOS devices are widely used in low power and high performance applications. Large capacity memory chips and high performance microcontrollers are made using miniaturized CMOS technology.

A CMOS device includes parasitic NPN and PNP bipolar transistors in the input and output circuitries. Those transistors combine to form a parasitic thyristor. In a CMOS device to which power-supply bias has been applied, sufficient noise in the form of e.g. an external surge can turn the parasitic thyristor on, causing a continuous excessive flow of current through the power supply line. This phenomenon, called latchup, is seen for example in inspection processes after the chip has been mounted on a circuit board, and can destroy the device. Since the miniaturized structures of recent LSI circuits make them particularly susceptible to the effects of such parasitic elements, these factors must be fully considered in the design process.

(2) Mechanism

Because basic CMOS devices use inverters made from MOS transistors with two different characteristics as basic elements, parasitic bipolar transistors occur everywhere on a chip.

Equivalent circuits differ slightly depending on the parasitic element combinations, but one example of a cross section is shown in Figure 3.67. Figure 3.68 shows the equivalent circuit for the parasitic transistor circuit in the cross-section example.

First we will consider the case where a sufficiently large positive DC or pulse current is applied to the output pin:

1. Transistor TR3 base-emitter junction is forward biased. TR3 turns on.
2. Current Ig flows through TR2 base resistance R_P to V_{SS}.
3. TR2 base potential increases due to R_P voltage drop. TR2 turns on.
4. Current flows from V_{CC} to V_{SS} through resistance R_N of TR1.
5. Due to voltage drop across R_N, TR1 base potential increases, and TR1 turns on.
6. Current flows from V_{CC} through turned on TR1 and base resistance R_P to V_{SS}.
7. The TR2 base current is biased again by this current.

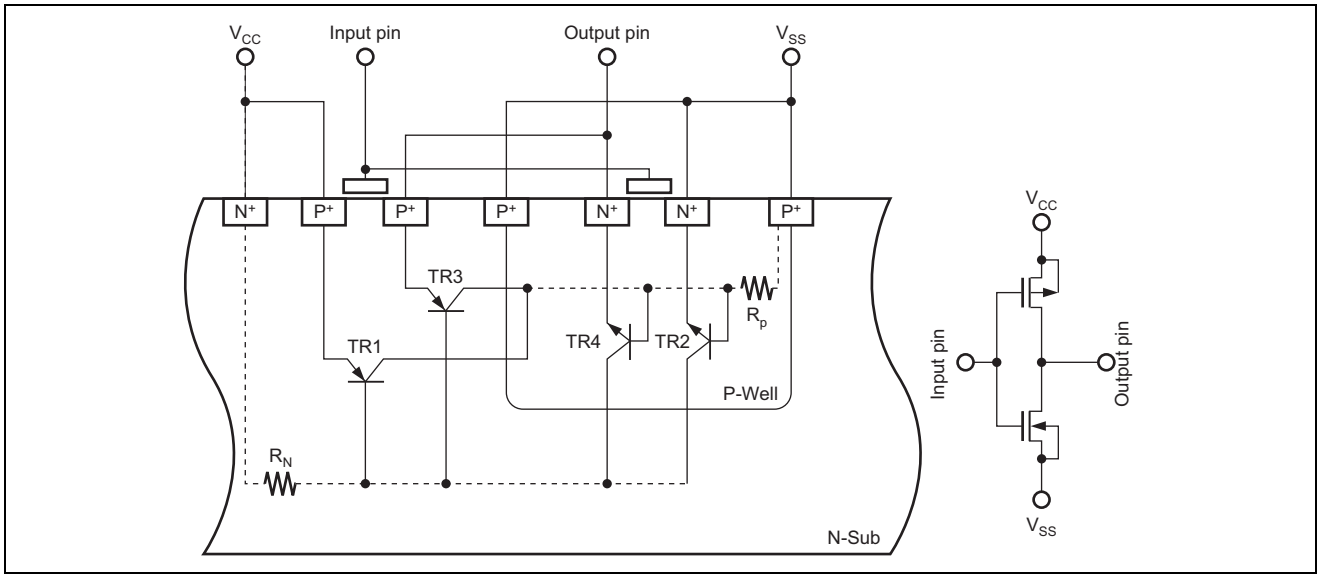


Figure 3.67 Cross Section of CMOS Inverter

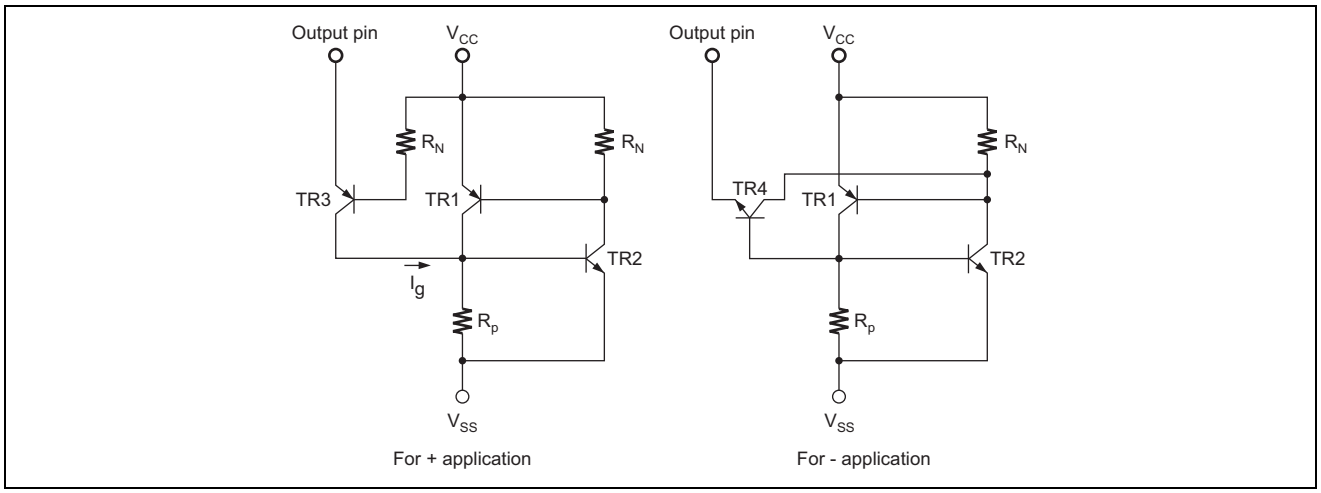


Figure 3.68 Parasitic Thyristor Equivalent Circuit

Positive feedback in the TR1-TR2 closed loop circuit maintains the current flow between V_{CC} and V_{SS} even if the trigger stops. TR4 transfers negative triggers. Positive feedback in the TR1-TR2 closed loop circuit maintains current flow just as in the case of the positive trigger.

(3) Evaluation Method

There are various methods to evaluate a circuit's susceptibility to latchup. Two methods defined in EIAJ ED-4701/test method 306, and JEDEC/JESD78 are explained below.

(a) Current Pulse Injection Method

A trigger pulse is applied to the input or output pin of a device with the specified supply voltage applied, as in Figure 3.69. The current of the trigger pulse is increased until latchup occurs.

If input/output resistances are high and the trigger current cannot be injected, the application of the output voltage from the trigger pulse current source is stopped at a maximum value (clamp voltage) to prevent destruction of the device. Care must be taken not to cause destruction due to excessive current injection. After the latchup test it is important to confirm that the device being tested has not been destroyed.

(b) Power Supply Over-Voltage Method

The power supply over-voltage method is shown in Figure 3.70. The device is evaluated with its supply voltage set to the recommended supply voltage to measure the resistivity to latchup.

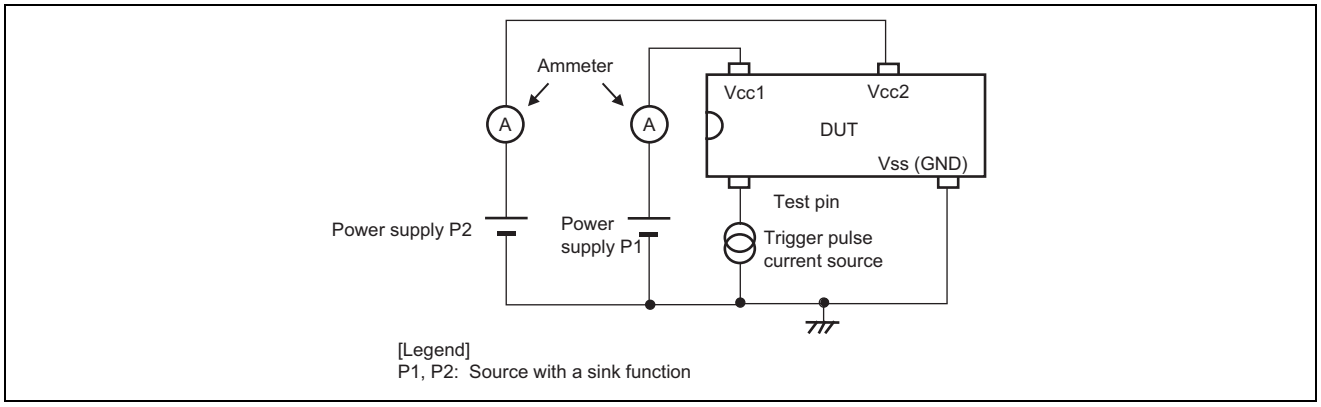


Figure 3.69 Latchup Test Circuit (Pulse Current Injection Method)

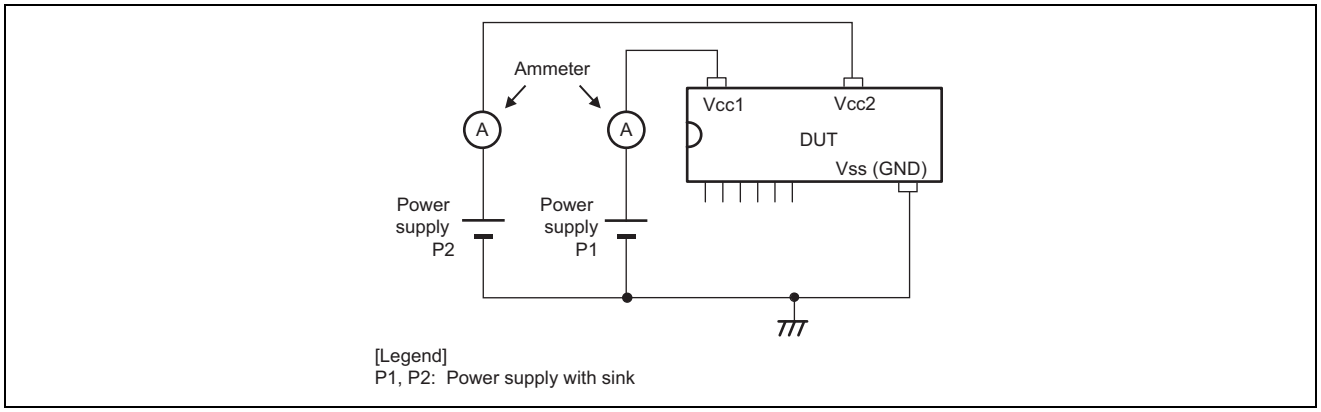


Figure 3.70 Latchup Test Circuit (Power Supply Over-Voltage Method)

3.5.3 Power MOS FET Damage

Power MOS FETs are superior power devices with excellent high-speed switching characteristics and a negative temperature characteristic. Power MOS FETs are therefore widely used in switching power supplies and motor controls where high efficiency and accuracy are important considerations. Their uses in electrical equipment for automotive application, office automation (OA), and lighting are expanding.

However, damage occurs in high frequency and high power applications due to the miniaturized cell design peculiar to power MOS FETs (Figures 3.71 and 3.72).

(1) Inductive Load Damage (Avalanche Breakdown)

Avalanche breakdown of a power MOS FET is a phenomenon due to the operation of the parasitic transistor that exists in the MOS FET structure. If a flyback voltage generated in the off period (during high-speed switching) during operation with inductive loads such as transformers or motors or a spike voltage due to leakage inductance exceeds the power MOS FET's rated drain voltage, the avalanche state occurs between the drain and the source and an avalanche current flows in the device.

Part of this avalanche current flows through the base resistor R_B under the source (N^+) area of the transistor. Accordingly, if either R_B is large or the current is large, a potential difference is created between the base and emitter and the parasitic transistor may operate. If this occurs, it produces a concentration of current that destroys the power MOS FET.

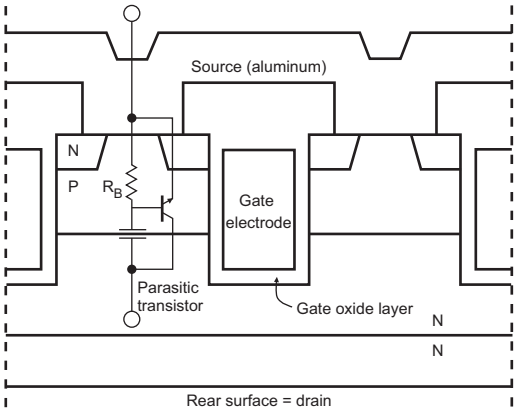


Figure 3.71 Section View of Power MOS FET

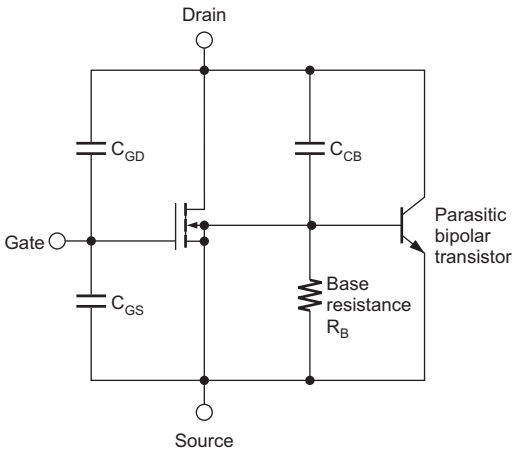


Figure 3.72 Equivalent Circuit of a Power MOS FET

Figures 3.73 and 3.74 show the circuit diagram for avalanche resistance evaluation and its operating waveforms. At turn off, when the gate voltage VGS falls below the threshold value, the drain current ID flowing in the inductance L falls and the drain voltage V_{DS} rises rapidly. When that voltage reaches $V_{DSX(SUS)}$, the power MOS FET goes to the avalanche state and the drain voltage becomes constant. The energy stored in the inductance L flows within the power MOS FET as an avalanche current and is dissipated as heat. As shown above, the avalanche resistance indicates how much energy stored in the inductance L the power MOS FET can dissipate without being destroyed.

Note that to determine whether or not avalanche operation is allowed, the following items must be thoroughly checked and analyzed: (1) that the time will be fixed at startup and other times (that the maximum ratings are not exceeded in steady-state operation) and (2) that the avalanche current is within the maximum ratings.

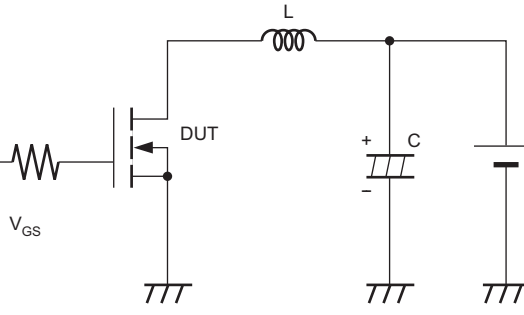


Figure 3.73 Avalanche Tolerance Evaluation Circuit Diagram

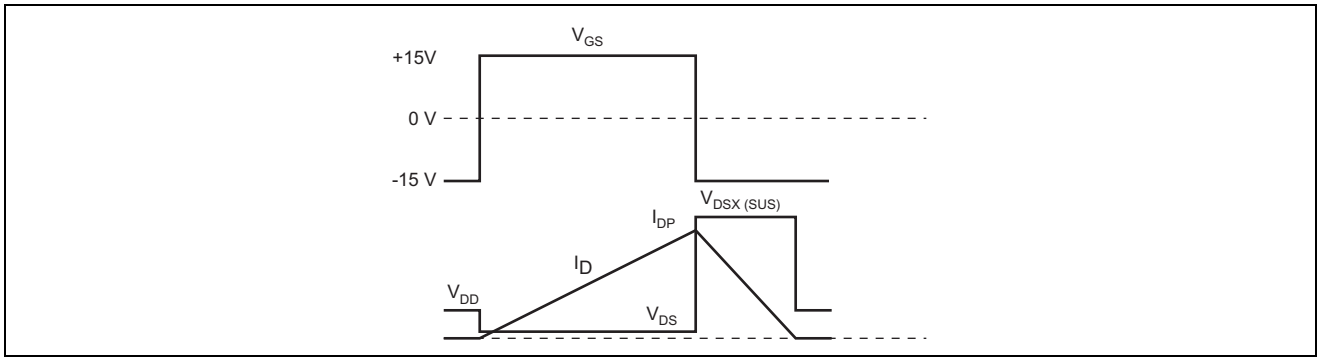


Figure 3.74 Avalanche Waveforms

(2) Electrostatic Discharge of Gate Oxide Film

Power MOS FETs are power elements, but they are susceptible to damage due to electrostatic surges or excessive gate voltages because they incorporate MOS structures. There are also products that include gate protection devices to prevent this from occurring (see Figures 3.75 and 3.76). However, a vertical-type power MOS FET with the DMOS structure is optimized for high-voltage and high-capacitance applications, so incorporation of protective elements using PN junctions is difficult due to their parasitic effect. Therefore, resistance to ESD is improved in power MOS FETs that do not have built-in protective devices by using polycrystalline silicon devices formed above the dielectric film.

The following three measures have been proposed to prevent electrostatic destruction of the gate oxide film.

1. Grounding personnel through a 1 MΩ resistor to ground when handling devices.
2. Assuring that all equipment is grounded.
3. Inserting gate resistors and zener diodes as a measure to prevent the application of possible gate surges after devices have been mounted on a board.

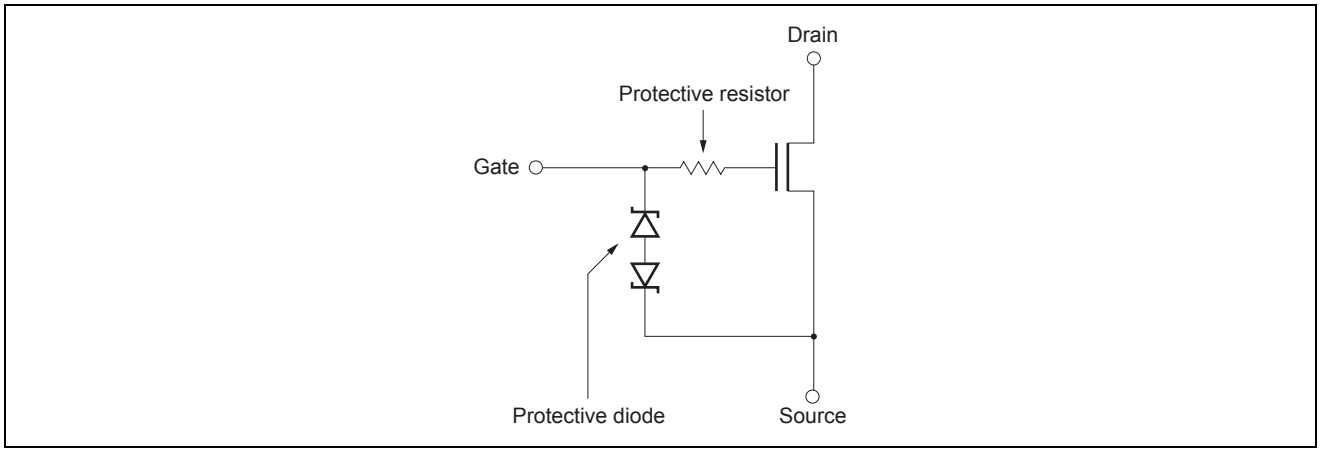


Figure 3.75 Gate Protection Circuit

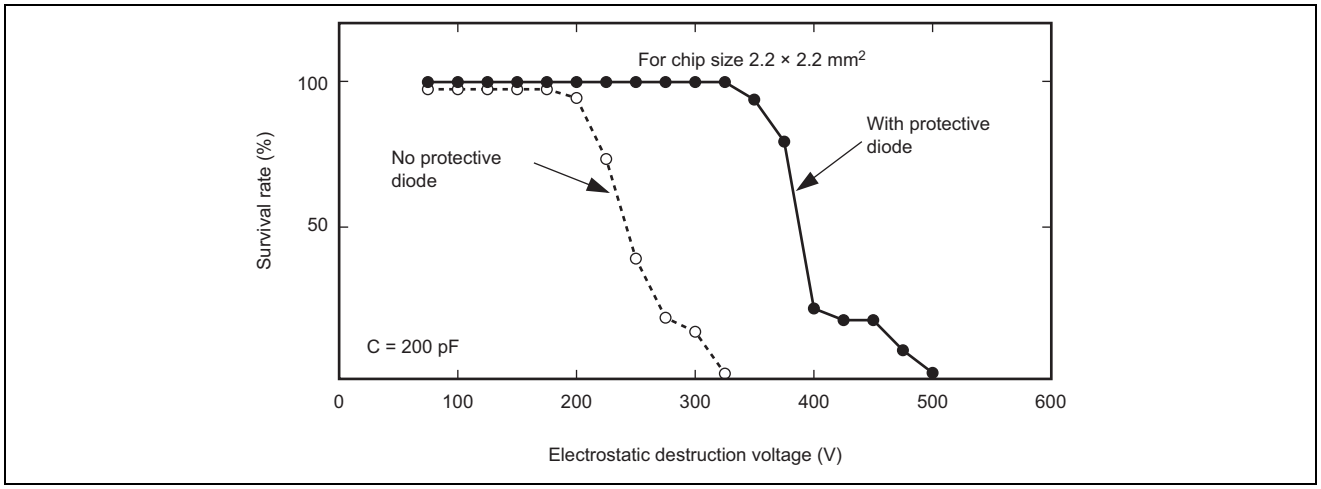


Figure 3.76 Electrostatic Discharge Strength of a Gate Oxide Film

(3) Damage by Operating Voltage Drop

If the gate drive voltage falls during MOS FET operation (note that except for special devices that can operate at 4 V, about 10 V is usually required for operation), the device enters the active mode region (Figure 3.77) and as a result operation may exceed the SOA (safe operating area) as determined by the thermal design and the device may be destroyed. Therefore, it is necessary to check the excessive load, and that the gate voltage has not been lowered transitionally due to the change of the power supply voltage at power-on.

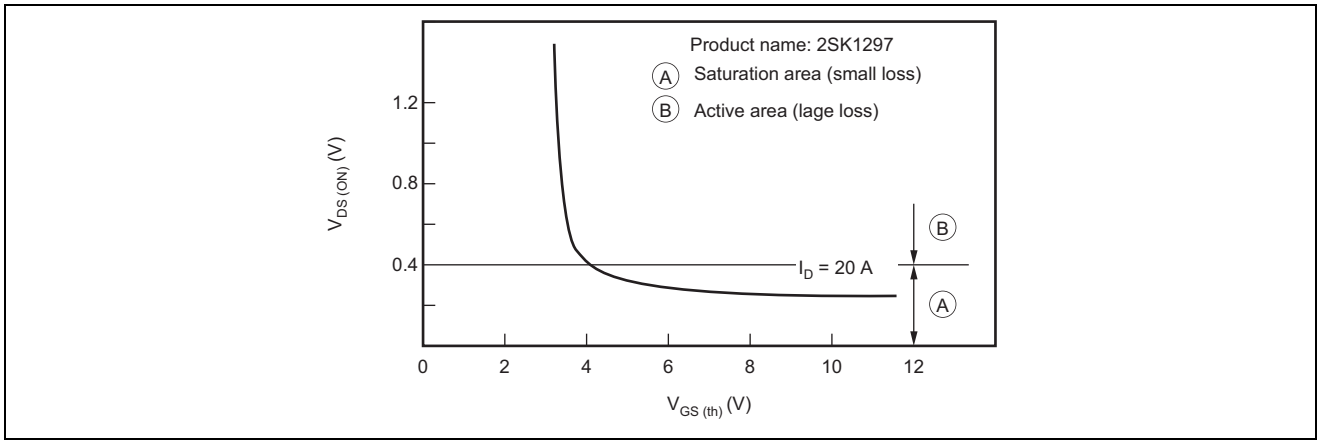


Figure 3.77 $V_{ds(ON)}$ - $V_{gs(th)}$ Characteristics in Practical Use

(4) Secondary Breakdowns in Power Transistors

A failure that involves momentary and unrecoverable shorting between the collector and emitter can occur during a power transistor's switching operations even when the operating conditions are within the rated voltage, rated current, and allowable dissipation. This phenomenon is called a secondary breakdown.

Figure 3.78 shows safe operating area (SOA).

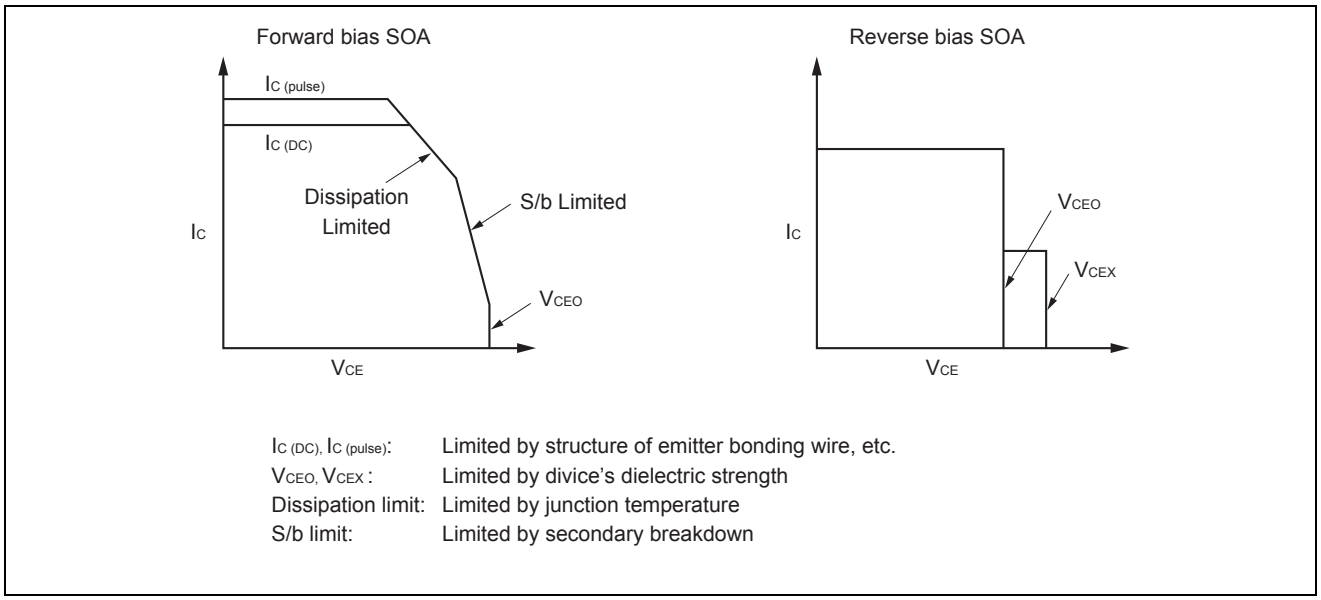


Figure 3.78 Safe Operating Area (SOA)

Secondary breakdowns include forward secondary breakdown that is observed when the transistor is operated in active area (base is forward biased) and reverse secondary breakdown that is observed when the transistor is turned off.

In the data book, the breakdown resistance values for these types of breakdowns are guaranteed based on a forward bias SOA curve and a reverse bias SOA curve.

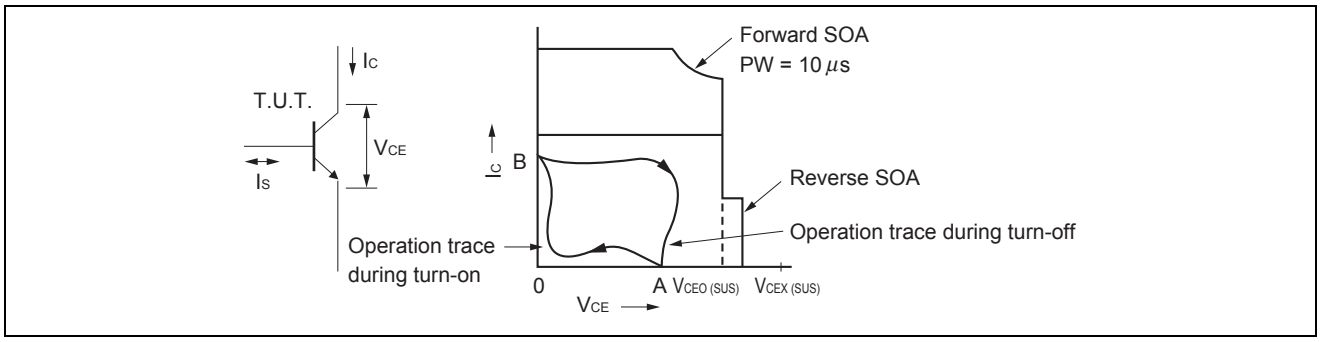


Figure 3.79 Safe Operating Area During Switching Operation

As shown in Figure 3.79, when a switching operation is performed for an inductive load in an ordinary transistor, there are operation traces from [A] to [B] during turn-on, and from [B] to [A], during the turn-off, in the cut-off area [A] and the saturated area [B].

The relative safety of switching operations can be determined by confirming whether the operation traces of the turn-on and turn-off operations are within the areas rated as the forward bias SOA and reverse bias SOA, respectively, and applying an appropriate derating as needed.

[Failure mode in forward secondary breakdown]

The base current flows from the base electrode to the emitter. At that point, current is concentrated at the periphery of the emitter and a fringing effect occurs. When current concentration occurs, the local temperature starts to rise. As the temperature rises, a positive feedback effect lowers the resistance at the warming areas, which allows more current to enter until the silicon itself melts, resulting in “hot spot” damage.

As an improvement to reduce such current concentration, some devices have a structure that also includes ballast resistors in the emitter stripe.

[Failure mode in reverse secondary breakdown]

Reverse secondary breakdowns occur when the transistor is performing high-speed operations under an inductive load. During the turn-off state, the base current is drawn toward the base electrode, but since the emitter-base junction remains in a forward biased state in the central area of the emitter, a pinch-in effect occurs where the current path remains in the central area only. This concentration of current in the remaining current path leads to a failure.

The above is a brief explanation of secondary breakdown phenomena. While resistance to forward secondary breakdowns decreases as the junction temperature rises, resistance to reverse secondary breakdowns increases at higher junction temperatures. Thus, reverse secondary breakdowns occur due to electrical instability (unevenness), and not due to thermal instability (see Figure 3.80).

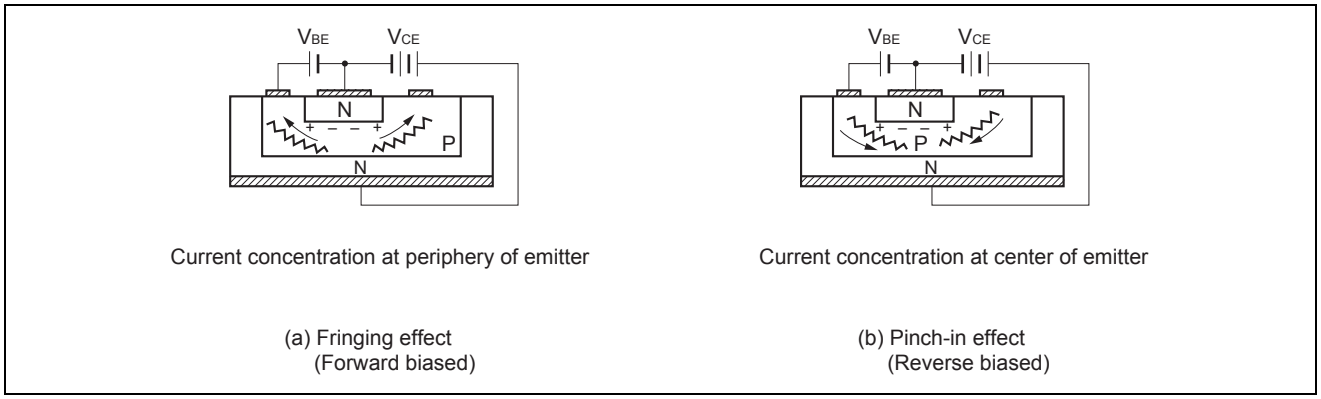


Figure 3.80 Breakdown Phenomena During Secondary Breakdowns

References:

[1] "Report on Failure Model and Acceleration Factor of Reliability Test for LSI," Reliability Center for Electronic Components of Japan, R-2-RS-02 (1990)

[2] "Report on In-process Reliability Technique for ICs," Reliability Center for Electronic Components of Japan, R-6-RS-02 (1995)

[3] E.Wu et al.: "Polarity-Dependent Oxide Breakdown of NFET Devices for Ultra-Thin Gate," Proc. 2002. IEEE IRPS, pp. 60-72

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4. Failure Analysis

4.1 Why Failure Analysis Is Necessary?

Failure analysis of semiconductor devices is necessary to clarify the cause of failure and provide rapid feedback of this information to the design and manufacturing process stages. With the demand for higher reliability in the market and the development of devices with higher integration density and larger chip sizes, advanced technologies are required to perform the failure analysis.

It is clear that reliability must be built into the device at the design and manufacturing process stages to ensure reliability. However, it is impossible to eradicate failures during the manufacturing process and at field use. Therefore it is important to strive to prevent reoccurrence of failures by quickly performing failure analysis and implementing appropriate countermeasures.

The wafer fabrication and assembly process involve several hundreds of steps using various types of materials. This, combined with the fact that devices are used in a variety of environments, requires a wide range of knowledge about the design and manufacturing processes.

4.2 What Is Failure Analysis?

The failure analysis begins when a device under observation is determined to have lost its basic functions according to the failure criteria. Failures include complete loss of functions and various levels of degradation. As the electronic equipment becoming more sophisticated, failures are not limited to individual components but also complicated failures with respect to an entire system. Failure analysis without considering these factors could result in erroneous corrective actions.

Failure analysis is an investigation of failure mode and mechanism using optical, electrical, physical, and chemical analysis techniques. Before starting the analysis, it is necessary to collect details of the failure circumstances and symptoms. This includes various investigation in electrical characteristics and other historical data leading to the failure such as operating environment, stress conditions, mounting, and possibility of human errors. These factors may suggest the potential failure mode and mechanism. Based on this assumption, the most appropriate method and procedure are determined. Insufficient information on the failure circumstances and symptoms may lead to an unsuitable choice of analysis technique, consequently waste of valuable material and time. Comparing failure devices with good devices is another technique that can speed up the analysis process.

4.3 Procedure of Failure Analysis

The most important item is to find out the failure site by a failure analysis with maintaining an electrical signal and an abnormal symptom. Recently, an analytical tool enable us to analyze logic states and operating conditions within LSIs without touching or damaging the LSIs. EB testers and LVP units are typical examples of equipment used for this purpose. These units shine an electron beam or IR laser on the sample and can obtain a logical contrast image or the dynamic waveform of a specified line without making physical contact with the device under test. Meanwhile, ongoing LSI development trends include miniaturization, multilayer interconnection structures, larger-scale integration, faster processing speed, and hybridization. All of these trends pose challenges for failure analysis. Developers of processing technologies must consider ways to enable non-destructive analysis of failures and abnormal conditions in electrical circuits. The processing technology with laser, FIB (Focused Ion Beam), and FLB (Focused Laser Beam) technique has been developed.

Advances have also been made in software-based failure analysis methods that enable failure sites to be identified without performing any physical analyses. A typical example is a method that uses abnormal logical output data from a device’s output pins to trace the logical development in reverse, back to the cause within the LSI. Another new method enables abnormal current sites to be deduced using IDDQ abnormalities (power supply current abnormalities that occur during the static state) and CAD data.

As mentioned, the analysis depends on many factors of the failure. Figure 4.1 is the flowchart of failure analysis procedure. The key is to clarify the cause-and-effect relationships at each step while working toward the next step. Failure analysis is not completed until the results of analysis can explain the abnormal operations that are occurring in the electrical circuits.

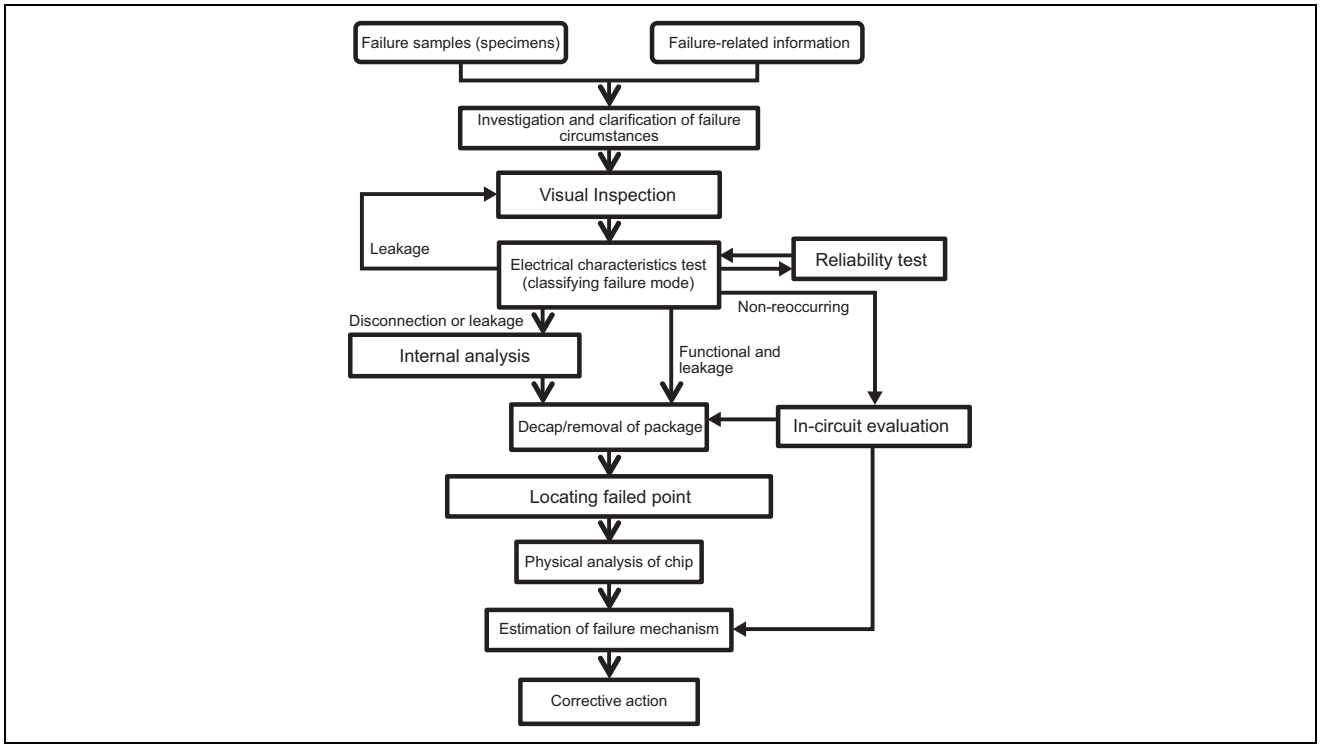


Figure 4.1 General Failure Analysis Procedure

4.3.1 Investigation and Clarification of Failure Circumstances

The circumstances of the failure must be investigated by checking the following items:

(a) Verification (production date, inventory period, and storage conditions)
(b) Production records (process conditions in wafer fabrication and assembly process, delivery date, conditions and results of acceptance inspection, conditions through mounting and/or assembly, and records of similar failures occurred so far)
(c) Conditions of use (operating conditions, thermal/mechanical stress, operating environment (indoors/outdoors, temperature, humidity, atmosphere), operating period before failure occurred)
(d) Details of failure (type of failure (degradation of characteristics, complete, intermittent), failure rate, and lot characteristics)

4.3.2 Visual Inspection

Visually inspecting the external condition of the device provides valuable information for subsequent analysis. First the device is inspected by eyes to check for any differences from good ones. Then microscopic inspections are carried out for detailed observation. A stereomicroscope with magnifying power 4x to 80x is used. Illumination from various angles is used to obtain the best view of the sample. A regular microscope with higher magnification power (10x to 1000x) is sometimes used to search for failure spots. If further observation is required to detect package cracks, surface wear, particles, whiskers, discoloration, or migration, a scanning electron microscope (SEM) is used. If elemental analysis is required and a sufficient amount of sample is available, atomic absorption photometry is performed. If the failure is limited in a very small area and it is difficult to obtain the substance in question, electron probe micro analysis (EPMA) should be used.

4.3.3 Evaluation for Electrical Characteristics

(1) Evaluation Using an LSI Tester

This test evaluates detailed electrical characteristics of the sample test equipment and sequence used in mass production and when necessary further test programs which have been created for design evaluation. The test results may suggest the failure mode, failure mechanism, and refine the estimation made from the failure circumstances. At the same time, the test enables the choice of onward analysis method, as shown in Figure 4.1.

Detailed evaluation of electrical characteristics is very important. In the case of memory devices, these tests can locate an exact failure spot on the chip.

(2) DC Characteristics Test

The DC characteristics of the semiconductor device are evaluated using a curve tracer, picoammeter, oscilloscope, and other equipment. Within an actual semiconductor device, there exist components such as parasitic diodes, that are not indicated on the equivalent circuit for the semiconductor chip, and since currents do not necessarily flow according to the equivalent circuit, it is desirable to perform this evaluation by comparing the device under test to the characteristics of a non-defective device.

(3) Logic/Failure Simulation Analysis

When a function test performed by an LSI tester or by DC characteristics evaluation results in a fail, the data obtained in the function test is analyzed to locate the faulty module in the chip. The failure mode is then examined according to the voltage, temperature, frequency, and other test conditions. A procedure that makes use of the information obtained by the analysis and examination in a logical simulation or failure simulation environment to accurately determine the faulty logical function module is generally called failure diagnosis. The accuracy of locating the failure improves if it is made possible in the failure diagnosis to identify the location of the failure in the order of 10 cells or 10 nets in the chip. There are four types of failure diagnosis methods: the failure dictionary method, which is used with a failure simulator, the tracing diagnosis method, the guided probe diagnosis method, and the IDDQ test diagnosis method.[1] [2] [3] [4] [5] The IDDQ test is a method that makes a pass-fail judgment by measuring current values in a static operating state by applying the fact that a perfect CMOS structure has no DC path on the source lines. IEEE has defined it as a quiescent power supply current in MOS circuits. This test method is a historical test method developed after the invention of CMOS.

Figure 4.2 shows a failure analysis flow based on failure diagnosis. The failure diagnosis flow roughly divides into function test failure steps and current system (DC/IDDQ) test failure steps. For a function test failure, a failure analysis is performed with a failure simulation, and the failure is located by EB testing, LVP, TRE and other types of operation analysis. For a current system test failure, light-emission analysis, OBIRCH analysis, and other static analyses are performed (for these measures for locating failures, see section 4.3.5).

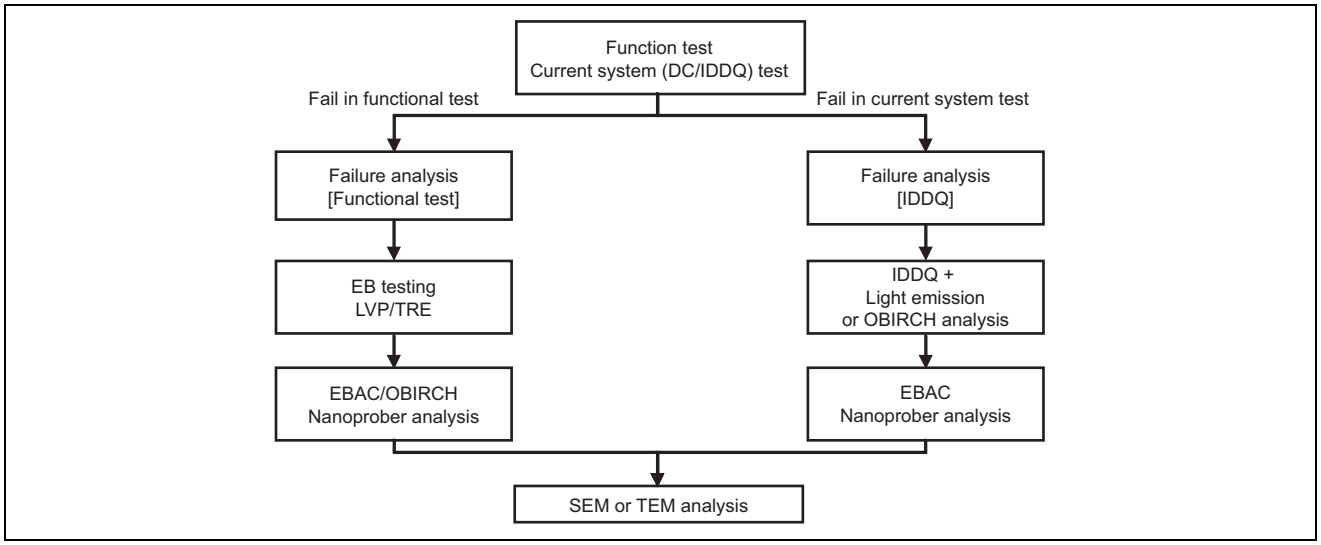


Figure 4.2 Analysis Flow with Failure Diagnosis

Figures 4.3 and 4.4 provide overviews of the failure diagnoses that we are using for function test failures and current system testing (IDDQ test failures). Function test failures require such procedures as logical analysis and failure dictionary creation for each failure condition, so analysis takes a long time. However, for faulty products that were made by external manufacturers and for malfunctions in systems already on the market, the method is effective and locating a failure spot. IDDQ test failures can be diagnosed quickly because a failure dictionary for failure diagnosis has been created. In addition, no logical and functional analysis is required. IDDQ test failures are also appropriate for hardware analysis machines and have the advantage that a failure can be located in less time than a function test failure.

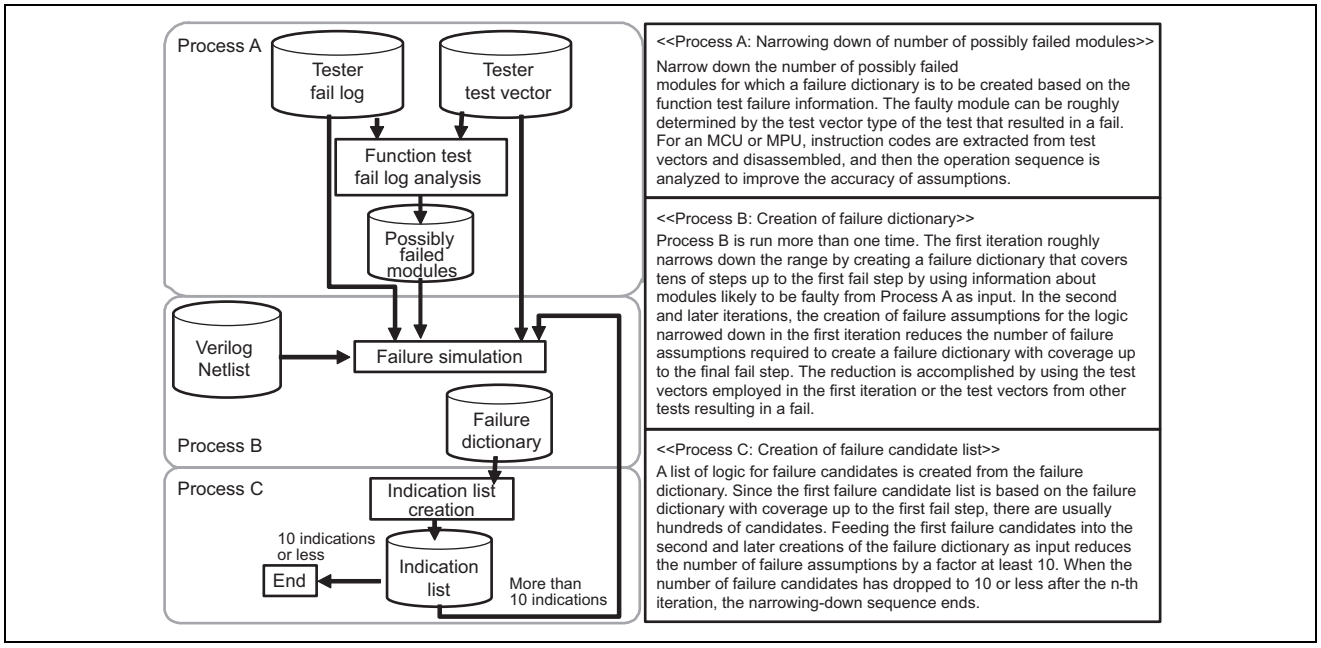


Figure 4.3 Function Test Failure Diagnosis Flow

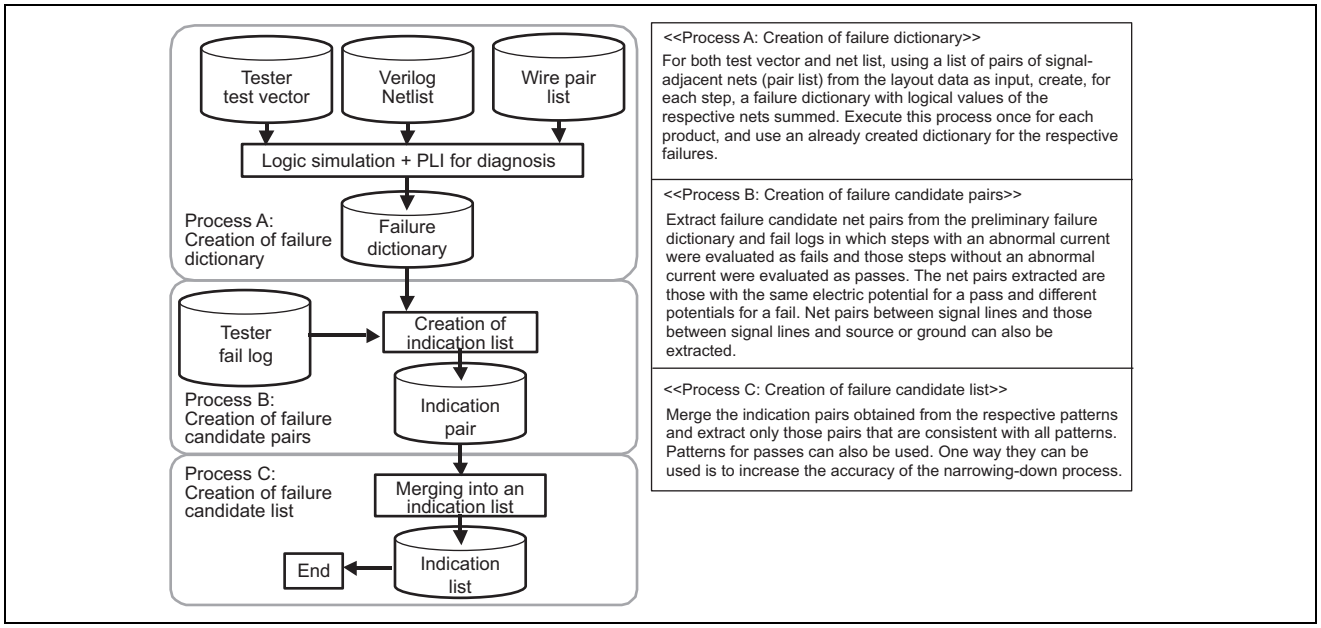


Figure 4.4 Current System Test Failure Diagnosis Flow

(4) Experiment for Failure Reproduction Using Actual Equipment

If a product is evaluated as a pass in the tests described above, an experiment must be conducted with actual equipment to reproduce the failure. It is possible that the failure cannot be reproduced because the circumstances of the failure cannot be adequately simulated in the tests. It is also possible that the failure occurred due to a problem related to use of the device (for example, a malfunction due to a circuit constant or noise). For some types of failure, an experiment with actual equipment might cause secondary damage, so care must be taken.

4.3.4 Internal Analysis of a Package

(1) Nondestructive Internal Analysis

Techniques used to check the internal state of a device without opening or removing the package include X-ray examination, infrared microscopy, and scanning acoustic microscopy. X-ray examination uses the fact that X-ray penetration varies according to the type of material and thickness (i.e., the smaller the atomic weight, the greater the penetration). The differences create an X-ray image. This method is effective for detecting foreign particles, breakage or looping abnormality of bonding wires, and voids or delamination in mold resins or the die bonding section inside the plastic encapsulated package.

Infrared light passes through silicon but is reflected by metals and mold resins. When inspecting plastic encapsulated packages, the chip is sometimes exposed by removing the plastic with a solvent. However, the solvent also removes foreign particles and wiring, which makes failure detection difficult. In the infrared microscopy, a part of the package is removed by grinding the bottom to expose the silicon chip. The infrared examination of the chip shows the state of the metal wiring and any abnormalities in the bonding pads.[6]

An ultrasonic wave divides into reflected wave and penetrating wave at a boundary between different materials. The reflected wave has different intensity and phase according to the difference of acoustic impedance of the two materials (if the acoustic impedance of the first material is higher than the second, the phase inverts).

A semiconductor device sealed in a plastic package is placed underwater, ultrasonic waves are applied to the package surface, and reflected waves are returned, one after another, from the package, chip, and lead surfaces. At places where there are voids at these boundaries, however, the intensity and phase of the reflected waves will differ from waves reflected from devices where there are no such voids. Using this effect, it is possible to determine the positions and states in which they were generated of any voids, peeling, or cracks that may exist within the package.[7]

(2) Analysis of Residual Gas

If contamination of the chip surface is suspected to be the cause of failure in metal or ceramic packages, the gas inside the casing should be investigated by opening a hole in the lid.

(3) Airtightness Test

Metal or ceramic packages are sealed with dry air or nitrogen gas enclosed to shut out the external atmosphere. Since the presence of water facilitates the movement of impurity ions and can cause degradation of device characteristics as well as corrosion of aluminum leads, the amount of water in the atmosphere inside the package is kept under several hundred ppm and gas leakage from the package is minimized. There are two airtightness test methods: helium tracer method to measure fine leaks and the fluorocarbons method to measure gross leaks.

For measuring fine leaks ranging from 10^{-8} to 10^{-9} atm • ml/s, a helium tracer leakage detector is used. It can measure leakage less than 10^{-9} atm • ml/s. For measuring relatively large leaks from 10^{-3} to 10^{-5} atm • ml/s, a fluorocarbons leakage detector is employed. A depressurization/pressurization container is required for leaks under 10^{-5} atm • ml/s.

These techniques can detect small cracks in the package, voids in welding or solder materials, pinholes in the welding flange section, and faults in the hermetic seal.

4.3.5 Fault Isolation

In failure analysis of a chip, the point of the failure is located using fault isolation techniques. Then physical analyses, including structural analysis and composition analysis, are carried out to determine the cause of the failure.

Fault isolation uses electron beam testing, LASER Voltage Probing (LVP), emission/thermal analysis, Optical Beam Induced Current (OBIC), and Optical Beam Induced Resistance Change (OBIRCH) techniques. These techniques involve emission of an electron beam onto the chip surface and detection of the light emitted from the chip surface. Therefore, the chip must be exposed without taking it out of the package. This requires some preprocessing such as disassembly of the package and removal of the chip coating.

A different fault isolation technique is used for each type of failure. Electron beam testing or LVP is used for a functional failure in which the logic generates an erroneous output. Emission analysis or OBIRCH is employed for a leakage failure with an increased power current.

Recently, the nanoprobe method, which directly measures electrical characteristics of minute circuits, and other methods have made it possible to locate a failure with more precision after narrowing down the failure location with the techniques already mentioned.[8] [9] [10] [11]

4.3.6 Physical Analysis

(1) Introduction

The physical analysis observes and analyzes the failed point by performing physical treatments on the chip. Its purpose is to clarify the cause of failure. It provides final information that is fed back to the design and manufacturing processes.

The defect, which is the cause of failure, sometimes exists between the surface and lower layers. In such a case, the dielectric film and metallic wiring must be removed. This procedure is performed while observing the spot using an optical microscope or SEM. It is sometimes necessary to observe the cross section of the chip with Focused Ion Beam (FIB). If any discoloration or particle is found at the failed location, composition analysis is carried out to clarify how it happened.

(2) Points of Observation

(a) Breaking, Short Circuit, and Leakage by Excess Voltage or Current

Abnormal external voltage or current can melt the metal wiring and polysilicon resistors. In some cases where the current is very high, the internal leads blow out. Abnormal alloy generation is occasionally observed at a PN-junction (between emitter and collector for a bipolar transistor). Other cases include dielectric breakdown of an oxide film and a short circuit between metal interconnects.

(b) Breaking of Wire Bonding

This failure is investigated by the X-ray inspection and the optical microscope inspection after decapsulating. If the wires are peeled off from the bonding, the alloy formation of the detached part and misalignment of bonding should be checked. Gold and aluminum forms various Au-Al compounds at high temperatures. As the diffusion rate of gold is slower than aluminum, mass movement between two layers shifts the boundary, which generates a hole (Hartley-kirkendall effect). It can reduce the strength of bonding, increase the resistance, and cause detachment.

(c) Corrosion of Metal Interconnection

Penetration of moisture, phosphoric acid (P_2O_5 disengaged from passivasion film) and chlorine ion, insufficient chemical treatment in process, cell effect and electric field caused by contact of different metals can corrode aluminum, which results in disconnection. In many disconnection cases, aluminum elutes completely and sometimes a short circuit occurs between adjacent wiring. Corroded aluminum often turns black. It can be easily found by observation of the chip surface using an optical microscope. This failure mode should be handled with care. Inappropriate selection of etching time, temperature, and solution when removing mold resin can promote aluminum corrosion. For this reason, plasma etching is sometimes used.

(d) Chip Cracks

Heat stress often causes cracks in a silicon chip, which results in disconnection, short circuit, and leakage. These cracks are random lines crossing the chip surface, which is sometimes missed in observation with low magnification. The passivation film must be removed to observe the cracks because cracks can be limited in this film. It becomes easy to observe with an infrared microscope, because the strain around the crack area can be more emphasized than observing with an usual microscope.

(e) Mask Misalignment

Misalignment in diffusion, contact/via holes, or metal wiring can cause various failures. To investigate this defect, the alignment of PN-junctions, contact/via holes, and wiring must be checked carefully.

(f) Contact-via Failure

This failure includes disconnection or ohmic failure at a step of a contact/via hole, and increased contact resistance due to the generation of a high-resistance layer and a closed contact/via hole caused by an inappropriate wafer fabrication process. Observation of a cross section using FIB is useful for investigating this type of failure.

(g) Particle Induced Failure

A particle on the chip surface or inside the chip can cause failure. Locating the layer where the particle exists and analyzing its composition may provide some clue to estimate the process and reason of contamination. Observation of a cross section using FIB clarifies the contaminated layer. Electron Probe Micro-Analysis (EPMA) or scanning auger microscopy (SAM) is useful for analyzing the particle contamination. However, care must be taken not to contaminate the sample further during analysis.

(h) Electrostatic Discharge

The gate oxide film of metal-oxide semiconductor (MOS) is very thin and has low dielectric resistance. Electrostatic pulses generated by a human body or inspection instruments can break the device. This breakage can be detected by the increase of input current or change in Vth. In case of a bipolar transistor, when ESD is impressed, the breakdown voltage of junction is decreased. As a result, a part of the junction melts. Other symptoms include increased leakage current, decreased breakdown voltage, and hFE, and increased noise. If the aluminum wiring at the failed point has turned black, it is easily detected using an optical microscope. For other cases, emission microscopy and OBIC are effective for locating the failed site.

(i) Electro/Stress Migration

Excess current or stress to aluminum wiring can cause a hillock or voiding. A hillock may result in a short circuit within a layer or between layers. Voiding can lead to increased wiring resistance or disconnection. It is easy to locate the disconnection spot with electron beam testing. It is also possible to locate the voiding or disconnection using heat by laser irradiation, in which changes in resistance or thermo-electromotive force of aluminum wiring are detected.[18] [19]

(j) Junction Breakdown

Stress by oxide film disengagement or abnormal growth of alloy, contamination, and crystal defects of silicon substrate can cause defective junctions. The junction is observed from the chip surface or the cross section depending on the type of failure. Wright-etching after the junction is exposed facilitates the observation.

(k) Dielectric Breakdown

Destruction of a dielectrics occurs when a strong electric field stress is applied to a transistor or capacitor block of a semiconductor device. Possible causes of the stress are external noise such as ESD, a design-based defect, a defect in the wafer process, time degradation, and other various factors. Since the symptom of a dielectric breakdown is a leakage failure, photo emission analysis, OBIC, OBIRCH, or the like are effective methods.

4.3.7 Impurity and Composition Analysis

For impurity and composition analysis of a semiconductor chip, an electron beam, X-ray, or ion beam is emitted onto the sample. Then secondary electrons, X-ray, and ions are detected and analyzed.

4.3.8 Estimation of Failure Mechanism

A careful investigation is required to determine the abnormalities discovered by various failure analysis techniques as the true cause of the device failure. The investigation must be conducted from a variety of angles to prove a consistent explanation of the device failure in terms of the electrical characteristics of the failure identified. It is rare that all of the detected abnormalities are directly linked to the failure, and an incorrect judgment results in incorrect corrective action being taken without any improvement.

As the integration density of semiconductor devices and the level of circuit complexity increase, the nature of failures has also become more complex. That makes discovering the cause of failure more difficult. Clarifying the failure mechanism requires failure verifying simulations and a database of previous failure analyses. A design to facilitate testing (analysis) at the development stage also contributes to the resolution of failure mechanism.

4.4 Failure Analysis Methods

4.4.1 SAT (Scanning Acoustic Tomography)

[Objective]

We observe the internal information of the sample (crack, void, and its location, etc.) non-destructively by using the reflected wave of the ultrasonic.

[Principle]

Figure 4.5 shows a configuration diagram of this device and describes how it produces images.

A repeated pulse voltage is applied to an ultrasonic sensor assembly that includes an ultrasonic oscillator and an acoustic lens. Ultrasound waves that are emitted from the ultrasonic sensor are reflected from the specimen's surface (including any surface defects) and return to the ultrasonic sensor. A piezoelectric element outputs the reflected ultrasound waves as voltage values to a receiver. The receiver amplifies the weak signals that represent raw data and then outputs the signals to a detector. The detector outputs DC voltage values corresponding to peak values for a section that will be converted into an image, such as by using a detection circuit (gate circuit) to process the ultrasound waves that were reflected from the surface of a bonding layer.

Meanwhile, the ultrasonic sensor is attached to a scanner which outlines (via a controller) the horizontal or vertical plane of the specimen. The A/D conversion of the above-mentioned DC voltage values is performed using the specified measurement pitch during the scanning operation, after which the converted values are processed and stored to display addresses corresponding to their original X/Y coordinates so as to provide a real-time display of scanned images, such as the above-mentioned bonding layer surface.[7]

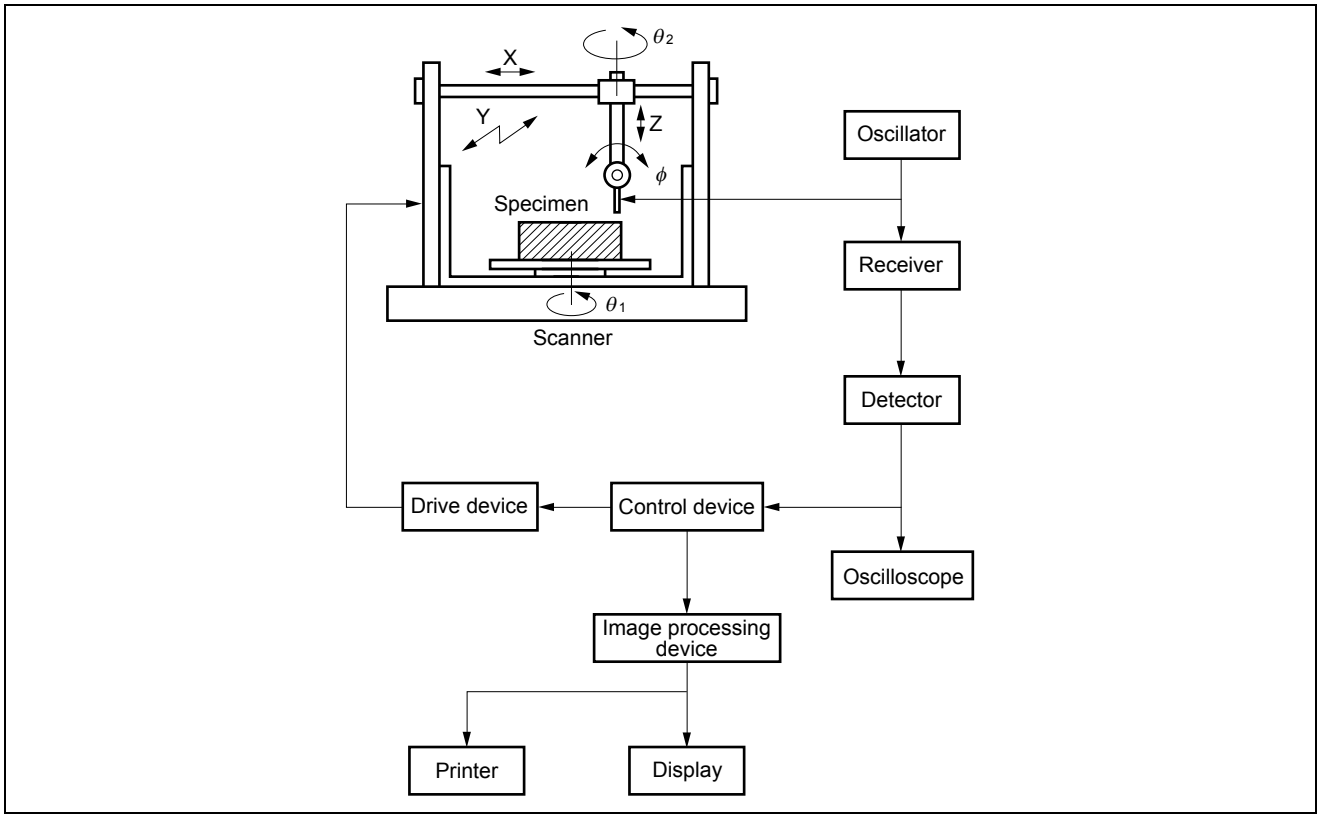


Figure 4.5 Configuration Diagram of SAT Device

[Specific applications]

- Evaluation of adhesion strength between silicon chip and mold resin (see Figure 4.6)
- Evaluation of adhesion strength between lead frame and mold resin
- Die bonding evaluation
- Observation of voids in mold resin
- Observation of package cracking
- Observation of chip cracking

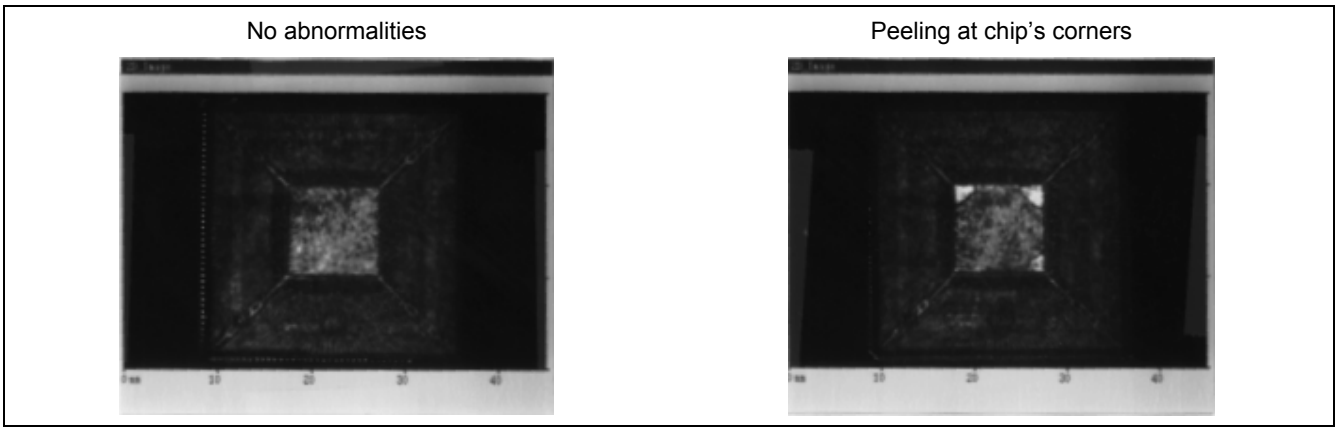


Figure 4.6 Observation Result of Adhesion Strength between Chip and Mold Resin

4.4.2 SEM (Scanning Electron Microscopy) and EPMA (Electron Probe Micro Analysis)

[Objective]

The chief objectives are to observe the condition (smoothness, etc.) of solid surfaces and to analyze the surface constituent materials.

[Function]

SEM allows researchers to easily observe three-dimensional shapes at various depths of focus and under high magnification. SEMs enable observation of defects, detailed structures, and tiny impurities that are too small to be observed using optical microscopes. An EPMA enables researchers to learn more about the constituent materials of solid surfaces (qualities of elements existing at a specified site, quantitative analysis, and distribution of specified elements).

[Principle]

An electron beam that is output from an electron gun passes through several electron lenses to become finely focused as it irradiates the specimen. The size of the electron beam can be adjusted to between several nm and a few tens of μm to suit the object being measured. As shown in Figure 4.7, secondary electrons, back-scattered electrons, and characteristic X-rays are among the objects that are reflected from the surface of the specimen. The SEM's secondary electron images are synchronized with the electron beam scanning of the specimen surface and the intensity values of secondary electrons are converted to luminance values in the monitor display. The luminance values of secondary electrons differ according to the surface smoothness, constituent elements, and surface potential. Such changes can be observed in the secondary electron images.

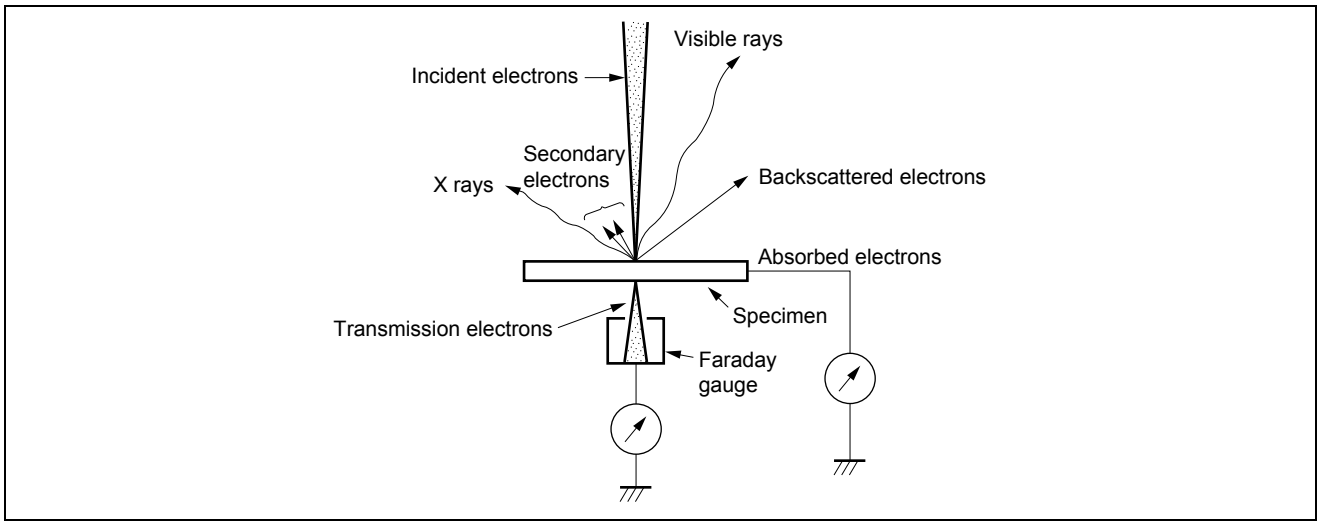


Figure 4.7 Electrons and X Rays Reflected from Surface of Specimen

An EPMA applies a tightly focused electron beam to the material to be analyzed and measures and analyzes the characteristic X-rays that are emitted from the sample surface. This allows the elements present at the sample surface to be determined. Figure 4.8 shows the mechanism of characteristic X-ray generation. When an accelerated electron strikes an atom, a hole is generated and the atom ionized with a certain probability. This ionized state is a high-energy excited state, and, for the atom to return to a stable state, an electron in an outer shell at an even higher energy level than the energy that generated the hole must fall into and fill that hole. The electromagnetic radiation generated by this process is called a characteristic X-ray. Since the characteristic X-rays are unique to each element, by identifying the elements based on the energy or wavelength of the characteristic X-rays, it is possible to determined the detailed structure of the elements present on the surface of the sample. Like SEM units, EPMA units synchronize electron beam scanning of the target surface. The characteristic X-rays of a specified element that have been detected are displayed on the monitor as numerous dots that together form a "map" showing the specified element's distribution (this is called "elemental mapping"). Researchers can also determine the concentration of the specified element by comparing the density of a pre-measured standard specimen with the specimen.[12]

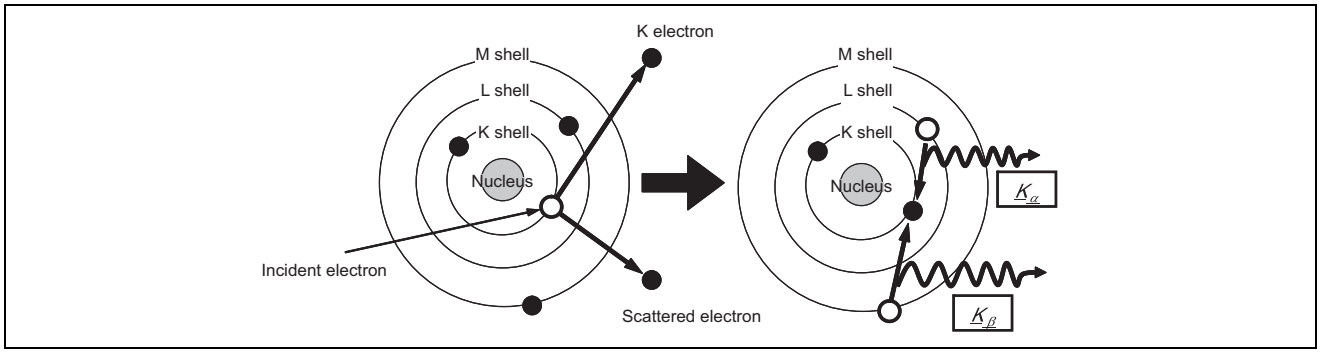


Figure 4.8 Characteristic X-Ray Generation Mechanism

[Analysis example]

Figure 4.9 shows the mapping of the distribution of various elements in a defective section of an Al wiring pattern. One can see that there are large amounts of Al, Ti, and N in the part of the pattern that is defective. After performing the EPMA analysis of this defect, it was determined that foreign material consisting of Al, Ti, and N was adhering to the Al wiring by FIB cross sectional analysis.

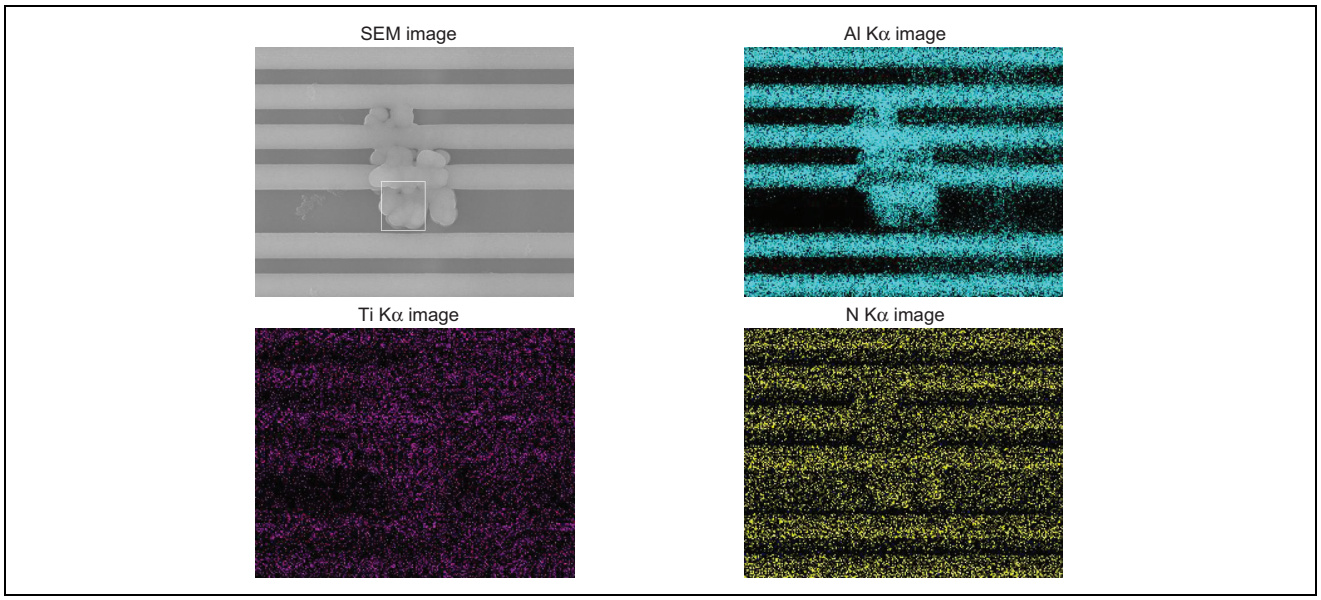


Figure 4.9 EPMA Analysis Results for an Al Wiring Pattern Defect

4.4.3 EB Tester (Electron Beam Tester)

[Objective]

An electron beam is used for detecting logical information (potential contrast images, logical operation waveforms) on the LSI device in the vacuum chamber, driven by an LSI tester.[13] (see Figure 4.10)

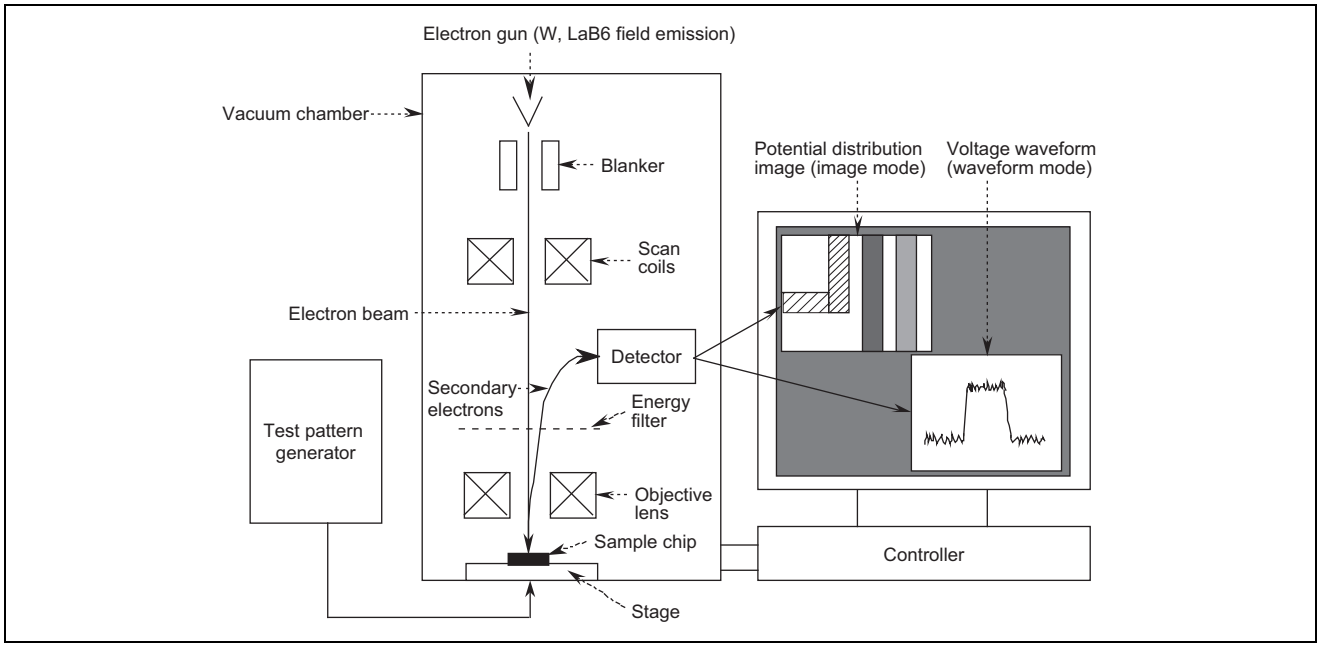


Figure 4.10 Outline Drawing of EB Tester

[Function]

(1) Potential contrast images: A potential contrast image corresponding to the potential differences among the wirings can be viewed [14] (black = high potential, white = low potential) (see Figure 4.11).

(2) Logical operation waveforms (voltage waveforms): Waveforms can be obtained like a conventional sampling oscilloscope. For example, waveforms can be obtained and examined. Comparing an input signal waveform and its related output signal waveforms [15] (see Figure 4.12).

Using the functional features described above, Renesas has developed new analytical methods that are easy-to-use and efficient. One of these methods is the CGFI (Continuous Gated Fault Imaging) method, which is used to quickly obtain potential contrast images having high S/N ratios. Another method is the AFI (Activated Fault Imaging) method, that can blinkedly highlight the fault signal propagated portions, which guide the operator to the failing cell location.

(3) CGFI method: A continuously emitted primary electron beam is used to effectively eliminate charge-up phenomena and prolonged gate pulses generate rich signal so that high-contrast potential contrast images can be quickly obtained.[16]

(4) AFI method: Only the wiring through which failure signals propagate can be blinked and monitored by using the CGFI method on marginal defective LSIs, such as voltage margin, while switching acceptable product condition and defective product condition at high speeds [17] (see Figure 4.13).

Furthermore, with the improved accuracy in semiconductor chip rear surface processing technologies (such as mechanical grinding, laser, and FIB), approaches to measurement from the chip rear surface are studied.[18] [19]

[Principle]

When electrons emitted from an electron gun are irradiated onto the surface of an LSI, secondary electrons are generated. The quantity of secondary electrons is a constant, but their energy distribution varies according to the potential, so logic states can be inferred once the energy distribution has been identified. Relative to the GND potential, the curve on the left in the Figure represents the energy distribution for a positive potential and the curve that is shifted to the right represents the energy distribution for a negative potential. If a potential barrier is attached between the LSI and the secondary electron detector, only those electrons that have enough energy to cross the barrier reach the detector. This means that the LSI's potentials can be compared relatively based on a comparison of detected secondary electrons. (see Figure 4.14)

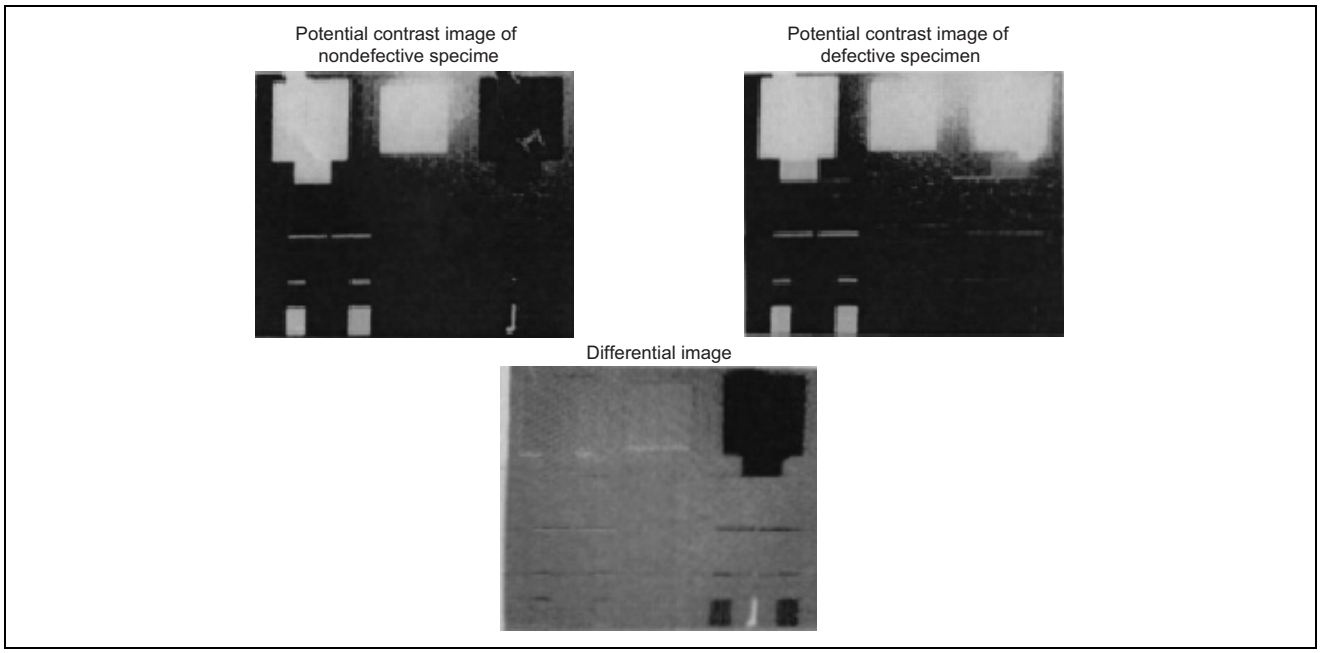
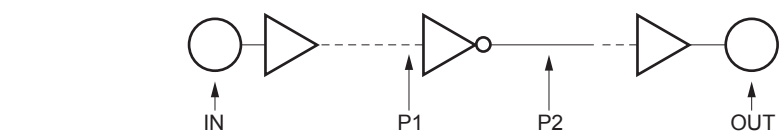
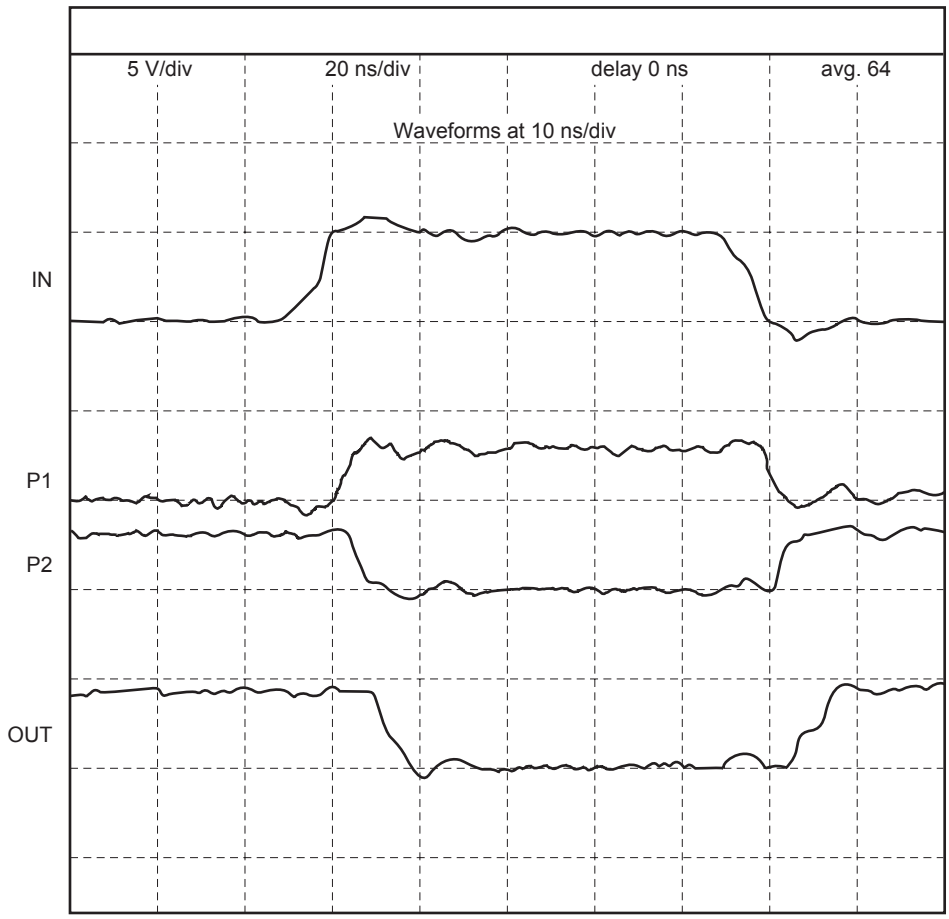


Figure 4.11 Potential Contrast Images





Changes in logical operation waveforms in CMOS circuit
IN, OUT: Observed on upper part of bonding pad
P1, P2: Observed on passivation layer

Figure 4.12 Logical Operation Waveforms

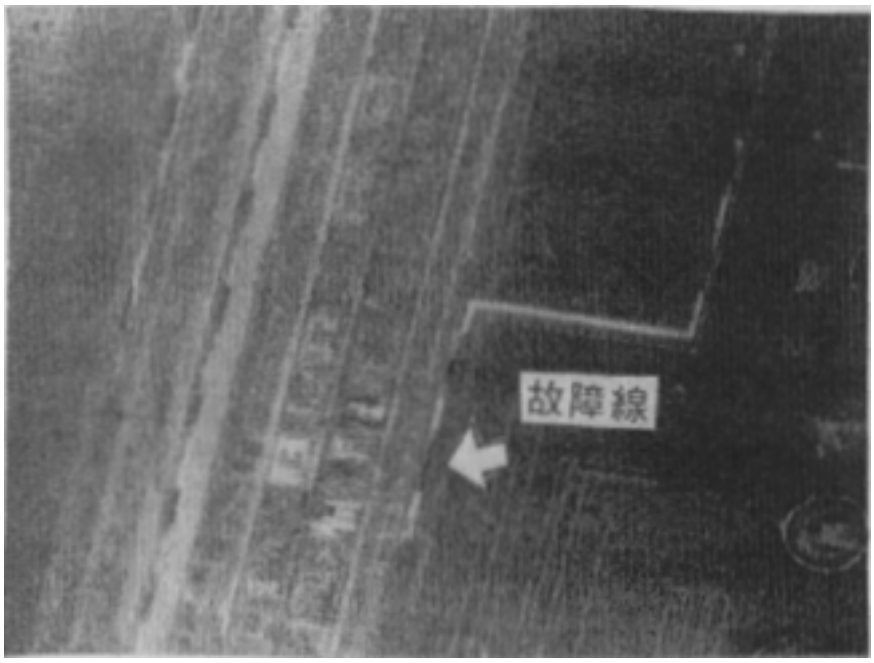


Figure 4.13 AFI Image

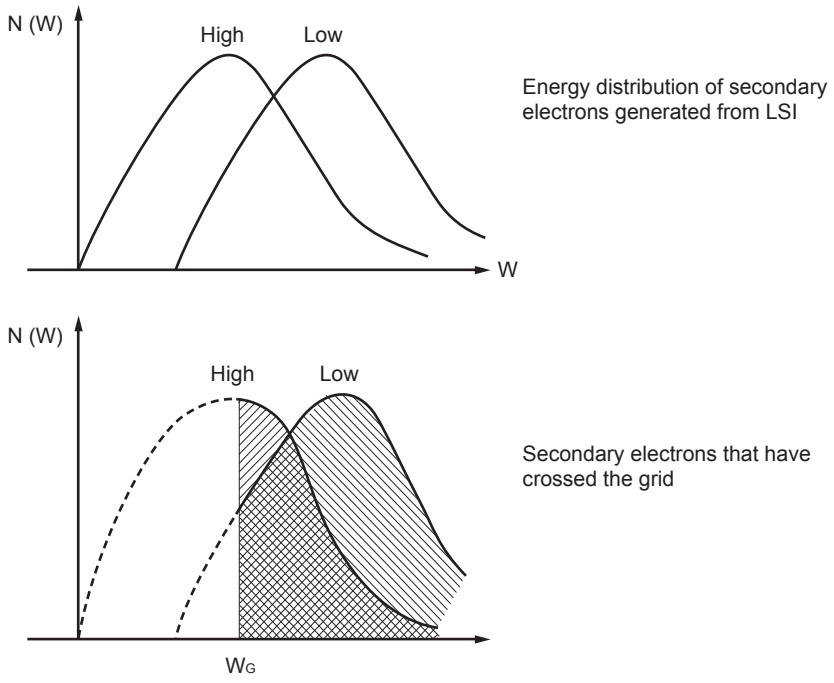


Figure 4.14 Energy Distribution of Secondary Electrons

4.4.4 Laser Voltage Probing (LVP) and Time Resolved Photo Emission Microscopy (TRE)

[Objective]

These methods are used for observing operational timing from the chip bottom surface of a flip-chip device or multilayer interconnection device whose waveforms are unobservable using an electron beam tester.

[Function]

Like the EBT method, these methods make possible no-load, high-impedance measurement with an LSI tester or equivalent tool while the device is operating as well as, among other things, high accuracy measurements for waveform timings (frequency band: up to 9 GHz).

(1) Laser Voltage Probing (LVP)

This method can measure potential waveforms and timings optically from the chip bottom surface of a flip-chip device or multilayer interconnection device whose waveforms are unobservable using an electron beam tester.

(2) Time Resolved Photo Emission Microscopy (TRE)

After the chip bottom surface has been mirror-polished to about 100-µm thickness, the TRE method can capture subtle near-infrared emissions in the order of picoseconds that occur at transistor switching (status transition) from the bottom surface of a silicon substrate to measure operational timing.

[Principle]

(1) Laser Voltage Probing (LVP):

After the bottom surface of a chip has been mirror-polished to about 100-µm thickness, the LVP measurement method is used to penetrate pulsed near-infrared laser beams of 0.5-0.7 µm in diameter (1,064-nm wavelength) from the bottom surface of the Si substrate into the operating transistor diffused layer (drain) and to detect the light that is reflected (Figure 4.15). When an electric field is applied to a pn-junction, the bandgap degrades and the incident laser absorption increases, after which the reflected light intensity decreases (Franz-Keldysh effect).

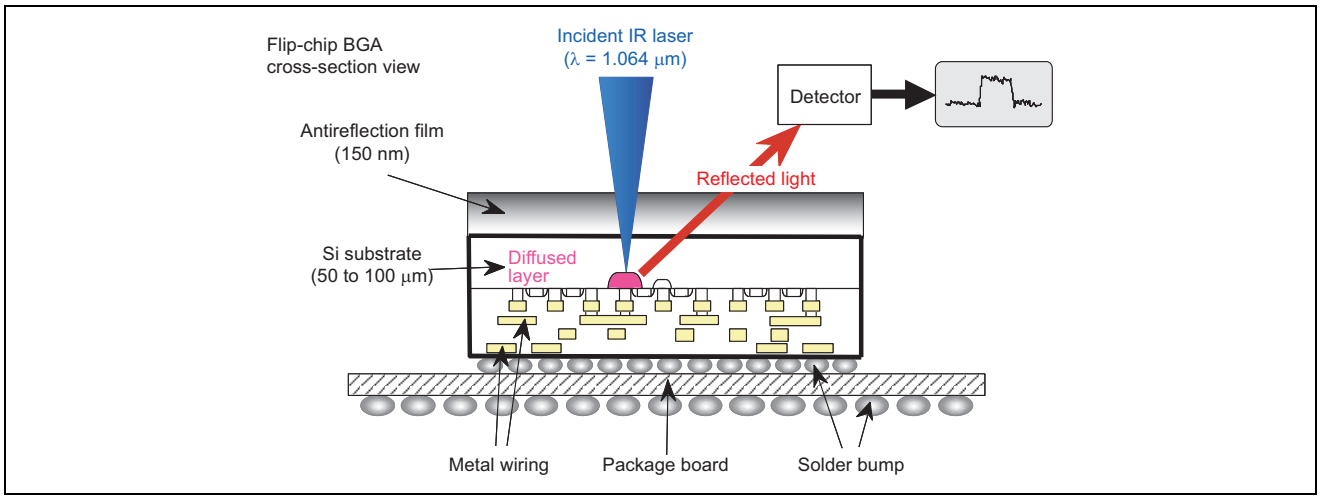


Figure 4.15 LVP Principle

Moreover, a phase difference occurs in the reflected light due to a change in carrier density from the potential difference of the pn-junction. Detecting changes of phase difference and reflected light intensity by the Franz-Keldysh effect makes possible contactless measurements of potential waveforms in the transistor diffused layer inside the chip.[20] [21]

Laser scanned images are used for pattern observation and probing (Figure 4.16), but like EBT, LVP allows information about waveforms and logic and timing to be obtained (Figure 4.17). Therefore, comparison with expected values is required to locate a failure. A CAD navigation tool linked with the layout and net information needs to be used to trace the transistor and narrow down the range of possible failures.

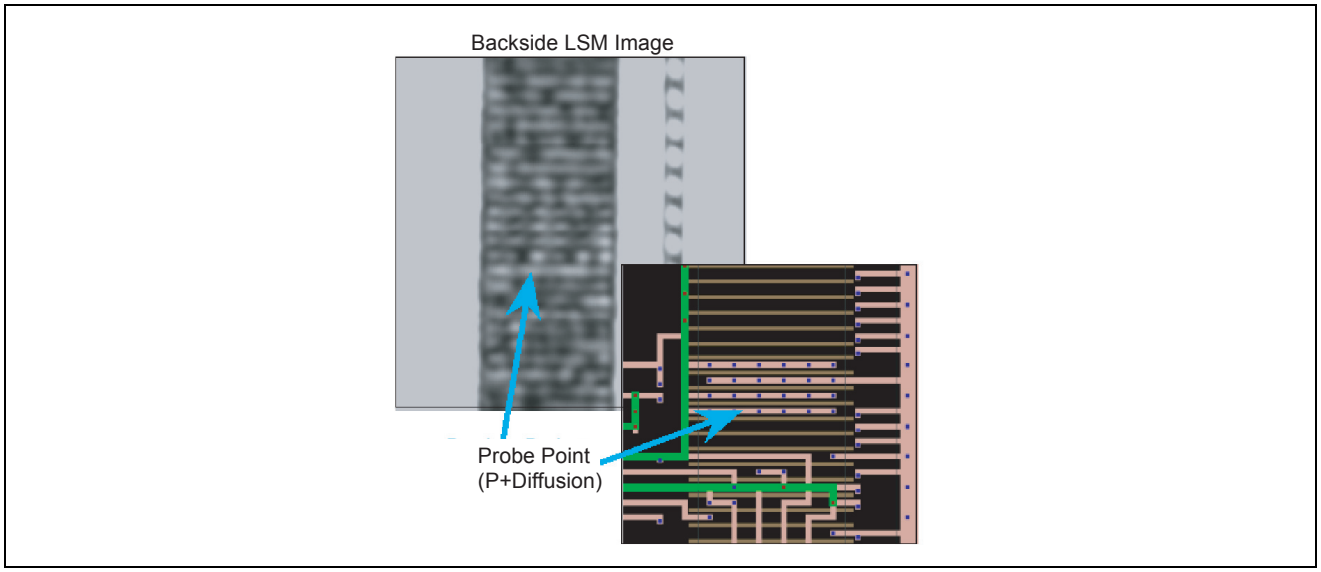


Figure 4.16 Laser Scanned Image/Layout

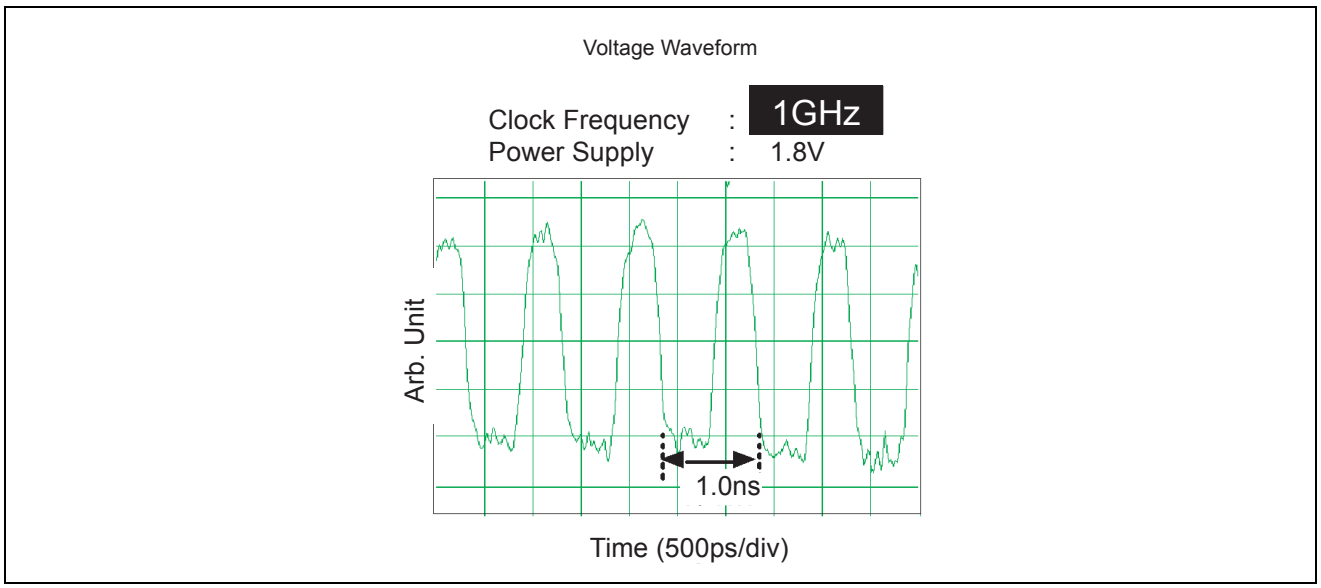


Figure 4.17 LVP Potential

(2) Time Resolved Light Emission (TRE) Analysis:

After the chip bottom surface has been mirror-polished to about 100-µm thickness, photons that leak slightly from the bottom surface of a silicon substrate are captured by an ultrasensitive time-resolved infrared camera with a quantum efficiency of about 60%, while the condensation effect of a SIL (solid immersion lens, NA = 2.45) is employed for greater sensitivity and spatial resolution (Figures 4.18 and 4.19).[22] [23] TRE allows data about emission intensity to be obtained when switching occurs (and not data about signal waveforms that EBT and LVP provide). This data indicates the timing of transistor operation. Like EBT and LVP, TRE requires a comparison of values with the expected values to locate the failure. A CAD navigation tool linked with the layout and net information needs to be used to trace the transistor and narrow down the range of possible failures.

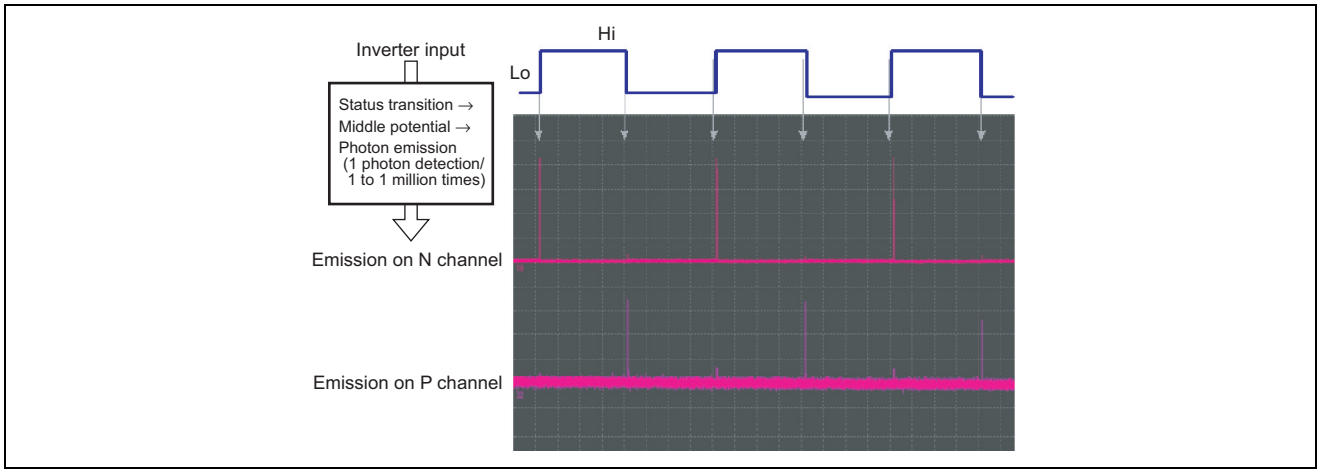


Figure 4.18 TRE Waveform for n-ch/p-ch Transistor

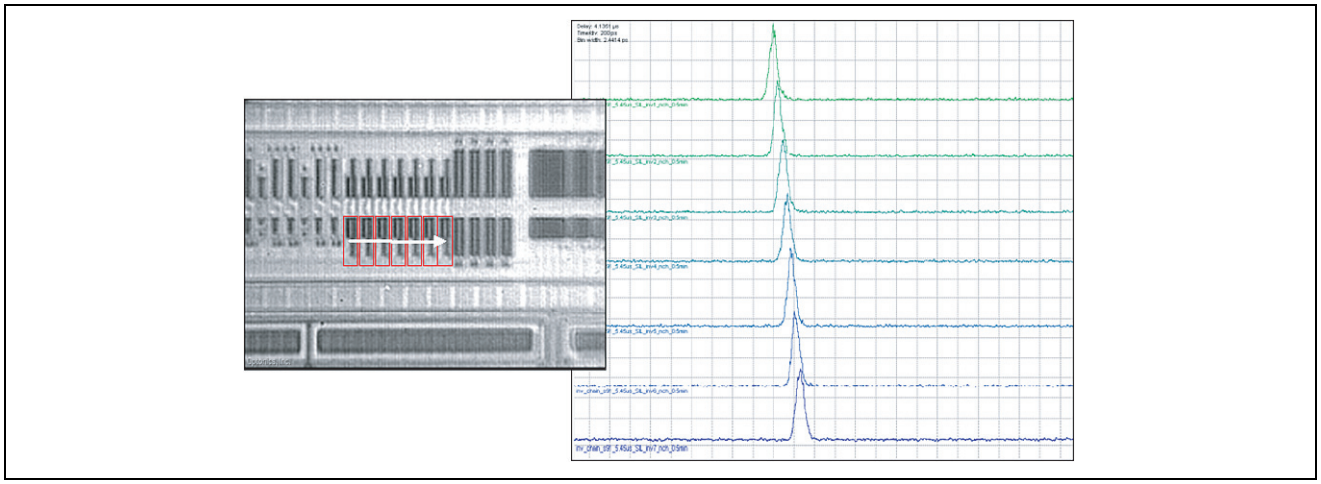


Figure 4.19 SIL-Employed Inverter Chain TRE Waveform Measurements

4.4.5 Liquid Crystal Analysis

[Objective]

A coating of liquid crystal is applied on top of an LSI. A polarizing microscope is then used to observe changes in the crystalline structure of the liquid crystal that occur in response to the temperature and electric field conditions on the LSI.[24]

[Function]

(1) Detects sites where leakage or shorting defects occur due to heat generation. This method is used to detect the abnormal IDDQ sites and ESD/EOS-related breakdown sites.

(2) Displays potential contrast images created by changes in liquid crystal's crystalline structure due to changes in electric field. This method is mainly used to detect open (unconnected) sites.

[Principle]

(1) Detection of Hot Spots in LSIs

Liquid crystal undergoes a phase transition when its temperature is raised. Its optical properties change from double refractive to isotropic. These changes can be observed using a polarizing microscope. There are two methods for detecting very slight hot spots. Figure 4.20 shows the detecting method and Figure 4.21 shows the detection result.

— First method

This method requires the LSI specimen to be kept at a temperature below the temperature where changes occur in the crystalline properties of the liquid crystal (this temperature is called the phase transition temperature or Tc). Contact with the LSI rear surface is made via a temperature-controlled metal plate for heat-conduction (such as aluminum). This method enables control of the LSI's temperature within 0.1°C and provides leakage sensitivity on the order of several μWs.[25] [26]

— Second method

After the liquid crystal undergoes a forced phase transition, a natural cooling process is used to lower its temperature back below the phase transition point. This method uses the sensitivity at the time when the liquid crystal is being cooled to below the phase transition point. The leakage sensitivity provided by this method is on the order of a few tens of μWs.[27]

(2) Display of Potential Contrast Images Indicating Liquid Crystal's Crystalline Structure Changes Caused by Electric Field Changes

Liquid crystal is sandwiched between the target LSI and an electrically conductive plate. After a potential is applied between the LSI and conductive plate, the LSI is operated. At that point, an electric field differential occurs between the potential value generated within the LSI and the potential of the conductive plate. This electric field differential causes the structure of the liquid crystal phase to change, which in turn causes optical changes in reflected images. These optical changes can be detected as colors.

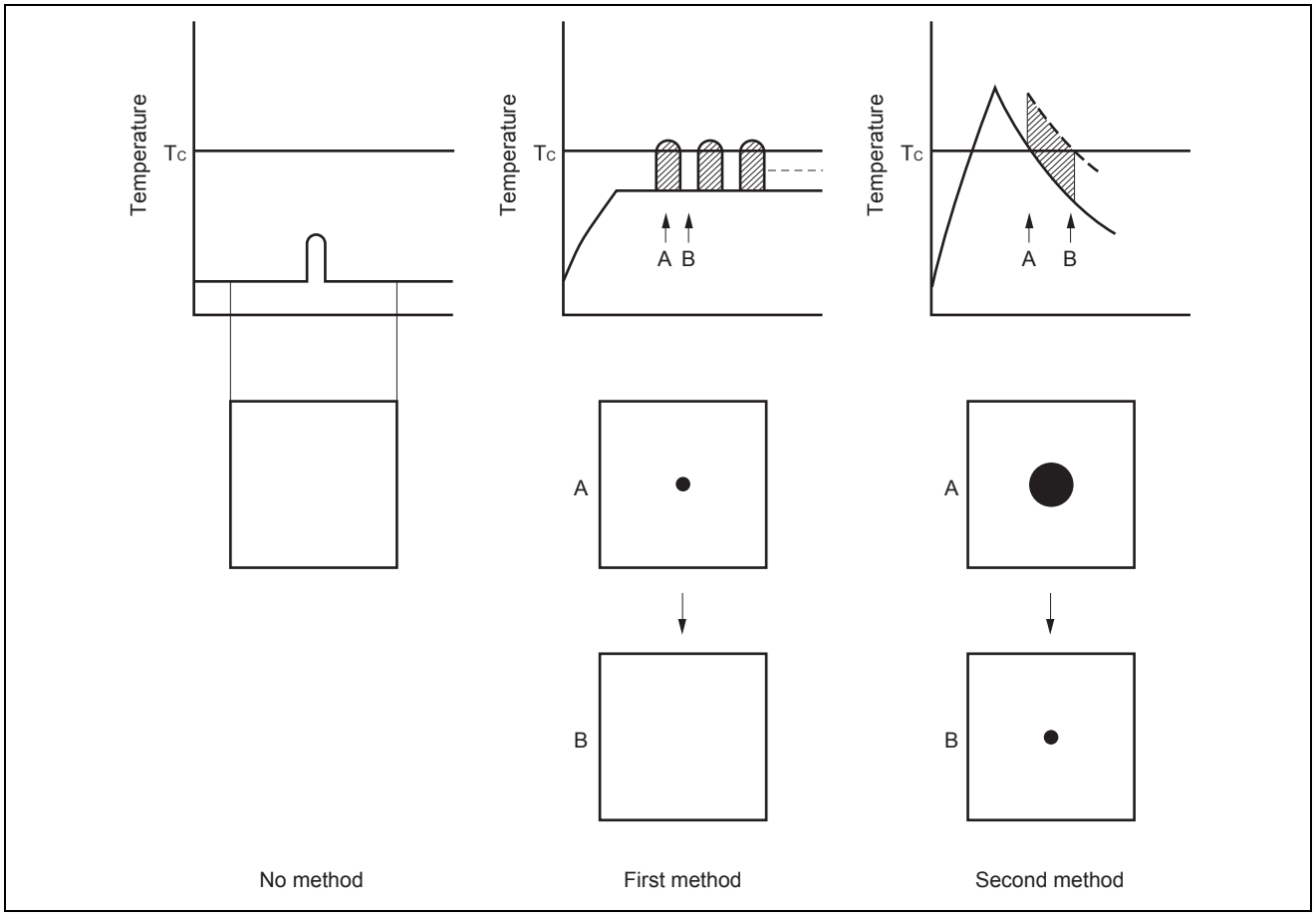


Figure 4.20 Method for Detection of Slight Hot Spots

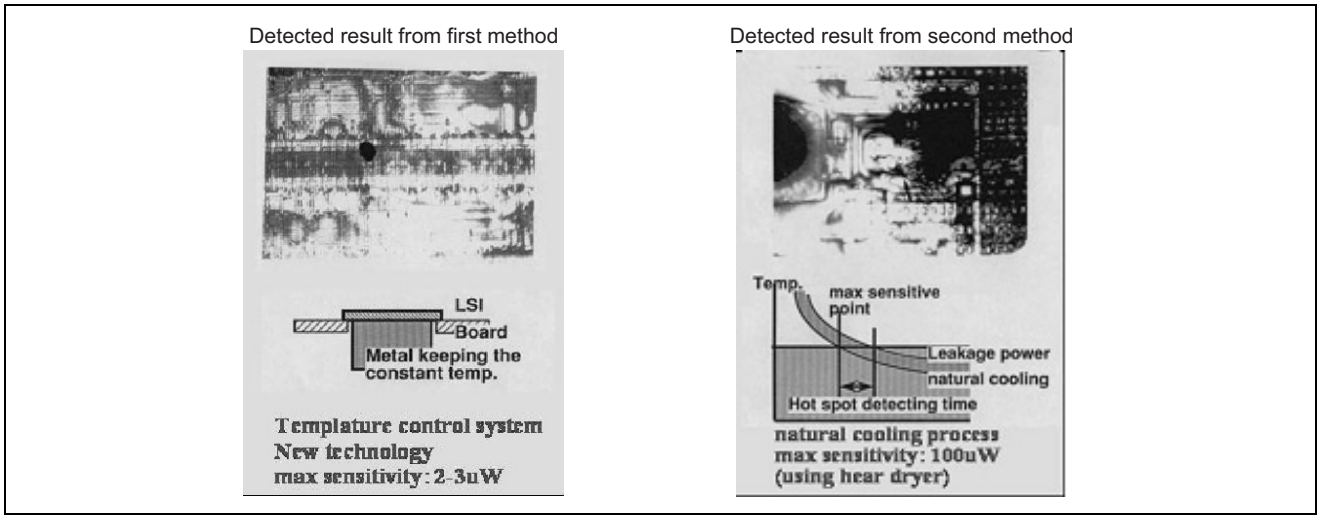


Figure 4.21 Detected Result of Slight Hot Spots

4.4.6 Photoemission Microscopic Analysis

[Objective]

This device detects photoemission phenomena that occur when a voltage is applied to an LSI. This device detects small photoemissions with a highly sensitive detector, stores them, overlays them on optical images, and then outputs them on a monitor to detect an abnormal location.

[Function]

(1) Detection of sites where hot carriers occur
(2) Detection of dielectric layer and pn junction failure sites (shorting, leakage)
(3) Detection of photoemissions due to recombination of minority carriers when pn junction is forward biased
(4) Detection of latchup sites
(5) Observation of photoemissions during a function's operating state (when linked to LSI tester)
(6) Observation of photoemissions from rear surface
(7) Spectral analysis of photoemissions

[Principle]

When junction leakage or dielectric layer defect occurs, application of a voltage will cause an electric field to become concentrated at the failure site, which generates hot carriers. A detector is used to detect the photons that are discharged when recombination occurs. This detector includes a highly sensitive near-infrared camera with a built-in image intensifier as well as a high-sensitivity high-resolution cooled CCD camera. In addition to being sensitive enough to detect individual photons, the near-infrared camera provides a gate function for capturing rapid transient phenomena and a function that enables real-time observation of changes in photoemission. The CCD camera is sensitive across a wide range of wavelengths (from 300 to 1,100 nm) and is able to provide high-resolution pattern images. Very weak photons that are detected by this detector are treated as secondary photon images.[28] [29] [30] [31] By outputting these images to a monitor as overlay images on pattern images, it becomes possible to identify the photoemission sites.[32] (See Figures 4.22 and 4.23.)

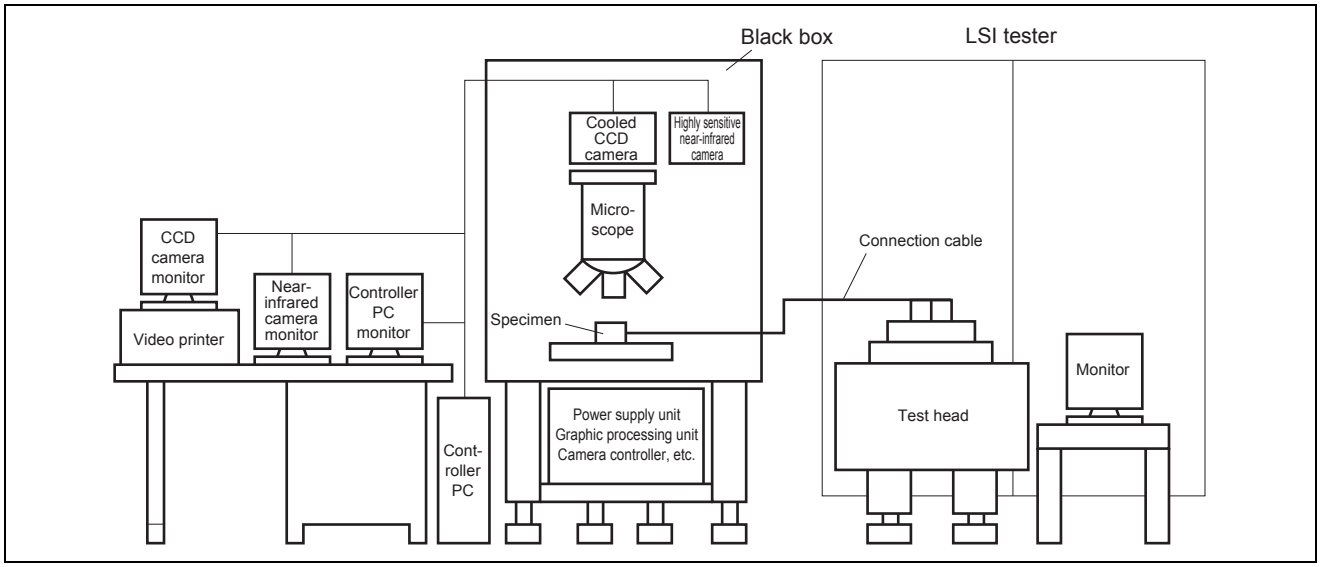


Figure 4.22 Outline Drawing of Photoemission Microscope System (When Linked to LSI Tester)

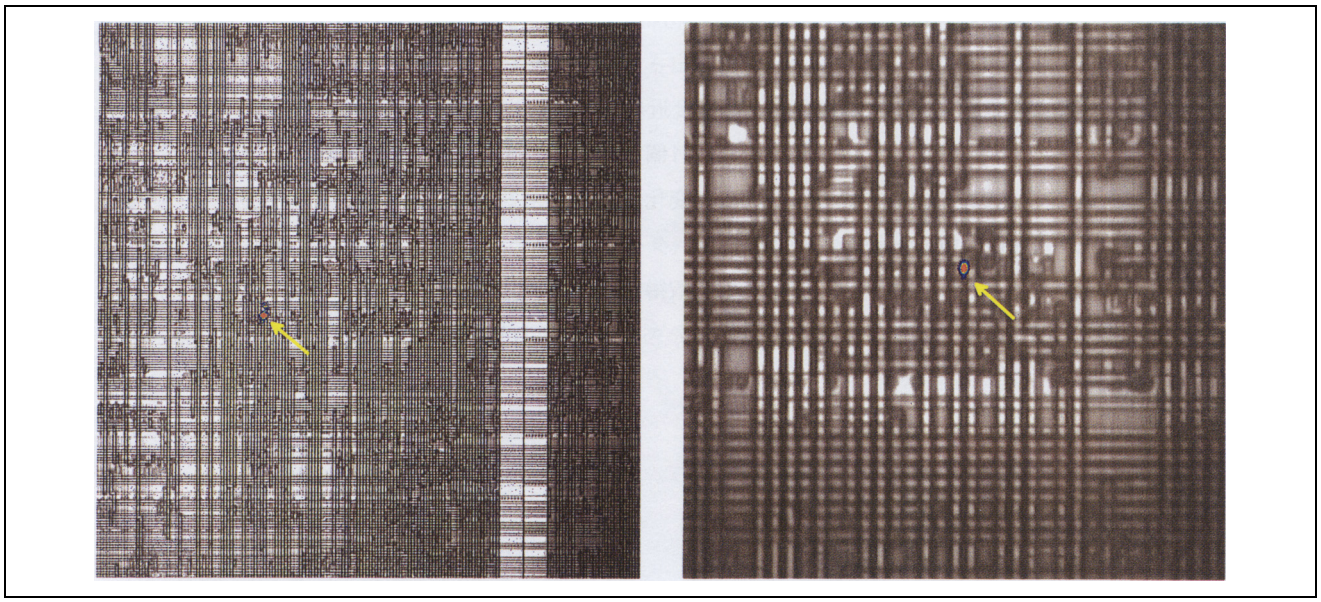


Figure 4.23 Emitted Photon Observation Examples

4.4.7 OBIRCH (Optical Beam Induced Resistance Change) Method

[Objective]

This method is basically used for non-contact analysis of interconnects on LSI chips, but it is sometimes used to detect substrate-related failures, depending on the causes of those failures.

[Function]

There are two different functions. These functions can be used not only on the chip's front side but from the rear surface as well.[33] [34] [35] [36]

(1) Detection of Current Path in Devices with Defects Which Cause Power Supply Current Increase, I/O Leakage Current Increase, etc.[37] [38] [39] [40]

Images of current flowing as DC current can be observed.

(2) Detection of Abnormalities Including Voids, Silicon Precipitation, and Parasitic High-Resistance Layers[41] [42] [43] [44] [45] [46]

This method enables detection not only of voids on metal surfaces but also voids and silicon precipitation that are buried in the metal layer. It can also detect voids in and around vias, as well as very thin (a few nm) high-resistance layers that are formed at the bottoms of vias.

[Principle]

The specimen is heated by a laser beam, after which the current changes produced by this event are observed and the two functions described above can be used. A detailed description is given as follows.

While a constant voltage is being applied to the specimen, a laser beam is used to scan the area being observed while power supply current changes in the scanned area are displayed on the monitor as changes in brightness. The displayed brightness increases and decreases as the current increases and decreases. When the laser beam irradiates the metal, the metal temperature rises, which raises the resistance value. As a result, a decrease in current is observed. This enables the interconnects which current flow to be shown as a dark area in contrast to surrounding areas. Since the momentary temperature rise that occurs when the laser beam irradiates a site having defects (voids, silicon precipitation, etc.) that degrade thermal conduction in the interconnect material is greater than the momentary temperature rise that occurs when the laser beam irradiates a site where no such defects are present, the greater temperature rise causes a greater increase in resistance and a greater reduction in current, so that the defect site is shown as a dark image. The parasitic high-resistance layers that occur at the bottoms of vias often have negative temperature characteristics. Consequently, when the laser beam irradiates one of these layers, resistance decreases and a bright image is displayed corresponding to that site.

An ordinary OBIC (Optical Beam Induced Current) device is used to implement the OBIRCH method. However, the sensitivity must be higher than that required for detecting ordinary OBIC signals. Figure 4.24 shows a configuration example for this system. This system is available in two types: a type that uses a visible laser (wavelength: 632.8 nm) and a type that uses a near-infrared laser (wavelength: 1,300 nm). Although higher spatial resolution can be obtained from the visible laser type, to make this system suitable for actual devices other than TEG (Test Element Group), some way must be devised. If the OBIC current is allowed to flow as a power supply current, the OBIC signals will interfere with the OBIRCH signals and will prevent OBIRCH images from being displayed. Devising a way to prevent OBIC current flow is very difficult, however. If a near-infrared laser (wavelength: 1,300 nm) is used instead, no OBIC signals will generated, which makes the system easily suitable for actual devices. Using a near-infrared laser also facilitates observations from the rear side of the chip: even if the chip is not a thin chip, about half of the laser beam will still reach the interconnects.

The surface of the specimen is scanned by a He-Ne laser (632.8 nm, 2 mW to 20 mW) that has been set to its minimum beam diameter (0.43 μm). In digital terms, the scan width is 512 × 512 pixels, and the dwell period for each pixel is about 2 μs, so that each scan takes about 0.5 seconds. Usually, an integration factor of 10 to 20 times is required to obtain a high-quality image. One step of a digital scan at maximum magnification (3,600, visual field: 35 μm × 35 μm) is approximately 0.068 μm. There are three types of current change detectors: one has a maximum conduction capacity of 200 mA and a current change detection resolution of 400 nA (when the S/N ratio is 2), the second has a maximum conduction capacity of 100 mA and a current change detection resolution of 1 nA, and the third has a maximum conduction capacity of 20 mA and a current change detection resolution of 100 pA.

The infrared laser devices use a laser diode (1,300 nm, 500 mW) that emits beams that can be focused to diameters ranging from 1.87 μm (theoretically, 83% of the total energy falls within this range when the visual field is 112 × 112 μm) to 21.1 μm (when the visual field is 5 × 5 mm). Scanning is an analog operation requiring about 5 seconds per scan. In cases where the S/N must be raised, an integration factor of up to 16 times is used. Images are captured as 512 × 512 pixels.

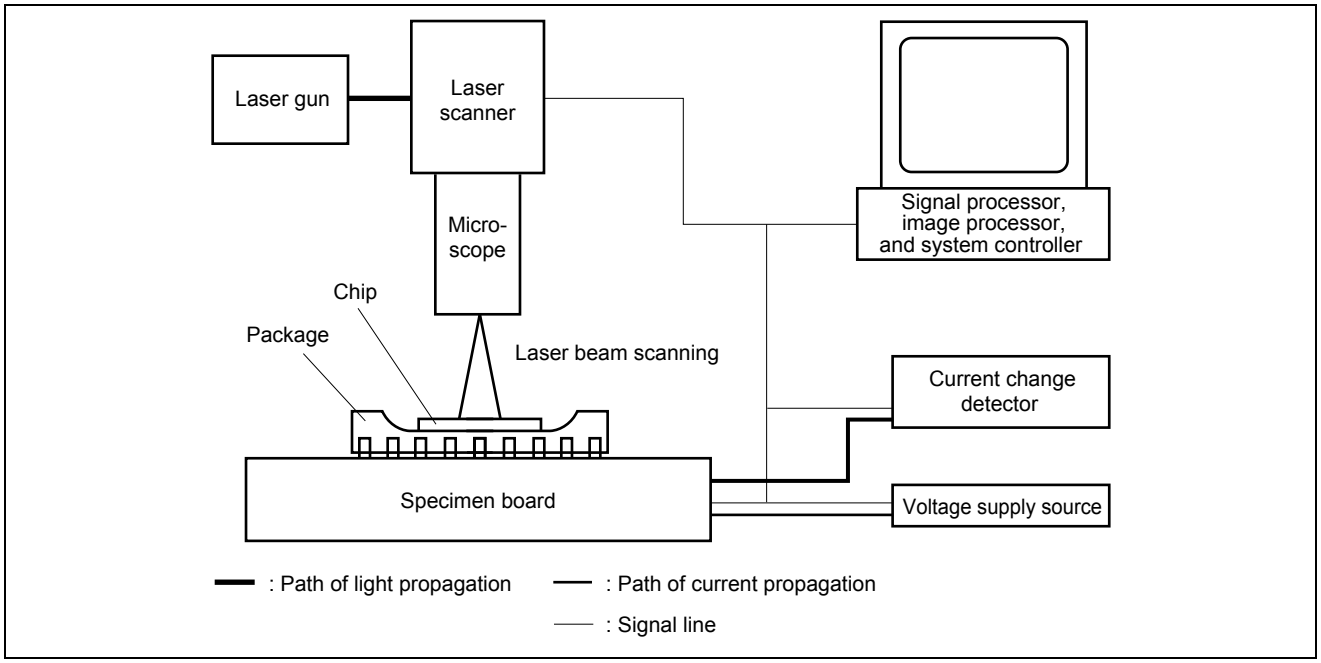


Figure 4.24 Configuration Required to Implement OBIRCH

[Analysis examples]

(1) Detection of Current Path in Device with Power Supply Current Defect

Figure 4.25 shows an example of a current path that was detected on the rear side of a chip. A near infrared laser system was used in this case. After the current path was detected within a wide visual field (5 mm × 5 mm), the device was set to a higher magnification to check the defect site. In this example, the wiring width is approximately 1.5 µm and the current that flows on the wiring has a value of about 1 mA. Note that although the beam diameter is approximately 20 µm when scanning the 5 mm × 5 mm area, it is still possible to observe current flowing on a line that is about 1.5 µm wide. There have also been examples in which current flowing on a line that is about 0.4 µm wide has been observed.

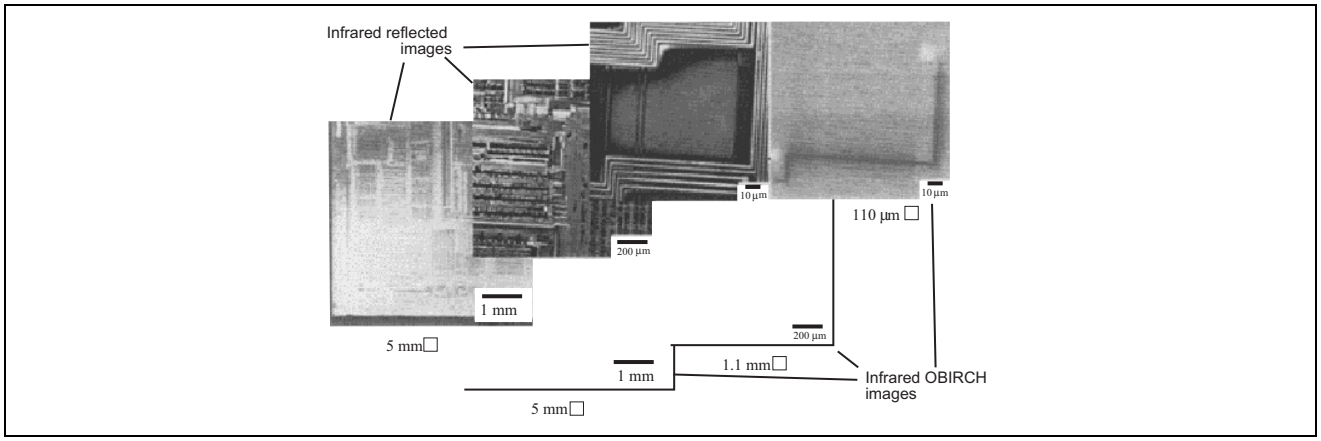


Figure 4.25 Current Path Observation Example

(2) Detection of Defects (Voids, Silicon Precipitation, Parasitic High Resistance Layers, etc.)

Figure 4.26 shows an example in which a visible laser system was able to detect voids created by electromigration.

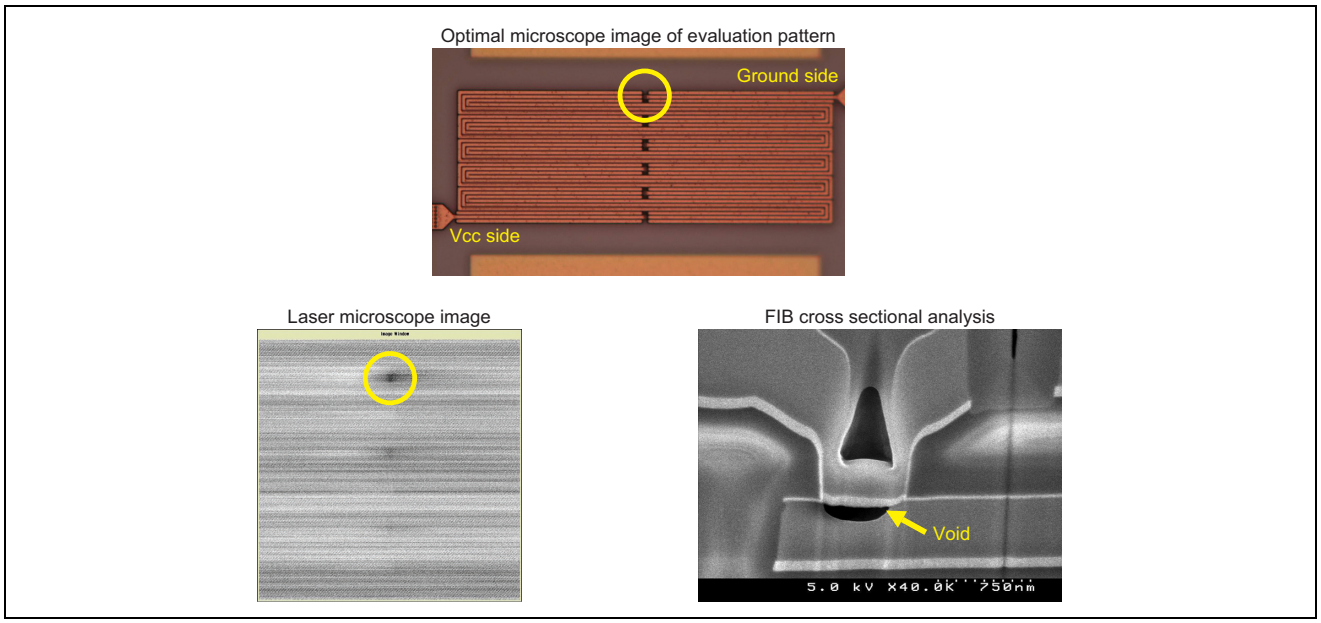


Figure 4.26 Example of Detected Voids in Via

4.4.8 Failure Analysis Techniques that Use IDDQ Abnormality Images

[Objective]

The objective is to use these techniques to investigate LSI power supply current-related phenomena in order to select defective products and localize fault sites without logic operation error. Renesas has developed testing and failure analysis techniques by these phenomena.

[Function]

These techniques can be applied to localize the fault portion and substituted to LSI testing and accelerated testing. A detailed description is provided below.

[Principle]

IDDQ (quiescent VDD supply current) phenomenon is a signal to present a physical damage in an LSI circuit (see Figure 4.27). While test vectors are applied to input, IDDQ values are measured for each vector and the abnormal signals are detected.

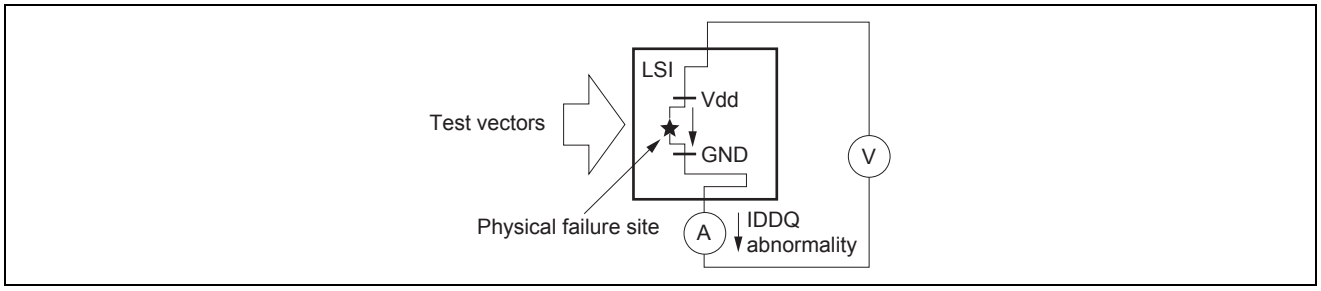


Figure 4.27 Penetration Current from VDD to GND Passing Through Physical Damage

(1) Testing

IDDQ test which is added to logical operation tests is applied to detect the fault of modes overlooked by logical operation tests alone and to compensate the fault detection rate logical operational testability. With increasingly high integration scales, IDDQ test has been indispensable.

Renesas has been involved in IDDQ tests from early on. Today, Renesas is working to develop new applications for IDDQ testing.

Figure 4.28 contains a graph that indicates the general relation between devices with logical operation defects and items with IDDQ defects. Note that while almost all logical operational errors are detected by IDDQ tests, but abnormal IDDQ defects are not always detected by operation tests. Renesas has been established the efficient IDDQ testing methods by studying characteristics of vector composition and by calculating toggle ratio of all test vectors.[47] [48] [49] [50] [51] [52]

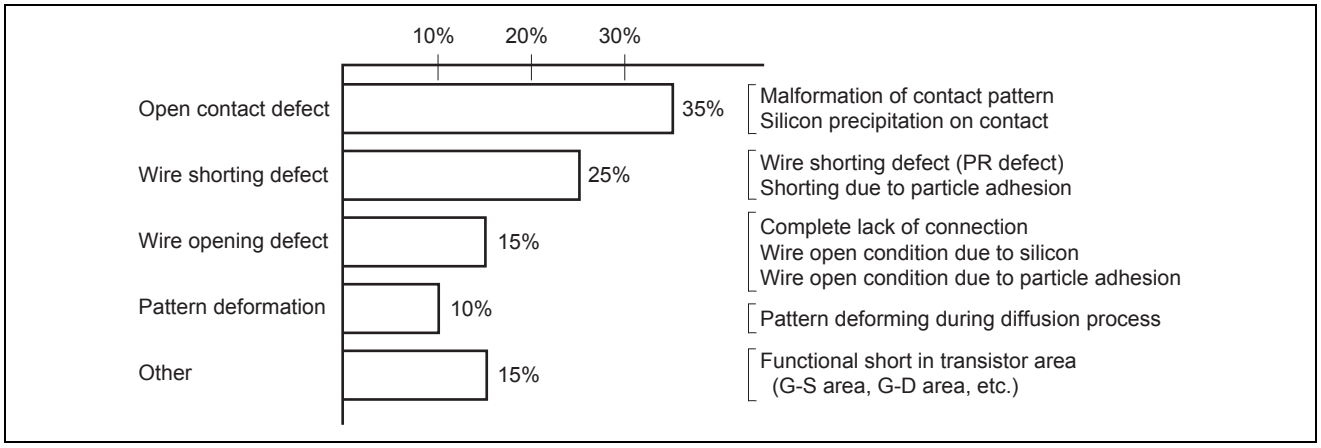


Figure 4.28 Graph of General Relation for Devices with Logical Operation Defects and Items with IDDQ Defects

(2) Application to Accelerated Testing

IDDQ tests has been studied to eliminate devices with early failures. Conventionally, such devices are screened out by the screening process. The basic reason for this application of IDDQ testing is that early failure devices detected under the accelerated tests (with higher temperature and voltage condition), have a latent fault mode and denote the significant difference of IDDQ values among the sound devices.

(3) Failure Analysis (Application to Physical Analysis)

These techniques are finding greater use in failure analysis as techniques for detecting physical failures.

Because IDDQ failure sites bring abnormal photon, abnormal heating, and abnormal current, and these phenomena make it easy to detect leakage sites. Emission microscopes (see 4.4.6 above) are typically used to detect photons and the liquid crystal coating method (see 4.4.4 above) is typically used to detect hot spots, while the OBIRCH method is used as a visual detection method for abnormal current paths. Improvements have been made in all of these methods, which has raised their analytical precision. Accordingly, Renesas's failure analysis flow starts with detection of IDDQ defects before going on to more detailed analyses.

(4) Failure Analysis (Localization of Failure Sites Through CAD Tools)

Advances in layout pattern configurations, package structures, and multilayer interconnect structures have made it more difficult to expose LSI surfaces in order to detect failure sites. Consequently, there has been an urgent need for failure site detection methods that do not rely on physical analysis. In response to this need, Renesas has developed a failure site detection method that uses IDDQ failure phenomena in a CAD application. This method includes algorithms specifically designed for detecting failure sites based on CAD (design) data and test vector data related to abnormal IDDQ. Currently, Renesas is preparing this method for practical use (see Figure 4.29).

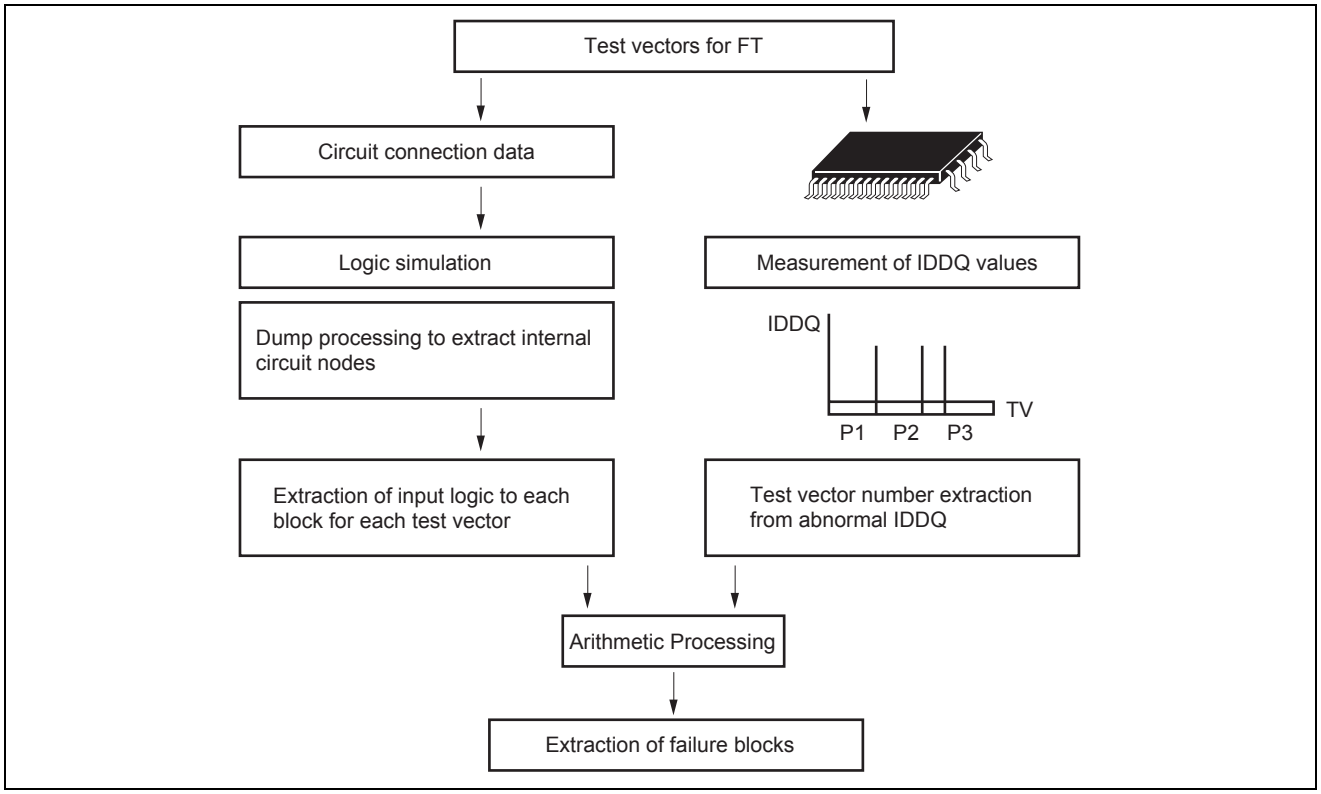


Figure 4.29 Failure Site Detection Method Using CAD Data and Test Vector Data for Abnormal IDDQ

4.4.9 AES (Auger Electron Spectroscopy)

[Objective]

AES (Auger Electron Spectroscopy) is a method for analyzing the top surface layer of very small areas. This method is used to examine the constituent materials in thin films, surface/boundary structures, diffusion of elements, particle components, residual dielectric layers on bonding pads, discoloration of leads, and impurities found between layers.

[Function]

(1) All elements except H and He can be detected. Detection limit ranges from 1 to 0.1 at% (atomic percent).

(2) Thin-film surfaces (to 5 nm depth) can be analyzed.

(3) Extremely small areas by focusing electron beam (the latest equipment model has a minimum electron beam diameter of approximately 20 nm) can be analyzed.

(4) The depth profile can be measured by the sputter etching.

(5) The one and two dimensional distribution of target elements can be measured by scanning with the electron beam.

(6) In some cases, atomic combinations can be inferred from Auger peak formations and energy shifts.

[Principle]

AES uses the Auger electrons that are discharged when a specimen is irradiated with an electron beam. Electron energy values can be used to identify or quantitatively analyze chemical elements. Auger electrons are discharged via the following process, which is called the Auger transition process.

(1) An electron beam ionizes inner-shell electrons from atoms in the specimen, which generates core holes.
(2) The core holes absorb outer-shell electrons. When that happens, energy equivalent to the energy differential between the core hole and the outer-shell electron is discharged.
(3) The discharged energy excites another outer-shell electron, causing it to be discharged from its atom. This discharged electron is called an Auger electron. The energy of Auger electrons being measured ranges from 50 to 2,000 eV. Auger electrons that are able to escape the specimen occur at a depth of about 5 nm from the surface. To detect these Auger electrons, AES uses an ultra-sensitive analytical method for the top surface.

[Example of analysis]

Figure 4.30 shows an example of the depth profile measured using sputter etching function of AES after it etches mechanically until the polysilicon of the gate electrode material is exposed. In this example, a gate oxide layer having a depth of 11 nm was detected.

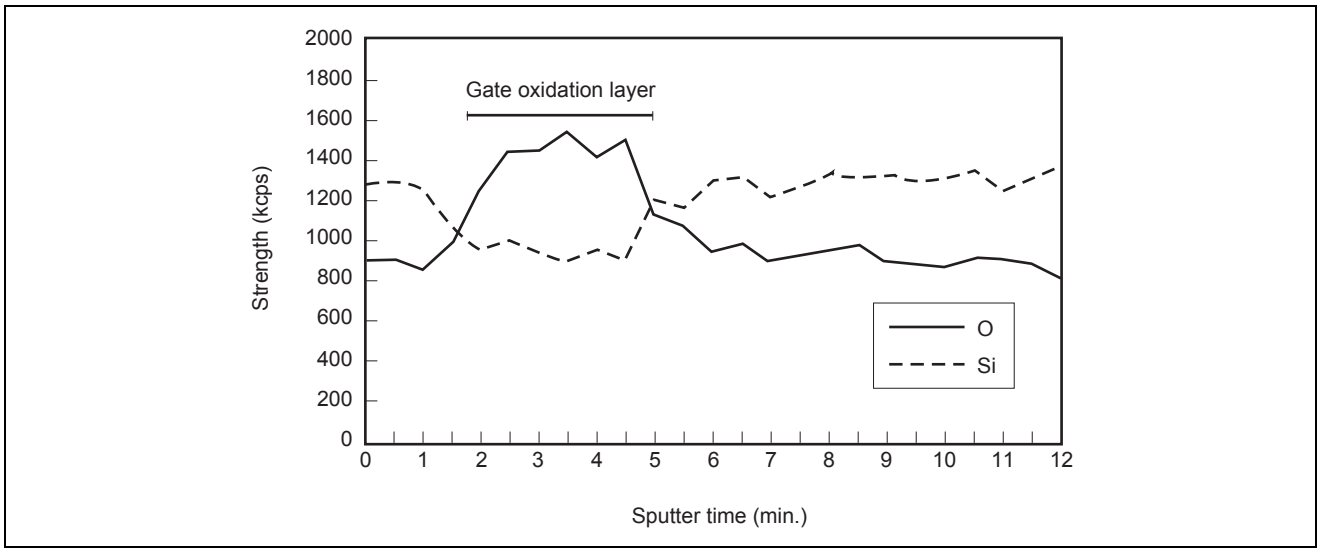


Figure 4.30 Depth Profile of Gate Oxide Layer

4.4.10 FT-IR (Fourier Transform Infrared Spectroscopy)

[Objective]

FT-IR (Fourier Transform Infrared Spectroscopy) is mainly suited for analysis of high-polymer substances such as rubber, paper, plastic, fibers, cloths, and adhesives. For semiconductors, this method is used to analyze impurities that are inside or on top of the silicon wafer.

[Function]

Infrared spectroscopy is an indispensable method for analyzing the structure of organic compounds. This technology is particularly noted for its ability to obtain motion-related information, such as elasticity or deformation vibration of the polymer functional group.

The generally used type of FT-IR device is able to very quickly make highly sensitive measurements of the spectral phenomena in the target area and to obtain high-resolution spectral data for highly precise wavelength values. It can also measure specimens that have very little mass or low permeability.

[Principle]

When a specimen is irradiated with an infrared beam, light is absorbed selectively (only in certain wavelengths). An infrared absorption spectrum can be obtained by recording the strength of an infrared beam that has permeated the target substance as the vertical axis and the infrared wavelength as the horizontal axis. Like fingerprints, each infrared absorption spectrum is unique to the measured substance, which makes it very useful as a means of identifying substances. Since the wavelengths around which certain types of component structures are absorbed are already known, this technology enables researchers to use spectrum data to determine the chemical structure of previously unknown substances.

As shown in Figure 4.31, an infrared beam is emitted from a light source and strikes a semi-transparent mirror (a beam splitter), where it is split in two directions. These two beams of infrared light are reflected by mirrors (a fixed mirror and a moveable mirror) and meet again at the semi-transparent mirror. While these measurements are being taken, the moveable mirror is moved back and forth so that a different optical path results in comparison to the fixed mirror. The differential between infrared beam's two optical paths is used as function for creating an interferogram. The interferogram are again split in two directions. One of the interferogram returns to the light source and the other penetrates the specimen and reaches the detector. At the detector, the electrical signals corresponding to the interferogram undergo Fourier transform processing via a computer to produce an infrared spectrum. The usual measurement method starts by measuring the background spectrum before setting up the specimen, then the specimen is set and the spectrum is again measured. The specimen's infrared spectrum is obtained by calculations based on a comparison of the two measured spectra.

The main analytical methods related to FT-IR technology include the thin-film transmission method, attenuated total reflectance (ATR) method, liquid ATR method, diffusion reflectance method, infrared microscopy method, GC/FT-IR method, and photo-acoustic spectroscopy.

The following are brief descriptions of two of these methods that are used relatively often: the attenuated total reflectance (ATR) method and the infrared microscopy method.

- Attenuated total reflectance (ATR) method

  The purpose of this method is to analyze the surface of the specimen. It is used for thin-film analysis and for cases in which the specimen's absorption strength is too strong to disable a good spectrum to be obtained via the thin-film permeation method (due to saturation).
- Infrared microscopy method

  An infrared microscope is used to perform transmission and reflection measurements of a small area (about 20 μm wide). This method is used to identify impurities that are introduced during production processes. In such cases, measurements can be made with almost no preprocessing of the specimen required.

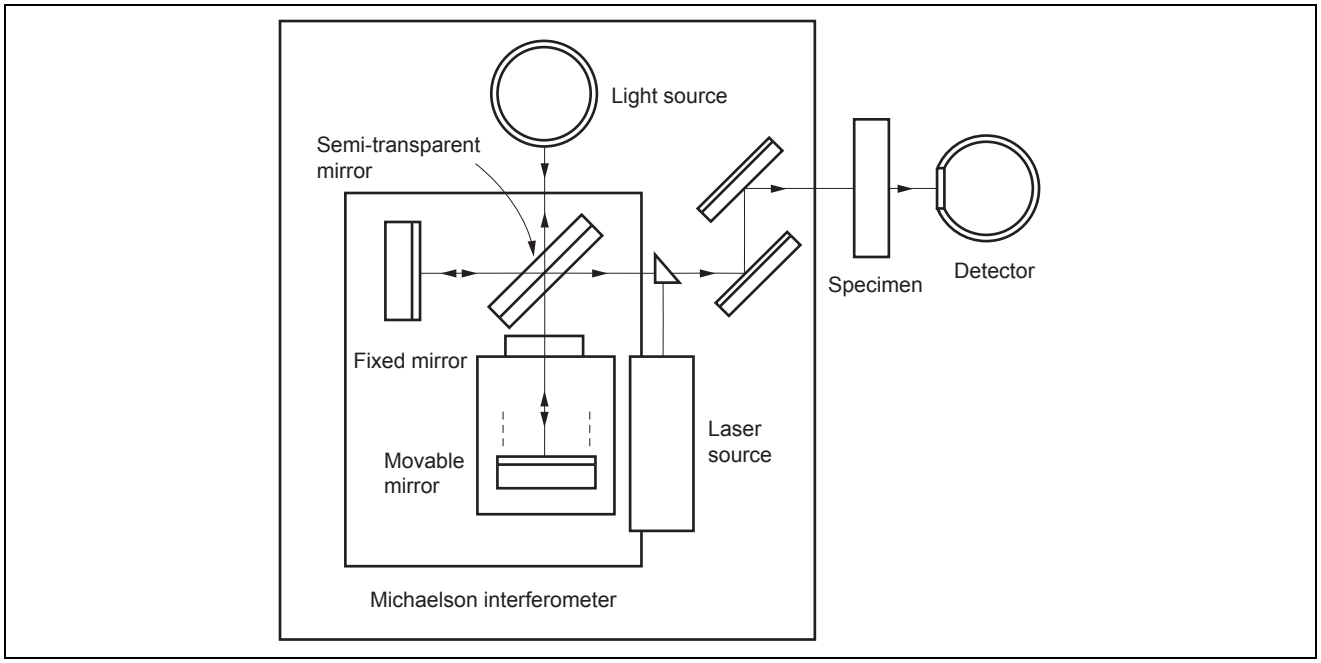


Figure 4.31 Configuration of FT-IR System

[Example of analysis]

(1) Evaluation of Si-H in Structure of SOG Layer

Figure 4.32 shows the result of a study of the optimum baking temperature of an SOG (Spin On Glass) layer. This study used FT-IR technology to measure the Si-H reduction trend that occurs when the SOG layer is under bake conditions. Temperature changes at the peak elasticity and vibration values for Si-H are shown in the figure. It is evident that higher baking temperatures result in fewer Si-H compounds and lower peak strength values.

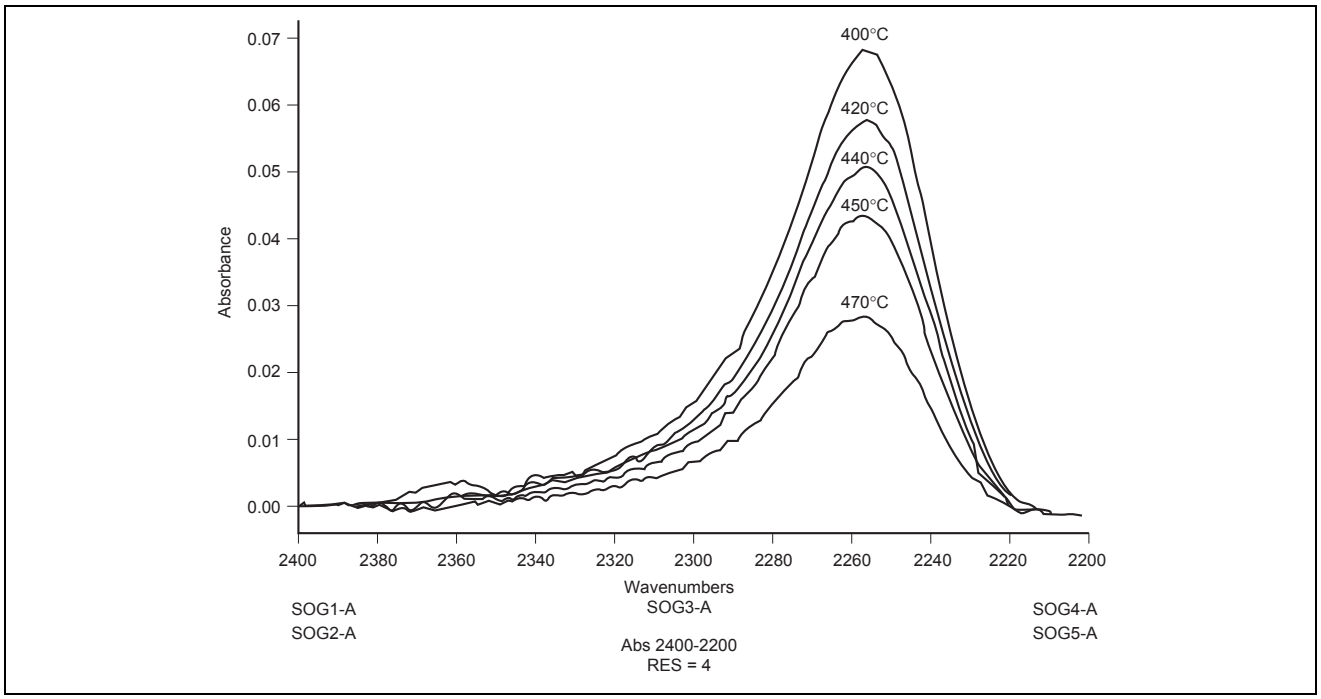


Figure 4.32 Temperature Changes at Peak Elasticity and Vibration Values for Si-H in SOG (Spin On Glass) Layer

(2) Use of ATR Method to Measure Growth Process of Natural Oxide

Figure 4.33 shows the results of a test in which silicon (100) is etched using a dilute hydrofluoric acid and is then exposed to ambient air while the oxidation growth process is measured over time. It is evident that, along with surface oxidation, the LO mode of Si-O vibration produces a shift toward the high shift side as peak strength values rise.

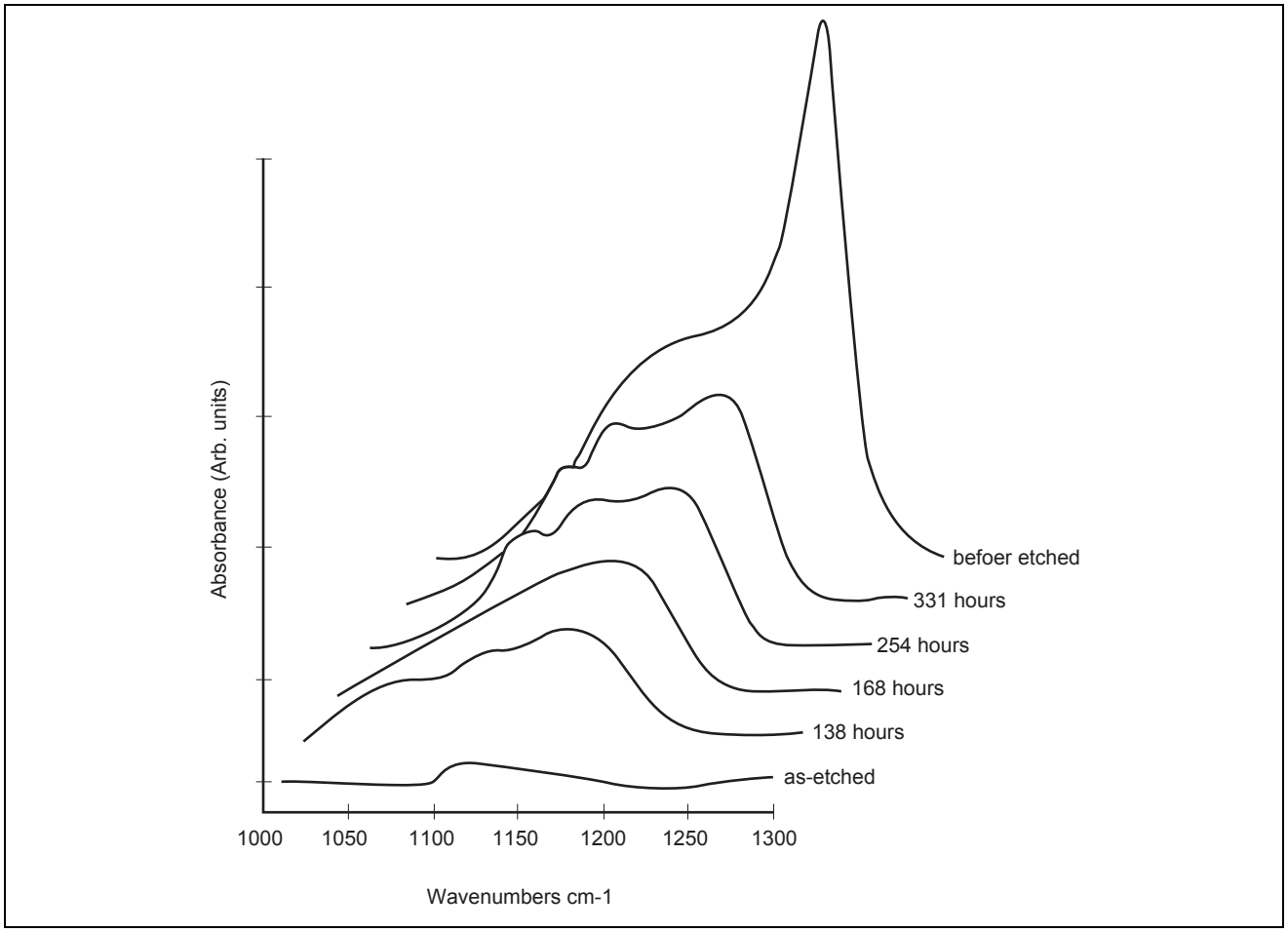


Figure 4.33 Growth Process of Silicon Native Oxide

4.4.11 TEM (Transmission Electron Microscopy)

[Objective]

The objective of TEM (Transmission Electron Microscopy) is to permeate a thin-layer coated specimen with electrons to observe corresponding images, analyze the crystal structure, and perform elemental analysis and chemical state analysis of very small areas.

[Function]

(1) Image Observation

TEM enables image observation at magnification factors of up to 10 million. Crystal defects (due to dislocation, etc.) can be observed.

(2) Crystal Structure Analysis

Electron beam diffraction is used to enable analysis of crystal structure, such as characteristics and crystal orientation, and to determine lattice constants.

(3) Analysis of Very Small Areas

An EDX spectrometer and/or an EELS can also be used to enable elemental analysis and chemical state analysis of very small areas.

[Principle]

The principle of TEM is similar to the principle for optical microscopy, except that highly accelerated electrons are fired against the specimen instead of light. An electromagnetic lens is then used to obtain enlarged images of the specimen at magnification factors of up to 10 million. If the specimen has a crystalline structure, interference between permeating electron waves and diffracted electron waves can be used to obtain lattice images. Electron diffraction images can be obtained by changing the focal distance of the electromagnetic lens. These diffraction images enable analysis of the crystal structures (including crystal characteristics that distinguish among amorphous, polycrystalline, and crystalline structures), crystal orientation, and lattice constants in the observed area. Figure 4.34 shows an outline of a TEM system and Figures 4.35 and 4.36 illustrate the above analysis example.

Elemental analysis of an area as small as 1 nmϕ can be performed when TEM is used with an energy dispersive X-ray spectrometer (EDS). This technology generates characteristic X-rays only from the electron beam-irradiated area while ignoring the electron beam's diffusion within the thin-film specimen, and the EDS spectrometer is then used to analyze the characteristic X-rays. The EELS (Electron Energy Loss Spectrometer), which is attached to the TEM, is used to perform elemental analysis and chemical state analysis of sites observed by the TEM. It is able to do this because of the energy loss that occurs in an electron beam as it permeates and reacts with the materials in a specimen. The energy distribution of electrons that have experienced energy loss differs in ways that reflect the local structure or atomic structure of the specimen's materials. Consequently, elemental and chemical analyses can be performed based on this energy distribution data.

When using TEM to observe semiconductor devices, a thin film must be deposited on the area that will be irradiated with an electron beam and observed. When observing silicon using a TEM set for accelerated voltage (200 kV), a film no thicker than 100 nm is appropriate. One typical film deposition method for semiconductor devices made of heterogeneous materials is a method that uses mechanical grinding and argon ions to etch the specimen. Recently, a FIB (Focused Ion Beam) device was used to deposit a thin film on an area measured with submicron precision as preparation for TEM observation. This method makes it possible to observe items such as particular contact/via hole or particular memory cells.

[Example of analysis]

TEM technology enables observation at the atomic level. TEM devices have been successfully used to evaluate interfaces between differential materials when electric resistance abnormalities occur, and to observe reactions between metal and silicon materials and cross sections of defective cells. An example of an analysis performed using TEM technology is described below.

In this example, a TEM unit is used to analyze areas where electrical resistance has increased between silicon substrates and polysilicon electrodes. By setting the magnification factor high enough to observe the crystal lattice in the silicon substrate, researchers discovered that an amorphous are about 1 nm thick had formed in the interface between the silicon substrate and the polysilicon (see Figure 4.35). Also, part (1) of Figure 4.36 shows an EDS profile that was taken while an electron beam was being fired specifically at that area. The EDS profile that was made from the silicon substrate for comparison purposes is shown in part (2) of Figure 4.36. These profiles indicate that oxygen, arsenic, phosphorus, and other elements are abundantly present in the silicon substrate. Armed with these analytical results, researchers were able to reduce the electrical resistance by making modifications to the preprocessing that is performed prior to growing the polysilicon.

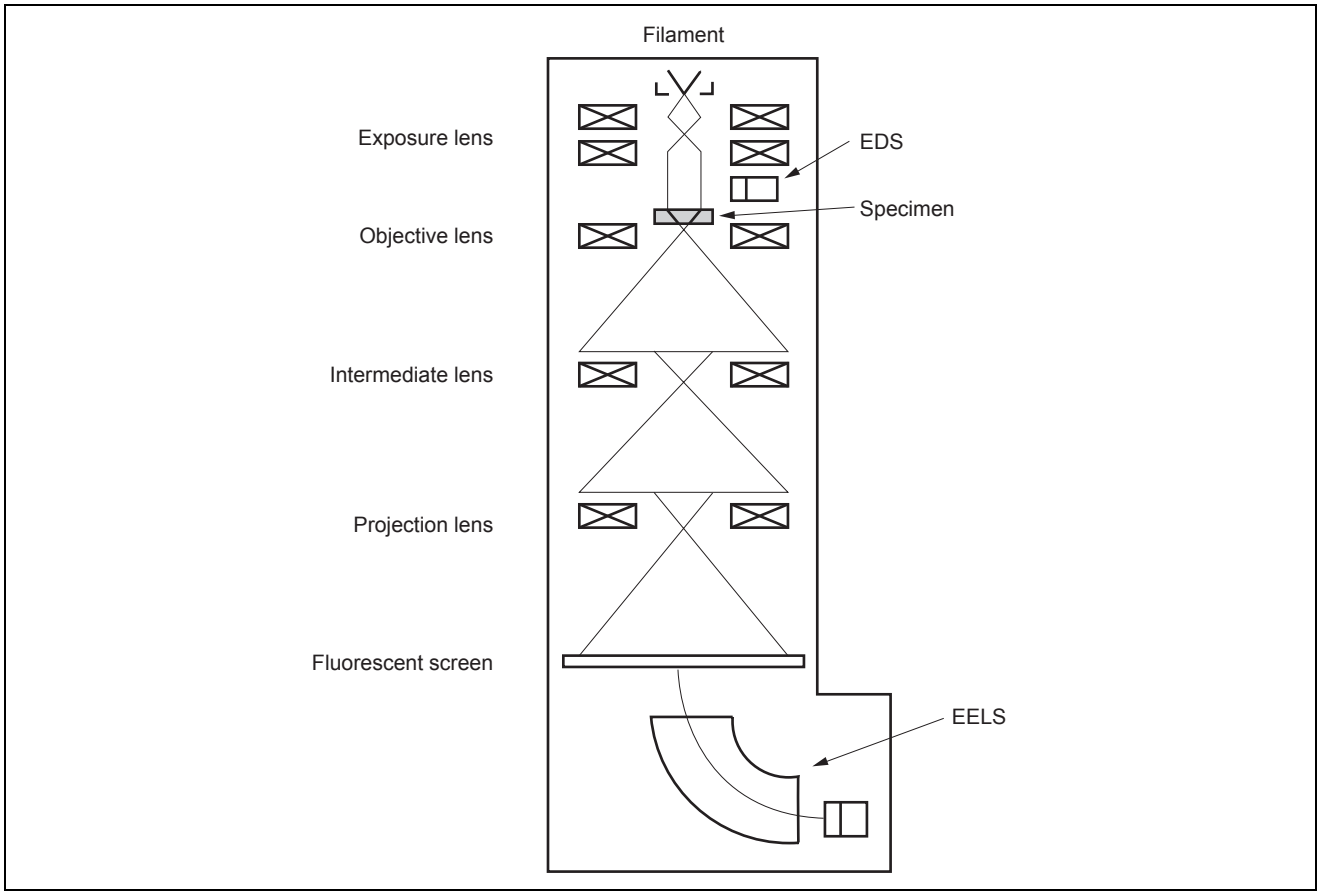


Figure 4.34 Outline of TEM System

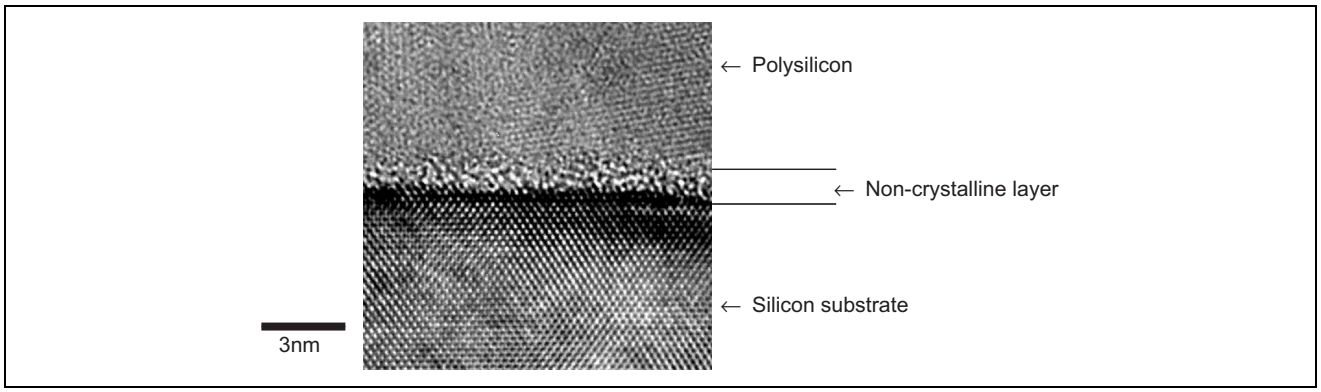


Figure 4.35 TEM Observation Example

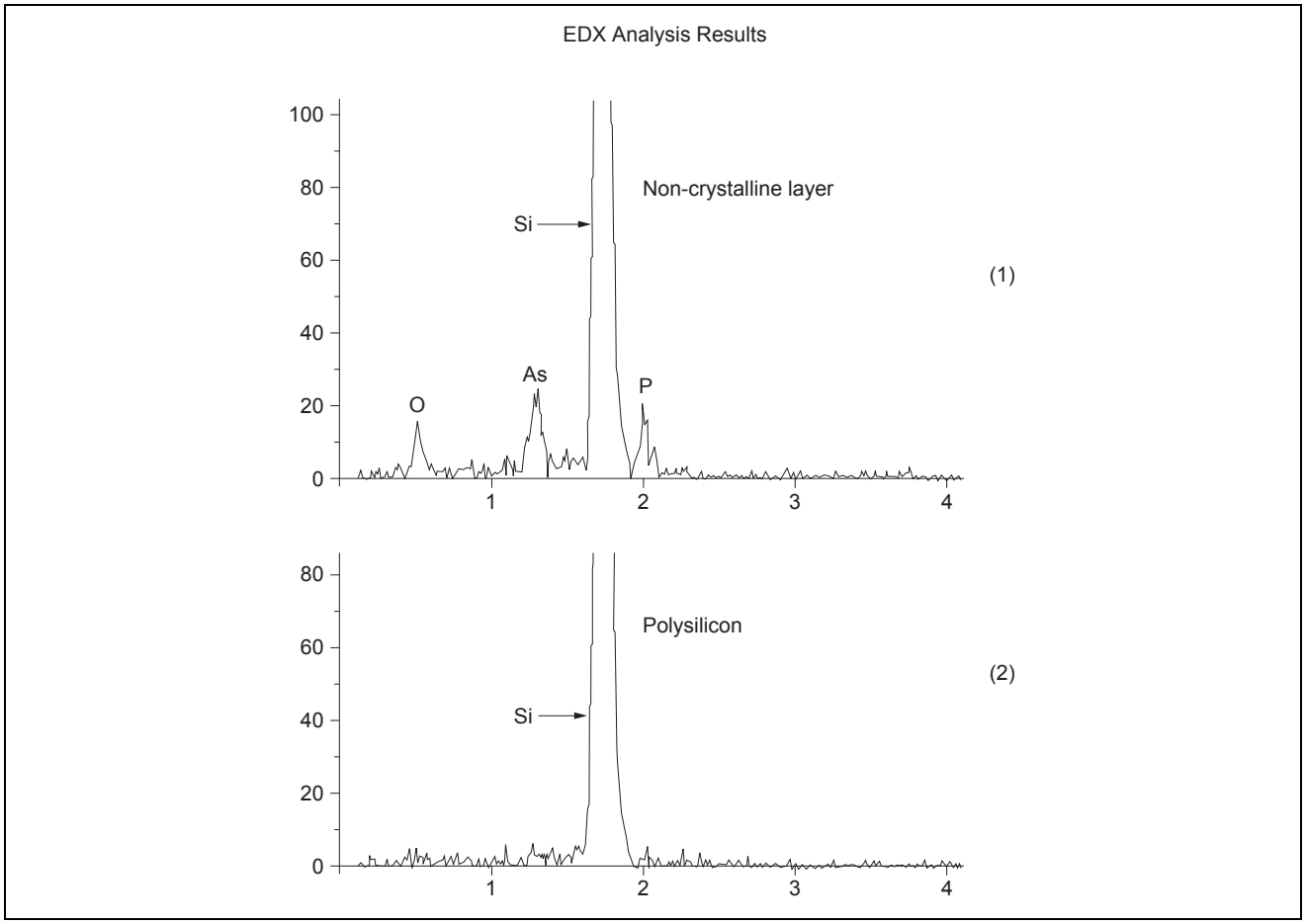


Figure 4.36 EDX Profile

4.5 Processing Technology for Analysis

4.5.1 Introduction

Failure analysis has become more difficult than ever due to the recent trends toward LSIs that are smaller, faster, more highly integrated, and are designed using a multilayer interconnect structure. Sophistication of the processing technology is explained below.

(1) Faster

Low-resistance metal deposition techniques are increasingly required for faster LSIs that need forming wiring bypass or repairing wiring.

(2) Higher Integration

Higher integration has created the need for implementation of bypasses to enable signal input/output directly to the circuit being observed.

(3) Multilayer Interconnect Structure

For the analysis of a device with a multilayer interconnect structure, technique must be found to expose semiconductor elements that are formed on buried wiring layers or substrates.

4.5.2 FIB (Focused Ion Beam)

[Objective]

FIB methods are used for ultra-fine processing or image observations in which a gallium ion beam focused to a minimum width of approximately 5 nm is radiated upon the specimen. Figure 4.37 shows an outline of an FIB system.

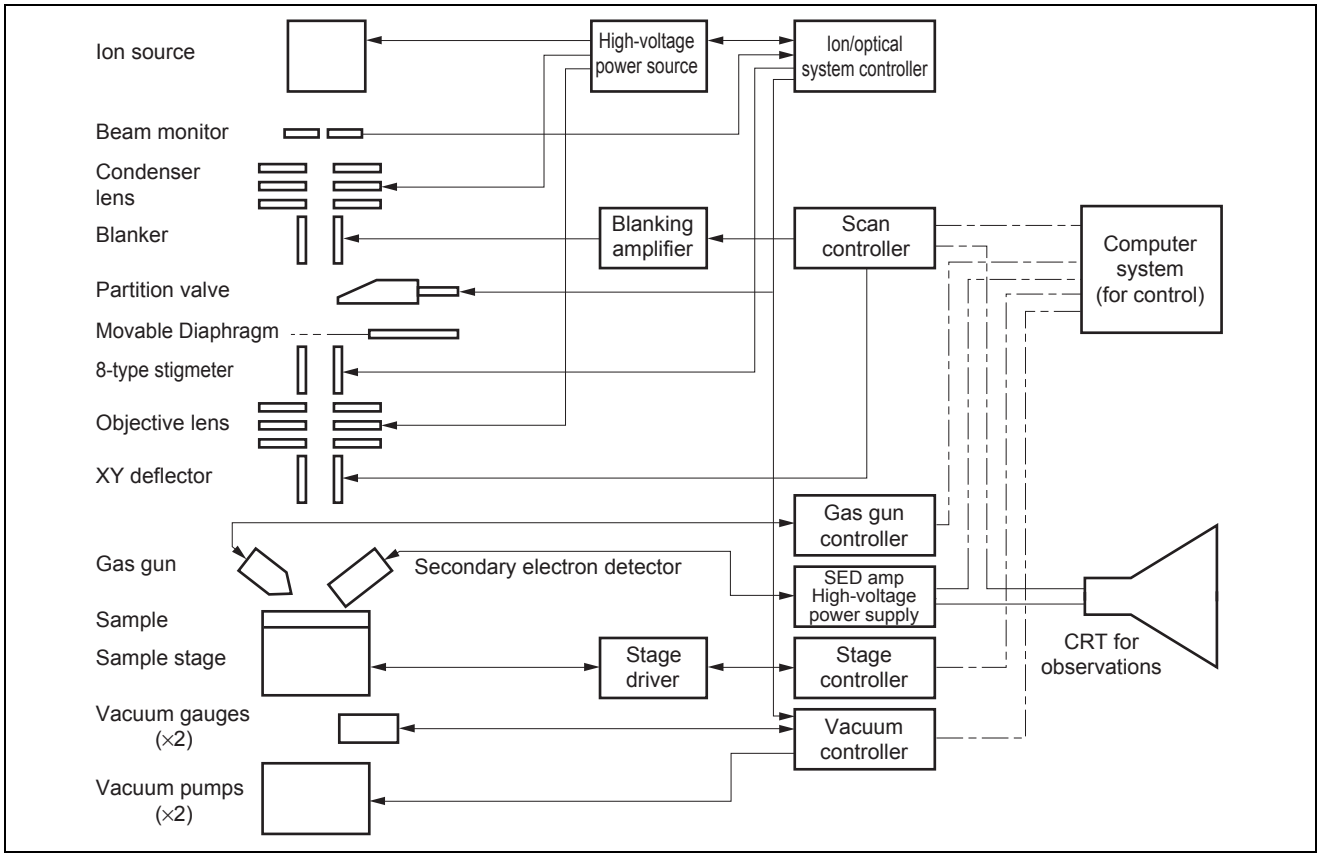


Figure 4.37 Outline of FIB System

[Function] (See Figure 4.38)

(1) Selective Etching

Etching can be performed at any site on the specimen. The site specification is accurate to within approximately 0.1 μm.

(2) Selective Metallization

When the gallium ion beam is shone upon the specimen, $W(CO)_6$ gas is blown onto the specimen, which is used to a tungsten layer at any specified site.

(3) Selective Attachment of Dielectric Layer

When the gallium ion beam is shone upon the specimen, TEOS gas is blown onto the specimen, which is used to a dielectric layer of silicon dioxide at any specified site.

(4) SIM Function

Gallium ions are fired on the specimen being scanned. The secondary electrons produced by this action are detected and their relative strength values are used to detect a contrast-based image.

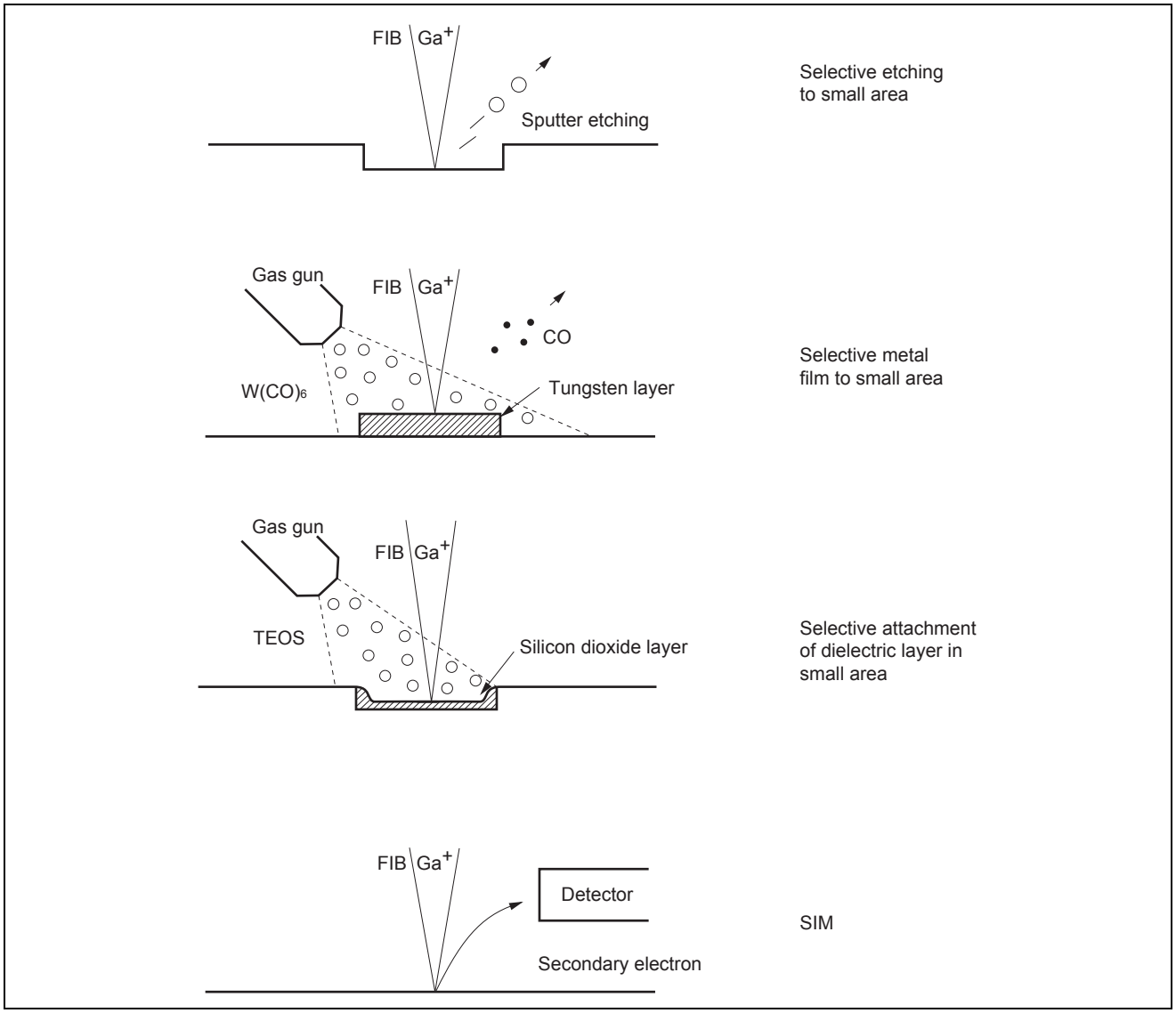


Figure 4.38 Four Functions of FIB

[Example of analysis]

(1) Selective Sectioning and Observation

When using selective etching with a SIM (Scanning Ion Microscope) function, it becomes possible to slice off and observe an LSI cross section at any specified site. During a three-dimensional analysis, the LSI's shape can be observed as a cross section that is sliced off depthwise. This method has greatly advanced the capabilities of cross section observations.[53] [54] (See Figures 4.39, 4.40 and 4.41)

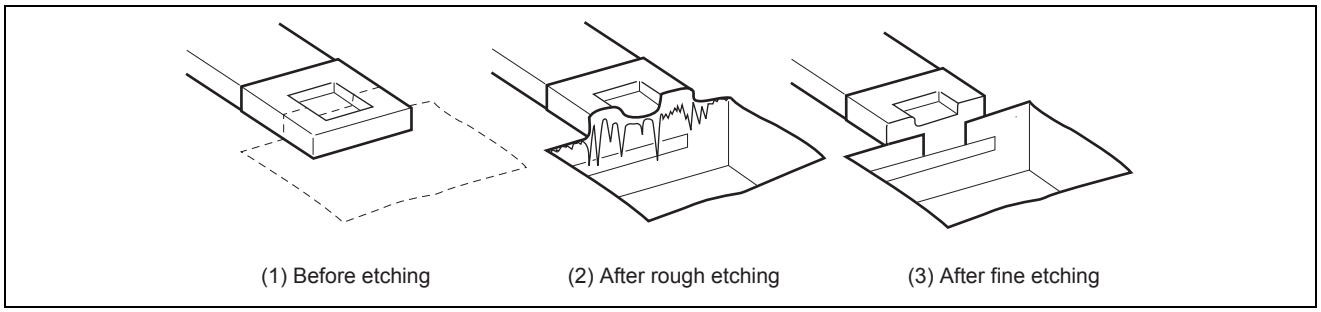


Figure 4.39 Cross-Sectioning Method Using FIB

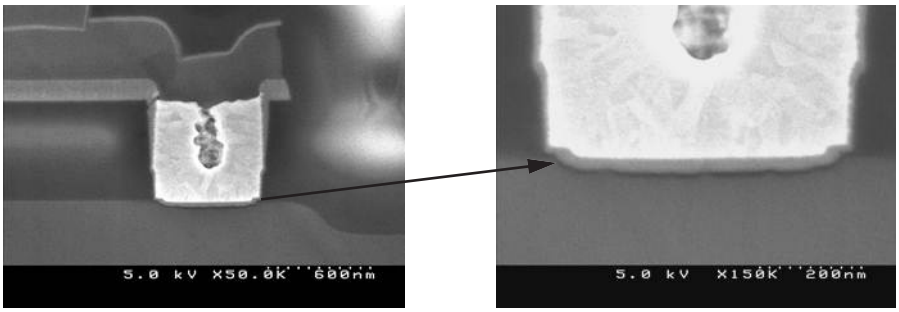


Figure 4.40 Cross Sectional Analysis Example 1 (poor contact)

Analysis example in which an open circuit has occurred due to an insulating layer a few nm thickness seen as a dark color at the Al/W plug contact interface.

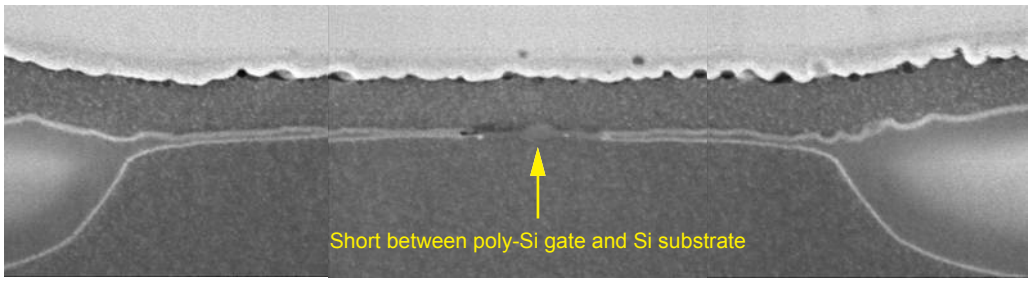


Figure 4.41 Cross Sectional Analysis Example 2 (gate oxide film destruction)

(2) Observation for Fine Structure of Metal Wiring

When a SIM function is used, it becomes possible to obtain images that reflect the fine structure of metal wiring, which is to say the shape, size, and orientation of the crystal grains. This is because the mass of secondary electrons differs depending on the orientation of the crystal grains. When IC chips that are determined to have short and long lifetimes as the result of the electromigration reliability test are compared, we see that the chip with the smaller grain size has the shorter life. (See Figure 4.42)

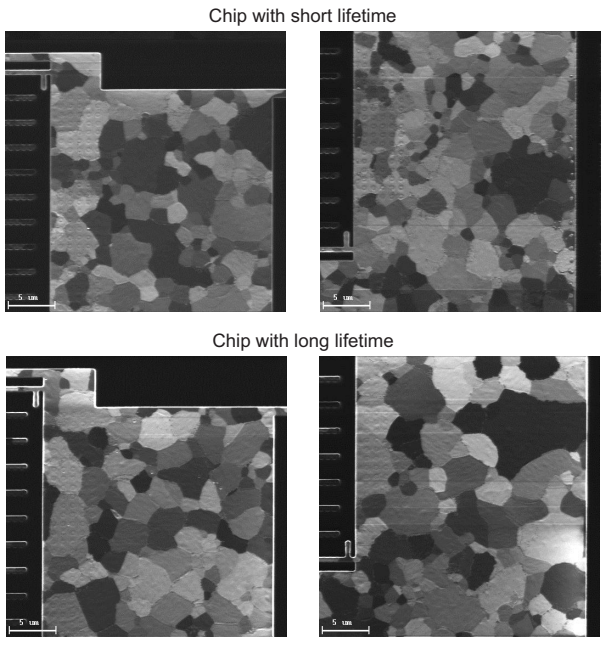


Figure 4.42 Al Grain Observation Using SIM Imaging

4.5.3 Excimer Laser

[Objective]

Passivation and metallization layers can be locally removed by irradiation from an excimer laser. In particular, in an LSI with multilayer interconnections, the excimer laser technology is an effective processing method, when the lower part covered with the upper metallization layer is analyzed.[56] (See Figure 4.43)

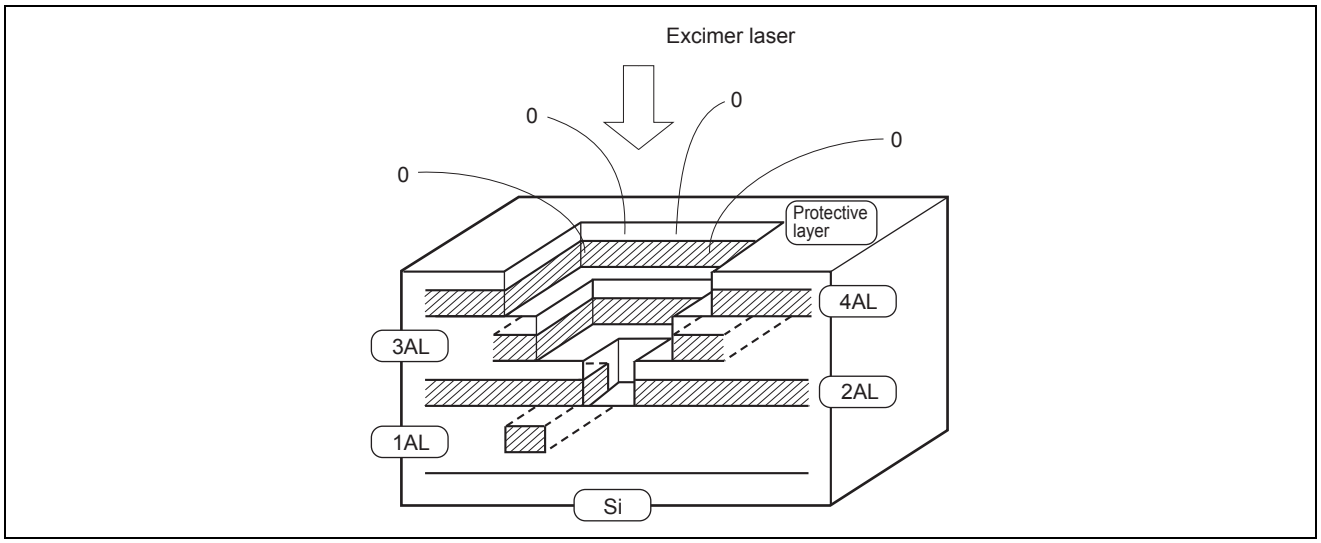


Figure 4.43 Use of Excimer Laser for Peeling Processing

[Function]

Because peel processing that uses an excimer laser can be performed while optical images of the specimen are being observed through a metallographic microscope, this operation can be performed even by inexperienced operators. (See Figures 4.44 and 4.45)

(1) Processing of protective layers and films between layers

Peel processing can be performed precisely at any desired site. This processing is used to cut a window for probes and observation of waveforms using an EB tester.

(2) Processing of aluminum wiring

Locally removing upper-layer wiring enables wiring at lower layers to be analyzed. This method is also useful for cutting thick, wide wiring such as power supply or ground lines.

(3) Marking

When secondary electron images are used for analysis, such as when using an EB tester or FIB system, marking the chip surface beforehand (i.e., etching the protective layer) makes it easier to find the site to be analyzed.

(4) Other

An excimer laser also has many other uses, such as coarse cutting before using an FIB for cross-sectioning, removing remnants after mold etching, preparing specimens before wet etching or breaking bonding wire.

[Principle]

An excimer laser is a type of gas laser that typically uses a mixture of rare gas and halogen gas and that fires short pulses of ultra-violet laser from a discharger. Since an excimer laser that has a short oscillation frequency has a large amount of photon energy, it is able to dissect combined molecules. The high absorptivity of the specimen's surface enables peeling processing to peel away very thin layers. The type of excimer laser that is most often used for such operations is the KrF laser source(wavelength: 248 nm).

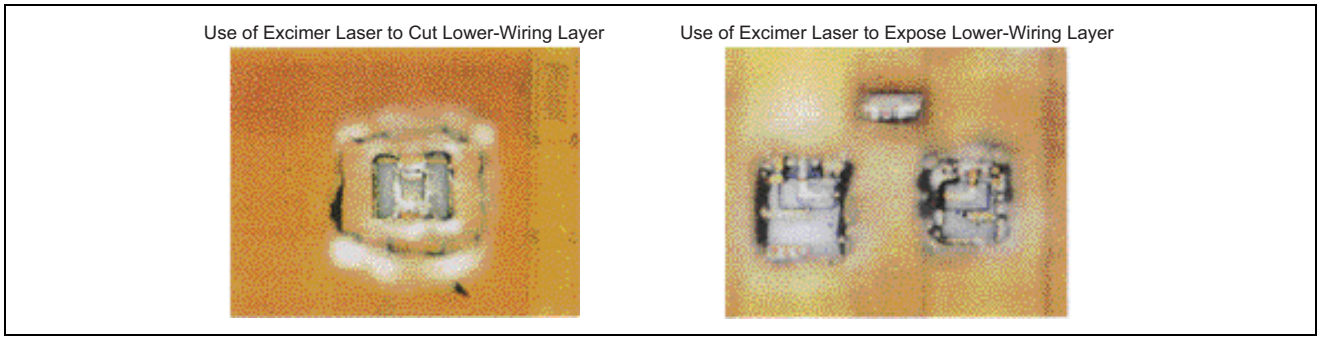


Figure 4.44 Examples of Processing Using Excimer Laser

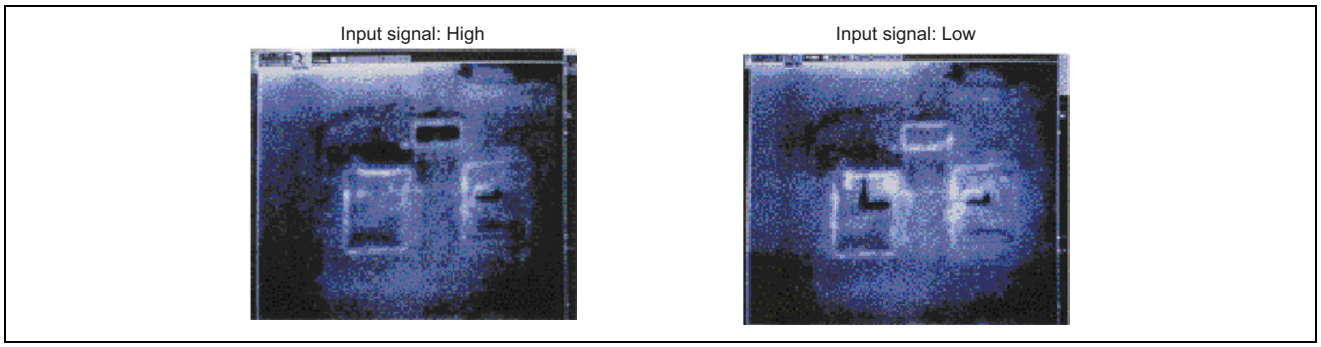


Figure 4.45 Use of EB Tester to Obtain Potential Contrast Image of Observed Lower-Wiring Layer

4.5.4 RIE (Reactive Ion Etching)

[Objective]

The objective is to expose an entire metal layer in an LSI having a multilayer interconnect structure without destroying any electrical circuits or failure state.

[Function]

RIE exposes an entire metal layer in an LSI without destroying any electrical circuit while removing dielectric layers (silicon dioxide, silicon nitride, silicon oxide and nitride, silicon oxynitride, polyimide, etc.). The ions perform anisotropic etching, which leaves any dielectric layer below the target metal layer intact while removing all other dielectric layers. Once the entire metal layer is exposed, an EB tester or other device can be used to more effectively analyze the LSI.[57] [58] [59] [60] [61]

[Principle]

When the RIE system's etching gas is in a plasma state, the reactive ions are accelerated by the potential gradient generating at the cathode side and the ions collide perpendicular to the LSI substrate to etch the target layer.

The etching mechanism is bombarding the reactive ions onto the target layer by electrode acceleration. The target layer is activated and chemically reacts with the target layer and then the layer is changed into a volatile substance. (See Figure 4.46)

The following techniques can be used to make anisotropic etching more effective.

(1) Make a steeper sheath potential (the potential gradient that occurs at the cathode side).
(2) Change the etching gas mixture (use CF_4/O_2 gas).
(3) Prevent side etching (use side protection effect).
(4) Prevent RIE processing of glass (change ratio of ions to radicals and use 1, 3, 5 effect)
(5) Protect non-target areas (use Teflon coating)

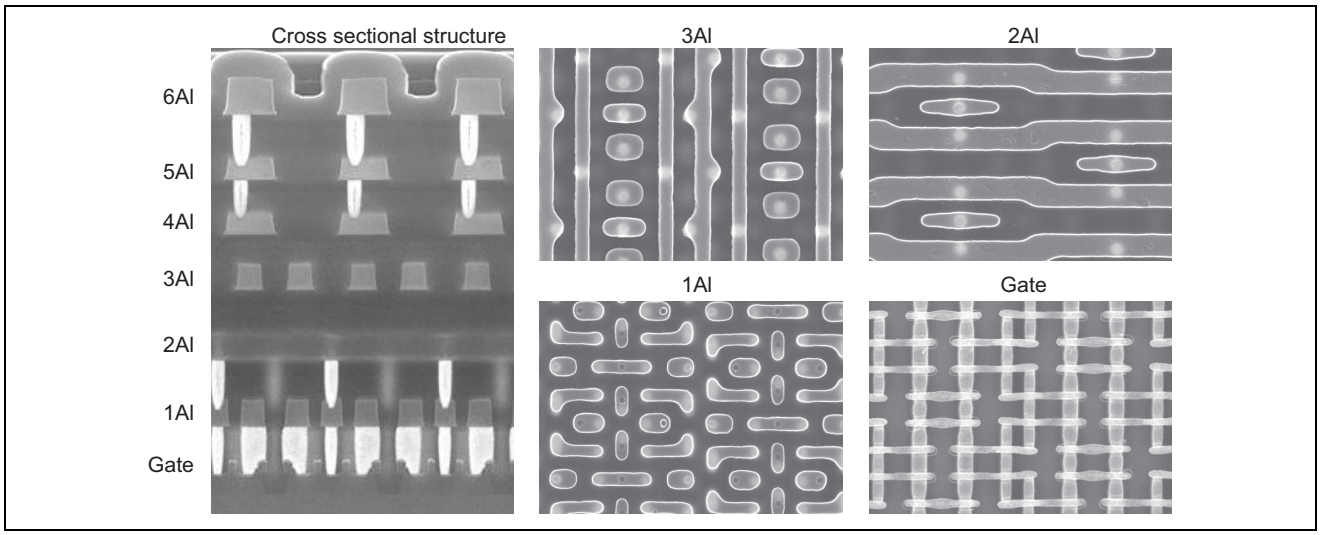


Figure 4.46 IC Chip Layer Removal Examples Using Polishing and RIE

4.5.5 FLB (Focused Laser Beam)

[Objective]

An FLB system is the unique tool to cut wiring, make a hole in dielectric layers, and perform metal deposition (using tungsten) by using a second harmonic YAG or argon laser. Three different types of lasers are applied to these three types of processing. (See Table 4.1)

This system was developed by Renesas.

Table 4.1 Laser Types and Applications

Laser Type	Type of Microprocessing
Pulse Nd-YAG	Cut wiring Form holes in dielectric layer or protective layer
CWQ Nd-YAG	Deposit tungsten metal for wiring at any site by using laser CVD method
Argon	Deposit tungsten metal for probing pad at any site by using laser CVD method

[Function]

(a) Wiring cuts, formation of holes in dielectric layer, formation of via holes [62]

(b) A laser beam with a narrow pulse width is irradiated on the LSI's surface and vaporization is used to process the wiring surface. Tungsten plugging and pad formation [63]

(c) Laser CVD processing is performed using localized processing, in which a laser beam is focused and fired on a wiring area. $W(CO)_6$ is used as the material gas, which forms tungsten wiring through thermal decomposition.

Figure 4.47 shows an outline of an FLB system and Figure 4.48 illustrates an example of microprocessing using an FLB.

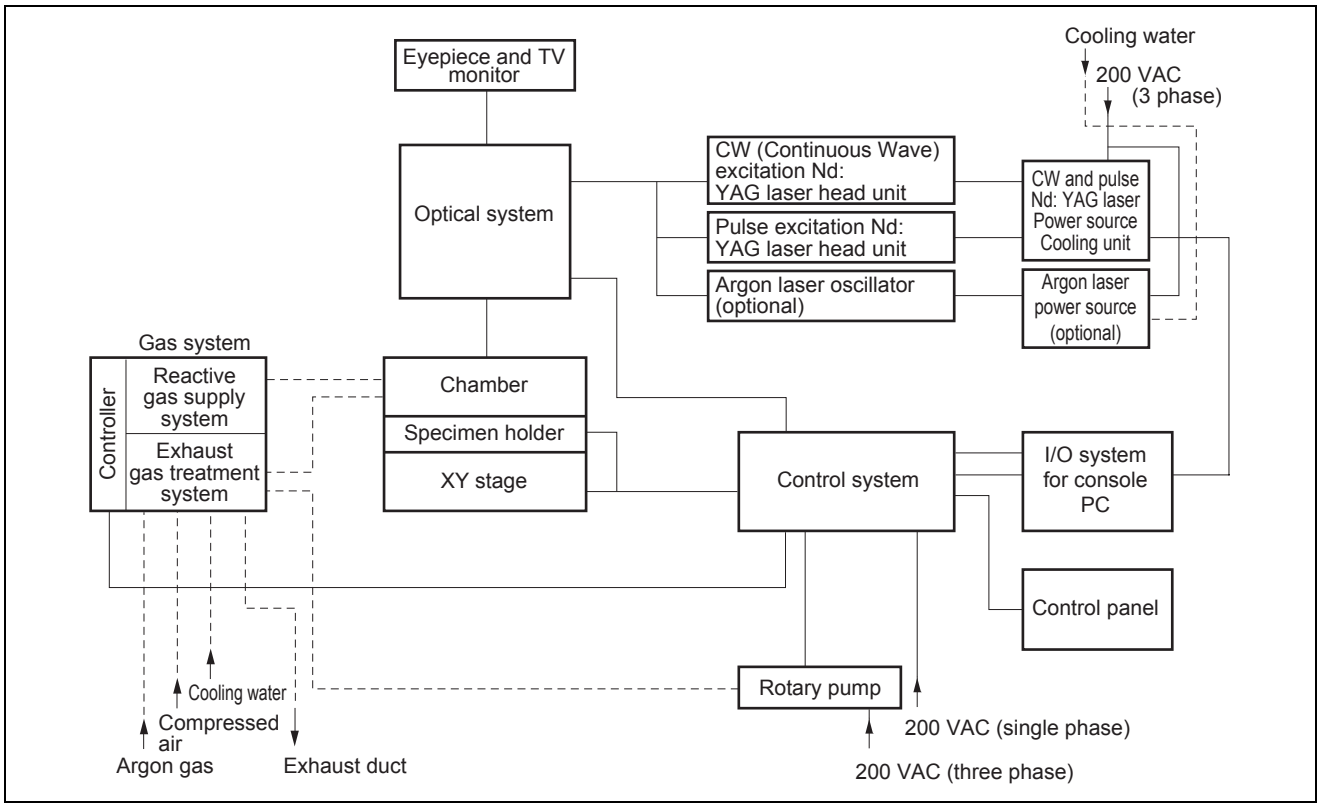


Figure 4.47 Outline of FLB System

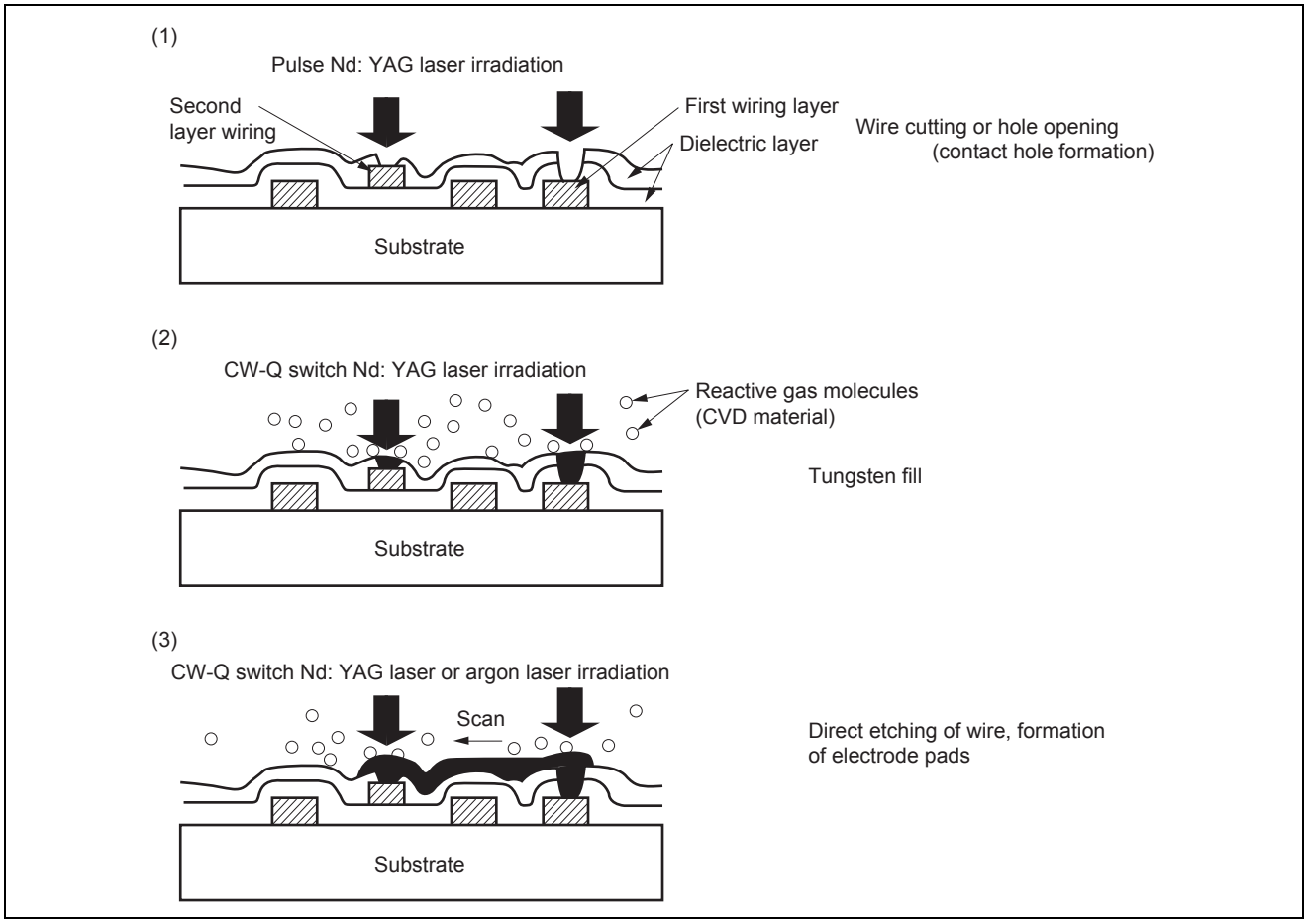


Figure 4.48 Microprocessing by FLB

[Example of application]

(1) For multilayer Interconnect Structure

There are various methods for exposing the interior of an LSI, and FLB systems are used to form large opening window.

(2) For High-Speed LSIs

Low-resistance metal deposition techniques are mainly used for forming wiring bypasses or repairing wiring connections. (See Figure 4.49)

An FLB system can be used for metal (tungsten) deposition. The forming metal layer has low resistance (about 1/100th of the resistance value produced by the FIB method), which makes it better suitable for repairing LSIs that perform high-speed operations. In addition, the metal layer has superior mechanical strength. Tests have shown that the metal layer can withstand up to five ohmic contacts during metal probing of a tungsten deposition layer whose thickness is 100 nm. (See Figure 4.50)

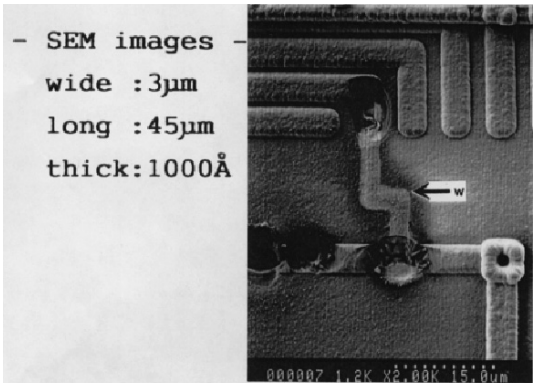


Figure 4.49 Bypass Formation Example

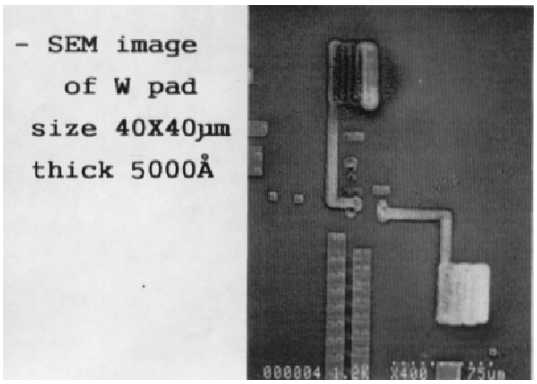


Figure 4.50 Example of Probing Pad Formation

4.6 Appendix

(1) List of Failure Analysis Techniques

Item	Technique (Equipment)	Description	Purpose
External visual check	• Observation by eyes • Stereomicroscope		Checking the external conditions
	• SEM	• Detects secondary electrons emitted by electron beam irradiation	
	• EPMA	• Analyzes the wavelength and energy of characteristic X-rays generated by electron beam irradiation	Analyzing contamination between leads and element analysis (i.e. metallic migration)
Electric characteristics evaluation	• Functional characteristics (With LSI tester) • DC characteristics (With curve tracer) • Logic simulation		Evaluating functions, DC characteristics, and internal logic analysis
Internal check before opening package	• X-ray	• Radioscopic observation	• Observation of bonding wires
	• Infrared (Microscope)	• Observes infrared radiation reflected at the reverse side of the chip.	• Observation of bonding pads
	• Ultrasonic (Scanning acoustic microscope)	• Detects reflected ultrasonic wave	• Investigation of voiding, peeling, and cracks
	• Fine leak measurement • Gross leak measurement	• Uses helium tracer gas • Uses fluorocarbons	Evaluating of airtightness of metal and ceramic packages
Opening package and locating fault point	• Opening a hole in a mold package (With opener)	• Upper resign	• Removing only upper resin
	• Plasma etching	• Chemical reaction by plasma	• Removing passivation film
	• RIE	• Removes dielectric film between layers with anisotropic etching using upper aluminum as a mask.	• Exposing lower layer aluminum
	• FIB processing	• Ion beam spattering using W (CO6) gas to form W	• Forming pads for probing
	• Nanoprober-based analysis	• Evaluates electrical characteristics of the internal circuitry of an LSI device using a submicron probe.	Logical measurement and locating disconnection of internal wiring
	• Electron beam testing (With EB tester)	• Analyzes distribution of secondary electrons emitted by electron beam irradiation	

Item	Technique (Equipment)	Description	Purpose
Opening package and locating fault point	• LVP	• Detects the light reflected by pulsed laser irradiation (effective for backside/flip-chip analysis)	
	• TRE	• Detects a weak light in the order of picoseconds generated when a transistor switches; used to analyze the operating timing (effective for backside analysis)	
	• Emission analysis (With emission microscope)	• Detects faint light emission.	Locating leakage at oxide film and PN-junctions, or short circuits of wiring
	• Thermal analysis (Liquid crystal and infrared microscope)	• Detects heat.	
	• OBIC/OBIRCH	• Detects optically excited current by electron beam irradiation • Detects the change of resistance (current) using the thermal effect	
	• EBAC	• Detects and produces an image of the absorption current generated by electron beam irradiation (effective for detecting wiring abnormality).	
Physical analysis and observation of shape and state of chip	• Optical microscope observation		Surface observation
	• SEM observation	• Detects secondary electrons emitted by electron beam irradiation	
	• EBSP	• Observes the crystal orientation by analyzing the diffraction pattern of the reflected electron increase at the crystal lattice.	
	• Grinding		Surface observation
	• FIB processing	• Spattering by ion beam irradiation	
	• TEM	• Detects electrons that pass through the sample	

Item	Technique (Equipment)	Description	Purpose
Elemental analysis	• EPMA	• Analyzes the wavelength and energy of characteristic x-rays generated by electron beam irradiation.	• Analyzing components of particles
	• SAM	• Analyzes the energy of auger electrons generated by electron beam irradiation.	• Analyzing contamination and impurity on the surface (less than 1 nm to several nm deep)
	• XPS	• Analyzes the energy of photoelectrons generated by x-ray irradiation.	• Investigation of the conditions of chemical bonds
	• SIMS	• Analyzes the mass of secondary electrons generated by ion beam irradiation.	• High sensitivity analysis of impurity

(2) List of Failure Analysis Techniques

Technique	Probed Particle	Observed Particle	Principle and Method
Electron Probe Micro Analysis (EPMA)	Electron (Tens of kV)	X-ray	Surface topography by scanning Element analysis by characteristic X-ray
Scanning Electron Microscopy (SEM)	Electron (Tens of kV)	Secondary electron	Surface topography by scanning EBIC and stroboscopic
Transmission Electron Microscopy (TEM)	Electron (Up to 300 kV)	Electron	Magnified observation of surface topograph using replica method Evaluation of crystallinity using diffraction image
Auger Electron Spectroscopy (AES)	Electron (Several hundreds to several kV)	Auger electron	Element analysis by measuring energy of auger electrons
Scanning Auger Microprobe (SAM)	Electron (1 to 10 kV)	Auger electron	Element analysis by measuring energy of auger electrons
Reflection High Energy Electron Diffraction (RHEED)	Electron (Tens of kV)	Scattered electron	Scattering and angled incidence/reflection by surface thin layer atoms
Secondary Ion Mass Spectroscopy (SIMS)	Ion (Several hundreds to 20 kV)	Secondary ion	Mass spectrometry of spatter ions
Rutherford Back Scattering (RBS)	He^+ or H^+ Ion (Up to 1 MV)	Back scattering ion	Analysis of intensity and energy of back scattering ions
X-ray Photoelectron Spectroscopy (XPS)	Characteristic X-ray	Photo-electron	Determination of shell levels by measuring photoelectron energy
Ultra Violet Photoelectron Spectroscopy (UPS)	Ultra violet	Photo-electron	Determination of shallow shell levels by measuring photoelectron energy
X-ray Fluorescence Spectroscopy (XRF)	X-ray	X-ray	Spectrometry of characteristic X-ray generating by photoelectric effect by X-ray irradiation
Scanning Acoustic Microscopy (SAM)	Ultrasonic wave	Ultrasonic wave	Analyzing elasticity by measuring ultrasonic propagation
Infrared Spectroscopy (IR)	Infrared	Reflected infrared spectral	Measuring infrared absorption spectral in surface reflection
Cathode-ray Luminescence (CL)	Electron	Optical spectral	Measuring spectral of light generated by electron collision and band excitation
Focused Ion Beam (FIB)	Ion (Up to 50 kV)	Secondary electron	Spattering by ion beam irradiation
Focused Laser Beam (FLB)	Laser	—	Spattering by laser beam irradiation

(3) List of Failure Analysis Techniques

Information Obtained	Sensitivity	Area of Analysis	Depth of Analysis	Description
Surface topograph and element distribution elements analyzed: B-U	100 to 1000 ppm 10^{-2} ML*	10^{-3} to 0.3 mmϕ	Up to 1 μm	Quantitative compensation established. High sensitivity for heavy elements. Submicrometer resolution is impossible.
Surface topograph, crystal defect, carrier lifetime, and signal propagation of device in operation	Secondary electron: Up to 0.6 nm	10^{-3} to 0.3 mmϕ	Up to 1 μm	High-resolution observation of the surface of a bulk sample. Various information including electromotive current.
Surface topography characteristics, crystallinity evaluation, and internal structure	Lattice image: Up to 0.14 nm Particle image: Up to 0.2 nm		Several μm	Sample must be a thin film. Sharp contrast of crystal defect. High resolution.
Surface element determination and depth distribution	10^{-3} ML* 0.01 to 0.1%	30 to 1 mmϕ	Several nm	High sensitivity for light elements. High mass sensitivity. Difficult to determine heavy elements because of complex spectral. Combined with ion spattering provides composite distribution along the depth of limited area.
Surface element determination, depth distribution, and three-dimensional element distribution	0.1 to 1%	5×10^{-4} to 0.1 mmϕ	Several nm	High sensitivity for light elements. High mass sensitivity. Difficult to determine heavy elements because of complex spectral. Combined with ion spattering provides composite distribution along the depth of limited area.
Symmetry of surface atoms and absorption atoms, and atomic interval	10^{-2} ML*	0.5 to 5 mm^2	Several to tens of nm	Surface structure and chemical composition.
Element determination, surface element distribution, topography elements analyzed: From H to U	10^{-5} ML* ppb to ppm	10^{-3} to 1 mmϕ	ML* to several ML*	Easy measurement of element distribution on surface and along depth. Applicable to all elements. Drawback: Large difference of secondary ion generation rate among elements. (>10^3)
Element determination, quantitative and depth analysis	10^{17} to 10^{14} atom/cc	Up to 1 mmϕ	Up to 1 μm Depth accuracy: Up to 15 nm	Nondestructive qualitative, quantitative, and depth analysis. Secondary analysis is impossible. Huge equipment.
Element determination and chemical shift	2×10^{-3} ML*	100 μm^2 to 0.3 mm^2	5 to 2 nm	Measurement of chemical bonds and compounds using chemical shifts. Low sensitivity but nondestructive.
Band structure and vibration level	2 to 10^{-3} ML*	Up to 0.1 mm^2	ML* to 3 nm	Band structure information can be obtained. Element analysis is impossible. Sensitive to surface conditions.

Information Obtained	Sensitivity	Area of Analysis	Depth of Analysis	Description
Element determination elements of quantitative analysis: From F	Heavy elements: 5 ppm Light elements: 500 ppm		Tens of nm	Quick nondestructive qualitative and quantitative analysis.
Crystal defect and multi-layer structure analysis			Tens of nm	Nondestructive analysis of cross-sectional structure.
Surface molecular structure and bonding state	10^{-3} to 10^{-7} g	Several to tens of mmϕ	Up to 1 μm	Chemical type and orientation of surface absorbed substances.
Energy band structure and wave length change by structure	Up to ppm	0.1 to 1.0 μmϕ	Up to 1 μm	Only applicable to measurement of light emitting substances and solid plasma emission.
Cross-sectional structure	Secondary electron: Up to 5 nm	—	—	Cross-sectional observation of limited areas.

Note: * ML: Mono Layer

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[63] M. Sanada, Y. Morishige “Evaluation of Direct Writing Tungsten Metal using Focused Laser Beam - Fabrication for Failure Analysis on Advanced LSIs -” LAMP '92 Vol. 2, pp. 1203-1208 June/1992.

5. Basic Recommendations for Handling and Using Semiconductor Devices

This section presents some common precaution or instruction for using semiconductor products that our customers should understand and follow.

To ensure the desired functions, performance, quality, reliability, and safety features in sets developed and manufactured by customers, both Renesas as the supplier of semiconductor devices and the customer as the user of such devices have roles to play in promoting safe and proper use of semiconductor devices.

As part of its role, Renesas implements design and manufacturing plan to ensure the quality, reliability, and safety of semiconductor devices, provides product labels and documents describing cautions and restrictions or handling and use, and recommends appropriate products for each application. The various quality assurance measures that Renesas implements during semiconductor device development, manufacture, and sales have been described in section 1.

In contrast, the measures that shall be implemented by customers who develop and manufacture sets include selecting semiconductor devices that have quality and reliability features that are appropriate for the set's requirements, avoiding the application of stresses that exceed the semiconductor device's stress resistance capacity, implementing design for safety and other safety measures for each set, and fully implementing evaluation of each set's functions, performance, quality, reliability, and safety features before using the set.

With the above considerations, this section presents general recommendation for handling and usage of semiconductor devices deemed necessary to ensure the quality, reliability, and safety of sets. These cautions concern the set design, handling, packaging, storage, shipment, and testing of semiconductor devices as well as issues such as ESD, latch-up, and device mounting.

Customers shall refer to individual semiconductor device documentation (manuals, etc.) for cautions pertaining to specific semiconductor devices in addition to understanding the general cautions described in this section.

5.1 Product Safety

Since July 1995 the Product Liability (PL) Law has been in effect in Japan, but even before that Renesas considered safety an integral element of product quality and has promoted safety of semiconductor products as part of our efforts to improve them.

Ordinarily, semiconductor devices are not hazardous products (i.e., they do not emit toxic gas, etc.). Consequently, semiconductor safety considerations relate to safe handling of semiconductor devices in the sets being designed by customers, improving fire resistance, minimizing the environmental impact of disposing of sets that are no longer used, and other issues.

To support our customers' safe and effective usage of semiconductor devices in end products, Renesas provides the information our customers need to design those end products in a wide range of technical documents.

To help improve fire resistance under actual use conditions, Renesas has made sure that all of its plastic-encapsulated semiconductor products use plastic materials that meet UL standards for flame resistance.

To help minimize the environmental impact of set disposal, Renesas performs safety and environmental safety assessments on semiconductor devices as part of its product design assessment audits.

Note that the product safety of Renesas' semiconductor devices consists of the safety aspects ordinarily required in the semiconductor devices themselves as components used in other systems; the user shall assume full responsibility for meeting safety requirements connected with the way these products are used and the environment in which they are used.

Renesas's basic philosophy on product safety and efforts to improve it are as follows.

(1) Product Safety Measures from the Beginning

In the “the reliability program example” and “quality certification flows” shown in the Quality Assurance System, the checking items of the product-safety are set and taken into consideration among the specification, the development, and the design of the product. The principal safety measures that are taken in the major steps from product development through shipment are listed in Table 5.1.

Table 5.1 Principal Product Safety Measures

Principal Categories	Considerations (main points)
Product Development	On the way the user uses the product
Determination of Specifications	On the environment in which the product is used
Design	On destruction mode
	On malfunction mode
Manufacture	Observance and clarification of manufacturing rules
Quality Assurance	Quality assurance and evaluation checks at each stage of production
Sales	Issuance of documents

(2) Documentation

In order for semiconductor devices to be used safely, there are a number of documents including data sheets that indicate the product performance. Renesas also issues a number of documents specifically related to product safety so that the maximum utilization can be taken of the product specifications (see Table 5.2).

Table 5.2 Documents Concerning Product Safety

Category	Examples of Specific Documents
Documents that give product specifications	Data sheets, Data books, Technical information, Delivery specifications (Purchase specifications), etc.
Documents that give precautions in use	Reliability handbook, Renesas Surface Mount Package User’s Manual, etc.
Other documents (documents prepared for individual users)	Sale agreements, Quality agreements, etc.

(3) Consultations on Specifications and Quality

Quality consultations are held to assist the user in using the products under conditions that are appropriate for the product specifications. As stated above, these conditions are announced in a variety of documents, but discussion are held in order to give more detailed conditions for use and help the user to select the most suitable product for each application.

5.2 Semiconductor Device Selection

5.2.1 Application-Related Cautions

The first requirement for using semiconductor devices is to select a semiconductor device that is appropriate for its intended use: in other words, it shall have the quality and reliability features needed for the target electronic equipment. Renesas classifies its products into two quality grades. Table 5.3 lists the applications in which these products are mainly intended to be used.

Table 5.3 Quality Grades for Renesas Semiconductor Devices

Quality Grades	Representative Examples of Use Application
High Quality	Transportation equipment (automobiles, trains, ships, etc.), traffic control (signals) , large-scale communication equipment, key financial terminal systems, safety control equipment, etc.
Standard	Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment, industrial robots, etc.

Unless specifically stated otherwise in the datasheet, data book, delivery specifications or other documentation, semiconductor devices designed, developed, manufactured, or sold by Renesas are of the Renesas standard quality grade. These devices may not be used in applications that assume a high quality grade. Furthermore, Renesas semiconductor devices of the Renesas standard quality grade are not intended for use in, and may not be used in, equipment or systems that may present risks to human safety or life (e.g. life support systems or applications that will be embedded in a patient's body), or equipment or systems that could cause major property damage (e.g. nuclear power plant control systems or military equipment). In particular, Renesas assumes no responsibility for any financial loss or harm that occurs to a customer or any third party due to the use of a Renesas product in an application for which it was not intended. If you have any questions regarding this, contact your Renesas sales representative.

5.2.2 Maximum Ratings

The maximum ratings for semiconductor devices are ordinarily specified as “Absolute Maximum Ratings”. Absolute maximum ratings are defined under JIS C 7032 as limit values that shall not be exceeded even momentarily or limit values that shall be simultaneously maintained for several parameters when ratings have been specified for those parameters.

If a maximum rating is exceeded even for an instant, a semiconductor device may be damaged or destroyed, or the subsequent lifetime of the device may be greatly shortened. Furthermore, due to differences in the strengths of individual semiconductor devices, although a certain semiconductor device may be able to withstand the stress when a maximum rating is exceeded, other devices in the same end product may be easily destroyed by this stress.

Therefore, when designing a circuit using a given semiconductor device, designers shall design the circuit so that the maximum ratings for that semiconductor device are never exceeded, whatever fluctuations occur in the external conditions during circuit operation.

Furthermore, semiconductor devices shall be used not only within their DC maximum ratings, but also within the safe operating areas for voltage, current, power, and time for all points on the load locus curve. Note that since the power supply and ground lines function as the reference points for semiconductor device operation, special care shall be taken to assure that the maximum ratings are not exceeded even for transient states.

5.2.3 Derating

Derating is defined under JIS Z 8115 as the systematic reduction of stress for the sake of improved reliability.

The quality and reliability of semiconductor devices are greatly influenced by the environment of use. That is, products with the same quality may be less reliable in harsh environments, and more reliable when the usage environment is less harsh. Even when used within the maximum ratings, if semiconductor device is used under extremely stringent conditions equivalent to lifetime tests, wear-out-like failures may result. Hence derating is critically important and shall be considered in equipment design.

Derating is applied to product groups, such as discrete devices and power ICs, that require adjustment of the operating conditions, such as ambient temperature, junction temperature, voltage, current, and power, which are mutually related. This is because in addition to having wide usage condition ranges these products have the property that even if they are operated within the corresponding usage range (e.g. voltage), concern for the junction temperature will be required due to the relationships between characteristics such as the power generated, ambient temperature, and heat sink used.

Derating may be approached from two perspectives: derating with respect to design limits, and derating with respect to manufacturing variations.

(a) Derating with Respect to Design Limits

When usage conditions become extremely harsh, the wear-out failure range may be entered during the time of actual use, and if derating is not employed, in actual use, it may become necessary to schedule replacement of all semiconductor devices as part of maintenance after operation for a certain length of time in the application.

(b) Derating with Respect to Manufacturing Defects

Although the wear-out failure range is not entered while in actual use, if conditions of use are harsh, the probability of occurrence of defects in the random failure range may no longer be negligible.

Table 5.4 lists an example of an approach to derating. The temperature item assumes all night continuous operation. Also, values shown in parentheses assume intermittent use (about 3 hours per day).

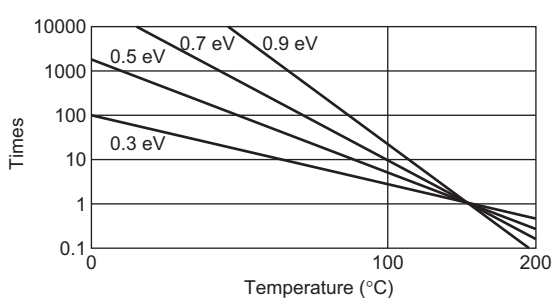
Table 5.4 Standard Examples of Derating Design*1

Derating Element*2		Diodes	Transistors	Power ICs	HyICs	LDs
Temperature	Junction temperature *3	Tj = 60°C or lower (Tj = 110°C or lower)			—	—
	Device ambient temperature	Ta = 0 to 45°C		Topr min to Topr max Ta = conform to delivery specification conditions		
	Other	Power consumption, ambient temperature, heat-dissipation conditions Tj = Pd × θja + Ta			—	—
Humidity	Rel. humidity	Relative humidity = 45 to 75%				
	Other	Normally, if there is condensation due to rapid changes in temperature or for other reasons, the printed circuit board is coated.				No condensation
Voltage	Breakdown voltage*3	Maximum rating × 0.5 or less (maximum rating × 0.8 or less)	Maximum rating × 0.8 or less	Conform to delivery specification conditions	Conform to delivery specification conditions	
	Overvoltage	Take measures to prevent overvoltage application, including electrostatic discharge				
Current	Average current*3	Ic × 0.25 or less (Ic × 0.5 or less)	Ic × 0.5 or less	Ic × 0.5 or less	Conform to delivery specification conditions	
	Peak current	IF (peak) × 0.8 or less	IF (peak) × 0.8 or less	Ic (peak) × 0.8 or less	Conform to delivery specification conditions	
	Other	—	—	Take fanout, load impedance into consideration	—	Take optical output Pomax into consideration
Power	Average power	Maximum rating × 0.5 or less (especially power diodes)	Maximum rating × 0.5 or less (especially power transistors)	Maximum rating × 0.5 or less	Conform to recommended delivery specification conditions	VF × IF × Duty
Pulse*4	SOA	Shall not exceed delivery specification maximum ratings				
	Surge	IF (surge) or less	Ic (peak) or less		Conform to recommended delivery specification conditions	

Notes: 1. Not applicable to special usage conditions, for example, extreme high temperatures.
2. These derating elements shall be satisfied simultaneously wherever possible.
3. Values shown in parentheses are made on the premise of intermittent use.
4. Generally where transient states are concerned, peak voltage including surges, current, electric power, and junction temperature shall be below maximum ratings, and derating for reliability shall be performed using the above average values. SOA (Safe Operating Area) will differ with the circuit used; please consult with one of our engineers.

An example of derating for temperature is given in Table 5.5. It is thought that as the temperature increases, chemical reactions in the materials constituting a semiconductor device are accelerated, leading to failure. Thus, reliability is usually estimated based on the idea that the degree to which war-out failures do not occur in actual use can be inferred from the reliability test results and the environmental conditions during actual use. Derating is performed after calculating the acceleration coefficient between the lifetime test data, which has been confirmed by assuming the activation energy for the chemical reactions for each failure mode, and the actual conditions of use. In general, temperature acceleration alone does not result in a sufficient acceleration rate, but is ordinarily used together with, for example, voltage and temperature difference. The acceleration limit for temperature shall be more carefully analyzed. It may have a possibility to cause a mistake which is made by other failure modes governed by different reactions from those in the normal temperature range such as the glass transition temperature of plastic material.

Table 5.5 Temperature Characteristics of Derating (Example)

<table>
<tr><th colspan="2">Example of Applications for Derating</th><th>Temperature Derating</th></tr>
<tr><td>Stress factor</td><td>Junction temperature</td><td rowspan="2"> 
</td></tr>
<tr><td>Failure judgment criteria</td><td>Deterioration of electrical characteristics</td></tr>
<tr><td>Failure mechanism</td><td>Deterioration by chemical reactions</td><td rowspan="2">How to calculate derating
We consider a lifetime test at Tj = 150°C to have an acceleration factor of α compared to the usage temperature in the marketplace. For example, assuming Ea = 0.5 eV and the usage temperature in the marketplace is 65°C, then the acceleration factor α is calculated to be 31.5 times as shown below.
α = exp [0.5/8.617 × 10^{-5}/(273 + 65)]
exp [0.5/8.617 × 10^{-5}/(273 + 150)] ≈ 31.5</td></tr>
<tr><td colspan="2">Outline
The horizontal axis is temperature and the vertical axis shows the multiplier. If device failures are considered to be due to chemical reactions between materials, then, in general, the chemical reaction will proceed faster with increasing temperature. According to the Arrhenius model, the lifetime can be expressed as follows:
<lifetime> = <constant> × exp(Ea/kT)
where Ea: activation energy (eV)
T: absolute temperature (degrees K)
k: Boltzmann constant (8.617 × 10^{-5}eV/K)</td></tr>
</table>

An example of derating for humidity is shown in Table 5.6. The primary purpose of this derating is to prevent corrosive breaks of Al wiring and to prevent any degradation of solderability accompanying storage of package leads. Due to advances in plastic materials, corrosion and breakage of Al wiring hardly ever occurs any more in the marketplace; but even today, use under extremely harsh conditions may still result in wear-out failures within the expected period of useful life of a device.

Table 5.6 Humidity Characteristics of Derating (Example)

Example of Application for Derating		Humidity Derating
Stress factor	Temperature, relative humidity	Saturation vapor pressure (KPa) table (based on Wagner's formula)
Failure judgment criterion	Deterioration of electrical characteristics	
Failure mechanism	Metallization corrosion	

Temperature (°C)	0	2	4	6	8
0	0.611	0.706	0.814	0.935	1.073
10	1.228	1.403	1.599	1.819	2.065
20	2.340	2.646	2.987	3.365	3.784
30	4.248	4.761	5.326	5.949	6.634
40	7.385	8.210	9.112	10.09	11.17
50	12.35	13.62	15.01	16.52	18.16
60	19.94	21.85	23.93	26.17	28.58
70	31.18	33.98	36.99	40.21	43.68
80	47.39	51.36	55.60	60.14	64.98
90	70.14	75.64	81.50	87.73	94.35
100	101.3	108.8	116.7	125.1	133.9
110	143.3	153.2	163.7	174.7	186.3
120	198.6	211.5	225.1	239.4	254.5
130	270.3	286.8	304.2	322.5	341.6

Outline

Since the supply of moisture accelerates metallization corrosion, the water vapor pressure is thought to be a stress that affects failures due to that process. In this model, the service live is approximated by a power of the water vapor pressure (absolute water vapor pressure model).

Service life = constant × (saturation vapor pressure) $^{-n}$

Taking the logarithms of both sides of this equation, we obtain:

log (service life) = -n × log (saturation vapor pressure) + (constant)

Taking the logarithm of saturation vapor pressure as the abscissa and the logarithm of the time required to reach the prescribed failure rate at that vapor pressure (service life) as the ordinate, the resulting graph is approximately a straight line.

Relative humidity expresses the humidity at a given temperature relative to the saturation vapor pressure, which is 100%.

How to calculate derating

We calculate the acceleration under typical conditions used in tests of ability to withstand humidity (65°C/95% RH) and typical conditions in the marketplace (Ta = 25°C/65% RH).

From the table, the saturation vapor pressure at 65°C is calculated by the interpolation method to be 25.05 KPa and the saturation vapor pressure at 25°C is calculated to be 3.176 KPa. The vapor pressure is calculated by multiplying these values by 0.95 and 0.65, respectively.

Taking the ratio and using the typical acceleration constant n = 2, acceleration (α) can be calculated as follows:

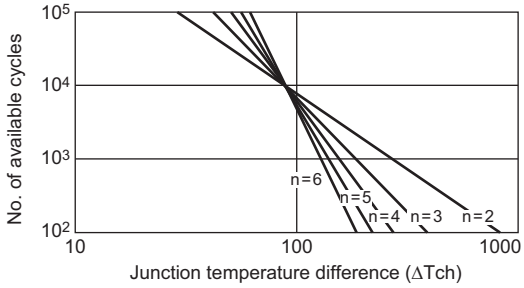
$\alpha = (23.80 / 2.064)^2 \fallingdotseq 133$

The result is thus 133 times.

An example of derating for temperature differences appears in Table 5.7. The failure mechanism assumes thermal fatigue failure of structural materials. This mode generally leads to wear-out failure modes, and so adequate derating calculations are important for power devices and other components. While designing thermal dissipation, the number of times heat stress is applied during the lifetime of the semiconductor device and the temperature difference of the stress shall be taken into consideration.

Voltage, current, and power derating is especially effective in preventing failure phenomena. In particular, temperature-difference derating is strongly related to the occurrence of such failures, that is, failures to which stress-strength models apply. In these cases, robustness against failure is weakened by the development of structural defects, resulting in failure under stress which does not initially lead to failure.

Table 5.7 Power Transistor Power Cycle Characteristics of Derating (Example)

Example of Application for Derating		Power Transistor Temperature Difference Derating
Stress factor	Junction temperature difference	Example of a product having the ability of 10,000 cycles at ΔTch = 90°C 
Failure judgment criterion	Deterioration of θch - c	
Failure mechanism	Solder fatigue	
Outline It is believed that the nth power of the temperature difference is proportional to the power cycle limit. Cycle count lifetime = constant × (temperature difference) $^{-n}$ Taking logarithms of both sides of this equation gives log (cycle count lifetime) = -n × log (temperature difference) + log (constant) Taking the logarithm of the junction temperature difference (ΔTch) at the time of power cycle ON or OFF as the abscissa and the logarithm of the limiting cycle count lifetime at that time as the ordinate, that graph can be approximated by a straight line. This line of reasoning permits us to estimate the number of years a device will last from the conditions under which the power transistor is used. Conversely, we can determine the power transistor heat radiation conditions from the number of years the device is required to last.		How data of derating are used This section presents an example of calculating the cycle lifetime under the condition Ta = 25°C. If Tcmax = 85°C and Pc = 20 W, then if we take the product θch-c to be 1.0°C/W, then Tjmax will be 85 × 20 × 1.0 = 105°C. The temperature difference ΔTj with Ta = 25°C will be 80°C, and the cycle lifetime can be calculated from the formulas at the left and power cycle test results.

In the marketplace, conditions of actual use are not so simple that they can be described by a single parameter. Moreover those conditions are not constant with time. Normally worst-case condition is assumed when performing the derating to determine whether or not it can be used; but when conditions cannot be combined into a single parameter, conditions are converted to standard conditions and derating performed as shown below.

Assuming that the number of conditions that apply to practical use has been reduced to n,

ti = within the lifetime of a component, the cumulative time that the component has been used in the market under the ith condition, and let

αi = the acceleration coefficient derived from the standard conditions and the ith condition. The equivalent time that has elapsed under the standard conditions can be expressed as $ti \times \alpha i$. The following equation can then be obtained by converting every condition into the time under standard conditions.

$$t = \sum ti \times \alpha i$$

The lifetime under actual use conditions can be replaced with the test time in the accelerated lifetime test by substituting the reliability test conditions for the standard conditions in this formula.

5.2.4 Safe Operating Area in Transistors

When a transistor is used as a switching element in an inductive load circuit, not only shall the maximum ratings be observed, but the SOA (safe operation area) shall not be exceeded as well.

Figure 5.1 describes SOA in the following four types of elements.

- Area I: Ic MAX
  This area is restricted by the collector current rating.
- Area II: Dissipation Limit
  This area is restricted by the total dissipation (thermal resistance).
  In the case of direct current (DC), the limit varies according to the thermal resistance (Rthj-c), and in the case of pulse, the limit varies according to the transient thermal resistance ΔRth, as shown in Figure 5.2.
- Area III: Secondary Breakdown Limit
  This area is limited by secondary Breakdown Phenomena.
- Area IV: VCEO MAX
  This area is limited by the collector voltage rating.

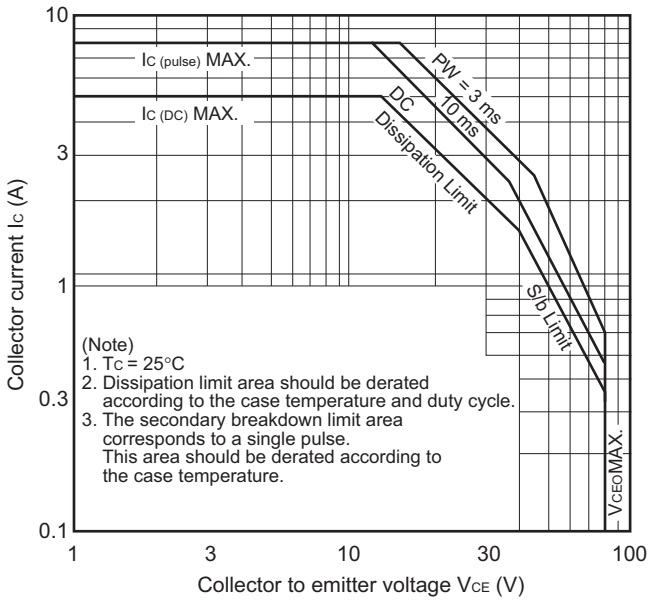


Figure 5.1 Example of Safe Operating Area

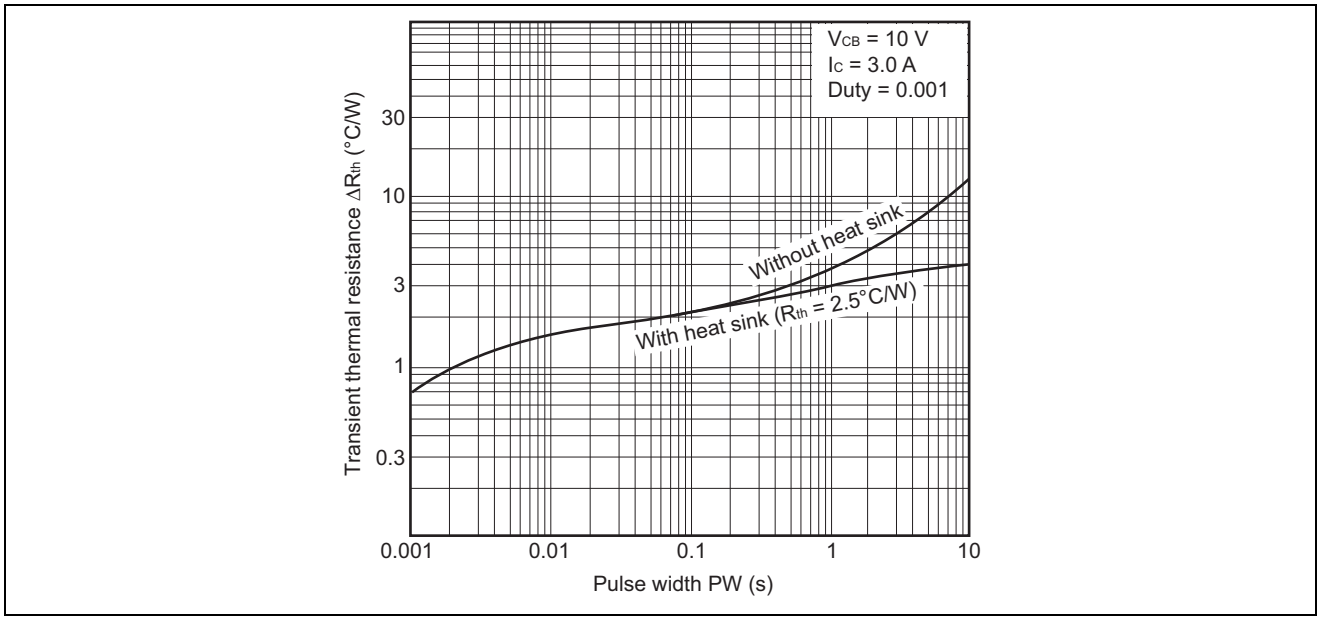


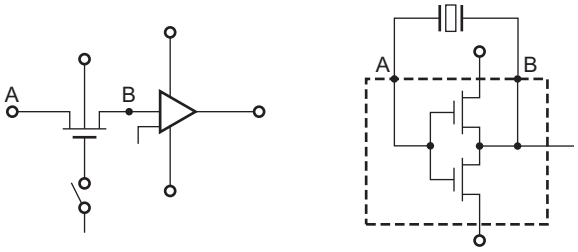
Figure 5.2 Example of Transient Thermal Resistance

5.2.5 Using a Device with Equivalent Function

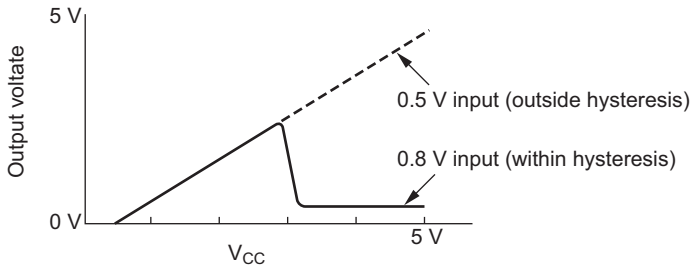
Of the characteristics of a semiconductor device, while there are items that are related to characteristics explicitly listed in the documentation, there are others that, while not explicitly listed in the documentation, can actually be used without problem. However, we strongly recommend that users thoroughly analyze these latter characteristics, including checking for variations between individual semiconductor devices.

Examples of this kind of situation would be using a standard digital circuit as an operational amplifier in an oscillator circuit, and using an output signal at a voltage at which operation is not guaranteed in a transient state when power is turned ON.

Example 1 Malfunction when a MOS IC is Used in an Analog Circuit

No. 1	Example	Malfunction when a MOS IC is used in an analog circuit
Type of device		MOS IC
Point		Caution is required as to the amount of margin in a circuit when the input leakage current fluctuates.
Outline of example/ phenomenon/cause		When a MOS IC was used as an oscillator circuit or analog switch, the allowable leakage current was less than that for a digital circuit; a leakage current that is too large can cause a malfunction. Not only leakage current in the semiconductor device itself, but also between terminals of the printed circuit board (due to adhering dust) is a problem. 
Countermeasures/ verification examples		1. Coat the printed circuit board so that dust will not adhere to it. 2. Improve the environment under which the device is used (reduce the humidity). 3. Design the printed circuit board so that the resistance between A and B will be 10^9 Ω or more.

Example 2 Erroneous Output from a Schmitt Trigger IC when Power is Turned ON

No. 2	Example	Erroneous output from a Schmitt trigger IC when power is turned ON
Type of device		TTL IC
Point		Exercise caution with regard to transitional phenomena when power is turned ON.
Outline of example/ phenomenon/cause		If the power to a circuit using a Schmitt trigger IC is turned ON while the input is at L level (0.8 V), even though the IC is an inverter the output became L. This phenomenon occurred because of the IC's hysteresis characteristics; if power is turned ON while the input is within the hysteresis range (about 0.7 V to 1.6 V) the output becomes unstable and the circuit does not operate normally. 
Countermeasures/ verification examples		1. Keep the input outside of the hysteresis range until Vcc has reached a steady state. 2. Use a type of semiconductor device that does not have hysteresis characteristics.

This applies also to recent microcontroller devices which include mask ROM versions, PROM versions, ZTAT and F-ZTAT versions, which have exactly the same functions but differ in the way of programming. There are differences in characteristics that are not stated explicitly in the specifications, such as noise margin without malfunction, noise generation, and oscillator circuit stability.

Example 3 Difference between ZTAT Version and Mask ROM Version in Electromagnetic Emission (EME)

No. 3	Example	Deterioration when subjected to noise, caused by changing the mask
Type of device		Microcontroller
Point		Care is required regarding performance not stipulated in the specifications when modifying the masks.
Outline of example/ phenomenon/cause		In a ZTAT microcontroller, prototyping and initial mass production were completed and then there was a switchover to a mask ROM version with the same pin layout in order to proceed to full-scale mass production. When that was done, the level of noise generation increased, causing malfunction of the scanning station selection function of an adjacent FM radio (noise caused the radio to judge that there was a station at a frequency at which there was not). Adjustments were made in the printed circuit board ground wiring pattern layout and in the location of the bypass capacitor, tentatively solving the problem, but this caused delay in the timing of mass production, and in the meantime it was necessary to continue using the expensive ZTAT microcontroller.
Countermeasure/ verification examples		The mask ROM version functional specifications have been adjusted to those of the ZTAT microcontroller as much as possible, but depending on the series used, there will be some products that differ somewhat in their functions. For example, even if the functions themselves are exactly the same, the products can differ in some characteristics that do not show up in official specifications (for example ability to withstand noise, latch-up, vulnerability to electrostatic breakdown, etc.), and these things shall be checked out in advance using the actual semiconductor device. If there are characteristics that make the device difficult to use or if improvements are necessary, please contact Renesas's technical marketing department.

5.2.6 When a Device is Used in a Severe Environment

In particular, it is necessary to thoroughly consider the possibility that a failure may be caused by wear-out. Unless derating is done correctly in the wear-out region, during the usage period, the device will enter the region where the failure rate increases rapidly with time, resulting in serious problems. Thus this is extremely important.

5.2.7 Package Selection

Semiconductor device package types include two main types: (1) hermetic sealed packages, such as metal sealed packages, ceramic sealed packages, glass sealed packages, low melting point glass sealed CERDIP (CERamic Dual-Inline Package) packages; and (2) plastic encapsulated packages.

In addition, packages are categorized as either THD (Through Hole Device) packages or SMD (Surface Mounted Device) packages according to how they are mounted.

Recently, advances in the functionality, miniaturization, and cost performance of sets that use semiconductor devices have led to higher integration of semiconductor devices and, consequently, higher pin counts, thinner packages, and a greater variety of structures and mounting methods.

The semiconductor device package (characterized by encapsulation type, shape, leads, etc.) that is used in a customer set shall be selected from among the various available packages as the package that best meets the set's entire array of requirements including its use objective, size, shape, use environment, reliability targets, semiconductor device mounting conditions, and so on.

When designing such sets, package-oriented device selection shall be based on how well the package's shape, functions, performance features, and reliability features meet the above-mentioned set requirements.

5.3 Cautions Concerning Design for Safety

5.3.1 What Is Design for Safety?

In the EC Mechanical Directives and U.S. MIL standards (MIL-STD-882), the following principles are set forth concerning the following type of design for safety efforts with regard to products, equipment, and systems.

1. Design to minimize risks. (Design for Safety Principle 1)
2. Use safety devices and/or protective measures to reduce any risks that cannot be eliminated. (Design for Safety Principle 2)
3. If an unacceptable amount of risk still exists after safety devices and/or protective measures are introduced, attach warning labels concerning the risk. (Design for Safety Principle 3)
4. Establish clear-cut training procedures for users concerning all work processes including proper wear of protective garments. (Design for Safety Principle 4)

Here the term “risk” refers to the probability that damage or harm may occur due to products or equipment, and to the size of that liability. The size of a loss occurrence is determined by the degree of the harm to human life or property.

Under current product liability laws, the existence of defects in manufactured goods is a correlation between the utility of the manufactured goods (products, equipment, etc.) and the amount of risk as defined above, and such defects are judged to exist when a risk exists that is not within the design tolerances or socially accepted norms. If damage or injury to human safety or life, property, or the environment occurs due to a manufactured product and if the existence of a defect in said product and the causal relationship between that defect and that damage or injury are both confirmed, it is common knowledge that the manufacturer bears liability for compensation of the damage and/or injury.

Design for safety as it relates to products and equipment is intended to prevent damage or injury to human safety or life, property, and the environment by eliminating or at least reducing to acceptable levels any risk of such damage or injury. Therefore, the types of design measures described in 1 to 4 above are implemented as part of the design for safety approach.

Regardless of whether or not the above-mentioned EC directives or MIL standards are applied, it is clearly essential for design for safety to be implemented as part of the company’s obligations toward the customers of the client companies that plan, design, develop, and manufacture sets as well as toward society as a whole.

For its part, Renesas implements a variety of design-, manufacturing-, and labeling-related measures to eliminate or at least minimize faults and defects in semiconductor devices.

Renesas’s design for safety approach can be understood based on this manual’s contents.

In view of the above liability considerations, all of Renesas’s semiconductor device data sheets, data books, user’s manuals, and other documentation include the message concerning product liability.

5.3.2 System Safety Concepts

Many of the sets or electronic equipment units that use semiconductor devices are system equipment, as is typical of high-tech products. As such, these products tend to contain numerous parts, materials, components, software, and sub systems that have been manufactured or purchased by set manufacturers (Renesas’s customers), all of which are integrated according to the use objectives. Furthermore, in many cases, such system equipment is often used in combination with other system equipment models that are manufactured by a third party.

Accordingly, the safety of such a system depends profoundly on the functions and safety of the equipment, parts, materials, components, software, subsystems and third party equipment that comprise that system.

Design for safety as it relates to such system goes beyond the concept of product safety (PS) and is instead based on what MIL-STD-882 refers to as “system safety”.

The system safety concept refers to systematic engineering and management methods to optimize the safety of systems. These methods have the following two characteristics.

1. Clearly defined management of the interface conditions existing among parts, materials, components, software, sub systems, the people using systems, and the use environment, along with clarification of the risk-related liabilities.
2. Evaluation of risks at each phase in the life cycle of a system, from planning to design, development, manufacture, operation, and disposal, along with planning to eliminate or reduce such risks.

Renesas asks all of its customers to implement design for safety with regard to the sets they manufacture, based on the above system safety concept.

5.3.3 Design for Safety Concerning Sets that Use Semiconductor Devices

When designing a set that uses semiconductor devices, the above-mentioned system safety concept demands that design for safety be implemented so as to evaluate the risk of failures and defects in semiconductor devices at every phase in the set's life cycle and to reduce such risks to acceptable levels.

The first step in design for safety for sets that use semiconductor devices is to select semiconductor devices that have the required quality, reliability, and safety characteristics. The second step is to select the most important elements in terms of reducing applied stresses.

The amount of risk that is considered acceptable differs according to the application. It is therefore necessary to select semiconductor devices that have sufficiently high reliability and/or low failure rates to keep the risk within the allowable range.

The reliability, degradation, and failure of semiconductor devices also depends on the amounts of various stresses that are applied to semiconductor devices, such as voltage, current, power, temperature, humidity, mechanical stresses such as vibration and shock, thermal stresses, electromagnetic wave, light, radioactive rays, corrosive gas, and dust.

Therefore, a set's design conditions, use conditions, and environmental conditions shall not only meet with maximum allowable stress levels of semiconductors to be used, but shall also have stress levels set as derated as possible.

Appropriate derating of stress, along with careful selection of semiconductor devices with a view toward appropriate quality, reliability, and safety features for the target set will enable risks associated with semiconductor device faults or defects to be reduced, which in turn will eliminate or reduce to acceptable levels the risks associated with the target set that contains semiconductor devices.

5.4 Precautions in Circuit Design

Circuits are classified into two categories, analog circuits and digital circuits.

Analog circuits, typified by PLL circuits, sacrifice gain to obtain accurate amplification factor by means of a feedback circuit between the input signal and the output signal. They can also generate a variety of functions. They can also compare, detect, and integrate the phase difference between input signals, and use a voltage-frequency conversion circuit to tune the phase difference. In all cases small differences between input signals are greatly amplified for use, so it is easy for noise that is included in the input signal to have a considerable effect, and the output is very sensitive to fluctuations in the electrical characteristics of constituent elements. Consequently, small changes in leakage current and changes in gain can develop into a malfunctioning condition. Therefore it is necessary to design the circuit while comprehending the worst case conditions among the electrical characteristic specifications in sensitive parts of the circuit.

In contrast, in a digital circuit, the levels of the input signal and the output signal are standardized, and a noise margin between the two signals is set, which is advantageous with respect to fluctuations in the characteristics of constituent elements. On the other hand, if a malfunction does occur, it has the potential to grow into a very serious malfunction, depending on the meaning of the signal that is affected. Recently, in semiconductor devices which contain programs such as microcontrollers, once the content of the program is changed, even if the immediate cause of the malfunction is removed the original operation cannot be restored, so that the damage caused is greater than in the case of an analog

circuit. When malfunction occurs in a digital circuit, whether the input level, output level and timing margin are being observed correctly are important points. In addition, particularly during transient periods such as when the power is turned ON or OFF, one important precaution is to design the circuit so that the effect of environmental conditions under which correct operation is not guaranteed does not remain after regular operation starts.

(1) General Cautions

The following measures shall be implemented during circuit design for reliable designs, preventing malfunctions (such as latchup) due to noise or external stresses, to prevent functional degradation, and for safe designs.

1. Set operating conditions such as voltage, current, power, and ambient temperature within the maximum ratings.
2. Perform a careful thermal design and keep the ambient temperature as low as possible.
3. Variations in the supply voltage applied to semiconductor device shall be held to within the range stipulated in the product documentation.
4. Isolate GND lines.
5. Insert filters or other mechanisms to attenuate surges on power supply lines.
6. Insert (between VDD and GND) capacitors matched to the frequency for eliminating surge or noise to each node of the PCB power supply lines.

   Examples: High-frequency filter: 0.01 to 0.1 μF
   Low-frequency filter: 10 to 100 μF
7. Use a low-impedance shield line for long wiring on the PCB.
8. Suppress the noise level by inserting (parallel to noise sources) diodes and capacitors that have good high-frequency characteristics.
9. Set up correction circuits to increase the noise margin in target circuits.
10. Prevent external factors (such as noise, surges, vibration, ambient temperature, the operating environment) that may become external stresses from affecting circuits.
11. Avoid generation of static electricity discharges during use or minimize their effect.

(2) Cautions Concerning Circuit Design of Systems Using Semiconductor Devices

(a) Cautions Related to Power Activation

Semiconductor devices are susceptible to being damaged as a result of any over-currents that flows during the interval between power on and reset signal input. Such an over-current may be floating in the device before power on and may flow if it is not first initialized. Inputting a reset signal initializes the device and eliminates over-current. Semiconductor devices that have a power on reset circuit never have such over-current flow problems.

As shown in Figure 5.3, when the LSI's shared I/O pins are used in input mode, any external output circuit that outputs a signal shall be connected to one of these pins. Right after the power is activated, the LSI remains internally uninitialized, so it is impossible to know when the LSI's internal output enable signal becomes active (high). Thus, when the LSI's internal output buffer and an external output circuit have different potentials, an over-current measuring at least several dozen mA flows. If a reset signal is input, all shared I/O pins will be set to input mode (output enable signal becomes inactive), stopping the over-current's flow.

Perform the following measures to prevent overcurrent damage at power on.

1. Insert a resistor (about 1 kΩ) between the external output circuit and the shared I/O pin. Note, however, that in such cases the resistor may reduce the propagation speed of the output signal from the external output circuit.
2. Set up a power on reset circuit external to the LSI and input a reset signal and a power on signal at the same time.

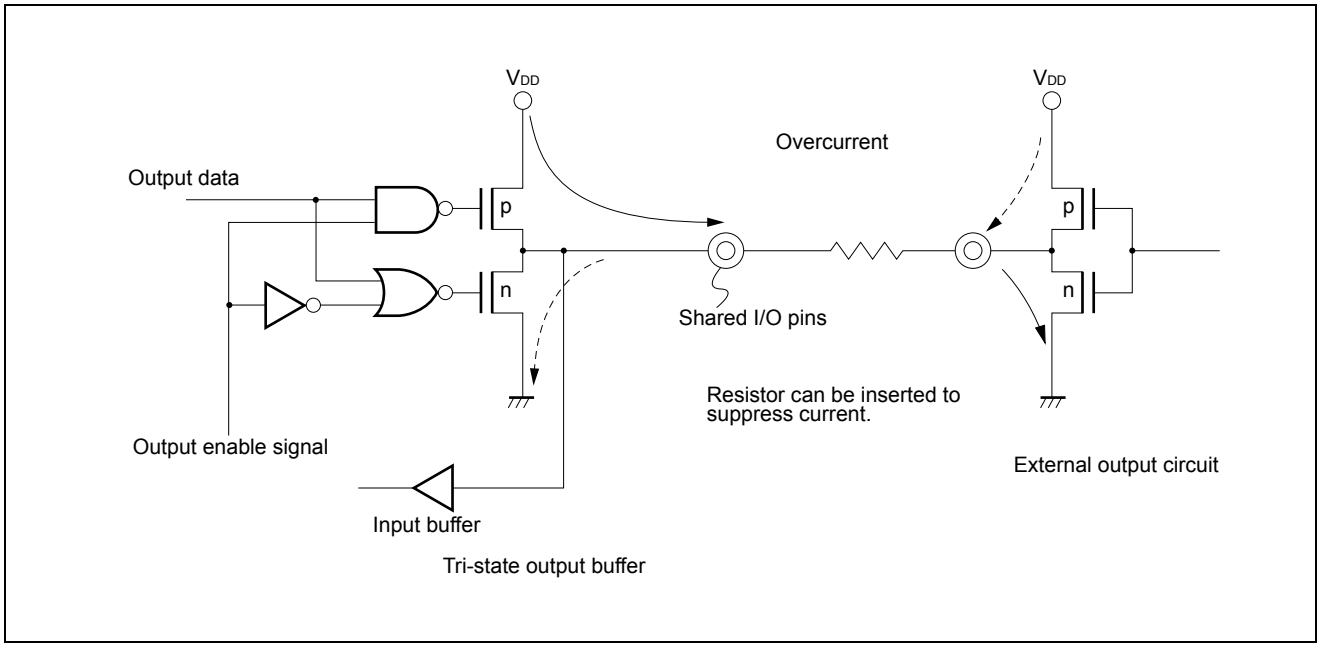


Figure 5.3 Example of LSI with Reset Signal Input Pin

When a composite power supply is used, observe the power-on sequence to prevent malfunction or destruction of products. For details, see the User's Manual of each product.

(b) Cautions on Load Drivers

LSI output circuits have a maximum output current rating. If the resistance value is too low, such as in a current limiting resistor for an LED driver (shown in Figure 5.4) or in an open drain pin's pull-up resistor (shown in Figure 5.5), the LSI risks being damaged by an overcurrent. Be sure to determine resistance values that will keep the output current to within the rated values.

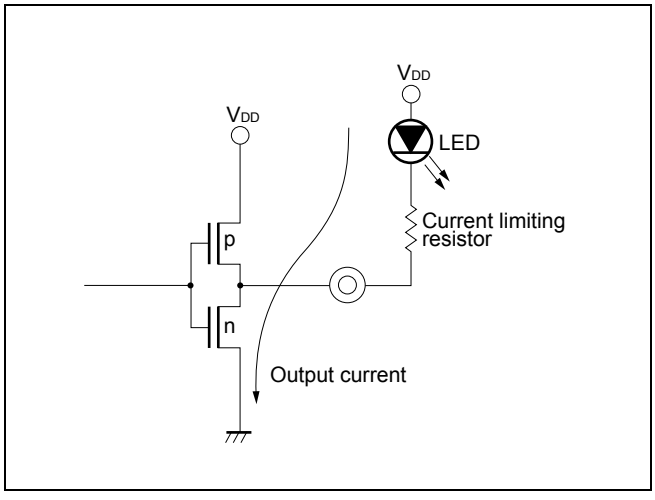


Figure 5.4 Caution Concerning Load Driver

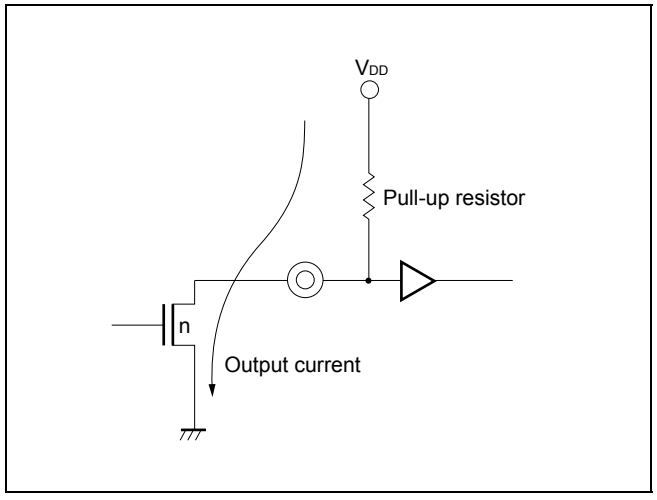
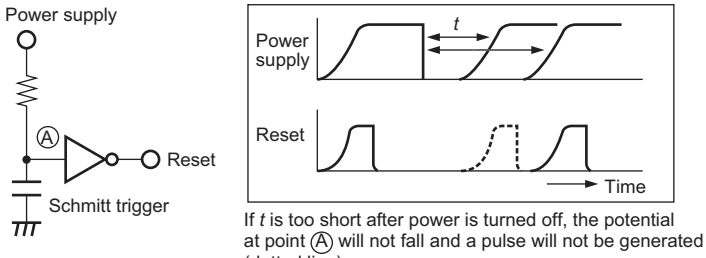
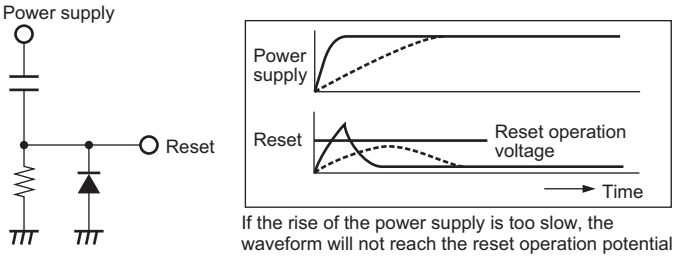
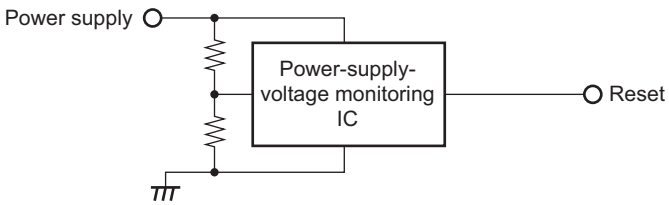


Figure 5.5 Caution Concerning Load Driver

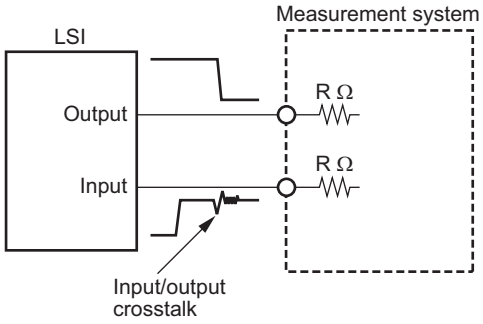
Example 4 TTL-CMOS Interface

No. 4	Example	TTL-CMOS interface
Type of device		TTL, CMOS IC
Point		Undershoot and overshoot shall be within the specified range.
Summary of example/ phenomenon/ cause		When CMOS LSIs are driven by TTL ICs, a malfunction may occur due to undershoot noise or insufficient input level. Undershoot is caused by reflection due to the imbalance between the low output impedance of the TTL IC and the extremely high input impedance of the CMOS LSI. Insufficient input level is also caused by the significant difference in the input level between TTL and CMOS. Particularly, the TTL level output does not rise to Vcc level, which will cause a problem.
Countermeasure/ verification examples		1. Insert a resistor at output pins of TTL IC to prevent undershoot. 2. Attach a pull-up resistor to input pins of CMOS IC. 3. Use a special interfacing IC.

Example 5 Malfunction of Power-On Reset Circuit

No. 5	Example	Malfunction of power-on reset circuit
Type of device		IC, LSI
Point		An appropriate type of power-on reset circuit shall be used for the power-up waveform.
Summary of example/ phenomenon/ cause		There are two types of power-on reset circuits, integral and differential. The integral type is vulnerable to short-time power supply interruption, whereas the differential type is vulnerable to slow rises in voltage. Due to this, circuits may malfunction as shown in the figure below. 1. Malfunction of integral circuit  If *t* is too short after power is turned off, the potential at point Ⓐ will not fall and a pulse will not be generated (dotted line). 2. Malfunction of differential circuit  If the rise of the power supply is too slow, the waveform will not reach the reset operation potential and a reset will not be effected (dotted line).
Countermeasure/ verification examples		Replace the current power-on reset circuit with the power-supply-voltage monitoring IC shown in the figure below. 

Example 6 Malfunction during Measurement

No. 6	Example	Malfunction during measurement
Type of device		MOS LSI
Point		The impedance of measurement systems shall be appropriate.
Summary of example/ phenomenon/ cause		During measurement, resistors were connected to the measurement system (see figure below) to prevent damage. This caused cross-talk between adjacent input and output pins, thus resulting in a defective input voltage margin. A single measurement system was shared for testing products with different pin layouts, with a resistor connected not only to the output pin but also to the input pin during measurement. 
Countermeasure/ verification examples		Modify the system so that the appropriate resistor for protecting the measurement system can be selected by a relay depending on the pin specifications (input/output) to allow selecting the 0-Ω resistor for input and R-Ω resistor for output.

5.5 Cautions on Thermal Designing

The effects of thermal factors on the reliability of semiconductor devices during actual use can be profound. In particular, the advent of ever smaller, flatter, and faster semiconductor devices in recent years has made thermal resistance a matter that cannot be ignored.

The operating junction temperature of ordinary semiconductor devices is determined by a mutual interaction between temperature conditions in the device's environment and increases in junction temperature that occur within the devices themselves.

Figure 5.6 illustrates an SMD that has been mounted on a PCB.

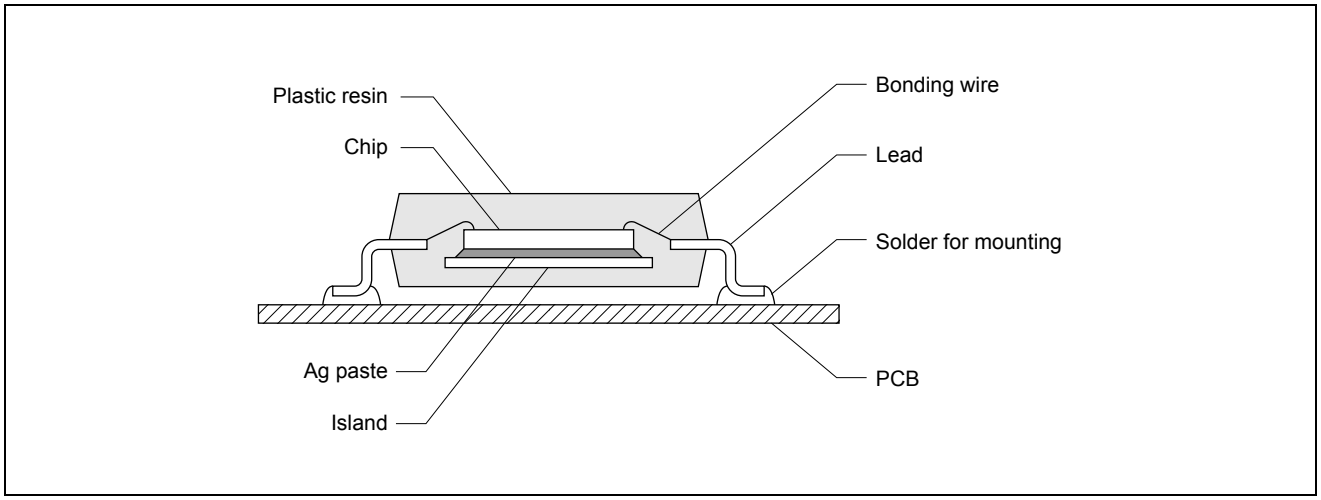


Figure 5.6 Example of SMD Mounted on PCB

Generally, heat is propagated in three ways: by conduction, convection, and radiation. In SMDs, heat propagation is determined by conduction and convection, as shown in Figure 5.7. Heat that occurs at a junction is dispersed by thermal conduction to various other areas, after which it is released to the outer air by convection from the surface of the SMD. However, an adiabatic condition occurs in the gaps between the surface of an SMD and the PCB due to the fact that the gap is too narrow (less than 1 mm) to disable convection.

The ease (or difficulty) with which heat is propagated is called thermal resistance.

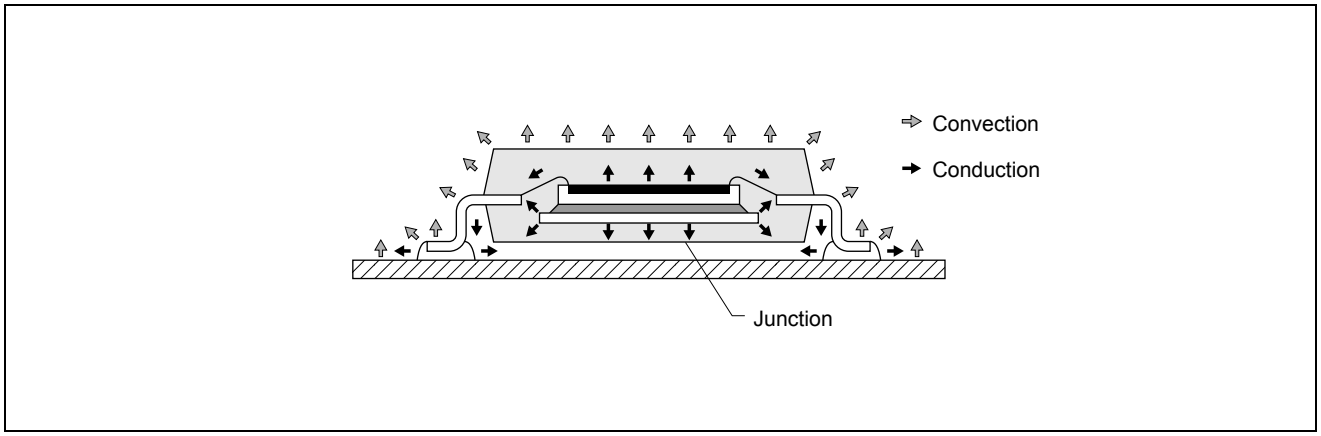


Figure 5.7 Propagation of Heat in SMD

In the recent trends toward smaller, flatter, and faster ICs, heat has become an important factor affecting reliability. At the same time, the amount by which thermal resistance can be lowered in semiconductor devices themselves is approaching the limit. Given this situation, the thermal design of entire systems that include semiconductor devices is becoming an increasingly important issue.

5.6 Cautions on Use Environment

This section describes cautions on the storage and use environments of semiconductor devices that are built into a set.

(1) Temperature Environment

Do not store end products (that are in the power off state) at temperatures that exceed the maximum rated range of the storage temperature for the semiconductor devices used in that product. The electrical characteristics of semiconductor devices are acutely sensitive to temperature. To achieve the desired electrical characteristics, the ambient temperature or the chassis temperature shall be controlled to be within the operating temperature range. Also, to prevent degradation of the semiconductor devices and to assure the lifetime of those devices, consider derating the operating temperature.

(2) Humidity Environment

End products shall be designed so that the environmental humidity around the semiconductor devices within the end product is maintained at about 45 to 75 %RH, and furthermore, care shall be exercised in using the end products to assure this condition is met. Also, since condensation is a concern when the end product is used in enclosed spaces or places subject to rapid temperature changes, avoid using end products in such environments.

If a set is used for a long time in a highly humid environment or an environment in which condensation occurs, plastic-encapsulated semiconductor devices may absorb moisture, and such moisture absorption can cause chip degradation or faults. Recent semiconductor devices tend to have higher pin counts and a smaller pin pitch (interval between lead pins), which makes it easier for leakage to occur between pins on the PCB, which in turn can cause operation faults.

If a high-humidity environment cannot be avoided due to the purpose of use or the installation site, consider implementing appropriate anti-humidity measures for the semiconductor devices and the PCB.

When a set is used in a low-humidity environment, there is a risk of semiconductor device wear-out damage due to electrostatic discharge (ESD). If a low-humidity environment cannot be avoided, consider implementing ESD countermeasures such as those described in section 5.7 below.

(3) Strong Electromagnetic Field

If a set contains a power supply that generates a strong electromagnetic field or if a strong electric field or electromagnetic field is otherwise generated near a set (such as office equipment, production machinery, etc.), the set or its internal circuits may suffer electromagnetic disturbances. Such disturbances include conduction noise on power supply lines or telephone lines or radiant noise that is propagated as electromagnetic waves. This noise can cause semiconductor devices or circuits to operate incorrectly. To prevent circuit function faults caused by electromagnetic disturbances, consider optimizing the circuit layout pattern on the PCB, making the power supply and GND lines thicker, using shield lines, and designing the layout so that electromagnetic shields are also attached to semiconductor devices or circuits.

(4) Electromagnetic Interference

Electromagnetic interference waves include conductive noise that is transmitted over power supply lines and telephone lines, and radiation noise that is directly radiated from a system as electromagnetic waves. The measurement method and countermeasures to be taken against these waves differ for each type of noise. One aspect that makes it difficult to prevent and contain these waves is that there is no way to calculate the strength of the electromagnetic waves generated from the respective parts of the system at the design stage. Possible countermeasures include selecting and providing optimum shielding in the finished product, taking the measurement result for the finished product into consideration.

(5) Radioactive Rays

Semiconductor devices that are not designed to be anti-radioactive devices may suffer wear or operation faults caused by radioactive rays or strong cosmic rays. Unless otherwise noted, Renesas's standard-grade semiconductor devices are not designed as anti-radioactive devices. Therefore, when using such devices in an environment in which radioactive rays may be generated or received, design measures shall be taken to shield the semiconductor devices or circuits from radioactive rays and cosmic rays. In some products, radiation such as cosmic rays arriving on earth might cause an unpredictable error (for example, bit inversion in a memory cell). This type of error is called soft error. Consider using an error-correcting code or other safety design feature suitable for the system environment when the device is designed.

(6) Corrosive Gas, Salty Air, Dust, Oil Fumes, etc.

If semiconductor devices are used in an environment containing a corrosive gas such as SO_x or NO_x or if the air is very salty, leads can become corroded, causing degradation of characteristics. If such an environment is also a high-humidity environment, such degradation can accelerate and a large amount of leakage may occur due to chemical reactions between leads. If semiconductor devices are used in an environment containing a lot of dust or oil fumes, similar degradation or leakage between leads may occur due to the humidity-preserving tendencies of dust and oil. Therefore, use in such environments shall be avoided or, if unavoidable, consider including measures to prevent such degradation or leakage between leads in the set design.

(7) Vibration, Shock, and Stress

Semiconductor devices shall be designed, manufactured, stored, shipped, and used in ways that protect them from exposure to vibration, shock, mechanical stresses, and thermal stresses during their entire service life from PCB mounting to usage in sets. When a strong vibration, shock, mechanical stress, or thermal stress is applied to a semiconductor device, problems such as reduced reliability, wire breakage, and package or chip cracking may occur. Special care shall be taken to avoid exposing semiconductor devices to mechanical shock and thermal shock as they are mounted, as well as to vibrations or shocks that can occur during shipment or use of sets.

(8) Optical Effects

Optoelectronic effects in semiconductors is a well known issue and irradiating a semiconductor device in light can cause electromotive force to occur, which can lead to operation faults. To prevent leakage or operation faults that may occur due to irradiated light, design sets so that their semiconductor devices are not unnecessarily exposed to direct sunlight, ultraviolet rays, fluorescent lamps, etc.

(9) Smoke and Flames

Since semiconductor devices are not fireproof, there is a risk that such devices may begin to smoke or burn when exposed to an overcurrent. Toxic gas may also be emitted from smoking or burning devices. To prevent such occurrences, overcurrent prevention measures such as inserting series resistors between the power supply and semiconductor devices may be required to prevent overcurrents from flowing when an operation fault or a short occurs. Also, do not use the end product in the vicinity of heating elements, incendiary materials, or flammable materials.

(10) External Noise

If the wiring lines (including those for I/O signals and other signal lines) on the PC board are too long, the semiconductor devices on the board may be more easily affected by externally induced noise and surge currents, and certain devices may malfunction. As countermeasures, consider keeping the wiring length short, lowering the impedance, and inserting a noise eliminators.

Example 7 Decrease of the Operation Margin by Light Illumination

No. 7	Example	Decrease of the operation margin by light illumination
Type of device		Microcontroller
Point		For an application in which strong light is to be used, measure under the actual conditions of use.
Summary of example/ phenomenon/ cause		When strong light is applied on a semiconductor, photoelectrons are produced. If there is a possibility that strong light will be incident on the LSI during use, exercise caution. Caution is particularly necessary when the package is thin and/or chips are purchased and assembled.
Countermeasure/ verification examples		1. When the electric characteristics of a bare chip are measured, shut off the incoming light. 2. For an application in which strong light is to be applied to a packaged product, measure the electric characteristics while applying light.

Example 8 Leakage Defect Caused by Sulphide Gas Emitted by Natural Rubber

No. 8	Example	Leakage defect caused by sulphide gas emitted by natural rubber
Type of device		IC, LSI
Point		A substance of which sulphur is the main constituent, such as rubber, shall not be in close proximity to the IC.
Summary of example/ phenomenon/ cause		Malfunction of unknown origin occurred in the market; as the result of an investigation it was judged that a sulphide substance had crystallized between LSI pins, amplifying the leakage current and causing malfunction. The result of the investigation further revealed that there was a buffer component made of a substance that had sulphur as its main constituent, such as rubber, in close proximity to the LSI; sulphide gas emitted from that substance cause dew in high humidity, causing the foreign chemical substance to be formed between the LSI leads. In an experiment conducted to reproduce the phenomenon in a high temperature, high humidity tank, it could not be reproduced, but when an identical rubber component was inserted into a desiccator and a test was conducted at high temperature and high humidity, it was reproduced. (This defect does not occur in a well-ventilated location.)
Countermeasure/ verification examples		Do not place or mount any substance having sulphur as its principal constituent, such as rubber, in close proximity to an IC.

Example 9 Malfunction Caused by Surge Current when Power is Turned ON

No. 9	Example	Malfunction caused by surge current when power is turned ON
Type of device		Microcontroller
Point		The power-supply current is correct between the time the power is turned ON and the start of oscillations.
Summary of example/ phenomenon/ cause		After power is turned ON, until clock input, there was an indeterminate section in the internal logic, and a current exceeding the current rating flowed in the power supply. Part of the users system had internal circuits to detect excess current flow; this current caused the device to malfunction.
Countermeasure/ verification examples		In an application in which it is necessary to detect excess current, the peak power-supply current, as well as the average power-supply current, shall be specified.

5.7 Protecting Semiconductor Devices from Electrical Damage

Defects due to electrical damage are the most frequently occurring type of semiconductor device failure and it is very difficult to trace the cause of destruction from its aftermath. When the incidence of destruction is high, additional testing is conducted and specific measures are taken in an attempt to find the conditions that reproduce the same form of destruction, but in reality, it is extremely difficult to reproduce the forms of destruction that are exactly the same as those in the field.

This section, focusing on destruction mechanisms, summarizes the characteristics of destruction, and the approach to prevention and countermeasures. Correct, careful handling of sensitive semiconductor devices during production processes can be expected to have a large effect on the reduction of defects during both the clients' production processes and the period of early failures in the field.

5.7.1 ESD Damage

Damage due to electrostatic discharge is the most frequently occurring mode of destruction defects. Following, we summarize the mechanisms that charge semiconductor devices, the mechanism of damage and general precautions.

Damage of semiconductor devices by electrostatic discharge is caused by sudden discharges resulting from excessive electrical voltages and excessive currents. Except for certain devices designed to handle extremely high frequencies, most semiconductor devices include internal protective elements to prevent damage from ESD. Damage of the devices due to electrostatic discharge will still, however, occur when static electricity that exceeds the level of protection provided by the protective elements is applied to the device, or when a high-frequency surge exceeds the speed of the protective elements.

After semiconductor device has been mounted on a circuit board or apparatus, from the concept of distributed-constant circuits, applied static electricity concentrates at the point of lowest impedance to become a stray current, and then causes destruction at the weakest point. The semiconductor device itself is processed and manufactured at extremely high temperatures, so destruction will not result in a short time if the temperature rises. However, when energy consumed is intensely concentrated, the temperature rises locally and destruction occurs instantly. When the static electricity itself causes the destruction, the voltage is high and the amount of energy is comparatively low, so there is a minute damage and, in many cases, it cannot be observed. If static electricity is applied when the electric power is on-state, the resulting electrostatic destruction will in some cases induce secondary thermal runaway and Safe Operating Area (SOA) destruction.

(1) Mechanisms for the Generation of Static Electricity

Static electricity is the charging of a material by either excess or a shortage of electrons. When a material has an excess of electrons it is negatively charged, and when it has a shortage of electrons it is positively charged.

Materials generally have an electrical quality of either acquiring electrons or of giving them up (the triboelectric series). For this reason, when two materials rub, make contact, separate, or create friction, one material acquires electrons while the other gives them up (Figure 5.8). When a conductive material comes into proximity with a charged material, local charging will occur because of electrostatic induction (Figure 5.9). The amount of charge in the materials depends on the material properties, the surrounding conditions (temperature and humidity), and the conditions in terms of friction. However, large charges are generally generated in chemical fibers and plastics (these materials are easily charged). Since static electricity charges the surface of a material, the material's surface conductivity will also have a strong effect on charge transfer. When the surface conductivity is high, the charge will diffuse quickly. Table 5.8 shows examples of electrostatically generated voltages. Since surface conductivity increases with humidity, the higher the relative humidity the lower the electrostatic voltage.

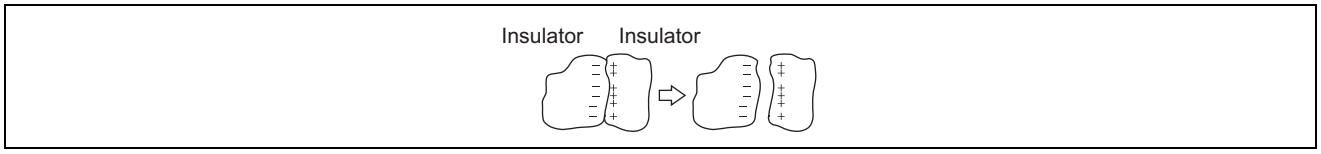


Figure 5.8 Triboelectric Charging

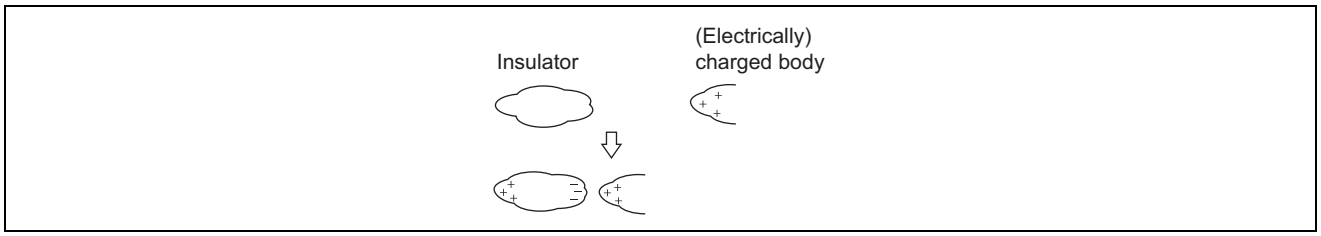


Figure 5.9 Electrostatic Induction

Table 5.8 Examples of Typical Electrostatic Voltages (From DOD-HDBK-263)

Source	Electrostatic Voltage Potential	
	10 to 20%RH	65 to 90%RH
A person walking on a carpet	35,000 V	1,500 V
A person walking on a vinyl floor	12,000 V	250 V
A person working at a bench	6,000 V	100 V
Vinyl covering	7,000 V	600 V
Lifting a polythene bag from a bench	20,000 V	1,200 V
Polyurethane packed chair	18,000 V	1,500 V

(2) Mechanisms that Charge Semiconductor Devices

Of the recent cases of static destruction of semiconductor devices, cases due to the charged device model are increasing. This mode of destruction occurs when a charged semiconductor device model discharges to a conductor. The mechanisms that charge semiconductor devices that induce discharges are described below.

(a) Triboelectric Charging of Package Surfaces

Friction is often applied to semiconductor device in the manufacturing process or during assembly of the devices into electronic instruments. Examples are friction with the rubber roller of the device-stamping machine, within the IC magazines, and device handling instruments. When friction is applied to plastic packages, the surface of the package becomes charged. When the package is charged, electric charge is electrostatically induced in the chip and its leads by electric fields within the package, and the leads discharge when they make contact with a conductor (Figure 5.10).

(b) Device Charging by Electrostatic Induction

In addition to description (a) above, Figure 5.11 gives examples of charging that occurs even in the absence of friction. When semiconductor device is placed on a charged plastic board, electrostatic induction takes place in the chip and leads as shown in Figure 5.11 (i).

Then discharge occurs when tools or human bodies make contact with the leads of Figure 5.11 (ii). Also, after the device is removed from the plastic board, there is a further danger of discharge after it has been picked up from a board as shown in Figure 5.11 (iii).

This shows that there is a danger of semiconductor device discharge when charged materials are simply brought into proximity with each other. The containers into which semiconductor devices or completed boards are placed, conveyor belts, and non-conductive gloves can all cause semiconductor device discharge.

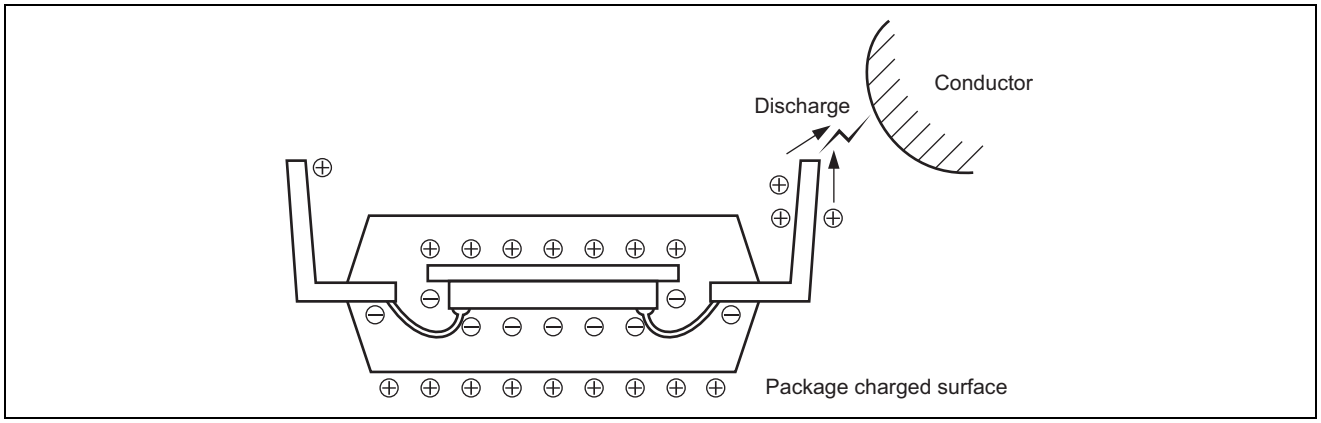


Figure 5.10 Internal Electrostatic Induction and Discharge when the Package Surface is Charged

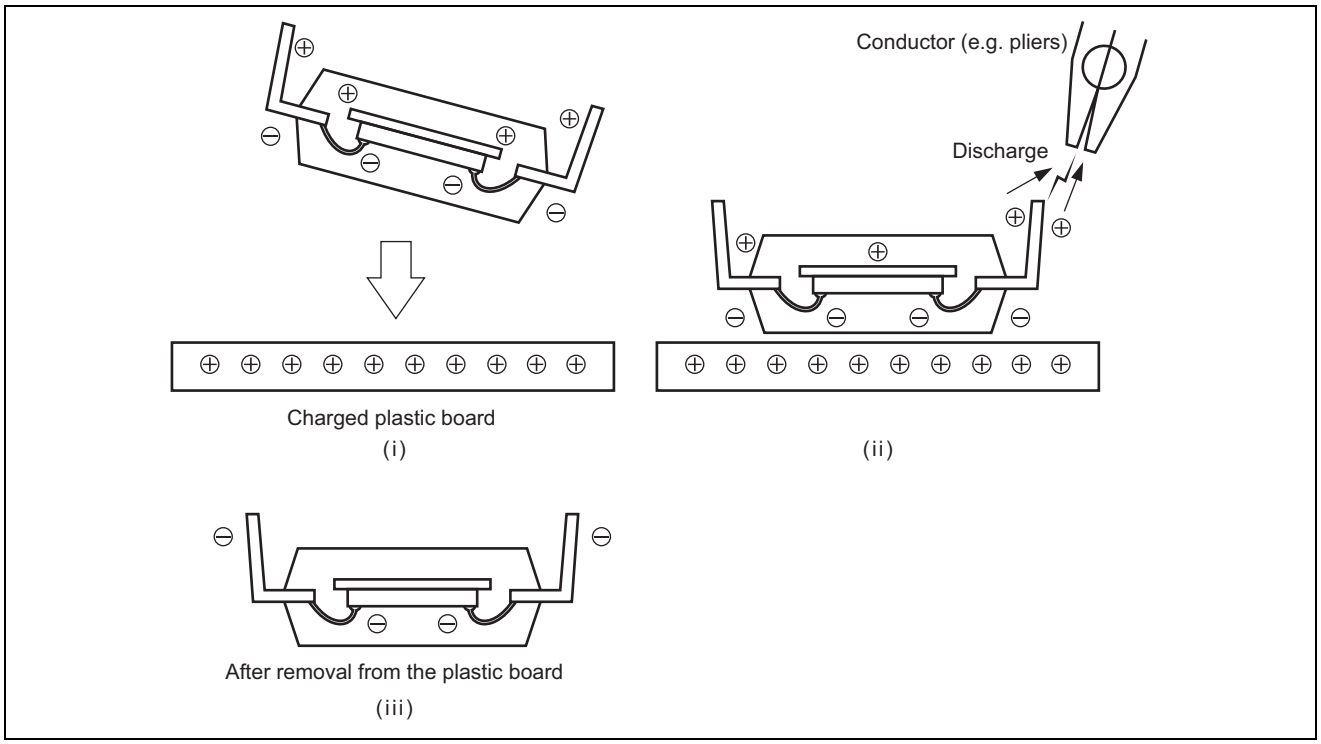


Figure 5.11 Process of Device Charging by Electrostatic Induction

(3) General Precautions against ESD Damage

Caution is necessary in handling semiconductor devices since they are generally susceptible to destruction due to electrostatic discharge. The possibility of electrostatic discharge is especially high in the cases listed below. This section presents the most common countermeasures used for preventing damage by static electricity.

(a) Contact between Devices and Conductors

When conductors or semiconductor devices are charged, discharges can occur between them. All personnel who handle such devices and equipment shall be grounded through a resistance of 1 MΩ or greater. For metals objects, the danger of semiconductor device destruction is greater due to rapid discharge. Bringing semiconductor devices into contact with metal objects shall be avoided as much as possible, but, when such contact is unavoidable, the metal shall be grounded and any residual charge shall be removed from the semiconductor devices.

(b) Device Subjected to Friction

Packages become charged when they are subjected to friction, and when the lead pins are rubbed, the chips and lead pins also become charged. It is necessary to reduce the amount of charge by preventing friction or changing the material that may be subjected to friction.

(c) Charged Tools Brought into Proximity with Semiconductor Devices

Semiconductor devices are charged by electrostatic induction. The material of tools shall therefore be exchanged for anti-static material.

(d) Drops in the Humidity of Surroundings

When handling semiconductor devices, if the humidity in the vicinity falls, semiconductor devices or tools, once charged, can not easily return to their original condition. Since static electricity is invisible, it is not easy to institute perfect countermeasures to the above-mentioned factors (a)–(c). When executing these countermeasures, greater effectiveness can be expected if the humidity is also controlled.

(4) Basic Methods for Preventing ESD when Handling Semiconductor Devices

To prevent ESD-related degradation or damage to semiconductor devices, the electrostatic voltage of all charged bodies in the environment in which semiconductor devices are handled shall be kept to within 100 V. The basic methods for doing this include suppressing the occurrence of static electricity whenever possible and enabling any electrostatic charge that does occur to be safely discharged.

Five basic methods for controlling ESD while handling semiconductor devices are described below.

1. Use grounding and avoid using insulating materials on all objects (including human bodies) that touch or approach semiconductor devices. To avoid buildup of electrostatic charges, it is better to use a conductive material that has a high resistivity or a semi-conductive material rather than an insulating material. Grounding is necessary to provide a safe discharge route for electrostatic charges.
2. Whenever possible, do not allow semiconductor devices to rub against each other or against other objects. Such friction is a cause of electrostatic generation.
3. Do not approach or touch a charged body (including human bodies). This helps to prevent induction of electrostatic charges from charged bodies to semiconductor devices.
4. Avoid rapid discharges. To prevent rapid discharge, all objects that may come in contact with semiconductor devices shall be made from conductive materials that have a high resistivity value, as in the countermeasures described in item (3)(a). If metal objects are used in contravention of this rule, they shall be grounded through a series resistor with a high resistance value. Rapid electrostatic discharges from semiconductor devices can degrade or damage them.
5. Do not allow the ambient humidity to fall below 40%. Electrostatic charges occur more easily at lower humidity levels, and this tendency increases rapidly when the humidity level drops below 40%. This is because electrical conductivity on the surface of objects decreases at lower humidity levels, making it easier for a charge to accumulate on an object’s surface.

(5) ESD-related Cautions on Handling of Semiconductor Devices

First, it is important to implement the five basic methods (see (4) above) for controlling static electricity in work environments in which semiconductor devices are stored, conveyed, accepted, mounted, or inspected. In addition, customers shall implement other anti-static methods during the design, manufacture, or inspection of sets, such as measuring and monitoring electrostatic discharges and the conditions under which they occur, and then devising appropriate countermeasures.

The following are general anti-static measures that are based on the above-mentioned five basic methods for preventing degradation or damage that can occur in semiconductor devices due to electrostatic discharges when the semiconductor devices are being handled.

1. Storage and conveyance
   1. Use anti-static conductive gloves, conductive plastic containers, conductive magazine cases, conductive racks, etc. when storing or conveying semiconductor devices or PCBs on which such devices have been mounted. When packing, storing, or conveying such devices, avoid using insulating plastic containers that facilitate buildup of electrostatic charges, such as vinyl bags, polyethylene containers, and styrofoam boxes.
   2. To prevent storage containers for semiconductor devices or PCBs on which such devices have been mounted from rattling around (i.e., receiving vibration and friction) inside outer boxes during shipment, use containers that are designed for a tight fit and/or insert padding to prevent shifting of contents. This will help to prevent static electricity that can be generated by friction between semiconductor devices or PCBs and their containers as they are being shipped.
   3. Store electrostatically sensitive devices such as miniaturized LSIs, high-frequency devices, or optical devices on special anti-static storage shelves (shelves that are grounded and have a high resistance value of at least 1 MΩ).
   4. Ground all transport carts and transport vehicles through their wheels or ground them chained together.
   5. Use aluminum foil or a shorting bar to short the connectors of PCBs on which semiconductor devices have been mounted (see Figure 5.12).
   6. Use a conductive sheet to cover PCBs on which semiconductor devices have been mounted or a place a conductive mat in front of such PCBs.

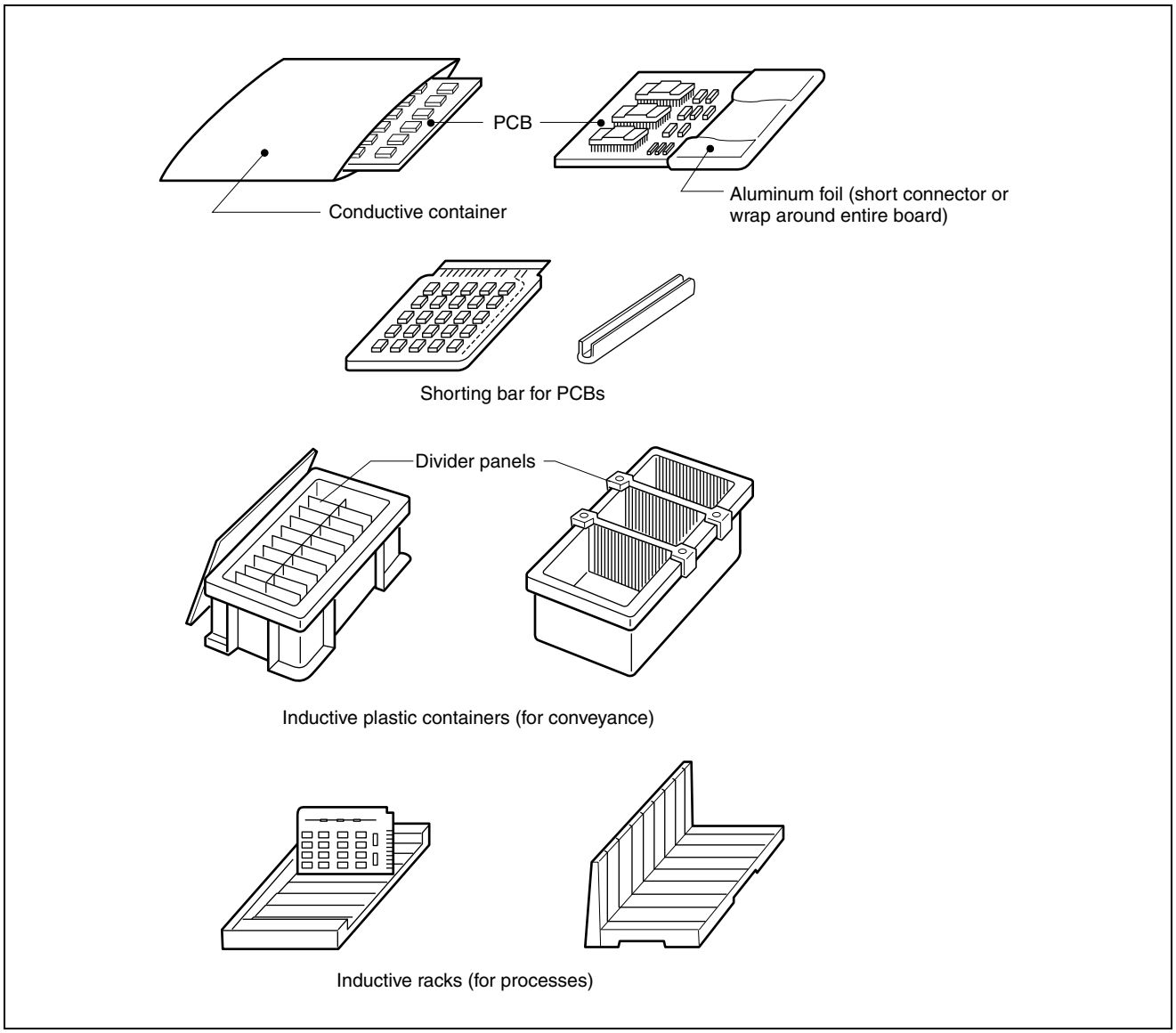
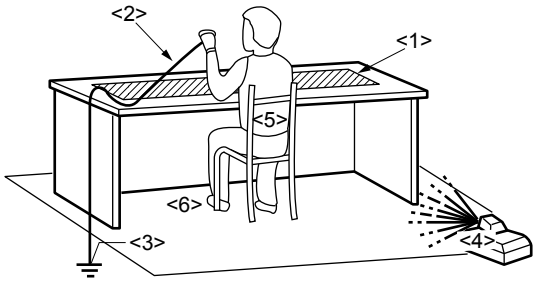


Figure 5.12 Example of Antistatic Protection Methods for PCBs

Example 10 ESD Damage during Storage and Transportation

No. 10	Example	ESD during storage and transportation
Type of device		MOS IC (Plastic encapsulation)
Point		Substances adjacent to semiconductor device shall not be allowed to charge to high voltage.
Summary of example/ phenomenon/ cause		During the end product production process a device which was within specifications before assembly becomes defective after mounting on a PCB. When the PCBs were stacked for transportation or storage, charge in a capacitor facing the IC was discharged and caused destruction of the IC.
Countermeasure/ verification examples		1. Place insulators between the PCBs during transport. 2. Discharge the capacitor. 3. Separate the PCBs keeping some distance between them.

2. Environment, equipment, tools, and jigs
   1. The relative humidity shall be maintained between 45% and 75% if at all possible. Use a humidifier to avoid excessively low humidity conditions when in dry regions (or dry seasons). If a humidifier alone is not sufficient, use an ionizer (ion neutralizer) also.
   2. Minimize air flow. If air flow cannot be eliminated, use an ionizer.
   3. To eliminate sites where static electricity can accumulate, make sure that various devices including measuring equipment, test equipment, conveyers, work table, floors, tools, solder baths, soldering irons are all grounded. Put high-resistance conductive mats (rated between 10^5 Ω/γ and 10^9 Ω/γ) down on work tables and floors and make sure each mat is grounded (see Figure 5.13).
   4. On equipment used to mount or test semiconductor devices on PCBs, all parts of the equipment that may come into contact with semiconductor devices shall be made of conductive material or high-resistivity conductive material and shall be grounded. If insulating materials that are susceptible to static electricity buildup are used (making it difficult for static electricity to be discharged), use of an ionizer-equipped air blower can be an effective countermeasure.
   5. Select jigs and tools that are treated with semi-conductive material that does not easily build up an electrostatic charge and does not rapidly discharge. If a metal jig or tool shall be used, ground the jig or tool via a resistor with a high resistance value.
   6. Use a semiconductor-type soldering iron (low voltage type, 12 V to 24 V) and connect a grounding source to the tip of the iron via a series resistor connection rate at about 1 MΩ (see Figure 5.14).
   7. Do not place any other materials that may generate static electricity in the vicinity.



<1> Conductive desktop mat
<2> Wrist strap
<3> Conductive floor mat
<4> Humidifier
<5> Anti-static work clothes
<6> Inductive shoes

Figure 5.13 Anti-Static Measures for Work Area

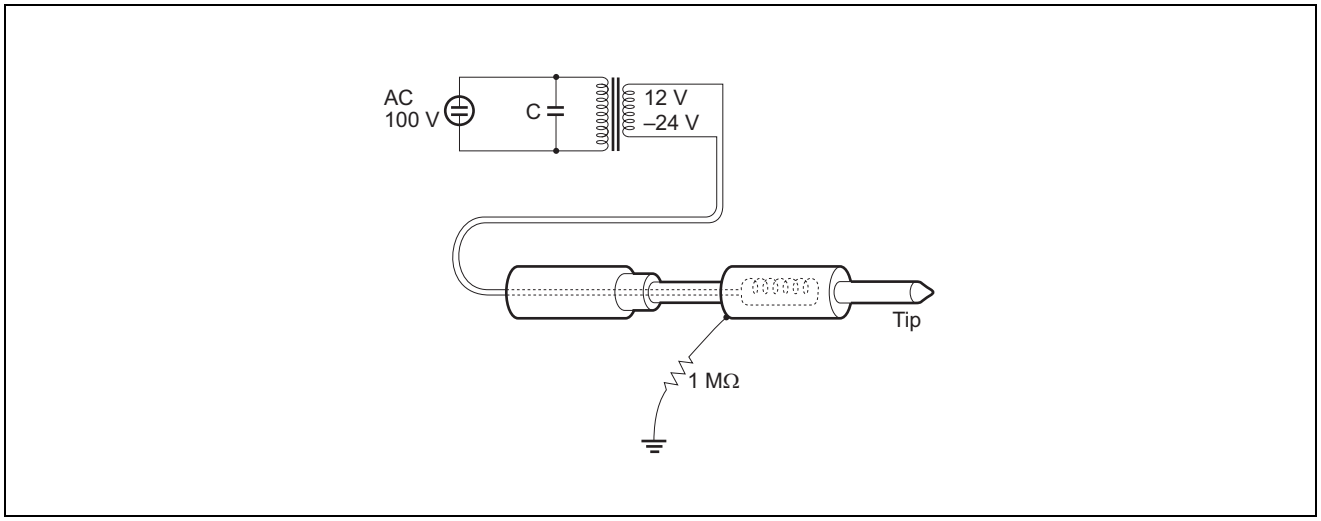


Figure 5.14 Grounding of Soldering Iron

3. Staff
   1. Anyone who is handling semiconductor devices, mounting them on PCBs, or testing or inspecting PCBs on which semiconductor devices have been mounted shall wear anti-static bands such as wrist straps and ankle straps which are grounded via a series resistance connection of about 1 MΩ (see Figure 5.15). Grounding of human bodies is an effective method for preventing electrostatic buildup in human bodies and electrostatic damage to semiconductor devices that such buildup can cause. However, this method is hazardous in that can amplify the effects of any electrical discharge felt by persons wearing anti-static bands. To avoid this hazard, be sure to insert a series of resistors between the body and the grounding source. The amount of resistance shall be determined based on the amount needed as an anti-static measure and the amount needed to protect people from electrical shocks. If a person receives an electrical shock when the resistance value is too low, the person may receive a large current, but too high a resistance value degrades the grounding effect. Therefore, a resistance value of about 1 MΩ is recommended.
   2. Footwear (shoes, sandals, etc.) shall be made of semi-conductive material.

      The resistance value of footwear shall be between 100 kΩ and 100 MΩ. Note, however, that footwear's resistance value varies due to factors such as dirt, friction, and humidity.
   3. Gloves and other work clothes shall be made anti-static semi-conductive materials (resistance: 10^6 Ω to 10^{11} Ω). Avoid using nylon or other easily charged insulating fabric.

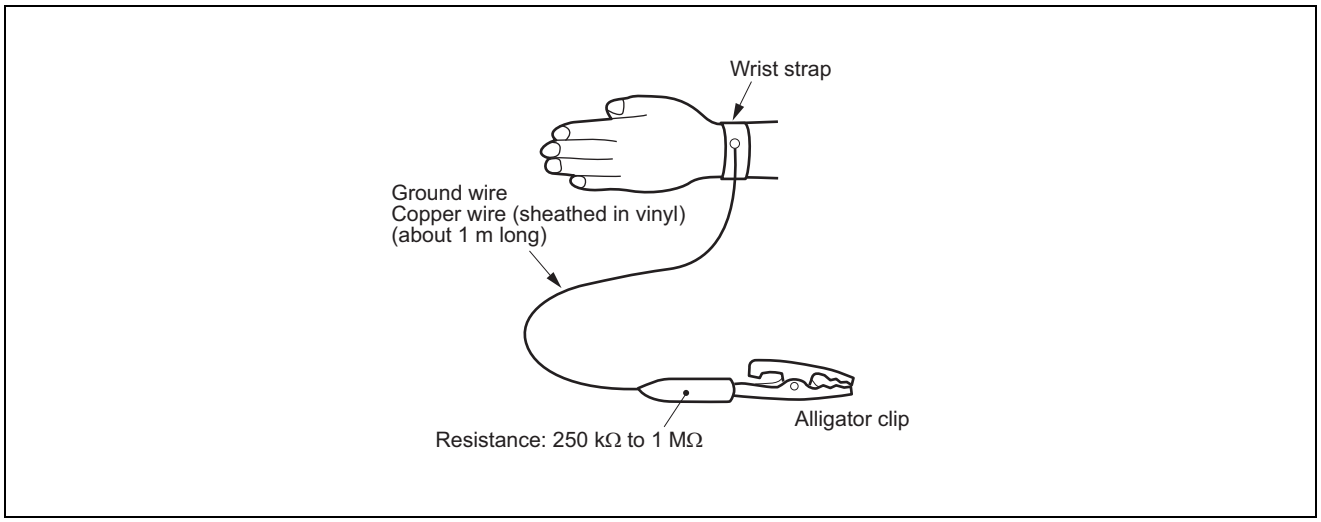


Figure 5.15 Body Grounding

4. Work methods
    1. As for supplies kept in the work area, avoid using easily charged insulating objects (such as objects made of chemical fibers or plastic) and instead use conductive items that have a high resistance value.
    2. The containers used to store or transport semiconductor devices in the work area shall be made of anti-static treated material or semi-conductive material (such as static-shield bag).
    3. At PCB assembly processes, make semiconductor devices the last components to be mounted whenever this is possible.
    4. Train operators to touch a grounded work table before starting an operation, or have them use an ionizer to remove electric charges before starting work.
    5. Do not directly touch semiconductor device leads or PCBs on which semiconductor devices are mounted. Use gloves made of anti-static materials to touch semiconductor devices and PCBs.
    6. When mounting semiconductor devices on PCBs, try to minimize the number of times each device is handled as well as how long it is handled. Working quickly and efficiently is an important way to prevent damage to semiconductor devices and PCBs.
    7. Be sure to shut off the power before attaching a connector to connect a PCB on which semiconductor devices have been mounted. This prevents abnormal voltage from being applied to semiconductor devices, which can damage them.

To make the above anti-static measures more effective, we recommend that electrostatic charges be measured at various places where semiconductor devices are handled.

5.7.2 Excess Voltage Destruction

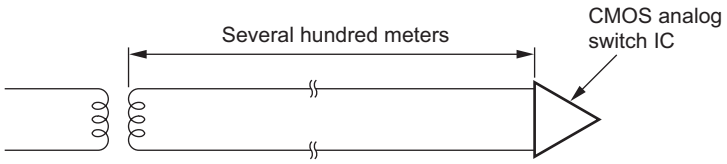
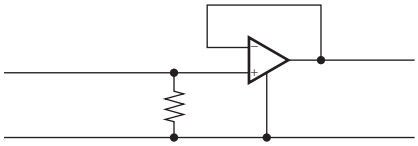
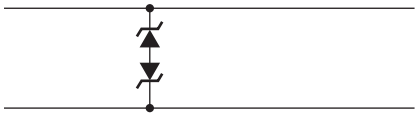
Other than static electricity another cause of destruction is the application of excess voltage, commonly called excess voltage destruction. There are various causes and features of excess voltage generation, but generally the form of destruction is determined by the amount of discharged energy and the size of the energy consuming area. When the temperature of local areas of silicon (Si) exceed 200°C the leakage current is extremely high and permanent destruction results with a further increase in temperature. Physically, when the temperature rises above 500°C, fusion of the Al metallization or damage to the Si substrate occur. The damaged area is obviously related to the amount of surge energy involved in the destruction.

Excess voltage surge includes extraneous surges induced by the activity and the switching on/off of other devices, unexpected lightening, and circuit-induced surges due to the activity of the device itself. Surges also arise during measurement and testing, procedures which are unrelated to the normal activity of devices.

5.7.3 Destruction due to External Surges

External surges are the most troublesome because incidence is generally extremely low, and investigating their causes or conducting simulation tests is difficult. To prevent the problem, it is necessary to record in detail the conditions of operation and the surroundings at the time trouble occurs.

Example 11 Destruction due to Voltage Surge

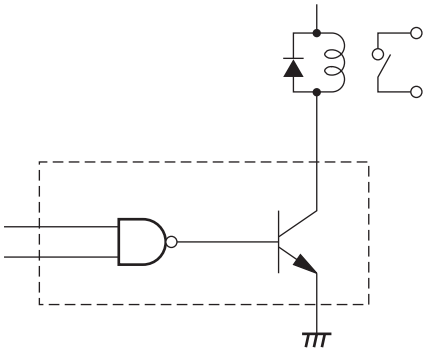
No. 11	Example	Destruction due to voltage surge
Type of device		CMOS analog switch IC
Point		Confirm the IC tolerance to input surge.
Summary of example/ phenomenon/ cause		In a customer's system that collect analog data, as the source of analog signal is far away from the analog/digital converter, an external surge was induced on the connecting line. A CMOS analog switch with an excess voltage protection circuit was used on the analog input, but the surge exceeded the breakdown voltage causing destruction. 
Countermeasure/ verification examples		1. Isolation amplifier added to the input circuit.  2. Zener diode is added to the input circuit to absorb the surge. 

5.7.4 Notes on Destruction of Semiconductor Devices by Overvoltages Generated by the Device Itself

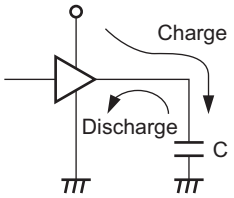
There are also surge currents that generate overvoltages due to the circuit operation of the semiconductor device itself. This is the case when inductive load circuits are driven, such an applied surge is absorbed by the avalanche breakdown of transistors. In such a case, incorporate protective elements. When they are already installed, control the surge voltage and derate the energy to maintain reliability. Also by adding protective elements to the circuit derating, characteristics are checked.

When a capacitor with a large capacitance as the load is driven, excess voltage sometimes arise because of the inductive element of the load circuit.

Example 12 A Driven Inductance Load

No. 12	Example	A driven inductance load
Type of device		TTL IC
Point		Confirm the voltage and current waveform when the load circuit L is switched on and off.
Summary of example/ phenomenon/ cause		When an inductive load such as a relay is driven through a logical circuit, and when the current flowing into the coil in a relay is reversed, the resulting reverse voltage is not absorbed and semiconductor device will suffer electrical destruction. The situation is the same when transistors are used. 
Countermeasure/ verification examples		1. Introduce a clamping diode. 2. Introduce a dumping circuit.

Example 13 Reactance Driven

No. 13	Example	Reactance driven
Type of device		TTL, CMOS IC
Point		Precautions against charging/discharging currents of capacitors
Summary of example/ phenomenon/ cause		If a capacitor is connected to an IC output, a charging current flows as its level changes from low to high, and a discharging current flows as its level changes from high to low. In the former case, a current corresponding to I_{OS} flows. In the latter case, a voltage corresponding V_{OH} is applied to the V_{OL} level output current, causing destruction in the output transistor. 
Countermeasure/ verification examples		1. Use a capacitor with a capacitance that is lower than the value. 2. Insert a resistor in series with the capacitor. 3. Design systems that do not use capacitive load.

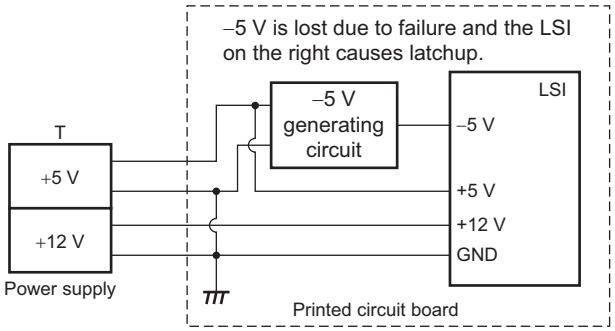
Example 14 Destructive Defects due to Noise from the Power Supply to the LCD Driver

No. 14	Example	Destructive defects due to noise from the power supply to the LCD driver
Type of device		LCD driver, microcontroller
Points		1. Never reverse the voltage of the power supply to the LCD driver. 2. The voltage applied to the CMOS input shall be between the value of the power supply and GND.
Summary of example/ phenomenon/ cause		An LCD driver which was used trouble-free at company A repeatedly failed, for unknown reasons, in product tests at company B. There was a large discrepancy in the ratio of defective units depending on the equipment in which the device was used, even for devices from the same lot. The ratio of defective units also varied with the test pattern. By the failure analysis, the destruction of the power supply section was confirmed. Defect analysis confirmed that cause of destruction was a build-up of spiking noise in the power supply to the liquid crystal display due to a capacitor load, and the reversal of the potential difference across the power supply. A bypass capacitor was placed across the power-supply connection providing a reversed-voltage to synchronize with the noise. The destruction no longer recurred.
Countermeasure/ verification examples		1. In order to avoid, for even a moment, the reversal of the voltage applied to the power supply of a liquid-crystal display driver, use a capacitor with the same phase to eliminate the noise as described above. 2. Widen and shorten the wiring runs of the power-supply pattern, and under the most severe condition for the timing of changes in the column signal, use a high-speed differential probe to check the waveform for the presence of reversed voltages between the power-supply lines.

5.7.5 Latch-Up

In semiconductor devices in which the structures have a parasitic thyristor, such as CMOS circuitry, a failure mode called latch-up often occurs. Latch-up is a phenomenon in which parasitic currents that flow because of an external surge act as a trigger and switch the parasitic thyristor on. This leads to heat-induced destruction. Such parasitic currents don't flow as long as the potential on each signal line of the LSI is within the standard values. However, when the ground potential is floating, and the potential between the input/output signal and the power supply is reversed, the current flows. As the thyristor itself acts as a normal semiconductor element, if the power supply is cut before the structure breaks down because of heat, this does not lead to destruction. Once the thyristor has been turned on, unless the power is cut the problem cannot be resolved, even if the input/output voltage returns to normal.

Example 15 Destruction due to Latch-Up of LSI with Multiple Power Supplies

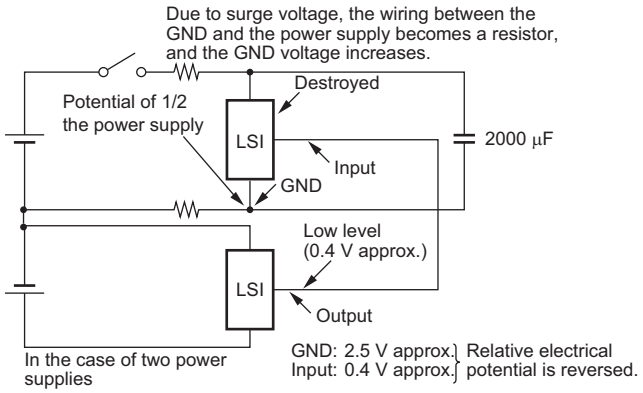
No. 15	Example	Destruction due to latch-up of LSI with multiple power supplies
Type of device		CMOS LSI
Point		If the proper sequence for the application of power is not followed, latch-up will result.
Summary of example/ phenomenon/ cause		After an LSI that had passed the acceptance inspection had been mounted on a printed board, the LSI suffered destruction during examination by an in-circuit tester. Normally, connections are made first and tests are carried out after adjusting the voltage in the –5 V generating circuit. In this case, however, the test was erroneously performed without the connection being made first. Consequently, –5 V was not being supplied to the LSI, latch-up arose, an abnormal current flowed to ground, and the LSI suffered destruction. When using CMOS devices, assume the worst so that even if latch-up does occur, the circuit is made fail-safe in terms of prevention of secondary damage, and protective resistors installed to limit self-generated heat. 
Countermeasure/ verification examples		1. Define the proper sequence for supplying and cutting power with multiple power supplies LSI. 2. Insert protective elements in anticipation of latch-up occurring.

Once latch-up occurs, a large current will continue to flow between the power supply voltage and ground and semiconductor device may be destroyed or burn. To prevent this from occurring, implement measures such as holding the levels of unused input pins fixed (at the supply voltage or ground level) and preventing output shorting. These measures s shall be concerned with the input and output pin voltage levels (i.e., that these levels do not exceed the supply voltage or fall below the ground level), exclusion of abnormal noise, and the timing with which power is applied.

5.7.6 Destruction Induced by Over-Current

Destruction that occurs because of Al metallization meltdown is generically referred to as over-current destruction. Al wiring has a positive temperature characteristic so its resistance is increased by the application of large currents. As a result, more energy is consumed in the wiring causing thermal runaway, the Al wiring exceeds Al-Si eutectic temperature and melts down. Transistors suffer destruction from over-current, and also there are cases of a large current flow and generating over-current destruction. Alternatively, over-current causes the temperature to rise and as a result a eutectic mixture of Al and Si breaks through a junction and transistors are destroyed. It is difficult to determine the cause of the destruction from the resulting condition of semiconductor device.

Example 16 Destruction due to Large-Capacitance Capacitor

No. 16	Example	Destruction due to large-capacitance capacitor
Type of device		CMOS LSI
Point		If the GND does not function properly, the LSI will suffer destruction.
Summary of example/ phenomenon/ cause		During the debugging of programs, program development equipment was destroyed for unknown reasons. Regardless of how many times equipment was repeatedly replaced, several TTL and CMOS devices continued to be destroyed at the same time. It was determined that latch-up occurred because a large-capacitance capacitor (2000 µF) was used and when the power was turned on, the LSI's ground potential rose to half of the power-supply level. 
Countermeasure/ verification examples		Replace the large-capacitance capacitors on printed-circuit boards with smaller-capacitance capacitors.

5.7.7 Handling Unused Pins

If a semiconductor device is used with its unused pins in the open state, the inputs may become unstable and this may cause abnormal operation, such as a rapid increase in the current drawn. Also, if an unused output pin is shorted to power, ground, or another output pin, that may cause the IC to operate incorrectly or be destroyed. Since the handling of unused input and output pins differs between products and pins, follow the pin handling descriptions in the catalog, data sheet, or individual documentation for each product used.

5.7.8 Thermal Runaway

Thermal runaway is a thermal characteristic of any circuits where the positive feedback of power results in the temperature rising without limit until destruction occurs. It is not too much to say that thermal runaway is the most common form of destruction. In addition to those cases where thermal runaway occurs because of local heating of semiconductor device, high-power devices have an additional risk of thermal runaway because of their structurally inadequate thermal dissipation. Caution shall therefore be exercised in terms of heat-radiation (thermal management) design.

5.7.9 SOA Destruction

SOA destruction is a destruction mode that occurs particularly in bipolar semiconductor devices. This is another kind of thermal runaway. In theory, due to the temperature characteristic of the base emitter voltage, when the temperature increases, the voltage V_{BE} falls, and the consumption of energy at the emitter increases locally. Further, as V_{BE} falls, local hot spots occur which lead to destruction.

In the case of a MOS device, since the ON resistance rises with temperature, one characteristic is the tendency to automatically equalize the generation of heat, this then greatly expands the area of possible SOA destruction.

5.7.10 Avalanche Breakdown

This is a failure mode which initiates an avalanche breakdown which in turn causes destruction due to the applied voltage exceeding the junction breakdown voltage of a semiconductor device. When the breakdown energy is small, immediate destruction does not occur. It can be considered that the destruction occurs when the amount of energy passing through the junction exceeds a fixed value. Except in designs where it is specifically intended, using avalanche breakdown is prohibited by maximum rating and other specifications, care is required.

5.8 Protecting Semiconductor Devices from Mechanical Damage

Semiconductor devices are mainly made up of a silicon chip which forms its core to perform its functions, bonding wires to carry electrical signals to and from the chip, lead wires, heat-sink plate to reliably radiate heat away, and mold resin to hold the whole package together mechanically and protect it from external stresses. Since the constituent elements of the device differ considerably in such properties as hardness and thermal expansion coefficient, the mechanical strength margin is less than it would be for semiconductor device consisting of a single material. Consequently, all of the stages in mounting components—bending the lead wires, attachment to an external heat sink, cleaning after mounting to the printed circuit board, correcting the bending—harbor the potential for mechanical breakage.

External mechanical forces can loosen the adhesive bonding of the resin to the leadframe, and cause the subsequent deterioration of the margin for moisture resistance; transmission of the stress to the bonding wires can cause deterioration of resistivity to temperature cycles; and in a severe case wires can be disconnected. In addition, mechanical stresses applied to the heat-sink plate and to the whole package can lead to chip cracks.

In the end product assembly process, caution shall be exercised when mechanical stress is applied, and the process shall be designed so as not to permit defects caused by mechanical stresses. If it appears that destruction will be caused by mechanical stress during the assembly process, it is possible that some damage will be caused not only to the actual defective components but also to components that do not qualify as defective. In this case the product might become defective in the market, so caution is required. In particular, in a type of product which is of hollow structure and bonding wires are not fixed in place, there is danger of breakage caused by ultrasonic cleaning and vibration stress. There is danger that narrow bonding wires will be disconnected by fatigue caused by resonance with ultrasonic waves, and that wire disconnection will be caused by vibration and flow of gel resin.

5.8.1 Lead Forming and Cutting

When semiconductor devices are mounted on a printed circuit board, there are cases in which outer leads are formed and/or cut in advance; if excessive force is applied to a lead during this operation, the semiconductor device can be broken or the seal can be damaged.

For example, if relative stress is applied between the package body and the leads of the semiconductor device, an internal connection could be loosen or a gap could be produced between the package body and the lead, deteriorating airtightness and causing loss of reliability. In the worst case, the mold resin or glass could break. For this reason, the following precautions shall be observed when lead forming or cutting lead wires.

1. When a lead is bent, fix the lead in place between the bending point and the package body so that relative stress will not be applied between the package body and the lead. Do not touch or hold the package body when bending a lead (see Figure 5.16). When a lead forming die is used to perform semiconductor device lead forming, provide a mechanism of holding the outer lead in place and make sure that this outer lead pressing mechanism itself does not apply stress to the device body (see Figure 5.17).

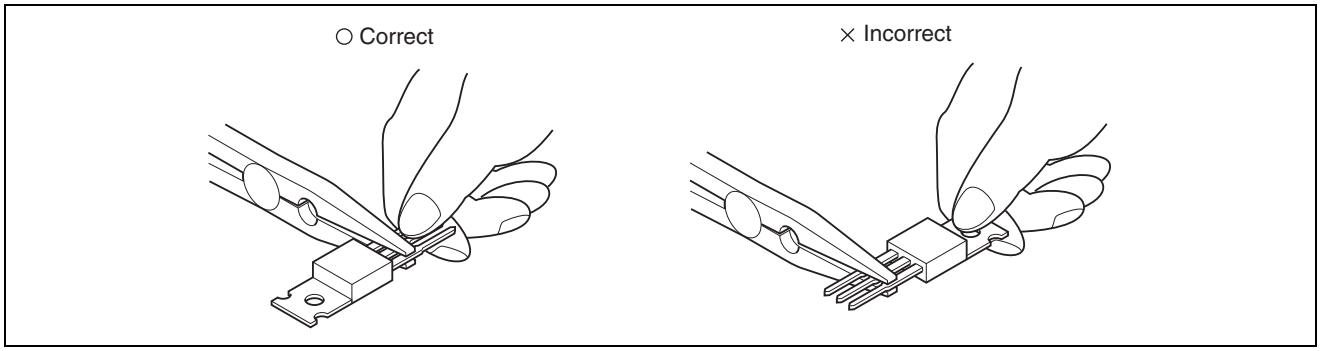


Figure 5.16 How to Bend Package Leads with Handling

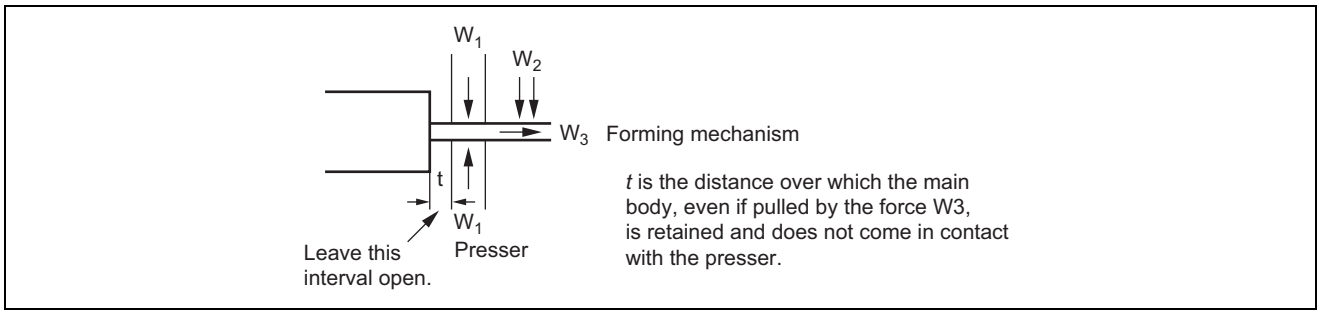


Figure 5.17 Using the Lead Forming Die

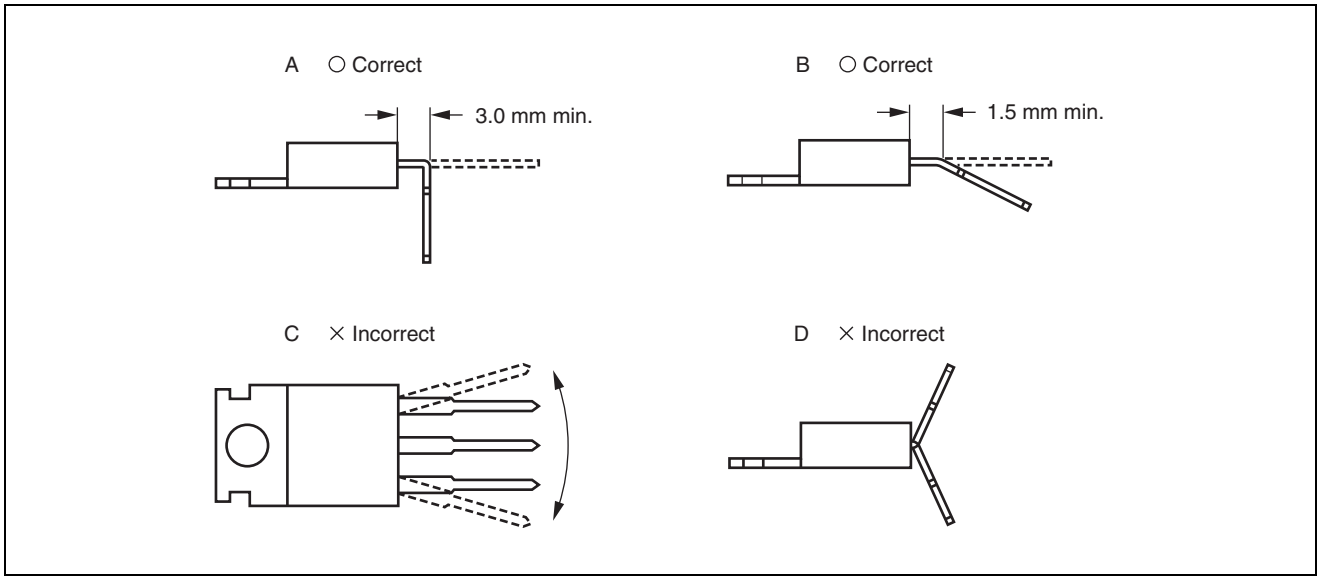


Figure 5.18 Locations and Directions for the Lead Forming of the Outer Lead

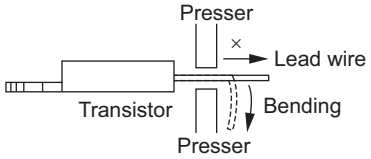
2. When the lead is bent to a right angle, it shall be bent at a location at least 3 mm from the package body. Do not bend the outer lead more than 90 degrees (see Figure 5.18A). When bending the lead less than 90 degrees, bend it at a location at least 1.5 mm from the package body (see Figure 5.18B).
3. Do not bend a lead more than once.
4. Do not bend a lead in the side direction (see Figure 5.18C). Do not bend a lead at the boundary between the mold resin and the lead (see Figure 5.18D).
5. A lead of semiconductor device can be broken by excessive stress (such as tension) in the axial direction, so do not apply more than the prescribed force. The prescribed stress will vary depending on the cross-sectional area of a lead. Depending on the shape of the bending jig or tool, the plated surface of an outer lead can be damaged, so exercise caution.

Transistor and diode products can be supplied with preformed leads on request. If desired, please contact Renesas's sales representative.

Example 17 A Chip Crack Defect that Formed During Lead Formation

No. 17	Example	A chip crack
Type of device		Gate array
Point		When forming a lead on a surface-mounted package, check whether a mechanical shock is being applied to the package body.
Summary of example/ phenomenon/ cause		In a user's process, the leads of a surface-mounted device were corrected before being placed on a circuit board using a lead correction machine. At this time, the clearance between the forming die pressing on the base of the lead and the package body was not left. For this reason, particles entered between the package body and the forming die and applied a stress, as a result of which a chip crack occurred.
Countermeasure/ verification examples		Set the clearance between the package body and the forming die considering the size of specks of particles.

Example 18 Wire Break Caused by a Lead Forming Defect

No. 18	Example	Wire break caused by a lead formation defect
Type of device		Power transistor (Type TO-202)
Point		A lead shall be held securely.
Summary of example/ phenomenon/ cause		When a transistor lead was formed, a lead presser was not used, so a disconnection defect was caused by loosening a pin. Since the pressing was insufficient, excessive tension was applied in the X direction and an internal bonding wire was disconnected when the lead wire was bent. 
Countermeasure/ verification examples		When forming a lead, fix it in place between the main body of a transistor and the point where the lead wire is bent (see figure above).
Reference item		Precautions when bending (section 5.8.1)

5.8.2 Mounting on a Printed Circuit Board

When a semiconductor device is mounted on a printed circuit board, be careful so that excessive stress is not applied to the leads of the device. The following are the principal precautions that need to be taken (see Figure 5.19).

1. The spacing between the semiconductor device mounting holes on the printed circuit board should match the spacing between the semiconductor device leads so that excessive stress is not applied when the semiconductor device is inserted and so that excessive residual stresses do not remain after mounting.
2. When semiconductor device is inserted into a printed circuit board, do not pull on the leads with excessive force from the backside, and prevent excessive stress from being applied between the leads and the case.
3. Leave a suitable space between the semiconductor device and the circuit board. A good way to do this is to use a spacer.
4. After fixing semiconductor device to the printed circuit board, avoid assembling the unit in such a way that stress will be applied between the leads and the device package. For example, when semiconductor device is connected to the heat-sink plate after soldering the leads to the printed circuit board, fluctuations due to tolerances in lead length and printed circuit board dimensions can result in stress being concentrated on the lead. This results in the lead being pulled out, package damage or a lead becoming disconnected. For this situation, solder the lead after semiconductor device is fixed in place.
5. When using automatic insertion equipment, one shall be especially careful so that mechanical shock is not applied to the package body at the time of insertion. This will help prevent cracks from forming in the package or the chip due to shock.
6. When the component is mounted in an IC socket and used under severe environmental conditions, the contact between the IC pins and the IC socket may degrade. One shall avoid using an IC socket as much as possible. Also, when an IC socket is used to mount a multi-pin grid array package device to a circuit board, the package can break or pins may bend when the package is inserted or removed. Therefore it is strongly recommended that a commercially available insertion/removal tool be used.

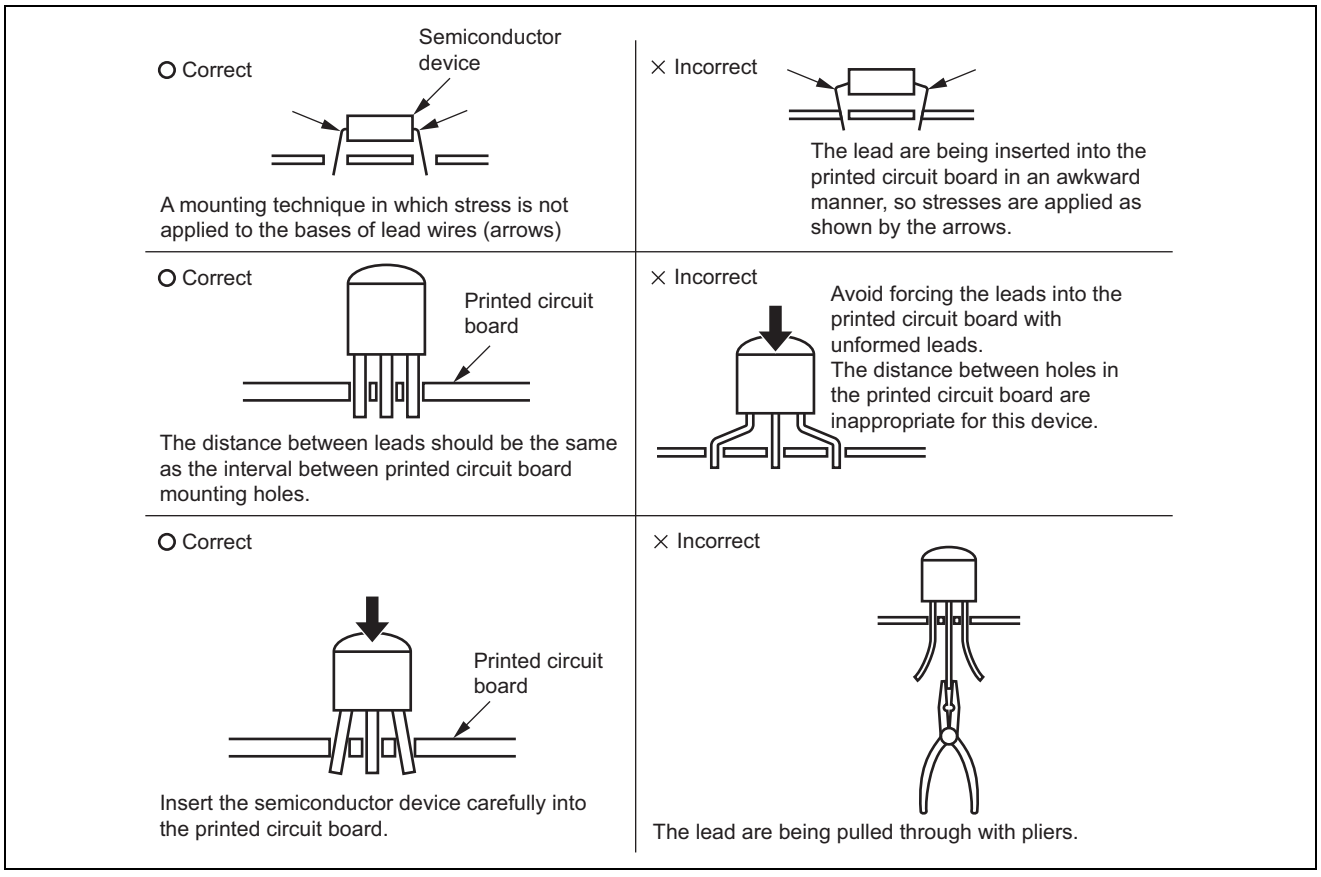
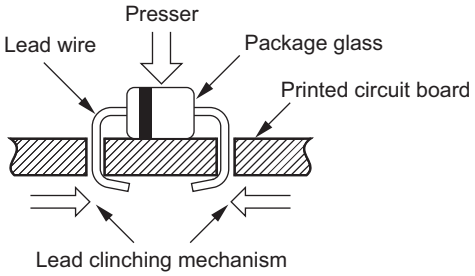


Figure 5.19 Methods of Mounting a Semiconductor Device on a Printed Circuit Board

Example 19 Destruction of a Package by Automatic Insertion

No. 19	Example	Destruction of a package by automatic insertion
Type of device		Silicon diode (DHD type)
Point		Stress shall not be applied to the main body of semiconductor device while a lead is being bent.
Summary of example/ phenomenon/ cause		In automatic insertion of a DHD type diode into a printed circuit board by a high-speed insertion ma chine, the package glass was broken either by excessive pressure on the device main body or by excessive force used to clinch leads on the rear side of the circuit board. 
Countermeasure/ verification examples		1. Adjust the position of the presser. Make the presser material that can provide a buffer against shock. 2. Keep the lead clinching force to a minimum.

Example 20 Solder Defect Caused by Warping of a Printed Circuit Board

No. 20	Example	Solder defect caused by warping of printed circuit board
Type of device		Microcontroller
Point		Be careful in correcting the warp of a circuit board by reflow.
Summary of example/ phenomenon/ cause		A defect involving the peeling off of solder under a surface-mounting reflow stress occurred. No matter how many times a solderability test was performed, no abnormality was detected, and the cause could not be determined. In the course of discussions the subject of warping following reflow was raised; examination of the circuit board involved showed that asymmetry of the copper pattern that positions the components was the cause and that the warping was abnormally large. It was judged that after reflow, while the circuit board was still hot, mechanical stress was applied to correct the warping. Although reflow soldering corresponds to an assembly-phase stress for the mounted semiconductor devices and can be a significant stress, it is also a significant stress for the printed circuit board. If the printed circuit board bends significantly during the heating stage during assembly, larger semiconductor devices may peel off after being attached. Users of semiconductor device must manage the warping of printed circuit boards appropriately.
Countermeasure/ verification examples		1. The circuit board pattern and the component layout are adjusted to prevent warping. 2. The frame material is changed to increase the mechanical strength per pin with respect to the circuit board.

Example 21 Chip Cracking at the Time of Mounting a Component on a Circuit Board

No. 21	Example	Chip cracking at the time of mounting a component on a circuit board
Type of device		Power transistor (DPAK), small-signal transistor (UPAK)
Point		It is necessary to determine if the exterior coating resin affects the stress on the semiconductor device.
Summary of example/ phenomenon/ cause		When an exterior-coating resin was used in mounting a component on a circuit board, the difference in thermal expansion coefficients between the epoxy resin in the semiconductor device and the phenol resin used for the coating caused an excessive stress to be applied to the inside of the element, ultimately leading to formation of a chip crack. Use of such a coating can adversely affect the semiconductor device, depending on the coating material and thickness. Use caution in such cases.
Countermeasure/ verification examples		When using an exterior-coating resin, apply a stress-absorbing resin between the coating resin and the epoxy resin in the semiconductor device.

5.8.3 Flux Cleaning Methods

Flux residue remaining after soldering may affect the components and circuit board wiring reliability, so as a general rule the flux shall be removed. Cleaning methods include ultrasonic cleaning, immersion cleaning, spray cleaning and steam cleaning. These have the following respective characteristics.

(a) Ultrasonic Cleaning

This is a cleaning technique in which ultrasonic vibrations are applied to semiconductor devices while they are immersed in a solvent. While this method is suited for cleaning even the smallest crevices, it can damage the connections between semiconductor devices and the printed circuit board on which they are mounted. Thus care is required when using this method. Avoid using ultrasonic cleaning for semiconductor devices in hermetically sealed packages in which ceramics are the main material used. This is because the internal wiring may resonate at the ultrasonic frequencies used, and this can result in open circuits.

(b) Immersion Cleaning

The semiconductor device is cleaned by immersion in a cleaning fluid. It is necessary for the cleaning fluid to have high purity.

(c) Spray Cleaning

A solvent is sprayed on the product under high pressure. When the clearance between components and the circuit board is small, the cleaning effectiveness can be increased by spraying at an angle.

(d) Steam Cleaning

A vaporized solvent is used for cleaning. This permits cleaning to be done with a solvent that does not contain impurities, so it is often used in the final cleaning step.

Normally a combination of these methods is used. The normal flow of cleaning is shown in Figure 5.20.

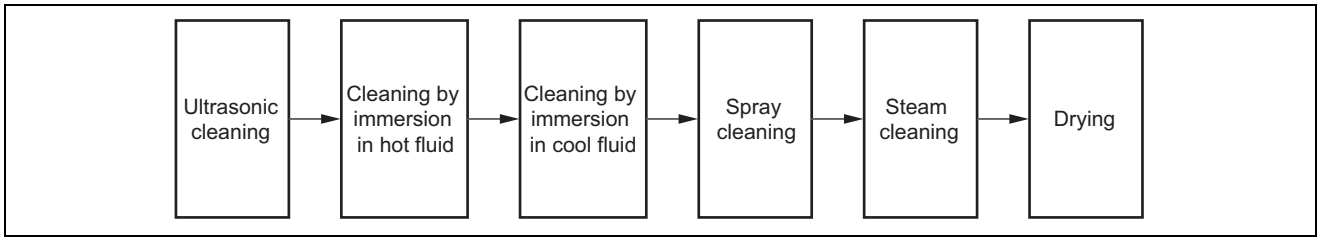


Figure 5.20 Normal Flow of Cleaning

One shall pay attention to the following points when cleaning.

1. To prevent damage to semiconductor device, caution is needed regarding the applied frequency, power (especially the peak power), time, and preventing the semiconductor device from resonating. An example of a set of ultrasonic cleaning conditions is presented below.
   - Frequency: 28 to 29 kHz (the semiconductor device shall not resonate).
   - Ultrasonic output: 15 W/L (one time)
   - Time: 30 seconds or less
   - The semiconductor device and the printed circuit board shall not directly contact the vibration source. In particular, ceramic package type QFNs (LCC) and QFPs (Ceramic) are cavity packages; when subjected to ultrasonic cleaning the connecting wires can resonate under certain conditions and become open or disconnected.
2. When cleaning is continued for a long time, the marking may be erased, so check the conditions that will be used by running an actual test before committing large amount of products.
3. When a solvent is used, public standards for the environment and safety shall be observed.
4. It is recommended that the MIL standards summarized in Table 5.9 be applied for the degree of printed circuit board cleanliness. For details of the MIL standards, see MIL-P-28809A.

Table 5.9 Cleanliness Standards of a Printed Circuit Board

Item	Standard
Residual Amount of Cl	1 μg/cm^2 or less
Electrical Resistance of Extraction Solvent (after extraction)	2 × 10^6 Ω • cm or more

Notes: 1. Circuit board area: Both sides of printed circuit board + mounted components
2. Extraction solvent: Isopropyl alcohol (75vol%) + H_2O (25vol%) (before extraction) (electrical resistance of extraction solvent shall be 6 × 10^6 Ω • cm or more).
3. Extraction method: Clean both surfaces of circuit board (for 1 minute or more) with at least 10 ml/2.54 × 2.54 cm^2 of solvent.
4. Measurement of electrical resistance of extraction solvent: With electrical conductivity meter

Example 22 Destruction by Ultrasonic Cleaning

No. 22	Example	Destruction by ultrasonic cleaning
Type of device		Ceramic package
Point		When cleaning a package with a cavity by ultrasonic, it is necessary to carefully monitor the power.
Summary of example/ phenomenon/ cause		After a ceramic package device was assembled, it was cleaned ultrasonically; the bonding wires resonated with the ultrasonic vibrations. The bonding wires suffered fatigue and become disconnected in a short time.
Countermeasure/ verification examples		Specify a frequency, output and time at which resonance will not occur.

Example 23 Problem that Occurred when a Circuit Board was not Cleaned

No. 23	Example	Problem that occurred when a circuit board was not cleaned
Type of device		Linear IC
Point		Be careful of minute leaks.
Summary of example/ phenomenon/ cause		When components were soldered to a circuit board, flux adhered to the surface of the IC package; subsequently, flux that remained on the surface of the IC package absorbed moisture, the surface leakage current between IC terminals increased, and the circuit board became defective.
Countermeasure/ verification examples		After a circuit board is soldered, the flux shall be cleaned off.

5.8.4 Attachment of the Heat-Sink Plate

In a power device, a heat-sink plate can be used to radiate heat that is produced and thus lower the junction temperature. Attaching an external heat sink to a semiconductor device is an effective way of dissipating heat. To avoid loss of reliability, it is necessary to take the following precautions.

(1) The Selection of Silicone Grease

To improve heat conduction between the semiconductor device and the heat-sink plate and increase the heat-sink effectiveness, silicone grease is uniformly applied in a thin uniform layer to the surface of the semiconductor device that contacts the heat-sink plate. Depending on the semiconductor device, in some cases the device can absorb oil from the silicone grease causing the chip coating material to swell. When selecting a silicone grease, we recommend the use of a grease formulated with an oil base that has low affinity for the package resin so that it will not cause the coating material to swell. Of course, an equivalent product may be used (however it is not necessary when using a metal can package).

(2) Use Suitable Torque When Tightening.

If the applied torque is too low, the thermal resistance will increase, while if it is too high semiconductor device can deform. This can cause chip damage and lead to breakage. Table 5.10 lists tightening torque values for representative packages. For details of tightening torque, contact your Renesas sales represetative before using the tightening torque values.

Table 5.10 Optimum Tightening Torque for Representative Packages

Package	Optimum Tightening Torque	
	[kgf • cm]	[N • m]
TO-3P	6 to 8	0.59 to 0.78
TO-3PFM	4 to 6	0.39 to 0.59
TO-220AB	4 to 6	0.39 to 0.59
TO-220FM	4 to 6	0.39 to 0.59
TO-126	4 to 6	0.39 to 0.59

(3) Give Adequate Consideration to the Flatness of the Heat-sink Plate

When attaching a heat sink to a semiconductor device, if the heat sink is not adequately level, this can interfere with the heat dissipation effect. Furthermore, excessive force applied during attachment can result in degradation in device properties or cracking in the resin package. Consequently, the following precautions shall be observed with the heat-sink plate.

1. For the case of aluminum, copper or iron plates, verify that there are no residual burrs, and certainly chamfer the screw holes.
2. It is necessary to polish the surface that will contact semiconductor device until it is quite flat.
3. Make certain there are no particles such as cutting filings caught in the space between the package surface and the heat-sink plate.
4. Do not solder anything directly to semiconductor device heat radiation plate. If something were soldered directly to the semiconductor device heat radiation plate, a great deal of thermal energy would be applied causing the device junction temperature to greatly exceed the temperature at which operation is guaranteed. This would seriously affect the semiconductor device, shortening its lifetime or even destroying it.
5. Do not apply mechanical stress to the semiconductor device. When tightening, if the tool used (screwdriver, jig, etc.) hits the plastic package directly, not only can cracks be produced in the package but the mechanical stress can be transmitted to the inside, accelerating fatigue of semiconductor device connection section and destroying the device or causing wire damage. One shall always use caution not to apply mechanical stress.

6. Do not attach a heat sink after the semiconductor device has been soldered to the printed circuit board. If a heat sink is attached to a semiconductor device after the device lead lines have been soldered to the printed circuit board, dispersions in lead length and differences in the dimensions of printed circuit boards and heat-sink plates can lead to excessive stress being concentrated in the leads. This can cause lead wires to be pulled out, packages to be destroyed and wires to be disconnected. Consequently, the semiconductor device shall be attached to the heat-sink plate first, and then the outer leads soldered.
7. Do not mechanically process or deform semiconductor device. If the semiconductor device is mechanically processed or deformed, the thermal resistance will be increased and abnormal stress applied to the interior of the semiconductor device, causing failures to occur.
8. When attaching a power device, use the components (spacer, washer, lug terminal, screws, nuts, etc.).
9. The screws that are used to attach semiconductor device to the heat-sink plate can be classified into cap screws and self tapping screws; the following precautions are needed in using these.
   — Use binding-cap screws conforming to the JIS-B1101 standard and screws that have heads equivalent to truss cap screws.
   — Absolutely do not use any flat-head screws since they will apply excessive stress to the semiconductor device (Figure 5.21).
10. When self tapping screws are used, adhere strictly to the tightening torque given above. When using self tapping screws, do not use screws that are larger than the hole diameter in semiconductor device attachment section. These screws tap not only the heat-sink plate but also the semiconductor device attachment holes, which can cause trouble.
11. Heat-sink plate screw hole diameter
   — If the hole is too large: Do not make the heat-sink plate hole diameter or chamfering larger than the head diameter of the screws to be used. In particular, in semiconductor device that uses copper plating as the flange material (TO-220, power IC, etc.), the tightening torque can cause deformation of the copper plating and the plastic package.
   — If the hole is too small: In particular, if a self tapping screw is used, the tightening torque will increase and exceed the recommended tightening torque that was discussed above, or else the desired contact resistance will not be obtained.
12. Other precautions and recommendations in attaching components to the heat-sink plate
   — If two or more semiconductor devices are attached to one heat-sink plate, the thermal resistance for each will increase (see Figure 5.22).
   — The heat-sink plate shall be of suitable size and shape for radiating heat away. In addition, forced air cooling shall be provided as necessary. Measure the product case temperature under actual use conditions, calculate the junction temperature using the published thermal resistance value.

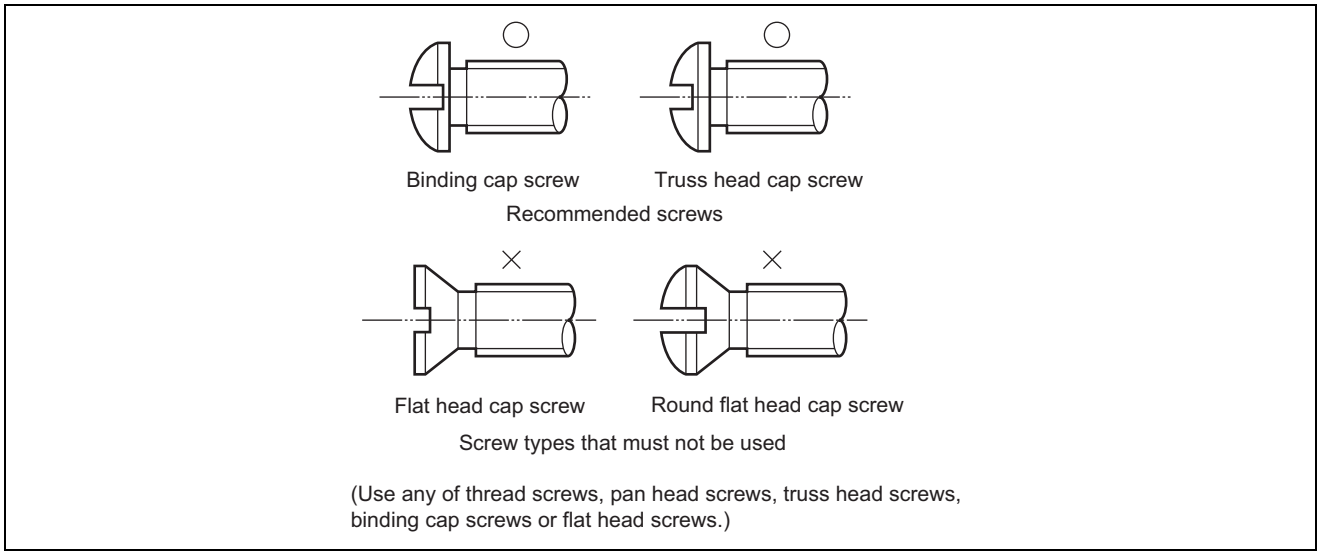
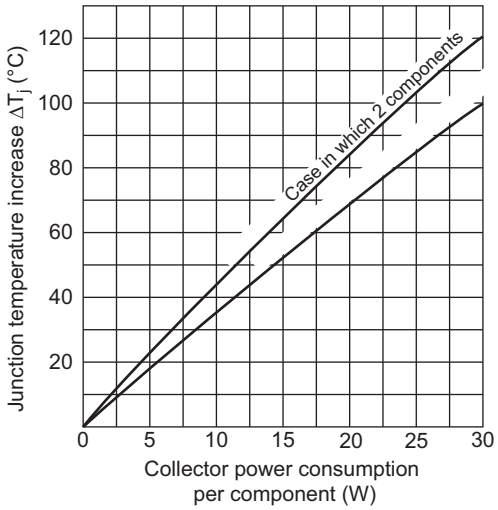


Figure 5.21 Types of Screws to be Recommended and not be Used



Notes: 1. Heat radiating plate 300 × 200 × 1.5 mm aluminum plate
2. Attachment method
a. Position (figure at right)
Unit: mm
b. Tightening torque 9 kg·cm
c. Silicone oil is applied to the contact surface; mylar is not used.
d. Natural convection, horizontal position

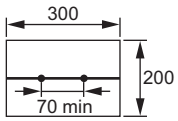


Figure 5.22 A Case in which Two Components are Attached to One Heat-Sink Plate

Example 24 Package Destruction during Mounting

No. 24	Example	Package destruction during heat sink mounting
Type of device		Power transistor (type TO-220)
Point		The torque used to tighten shall be checked.
Summary of example/ phenomenon/ cause		When a power transistor heat sink was attached, the compressed air screwdriver torque rose above 10 kgf • cm (0.98 N • m) and the mounting holes in the heat-sink plate were too large, so the header and the plastic boundary surface peeled off. Depending on the type of compressed air screwdriver, the dispersion in the tightening torque can become large. If the torque rises above 8 kgd • cm (0.78 N • m), the heat-sink plate mounting holes are larger than the screw diameter, or if the heat-sink plate mounting holes are not sufficiently flat, the header can be deformed or separate from the plastic.
Countermeasure/ verification examples		Use a torque within the recommended limits. For the type TO-220 the recommended limits are 4 to 6 kg • cm (0.39 + 0.59 N • m). Keep the flatness of the heat-sink plate mounting holes within 50 µm, make sure that the mounting holes do not open wider than the screw head diameter, and use the accessory metal washers (YZ033S).

5.9 Protecting Semiconductor Devices from Thermal Damage

As it was stated above, because of its construction a semiconductor device is very sensitive to mechanical and thermal stresses. In addition, materials used in construction have different thermal expansion coefficients. These differences have the potential to break the adhesive holding the different substances together. Repeated thermal stress on metals can cause fatigue fractures.

In particular, the recent emphasis on light, thin, short and small surface mounted devices has led to reduced margins for the following points.

- As the temperature rises, the mechanical strength of plastic assembly decreases considerably.
- When the temperature exceeds 100°C, moisture in the resin vaporizes and the vapor fills gaps, causing steam explosions.

One shall carefully check the storage conditions and assembly conditions for each product before using.

5.9.1 Solder Mounting

(1) Notes on Solder Mounting

In general, it is not desirable to expose a semiconductor device to a high temperature for a long time.

Also, when soldering, whether using a soldering iron or by a reflow method, it is necessary to do the processing at as a low temperature and in as a short time as possible to achieve the required attachment. When soldering using a soldering iron, limit soldering times to 10 seconds at 260°C or 3 seconds at 350°C.

An example of temperature increase during soldering, the increase of temperature in the joint section when soldering is done on a low power plastic-package power transistor, is shown in Figure 5.23. After heating in a soldering bath at 260°C for a specified time, the temperature of the joint section was measured. If the soldering temperature is high and/or the time is long, the temperature of the device increases; in some cases this can cause deterioration or breakage.

Note that if the flux used in soldering is strongly acidic or alkaline, the leads may be corroded. Avoid using such fluxes if at all possible (see section 5.8.3).

The soldering iron that is used shall either have three terminals including a ground terminal or the secondary voltage decreased using a transformer so that there is no leakage current at the tip of the iron. If possible, the tip shall always be grounded. In this case, one shall be careful that secondary damage is not caused by the ground (see Figure 5.24). In addition, the soldering shall be done as far as possible from the semiconductor device package.

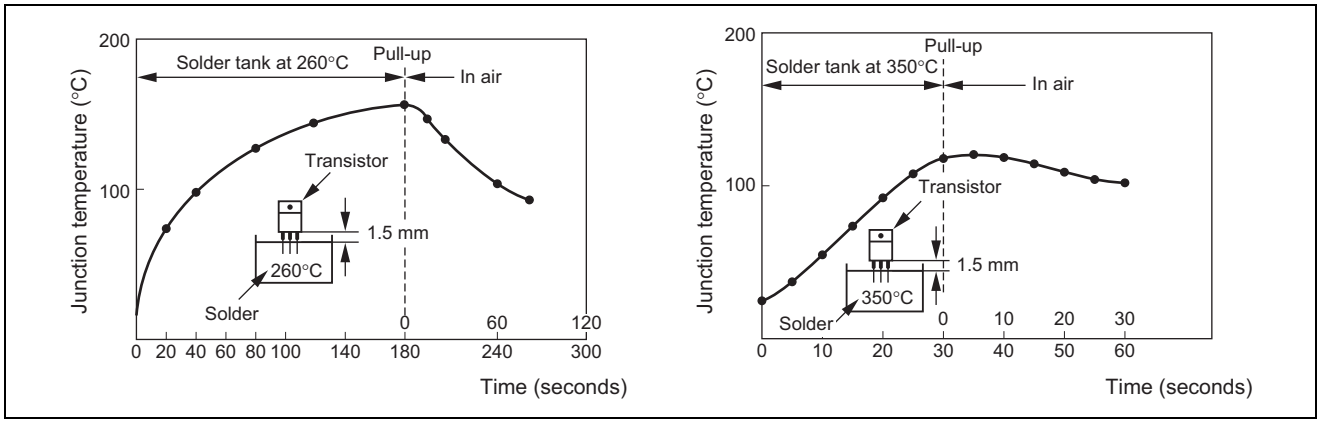
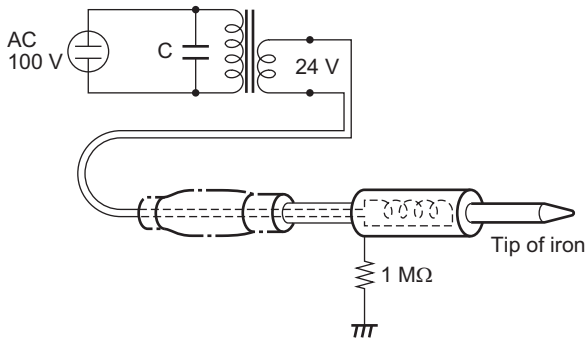


Figure 5.23 Junction Temperature during Soldering



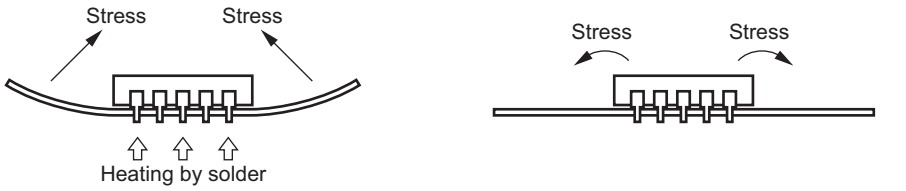
There must not be any leakage current at the tip of the soldering iron and a potential must not be produced. The tip should be grounded as far away as possible.

Figure 5.24 Grounding of the Tip of a Soldering Iron

(2) Soldering a Through Hole Device in Wave Solder Bath

In this method, the soldering is done by immersing the soldering sections of the package leads below the liquid surface in the jet flow solder bath. If the solder arrives at the semiconductor device, the package may break, so be sure that the solder does not come into direct contact with the device package.

In addition, when using a wave solder bath, the bottom surface of the board is heated by the hot solder, and the temperature difference between the top and bottom surfaces can cause the board to warp. If soldering is done while the board is warped, at the time of removal from the solder bath the board will try to return to its original shape, causing excessive stress being applied to the leads and the package. This in turn can cause the solder holding the joint together to crack and/or the leads and the package to break. For this reason, when a wave solder bath is used, the board shall be held in place by brackets so that it will not be warped (see Figure 5.25).



(a) Warping of a board by wave solder heating

(b) Residual stress applied to the package when the board temperature drops

Figure 5.25 Warping of a Board in a Wave Solder Bath

(3) Soldering Surface-Mount Device in a Wave Solder Bath

In this method, the semiconductor devices are first temporarily bonded to the board. The board is then turned over and the semiconductor device exposed to the solder flow. Since in this method, excess solder may remain to form bridges and large thermal stresses are applied directly to the semiconductor device, this method should only be used after carefully considering adequate countermeasures for these problems. Also note that the method is applicable to only a limited number of packages available from Renesas. Before using this method, therefore, you shall consult your Renesas sales representative to find out if it can be used for a particular product.

You shall also be careful when selecting the bonding agent used to temporarily bond samples to the board. If, for example, the bonding performance is not strong enough, semiconductor devices that are being mounted might fall off when the board is turned over. As mentioned in 5.9.1 (1), products may be subject to unexpected stress from warping of the board caused by the heat from the solder jets and semiconductor device might fall off. This is something else you need to consider when you select a temporary bonding agent.

5.9.2 Precautions in Handling a Surface-Mount Device

Here, we explain specific precautions and mounting conditions for surface-mount devices, the use of these has recently been expanding quite rapidly. Since surface mounting devices must be soldered from the side of the board on which the semiconductor devices are mounted, surface mounting is, intrinsically, a structure in which semiconductor devices can easily be subjected to thermal stress during mounting. In particular, if the mounting method involves heating the whole package, the following precautions shall be observed during mounting.

(a) Moisture Absorption in a Package

If the epoxy resin used in a plastic package is stored in a humid location, moisture absorption cannot be avoided. If the amount of moisture absorbed is sufficiently large, it can vaporize suddenly during soldering causing the resin to separate from the leadframe surface. In a particularly severe case, the package may crack (see section 3 for the mechanism). Consequently, it is important to store surface-mount packages in a dry atmosphere.

Moisture-absorption sensitive products shall be stored in moisture-proof packaging. This prevents moisture from being absorbed during transportation and storage. To prevent moisture absorption after opening the moisture-proof packagings shall be stored in the prescribed environment and mounted by reflow soldering within the defined storage time limit.

The semiconductor devices shall be baked before solder mounting in the following cases.

- For products that are packed with a humidity indicator card, if the detection area for the stipulated humidity has changed color to lavender (pink) when the packing is opened.
- The permissible storage time after opening the package has been exceeded while the products are being stored under the conditions stated above.
- The attached label states that it shall be baked. (There are some products attached to an ultra thin package or an extra large chip that need to be baked in any case.)

The magazine, tray, or tape and reel normally used in shipping cannot withstand much temperature, so the package typically cannot be baked as it is packed and received. Transfer the package to a heat resistant container. A tray with the words Heat Proof inscribed on it can be baked as is. However, avoid baking the package while it is inside moisture-proof packaging. Bake gradually, with the tray placed on a flat board, so that the tray will not warp.

(b) Dealing with Moisture Resistivity

Surface-mount products tend to have shorter distance from the outside lead to the inside IC chip than through DIP devices, so in some cases consideration needs to be given to moisture resistivity. For example, in semiconductor devices that are to be used outdoors or in which ability to withstand moisture is particularly important, an appropriate measure such as resin coating is employed. Coating materials include polyurethane and silicon resins. Stresses produced by hardening of the resin, contraction stress and the difference in thermal expansion coefficients between the resin and substrate can cause the element to crack, and the solder joint between the lead and the substrate to crack or disconnect. Therefore the coating material shall be selected and applied carefully.

(c) Precautions for Carrier Tape

In the case of a carrier tape component or IC, electrical charging caused by separation of the cover tape or the carrier tape increases with the speed of the tape separation. To prevent the component from being damaged by static electricity, avoid rapid separation.

(d) Precautions for Mounting

When relative humidity decreases, it becomes easier for objects to become charged with static electricity. Surface-mount products shall be stored in a dry atmosphere to prevent moisture absorption. Since the packages are not subject to friction, they will not become electrostatically charged. During handling in which friction or ESD are possible, and when mounting on a printed circuit board, the relative humidity shall be kept between 45% and 75% if at all possible to minimize the possibility of ESD damage.

5.9.3 Recommended Conditions for Various Methods of Mounting Surface-Mount Devices

The most widely used methods of mounting surface-mount devices are the infrared reflow, the vapor phase reflow and the flow solder methods (wave soldering). These mounting methods all involve heating the entire package. Strong thermal stress is applied to the package. From the point of view of maintaining reliability, it is necessary to monitor the package surface temperature as well as the temperature of the solder joint. Renesas's recommended mounting conditions include the package surface temperature in the case of the reflow method; the solder temperature and immersion time in the case of flow solder.

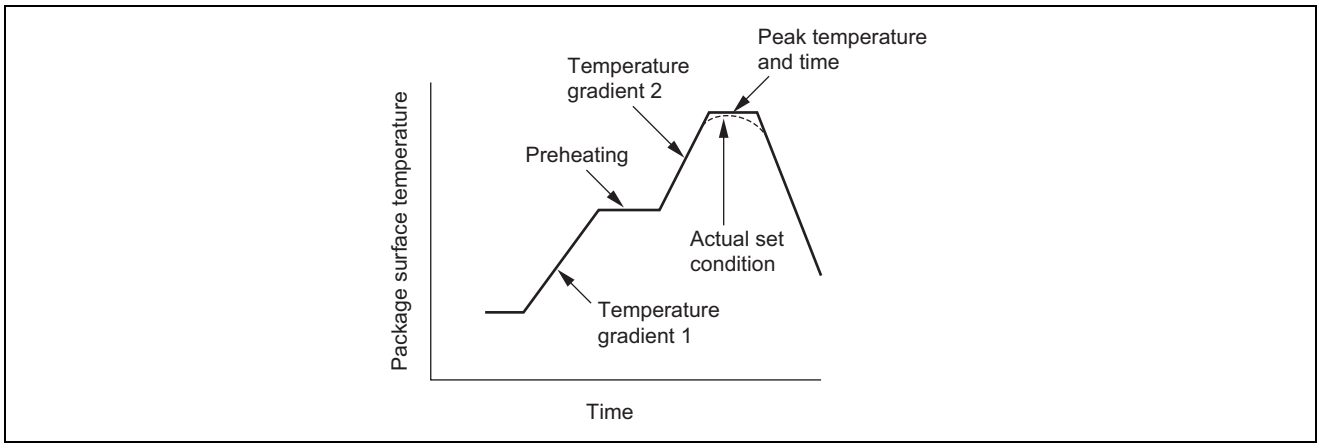


Figure 5.26 Example of Recommended Conditions

We will now present our thinking behind the recommended conditions, with reference to Figure 5.32.

(a) Temperature Gradient 1

When the temperature increases suddenly rapidly, the temperatures of the different parts of a surface-mount device (such as the package surface, interior and rear) become different, so the package warps due to the difference in thermal expansion coefficients among the different materials, in some cases this leads to damaging the chip. Consequently, attention shall be paid to the upper limit of the rate of temperature increase. The lower limit is determined by the operating efficiency of the reflow equipment.

(b) Preheating

The temperatures of the components and the board are kept below the melting point of the solder to stabilize the solder joint and lessen the thermal shock. In general, this is set near the rated temperature of the surface-mount device.

(c) Temperature Gradient 2

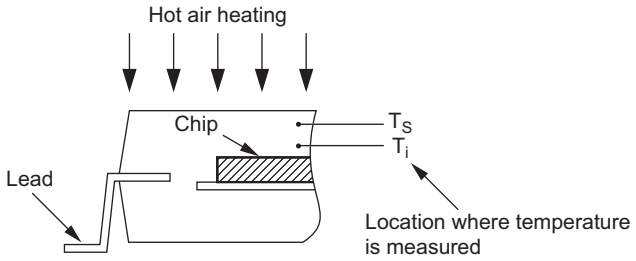
The upper limit of the rate of temperature increase is determined as in (a) above. The lower limit is determined by the need to keep temperature and the time within limits specified in (d).

(d) Peak Temperature and Duration

These are the most important factors requiring attention to keep any damage suffered by the package to a minimum. The peak temperature directly affects the drop in strength of the package (due to the temperature characteristics of the resin) and the water vapor pressure inside the package, so as low a temperature as practical is desired. In addition, since the water vapor pressure increases with time, it is necessary to keep the time as short as possible.

Observe these conditions in determining permissible heating conditions in making of the solder joints, taking into account the characteristics of the board, the components to be mounted, the solder paste, and the reflow equipment.

Example 25 Chip Cracks in a Surface-mount Device

No. 25	Example	Chip cracks in a surface-mount device
Type of device		QFP package
Point		Whether the package surface temperature satisfies the recommended temperature.
Summary of example/ phenomenon/ cause		When a semiconductor surface-mount device (QFP) is mounted on a board by hot air reflow soldering, the transient temperature difference (T_S – T_i = 60°C) that occurs inside the package during the sudden heating applied for reflow soldering causes the package to warp. This then produces a stress that can crack the chip. 
Countermeasure/ verification examples		Change the conditions so that the temperature increase during mounting becomes more gradual.

Example 26 Reflow Mounting Defects

No. 26	Example	Reflow mounting defects
Type of device		Surface-mount package diode and transistor
Point		Poor mounting balance will cause problems such as product displacement and float.
Summary of example/ phenomenon/ cause		If the mounting balance is poor when a surface mounted device (URP, UFP, LLD, DPAK, LFPAK etc.) is mounted using reflow soldering, mounting problems can occur such as the package becoming displaced or not fixed on the surface. Care is particularly required when lead-free materials or processes are being handled. 1. The land pattern does not have left-right symmetry. 2. The amount of solder cream applied is not uniform. 3. The soldered parts are not all heated at the same time. If some parts are in the shadow of neighboring components, the left-right temperature difference of the soldered section can become large. 4. The ratio of flux contained fluctuates.
Countermeasure/ verification examples		Check for the problems listed above.
Reference item		Diode Package Data Book and Surface Mount Package User's Manual

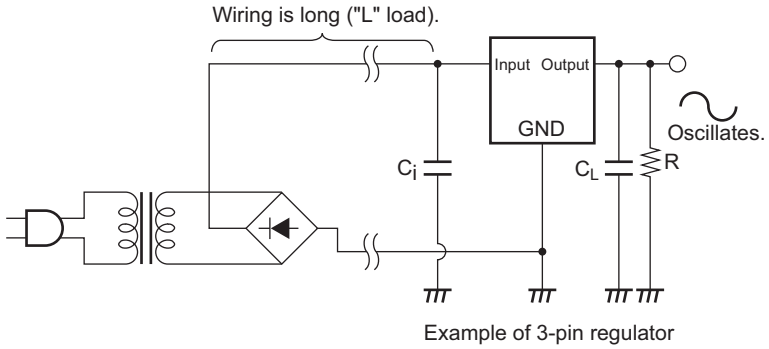
5.10 Protecting Semiconductor Devices from Malfunctions

There are several types of semiconductor malfunction. The semiconductor itself can become damaged or degraded, making normal operation permanently impossible. In other cases, even though a semiconductor has a slight defect, it will operate normally until a change in the conditions of use and/or environmental conditions causes the latent defect to become critical. In this section we explain mainly the latter case.

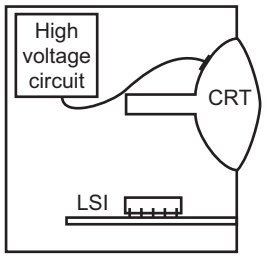
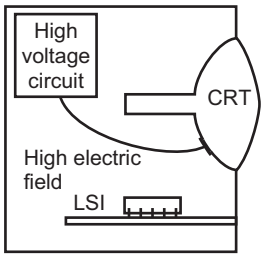
5.10.1 Precautions for Board Mounting

Semiconductor devices are not used alone; they are mounted and used on various boards such as printed-circuit boards, on which other devices are also mounted. Therefore, semiconductor devices share a power-supply line with other devices and are subject to influence by extraneous signals used for the circuits located near the semiconductor devices. Special consideration is thus necessary regarding positioning of the signal lines that are likely to be affected by subtle signal waveforms.

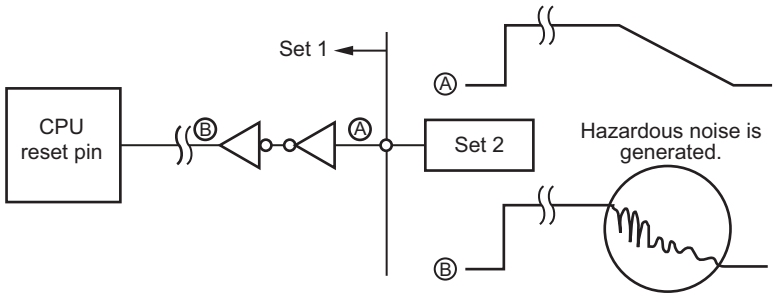
Example 27 Linear IC Oscillation

No. 27	Example	Linear IC oscillation
Type of device		Linear IC
Point		Oscillation shall be checked.
Summary of example/ phenomenon/ cause		If a long line is connected to an input pin of a linear IC, equivalent inductive (L) load is generated on the input pin, causing oscillation. If a small signal line runs parallel to a large-current output line, mutual induction is generated, also causing oscillation of the output waveform.  Example of 3-pin regulator
Countermeasure/ verification examples		1. Make input lines as short as possible to reduce inductive (L) load on the input. 2. If input lines are inevitably long, monitor the waveform on the input pins while varying the capacitance of input capacitor C_i and output capacitive load C_L. 3. Separate large-current lines from small signal lines. 4. In a printed-circuit board, insert a GND pattern between the signal line patterns.

Example 28 Malfunction due to Design Changes of Terminal Equipment

No. 28	Example	Malfunction due to design modification of terminal equipment
Type of device		MOS LSI
Point		LSIs shall not be operated under high voltage.
Summary of example/ phenomenon/ cause		After the design of CRT display equipment had been changed, a non-repeatable runaway failure occurred abruptly. It recovered from the failure after temporarily being left turned off. By reviewing the changes, it was found that the cause was a shift in a threshold voltage due to a high electric field (anode voltage was 20 kV).  Before design modification (operates correctly.)  After design modification (mulfunction occurred.)
Countermeasure/ verification examples		1. Modify the CRT connection manner to prevent high electric field application. 2. Shield the LSI from electric charge.

Example 29 Reset Malfunction due to Hazardous Noise

No. 29	Example	Reset malfunction due to hazardous noise
Type of device		IC, LSI
Point		Anti-noise measures shall be taken for mechanical switches.
Summary of example/ phenomenon/ cause		With set 1 connected to set 2, when the reset switch of the application circuit was pressed, the application circuit was not reset, and instead malfunctioned. Specifically, the reset signal of set 2 fell so slowly that hazardous noise was generated in the reset-input circuit in set 1, thus disabling correct reset function. 
Countermeasure/ verification examples		Modify set 1 to prevent generation of hazardous noise.

Example 30 Oscillation Circuit and Patterns on a Board

No. 30	Example	Oscillation circuit and patterns on a board
Type of device		Microcontroller
Point		Oscillation-start time shall be constant.
Summary of example/ phenomenon/ cause		An intermittent failure occurred in microcontrollers. The failure-occurrence ratio depended on the product model despite the fact that the products were assembled by the same manufacturer. By analyzing the oscillation waveforms of the products presenting the high failure-occurrence ratio, it was found that it sometimes took so long for oscillation to start that the reset signal was cancelled before oscillation became stabilized, thus causing malfunction. It was also found that the difference in the failure-occurrence ratio between product models was caused by the difference in oscillation circuit patterns. That is, the products presenting the high malfunction ratio had no shield for the input pattern of the oscillation pin, and a high-speed signal line crossed the pattern. This signal line generated cross-talk, thus preventing stable oscillation.
Countermeasure/ verification examples		1. Oscillation circuit patterns were modified to the standard patterns recommended by the supplier. 2. Eliminating distortion of oscillation waveforms was confirmed by monitoring the waveforms. 3. Series resistors were inserted into the input to stabilize the oscillation circuit. Adequate margin was then confirmed.

5.10.2 Precautions against Malfunction due to Noise

Accompanying the increased speed of semiconductor device operations, the devices now generate more noise and have become more sensitive to noise that leads to malfunction. Extraneous noise, for example, was eliminated by conventional low-speed devices acting as noise filters, thus preventing malfunction of the subsequent devices, whereas the same noise is amplified by recent high-speed devices, thus sometimes increasing the incidence of malfunction.

Currently, CMOS devices capable of high-speed operation while at low power, have significantly higher signal impedance and higher noise sensitivity. Furthermore, as CMOS circuits are inevitably accompanied by large current changes synchronized with clock pulses on the power supply line, this large current change coupled with print circuit patterns, may generate a lot of noise. Specifically, sine-wave signals generate relevant frequency noise only, whereas square-wave signals generate various harmonics as noise.

Particular components of harmonic waves can be determined by performing Fourier analysis on the square waves.

When the original oscillation frequency is f_0 and a frequency that depends on the rise/fall gradient of waveforms is f_1, harmonic noise spectrum is attenuated at a rate of –10 dB/decade within the frequency domain between f_0–f_1 and –20 dB/decade above f_1. If harmonic signal waveforms are further superposed on square waveforms, still more noise in the form of harmonics will be generated.

Example 31 Malfunction due to Cross-Talk Noise from NC Pins

No. 31	Example	Malfunction due to cross-talk noise from NC pins
Type of device		IC, LSI
Point		NC pins adjacent to noise-sensitive pins shall be appropriately handled.
Summary of example/ phenomenon/ cause		The user's system malfunctioned in noise-tolerance testing during development. The noise level was found to be high and several anti-noise measures were tried. Grounding the NC pin was shown to be effective. After investigation, it was found that the open NC pin was near the high-frequency signal pattern on the printed circuit board, and the resulting cross-talk noise was input to the adjacent pin through the stray capacitance, thus causing malfunction.
Countermeasure/ verification examples		1. NC pins shall be grounded with an appropriate value of impedance, or connected to the power supply. 2. NC pins shall be handled carefully because they may serve as internal test pins.

Example 32 Noise Generation

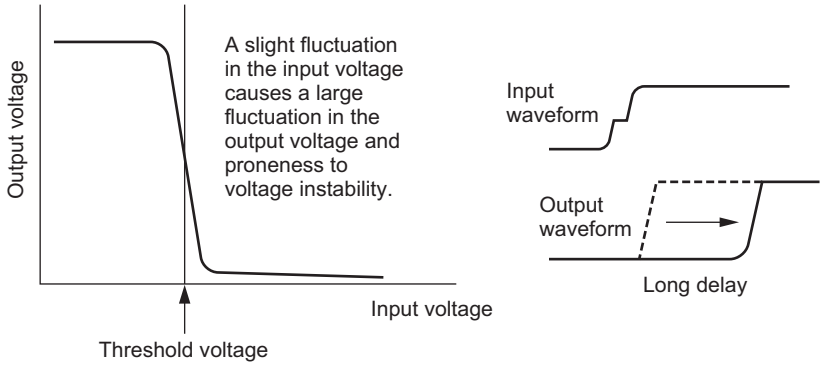
No. 32	Example	Noise generation (electrical)
Type of device		Microcontroller
Point		The capacitance and layout of the bypass capacitor shall be appropriate. The clock waveforms shall be appropriately shaped.
Summary of example/ phenomenon/ cause		Noise generated by digital circuits such as microcontrollers may cause malfunction of peripheral devices. The noise depends on various factors such as the clock waveforms and power supply current waveforms of the LSI, and the positioning of the bypass capacitor and routing of both the power and the GND lines on the printed circuit board.
Countermeasure/ verification examples		An LSI generates only a small electric waveform by itself. Power-supply-related electric waveforms can be eliminated using a bypass capacitor effectively to suppress the power supply current loop, and clock-related electric waveforms can be eliminated by shaping the rising and falling waveforms. In other words, monitoring the clock waveforms and power-supply waveforms of the LSI mounted on the board using a spectrum analyzer provides the means of preventing noise generation. 1. Shape the rising and falling waveforms of the clock (t_r,t_f) and reduce the speed to accelerate attenuation of the harmonic waveforms. The harmonic waveforms will be attenuated at a rate of -10 dB/decade within the frequency range between the original oscillation frequency and t_r (f_f) and at -20 dB/decade above this. 2. Absorb harmonic spectrum component using the bypass capacitor. Selecting an appropriate capacitor that has excellent frequency characteristics and is capable of absorbing the harmonic spectrum component is important, and appropriate positioning of the bypass capacitor, which determines magnitude of the power supply loop, is also important.

5.10.3 Precautions on Signal Waveforms

Due to the increasing speeds of electronic systems, noise and distorted waveforms, which did not cause problems previously, have become likely to affect basic LSI operations. It becomes increasingly difficult to test the stability of the semiconductor device operations. This is because not only finding the conditions that most affect the operations is extremely difficult but also finding the combination of good samples and samples that adversely affects the operations in an evaluation and testing phase is also very difficult.

The best approach to effectively find and solve these issues is analyzing waveforms in detail. Recently, advanced waveform monitors incorporating glitch-detection function are available, and abnormal waveforms that were previously difficult to find can be quickly found today. However, even when abnormal waveforms are found, it is often difficult to determine how much the abnormal waveforms can affect the LSI. In such cases, please direct inquiries to Renesas's technical marketing department.

Example 33 Malfunction due to Distorted Input Waveforms

No. 33	Example	Malfunction due to distorted input waveforms
Type of device		IC, LSI
Point		Distortion of signals shall be monitored.
Summary of example/ phenomenon/ cause		When operating an IC, depending on the input waveform, distortion near the threshold voltage may cause unstable IC operation leading to malfunction. A certain logic product exhibited a significant propagation delay of the input waveform shown below. Specifically, the input waveform was distorted near the threshold voltage, which changed the input level and disturbed multi-gate operation, thus causing the delay. 
Countermeasure/ verification examples		Add a buffer gate and shape the waveform to eliminate distorted input waveforms.

Example 34 DRAM Malfunction due to Noise in Address Signals

No. 34	Example	DRAM malfunction due to noise in address signals
Type of device		DRAM
Point		Signal waveform of DRAM shall be appropriate.
Summary of example/ phenomenon/ cause		DRAM internal circuits are designed to be triggered when the voltage level of the address signals becomes stable. If a large noise above the specifications is applied to these signals, access time starts at the time of noise generation, thus causing malfunction. Particularly, special care for the waveforms of these signals shall be taken because they change depending on the retained data, and the word line selected immediately before.
Countermeasure/ verification examples		1. Find a large noise in the waveforms of various signals using the glitch-detection function and determine the worst pattern based on the characteristics. 2. Shape the waveform by improving the impedance matching with the driver, power-supply patterns, positioning of bypass capacitors.

In some cases, the operational margin for a circuit can be confirmed by analyzing signal waveforms in detail. For analog circuits such as oscillation circuits and PLL circuits in particular, waveform monitoring is one of the most effective means. If the phase difference between input and output signals, amplitude, distortion, noise level, and other factors are strictly measured and the waveforms are shaped to what it shall be, malfunction frequency can be reduced and the reliability can be improved greatly.

Example 35 Evaluation of Oscillation Circuit Stability

No. 35	Example	Evaluation of oscillation circuit stability
Type of device		Microcontroller
Point		Stability of oscillation circuits shall be carefully confirmed.
Summary of example/ phenomenon/ cause		Oscillation circuits are very difficult to handle and often cause intermittent failures. This is particularly because they depend on the compatibility between the LSI and the oscillator, the pattern routing on the printed circuit board, and the combination of external capacitors, resistors, and other elements. Therefore, the stability of oscillation circuits shall be carefully confirmed regarding temperature, power supply rising waveform, oscillation stabilization time, phase difference between input and output, and input/output waveforms.
Countermeasure/ verification examples		1. Confirm the temperature characteristics of the oscillation circuit because the circuit gain may vary depending on the temperature. 2. Test the system while varying the power supply power-on sequence waveform. Does the circuit operate correctly when the power supply level rises extremely slowly and extremely smoothly? 3. Create the distribution of oscillation stabilization time and infer the probability that oscillation will be stabilized after reset cancellation. 4. Find the limit for stability of oscillation start up by inserting series resistors in the feedback circuit. 5. If oscillation is not obtained, check for distortion in the input/output waveforms. 6. Oscillation stability can be predicted from the phase difference between input and output waveforms.

5.11 Measurement-Related Cautions

5.11.1 Cautions on Use of LSI Testers

The caution points concern the use of LSI testers for LSI acceptance inspections.

(1) Sequence of Voltage Application to Power Supply Pins and Input Pins

Voltage shall always be applied to LSIs via power supply pins. When voltage is applied via input pins prior to applying voltage via power supply pins, current will flow via the pins' protection circuits, causing latch-up.

Figure 5.27 shows the structure of a CMOS input protection circuit. When a voltage is applied to input pin I1 before it is applied to the power supply pin VDD, a forward bias occurs between the drain (P-type diffusion layer) and the well (N-type diffusion layer) for P-channel transistor T1, which triggers latch-up.

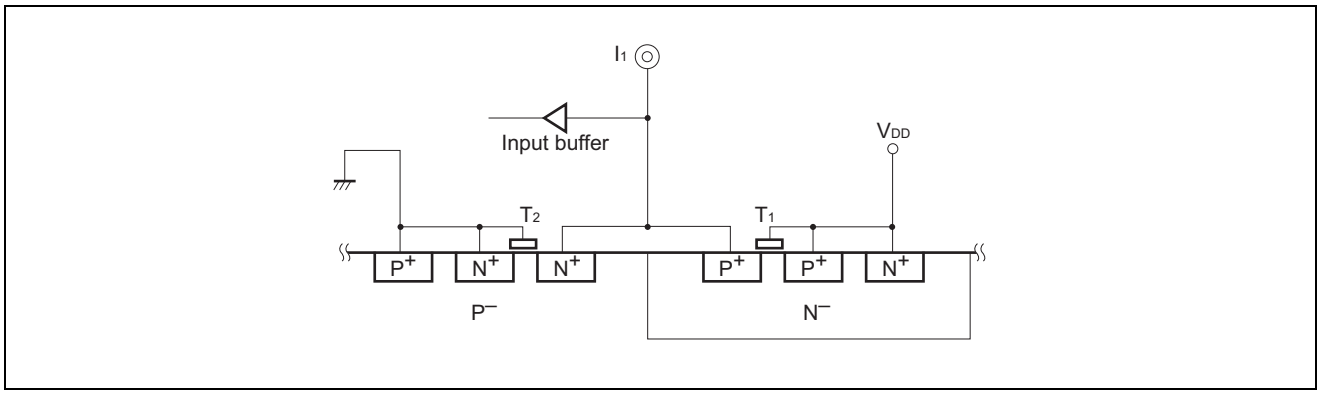


Figure 5.27 Structure of CMOS Input Protection Circuit

(2) I/O Switching

When in input mode, a voltage is applied from the LSI tester. When in output mode, the tester measures the LSI's output voltage. However, if the I/O switching timing between the LSI and the LSI tester is skewed, even though the LSI is outputting a voltage, the tester may also apply a voltage resulting in the flow of a large current. This may destroy the LSI (see Figure 5.28). In particular, the address output and the instruction code or data input is repeated on the address/data bus, which means that caution is needed to ensure correct timing in I/O switching. Check the individual data sheet for each semiconductor device since the I/O timing varies among different semiconductor devices.

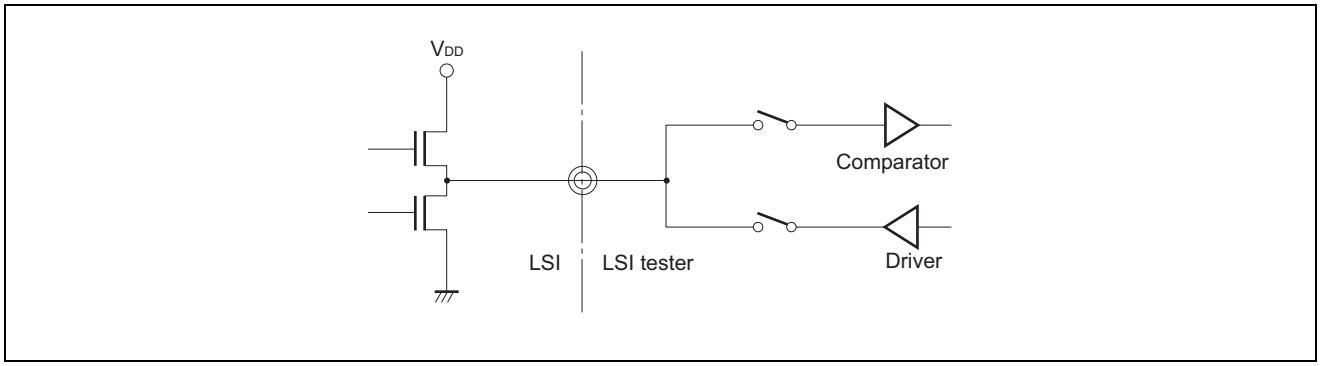


Figure 5.28 I/O Switching Modes

(3) When Using Several Power Supply Sources

LSIs that have an on-chip A/D converter or analog comparator may include several power supply pins in addition to the main power supply pin (V_{DD}), such as an analog power supply pin (AV_{DD}) or a reference voltage pin (V_{REF}) (see Figure 5.29).

In such cases, if the AV_{DD} or V_{REF} voltage is several volts greater than the V_{DD} voltage, latch-up may be triggered by a large current entering the protection circuits. The protection circuits for AV_{DD} and V_{REF} pins are similar to the protection circuits for input pins that were described in (1) above. Caution is required when changing the power supply voltage during testing.

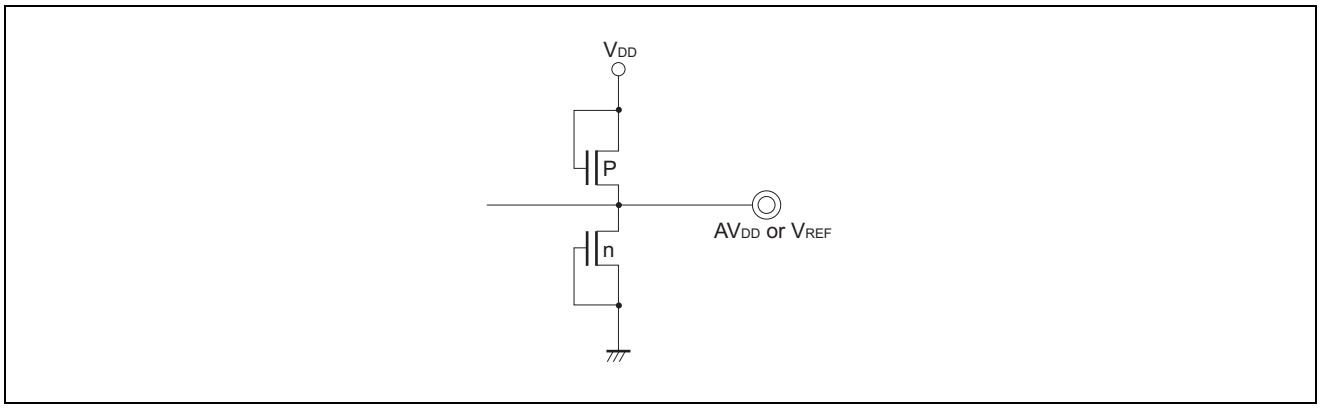


Figure 5.29 Example of Multiple Power Supply Sources

Example 36 Destruction due to Mistiming of Power Input

No. 36	Example	Destruction due to mistiming of power input
Type of device		Linear IC
Point		Confirm whether the power input sequence is the same as the specifications.
Summary of example/ phenomenon/ cause		When switching the mode, a malfunction of unknown cause occurred. The IC that malfunctioned operates on two power supplies. Only power supply 1 is used in normal operation, while power supply 2 is designed to turn on and function when switching the mode. The relevant IC was designed in such a way that unless the output signal is muted (Mute) until power supply 2 rises to the high level (5 V), pulse noise occurs and excessive current flows. It was confirmed that these precautions for use had not been followed, and as a consequence the noise surrounding the power supplies caused the semiconductor device to malfunction.
Countermeasure/ verification examples		Confirm and follow the precautions for use given in the catalog or specifications provided with the delivery documents. In the case that multiple power supplies are used, be especially sure to control the timing of each on/off event.

(4) Overshoot, Undershoot, and Spike Noise

(a) Power Supply Voltage Overshoot

When an overshoot occurs in the power supply voltage supplied from the LSI tester, an overvoltage is applied to the LSI, which may damage the LSI.

(b) Overshoot and Undershoot of Signal Voltage

When an overshoot or undershoot occurs in the signal voltage applied to input pins, a current flows across the LSI's on-chip protection circuits, causing latch-up. An overshoot causes a current to flow from the P-channel transistor T1's drain to the power supply pin VDD and an undershoot causes a current to flow from the N-channel transistor T2's drain to the GND pin (see Figure 5.27 above).

(c) Spike Noise

If spike noise occurs in the power supply voltage and signal voltage applied by the LSI tester, the LSI may be destroyed depending on the peak voltage. Note that even if the LSI is not destroyed, it may still be damaged or its reliability may be degraded.

Since overshoot, undershoot, and spike noise have a powerful effect on the reliability of LSIs, it is important to check the voltage waveform to ensure that overshoot, undershoot, and spike noise do not occur. When using an LSI tester, it is very important to properly maintain and carefully program it.

(d) Protection Against Voltage and Current Surges

Take care to ensure that surging voltages are not applied from testers during characteristic measurement, or use such countermeasures as adding clamping circuitry to the tester, or ensure that abnormal voltages are not applied due to faulty connections during current driving measurement.

When capacitors are installed to prevent noise on input/output terminals and are connected carelessly, there is a chance that semiconductor devices will suffer electrical destruction because of peak currents that result from charging and discharging of the capacitor. For example, during intermediate inspections using board testers or in-circuit testers if the capacitor remains charged when the next board is tested, destruction of semiconductor devices may result. In cases where the capacitors on a board remain charged after a test, there is also a possibility of discharge later in the storage case, so all capacitors in the tester and on the board shall be completely discharged. In the same manner, when a bypass capacitor with a large capacitance is inserted on the tester power supply, care shall be taken to ensure that an unnecessary charge does not remain after the power supply is disconnected.

Example 37 ESD Damage during Measurement

No. 37	Example	ESD damage during measurement
Type of device		MOS IC (plastic encapsulation)
Point		Measure the amount of charge after exposure to friction and take countermeasures
Summary of example/ phenomenon/ cause		Because a plastic guide rail was used to feed the IC to an automatic measuring IC, the IC's plastic materials became charged with static electricity as the IC slid along the guide rail. This charge was discharged at the measuring head (metal), and caused destruction of the IC's input circuit. This occurred not at high humidity, but at low humidity.
Countermeasure/ verification examples		1. Replace the plastic guide rail with a metal one, to avoid the generation of electrostatic charge. 2. GND the guide rail. 3. If these measures do not sufficiently reduce the amount of charge, use an ionizing blower as well.

Example 38 Destruction during Measurement

No. 38	Example	Destruction during measurement
Type of device		TTL IC
Point		Beware of voltage surges when power is applied.
Summary of example/ phenomenon/ cause		1. When measuring the bus-driver output voltage V_{OL}, destruction occurred because the input current I_{OL} (100–300 mA) was kept constant. 2. When measuring the breakdown voltage (for an IC of 70 V or greater) with a current of 1 mA, the same destruction (as in (1) above) occurred. 3. When measuring the breakdown voltage (as in (2)), noise superimposed on the constant current source, entered the negative range and caused destruction.
Countermeasure/ verification examples		1. Use methods that apply voltages rather than current injection. 2. Apply voltages, within the breakdown voltage and measure the current. 3. When a method that includes the application of a current shall be used, it is effective to check the contacts in the previous sequence.

Example 39 Destruction during Measurement

No. 39	Example	Destruction during measurement
Type of device		Small surface mount device
Point		Beware of contact defects when taking measurements
Summary of example/ phenomenon/ cause		When the semiconductor device to be measured was inserted into the tester socket at an angle, a spike surge occurred due to contact defects between the pins of the device and the tester socket, resulting in destruction of the IC.
Countermeasure/ verification examples		Place the contact check for the very beginning of the testing program. When contact defects are detected, the inspection shall be discontinued. In the case of reverse insertion, the inspection shall also be halted.

Example 40 Destruction due to Faulty Connections

No. 40	Example	Destruction due to faulty connections
Type of device		Linear IC
Point		Ensure correct connection and clarify emergency measures against faulty connections.
Summary of example/ phenomenon/ cause		When installing a set, the GND line was open and the V_{CC} connected, an IC failed due to a contact between its output terminals and GND. The moment the output terminals made contact with GND, high currents were drawn through an electrolytic capacitor between V_{CC} and GND, causing destruction.
Countermeasure/ verification examples		Place a clamping diode between the output terminals and GND.

5.11.2 Cautions During Inspections and Adjustments

When using an oscilloscope probe while inspecting or adjusting assembled printed circuit boards, be careful to avoid shorting the LSI's pins. Shorting the pins not only causes operation faults but also can lead to overcurrents which can damage the LSI.

1. When measuring, avoid the misconnection of terminals, reverse insertion, and shorting between terminals. When checking board (substrate) operations, check that there are no solder bridges or particle bridges before switching the power on.
2. Do not directly connect tester probes to LSI pins: instead, provide dedicated test pins. Even in circuits that operate correctly in normal use, the load capacitance increases when a semiconductor device is connected to an oscilloscope probe or test instruments for measurement. Noise or oscillation may be generated and circuits may malfunction. This can even lead to the destruction of the semiconductor device. Thus care is required when testing semiconductor devices. The wiring shall be kept short enough to prevent electrostatic induction and electromagnetic induction and the wiring capacitance shall be kept low. Avoid the use of long wiring to facilitate measurement.
3. When using a board check tester, note the same caution points (described above) as when using an LSI tester.
4. Connect unused input pins to VDD or GND to lower the input impedance. Although leaving some unused input pins unconnected may afford more flexibility for making design changes, it is not advisable because it reduces anti-noise protection.
5. Adequate control of electrical equipment is required so that leakage does not occur from electrical equipment such as AC power supplies to terminals of curve tracers, oscilloscopes, pulse generators, or stabilized DC power supply.

Example 41 Destruction due to the Removal and Insertion of a Connector

No. 41	Example	Destruction due to the removal and insertion of a connector
Type of device		IC, LSI
Point		The removal and insertion of live connectors is strictly prohibited. If this cannot be avoided, the design shall allow for this possibility.
Summary of example/ phenomenon/ cause		In user processing, failures occurred frequently so that a motor did not run (average failure rate was 2 to 5%). Examination revealed that IC inputs had been destroyed. During board inspection, the customer erroneously removed and inserted the connector while the DC supply was switched on. When this procedure was discontinued, the defects did not recur.
Countermeasure/ verification examples		1. Always disconnect the power supply before connecting the board. 2. Insert protective resistors at the input terminals of the IC that was destroyed.

5.12 Software Precautions

The number of products in which microcontrollers are used has increased considerably in recent years. In most cases it has become possible for the user to customize the functions with software; this is very convenient, but is also a source of problems. If a problem occurs infrequently in the final product and is difficult to reproduce, it can be extremely difficult to determine whether the problem is in the LSI or in the user's program.

Typical examples include malfunctions that sometimes occur and sometimes do not depending on the internal RAM data pattern at power on.

From the viewpoint of protecting confidential information, many functions have come to be realized in software. We are entering an age in which functions such as error logging and the load-and-go execution of small programs in RAM are handled by combinations of hardware and software. When a failure occurs, confirm that software written for the system do not include an error.

Example 42 Program Malfunction in Referring to an Indeterminate RAM Area

No. 42	Example	Program malfunction in referring to an uninitialized RAM area
Type of device		Microcontroller
Point		Contents of uninitialized RAM shall not be used in a program.
Summary of example/ phenomenon/ cause		In a user's pre-production, small percentage of operation defects occurred when power was turned ON. When only a short time elapsed between turning power OFF and turning it ON again, reproducibility of the defects was very poor. When the smoothing capacitor was shorted and completely discharged after power was turned OFF, the defect became easy to reproduce. As a result of analyzing the user's program, it was found that uninitialized RAM content at a certain address was used as a branch in the program; it was judged that sometimes when power was turned ON this RAM data was inverted, causing the malfunction.
Countermeasure/ verification examples		1. RAM contents that are not initialized shall not be used as a branch statement. 2. When developing a program, check operation after the RAM content is initialized to set or reset state.

5.13 Being Prepared for Possible Malfunction

As the concept of "yield" indicates, semiconductor devices cannot be manufactured so that 100% of units produced function correctly. Furthermore, the fact that it is impossible to completely test 100% of units shipped means that it is not possible to achieve failsafe operation in end products for possible malfunctions with designs that only consider semiconductor devices as the component units. Such product as a relay that has certain characteristics as to how it behaves when it is destroyed. When the natural phenomenon of gravity could be utilized, that characteristic could be used in system design, but unfortunately the characteristics of semiconductor device failure are not that simple. Types of failures include broken or shorted wires, and open low stack or high stack. This fact can be used to judge that the output of a high or low-level signal (not a fixed level) is evidence of normal operation. In addition, by using this type of judgment together with the watchdog function, much higher fail-safe operation can be obtained than with a relay circuit. Considering these, the end user shall make the necessary adjustments in the user system.

Example 43 Watchdog and Fail Safe

No. 43	Example	Watchdog and fail safe
Type of device		Microcontroller
Point		The division of roles between hardware and software in the watchdog function is important.
Summary of example/ phenomenon/ cause		The watchdog function is effective in maintaining the safety of a system. The watchdog function uses both hardware and software to reverse the output at certain pins at regular intervals; if an interval deviates from the design value, the problem can be detected from a separate monitoring circuit and the system adjusted in the direction of safety to prevent the worst from happening. In this case, it is important that the reversal of output at regular intervals not be achieved with hardware alone. If this were done, it would no longer be possible to verify that software operation is normal.
Countermeasure/ verification examples		1. Let the program run away to test the cooperative protective functions. 2. Degenerate the hardware signal to test the cooperative protective functions.

With the development of digital processing technology including microcontrollers, it has become possible to let these systems perform very sophisticated judgments. At the same time, the number of cases of completely unexpected types of malfunction has been increasing. Between the hardware component manufacturer and the user who develops a system and software, great difficulties occur when malfunction is intermittent. In systems in which a high degree of reliability is required, it shall be considered that not only in cases of frequent occurrence of a fault but also in case of a fault that occurs infrequently and might be difficult to reproduce it in a test, an error logging function shall be built into the system. In the case of a microcontroller with a stored program, electronic components such as the register and memory can

change the flow of the program. A function shall be included in the system so that when abnormal operation is detected, the data from these important parts will be stored and can be investigated later. This will greatly contribute to finding leads that can be followed up to solve the problem. If possible, in addition to these functions, it is possible to obtain even greater analytic power by using a data load and go function for the RAM area.

Example 44 Microcontroller Intermittent Failure Analysis

No. 44	Example	Microcontroller intermittent failure analysis
Type of device		Microcontroller
Point		In analysis of intermittent defects, search for the cause starting from differences in the contents of RAM and registers during normal and erroneous operation.
Summary of example/ phenomenon/ cause		In a product that used a microcontroller, the program ran away intermittently, but the cause could not be determined and efforts to solve the problem took a long time. Since the device was being used in single-chip mode, the history of data changes on the address and data lines during the malfunction could not be ascertained; it was not possible to determine the reason for the microcontroller going into runaway execution from the data on the output pins alone.
Countermeasure/ verification examples		If it is confirmed that a problem has occurred but the failure is an intermittent one that occurs very infrequently, information regarding the problem will always remain in variable data areas. These data can also be used effectively as the information indicating that the logic of some parts operated correctly by elimination method. In applications that require high reliability, consideration shall be given to incorporating an error logging function from the beginning of development, and the system designed so that the cause of malfunction can be determined logically and appropriate action taken.

5.14 Cautions on Packing, Storage, Shipment and Handling

Recent semiconductor devices are of high quality and high reliability, but depending on such factors as handling by the user, mounting and the conditions of use, there are many factors that can lead to damage of the semiconductor device (electrostatic discharge, mechanical destruction, moist gas, etc.). First, let us discuss precautions with regard to possible damage of semiconductor devices in the storage case and during packaging.

5.14.1 Cautions on Handling Packing Containers

Renesas uses packing containers whose materials and structure are designed to preserve the original quality of the semiconductor devices they contain, even under the worst environment conditions that are expected. Note the following cautions when handling these packing containers.

(1) Tray Containers

When using a tray container that enables semiconductor devices to be divided into small groups, be careful to avoid bending of leads that can occur when the devices are bumped or pressed against the tray. If products will be baked while in a tray container, be sure to use a heat-proof tray. Make sure the tray is labeled either as “Heat Proof” or as “135°C $_{MAX}$ (heat-proof temperature)”. The baking conditions differ according to the product, so check the product specifications to avoid setting too high a baking temperature.

(2) Taped Products

The adhesive (non-peeling) strength of tape is affected by storage temperature and humidity conditions. The tape’s adhesive shall therefore be considered when transferring taped products to a mounting machine. In cases where mounting of products from adhesive tape is stopped and the remaining products are to be stored, avoid winding the tape too tightly, as it may cause some products to come loose from the tape.

(3) Products in Magazine Container

Be sure to use an anti-static agent on the magazine's outer material. Avoid excessive scraping or rinsing of the magazine's surface, which can remove the anti-static agent or reduce its effectiveness.

These storage cases are designed to be re-used and recycled. Therefore, both during and after use of the magazine container, be careful to protect it from damage and dirt while handling it. Re-using and recycling these containers is one way to reduce their environmental impact.

Use cases provided by Renesas when products shall be divided among several cases. If these cases cannot be used, note the following cautions when selecting the cases to be used.

1. Avoid materials that may cause chemical reactions or that may emit toxic gas.
2. The magazine must have a structure that is easy to transport and does not allow mechanical vibration and shock to destroy the contained semiconductor devices.
3. Use a conductive or static-proof material (such as by coating the material's surface with anti-static agent to protect product quality) in all parts of the case that come in contact with semiconductor device pins.

5.14.2 Packaging

A semiconductor device in a storage case shall be further packaged to protect it from outside effects such as a shock, rain water and soiling. The packages used for some common products are shown in Figure 5.30. Never reuse the magazines.

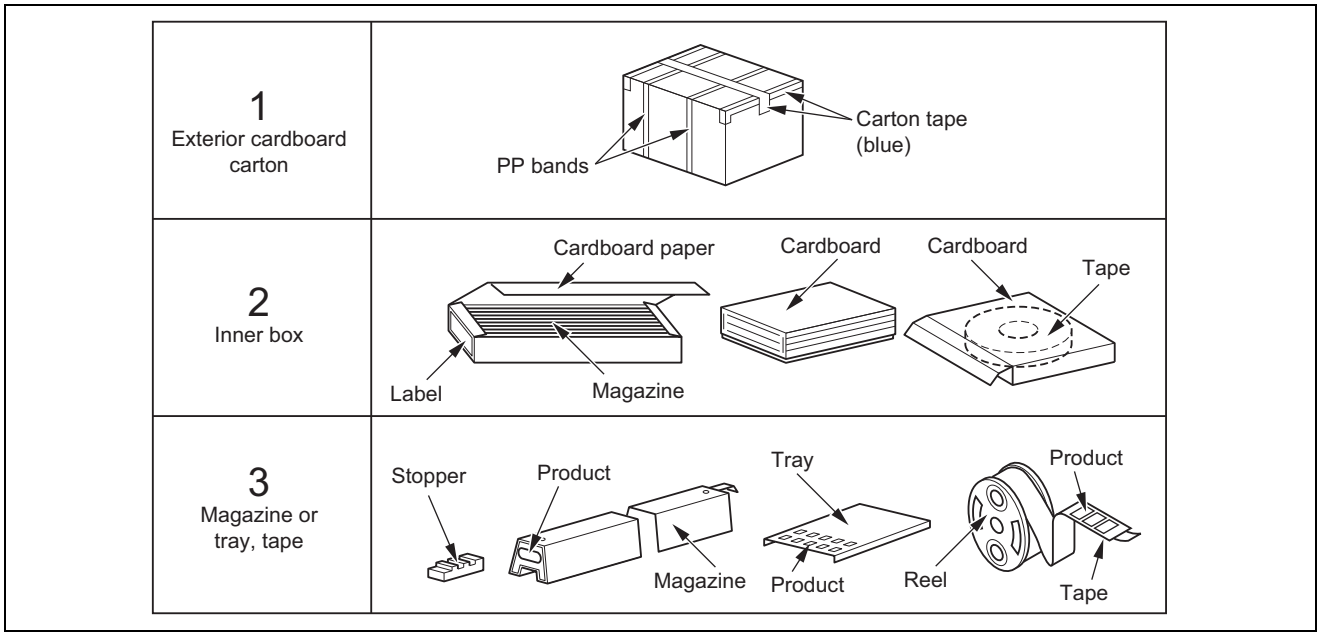


Figure 5.30 Example of Packaging

Opening the exterior cardboard carton reveals an inner box or boxes, inside of which is the storage case (magazine, tray or tape and reel), inside which the semiconductor devices reside. In the case of plastic surface-mount packages which have large chips, there is also moisture-proof packaging to prevent moisture absorption. Next, we give some precautions in packaging.

1. To keep the shock, vibrations and moisture to which the semiconductor device is subjected to a minimum, it is necessary to give serious consideration to using packaging that has sufficient mechanical strength, ability to withstand vibrations and ability to block moisture to meet the requirements of the transport method to be used. In general, the storage case is securely wrapped in polyurethane foam or vinyl, which in turn is put into a cardboard carton with sufficient packaging material to prevent vibrations, then the carton is closed with packing tape. Depending on the transport conditions, more secure packaging may become necessary.

2. The outside of the cardboard carton shall be labeled to indicate that the contents are fragile, shall not be allowed to become wet, which direction is up and so on. Figure 5.31 shows the example of such care mark labels.
3. If poor environmental conditions are anticipated, as in transport by sea, it is necessary to use vacuum packaging and sealed packaging.
4. The surfaces of transparent plastic magazines are treated to prevent them from becoming electrically charged, but this surface treatment degrades with time, so these magazines shall not be used for storage for more than the stipulated storage period. Never reuse the magazines.

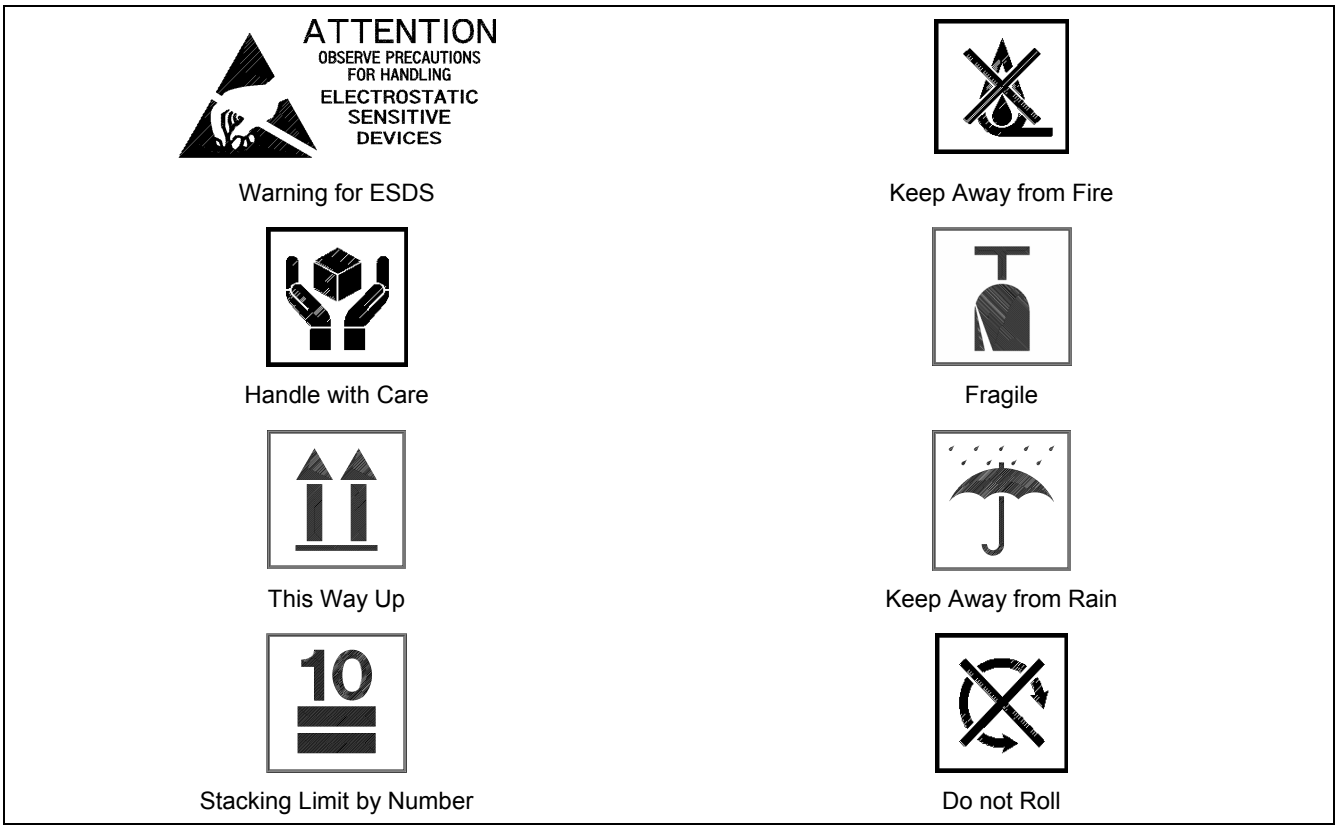


Figure 5.31 Example of Care Mark Labels Attached to Boxes

5.14.3 Storage Precautions

When storing semiconductor devices, it is necessary to protect them from environmental dangers including temperature, humidity, ultraviolet rays, poisonous or contaminating gases such as hydrogen sulphide, radiation including X-rays, static electricity and strong electromagnetic fields.

(1) Storage Environment

(a) Ambient Temperature and Humidity

The storage location shall be kept at normal temperature and humidity, that is 15 to 35°C and 45 to 75% relative humidity (some products have special restrictions on storage conditions, which shall be observed). Care shall be taken to avoid storage under temperature and humidity conditions that are significantly different from these. When it is very dry, such as during winter, it is necessary to use a humidifier. If tap water is used in the humidifier the chlorine in it can corrode leads of semiconductor devices, so purified or distilled water shall be used.

(b) Atmosphere and Cleanliness

Avoid storage in a location with corrosive gas or a large amount of dust.

(c) Temperature Variations

Sudden temperature variations can cause condensation to form on semiconductor devices and/or packing material, so avoid such an environment, and store semiconductor devices in a location where temperature variations are small and slow (and away from direct sunlight or other strong light).

(d) Electrical and Electromagnetic Environment

Store semiconductor devices in a location with free of radiation, static electricity and strong electromagnetic fields.

(2) Storage Conditions

1. In storing semiconductor devices, it is necessary to make sure that they are not subjected to heavy loads. In particular, when boxes are stacked, it is possible to subject the semiconductors to excessive loads without realizing it. Of course it is also necessary to avoid placing heavy objects on top of them (see Figure 5.32).

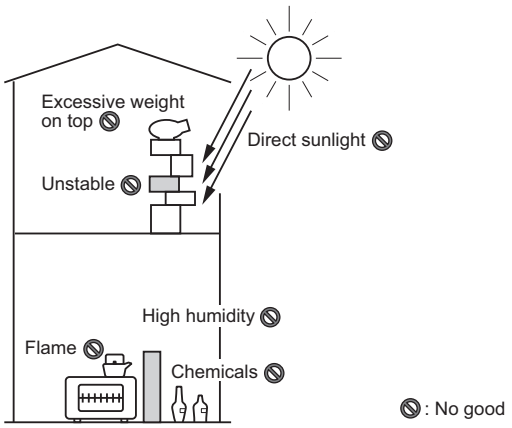


Figure 5.32 Examples of Poor Storage Locations and Practices

2. Store semiconductor devices without processing their external leads. This is to avoid degrading the adherence of solder during mounting due to, for example, rust (see Figure 5.33).

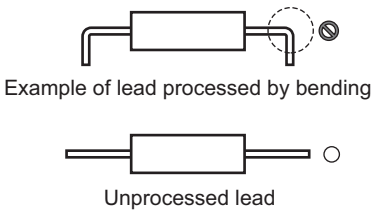


Figure 5.33 Storage Condition

3. Place semiconductor devices only in containers that do not readily become electrostatic-charged.

(3) Storage of Chips and Wafers

Semiconductor chips and wafers shall be stored under more strictly controlled conditions than package products. Absolutely avoid storing chips and wafers in conditions in which they are exposed to the outside air.

1. Store chips and wafers in the designated types of containers, and do not open and close the containers any more than absolutely necessary. Normally, chip storage containers are airtight sealed to protect chips and wafers from temperature, humidity and corrosive gases, and from vibrations and shock during transport (see Figure 5.34).
2. Do not store chips and wafers in opened containers. This is to prevent the chips and wafers from being oxidized or corroded due to changes in temperature and humidity, and the presence of gases, dust and chemicals.
3. Store chips and wafers in an atmosphere at 15 to 35ºC and 45 to 75% RH in principle, where they will not be affected by chemicals or volatile substances.
4. When putting a chip or wafer into or taking it out of a storage container, handle it gently using vacuum tweezers or a vacuum collet so that the surface will not be scratched.
5. Recommended storage conditions may vary from product to product. For details, contact your Renesas sales representative.

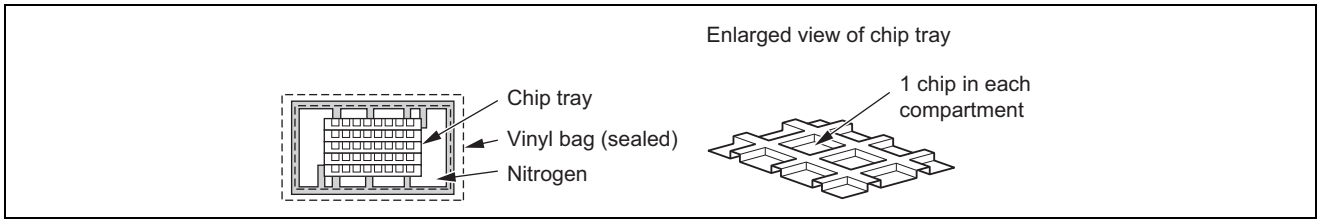


Figure 5.34 Examples of Chip Storage Containers

Example 45 Solderability Defects that can Develop during Storage

No. 45	Example	Solderability defects that can develop during storage
Type of device		IC
Outline of example		Magazines made of cardboard paper and black rubber were used for IC storage, causing the device lead wires to become discolored and leading to solderability defects. The lead surface material was converted to sulphide by sulphur compounds contained in the storage magazines.
Countermeasure example		Storage cases and magazines made of material that does not react with the lead wires shall be used. In particular, sulphur compounds shall be avoided.

5.14.4 Precautions in Transport

In transport of semiconductor devices and of units and subsystems which incorporate semiconductor devices, the same precautions shall be observed that are necessary for other electronic components; in addition, the points listed below shall be considered.

1. Handle the cardboard cartons used as the exterior packaging carefully. In particular, be careful not to subject them to shocks or drop them as this can damage the products inside.
2. Be particularly careful in handling the interior boxes. If these are dropped, stoppers can fall out of the magazines inside allowing the products to fall out and causing the leads to become deformed. Ceramic packages can be damaged, causing leakage defects.
3. It is necessary to make sure that the products do not become wet. Be particularly careful when transporting them through rain and/or snow (Do not permit products to become a wet).
4. Transport containers and jigs shall not be easily charged and not generate electrostatic charge when subjected to vibrations. One effective measure is to use conducting containers or aluminum foil.
5. To prevent components from being destroyed by electrostatic charge on the body and/or clothing, ground the body through a high resistance to discharge static electricity when handling semiconductor devices. The resistance shall be

about 1 MΩ. It is necessary for the resistor to be inserted into the connection between body and ground at a position relatively close to the body to prevent danger of electrical shock.

6. In transporting a printed circuit board with semiconductor devices mounted on it, it is necessary to take a measure, such as shorting the lead terminals to keep them at the same potential, to prevent them from becoming charged with static electricity. If a printed circuit board is transported on a belt conveyor, take an appropriate measure to prevent electrical charging by the belt rubber.
7. When transporting a semiconductor device or printed circuit board, keep mechanical vibrations and shocks to an absolute minimum.
8. Wafer shipments particularly shall be handled very carefully to prevent vibration and shock during transport and movement.

5.15 Examples of Other Categories of Problems

Finally, we introduce several examples that require mention and that do not fit into any of the categories that have been presented thus far.

Example 46 Tape Peeling Off Caused by High-Speed Peeling in the Case of Tape and Reel Products

No. 46	Example	Tape peeling off caused by high-speed peeling in the case of tape and reel products
Type of device		Embossed taping products
Point		The strength of embossed tape to being peeled off shall be measured at the actual speed to be used.
Summary of example/ phenomenon/ cause		Even though no problem occurred in the embossed taping certification test, the tape frequently peeled off during the users mounting process. An investigation revealed that, in the line in which the defect occurred, the most recent model of high speed mounting machine was being used, and the tape peel-off speed was faster than the previous speed in order to increase the component mounting index time. In a test in which the tape peel-off speed was increased, the defect was reproduced.
Countermeasure/ verification examples		1. In the embossed tape peel-off test, attention shall be paid to the peel-off speed. 2. In the embossed tape peel-off test, one shall not forget to apply the stress of storage as preprocessing.

Example 47 Changes in Characteristics Caused by X-ray Irradiation

No. 47	Example	Changes in characteristics caused by X-ray irradiation
Type of device		MOS IC (plastic sealed)
Outline of example		In an X-ray penetration test, the semiconductor device was irradiated with X-rays for a long time, and the IC came to have defective characteristics. The IC's MOS parameter (Vth) fluctuated, causing deterioration of characteristics.
Countermeasure example		The X-rays with which the device is irradiated shall be kept as weak as possible.

Example 48 Bonding Stress in Mounting Chips that Have Been Shipped

No. 48	Example	Bonding stress in mounting chips that have been shipped
Type of device		Power MOS FET
Point		The oxide film below the bonding pad is destroyed by the stress of bonding.
Summary of example/ phenomenon/ cause		When the characteristics of chips that had been shipped (power MOS FETs) were tested after mounting by the user, the breakdown voltage between source and gate was insufficient. As a result of analysis, it was judged that the oxide film below the gate bonding was cracked, causing the breakdown voltage to deteriorate. The cause was inadequate checking of the conditions at the time of mounting.
Countermeasure/ verification examples		After the bonding conditions are set, the characteristics need to be checked, and, at the same time, the aluminum film below the bonded section shall be removed and the silicon oxide film s shall be checked for cracking.

Example 49 Leakage from Airtight Seal due to Electrolytic Corrosion

No. 49	Example	Leakage from airtight seal due to electrolytic corrosion
Type of device		Glass diode
Point		A voltage shall not be applied to a product to which moisture is adhering.
Summary of example/ phenomenon/ cause		Copper oxide (Cu_2O) that forms on the surface of the copper layer of a Dumet line diffuses into the glass, bonding to form an airtight construction. While a reverse bias is applied, water that adheres to the diode surface is decomposed electrolytically by reverse bias, and hydrogen (H_2) is generated on the anode side. This hydrogen reduces the cuprous oxide; water penetrates where the reduction took place, producing a cavity and destroying the airtightness. Destruction of the airtightness in turn permits more moisture to penetrate into the cavity. Moisture penetration produces a leakage current on the surface of the chip, increasing the reverse current (IR). If the reverse bias continues to be applied while the reverse current is flowing, migration of the silver (Ag) electrode of a chip occurs.
Countermeasure/ verification examples		The IR becomes large due to fluctuations in the electrical characteristics. View the inside from the glass package.
Reference item		Diode Data Book

Example 50 Signal Data Collision

No. 50	Example	Signal data collision
Type of device		IC, LSI
Outline of example		For memory ICs having common input/output terminals, when data is at output state and an input signal with the opposite direction is applied, data collision will occur and generate excessive current flow. The resulting supply voltage variation may cause malfunction or device destruction.
Countermeasure example		1. Timing design shall be made to prevent data collision. 2. Timing shall be changed using latch.

Example 51 Destruction of Device due to Condensation

No. 51	Example	Destruction of device due to condensation
Type of device		Power MOS FET
Outline of example		Although we knew that products already on the market were regularly being destroyed by condensation, we had difficulty determining the cause of the defect from destroyed devices. In fact, however, the problem was occurring only with the same model of a product purchased by particular customers. Our investigation into seasonal occurrence revealed that the problem worsened during the summer season. When we checked the customer's operating environment, we found that the customer had installed a system near the nozzle of an air conditioner. As a result, cold air from the air conditioner caused condensation, leading to leakage between terminals and destruction of the device. Once the system was relocated away from the air conditioner nozzle, the products were no longer being destroyed.
Countermeasure example		Check the environment where the product will be used to make sure that it is not a particular kind of environment.

A. Sampling Inspection

A.1 What Is Sampling Inspection?

Sampling inspection is a type of inspection that is performed on sample products which are randomly selected from a lot. The entire lot is either accepted or rejected based on the results of sampling inspection. In other words, this type of inspection allows certain amounts of risk: the producer's risk (probability α) that a nondefective lot may be rejected and the consumer's risk (probability β) that a defective lot may be accepted. Sampling inspections are the norm for semiconductor devices; full-lot inspections are not feasible since breakdown tests are sometimes required as reliability tests and lot sizes tend to be rather large.

This appendix describes the quality control type of sampling inspections that are performed as shipment inspections, and also briefly describes sampling inspections that are performed as part of reliability testing.

(1) OC Curve

Given "N" as the lot size, "p" as the defect rate, "n" as the number of samples taken from the lot, and "x" as the number of defective items among the samples, it is possible to calculate the probability of defectives as P (x). A hypergeometric distribution, binomial distribution, or Poisson distribution (see equations below) can be extracted based on factors such as the lot size. The following is a Poisson distribution.

$$P(x) = e^{-pn}\frac{(pn)^x}{x!}$$

The acceptance (α) or rejection (β) probability is expressed as follows.

$$1-\alpha = 1-L(P0)$$
$$\beta = L(P1)$$

Figure A.1 shows an OC curve that describes quality characteristics (such as the defect rate) by using the acceptance probability as its vertical axis and the rejection probability as its horizontal axis.

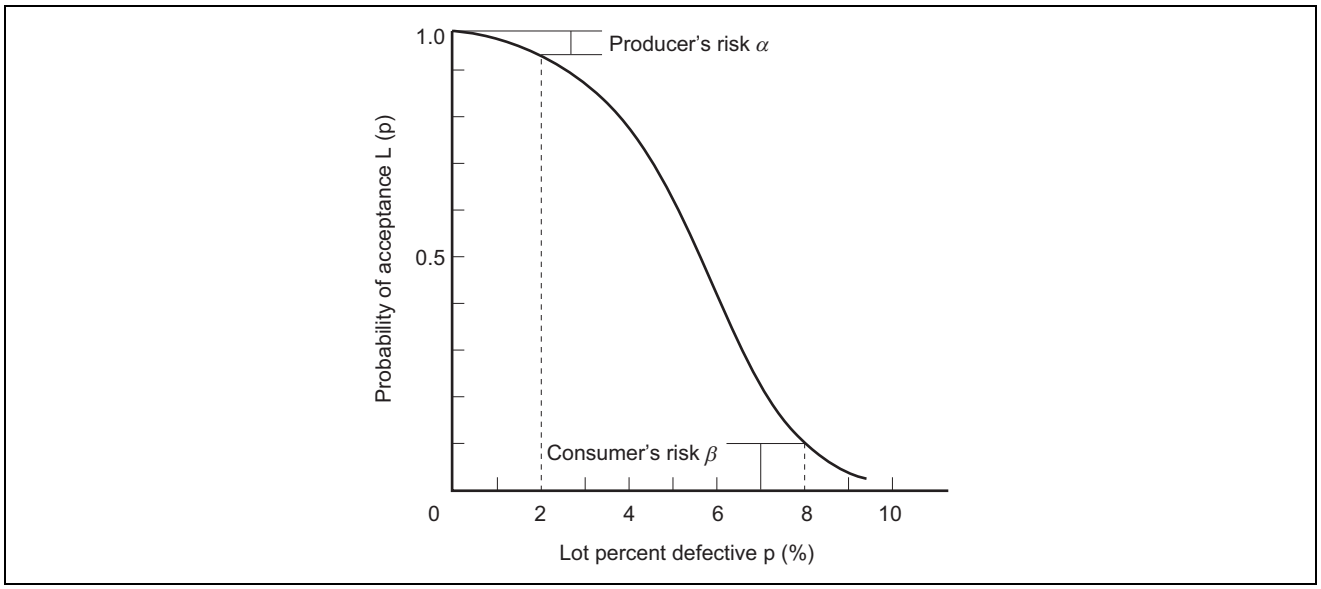


Figure A.1 OC Curve

The above diagram is called an "Operating Characteristic curve", or "OC curve" for short.

The OC curve is obtained when the conditions for the sampling method are determined. The probability a lot with a given quality will be accepted or rejected can be read from the OC curve.

For example, during single sampling inspection by attributes based on operating characteristics (as defined by JIS Z 9002), if P0 = 1.0% and P1 = 5.0%, then n = 120 and C = 3. The corresponding OC curve is shown in Figure A.2, and the lot acceptance probability can be interpreted as shown below.

If p = P0 = 1.0%, then *L(P0) ≈ 0.97*

If p = P1 = 5.0%, then *L(P1) ≈ 0.14*

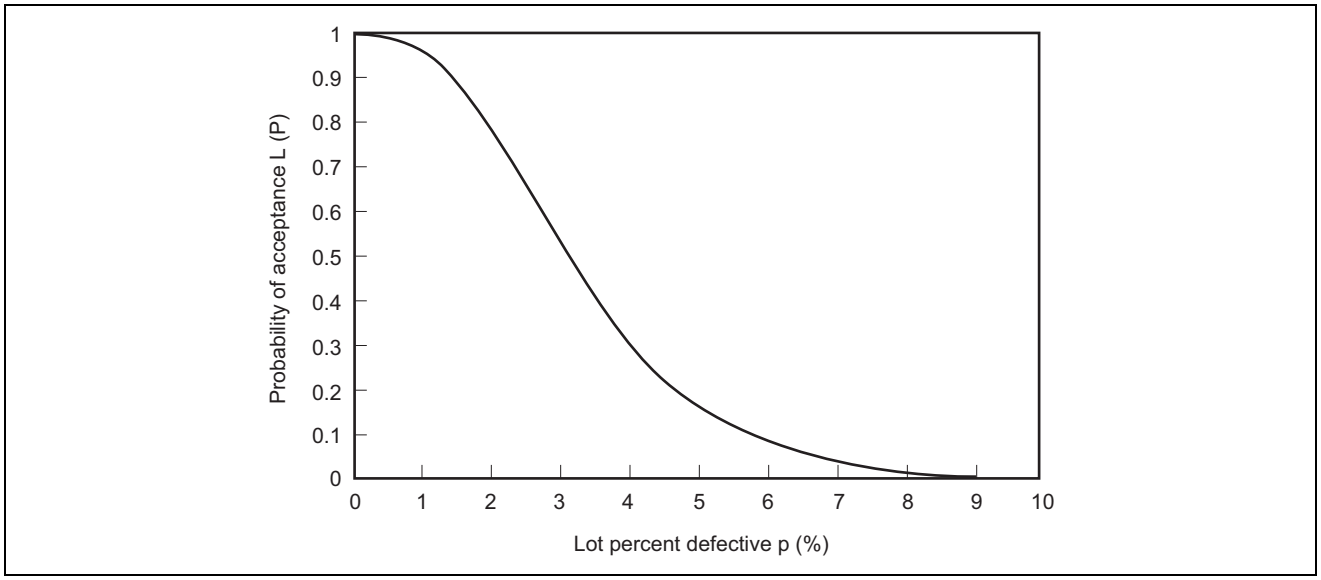


Figure A.2 OC Curve When P0 = 1% and P1 = 5%

In other words, this curve indicates that there is a 0.03% producer's risk (probability α) that a nondefective lot having defect rate P0 will be incorrectly judged as a rejected lot, or there is a 0.14% consumer's risk (probability β) that a defective lot having defect rate P1 will be incorrectly judged as an accepted lot.

The effectiveness of sampling curves is determined based not only on OC curves; it also depends greatly on the inspected lot's average defect rate and the amount of variation reflected in the rate.

(2) Types of Sampling Inspections

The following are some types of sampling inspections.

- Sampling inspection by attributes or by variables
- Sampling inspection based on operating characteristics, screening, adjustments, or continuous production
- Single, double, multiple, or sequential sampling inspection

For example, JIS Z 9002 describes single sampling inspection by attributes based on operating characteristics.

Below, AQL and LTPD methods are briefly explained as two of the many sampling inspection methods.

(3) AQL and LTPD

The AQL (Acceptable Quality Level) is established based on an OC curve which describes the probability (1−α) that a lot having defect rate P0 will be accepted. This method is part of the sampling inspection by attributes based on operating characteristics defined in MIL-STD-105 and JIS Z 9015.

The severity of sampling inspections is adjusted among the following three severity levels, according to quality level factors such as past lot inspection results.

- Normal level: Quality level has been generally near the AQL.
- Tightened level: Quality level has been clearly worse than the AQL.

- Reduced level: Quality level has been generally above the AQL and is expected to remain above the AQL.

In addition, an inspection level is established based on the relation between the lot size and the number of samples (i.e., the proportional inspection volume). The inspection level is also established based on other factors, such as inspection costs and consistency of quality within and between lots. Although there are seven inspection levels, including ordinary inspection levels I to III and special inspection levels S-1 to S-4, general level II is generally used unless a special level is specified.

The AQL resembles the defect rate (P0) used in OC curves in that both refer to a threshold value of quality as a criterion for accepting or rejecting sampled lots. However, AQL differs from P0 in the following ways.

1. P0 refers to an individual lot, while AQL refers to an average for a process.
2. P0 indicates one point on an OC curve as an attribute combined with the producer's risk (α) but this α value changes according to factors such as lot size when AQL is used instead of P0.

Example: At this time, given a lot size of 5000 and an AQL of 0.65, a 200-unit sample, Ac = 3, and Re = 4 is taken. The lot is accepted if there are no more than three defectives in the sample (the "acceptance number") and is rejected if there are four or more defectives (the "rejection number").

The LTPD (Lot Tolerance Percent Defective) is established based on an OC curve which describes the probability (1−β) that a lot having defect rate P1 will be rejected. There are exponential distribution single-sample sampling methods, for example, such as stipulated in MIL-PRF-195000. Note that MIL-PRF-19500 uses β = 0.1 as the probability. Consequently, LTPD is the defect rate for an inspection lot for which the acceptance probability in sampling inspections is β = 0.1, which corresponds to P1 on an OC curve.

The LTPD sampling table shown below was calculated based on a Poisson distribution and can be used when the lot size (N) is at least 200. Therefore, for lot sizes of less than 200, a sampling table calculated based on a hypergeometric distribution must be used.

The table's horizontal axis shows LTPD values (unit percentages), but when implementing a sampling inspection based on failure rates these values can also be viewed as lot tolerance failure rates (unit percentage divided by 1000 hours). However, when implementing a sampling inspection based on failure rates, the minimum number of defective units as read from the LTPD sampling table can be replaced by a component hour value (acceleration coefficient × units × time) that is 1,000 times greater.

Example: To guarantee (using "1" as the acceleration coefficient) the results of 1000 hours of testing in which the lot sizes were established as more than 200 units and in which λ = 1% / 1000 hours, if the acceptance number (C) is 0, a sample size (n) of 231 units is required.

(4) Sampling Tests as Part of Reliability Testing

There is no substantial difference between sampling tests performed as part of reliability testing and sampling tests performed as part of quality control. The main differences are explained below.

1. Scale Reliability: Failure rate (λ), MTBF, etc.
   Quality control: Defect rate (p)
2. Distribution Reliability: Mainly uses exponential distribution
   Quality control: Normal distribution
3. When used for reliability testing, sampling tests are sometimes cut short since a lot of time is needed to check failures in all sample units.
   λ0: Acceptable quality level
   ARL: Acceptable Reliability Level
   AFR: Acceptable Failure Rate
   λ1: LTFR (Lot Tolerance Failure Rate)
   α: Producer's risk (1−α = lot acceptance rate)
   β: Consumer's risk
   λ0/ λ1: Discrimination ratio (normally selectable between 1.5 and 3.0).

Example: Let us consider a fixed time single sampling LTFR method (repair-related). Total test period: if k times is the number of failures for nT, the acceptance rate can be determined as shown below.

$$Pr(x) = \frac{(n\lambda T)^x}{x!} e^{-n\lambda T}$$

$$L(p_k) = \sum_{k=0}^{c} \frac{(n\lambda T)^k}{k!} e^{-n\lambda T}$$

$$= \int_{2n\lambda T}^{\infty} g_{2(c+1)}(\zeta)\, d\zeta$$

The last term in the above expression is the density function of a chi-square distribution of degree of freedom 2 (c + 1). The following establishes L (λ) as less than β.

$$2n\lambda T > \chi^2(2(c+1), \beta)$$

Consequently, T must be obtained to satisfy the above expression.

Given n = 10, β = 0.1, λ = 0.001, and c = 0:

$$\chi^2(2(0+1), 0.1) = \chi^2(2, 0.1) = 4.61$$

$$T = \frac{4.61}{2 \times 10 \times 0.001} = 231$$

Thus, the lot is accepted if no failures occur during 231 hours of testing.

A.2 AQL Sampling Table (MIL-STD-105)

Table A.1 Sample Size Code Letters

Lot Size	Special Inspection Level				General Inspection Level		
	S-1	S-2	S-3	S-4	I (Table A.2)	II (Table A.3)	III (Table A.4)
2 – 8	A	A	A	A	A	A	B
9 – 15	A	A	A	A	A	B	C
16 – 25	A	A	B	B	B	C	D
26 – 50	A	B	B	C	C	D	E
51 – 90	B	B	C	C	C	E	F
91 – 150	B	B	C	D	D	F	G
151 – 280	B	C	D	E	E	G	H
281 – 500	B	C	D	E	F	H	J
501 – 1200	C	C	E	F	G	J	K
1201 – 3200	C	D	E	G	H	K	L
3201 – 10000	C	D	F	G	J	L	M
10001 – 35000	C	D	F	H	K	M	N
35001 – 150000	D	E	G	J	L	N	P
150001 – 500000	D	E	G	J	M	P	Q
500001 and over	D	E	H	K	N	Q	R

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Note: MIL-STD-105 is replaced by ANSI standard ANSI/ASQC Z 1.4.

Table A.2 Single Sampling Plan for Normal Inspection (Master Table)

Sample Size Code Letter	Sample Size	Acceptable Quality Level (AQL) (Normal Inspection)																												
		0.010	0.015	0.025	0.040	0.065	0.10	0.15	0.25	0.40	0.65	1.0	1.5	2.5	4.0	6.5	10	15	25	40	65	100	150	250	400	650	1000
		Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re
A	2	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	0 1	↓	↓	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	30 31	↑
B	3	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	0 1	↑	↓	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	30 31	44 45	↑
C	5	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	0 1	↑	↓	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	30 31	44 45	↑	↑
D	8	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	0 1	↑	↓	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	30 31	44 45	↑	↑	↑
E	13	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	0 1	↑	↓	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	30 31	44 45	↑	↑	↑	↑
F	20	↓	↓	↓	↓	↓	↓	↓	↓	↓	0 1	↑	↓	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	↑	↑	↑	↑	↑	↑	↑
G	32	↓	↓	↓	↓	↓	↓	↓	↓	0 1	↑	↓	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	↑	↑	↑	↑	↑	↑	↑	↑
H	50	↓	↓	↓	↓	↓	↓	↓	0 1	↑	↓	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	↑	↑	↑	↑	↑	↑	↑	↑	↑
J	80	↓	↓	↓	↓	↓	↓	0 1	↑	↓	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
K	125	↓	↓	↓	↓	↓	0 1	↑	↓	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
L	200	↓	↓	↓	↓	0 1	↑	↓	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
M	315	↓	↓	↓	0 1	↑	↓	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
N	500	↓	↓	0 1	↑	↓	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
P	800	↓	0 1	↑	↓	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
Q	1250	0 1	↑	↓	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
R	2000	↑	↑	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑

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↓ = Use first sampling plan below arrow. If sampling size equals, or exceeds, lot or batch size, do full-lot inspection.

↑ = Use first sampling plan above arrow.

Ac = Acceptance number

Re = Rejection number

Table A.3 Single Sampling Plan for Tightened Inspection (Master Table)

Sample Size Code Letter	Sample Size	Acceptable Quality Level (AQL) (Tightened Inspection)																											
		0.010	0.015	0.025	0.040	0.065	0.10	0.15	0.25	0.40	0.65	1.0	1.5	2.5	4.0	6.5	10	15	25	40	65	100	150	250	400	650	1000
		Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re
A	2	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	1 2	2 3	3 4	5 6	8 9	12 13	18 19	27 28	↑
B	3															0 1	↓	↓	↓	1 2	2 3	3 4	5 6	8 9	12 13	18 19	27 28	41 42	↑
C	5														0 1		↓	↓	1 2	2 3	3 4	5 6	8 9	12 13	18 19	27 28	41 42	↑	↑
D	8													0 1	↓	1 2	2 3	3 4	5 6	8 9	12 13	18 19	27 28	41 42	↑	↑	↑	↑	↑
E	13												0 1	↓	↓	1 2	2 3	3 4	5 6	8 9	12 13	18 19	27 28	41 42	↑	↑	↑	↑	↑
F	20											0 1	↓	↓	1 2	2 3	3 4	5 6	8 9	12 13	18 19	↑	↑	↑	↑	↑	↑	↑	↑
G	32										0 1	↓	↓	1 2	2 3	3 4	5 6	8 9	12 13	18 19	↑	↑	↑	↑	↑	↑	↑	↑	↑
H	50									0 1	↓	↓	1 2	2 3	3 4	5 6	8 9	12 13	18 19	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
J	80								0 1	↓	↓	1 2	2 3	3 4	5 6	8 9	12 13	18 19	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
K	125							0 1	↓	↓	1 2	2 3	3 4	5 6	8 9	12 13	18 19	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
L	200						0 1	↓	↓	1 2	2 3	3 4	5 6	8 9	12 13	18 19	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
M	315					0 1	↓	↓	1 2	2 3	3 4	5 6	8 9	12 13	18 19	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
N	500				0 1	↓	↓	1 2	2 3	3 4	5 6	8 9	12 13	18 19	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
P	800			0 1	↓	↓	1 2	2 3	3 4	5 6	8 9	12 13	18 19	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
Q	1250		0 1	↓	↓	1 2	2 3	3 4	5 6	8 9	12 13	18 19	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
R	2000	0 1	↑	↓	1 2	2 3	3 4	5 6	8 9	12 13	18 19	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
S	3150			1 2																									

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↓ = Use first sampling plan below arrow. If sampling size equals, or exceeds, lot or batch size, do full-lot inspection.

↑ = Use first sampling plan above arrow.

Ac = Acceptance number

Re = Rejection number

Table A.4 Single Sampling Plan for Reduced Inspection (Master Table)

Sample Size Code Letter	Sample Size	Acceptable Quality Level (AQL) (Reduced Inspection)																														
		0.010		0.015		0.025		0.040		0.065		0.10		0.15		0.25		0.40		0.65		1.0		1.5		2.5		4.0		6.5		10		15		25		40		65		100		150		250		400		650		1000	
		Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re
A	2																											0	1					1	2	2	3	3	4	5	6	7	8	10	11	14	15	21	22	30	31
B	2																															0	2	1	3	2	4	3	5	5	6	7	8	10	11	14	15	21	22	30	31
C	2																									0	1					1	3	1	4	2	5	3	6	5	8	7	10	10	13	14	17	21	24		
D	3																							0	1					0	2	1	3	1	4	2	5	3	6	5	8	7	10	10	13	14	17	21	24			
E	5																					0	1					0	2	1	3	1	4	2	5	3	6	5	8	7	10	10	13	14	17	21	24				
F	8																			0	1					0	2	1	3	1	4	2	5	3	6	5	8	7	10	10	13								
G	13																	0	1			0	2	1	3	1	4	2	5	3	6	5	8	7	10	10	13												
H	20															0	1					0	2	1	3	1	4	2	5	3	6	5	8	7	10	10	13												
J	32													0	1					0	2	1	3	1	4	2	5	3	6	5	8	7	10	10	13												
K	50											0	1					0	2	1	3	1	4	2	5	3	6	5	8	7	10	10	13														
L	80															0	2	1	3	1	4	2	5	3	6	5	8	7	10	10	13																
M	125							0	1					0	2	1	3	1	4	2	5	3	6	5	8	7	10	10	13																		
N	200					0	1			0	2	0	2	1	3	1	4	2	5	3	6	5	8	7	10	10	13																				
P	315			0	1			0	2	0	2	1	3	1	4	2	5	3	6	5	8	7	10	10	13																						
Q	500	0	1			0	2	1	3	1	4	2	5	3	6	5	8	7	10	10	13																										
R	800					0	2	1	3	1	4	2	5	3	6	5	8	7	10	10	13																										

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↓ = Use first sampling plan below arrow. If sampling size equals, or exceeds, lot or batch size, do full-lot inspection.

↑ = Use first sampling plan above arrow.

Ac = Acceptance number

Re = Rejection number

↑ = If acceptance number has been exceeded, but the rejection number has not been reached, accept the lot, but reinstate normal inspection.

A.3 LTPD Sampling Table (MIL-PRF-19500)

Table A.5 LTPD Sampling Table (1/2)

Minimum sample size required to guarantee with 90% reliability that lots having the defect rate specified by LTPD (or an equivalent defect rate) will not be accepted.

Maximum Defect Rate (LTPD) or λ	50	30	20	15	10	7	5	3
Acceptance number (C) (r = C + 1) Minimum sample size (For device hours required for life test multiply by 1000)								
0	5 (1.03)	8 (0.64)	11 (0.46)	15 (0.34)	22 (0.23)	32 (0.16)	45 (0.11)	76 (0.07)
1	8 (4.4)	13 (2.7)	18 (2.0)	25 (1.4)	38 (0.94)	55 (0.65)	77 (0.46)	129 (0.28)
2	11 (7.4)	18 (4.5)	25 (3.4)	34 (2.24)	52 (1.6)	75 (1.1)	105 (0.78)	176 (0.47)
3	13 (10.5)	22 (6.2)	32 (4.4)	43 (3.2)	65 (2.1)	94 (1.5)	132 (1.0)	221 (0.62)
4	16 (12.3)	27 (7.3)	38 (5.3)	52 (3.9)	78 (2.6)	113 (1.8)	158 (1.3)	265 (0.75)
5	19 (13.8)	31 (8.4)	45 (6.0)	60 (4.4)	91 (2.9)	131 (2.0)	184 (1.4)	308 (0.85)
6	21 (15.6)	35 (9.4)	51 (6.6)	68 (4.9)	104 (3.2)	149 (2.2)	209 (1.6)	349 (0.94)
7	24 (16.6)	39 (10.2)	57 (7.2)	77 (5.3)	116 (3.5)	166 (2.4)	234 (1.7)	390 (1.0)
8	26 (18.1)	43 (10.9)	63 (7.7)	85 (5.6)	128 (3.7)	184 (2.6)	258 (1.8)	431 (1.1)
9	28 (19.4)	47 (11.5)	69 (8.1)	93 (6.0)	140 (3.9)	201 (2.7)	282 (1.9)	471 (1.2)
10	31 (19.9)	51 (12.1)	75 (8.4)	100 (6.3)	152 (4.1)	218 (2.9)	306 (2.0)	511 (1.2)
11	33 (21.0)	54 (12.8)	83 (8.3)	111 (6.2)	166 (4.2)	238 (2.9)	332 (2.1)	555 (1.2)
12	36 (21.4)	59 (13.0)	89 (8.6)	119 (6.5)	178 (4.3)	254 (3.0)	356 (2.2)	594 (1.3)
13	38 (22.3)	63 (13.4)	95 (8.9)	126 (6.7)	190 (4.5)	271 (3.1)	379 (2.26)	632 (1.3)
14	40 (23.1)	67 (13.8)	101 (9.2)	134 (6.9)	201 (4.6)	288 (3.2)	403 (2.3)	672 (1.4)
15	43 (23.3)	71 (14.1)	107 (9.4)	142 (7.1)	213 (4.7)	305 (3.3)	426 (2.36)	711 (1.41)
16	45 (24.1)	74 (14.6)	112 (9.7)	150 (7.2)	225 (4.8)	321 (3.37)	450 (2.41)	750 (1.44)
17	47 (24.7)	79 (14.7)	118 (9.86)	158 (7.36)	236 (4.93)	338 (3.44)	473 (2.46)	788 (1.48)
18	50 (24.9)	83 (15.0)	124 (10.0)	165 (7.54)	248 (5.02)	354 (3.51)	496 (2.51)	826 (1.51)
19	52 (25.5)	86 (15.4)	130 (10.2)	173 (7.76)	259 (5.12)	370 (3.58)	518 (2.56)	864 (1.53)
20	54 (26.1)	90 (15.6)	135 (10.4)	180 (7.82)	271 (5.19)	386 (3.65)	541 (2.60)	902 (1.56)
25	65 (27.0)	109 (16.1)	163 (10.8)	217 (8.08)	326 (5.38)	466 (3.76)	652 (2.69)	1086 (1.61)

Notes: 1. The sample sizes are based on the Poisson binomial distribution exponent's limit.

2. The minimum quality (approximate AQL) required to accept on the average 19 of 20 lots is shown in parenthesis for information only.

Table A.5 LTPD Sampling Table (2/2)

(Single sampling)

2	1.5	1	0.7	0.5	0.3	0.2	0.15	0.1
116 (0.04)	153 (0.03)	231 (0.02)	328 (0.02)	461 (0.01)	767 (0.007)	1152 (0.005)	1534 (0.003)	2303 (0.002)
195 (0.18)	258 (0.14)	390 (0.09)	555 (0.06)	778 (0.045)	1296 (0.027)	1946 (0.018)	2592 (0.013)	3891 (0.009)
266 (0.31)	354 (0.23)	533 (0.15)	759 (0.11)	1065 (0.080)	1773 (0.045)	2662 (0.031)	3547 (0.022)	5323 (0.015)
333 (0.41)	444 (0.31)	668 (0.20)	953 (0.14)	1337 (0.10)	2226 (0.062)	3341 (0.041)	4452 (0.031)	6681 (0.018)
398 (0.50)	531 (0.37)	798 (0.25)	1140 (0.17)	1599 (0.12)	2663 (0.074)	3997 (0.049)	5327 (0.037)	7994 (0.025)
462 (0.57)	617 (0.42)	927 (0.28)	1223 (0.20)	1855 (0.14)	3090 (0.085)	4638 (0.056)	6181 (0.042)	9275 (0.028)
528 (0.62)	700 (0.47)	1054 (0.31)	1503 (0.22)	2107 (0.155)	3509 (0.093)	5267 (0.062)	7019 (0.047)	10533 (0.031)
589 (0.67)	783 (0.51)	1178 (0.34)	1680 (0.24)	2355 (0.17)	3922 (0.101)	5886 (0.067)	7845 (0.051)	11771 (0.034)
648 (0.72)	864 (0.54)	1300 (0.36)	1854 (0.25)	2599 (0.18)	4329 (0.108)	6498 (0.072)	8660 (0.054)	12995 (0.036)
709 (0.77)	945 (0.58)	1421 (0.38)	2027 (0.27)	2842 (0.19)	4733 (0.114)	7103 (0.077)	9468 (0.057)	14206 (0.038)
770 (0.80)	1025 (0.60)	1541 (0.40)	2199 (0.28)	3082 (0.20)	5133 (0.120)	7704 (0.080)	10268 (0.060)	15407 (0.040)
832 (0.83)	1109 (0.62)	1664 (0.42)	2378 (0.29)	3323 (0.21)	5546 (0.12)	3319 (0.083)	11092 (0.062)	16638 (0.042)
890 (0.86)	1187 (0.65)	1781 (0.43)	2544 (0.30)	3562 (0.22)	5936 (0.13)	8904 (0.086)	11872 (0.065)	17808 (0.043)
948 (0.89)	1264 (0.67)	1896 (0.44)	2709 (0.31)	3793 (0.22)	6321 (0.134)	9482 (0.089)	12643 (0.067)	18964 (0.045)
1007 (0.92)	1343 (0.69)	2015 (0.46)	2878 (0.32)	4029 (0.23)	6716 (0.138)	10073 (0.092)	13431 (0.069)	20146 (0.046)
1066 (0.94)	1422 (0.71)	2133 (0.47)	3046 (0.33)	4265 (0.235)	7108 (0.141)	10662 (0.094)	14216 (0.070)	21324 (0.047)
1124 (0.96)	1499 (0.72)	2249 (0.48)	3212 (0.337)	4497 (0.241)	7496 (0.144)	11244 (0.096)	14992 (0.072)	22487 (0.048)
1182 (0.98)	1576 (0.74)	2364 (0.49)	3377 (0.344)	4728 (0.246)	7880 (0.148)	11819 (0.098)	15759 (0.074)	23639 (0.049)
1239 (1.0)	1652 (0.75)	2478 (0.50)	3540 (0.351)	4956 (0.251)	8260 (0.151)	12390 (0.100)	16520 (0.075)	24780 (0.050)
1296 (1.02)	1728 (0.77)	2591 (0.52)	3702 (0.358)	5183 (0.256)	8638 (0.153)	12957 (0.102)	17276 (0.077)	25914 (0.051)
1353 (1.04)	1803 (0.78)	2705 (0.52)	3864 (0.364)	5410 (0.260)	9017 (0.156)	13526 (0.104)	18034 (0.078)	27051 (0.052)
1629 (1.08)	2173 (0.807)	3259 (0.538)	4656 (0.376)	6518 (0.269)	10863 (0.161)	16295 (0.108)	21726 (0.081)	32589 (0.054)

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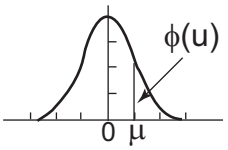
B. Attached Tables

B.1 Probability Density of Normal Distribution

$$\phi(u) = \frac{1}{\sqrt{2\pi}} e^{-\frac{u^2}{2}}$$



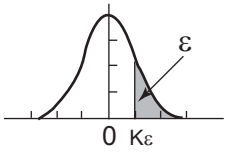
U	.00	.01	.02	.03	.04	.05	.06	.07	.08	.09
.0	.39894	.39892	.39886	.39876	.39862	.39844	.39822	.39797	.39767	.39733
.1	.39695	.39654	.39608	.39559	.39505	.39448	.39387	.39322	.39253	.39181
.2	.39104	.39024	.38940	.38853	.38762	.38667	.38568	.38466	.38361	.38251
.3	.38139	.38023	.37903	.37780	.37654	.37524	.37391	.37255	.37115	.36973
.4	.36827	.36678	.36526	.36371	.36213	.36053	.35889	.35723	.35553	.35381
.5	.35207	.35029	.34849	.34667	.34482	.34294	.34105	.33912	.33718	.33521
.6	.33322	.33121	.32918	.32713	.32506	.32297	.32086	.31874	.31659	.31443
.7	.31225	.31006	.30785	.30563	.30339	.30114	.29887	.29659	.29431	.29200
.8	.28969	.28737	.28504	.28269	.28034	.27798	.27562	.27324	.27086	.26848
.9	.26609	.26369	.26129	.25888	.25647	.25406	.25164	.24923	.24681	.24439
1.0	.24197	.23955	.23713	.23471	.23230	.22988	.22747	.22506	.22265	.22025
1.1	.21785	.21546	.21307	.21069	.20831	.20594	.20357	.20121	.19886	.19652
1.2	.19419	.19186	.18954	.18724	.18494	.18265	.18037	.17810	.17585	.17360
1.3	.17137	.16915	.16694	.16474	.16256	.16038	.15822	.15608	.15395	.15183
1.4	.14973	.14764	.14556	.14350	.14146	.13943	.13742	.13542	.13344	.13147
1.5	.12952	.12758	.12566	.12376	.12188	.12001	.11816	.11632	.11450	.11270
1.6	.11092	.10915	.10741	.10567	.10396	.10226	.10059	.098925	.097282	.095657
1.7	.094049	.092459	.090887	.089333	.087796	.086277	.084776	.083293	.081828	.080380
1.8	.078950	.077538	.076143	.074766	.073407	.072065	.070740	.069433	.068144	.066871
1.9	.065616	.064378	.063157	.061952	.060765	.059595	.058441	.057304	.056183	.055079
2.0	.053991	.052919	.051864	.050824	.049800	.048792	.047800	.046823	.045861	.044915
2.1	.043984	.043067	.042166	.041280	.040408	.039550	.038707	.037878	.037063	.036262
2.2	.035475	.034701	.033941	.033194	.032460	.031740	.031032	.030337	.029655	.028985
2.3	.028327	.027682	.027048	.026426	.025817	.025218	.024631	.024056	.023491	.022937
2.4	.022395	.021862	.021341	.020829	.020328	.019837	.019356	.018885	.018423	.017971
2.5	.017528	.017095	.016670	.016254	.015848	.015449	.015060	.014678	.014305	.013940
2.6	.013583	.013234	.012892	.012558	.012232	.011912	.011600	.011295	.010997	.010706
2.7	.010421	.010143	$.0^298712$	$.0^296058$	$.0^293466$	$.0^290936$	$.0^288465$	$.0^286052$	$.0^283697$	$.0^281398$
2.8	$.0^279155$	$.0^276965$	$.0^274829$	$.0^272744$	$.0^270711$	$.0^268728$	$.0^266793$	$.0^264907$	$.0^263067$	$.0^261274$
2.9	$.0^259525$	$.0^257821$	$.0^256160$	$.0^254541$	$.0^252963$	$.0^251426$	$.0^249929$	$.0^248470$	$.0^247050$	$.0^245666$
3.0	$.0^244318$	$.0^243007$	$.0^241729$	$.0^240486$	$.0^239276$	$.0^238098$	$.0^236951$	$.0^235836$	$.0^234751$	$.0^233695$
3.1	$.0^232668$	$.0^231669$	$.0^230698$	$.0^229754$	$.0^228835$	$.0^227943$	$.0^227075$	$.0^226231$	$.0^225412$	$.0^224615$
3.2	$.0^223841$	$.0^223089$	$.0^222358$	$.0^221649$	$.0^220960$	$.0^220290$	$.0^219641$	$.0^219010$	$.0^218397$	$.0^217803$
3.3	$.0^217226$	$.0^216666$	$.0^216122$	$.0^215595$	$.0^215084$	$.0^214587$	$.0^214106$	$.0^213639$	$.0^213187$	$.0^212748$
3.4	$.0^212322$	$.0^211910$	$.0^211510$	$.0^211122$	$.0^210747$	$.0^210383$	$.0^210030$	$.0^396886$	$.0^393557$	$.0^390372$
3.5	$.0^387268$	$.0^384263$	$.0^381352$	$.0^378534$	$.0^375807$	$.0^373166$	$.0^370611$	$.0^368138$	$.0^365745$	$.0^363430$
3.6	$.0^361190$	$.0^359024$	$.0^356928$	$.0^354901$	$.0^352941$	$.0^351046$	$.0^349214$	$.0^347443$	$.0^345731$	$.0^344077$
3.7	$.0^342478$	$.0^340933$	$.0^339440$	$.0^337998$	$.0^336605$	$.0^335260$	$.0^333960$	$.0^332705$	$.0^331494$	$.0^330324$
3.8	$.0^329195$	$.0^328105$	$.0^327053$	$.0^326037$	$.0^325058$	$.0^324113$	$.0^323201$	$.0^322321$	$.0^321473$	$.0^320655$
3.9	$.0^319866$	$.0^319105$	$.0^318371$	$.0^317664$	$.0^316983$	$.0^316326$	$.0^315693$	$.0^315083$	$.0^314495$	$.0^313928$
4.0	$.0^313383$	$.0^312858$	$.0^312352$	$.0^311864$	$.0^311395$	$.0^310943$	$.0^310509$	$.0^310090$	$.0^496870$	$.0^492993$
4.1	$.0^489262$	$.0^485672$	$.0^482218$	$.0^478895$	$.0^475700$	$.0^472626$	$.0^469670$	$.0^466828$	$.0^464095$	$.0^461468$
4.2	$.0^458943$	$.0^456516$	$.0^454183$	$.0^451942$	$.0^449788$	$.0^447719$	$.0^445731$	$.0^443821$	$.0^441988$	$.0^440226$
4.3	$.0^438535$	$.0^436911$	$.0^435353$	$.0^433856$	$.0^432420$	$.0^431041$	$.0^429719$	$.0^428499$	$.0^427231$	$.0^426063$
4.4	$.0^424942$	$.0^423868$	$.0^422837$	$.0^421848$	$.0^420900$	$.0^419992$	$.0^419121$	$.0^418286$	$.0^417486$	$.0^416719$
4.5	$.0^415984$	$.0^415280$	$.0^414605$	$.0^413959$	$.0^413340$	$.0^412747$	$.0^412180$	$.0^411636$	$.0^411116$	$.0^410618$
4.6	$.0^410141$	$.0^596845$	$.0^592477$	$.0^588297$	$.0^584298$	$.0^580472$	$.0^576812$	$.0^573311$	$.0^569962$	$.0^566760$
4.7	$.0^563698$	$.0^560771$	$.0^557972$	$.0^555296$	$.0^552739$	$.0^550295$	$.0^547960$	$.0^545728$	$.0^543596$	$.0^541559$
4.8	$.0^539613$	$.0^537755$	$.0^535980$	$.0^534285$	$.0^532667$	$.0^531122$	$.0^529647$	$.0^528239$	$.0^526895$	$.0^525613$
4.9	$.0^524390$	$.0^523222$	$.0^522108$	$.0^521046$	$.0^520033$	$.0^519066$	$.0^518144$	$.0^517265$	$.0^516428$	$.0^515629$

Note: The left-hand and top values are used to identify the value of the deviation u. The table value listed at the intersection of these two values is the probability density ϕ (u) at this value of u.

Example: For u = 2.96, find the value located at the intersection of 2.9 on the left and .06 on the top. This value, $.0^249929$ (= 0.0049929) is the value of ϕ (u) for u = 2.96.

B.2 Upper Probability of Normal Distribution

$$\varepsilon(K\varepsilon) : \varepsilon = \int_{K\varepsilon}^{\infty} \phi(u)\, du$$



Kε	.00	.01	.02	.03	.04	.05	.06	.07	.08	.09
.0	.50000	.49601	.49202	.48803	.48405	.48006	.47608	.47210	.46812	.46414
.1	.46017	.45620	.45224	.44828	.44433	.44038	.43644	.43251	.42858	.42465
.2	.42074	.41683	.41294	.40905	.40517	.40129	.39743	.39358	.38974	.38591
.3	.38209	.37828	.37448	.37070	.36693	.36317	.35942	.35569	.35197	.34827
.4	.34458	.34090	.33724	.33360	.32997	.32636	.32276	.31918	.31561	.31207
.5	.30854	.30503	.30153	.29806	.29460	.29116	.28774	.28434	.28096	.27760
.6	.27425	.27093	.26763	.26435	.26109	.25785	.25463	.25143	.24825	.24510
.7	.24196	.23885	.23576	.23270	.22965	.22663	.22363	.22065	.21770	.21476
.8	.21186	.20897	.20611	.20327	.20045	.19766	.19489	.19215	.18943	.18673
.9	.18406	.18141	.17879	.17619	.17361	.17106	.16853	.16602	.16354	.16109
1.0	.15866	.15625	.15386	.15151	.14917	.14686	.14457	.14231	.14007	.13786
1.1	.13567	.13350	.13136	.12924	.12714	.12507	.12302	.12100	.11900	.11702
1.2	.11507	.11314	.11123	.10935	.10749	.10565	.10383	.10204	.10027	.098525
1.3	.096800	.095098	.093418	.091759	.090123	.088508	.086915	.085343	.083793	.082264
1.4	.080757	.079270	.077804	.076359	.074934	.073529	.072145	.070781	.069437	.068112
1.5	.066807	.065522	.064255	.063008	.061780	.060571	.059380	.058208	.057053	.055917
1.6	.054799	.053699	.052616	.051551	.050503	.049471	.048457	.047460	.046479	.045514
1.7	.044565	.043683	.042716	.041815	.040930	.040059	.039204	.038364	.037538	.036727
1.8	.035930	.035148	.034380	.033625	.032884	.032157	.031443	.030742	.030054	.029379
1.9	.028717	.028067	.027429	.026803	.026190	.025588	.024998	.024419	.023852	.023295
2.0	.022750	.022216	.021692	.021178	.020675	.020182	.019699	.019226	.018763	.018309
2.1	.017864	.017429	.017003	.016586	.016177	.015778	.015386	.015003	.014629	.014262
2.2	.013903	.013553	.013209	.012874	.012545	.012224	.011911	.011604	.011304	.011011
2.3	.010724	.010444	.010170	$.0^{2}99031$	$.0^{2}96419$	$.0^{2}93867$	$.0^{2}91375$	$.0^{2}88940$	$.0^{2}86563$	$.0^{2}84242$
2.4	$.0^{2}81975$	$.0^{2}79763$	$.0^{2}77603$	$.0^{2}75494$	$.0^{2}73436$	$.0^{2}71428$	$.0^{2}99469$	$.0^{2}67557$	$.0^{2}65691$	$.0^{2}63872$
2.5	$.0^{2}62097$	$.0^{2}60366$	$.0^{2}58677$	$.0^{2}57031$	$.0^{2}55426$	$.0^{2}53861$	$.0^{2}52336$	$.0^{2}50849$	$.0^{2}49400$	$.0^{2}47988$
2.6	$.0^{2}46612$	$.0^{2}45271$	$.0^{2}43965$	$.0^{2}42692$	$.0^{2}41453$	$.0^{2}40246$	$.0^{2}39070$	$.0^{2}37926$	$.0^{2}36811$	$.0^{2}35726$
2.7	$.0^{2}34670$	$.0^{2}33642$	$.0^{2}32641$	$.0^{2}31667$	$.0^{2}30720$	$.0^{2}29798$	$.0^{2}28901$	$.0^{2}28028$	$.0^{2}27179$	$.0^{2}26354$
2.8	$.0^{2}25551$	$.0^{2}24771$	$.0^{2}24012$	$.0^{2}23274$	$.0^{2}22557$	$.0^{2}21860$	$.0^{2}21182$	$.0^{2}20524$	$.0^{2}19884$	$.0^{2}19262$
2.9	$.0^{2}18658$	$.0^{2}18071$	$.0^{2}17502$	$.0^{2}16948$	$.0^{2}16411$	$.0^{2}15889$	$.0^{2}15382$	$.0^{2}14890$	$.0^{2}14412$	$.0^{2}13949$
3.0	$.0^{2}13499$	$.0^{2}13062$	$.0^{2}12639$	$.0^{2}12228$	$.0^{2}11829$	$.0^{2}11442$	$.0^{2}11067$	$.0^{2}10703$	$.0^{2}10350$	$.0^{2}10008$
3.1	$.0^{3}96760$	$.0^{3}93544$	$.0^{3}90426$	$.0^{3}87403$	$.0^{3}84474$	$.0^{3}81635$	$.0^{3}78885$	$.0^{3}76219$	$.0^{3}73638$	$.0^{3}71136$
3.2	$.0^{3}68714$	$.0^{3}66367$	$.0^{3}64095$	$.0^{3}61895$	$.0^{3}59765$	$.0^{3}57703$	$.0^{3}55706$	$.0^{3}53774$	$.0^{3}51904$	$.0^{3}50094$
3.3	$.0^{3}48342$	$.0^{3}46648$	$.0^{3}45009$	$.0^{3}43423$	$.0^{3}41889$	$.0^{3}40406$	$.0^{3}38971$	$.0^{3}37584$	$.0^{3}36243$	$.0^{3}34946$
3.4	$.0^{3}33693$	$.0^{3}32481$	$.0^{3}31311$	$.0^{3}30179$	$.0^{3}29086$	$.0^{3}28029$	$.0^{3}27009$	$.0^{3}26023$	$.0^{3}25071$	$.0^{3}24151$
3.5	$.0^{3}23263$	$.0^{3}22405$	$.0^{3}21577$	$.0^{3}20778$	$.0^{3}20006$	$.0^{3}19262$	$.0^{3}18543$	$.0^{3}17849$	$.0^{3}17180$	$.0^{3}16534$
3.6	$.0^{3}15911$	$.0^{3}15310$	$.0^{3}14730$	$.0^{3}14171$	$.0^{3}13632$	$.0^{3}13112$	$.0^{3}12611$	$.0^{3}12128$	$.0^{3}11662$	$.0^{3}11213$
3.7	$.0^{3}10780$	$.0^{3}10363$	$.0^{4}99611$	$.0^{4}95740$	$.0^{4}92010$	$.0^{4}88417$	$.0^{4}84957$	$.0^{4}81624$	$.0^{4}78414$	$.0^{4}75324$
3.8	$.0^{4}72348$	$.0^{4}69483$	$.0^{4}66726$	$.0^{4}64072$	$.0^{4}61517$	$.0^{4}59059$	$.0^{4}56694$	$.0^{4}54418$	$.0^{4}52228$	$.0^{4}50122$
3.9	$.0^{4}48096$	$.0^{4}46148$	$.0^{4}44274$	$.0^{4}42473$	$.0^{4}40741$	$.0^{4}39076$	$.0^{4}37475$	$.0^{4}35936$	$.0^{4}34458$	$.0^{4}33037$
4.0	$.0^{4}31671$	$.0^{4}30359$	$.0^{4}29099$	$.0^{4}27888$	$.0^{4}26726$	$.0^{4}25609$	$.0^{4}24536$	$.0^{4}23507$	$.0^{4}22518$	$.0^{4}21569$
4.1	$.0^{4}20658$	$.0^{4}19783$	$.0^{4}18944$	$.0^{4}18138$	$.0^{4}17365$	$.0^{4}16624$	$.0^{4}15912$	$.0^{4}15230$	$.0^{4}14575$	$.0^{4}13948$
4.2	$.0^{4}13346$	$.0^{4}12769$	$.0^{4}12215$	$.0^{4}11685$	$.0^{4}11176$	$.0^{4}10689$	$.0^{4}10221$	$.0^{5}97736$	$.0^{5}93447$	$.0^{5}89337$
4.3	$.0^{5}85399$	$.0^{5}81627$	$.0^{5}78015$	$.0^{5}74555$	$.0^{5}71241$	$.0^{5}68069$	$.0^{5}65031$	$.0^{5}62123$	$.0^{5}59340$	$.0^{5}56675$
4.4	$.0^{5}54125$	$.0^{5}51685$	$.0^{5}49350$	$.0^{5}47117$	$.0^{5}44979$	$.0^{5}42935$	$.0^{5}40980$	$.0^{5}39110$	$.0^{5}37322$	$.0^{5}35612$
4.5	$.0^{5}33977$	$.0^{5}32414$	$.0^{5}30920$	$.0^{5}29492$	$.0^{5}28127$	$.0^{5}26823$	$.0^{5}25577$	$.0^{5}24386$	$.0^{5}23249$	$.0^{5}22162$
4.6	$.0^{5}21125$	$.0^{5}20133$	$.0^{5}19187$	$.0^{5}18283$	$.0^{5}17420$	$.0^{5}16597$	$.0^{5}15810$	$.0^{5}15060$	$.0^{5}14344$	$.0^{5}13660$
4.7	$.0^{5}13008$	$.0^{5}12386$	$.0^{5}11792$	$.0^{5}11226$	$.0^{5}10686$	$.0^{5}10171$	$.0^{6}96796$	$.0^{6}92113$	$.0^{6}87648$	$.0^{6}83391$
4.8	$.0^{6}79333$	$.0^{6}75465$	$.0^{6}71779$	$.0^{6}68267$	$.0^{6}64920$	$.0^{6}61731$	$.0^{6}58693$	$.0^{6}55799$	$.0^{6}53043$	$.0^{6}50418$
4.9	$.0^{6}47918$	$.0^{6}45538$	$.0^{6}43272$	$.0^{6}41115$	$.0^{6}39061$	$.0^{6}37107$	$.0^{6}35247$	$.0^{6}33476$	$.0^{6}31792$	$.0^{6}30190$

Note: The above table gives the upper probability for a normal distribution for the values of Kε = 0.00 to 4.99.

Example: For Kε = 3.18, find the value located at the intersection of 3.1 on the left and .08 on the top.

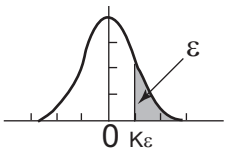
The value ε = $.0^{3}73638$ = 0.00073638 is the value of the upper probability for Kε = 3.18.

Similarly, for Kε = 1.96, ε = .024998, and for Kε = 2.58, ε = $.0^{2}49400$ = 0.0049400.

If two-sided probability of distribution is considered, then the above values, respectively, correspond to 2.ε = 0.049996 ≥ 0.05 and 0.00988 ≈ 0.01.

B.3 Percent Points of Normal Distribution

$$K\varepsilon(\varepsilon): \varepsilon = \int_{K\varepsilon}^{\infty} \phi(u)\, du$$



ε	.000	.001	.002	.003	.004	.005	.006	.007	.008	.009
.00	∞	3.09023	2.87816	2.74778	2.65207	2.57583	2.51214	2.45726	2.40892	2.36562
.01	2.32635	2.29037	2.25713	2.22621	2.19729	2.17009	2.14441	2.12007	2.09693	2.07485
.02	2.05375	2.03352	2.01409	1.99539	1.97737	1.95996	1.94313	1.92684	1.91104	1.89570
.03	1.88079	1.86630	1.85218	1.83842	1.82501	1.81191	1.79912	1.78661	1.77438	1.76241
.04	1.75069	1.73920	1.72793	1.71689	1.70604	1.69540	1.68494	1.67466	1.66456	1.65463
.05	1.64485	1.63523	1.62576	1.61644	1.60725	1.59819	1.58927	1.58047	1.57179	1.56322
.06	1.55477	1.54643	1.53820	1.53007	1.52204	1.51410	1.50626	1.49851	1.49085	1.48328
.07	1.47579	1.46838	1.46106	1.45381	1.44663	1.43953	1.43250	1.42554	1.41865	1.41183
.08	1.40507	1.39838	1.39174	1.38517	1.37866	1.37220	1.36581	1.35946	1.35317	1.34694
.09	1.34076	1.33462	1.32854	1.32251	1.31652	1.31058	1.30469	1.29884	1.29303	1.28727
.10	1.28155	1.27587	1.27024	1.26464	1.25908	1.25357	1.24808	1.24264	1.23723	1.23186
.11	1.22653	1.22123	1.21596	1.21073	1.20553	1.20036	1.19522	1.19012	1.18504	1.18000
.12	1.17499	1.17000	1.16505	1.16012	1.15522	1.15035	1.14551	1.14069	1.13590	1.13113
.13	1.12639	1.12168	1.11699	1.11232	1.10768	1.10306	1.09847	1.09390	1.08935	1.08482
.14	1.08032	1.07584	1.07138	1.06694	1.06252	1.05812	1.05374	1.04939	1.04505	1.04073
.15	1.03643	1.03215	1.02789	1.02365	1.01943	1.01522	1.01103	1.00686	1.00271	.99858
.16	.99446	.99036	.98627	.98220	.97815	.97411	.97009	.96609	.96210	.95812
.17	.95417	.95022	.94629	.94238	.93848	.93459	.93072	.92686	.92301	.91918
.18	.91537	.91156	.90777	.90399	.90023	.89647	.89273	.88901	.88529	.83159
.19	.87790	.87422	.87055	.86689	.86325	.85962	.85600	.85239	.84879	.84520
.20	.84162	.83805	.83450	.83095	.82742	.82389	.82038	.81687	.81338	.80990
.21	.80642	.80296	.79950	.79606	.79262	.78919	.78577	.78237	.77897	.77557
.22	.77219	.76882	.76546	.76210	.75875	.75542	.75208	.74876	.74545	.74214
.23	.73885	.73556	.73228	.72900	.72574	.72248	.71923	.71599	.71275	.70952
.24	.70630	.70309	.69988	.69668	.69349	.69031	.68713	.68396	.68080	.67764
.25	.67449	.67135	.66821	.66508	.66196	.65884	.65573	.65262	.64952	.64643
.26	.64335	.64027	.63719	.63412	.63106	.62801	.62496	.62191	.61887	.61584
.27	.61281	.60979	.60678	.60376	.60076	.59776	.59477	.59178	.58879	.58581
.28	.58284	.57987	.57691	.57395	.57100	.56805	.56511	.56217	.55924	.55631
.29	.55338	.55047	.54755	.54464	.54174	.53884	.53594	.53305	.53016	.52728
.30	.52440	.52153	.51866	.51579	.51293	.51007	.50722	.50437	.50153	.49869
.31	.49585	.49032	.49019	.48736	.48454	.48173	.47891	.47610	.47330	.47050
.32	.46770	.46490	.46211	.45933	.45654	.45376	.45099	.44821	.44544	.44268
.33	.43991	.43715	.43440	.43164	.42889	.42615	.42340	.42066	.41793	.41519
.34	.41246	.40974	.40701	.40429	.40157	.39886	.39614	.39343	.39073	.38802
.35	.38532	.38262	.37993	.37723	.37454	.37186	.36917	.36649	.36381	.36113
.36	.35846	.35579	.35312	.35045	.34779	.34513	.34247	.33981	.33716	.33450
.37	.33185	.32921	.32656	.32392	.32128	.31864	.31600	.31337	.31074	.30811
.38	.30548	.30286	.30023	.29761	.29499	.29237	.28976	.28715	.28454	.28193
.39	.27932	.27671	.27411	.27151	.26891	.26631	.26371	.26112	.25853	.25594
.40	.25335	.25076	.24817	.24559	.24301	.24043	.23785	.23527	.23269	.23012
.41	.22754	.22497	.22240	.21983	.21727	.21470	.21214	.20957	.20701	.20445
.42	.28189	.19934	.19678	.19422	.19167	.18912	.18657	.18402	.18147	.17892
.43	.17637	.17383	.17128	.16874	.16620	.16366	.16112	.15858	.15604	.15351
.44	.15097	.14843	.14590	.14337	.14084	.13830	.13577	.13324	.13072	.12819
.45	.12566	.12314	.12061	.11809	.11556	.11304	.11052	.10799	.10547	.10295
.46	.10043	.09791	.09540	.09288	.09036	.08784	.08533	.08281	.08030	.07778
.47	.07527	.07276	.07024	.06773	.06522	.06271	.06020	.05768	.05517	.05766
.48	.05015	.04764	.04513	.04263	.04012	.03761	.03510	.03259	.03008	.02758
.49	.02507	.02256	.02005	.01755	.01504	.01253	.01003	.00752	.00501	.00251

Note: The above table gives the value of Kε for the upper probability of normal distribution ε = 0.000 to 0.499.
The Kε value is known as 100 ε percent point.

Example: For ε = 0.200 we find the value at the intersection of .20 on the left side and the .000 on the top.
The value is Kε = .84162. This is referred to as (upper) 20 percent point.
The 2.5% point is represented by the value of ε = 0.025 for which Kε = 1.95996 ≈ 1.96 and the 0.5% point by the value of ε = 0.005, for which Kε = 2.57583 ≈ 2.58.

B.4 Poisson Distribution (Probability)

x	m									
	0.1	0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.9	1.0
0	.9048	.8187	.7408	.6703	.6065	.5488	.4966	.4493	.4066	.3679
1	.0905	.1637	.2222	.2681	.3033	.3293	.3476	.3595	.3659	.3679
2	.0045	.0164	.0333	.0536	.0758	.0988	.1217	.1438	.1647	.1839
3	.0002	.0010	.0033	.0072	.0126	.0198	.0284	.0383	.0494	.0613
4	.0000	.0001	.0002	.0007	.0016	.0030	.0050	.0077	.0111	.0153
5	.0000	.0000	.0000	.0001	.0002	.0004	.0007	.0012	.0020	.0031
6	.0000	.0000	.0000	.0000	.0000	.0000	.0001	.0002	.0003	.0005
7	.0000	.0000	.0000	.0000	.0000	.0000	.0000	.0000	.0000	.0001

x	m									
	1.1	1.2	1.3	1.4	1.5	1.6	1.7	1.8	1.9	2.0
0	.3329	.3012	.2725	.2466	.2231	.2019	.1827	.1653	.1496	.1353
1	.3662	.3614	.3543	.3452	.3347	.3230	.3106	.2975	.2842	.2707
2	.2014	.2169	.2303	.2417	.2510	.2584	.2640	.2678	.2700	.2707
3	.0738	.0867	.0998	.1128	.1255	.1378	.1496	.1607	.1710	.1804
4	.0203	.0260	.0324	.0395	.0471	.0551	.0636	.0723	.0812	.0902
5	.0045	.0062	.0084	.0111	.0141	.0176	.0216	.0260	.0309	.0361
6	.0008	.0012	.0018	.0026	.0035	.0047	.0061	.0078	.0098	.0120
7	.0001	.0002	.0003	.0005	.0008	.0011	.0015	.0020	.0027	.0034
8	.0000	.0000	.0001	.0001	.0001	.0002	.0003	.0005	.0006	.0009
9	.0000	.0000	.0000	.0000	.0000	.0000	.0001	.0001	.0001	.0002

x	m									
	2.1	2.2	2.3	2.4	2.5	2.6	2.7	2.8	2.9	3.0
0	.1225	.1108	.1003	.0907	.0821	.0743	.0672	.0608	.0550	.0498
1	.2572	.2438	.2306	.2177	.2052	.1931	.1815	.1703	.1596	.1494
2	.2700	.2681	.2652	.2613	.2565	.2510	.2450	.2384	.2314	.2240
3	.1890	.1966	.2033	.2090	.2138	.2176	.2205	.2225	.2237	.2240
4	.0992	.1082	.1169	.1254	.1336	.1414	.1488	.1557	.1622	.1680
5	.0417	.0476	.0538	.0602	.0668	.0735	.0804	.0872	.0940	.1008
6	.0146	.0174	.0206	.0241	.0278	.0319	.0362	.0407	.0455	.0504
7	.0044	.0055	.0068	.0083	.0099	.0118	.0139	.0163	.0188	.0216
8	.0011	.0015	.0019	.0025	.0031	.0038	.0047	.0057	.0068	.0081
9	.0003	.0004	.0005	.0007	.0009	.0011	.0014	.0018	.0022	.0027
10	.0001	.0001	.0001	.0002	.0002	.0003	.0004	.0005	.0006	.0008
11	.0000	.0000	.0000	.0000	.0000	.0001	.0001	.0001	.0002	.0002
12	.0000	.0000	.0000	.0000	.0000	.0000	.0000	.0000	.0000	.0001

x	m									
	3.1	3.2	3.3	3.4	3.5	3.6	3.7	3.8	3.9	4.0
0	.0450	.0408	.0369	.0334	.0302	.0273	.0247	.0224	.0202	.0183
1	.1397	.1304	.1217	.1135	.1057	.0984	.0915	.0850	.0789	.0733
2	.2165	.2087	.2008	.1929	.1850	.0771	.1692	.1615	.1539	.1465
3	.2237	.2226	.2209	.2186	.2158	.2125	.2087	.2046	.2001	.1954
4	.1734	.1781	.1823	.1858	.1888	.1912	.1931	.1944	.1951	.1954
5	.1075	.1140	.1203	.1264	.1322	.1377	.1429	.1477	.1522	.1563
6	.0555	.0608	.0662	.0716	.0711	.0826	.0881	.0936	.0989	.1042
7	.0246	.0278	.0312	.0348	.0385	.0425	.0466	.0508	.0551	.0595
8	.0095	.0111	.0129	.0148	.0169	.0191	.0215	.0241	.0269	.0298
9	.0033	.0040	.0047	.0056	.0066	.0076	.0089	.0102	.0116	.0132
10	.0010	.0013	.0016	.0019	.0023	.0028	.0033	.0039	.0045	.0053
11	.0003	.0004	.0005	.0006	.0007	.0009	.0011	.0013	.0016	.0019
12	.0001	.0001	.0001	.0002	.0002	.0003	.0003	.0004	.0005	.0006
13	.0000	.0000	.0000	.0000	.0001	.0001	.0001	.0001	.0002	.0002
14	.0000	.0000	.0000	.0000	.0000	.0000	.0000	.0000	.0000	.0001

x: number of failures detected (percent defective)

m: number of expected failures (number of defective items)

x	m									
	4.1	4.2	4.3	4.4	4.5	4.6	4.7	4.8	4.9	5.0
0	.0166	.0150	.0136	.0123	.0111	.0101	.0091	.0082	.0074	.0067
1	.0679	.0630	.0583	.0540	.0500	.0462	.0427	.0395	.0365	.0337
2	.1393	.1323	.1254	.1188	.1125	.1063	.1005	.0948	.0894	.0842
3	.1904	.1852	.1798	.1743	.1687	.1631	.1574	.1517	.1460	.1404
4	.1951	.1944	.1933	.1917	.1898	.1875	.1849	.1820	.1789	.1755
5	.1600	.1633	.1662	.1687	.1708	.1725	.1738	.1747	.1753	.1755
6	.1093	.1143	.1191	.1237	.1281	.1323	.1362	.1398	.1432	.1462
7	.0640	.0686	.0732	.0778	.0824	.0869	.0914	.0959	.1002	.1044
8	.0328	.0360	.0393	.0428	.0463	.0500	.0537	.0575	.0614	.0653
9	.0150	.0168	.0188	.0209	.0232	.0255	.0280	.0307	.0334	.0363
10	.0061	.0071	.0081	.0092	.0104	.0118	.0132	.0147	.0164	.0181
11	.0023	.0027	.0032	.0037	.0043	.0049	.0056	.0064	.0073	.0082
12	.0008	.0009	.0011	.0014	.0016	.0019	.0022	.0026	.0030	.0034
13	.0002	.0003	.0004	.0005	.0006	.0007	.0008	.0009	.0011	.0013
14	.0001	.0001	.0001	.0001	.0002	.0002	.0003	.0003	.0004	.0005
15	.0000	.0000	.0000	.0000	.0001	.0001	.0001	.0001	.0001	.0002

x	m									
	5.1	5.2	5.3	5.4	5.5	5.6	5.7	5.8	5.9	6.0
0	.0061	.0055	.0050	.0045	.0041	.0037	.0033	.0030	.0027	.0025
1	.0311	.0287	.0265	.0244	.0225	.0207	.0191	.0176	.0162	.0149
2	.0793	.0746	.0701	.0659	.0618	.0580	.0544	.0509	.0477	.0446
3	.1348	.1293	.1239	.1185	.1133	.1082	.1033	.0985	.0938	.0892
4	.1719	.1681	.1641	.1600	.1558	.1515	.1472	.1428	.1383	.1339
5	.1753	.1748	.1740	.1728	.1714	.1697	.1678	.1656	.1632	.1606
6	.1490	.1515	.1537	.1555	.1571	.1584	.1594	.1601	.1605	.1606
7	.1086	.1125	.1163	.1200	.1234	.1267	.1298	.1326	.1353	.1377
8	.0692	.0731	.0771	.0810	.0849	.0887	.0925	.0962	.0998	.1033
9	.0392	.0423	.0454	.0486	.0519	.0552	.0586	.0620	.0654	.0688
10	.0200	.0220	.0241	.0262	.0285	.0309	.0334	.0359	.0386	.0413
11	.0093	.0104	.0116	.0129	.0143	.0157	.0173	.0190	.0207	.0225
12	.0039	.0045	.0051	.0058	.0065	.0073	.0082	.0092	.0102	.0113
13	.0015	.0018	.0021	.0024	.0028	.0032	.0036	.0041	.0046	.0052
14	.0006	.0007	.0008	.0009	.0011	.0013	.0015	.0017	.0019	.0022
15	.0002	.0002	.0003	.0003	.0004	.0005	.0006	.0007	.0008	.0009
16	.0001	.0001	.0001	.0001	.0001	.0002	.0002	.0002	.0003	.0003
17	.0001	.0000	.0000	.0000	.0000	.0001	.0001	.0001	.0001	.0001

x	m									
	6.1	6.2	6.3	6.4	6.5	6.6	6.7	6.8	6.9	7.0
0	.0022	.0020	.0018	.0017	.0015	.0014	.0012	.0011	.0010	.0009
1	.0137	.0126	.0116	.0106	.0098	.0090	.0082	.0076	.0070	.0064
2	.0417	.0390	.0364	.0340	.0318	.0296	.0276	.0258	.0240	.0223
3	.0848	.0806	.0765	.0726	.0688	.0652	.0617	.0584	.0552	.0521
4	.1294	.1249	.1205	.1162	.1118	.1076	.1034	.0992	.0952	.0912
5	.1579	.1549	.1519	.1487	.1454	.1420	.1385	.1349	.1314	.1277
6	.1605	.1601	.1595	.1586	.1575	.1562	.1546	.1529	.1511	.1490
7	.1399	.1418	.1435	.1450	.1462	.1472	.1480	.1486	.1489	.1490
8	.1066	.1099	.1130	.1160	.1188	.1215	.1240	.1263	.1284	.1304
9	.0723	.0757	.0791	.0825	.0858	.0891	.0923	.0954	.0985	.1014
10	.0441	.0469	.0498	.0528	.0558	.0588	.0618	.0649	.0679	.0710
11	.0245	.0265	.0285	.0307	.0330	.0353	.0377	.0401	.0426	.0452
12	.0124	.0137	.0150	.0164	.0179	.0194	.0210	.0227	.0246	.0264
13	.0058	.0065	.0073	.0081	.0089	.0098	.0108	.0119	.0130	.0142
14	.0025	.0029	.0033	.0037	.0041	.0046	.0052	.0058	.0064	.0071
15	.0010	.0012	.0014	.0016	.0018	.0020	.0023	.0026	.0029	.0033
16	.0004	.0005	.0005	.0006	.0007	.0008	.0010	.0011	.0013	.0014
17	.0001	.0002	.0002	.0002	.0003	.0003	.0004	.0004	.0005	.0006
18	.0000	.0001	.0001	.0001	.0001	.0001	.0001	.0002	.0002	.0002
19	.0000	.0000	.0000	.0000	.0000	.0000	.0000	.0001	.0001	.0001

x	m									
	7.1	7.2	7.3	7.4	7.5	7.6	7.7	7.8	7.9	8.0
0	.0008	.0007	.0007	.0006	.0006	.0005	.0005	.0004	.0004	.0003
1	.0059	.0054	.0049	.0045	.0041	.0038	.0035	.0032	.0029	.0027
2	.0208	.0194	.0180	.0167	.0156	.0145	.0134	.0125	.0116	.0107
3	.0492	.0464	.0438	.0413	.0389	.0366	.0345	.0324	.0305	.0286
4	.0874	.0836	.0799	.0764	.0729	.0696	.0663	.0632	.0602	.0573
5	.1241	.1204	.1167	.1130	.1094	.1057	.1021	.0986	.0951	.0916
6	.1468	.1445	.1420	.1394	.1367	.1339	.1311	.1282	.1252	.1221
7	.1489	.1486	.1481	.1474	.1465	.1454	.1442	.1428	.1413	.1396
8	.1321	.1337	.1351	.1363	.1373	.1382	.1388	.1392	.1395	.1396
9	.1042	.1070	.1096	.1121	.1144	.1167	.1187	.1207	.1224	.1241
10	.0740	.0770	.0800	.0829	.0858	.0887	.0914	.0941	.0967	.0993
11	.0478	.0504	.0531	.0558	.0585	.0613	.0640	.0667	.0695	.0722
12	.0283	.0303	.0323	.0344	.0366	.0388	.0411	.0434	.0457	.0481
13	.0154	.0168	.0181	.0196	.0211	.0227	.0243	.0260	.0278	.0296
14	.0078	.0086	.0095	.0104	.0113	.0123	.0134	.0145	.0157	.0169
15	.0037	.0041	.0046	.0051	.0057	.0062	.0069	.0075	.0083	.0090
16	.0016	.0019	.0021	.0024	.0026	.0030	.0033	.0037	.0041	.0045
17	.0007	.0008	.0009	.0010	.0012	.0013	.0015	.0017	.0019	.0021
18	.0003	.0003	.0004	.0004	.0005	.0006	.0006	.0007	.0008	.0009
19	.0001	.0001	.0001	.0002	.0002	.0002	.0003	.0003	.0003	.0004
20	.0000	.0000	.0001	.0001	.0001	.0001	.0001	.0001	.0001	.0002
21	.0000	.0000	.0000	.0000	.0000	.0000	.0000	.0000	.0001	.0001

x	m									
	8.1	8.2	8.3	8.4	8.5	8.6	8.7	8.8	8.9	9.0
0	.0003	.0003	.0002	.0002	.0002	.0002	.0002	.0002	.0001	.0001
1	.0025	.0023	.0021	.0019	.0017	.0016	.0014	.0013	.0012	.0011
2	.0100	.0092	.0086	.0079	.0074	.0068	.0063	.0058	.0054	.0050
3	.0269	.0252	.0237	.0222	.0208	.0195	.0183	.0171	.0160	.0150
4	.0544	.0517	.0491	.0466	.0443	.0420	.0398	.0377	.0357	.0337
5	.0882	.0849	.0816	.0784	.0752	.0722	.0692	.0663	.0635	.0607
6	.1191	.1160	.1128	.1097	.1066	.1034	.1003	.0972	.0941	.0911
7	.1378	.1358	.1338	.1317	.1294	.1271	.1247	.1222	.1197	.1171
8	.1395	.1392	.1388	.1382	.1375	.1366	.1356	.1344	.1332	.1318
9	.1256	.1269	.1280	.1290	.1299	.1306	.1311	.1315	.1317	.1318
10	.1017	.1040	.0163	.1084	.1104	.1123	.1140	.1157	.1172	.1186
11	.0749	.0776	.0802	.0828	.0853	.0878	.0902	.0925	.0948	.0970
12	.0505	.0530	.0555	.0579	.0604	.0629	.0654	.0679	.0703	.0728
13	.0315	.0334	.0354	.0374	.0395	.0416	.0438	.0459	.0481	.0504
14	.0182	.0196	.0210	.0225	.0240	.0256	.0272	.0289	.0306	.0324
15	.0098	.0107	.0116	.0126	.0136	.0147	.0158	.0169	.0182	.0194
16	.0050	.0055	.0060	.0066	.0072	.0079	.0086	.0093	.0101	.0109
17	.0024	.0026	.0029	.0033	.0036	.0040	.0044	.0048	.0053	.0058
18	.0011	.0012	.0014	.0015	.0017	.0019	.0021	.0024	.0026	.0029
19	.0005	.0005	.0006	.0007	.0008	.0009	.0010	.0011	.0012	.0014
20	.0002	.0002	.0002	.0003	.0003	.0004	.0004	.0005	.0005	.0006
21	.0001	.0001	.0001	.0001	.0001	.0002	.0002	.0002	.0002	.0003
22	.0000	.0000	.0000	.0000	.0001	.0001	.0001	.0001	.0001	.0001

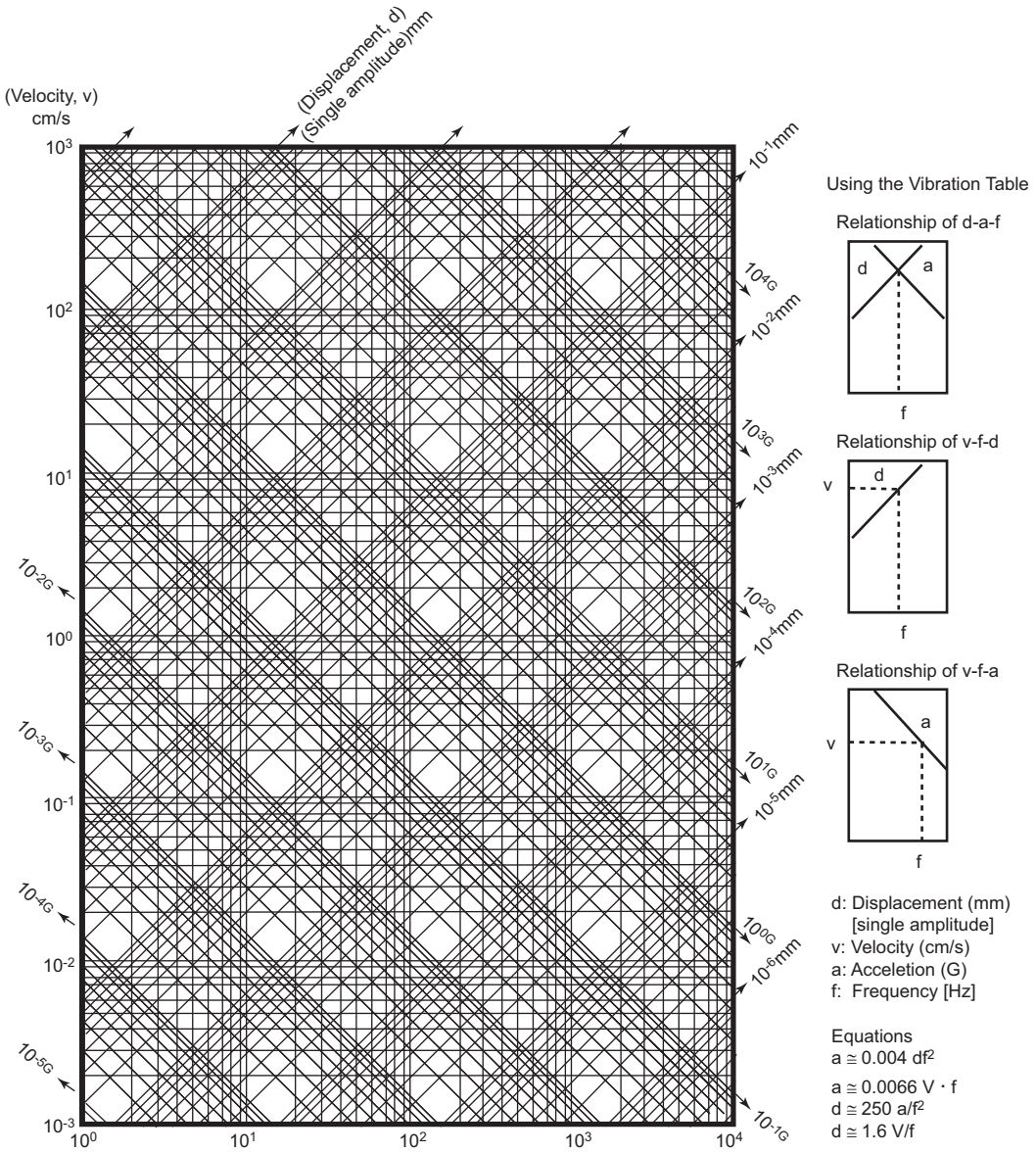
x	m									
	9.1	9.2	9.3	9.4	9.5	9.6	9.7	9.8	9.9	10
0	.0001	.0001	.0001	.0001	.0001	.0001	.0001	.0001	.0001	.0000
1	.0010	.0009	.0009	.0008	.0007	.0007	.0006	.0005	.0005	.0005
2	.0046	.0043	.0040	.0037	.0034	.0031	.0029	.0027	.0025	.0023
3	.0140	.0131	.0123	.0115	.0107	.0100	.0093	.0087	.0081	.0076
4	.0319	.0302	.0285	.0269	.0254	.0240	.0226	.0213	.0201	.0189
5	.0581	.0005	.0530	.0506	.0483	.0460	.0439	.0418	.0398	.0378
6	.0881	.0851	.0822	.0793	.0764	.0736	.0709	.0682	.0656	.0631
7	.1145	.1118	.1091	.1064	.1037	.1010	.0982	.0955	.0928	.0901
8	.1302	.1286	.1269	.1251	.1232	.1212	.1191	.1170	.1148	.1126
9	.1317	.1315	.1311	.1306	.1300	.1293	.1284	.1274	.1263	.1251

x	m									
	9.1	9.2	9.3	9.4	9.5	9.6	9.7	9.8	9.9	10
10	.1198	.1210	.1219	.1228	.1235	.1241	.1245	.1249	.1250	.1251
11	.0991	.1012	.1031	.1049	.1067	.1083	.1098	.1112	.1125	.1137
12	.0752	.0776	.0799	.0822	.0844	.0866	.0888	.0908	.0928	.0948
13	.0526	.0549	.0572	.0594	.0617	.0640	.0662	.0685	.0707	.0729
14	.0342	.0361	.0380	.0399	.0419	.0439	.0459	.0479	.0500	.0521
15	.0208	.0221	.0235	.0250	.0265	.0281	.0297	.0313	.0330	.0347
16	.0118	.0127	.0137	.0147	.0157	.0168	.0180	.0192	.0204	.0217
17	.0063	.0069	.0075	.0081	.0088	.0095	.0103	.0111	.0119	.0128
18	.0032	.0035	.0039	.0042	.0046	.0051	.0055	.0060	.0065	.0071
19	.0015	.0017	.0019	.0021	.0023	.0026	.0028	.0031	.0034	.0037
20	.0007	.0008	.0009	.0010	.0011	.0012	.0014	.0051	.0017	.0019
21	.0003	.0003	.0004	.0004	.0005	.0006	.0006	.0007	.0008	.0009
22	.0001	.0001	.0002	.0002	.0002	.0002	.0003	.0003	.0004	.0004
23	.0000	.0001	.0001	.0001	.0001	.0001	.0001	.0001	.0002	.0002
24	.0000	.0000	.0000	.0000	.0000	.0000	.0000	.0001	.0001	.0001

x	m									
	11	12	13	14	15	16	17	18	19	20
0	.0000	.0000	.0000	.0000	.0000	.0000	.0000	.0000	.0000	.0000
1	.0002	.0001	.0000	.0000	.0000	.0000	.0000	.0000	.0000	.0000
2	.0010	.0004	.0002	.0001	.0000	.0000	.0000	.0000	.0000	.0000
3	.0037	.0018	.0008	.0004	.0002	.0001	.0000	.0000	.0000	.0000
4	.0102	.0053	.0027	.0013	.0006	.0003	.0001	.0001	.0000	.0000
5	.0224	.0127	.0070	.0037	.0019	.0010	.0005	.0002	.0001	.0001
6	.0411	.0255	.0152	.0087	.0048	.0026	.0014	.0007	.0004	.0002
7	.0646	.0437	.0281	.0174	.0104	.0060	.0034	.0018	.0010	.0005
8	.0888	.0655	.0457	.0304	.0194	.0120	.0072	.0042	.0024	.0013
9	.1085	.0874	.0661	.0473	.0324	.0213	.0135	.0083	.0050	.0029
10	.1194	.1048	.0859	.0663	.0486	.0341	.0230	.0150	.0095	.0058
11	.1194	.1144	.1015	.0884	.0663	.0496	.0355	.0245	.0164	.0106
12	.1094	.1144	.1099	.0984	.0829	.0661	.0504	.0368	.0259	.0176
13	.0926	.1056	.1099	.1060	.0956	.0814	.0658	.0509	.0378	.0271
14	.0728	.0905	.1021	.1060	.1024	.0930	.0800	.0655	.0514	.0387
15	.0534	.0724	.0885	.0989	.1024	.0992	.0906	.0786	.0650	.0516
16	.0367	.0543	.0719	.0866	.0960	.0992	.0963	.0884	.0772	.0646
17	.0237	.0383	.0550	.0713	.0847	.0934	.0963	.0936	.0863	.0760
18	.0145	.0256	.0397	.0554	.0706	.0830	.0909	.0936	.0911	.0844
19	.0084	.0161	.0272	.0409	.0557	.0699	.0814	.0887	.0911	.0888
20	.0046	.0097	.0177	.0286	.0418	.0559	.0692	.0798	.0866	.0888
21	.0024	.0055	.0109	.0191	.0299	.0426	.0560	.0684	.0783	.0846
22	.0012	.0030	.0065	.0121	.0204	.0310	.0433	.0560	.0676	.0769
23	.0006	.0016	.0037	.0074	.0133	.0216	.0320	.0438	.0559	.0669
24	.0003	.0008	.0020	.0043	.0083	.0144	.0226	.0328	.0442	.0557
25	.0001	.0004	.0010	.0024	.0050	.0092	.0154	.0237	.0336	.0446
26	.0000	.0002	.0005	.0013	.0029	.0057	.0101	.0164	.0246	.0343
27	.0000	.0001	.0002	.0007	.0016	.0034	.0063	.0109	.0173	.0254
28	.0000	.0000	.0001	.0003	.0009	.0019	.0038	.0070	.0117	.0181
29	.0000	.0000	.0001	.0002	.0004	.0011	.0023	.0044	.0077	.0125
30	.0000	.0000	.0000	.0001	.0002	.0006	.0013	.0026	.0049	.0083
31	.0000	.0000	.0000	.0000	.0001	.0003	.0007	.0015	.0030	.0054
32	.0000	.0000	.0000	.0000	.0001	.0001	.0004	.0009	.0018	.0034
33	.0000	.0000	.0000	.0000	.0000	.0001	.0002	.0005	.0010	.0020
34	.0000	.0000	.0000	.0000	.0000	.0000	.0001	.0002	.0006	.0012
35	.0000	.0000	.0000	.0000	.0000	.0000	.0000	.0001	.0003	.0007
36	.0000	.0000	.0000	.0000	.0000	.0000	.0000	.0001	.0002	.0004
37	.0000	.0000	.0000	.0000	.0000	.0000	.0000	.0000	.0001	.0002
38	.0000	.0000	.0000	.0000	.0000	.0000	.0000	.0000	.0000	.0001
39	.0000	.0000	.0000	.0000	.0000	.0000	.0000	.0000	.0000	.0001

B.5 Vibration Tables (Amplitude, Velocity, and Acceleration vs. Frequency)

The relationship between amplitude, velocity, and acceleration vs. frequency is shown blow.



B.6 Water Vapor Pressure Tables

Saturated Water Vapor Table (By Temperature)

Temperature °C t	Saturation Pressure kg/cm² P_S	Temperature °C t	Saturation Pressure kg/cm² P_S
0	0.006228	125	2.3666
5	0.008891	130	2.7544
10	0.012513	135	3.1923
15	0.017378	140	3.6848
20	0.023830	145	4.2369
25	0.032291	150	4.8535
30	0.043261	155	5.5401
35	0.057387	160	6.3021
40	0.075220	165	7.1454
45	0.097729	170	8.0759
50	0.12581	175	9.1000
55	0.16054	180	10.224
60	0.20316	185	11.455
65	0.25506	190	12.799
70	0.31780	195	14.263
75	0.39313	200	15.856
80	0.48297	210	19.456
85	0.58947	220	23.660
90	0.71493	230	28.534
95	0.86193	240	34.144
100	1.03323	250	40.564
105	1.2318	260	47.868
110	1.4609	270	56.137
115	1.7239	280	65.456
120	2.0245	290	75.915
		300	87.611

Saturated Water Vapor Table (By Pressure)

Pressure kg/cm² P	Saturation Temperature °C ta	Pressure kg/cm² P	Saturation Temperature °C ta
0.1	45.45	3.6	139.18
0.2	59.66	3.8	141.09
0.3	68.67	4.0	142.92
0.4	75.41	4.2	146.38
0.5	80.86	5.0	151.11
0.6	85.45	6	158.08
0.7	89.45	7	164.17
0.8	92.99	8	169.61
0.9	96.18	9	174.53
1.0	99.09	10	179.04
1.1	101.76	11	183.20
1.2	104.25	12	187.08
1.3	106.56	13	190.71
1.4	108.74	14	194.13
1.5	110.79	15	197.36
1.6	112.73	16	200.43
1.8	116.33	17	203.36
2.0	119.62	18	206.15
2.2	122.64	19	208.82
2.4	125.46	20	211.38
2.6	128.08	25	222.90
2.8	130.55	30	232.75
3.0	132.88	35	241.41
3.2	135.08	40	249.17
3.4	137.18	45	256.22
		50	262.70

(Source: The Japan society of machinery water vapor tables (new edition))

Note: 1 kg/cm² = 0.9678 atm

C. Reliability Theory

C.1 Reliability Criteria

C.1.1 Failure Rate and Reliability Function

If we observe a sample of n devices at fixed time intervals h, we obtain a frequency distribution of the number of failures as shown in Figure C.1. In this analysis, ri devices fail in the period

ti−ti−1 = h, with all devices failing before the time tn.

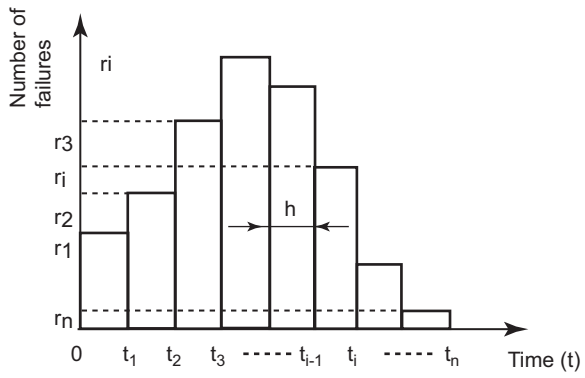


Figure C.1 Discrete Failure Distribution

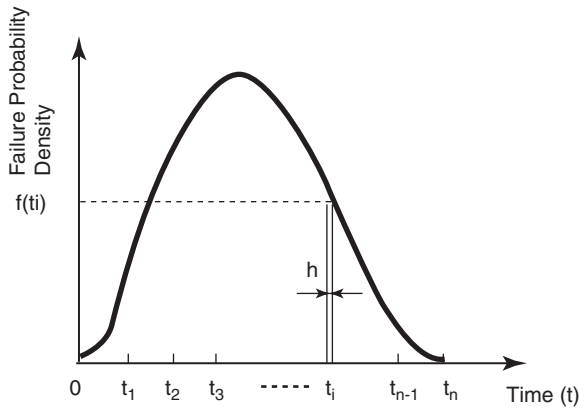


Figure C.2 Continuous Failure Distribution

The number of devices left after the i-th measurement period is given as $ni = n - \sum_{i=1}^{i} ri$. The average failure rate $\hat{\lambda}\,(t\,i-1,\,ti)$ in the period between ti-1 and ti is given by the expression

$$\hat{\lambda}\,(ti-1,ti) = \frac{ri}{ni-1} \bullet \frac{1}{h} \qquad \text{(App-1)}$$

If we make the time interval h increasingly small and use the failure rate density function f(t), the instantaneous failure rate λ (ti, ti + h) in the interval from ti to ti + h, shown in Figure C.2, is given by

$$\lambda\ (t_i, t_i + h) = \frac{f(t_i) \bullet h}{\int_{ti}^{\infty} f(t)dt} \bullet \frac{1}{h} = \frac{f(t_i)}{\int_{ti}^{\infty} f(t)dt} \qquad \text{(App-2)}$$

Equation App-2 is the generalization of the model in Figure C.2 with tn as infinity.

The probability that a device will fail before the time ti is known as the failure (or non-reliability) distribution function f(ti). Also, the probability that a device will not fail before time ti is the reliability function R(ti). These functions are shown in Figure C.3.

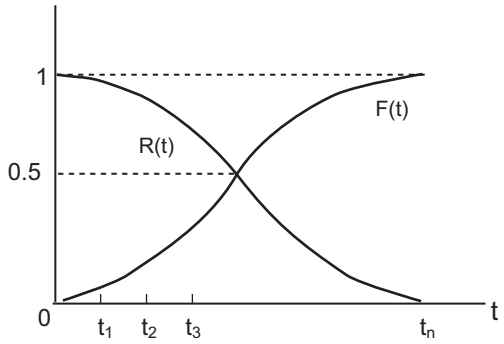


Figure C.3 Failure Distribution Function F(t) and Reliability Function R(t)

$$F(ti) = \int_0^{ti} f(t)dt \qquad \text{(App-3)}$$

$$R(ti) = 1 - F(ti) = \int_{ti}^{\infty} f(t)dt \qquad \text{(App-4)}$$

The probability P that a given semiconductor device will fail in the period between t and t + dt is the product of the probability R(t) that it will not fail before t and the instantaneous failure rate λ(t)dt in the period t to t + dt.

$$P = f(t)dt = R(t) \cdot \lambda(t)dt$$

$$\therefore \lambda(t) = \frac{f(t)}{R(t)} \qquad \text{(App-5)}$$

For the failure rate λ (t), using the relationship of equation App-4 we have

$$\lambda(t) = -\frac{1}{R(t)}\frac{d}{dt}R(t) = \frac{d}{dt}\,1nR(t) \qquad \text{(App-6)}$$

$$R(t) = exp\,(-\int_0^t \lambda(t)dt) \qquad \text{(App-7)}$$

C.1.2 Definition of Reliability Index

Mean value (or expected value) μ and variance σ^2 (where σ is the standard deviation) are defined as characteristics of the distributions of Figures C.1 and C.2 by the following expressions:

$$\left.\begin{aligned} \mu &= \int_0^{\infty} tf\,(t)\,dt \\ \sigma^2 &= \int_0^{\infty} (t-\mu)^2\, f(t)dt = \int_0^{\infty} t^2\, f(t)dt - \mu^2 \end{aligned}\right\} \text{(Continuous distribution)} \qquad \text{(App-8)}$$

$$\left.\begin{aligned} \mu &= \sum_{i=0}^{\infty} tif(t_i) \\ \sigma^2 &= \sum_{i=0}^{\infty} (t_i-\mu)^2\, f\,(ti) = \sum_{i=0}^{\infty} t_i^2\, f(ti) - \mu^2 \end{aligned}\right\} \text{(Discrete distribution)} \qquad \text{(App-9)}$$

The expected lifetime (remaining lifetime) L(t) of a device which has been operated for time t is given by the following expressions:

$$\left.\begin{aligned} L(t) &= \frac{1}{R(\gamma)}\left\{\gamma - t + \int_{\gamma}^{\infty} R(t)dt\right\} && (t \le \gamma) \\ L(t) &= \frac{1}{R(t)}\int_{\gamma}^{\infty} R(x)dx = \frac{1}{R(t)}\int_{0}^{\infty} R(t+y)dy && (\gamma \le t) \end{aligned}\right\} \quad \text{(App-10)}$$

Note that the device failure distribution function (equation App-3) takes on the constant g in the range $0 \le t \le \gamma$, that is,

$F(t) = 0\ (0 \le t \le \gamma)$

and that after the passage of time g it assumes a value (g is the order of position).

When equipment can be repaired by renewing a failed device, the mean value of the interval that operation is possible between occurrences of failures is know as the MTBF (Mean Time Between Failures).

If the operating time between subsequent failures of a device throughout its life until discarded is given by t1, t2, ..., tn, the MTBF is given by

$$MTBF = \frac{t1 + t2 + \ldots + tn}{n} \quad \text{(App-11)}$$

Since we are dealing with the measure of the entire operating life of the device, we will call (t1, t2, ..., tn) a complete sample. MTBF known after the life of equipment is of no practical use. Therefore, the MTBF for a truncated portion of the life of the equipment up to the time T0 is estimated using the following expression:

$$MTBF = \frac{t1 + t2 + \cdots + tr + (n - r)\,To}{n} \quad \text{(App-12)}$$

In equation App-12, r is the number of failures occurring until the time T0.

We can also estimate the MTBF truncated after the number of failures = r.

$$MTBF = \frac{t1 + t2 + \cdots + tr + (n - r)\,tr}{r} \quad \text{(App-13)}$$

In equations App-12 and App-13, the value n is determined by the type of failures for the device being considered (including such factors as the total number of semiconductor devices used and maximum number of failures before the equipment is disposed of).

In general, once a semiconductor device has failed, it cannot be repaired and used again. That is, it is a non-maintainable component. For this type of device, the mean time to the occurrence of a failure is know as the MTTF (Mean Time to Failure). As can be seen from equation App-10, the remaining expected life L(t) is not equal to the MTTF minus the actual operating time. This is analogous to the fact that the remaining life of an adult is not necessarily equal to the expected lifetime of a new born child minus the adult's actual age.

In the period that failure rate λ (t) is time-independent and is constant, taking the value λ, we can use equation App-7 to obtain

$$MTTF = \int_{0}^{\infty} R(t)dt = \int_{0}^{\infty} e^{-\lambda t}\,dt = \frac{1}{\lambda} \quad \text{(App-14)}$$

As a unit for the measure of failure rate,

1×10^9 *(failures/(number of operating devices × operating time)) = 1FIT* (App-15)

is used. For example, if we say that a given semiconductor device has a failure rate of 10 FITs, this means that one device fails for every 10^8 component hours. This, however, is not equivalent to saying the device lifetime is 10^8 hours. This is because the denominator of the defining expression equation App-15 (component hours) does not refer to any particular device.

C.2 Reliability of Composite Devices

C.2.1 Parallel and Series Models

Assume that we have n semiconductor devices used in series, and one device failure will result in the total group of devices failing. Such a system is known as a series system of redundancy of 0 (Figure C.4). If all the individual devices have failure mechanisms that are mutually independent, and the reliability function of the i-th device is given by the expression Ri(t) (where i = 1, 2, ..., n), the reliability function R (t) of this series system is

$$R(t) = \prod_{i=1}^{n} Ri(t) \qquad \text{(App-16)}$$

Equation App-3 used for integrated circuit models can be modified to

$$\lambda p = C_1 \pi_1 + C_2 \pi_2$$

$$\text{Where} \quad \pi_1 = \pi_Q \times \pi_T \times \pi_V \times \pi_L$$

$$\pi_2 = \pi_Q \times \pi_E \times \pi_L$$

Then the reliability function equation App-7 for integrated circuits can be expressed as follows using equation App-16.

$$R(t) = e^{-\lambda pt} = e^{-C1\pi 1t} \cdot e^{-C2\pi 2t} = R_1(t) \cdot R_2(t)$$

$$\text{Where} \quad R_1(t) = e^{-C1\pi 1t}$$

$$R_2(t) = e^{-C2\pi 2t}$$

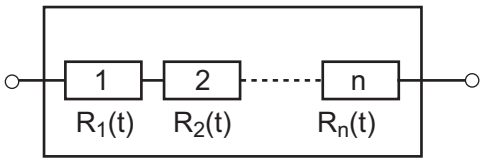
Hence equation App-3 is an equation derived by applying a series model of redundancy of 0 (Figure C.4) involving a failure factor (C_1) attributable to circuit complexity and a failure factor (C_2) caused by package complexity to integrated circuits.

There are other systems that n semiconductor devices are used in parallel, and as long as at least one of the devices is operating, the overall multiple device still functions. This is a parallel system with a redundancy of n -1 (Figure C.5). In this case as well, the failures of individual devices are taken to be mutually independent and to have no influence on other devices.

If the failure distribution function for the i-th device is Fi(t) (where i = 1, 2, ..., n), the failure distribution probability function F(t) for the parallel system is

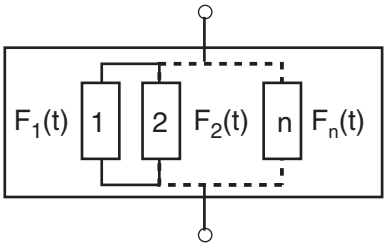
$$F(t) = \prod_{i=1}^{n} Fi(t) \qquad \text{(App-17)}$$

$$R(t) = 1 - F(t) \qquad \text{(App-18)}$$



$$R(t) = \prod_{i=1}^{n} Ri(t)$$

Figure C.4 Reliability Function for Series Model



$$R(t) = 1 - F(t)$$

Figure C.5 Reliability Function for Parallel Model

C.2.2 Application Example

Let us consider the reliability function of the system in Figure C.6. This model consists of m units connected in series, which i-th unit has ni devices connected in parallel. Moreover, we consider the system in Figure C.7, in which units of m series connected devices are connected in parallel up to n units. For the system in Figure C.6, let us assume that the reliability function for devices in the i-th unit is the same, which is Ri(t). In Figure C.7, we assume that the reliability function for the i-th series connected devices Rij (where j = 1, 2, ..., m) is the same and is Ri(t).

For the system in Figure C.6 we have

$$R(t) = \prod_{i-1}^{m} \{1 - (Ri(t))^n\} \qquad \text{(App-19)}$$

and for the system in Figure C.7 we have

$$R(t) = 1 - (1 - \prod_{i=1}^{m} Ri(t))^n \qquad \text{(App-20)}$$

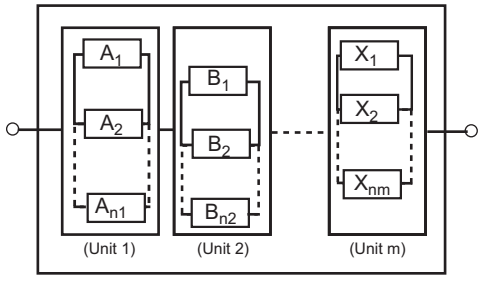


Figure C.6 Series-Parallel Composite Model (1)

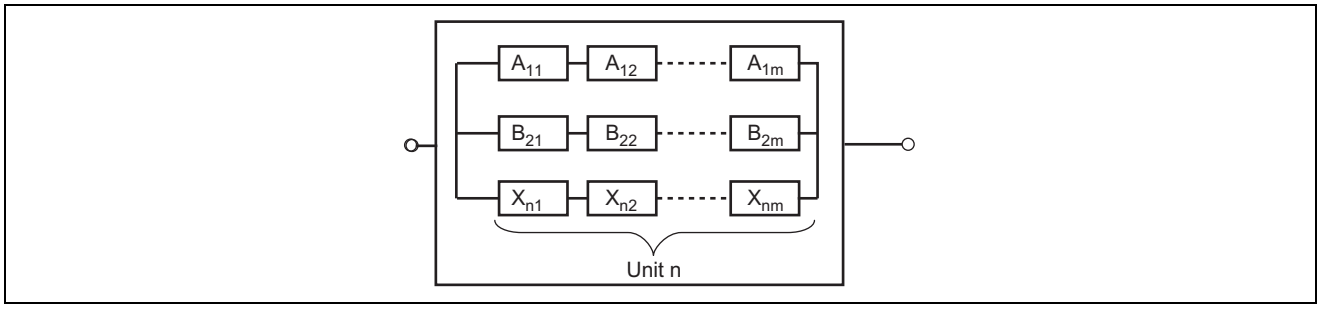


Figure C.7 Series-Parallel Composite Model (2)

C.2.3 Stand-by Redundancy System

If we attach a selector switch to n devices in the parallel model shown in Figure C.5, we can select another device should one particular device experience a failure (Figure C.8).

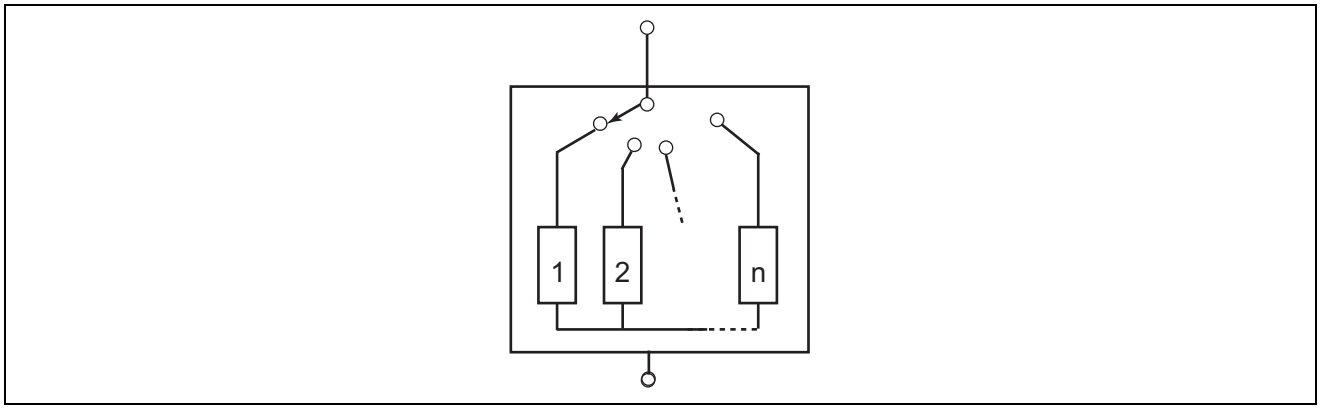


Figure C.8 Stand-by Redundancy Model

We will assume for simplicity that the switch does not fail and that the failure rates for the n devices are all equal to l. The reliability function R(t) for this system is given by the Poisson partial sum. An explanation of this equation will be given in D.9, Poisson Distribution.

$$R(t) = e^{-\lambda t} \sum_{i=0}^{n-1} \frac{(\lambda t)^{i}}{i!} \qquad \text{(App-21)}$$

If we now assume that the failure rate of the switch is equal to λ_K for any tap, the overall reliability function becomes

$$R(t) = e^{-\{\lambda + (n-1)\lambda_k\} t} \sum_{i=0}^{n-1} \frac{(\lambda t)^{i}}{i!} \qquad \text{(App-22)}$$

C.3 Failure Models for Accelerated Life Testing

C.3.1 Reaction Theory Model

A particular characteristic of a device has the value X. Let us assume that the device will fail when the characteristic value changes to X_L. If the amount of change in the characteristic value is found to be accelerated by thermal stress, in many cases the Arrhenius chemical reaction kinetics model can be applied to this phenomenon.

In chemical reactions, if molecules reach the temperature above which they may react (the activation energy), a reaction occurs. The higher the temperature of the molecules, the higher becomes their energies, and so increasing the temperature quickens reactions. Arrhenius expressed the chemical reaction rate, K, experimentally as follows:

$$K = \Lambda e^{-\frac{\Delta E}{kT}} \quad \text{(App-23)}$$

where

- Λ: experimentally derived constant
- k: Boltzmann constant
- ΔE: activation energy (kcal/mol)
- T: absolute temperature (K).

When considering the reliability of semiconductor devices, the activation energy is usually expressed in units of electron volts (eV), so that the Arrhenius relationship becomes

$$K = \Lambda e^{-\frac{\Delta E}{kT}} = \Lambda e^{11606 \times \left(-\frac{B}{T}\right)} \quad \text{(App-24)}$$

where

- B: activation energy (eV).

1eV is equivalent to 23.05 kcal/mol or 11,606 K.

C.3.2 Eyring Model

The Eyring model is an extension of the Arrhenius model, and takes into consideration both mechanical stress and voltage stress as well as thermal stress. The reaction rate K using this model is given by the following expression:

$$K = A\left(\frac{kT}{h}\right) \cdot e^{-\frac{\Delta E}{kT}} \cdot e^{\left\{f(s) \cdot \left(C + \frac{D}{kT}\right)\right\}} \quad \text{(App-25)}$$

where

- A, C, and D: constants
- ΔE: activation energy
- k: Boltzmann constant
- T: absolute temperature (K)
- h: Planck's constant
- f(s): stress function representing non-thermal stresses s

Here

$$f(s) = 1ns,\ C + \frac{D}{kT} = F$$

so that for small ranges of T, an approximation of equation App-25 becomes

$$K = \Lambda T e^{-\frac{B}{T}} s^{F} \quad \text{(App-26)}$$

C.3.3 Acceleration Factor

Let us assume that an intermittent operation life test performed on a semiconductor device detected, as a result of the stress placed on the device, a leakage current which increases with time. As the device is subjected to more and more cycles of intermittent operation (n), as shown in Figure C.9, the leakage current increases. The level of degradation of the device can be expressed as a function of the leakage current i. If we take this current i as the device characteristic X discussed in C.3.1, we can say that there is a failure criterion current iR MAX which corresponds to the device failure point XL. That is,

$$f = f(i) \quad \text{(App-27)}$$

Since the reaction rate K in the accelerated life test is basically defined as the rate of degradation of the device, we have

$$K = \frac{df(i)}{dt} \quad \text{(App-28)}$$

$$\therefore f(i) = Kt \quad \text{(App-29)}$$

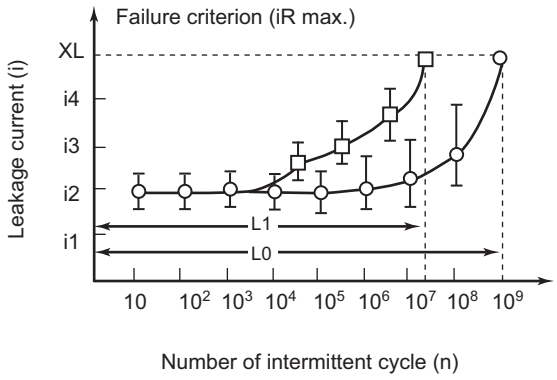


Figure C.9 Data Example for Intermittent Operation Life Test

The pattern of degradation f caused by the intermittent test varies depending upon the current flowing in the device. In Figure C.9 the curve marked with circles represents such test performed at the rated current of the device, while that marked with squares shows the results of operating the device intermittently at 1.5 times the rated current. Since in either case the device fails when i = iR MAX, if we use the subscripts 0 and 1 to represent test conditions for these two cases, we have

$$L_0 = \frac{f(iR\ MAX)}{K0},\ L_1 = \frac{f(iR\ MAX)}{K1} \quad \text{(App-30)}$$

In this case, the current acceleration factor α1 is

$$\alpha_1 = \frac{L_0}{L_1} = \frac{K_1}{K_0} \quad \text{(where the subscript 0 represents operation at the rated current)} \quad \text{(App-31)}$$

For the purposes of the explanation we have used an actual example, as shown in Figure C.9. We can, however, make a generalization about the state function f(X) and the characteristic value X that defines the state. If we use the relationship in equation App-29 in the Arrhenius equation of equation App-24, we have

$$K = \Lambda e^{-\frac{\Delta E}{kT}} = \frac{f(X)}{X} \quad \text{(App-32)}$$

If we assume that the device reaches the end of its life when the characteristic value X = XL, as discussed in C.3.1, equation App-32 will be

$$K = \frac{f(X_L)}{L} \qquad \text{(App-32')}$$

Then we have the relationship between temperature and life as

$$lnL = lnf(X_L) - ln\Lambda + \frac{\Delta E}{kT} \qquad \text{(App-33)}$$

Life tests using temperature as a dominant factor are verified by a logarithmic normal distribution. This is based on equation App-33. If we let T0 and L0 be the reference conditions (such as the standard operating conditions) for temperature and life, and T1 and L1 be the corresponding temperature and life for accelerated conditions, the temperature acceleration factor αT is referring to equation App-32,

$$\alpha_T = \frac{L_0}{L_1} = e^{\frac{\Delta E}{k}\left(\frac{1}{T0} - \frac{1}{T1}\right)} \qquad \text{(App-34)}$$

As can be seen by equation App-34, acceleration caused by heat varies depending on the activation energy ΔE. The relationship between activation energy and the acceleration factor is shown in Figure C.10.

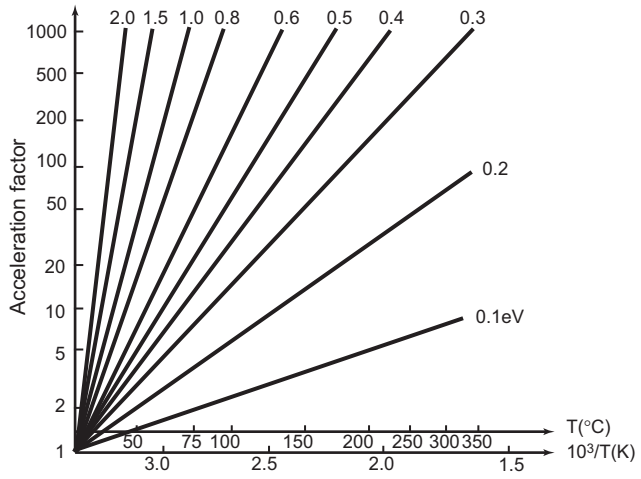


Figure C.10 Activation Energy Versus Acceleration Factor

C.4 Analysis of Test Results

C.4.1 Weibull Probability Paper [4] [5]

(a) Purpose

Weibull probability paper is used 1) to determine if the life span or strength data obtained from the reliability test conforms to the Weibull distribution and 2) to obtain the parameter of the Weibull distribution from the chart. The data is plotted as pairs of test time t (or value of stress strength) and cumulative failure rate F(t).

(b) Format

Figure C.11 illustrates the basic format of Weibull probability paper. As shown in the right hand margin, the vertical axis is scaled evenly with a space of lnln {1/(1 – F(t))}, and the horizontal axis in the upper margin is scaled evenly with ln t. The corresponding F(t) is scaled in the left hand margin and the t is scaled in the lower margin.

The main axis scaled with lnln {1/(1 – F(t))} = 0 is hereafter referred to as X_0 and the main axis scaled with ln t = 0, as Y_0. The point where $X_0 = 1$ and $Y_0 = 0$ is indicated by "○". Typical Weibull probability paper also contains the nomographs μ/η, σ/η, and F(μ) corresponding to m. Figure C.12 is an example of Weibull probability paper.

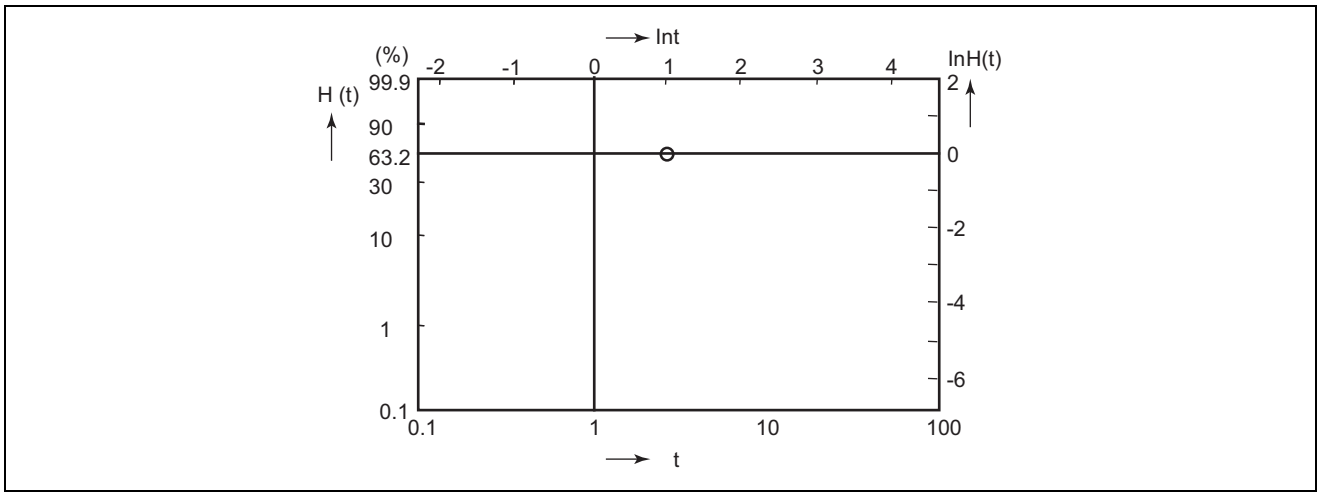


Figure C.11 Basic Format of Weibull Probability Paper

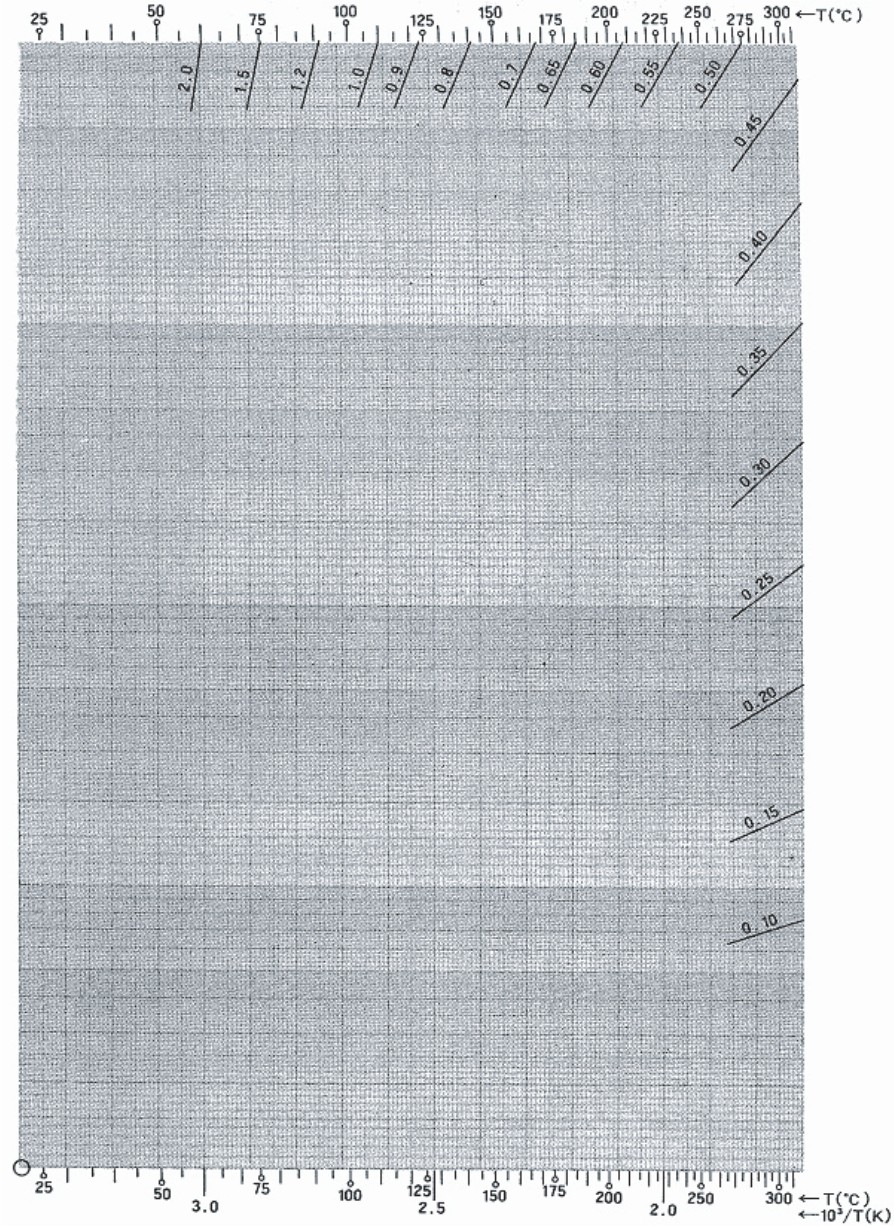


Figure C.12 Chart for Determining Relationship between Activation Energy and Acceleration Factor

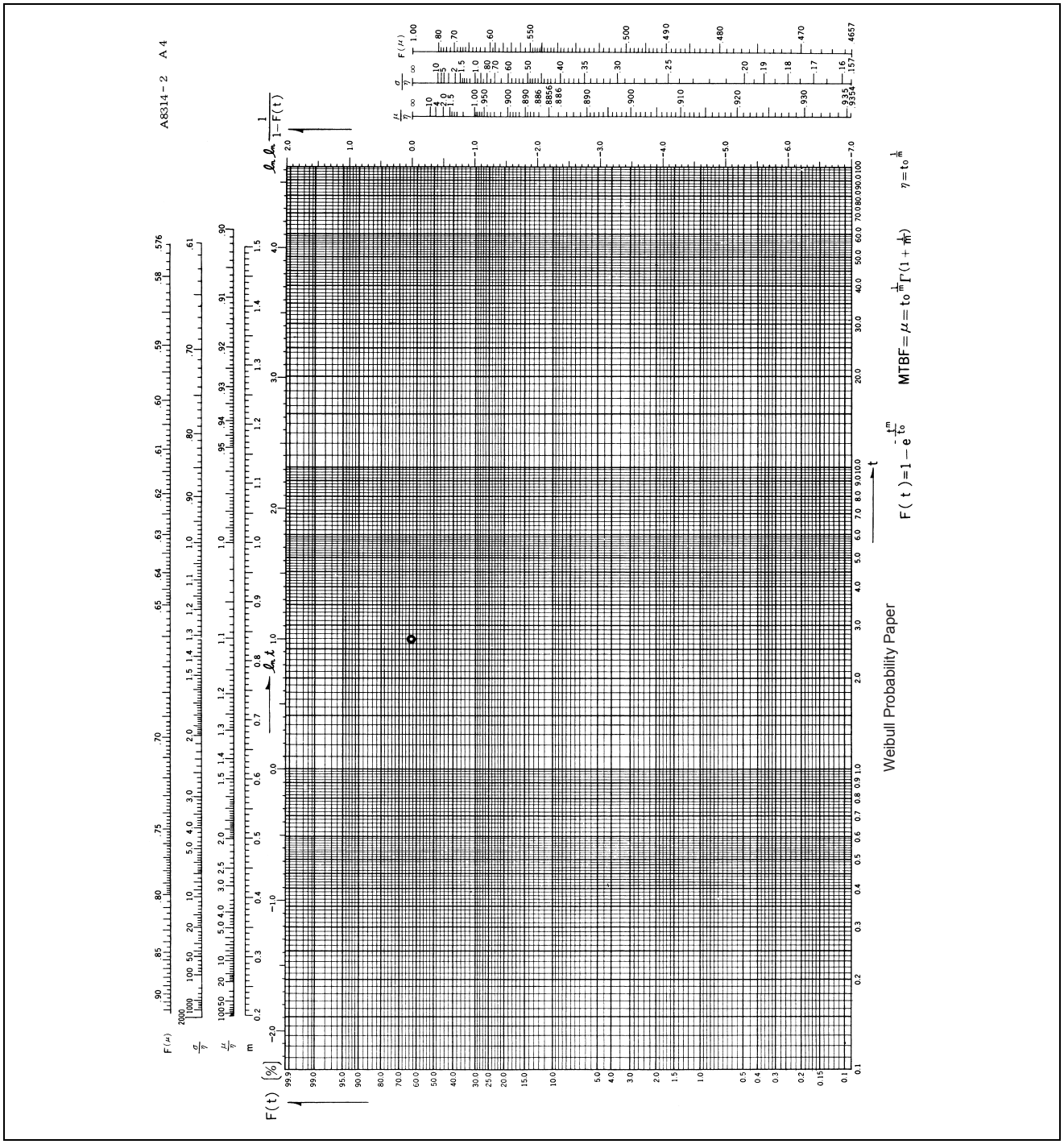


Figure C.13 Example of Weibull Probability Paper

(c) Theory

The failure rate on the Weibull distribution is obtained from the Weibull failure distribution function using shape parameter m, scale parameter t_0, and characteristic life $\eta = t_0^{1/m}$ with position parameter $\gamma = 0$.

$$F(t) = 1 - e^{\frac{t^m}{t_0}} = 1 - e^{-(\frac{t}{\eta})^m} \qquad \text{(AppC4-1)}$$

This is shown as a straight line on the Weibull probability plotting paper described in Figure C.13. The mean value μ, standard deviation σ, and failure distribution F(μ) of the Weibull distribution are expressed as follows,

using the gamma function $\Gamma(z) = \int_0^\infty e^{-t}\ t^{z-1}\ dt$

$$\mu = \eta \Gamma \left(1 + \frac{1}{m}\right) \quad \text{(AppC4-2)}$$

$$\sigma = \eta \sqrt{\Gamma \left(1 + \frac{2}{m}\right) - \Gamma^2 \left(1 + \frac{1}{m}\right)} \quad \text{(AppC4-3)}$$

$$F(\mu) = 1 - e^{-\left\{\Gamma\left(1 + \frac{1}{m}\right)\right\}^m} \quad \text{(AppC4-4)}$$

μ/η, σ/η, and $F(\mu)$ are the functions of m only and can constitute a nomograph corresponding to m.

(d) Usage

1. Plot the data on the Weibull probability paper

   Obtain F(t) = r / (n + 1) by the average ranking method where n is the total number of samples, t is the time when each sample fails, and r is the cumulative number of failure samples at t.

   Plot the points on the Weibull probability paper and fit a straight line. To ensure that the points are entered correctly, the lower scale is multiplied by 10^{α} (where α is a positive or negative integer). When a curve can be fit, search for a proper γ and replace t with $(t - \gamma)$ for plotting so that a straight line fits.
2. Obtain parameters on the Weibull probability paper

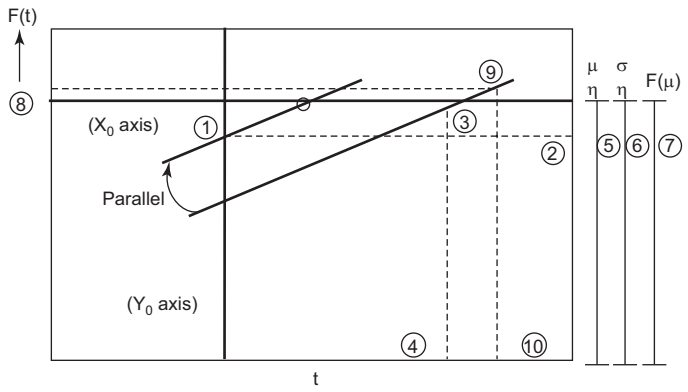


Figure C.14 Procedure for Use of Weibull Probability

Next, obtain the gradient m of the straight line from the scales at the upper and right hand margins. To simplify the procedure, using the scale on the right hand margin, read the value of the point where the line that is parallel to the plot line goes through the point circled ("○") which crosses the Y_0 axis. Then invert the value to obtain m (① → ② as in Figure C.14).

η is read from the point that the plot line crosses the X_0 axis, using the scale at the lower margin (③ → ④). If the plot line is too low, the value can be recalculated by equation

$$\eta = e^{\left(\frac{1}{m} \cdot Int_0\right)}$$

as the value of the point that crosses the Y_0 axis, read on the right hand scale, corresponds to the value $-\ln t_0$.

The values of μ and σ, which correspond to the value of m, are obtained by reading the values on the μ/η scale and σ/η scale and multiplying them η (② → ⑤, ⑥). The enlarged scale nomograph at the upper margin on the Weibull probability paper can also be used. To obtain μ more simply, obtain $F(\mu)$ that corresponds to m from the $F(\mu)$ scale and use t as μ that corresponds to the plot line $F(\mu)$ (② → ⑦ → ⑧ → ⑨ → ⑩).

Where γ is used in (1), obtain μ corrected to $(\mu + \gamma)$ and η corrected to $(\eta + \gamma)$.

3. Interpretations of Weibull Plotting [3]

   Figure C.15 shows major interpretations of the obtained value m and the corresponding failure number including those of complex models.

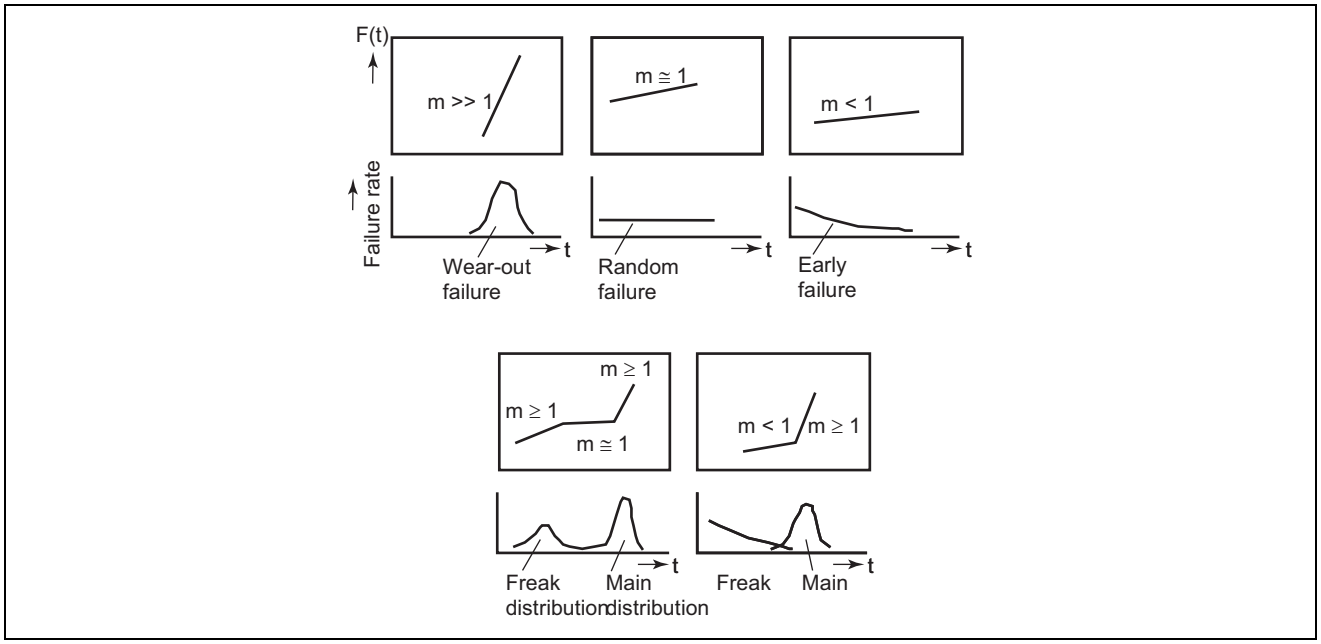


Figure C.15 Example of Weibull Probability Results

C.4.2 Cumulative Hazard Paper [4] [5]

(a) Purpose

When there are several failure modes in the reliability tests and when the distribution parameter must be checked for each failure mode, or when there are some suspended data, plotting on the Weibull probability plotting paper may require a complicated procedure. In this case plotting on the cumulative hazard paper is less complicated. The data is plotted as pairs of test time t (or stress intensify) and cumulative hazard H(t). Weibull type cumulative hazard paper is explained below.

(b) Format

Figure C.16 illustrates the basic format of the Weibull type cumulative hazard paper.

Compared with the Weibull probability plotting paper in Figure C.11, the only difference is that the vertical axis is scaled with cumulative hazard function H(t). The example in Figure C.17 (made by the Union of Japanese Scientists and Engineers (JUSE)) shows the nomograph as having the μ/η, σ/η, and t*/η scales, and no F(μ) scale. The F(t) scale on the left margin corresponds to H(t).

(c) Theory

When the cumulative hazard is $H(t) = \int_0^t h(t)\,dt$,

$$F(t) = 1 - e^{-\int_0^t h(t)\,dt} = 1 - e^{-H(t)} \qquad \text{(AppC4-5)}$$

and if this is compared to the equation (AppC4-5) indicating the Weibull distribution, then

$$1 - e^{-H(t)} = 1 - e^{-(\frac{t}{\eta})^m}$$

Therefore, $H(t) = (\frac{t}{\eta})^m$

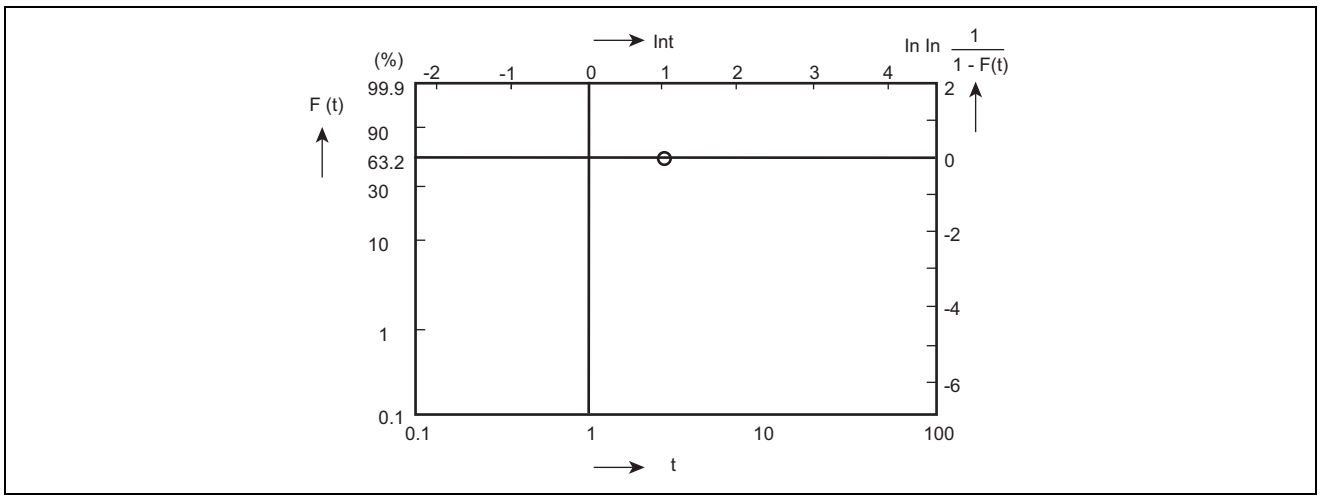


Figure C.16 Basic Format of Weibull Type Cumulative Hazard Paper

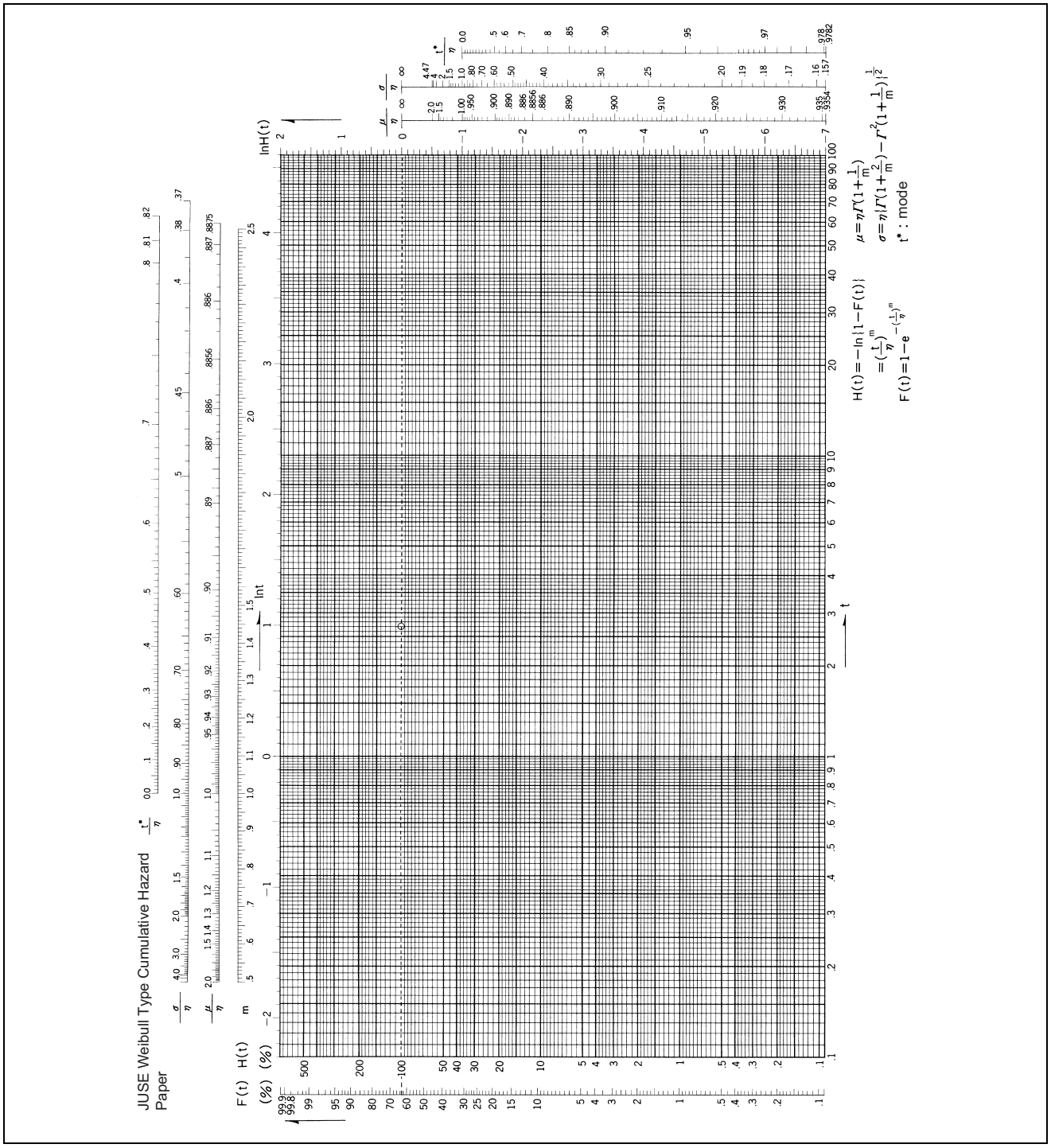


Figure C.17 Example of Weibull Type Hazard Paper

Taking the logarithm of both sides, we get

$$lnH(t) = m(lnt - ln\ \eta) \qquad \text{(AppC4-6)}$$

When we let $Y = ln\ H(t)$, $X = lnt$, and $b = -ln\ \eta\ m$, (AppC4-6) becomes an equation of the direct function with $Y = mX + b$, shown as a straight line on the Weibull type hazard paper described in Figure C.17.

For a reference, Figure C.18 shows an example of the relationship between cumulative failure rate F(t) obtained from equation (AppC4-5) and cumulative hazard H(t). When $t = \eta$ (characteristic lifetime), $H(\eta) = 1$ and $F(\eta) = 0.632$.

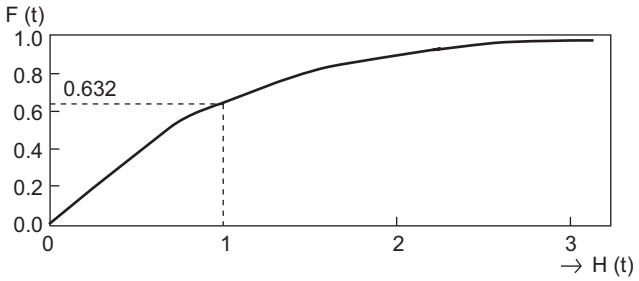


Figure C.18 Relationship between F(t) and H(t)

(d) Usage

1. Prepare a work sheet

   Prepare a work sheet as shown in Figure C.19 to obtain the cumulative hazard value from the test data.
2. Fill in the work sheet

   Enter the observed failure time and censored time in ascending order into the ti column of the work sheet. Enter sequence i starting from 1 and enter the sample number and failure modes, displaying ti in the graph on the right hand margin. Then visually reconfirm the data in the graph. When entering the failure mode, mark censored data as C (censored).
3. Obtain cumulative hazard H(ti)

   Obtain the hazard value h(ti). Calculate the reverse sequence $Ki = n - i + 1$ from sequence j where total number of samples is n, and enter the value into the work sheet. Then obtain the hazard value $h(ti) = 1/Ki \times 100(\%)$ and enter it in the chart. H(ti) is obtained by accumulating h(ti). If several must be analyzed, use Hj(ti) to that h(ti) corresponding to Mi and add one by one.

   An example is shown in Figure C.20.

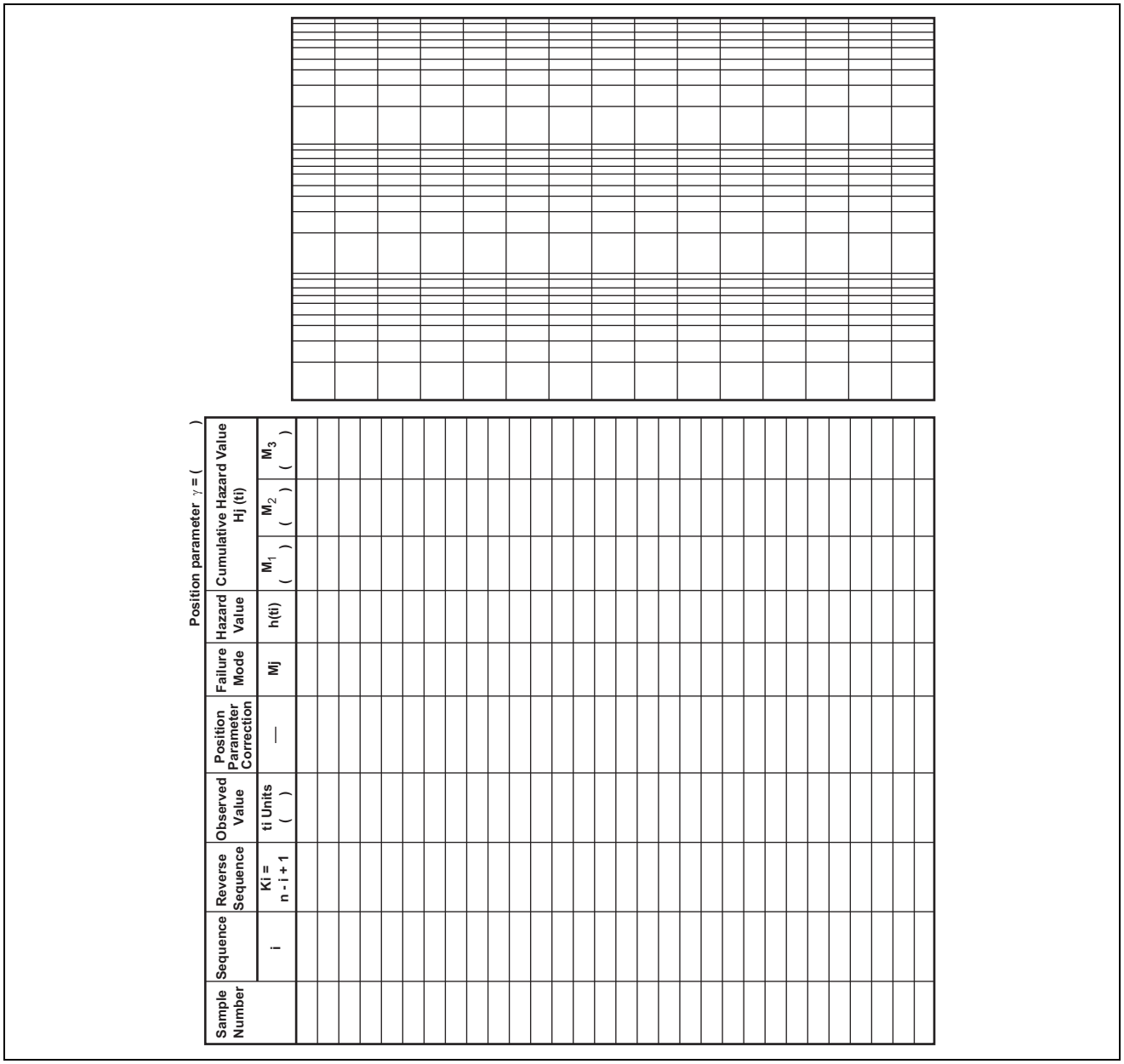


Figure C.19 Example of Work Sheet Used for Data on Cumulative Hazard Paper

Sample Number	Sequence	Reverse Sequence	Observed Value	Position Parameter Correction	Failure Mode	Hazard Value	Cumulative Hazard Value Hj (ti)		
	i	Ki = n – i + 1	ti Units (h)	—	Mj	h(ti) %	M_1 (A)	M_2 (B)	M_3 ( )
#4	1	10	200		A	10.0	10.00		
#7	2	9	300		B	11.11		11.11	
#5	3	8	300		A	12.50	22.50		
#9	4	7	800		C				
#2	5	6	800		A	16.67	39.17		
#8	6	5	800		C				
#1	7	4	900		B	25.00		36.11	
#3	8	3	1000		C				
#6	9	2	1600		B	50.00		86.11	
#10	10	1	2500		B	100.0		186.11	

Notes: **C: Censored**
Position parameter $\gamma = 0$

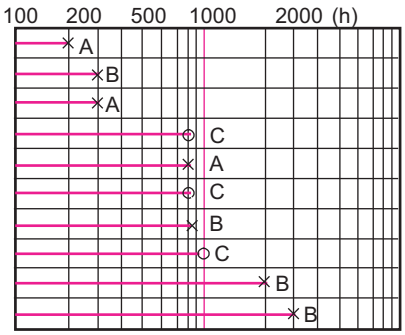


Figure C.20 Fill-in Example of Work Sheet

4. Plot data on the cumulative hazard paper

   Plot the point that is a pair of Hj(ti) and ti for each failure mode and try to fit a straight line. If a curve fits, search for proper γ and replace t with (t-γ) so that a straight line fits.

   Then obtain m, η, μ, and σ as described in section C.4.1. The mode t* (most frequent value) can be obtained using the method shown in Figure C.17.

C.4.3 Prediction Method from MIL-HDBK-217

Though reliability prediction based on reliability test data is used in most cases, the prediction method from MIL-HDBK-217 may be used by users when there is no reliability data. However, note that the calculated value of this prediction tends to be greater than that of prediction based on reliability data as described later.

The purpose of creating the MIL-HDBK-217 is to establish a uniform methodology for predicting the reliability of military electronic equipment and systems and to provide a common basis for reliability predictions performed at the acquisition program stage for military electronic equipment and systems. This handbook also establishes a common basis for comparing and evaluating reliability predictions of related or competing designs.

The data in the MIL-HDBK-217 handbook has been collected as field usage data for vast numbers of military electronic equipment that is purchased under MIL standards. Since compliance with MIL-HDBK-217 has been established by the Pentagon as a requirement in the military electronic equipment that it purchases, a safety coefficient must be fully taken into account for each factor.

Therefore, calculated failure rate normally tends to be higher than the failure rate predicted based on reliability tests. When the failure rate of the same product is compared by using the prediction based on reliability tests and the prediction based on MIL-HDBK-217, the failure rate calculated based on MIL-HDBK-217 is 10 to 100 times higher than the failure rate based on reliability tests.

D. Probability Models Used in Reliability Analysis

D.1 Bernoulli Trial

From a given population of semiconductor devices a single device is sampled and tested. The possible test results are limited to either (1) “failure or defect” or (2) “no failure or acceptance,” with no possibility of such results as “pending decision” or “exception acceptance” allowed. This cycle of sampling, testing, and rejection/acceptance is repeated n times. In a single such test the probability of (1) “failure” is p and the probability of (2) “no failure” is q (p + q = 1). The values of p and q will be uniform for all test results. Each test result is independent from one another. This discrete model is termed the Bernoulli trial or sampling. For ease of understanding we have chosen “failure” and “no failure” for results (1) and (2), respectively. The fundamental condition of the Bernoulli trial is that results are only two types and they are definitely identified.

D.2 Binomial Distribution: fBin(x, n, p)

In the Bernoulli trial, assume that x of n tests result in (1) and n – x tests result in (2). Such a phenomenon occurs with some probability. This probability is described by the binomial probability distribution fBin(x, n, p).

$$\left.\begin{aligned} f_{Bin}(x,\ n,\ p) &= \binom{n}{x} p^x q^{n-x} = \frac{n!}{x!(n-x)!} p^x q^{n-x} \\ \mu &= np,\quad \sigma^2 = npq \end{aligned}\right\} \qquad \text{(App-35)}$$

A sample lot comprising n devices randomly selected from a large population whose average fraction defective is p, contains x defective devices with some probability. Such a probability is a typical example of the binomial probability distribution.

D.3 Negative Binomial Distribution: fneg – bin(x, n, p) and Multinomial Distribution: fmulti-bin(x1, x2, ..., xm, n, p1, p2, ..., pm)

Let us consider the number of tests n required before we encounter (1) “failure” x times in the Bernoulli trial. By the (n−1) th test there have been x−1 times of (1) and (n−1)−(x−1) = n−x times of (2), and the x-th failure occurs on the n-th test. The probability of this, fneg-bin(x, n, p) is

$$f_{neg-}\ bin(x,\ n,\ p) = \binom{n-1}{x-1} p^{x-1} \cdot q^{(n-1)-(x-1)} \cdot p = \binom{n-1}{n-x} p^x q^{n-x} \qquad \text{(App-36)}$$

Using the characteristics of binomial coefficients, we have

$$\binom{-x}{x-1} = (-1)^{n-x} \binom{n-1}{n-x}$$

Hence from equation App-36,

$$\sum_{n=x}^{\infty} f_{neg}-bin(x,\ n,\ p) = \sum_{n=x}^{\infty} \binom{n-1}{n-x} p^x q^{n-x} = p^x \sum_{n=x}^{\infty} (-1)^{n-x} \binom{-x}{n-x} q^{n-x}$$

$$= p^x \sum_{r=0}^{\infty} \binom{-x}{r} (-q)^r = p^x (1-q)^{-x} = 1 \qquad \text{(App-37)}$$

Since fneg-bin (x, n, p) ≥ 0, we have, from equation App-37

$$\left.\begin{aligned} f_{neg}\ -bin(x,\ n,\ p) &= \binom{n-1}{n-x} p^x q^{n-x} = \binom{-x}{n-x} p^x q^{n-x} \\ \mu &= \frac{xq}{p},\quad \sigma^2 = \frac{xq}{p^2} \end{aligned}\right\} \qquad \text{(App-38)}$$

There is a case that test results are not limited to two possible results of acceptance and rejection but fall into m classes (E1, E2, ..., Em). Let us examine the probability fmulti-bin(x1, x2, ..., xm, n, p1, p2, ..., pm) with which tested devices fall into these classes. After n times of tests, any one of the results is E1, E2, ..., or Em. The result Ei occurs with the probability pi. The result Ei is observed xi times ($\sum_{i=1} xi = n,\ n \geq xi \geq 0$) during n tests. Hence, results fall into m classes (E1, E2, ..., Em) numbering x1, x2, ..., xm with the probability fmulti-bin(x1, x2, ..., xm, n, p1, p2, ..., pm). This is known as the multinomial distribution.

$$f_{multi-bin}(x1,\ x2, \ldots xm, n,\ p1,\ p2 \ldots pm) = \frac{n!}{x1!x2! \ldots xm!} p1^{x1} p2^{x2} \ldots pm^{xm} \qquad \text{(App-39)}$$

The multinomial distribution is an extended binomial distribution with m variables.

D.4 Geometric Distribution: fGeo(n, p)

In the Bernoulli trial, the first 1 “failure” is encountered on the n-th test. The probability of this phenomenon is expressed by the geometric distribution fGeo(n, p)

$$\left.\begin{aligned} & f_{Geo}(n,\ p) = q^{n-1} p \quad (n = 1,2, \ldots) \\ & \mu = \frac{q}{p},\ \sigma^2 = \frac{q}{p2} \end{aligned}\right\} \qquad \text{(App-40)}$$

The geometric distribution is a case of equation App-38 for the negative binomial distribution where x = 1. The mean value of the geometric distribution μ is the expected value for the number of tests in Bernoulli trial before the first occurrence of 1. The failure distribution function of the geometric distribution is

$$F_{Geo}(N,\ p) = \sum_{n=1}^{N} f_{Geo}(n,\ p) = p + qp + q^2 p + \ldots + q^{N-1} p = 1 - q^N$$

which indicates that even if the acceptance rate q on any particular test is high (q 1), a failure will eventually occur ($\lim_{N \to \infty} F_{Geo}(N,\ p) = 1$) with a larger number of tests N.

D.5 Hypergeometric Distribution: fH – geo(N, R, n, x)

In the mass production of semiconductor devices a widely used technique is the sampling of a small number of devices n from a large population of N devices and making decision on the total population based on observation of the sample alone. An overall population of N devices has R defective devices (R is not known unless 100% inspection is performed). By inspecting n randomly sampled devices, x defective devices are detected with the probability fH – geo (N, R, n, x). If min (R, n) represents the smaller of R and n, we have

$$\left.\begin{aligned} & f_{H-geo}(N, R, n, x) = \frac{\binom{R}{x}\binom{N-R}{n-x}}{\binom{N}{n}} \quad (0 \leq x \leq min\,(R, n)) \\ & \mu = n\frac{R}{N} = np,\quad \sigma^2 = \frac{N-n}{N-1} npq \end{aligned}\right\} \qquad \text{(App-41)}$$

This is referred to as the probability function of hypergeometric distribution. Different ways are available for sampling n devices from N devices. If the sampled device is returned each time to choose a device from N constantly, or using replacement operations in other words, we will obtain a binomial distribution. If the sampled device is not returned (non-replacement), we will have a hypergeometric distribution. If the original population is large, however, the fraction defective obtained through a sampling inspection can be approximated by the binomial distribution. By expanding equation App-41 and reordering the product terms, we have

$$f_{H-geo}(N, R, n, x) = \binom{n}{x} \prod_{j=0}^{x-1} \frac{R-i}{N-i} \prod_{j=0}^{n-x-1} \left(1 - \frac{R-x}{N-x-j}\right) \qquad \text{(App-42)}$$

If N and R increase to infinity while maintaining $\frac{R}{N} = p$ constant, for finite n (and therefore finite x) we have

$$\lim_{N,R\to\infty} \prod_{i=0}^{x-1} \frac{R-i}{N-i} = \left(\frac{R}{N}\right)^x = p^x, \quad \lim_{N,R\to\infty} \prod_{j=0}^{n-x-1} \left(1-\frac{R-x}{N-x-j}\right) = \left(1-\frac{R}{N}\right)^{n-x} = (1-p)^{n-x}$$

If we focus on this, in the limit where N and R go to infinity, from equation App-42 we obtain

$$f_{H-geo}(N, R, n, x) \to \binom{n}{x} p^x (1-p)^{n-x} = f_{Bin}(x, n, p) \qquad \text{(App-43)}$$

An actual sampling plan sets a rejection criterion number c. If the number of defective devices x detected in a sample of n devices does not exceed c, the entire lot is considered to have passed inspection. When n devices are sampled from a population with fraction defective ($p\left(=\frac{R}{N}\right)$) the number of defective devices x will not exceed c with some probability. This probability Ψ with which the lot is judged to be accepted (the lot acceptance rate) is given by equation App-44.

$$\Psi = \sum_{x=0}^{c} f_{H-geo}(N, Np, n, x) = \sum_{x=0}^{c} \frac{\binom{Np}{x}\binom{Nq}{n-x}}{\binom{N}{Np}} \qquad \text{(App-44)}$$

The lot acceptance rate Ψ varies depending on how the values of n and c are chosen for populations of the same quality level (i.e., p being the same value), as is clearly indicated by equation App-44. How the lot acceptance rate changes is illustrated by the operation characteristic curve (OC curve) in Figure D.1. The fraction defective ($p\left(=\frac{R}{N}\right)$) with which the population contains defective devices is plotted on the horizontal axis. The probability Ψ with which the lot is judged to be accepted through sampling inspection is plotted on the vertical axis.

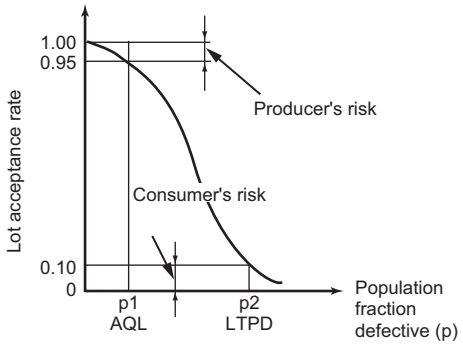


Figure D.1 OC Curve

In some sampling plans, the fraction defective p1 is set to control the lot acceptance rate to, for example, 95%. This plan is known as the AQL (Acceptable Quality Level) plan. In this case, 5% of lots whose quality level could be accepted (fraction defective p1) are rejected by sampling inspection. The producer gives up shipping the 5%. The risk of this rejection implies the producer's loss, so the risk is referred to as producer's risk.

In some other inspection plans, lots whose fraction defective is p2 are accepted with a probability of, for example, 10%. Such an inspection plan is known as the LTPD (Lot Tolerance Percent Defective) plan. This implies that the consumer takes a risk of purchasing a lot whose fraction defective is p2 with a probability of 10%. This is known as consumer's risk.

The AQL plan measures the lot whose fraction defective is p1 as having the lowest acceptable quality level. In contrast, the LTPD plan verifies that the fraction defective is no more than p2 with 90% probability.

D.6 Exponential Distribution: fexp(t)

The failure rate is constant with time in the random failure period. Therefore, from equation App-7, we have

$$R(t) = e^{-\lambda t}$$
$$f_{exp}(t) = \lambda e^{-\lambda t} \quad \text{(App-45)}$$

$$\mu = \frac{1}{\lambda} = MTTF \text{ (or } MTBF), \quad \sigma^2 = \frac{1}{\lambda^2} \quad \text{(App-46)}$$

Observation of a model with a constant failure rate may be either continuous or discrete at fixed intervals. By considering the probability of detecting the first failure at time t, the relation of exponential and geometric distributions can be identified.

Let us assume that floating dust causes an average of r mask defects on the surfaces of silicon wafers of a given lot. The area of the wafer surface S is divided into many portions. From one end of the wafer, each portion is inspected with a microscope. Since the location of the dust particles on the wafer surface is unpredictable, we can assume that mask defects occur completely at random. Therefore, the failure rate λ is uniform over the wafer's entire surface, so $\lambda = \frac{r}{S}$, the probability p of a mask defect existing in a divided portion is

$$p = C\lambda \quad \text{(App-47)}$$

where C is the area of the portion.

If the first detection of a mask defect is in the x-th portion, that is, the first detection occurs when the inspected area reaches t (t = Cx), the probability that this phenomenon will occur is expressed by the geometric distribution $pq^{x-1} = p\,(1 - p)^{x-1}$ on the average in the portion C that includes t. A mask defect can be detected at the same level of expectation at the inspection area t and at the number of inspection cycles x (Figure D.2).

$$\text{Mask defect expectation} = \lambda t = xp \quad \text{(App-48)}$$

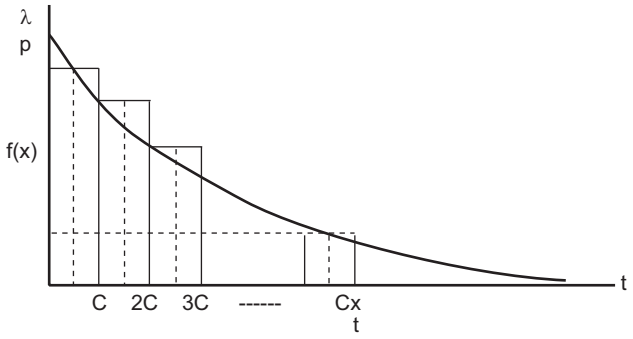


Figure D.2 Relation between Geometric and Exponential Distributions

Incidentally, continuous observation is in this case equivalent to reduction of the area C to the limit. The average probability of finding a mask defect within the area C approaches the probability that a mask defect exists on a point on the surface of the wafer. Noting the relations expressed by equations App-47 and App-48, we have

$$\lim_{C\to 0}\frac{1}{C}pq^{x-1} = \lim_{C\to 0}\frac{P}{C}(1-p)^{x-1} = \lambda \lim_{p\to 0}\left[(1-p)^{\frac{1}{p}}\right]^{\lambda t}\cdot\frac{1}{1-p} = \lambda e^{-\lambda t} \quad \text{(App-49)}$$

This implies that the exponential distribution is equivalent to the limit of the geometric distribution.

D.7 Pascal Distribution: fPas(x, y, p)

In a Bernoulli trial comprising n = x + y tests, there may be a case that the last n-th test result is (1) “failure” after x times of (1) “failure” and y times of (2) “no failure.” The probability that this phenomenon occurs is expressed by the Pascal probability distribution fPas(x, y, p).

$$\left.\begin{aligned} f_{Pas}(x,\ y,\ p) &= \binom{x+y-1}{y} P^x q^y \\ \mu &= \frac{qy}{p},\quad \sigma^2 = \frac{qy}{p^2} \end{aligned}\right\} \qquad \text{(App-50)}$$

If x = 1 in a specific case, the Pascal distribution is the same as the geometric distribution.

$$f_{Pas}(1,\ y,\ p) = pq^y = f_{Geo}(y+1,\ p) \qquad \text{(App-51)}$$

Consider that products are randomly sampled from a flow process in a production line for the purpose of intermediate inspection. The probability of defective items produced in the manufacturing process is p. For a sampling inspection of n = x + r items, the probability that the r-th failed product is detected is expressed by the Pascal distribution.

We can find a relation between the Pascal distribution and the binomial distribution if we interpret the Pascal distribution as a Bernoulli trial comprising n−1 tests with phenomenon 1 invariably occurring at the last n-th time after x−1 times of phenomenon 1.

$$f_{Pas}(x,\ y,\ p) = p\, f_{Bin}(x-1,\ n-1,\ p) \qquad Where \quad n = x + y \qquad \text{(App-52)}$$

D.8 Gamma Distribution: fΓ(t, α, β)

We can derive the relation below from equation App-50 representing the Pascal distribution.

$$f_{Pas}(x,\ y,\ p) = \frac{p\,(n-1)}{x-1}\ f_{Pas}(x-1,\ y,\ p), \qquad Where\ n = x + y \qquad \text{(App-53)}$$

From equations App-51 and App-49, we have

$$f_{Pas}(1,\ y,\ p) = f_{Geo}(y+1,\ p) \rightarrow f_{exp}(\lambda t) = \lambda e^{-\lambda t} \qquad \text{(App-54)}$$

In equation App-54, the arrow → denotes the operation $\lim_{C \to 0}$ used to reduce the divided portion C for discrete observation, which is the relation shown by equation App-49. Noting the relation expressed by Eqs. App-53 and App-54, we can obtain Pascal probability distribution functions respectively for x = 1, 2, 3, ...

$$x = 1 : f_{Pas}(1,\ y,\ p) \rightarrow \lambda e^{-\lambda t} \qquad \text{(App-55)}$$

$$x = \ : f_{Pas}(2,\ y,\ p) = \frac{p(n-1)}{1}\ f_{Pas}(1,\ y,\ p) = \frac{\lambda t}{1}\ f_{Pas}(1,\ y,\ p) \rightarrow \frac{\lambda t}{1}\lambda e^{-\lambda t} \qquad \text{(App-56)}$$

In equation App-56, we used the relation represented by equation App-48. Similarly we have

$$x = 3 : f_{Pas}(3,\ y,\ p) = \frac{\lambda t}{1} \cdot \frac{\lambda t}{2} f_{Pas}(1,\ y,\ p) \rightarrow \frac{(\lambda t)^2}{2!}\lambda e^{-\lambda t}$$

Its generalized equation is

$$f_{Pas}(x,\ y,\ p) \rightarrow \lambda \frac{(\lambda t)^{x-1}}{(x-1)!} e^{-\lambda t} \equiv f\Gamma\ (t,\ x,\ \lambda) \qquad \text{(App-57)}$$

The function fΓ(t, x, λ) derived by equation App-57 from fPas(x, y, p) is known as the Gamma probability function. By calculating the normalized constant of $\int_0^\infty dt$ for equation App-57, we obtain the generalized expression of the Gamma distribution.

$$f\Gamma\ (t,\ \alpha,\ \beta) = \frac{\alpha}{\Gamma\ (\beta)} (\alpha t)^{\beta-1} e^{-\alpha t} \qquad \text{(App-58)}$$

In equation App-58 expressing the Gamma distribution, β is the shape parameter and α, the scale parameter. Figure D.3 shows graphs of equation App-57 where λ = 1.

$$f\Gamma\ (t,\ x,\ 1) = \frac{1}{(x-1)!} t^{x-1} e^{-1} \qquad \text{(App-59)}$$

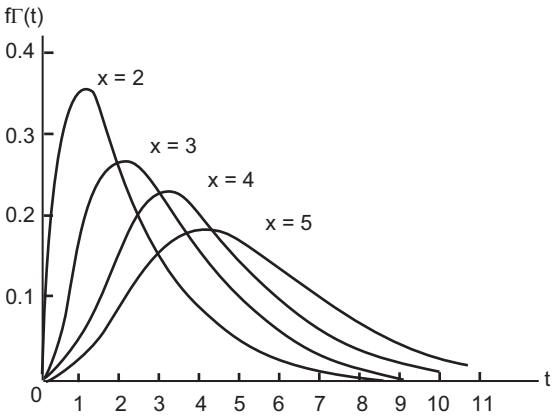


Figure D.3 Gamma Probability Density Functions fΓ(t, x, 1)

As can be seen from the derivation of the Gamma distribution given by equations. App-55 through App-57, the Pascal and Gamma distributions are the discrete and continuous probability distributions for the same probability model.

In particular, for the case of x = 1, the Gamma distribution (App-57) reduces to the exponential distribution (App-46). The Pascal distribution, if x = 1, becomes the geometric distribution (App-51). This is consistent with the fact that the geometric and exponential distributions are discrete and continuous distributions, respectively (App-49). The Gamma distribution is a failure probability density function if failure occurrence is considered to follow the Poisson process. We deal with this issue in D.9, Poisson Distribution.

D.9 Poisson Distribution: fPois(x)

Cosmic rays collide with semiconductor devices used in an artificial satellite completely at random. We cannot expect that there will be no collision for some time since one has just occurred. Similarly, we cannot say that a cosmic ray will soon collide with a semiconductor device because there have been no collisions for a moment.

This is an example of cases in which we can consider that a rare phenomenon will occur with some expectation if the period of observation is sufficiently long or the population to be observed is sufficiently large. Here we assume that the phenomenon does not occur twice or more at the same instant, and further that the probability of the phenomenon occurring is constant. In other words, the MTTF of the phenomenon = θ (or the instantaneous failure rate = λ) is constant. Such a probability process is known as the Poisson process.

If a phenomenon occurs in accordance with the Poisson process with the expectation x, the probability of the phenomenon occurring n times within the time interval $0 < T \leq t1$ is described by the Poisson distribution. Detailed discussions of the Poisson distribution are given below.

Let us determine the probability that the phenomenon occurs in a short moment dt in the time $0 < T \leq t1$. Using reliability functions applicable to times $0 < T \leq t1$ and $0 < T \leq t1 - t$ before and after dt, we obtain

$$R(t) \cdot \frac{dt}{\theta} \cdot R(t1 - t) \qquad \text{(App-60)}$$

Hence the probability $P1\left(\frac{t1}{\theta}\right)$ of the phenomenon occurring once in the time $0 < T \leq t1$ is

$$P1\left(\frac{t1}{\theta}\right) = \int_0^{t1} R(t)\ \frac{dt}{\theta}(t1 - t) = \int_0^{t1} e^{-\frac{t}{\theta}} \cdot \frac{dt}{\theta} \cdot e^{-\frac{t1-t}{\theta}} = \frac{1}{\theta} e^{-\frac{t1}{\theta}} \cdot t1 \qquad \text{(App-61)}$$

The probability $Pn\left(\frac{t1}{\theta}\right)$ that the phenomenon occurs n times within $0 < T \leq t1$ is obtained through repeated calculations of equation

$$Pn\left(\frac{t1}{\theta}\right) = \int_0^{t1} R(t)\ \frac{dt}{\theta} Pn - 1\left(\frac{t1}{\theta}\right) = \frac{1}{n!}\left(\frac{t1}{\theta}\right)^n e^{-\frac{t1}{\theta}} \qquad \text{(App-62)}$$

Eventually, when the expectation $x = \frac{t1}{\theta}$, the Poisson probability density function fPois(x) is

$$\left.\begin{aligned} f_{Pois}(x) &= \frac{1}{n!} x^n e^{-x} \\ \mu &= x, \quad \sigma^2 = x^2 \end{aligned}\right\} \qquad \text{(App-63)}$$

A three-dimensional representation of equation App-64 is shown in Figure D.4 within the range of $1 \leq n \leq 6$ and $0 \leq x \leq 6$. The values of f(x) for representative values in the range of $0 \leq n \leq 39$, and $0.1 \leq x \leq 20$ are shown in the attached table.

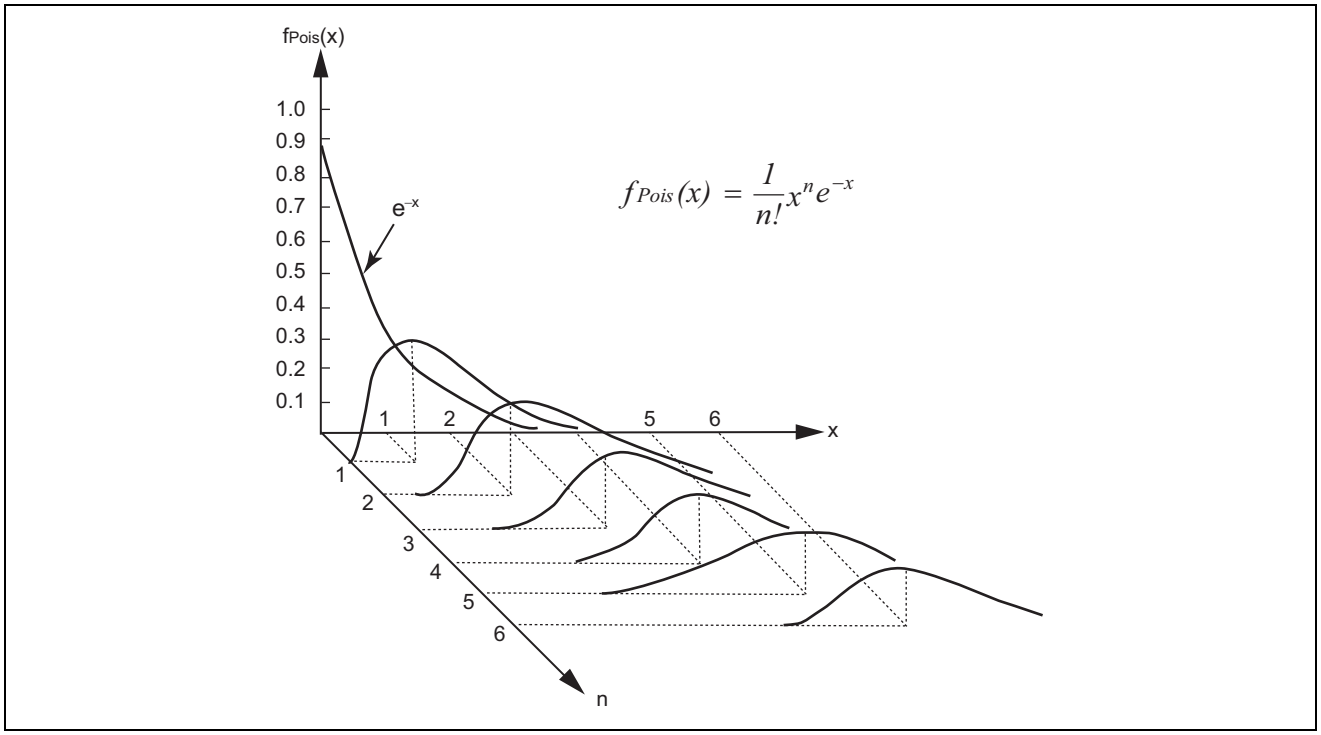


Figure D.4 Three-Dimensional Representation of Poisson Distributions

Let us determine the probability F(t1, k) that failures occur at least k times or more within the time 0 < T ≤ t1 in a Poisson process. This probability is expressed as follows using equation App-62 for the Poisson distribution.

$$F(t1,\ k) = 1 - \sum_{n=0}^{k-1} Pn\left(\frac{t1}{\theta}\right) = 1 - \sum_{n=0}^{k-1} \frac{1}{n!}\left(\frac{t1}{\theta}\right) n_e^{-\frac{t1}{\theta}} \quad \text{(App-64)}$$

In C.2.3, the stand-by redundancy system in Figure C.8 will not fail unless the n switches all fail. Therefore, based on equation App-64, the reliability function R(t) of this stand-by redundancy system is

$$R(t)=1 - F(t,\ k)$$

This equation leads to equation App-21.

If damage causing failure occurs randomly in accordance with the Poisson process, the failure distribution function of the device is equation App-64 assuming that the device breaks from k times or more of damage in the operating time 0 < T ≤ t1. In this case, the failure probability density function becomes equation App-57 for the Gamma distribution.

Using a fixed value, in equation App-64, for the number of damages k received before failure, consider the failure distribution function F(t1, k) as a function of time t1. Based on equation App-3, the failure probability density function f(t1) is

$$f(t1) = \frac{\alpha}{\alpha t1} F(t1,\ k) = \frac{1}{(k-1)!}\left(\frac{t1}{\theta}\right) k - 1_e^{-\frac{t1}{\theta}} = f\Gamma\ (t1,\ x,\ \frac{1}{\theta}) \quad \text{(App-65)}$$

If, on the other hand, only a single damage (n = 1) is fatal to the device, the failure probability density function becomes equation App-46 of the exponential distribution.

The Poisson distribution approximates the binomial probability distribution if the population is large and the phenomenon occurs with a low probability.

The binomial probability distribution should deal with Bernoulli samples, for which the probability p = constant is a premise. In contrast, the Poisson distribution handles phenomenons that the expectation x = Np = constant. It is important to note that N no longer denotes the number of tests of Bernoulli trial due to the approximation of the binomial probability distribution to the Poisson distribution. This process is explained in detail as follows.

$$f_{Bin}(n,\ N,\ P) = \frac{N!}{n!(N-n)!} p^n q^{N-n} = \frac{\left(1-\frac{1}{N}\right)\left(1-\frac{2}{N}\right)\cdots\left(1-\frac{n-1}{N}\right)}{n!} (Np)^n\ q^{N-n} \quad \text{(App-66)}$$

and,

$$logq^{N-n} = (N-n)\ log\ (1-p) = -(N-n) \sum_{k=1}^{\infty} \frac{p^k}{k} = -\left(1-\frac{n}{N}\right)\left(x + \frac{1}{2}\frac{x^2}{N} + \frac{1}{3}\frac{x^3}{N^2} + \cdots\right) \quad \text{(App-67)}$$

$$\therefore \lim_{N\to\infty} logq^{N-n} = -x,\ \lim_{N\to\infty} q^{N-n} = e^{-x} \quad \text{(App-68)}$$

N in these equations is not the number of tests of Bernoulli trial, but serves to indicate that the population size is expanded. Through these steps we obtain

$$\lim_{N\to\infty} f_{Bin}(n,\ N,\ P) = \frac{1}{n!} x^n e^{-x} \quad \text{(App-69)}$$

Thus understanding the Poisson distribution in different ways we can clarify its relations with other probability distributions. This will be illustrated later in appendix E, “Relations of Probability Distributions.”

D.10 Normal Distribution: fNorm(x)

The general character of a population comprising numerous, uniform, and random independent phenomena is expressed by the normal distribution fNorm (x). A typical example of this is the movement of molecules of a classical, ideal gas. (We will not discuss the correctness of this in a strict mathematical sense.)

Expected characteristics of the function fNorm (x) are these: the mean value μ is also the maximum value; the value smoothly decreases from the maximum value in a symmetrical manner; the broadening of the curve about the peak is proportional to the standard deviation σ. Wear-out-failures which almost suddenly outbreak after a certain period approximate the normal distribution.

Let us first examine a simple binomial distribution model to know concretely what the normal distribution expresses.

In the Bernoulli trial, the result of observation is either (1) + σ / $\sqrt{N}$ or (2) −σ / $\sqrt{N}$. The probability of (1) or (2) occurring is equally 1/2. The initial value for starting the trial is 0 and we perform N tests. We obtain n times of 1 and N−n times of (2), then the value x after N tests is

$$x = \frac{\sigma\,(2n - N)}{\sqrt{N}} \qquad \text{(App-70)}$$

This type of binomial distribution model approaches the normal distribution as we make the number of tests N sufficiently large.

$$f_{Bin}(n) = \frac{N!\left(\frac{1}{2}\right)^N}{n!(N-n)!} = \frac{N!\left(\frac{1}{2}\right)^N}{\left(\frac{1}{2}N + \frac{x}{2\sigma}\sqrt{N}\right)!\times\left(\frac{1}{2}N - \frac{x}{2\sigma}\sqrt{N}\right)!} \qquad \text{(App-71)}$$

If N is sufficiently large we can consider that x is a continuous variable. Hence

$$f_{Bin}(n)\,dn \to \phi(x)dx,\; dn \to \frac{\sqrt{N}}{2\sigma}dx \quad (N \to \infty) \qquad \text{(App-72)}$$

Here, ϕ (x) is given by

$$\phi(x) = \lim_{N\to\infty}\frac{\sqrt{N}}{2\sigma}f_{Bin}(n) = \lim_{N\to\infty}\left\{\frac{\frac{\sqrt{N}}{2\sigma}\cdot!\cdot\left(\frac{1}{2}\right)^N}{\left(\frac{1}{2}N + \frac{x}{2\sigma}\sqrt{N}\right)!\times\left(\frac{1}{2}N - \frac{x}{2\sigma}\sqrt{N}\right)!}\right\} \qquad \text{(App-73)}$$

Using Sterling's formula we can write

$$N! \approx \sqrt{2\pi N}\;N^N e^{-N} \qquad N > 10$$

$$\therefore\quad \phi(x) = \lim_{N\to\infty}\left\{\frac{1}{\sigma\sqrt{2\pi}}\frac{1}{\sqrt{1-\frac{x^2}{\sigma^2 N}}}\left(1+\frac{x}{\sigma\sqrt{N}}\right)^{-\frac{N}{2}-\frac{x}{2\sigma}\sqrt{N}}\cdot\left(1-\frac{x}{\sigma\sqrt{N}}\right)^{-\frac{N}{2}+\frac{x}{2\sigma}\sqrt{N}}\right\}$$

$$= \lim_{N\to\infty}\left\{\frac{1}{\sigma\sqrt{2\pi}}\left(1-\frac{x^2}{\sigma^2 N}\right)^{-\frac{N}{2}-\frac{1}{2}}\cdot\left(1+\frac{x}{\sigma\sqrt{N}}\right)^{\frac{x}{2\sigma}\sqrt{N}}\cdot\left(1-\frac{x}{\sigma\sqrt{N}}\right)^{-\frac{x}{2\sigma}\sqrt{N}}\right\} \qquad \text{(App-74)}$$

Here, using the exponential function

$$e^{Z} = \lim_{n\to\infty}\left(1+\frac{Z}{n}\right)^{n}$$

We obtain

$$\phi(x) = \frac{1}{\sqrt{2\pi}} exp\left(-\frac{x^2}{2}\right) \quad \text{(App-75)}$$

$\phi(x)$ is known as the standard normal distribution. The general form of the normal probability density function is

$$f_{Norm}(x) = \frac{1}{\sigma\sqrt{2\pi}} exp\left(-\frac{(x-\mu)^2}{2\sigma^2}\right) \quad \text{(App-76)}$$

By applying equation App-76 to equation App-8, we can calculate the mean value and the variance, which, we can confirm, will be μ and σ^2. The variable y used to convert fNorm (x) to equation App-76 is

$$y = \frac{x-\mu}{\sigma} \quad \text{(App-77)}$$

This is known as the standard normal variable. Figure D.5 shows the typical characteristics of fNorm(x) and $\phi(y)$. In Figure D.5, the following calculations can be made.

$$\int_{\mu-\sigma}^{\mu+\sigma} f_{Norm}(x)\,dx \cong 0.6826\,,\ \int_{\mu-2\sigma}^{\mu+2\sigma} f_{Norm}(x)\,dx \cong 0.9545\,,\ \int_{\mu-3\sigma}^{\mu+3\sigma} f_{Norm}(x)\,dx \cong 0.9973$$

When the value lnX rather than X behaves according to the normal distribution, we have a logarithmic normal distribution. To serve as an example, consider the life L in equation App-33. Let us assume that a given lot of semiconductor devices are storage tested at temperature T. As long as there is no great variation in the quality of this lot, the distribution of the life L as caused by the stress placed on the devices by the temperature T is expressed as a logarithmic normal distribution and should be analyzed as such. Moreover, the logarithmic normal distribution is also used for the analysis of oxide film life by TDDB.

$$f_{log-Norm}(x) = \frac{1}{\sigma x\sqrt{2\pi}} exp\left(-\frac{(InX-InX0)^2}{2\sigma^2}\right) \qquad X>0 \quad \text{(App-78)}$$

Mean value $= e^{InX_0+\frac{\sigma^2}{2}}$, $Variance = e^{2InX_0+\sigma^2}\times(e^{\sigma^2}-1)$

where X0 is the median value of the probability distribution: $\int_0^{X0} f_{log-Norm}(X)dX = \int_{X0}^{\infty} f_{log-Norm}(X)dX$

σ^2 is the variance of the normal distribution.

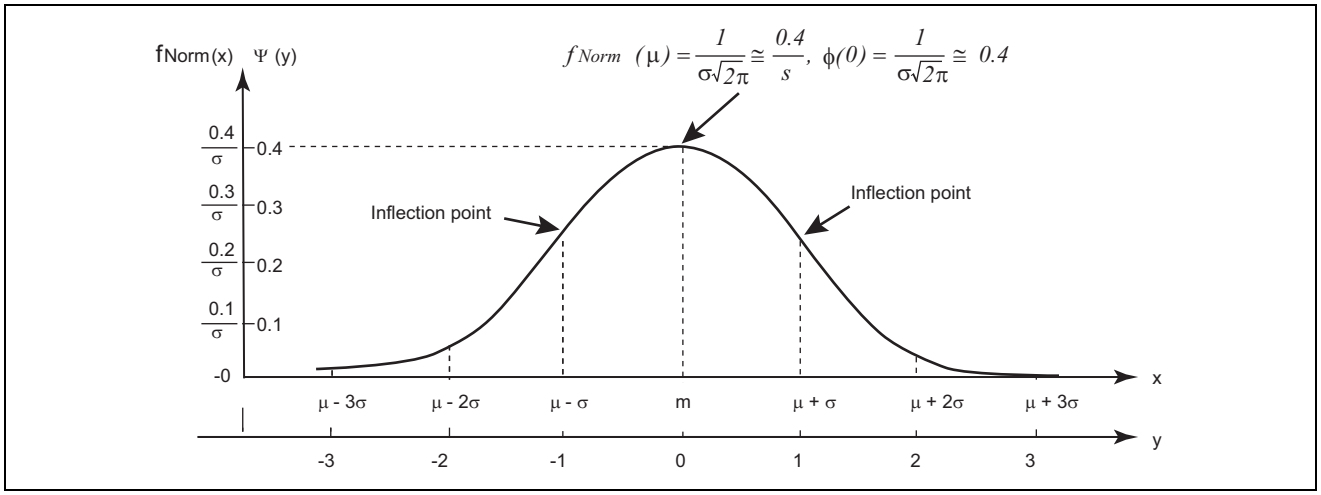


Figure D.5 Probability Density Function of Normal Distribution

D.11 Weibull Distribution: fWbl(t)

A set of n semiconductor devices is subjected to operation life test all together. As time t passes, the failure rate of these semiconductor devices changes. For studying the change, in this model, probabilities of individual devices failing by the time t are uniformly p(t), and the probability that at least one of the n devices will fail is F(t). Reversely the probability that none of the n devices will fail by the time t is R(t), which is, from equation App-4

$$R(t) = 1 - F(t) = \{1 - p(t)\}^n \quad \text{(App-79)}$$

The Weibull distribution characteristically assumes that the n devices are as a lot expressed by the following reliability function.

$$R(t) = \{1 - p(t)\}^n = e^{-\phi(t)} \quad \text{(App-80)}$$

Let us make arrangements to express properly the failure distribution trends that we know through experience in the function form of equation App-80.

We know through experience that no failures occur before a given test time γ and after γ the total number of failed devices increases with time t (or more correctly, maintains a non-decreasing trend). To express this empirically observed fact, ϕ (t) should have the characteristics below.

$$\phi(t) = 0 \quad (0 < t \leq \gamma)$$

$$\phi(t) \geq 0, \ \frac{d}{dt}\phi(t) \geq 0 \ (\gamma < t)$$

Hence we choose the following form of function.

$$\left.\begin{aligned} &\phi(t) = 0 \ (0 < t \leq \gamma) \\ &\phi(t) = \frac{(t-\gamma)^m}{t_0} \ (\gamma < t) \end{aligned}\right\} \quad \text{(App-81)}$$

Therefore,

$$F_{Wbl}(t) = 1 - \{1 - p(t)\}^n = 1 - e^{-\phi(t)} = 1 - exp\left\{-\frac{(t-\gamma)^m}{t_0}\right\} \quad \text{(App-82)}$$

Equation App-82 is referred to as the Weibull failure distribution function.

Equation App-83 of the Weibull distribution has three parameters, m, γ, and t0, which are the shape parameter, position parameter, and scale parameter, respectively. The position parameter γ = 0 if we assume that the probability of failure is already above 0 immediately before testing. From equation App-82 and according to equations App-3 and App-8

$$\left.\begin{aligned} F_{Wb1}(t) &= \frac{m(t-)^{m-1}}{t0}\ exp\left\{-\frac{(t-\gamma)^m}{t0}\right\} \\ \mu &= t0^{\frac{1}{m}}\,\Gamma(1+\frac{1}{m}),\ \sigma^2 = t0^{\frac{2}{m}}\left\{\Gamma\left(1+\frac{2}{m}\right)-\Gamma^2\left(1+\frac{1}{m}\right)\right\} \\ \lambda_{Wb1}(t) &= \frac{m}{t0}(t-\gamma)^{m-1} \end{aligned}\right\} \quad \text{(App-83)}$$

If m = 1, Wbl = 1/ t0 = constant, so the distribution is exponential.

If m > 1, Wbl (t) monotonically increases, representing a wear-out failure mode.

If m < 1, Wbl (t) monotonically decreases, representing an early failure mode.

The function form of the Weibull distribution is capable of representing different failure modes depending on the value of the parameter m. Figure D.6 shows how the form of fWb1(t) changes with various values of m under conditions of γ = 0 and t0 = 1.

When the position parameter γ = 0, equation App-79 of the Weibull reliability function becomes

$$R_{Wb1}(t) = \int_t^\infty f_{Wb1}(t)\,dt = \int_t^\infty \frac{m}{t0}t^{m-1}\,e-\frac{tm}{t0}dt = e-\frac{t^m}{t0} \quad \text{(App-84)}$$

If we take the natural logarithm of equation App-84 twice we obtain

$$In\ \ In\frac{1}{R_{Wb1}(t)} = In\ \ In\frac{1}{1-F_{Wb1}(t)} = m\ In\ \ t - In\ \ t0 \quad \text{(App-85)}$$

Here we rewrite as

$$In\ \ In\frac{1}{1-F_{Wb1}(t)} = Y,\ In\ t = X,\ In\ t0 = h$$

Then equation App-85 becomes

$$Y = mX - h \quad \text{(App-86)}$$

The Weibull chart is a chart in which the value of FWbl(t) being converted into the length $In\ \ In\frac{1}{1-F_{Wb1}(t)}$ is plotted on the vertical axis and time t is plotted on the horizontal axis on a logarithmic scale. The cumulative failure rate FWbl(t) determined from observed data is described by the Weibull distribution. It is represented by a straight line according to the relation expressed by equation App-86. The Weibull chart is useful for analysis of failure mode since observed data are graphed on the Weibull chart in the shape of an linear expression.

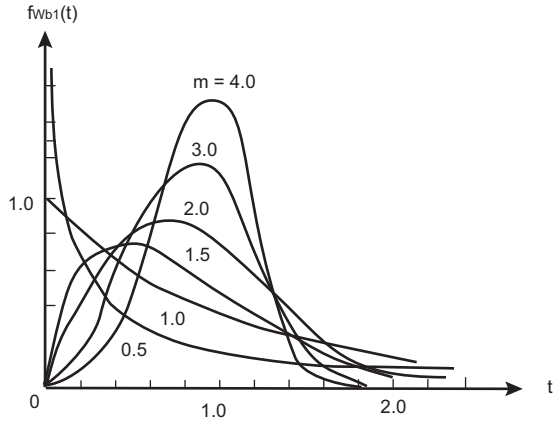


Figure D.6 Weibull Distribution

D.12 Double Exponential Distribution: fd-exp(x)

If $\gamma = 0$ in equation App-84 of the Weibull distribution

$$f_{Wb1}(t) = \frac{m}{t0} t^{m-1} e^{-\frac{t^m}{t0}} \qquad \text{(App-87)}$$

in which, if we perform logarithmic transformation of t so that x = ln t and t = ex, we have

$$f_{Wb1}(t)\,dt = \frac{m}{t0} e^{mx} \cdot e - \frac{e^{mx}}{t0} dx = m e^{mx - lnto} \cdot exp\,(-e^{(mx - lnto)})\,dx \qquad \text{(App-88)}$$

This is the logarithmic transformation of the original distribution. Here we restate

$$m = \lambda,\ lnto = \alpha$$

$$f_{d-exp}(x) = \lambda e^{\lambda x - \alpha} \bullet e^{-e\lambda x - \alpha} \qquad \text{(App-89)}$$

Equation App-89 is known as the double exponential (or extreme value) distribution. Here λ and α are the scale and position parameters, respectively.

$$\mu = \frac{\alpha - \gamma}{\lambda}, \quad \sigma^2 = \frac{\varepsilon^2}{\lambda^2}$$

$$where\ \gamma = Euler's\ constant = 0.577\cdots \quad \varepsilon = \frac{\pi}{\sqrt{6}} = 1.283\cdots$$

When performing reliability tests on devices and subjecting them to stress, the damage incurred by all parts of the device is not necessarily equal. The part of the device which is most susceptible to the applied stress will be the most damaged and will eventually fail. It becomes the determining factor in the life of the device. This occurs in the case of a surge pulse withstand or mechanical impact test. In such a case, stress is applied locally to the device and the life or the withstanding limit of the device depends on its weak point. The double exponential distribution is suitable for analysis of such kinds of phenomena. To simplify equation App-89 we use

$$-y = \lambda x - \alpha \qquad \text{(App-90)}$$

to yield

$$f_{d-exp}(y) = \lambda e^{-y} e^{-e-y} \qquad \text{(App-91)}$$

$$Fd-exp\,(y) = e^{-e-y} \qquad \text{(App-92)}$$

If we take the natural logarithm of this twice, we have

$$1n\ \ 1n\frac{1}{Fd-exp\,(y)} = y = \lambda x\ -\ \alpha \qquad \text{(App-93)}$$

As seen by equation equation App-87 related to the Weibull chart, the observed data can be plotted on extremal probability paper in the shape of a linear expression derived from equation App-93. Thus it is possible to determine the scale parameter λ and position parameter α.

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[2] Hiroshi Shiomi: 3rd edition of Introduction to Reliability Engineering. Maruzen. 1995 (In Japanese)

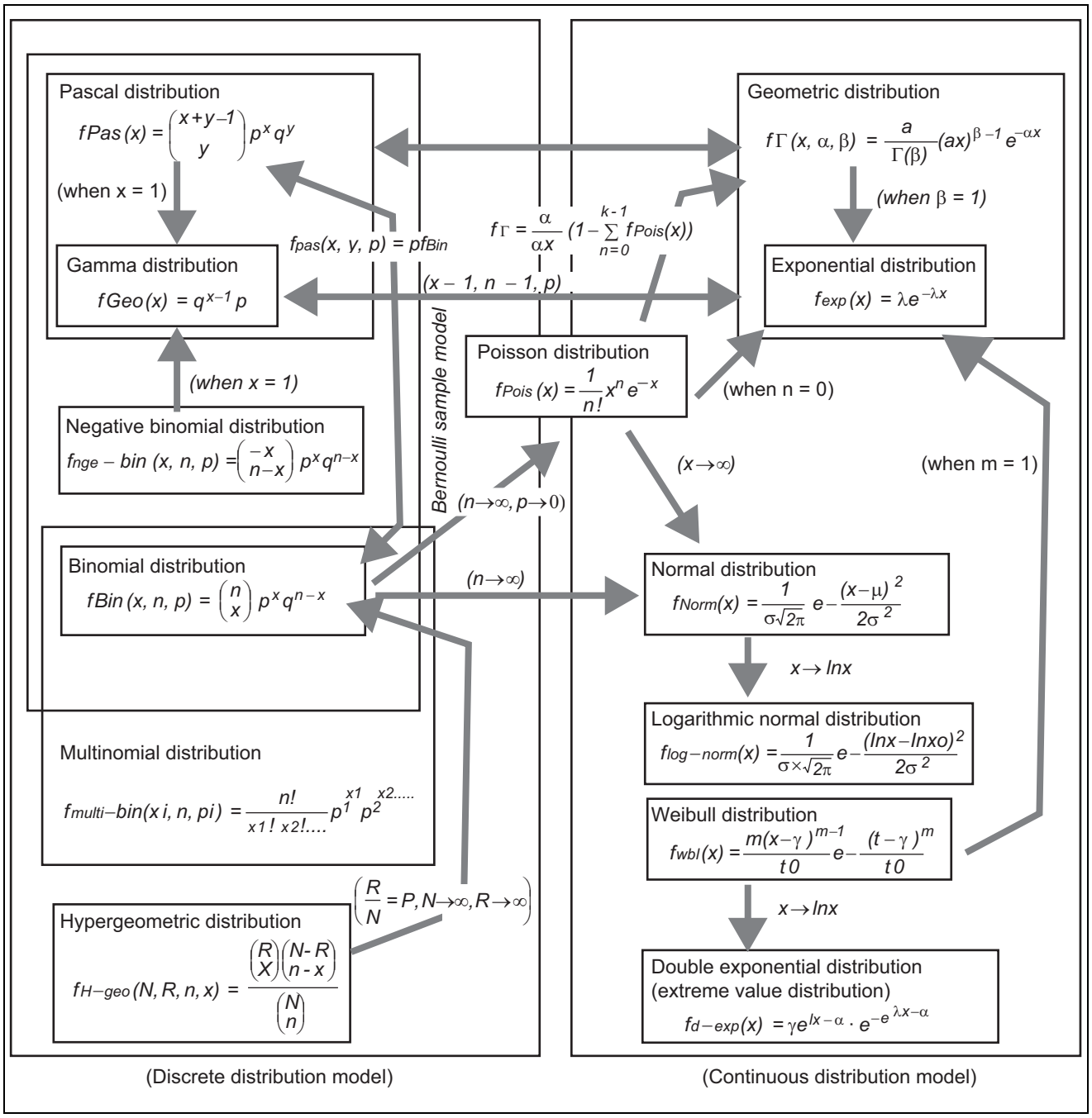
[3] Quality Control, New Edition, Japan Industrial Standards: 1977 (In Japanese)

[4] JUSE Committee for Reliability Probability Paper: “Know-how in Using Probability Paper,” Union of Japanese Scientists and Engineers (1981)

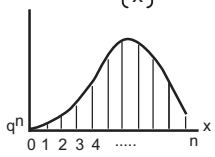
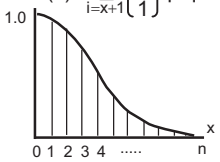
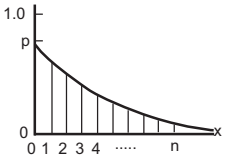
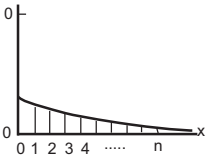
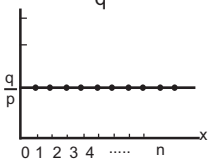
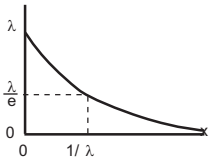
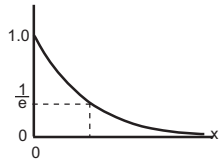
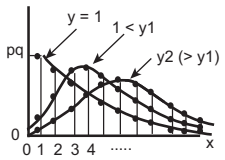
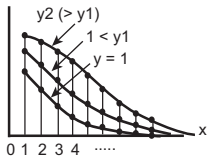
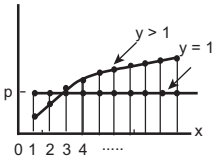
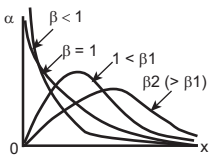
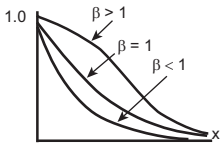
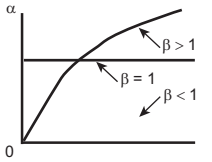
[5] Kimura: “How to Use Probability Plotting Paper,” Ostrich Manufacturing Co. (1976)

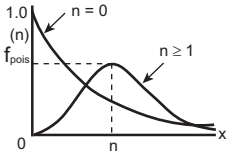
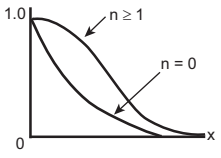
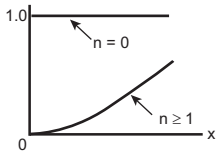
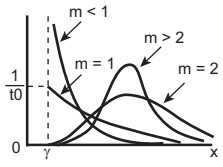
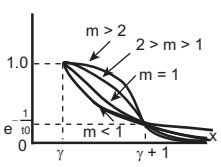
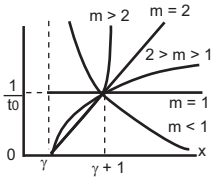
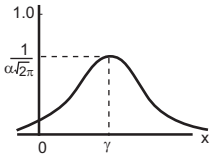
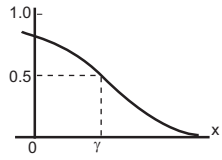
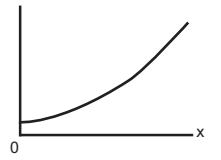
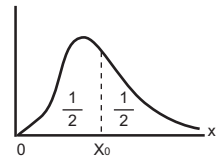
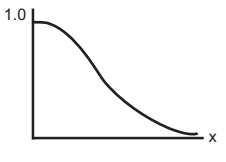
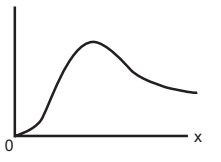
[6] M. J. Howes and D. V. Morgan: “Reliability and Degradation (The Wiley Series in Solid State Devices and Circuits),” A Wiley-Inter Science Publication (1981)

E. Relations of Probability Distributions



F. Probability Functions

Probability Distribution	Probability density function f(x)	Reliability function R(x)	Failure Rate λ(x)	Mean Value μ	Variance σ^2	Remarks
Binomial distribution	$f_{Bin}(x,n,p)=\left(\frac{n}{x}\right)p^x q^{n-x}$ 	$R_{Bin}(x)=\sum_{i=x+1}^{n}\left(\frac{n}{1}\right)p^i q^{n-i}$ 		np	npn	
Geometric distribution	$f_{Geo}(x) = q^x p$ 	$R_{Geo}(x) = q^{x+1}$ 	$\lambda_{Geo} = \frac{p}{q} = const$ 	$\frac{q}{p}$	$\frac{q}{p^2}$	
Exponential distribution	$f_{exp}(x) = \lambda e^{-\lambda x}$ 	$R_{exp}(x) = e^{-\lambda x}$ 	$\lambda_{exp} = \lambda = \text{const}$ 	$\frac{1}{\lambda}$	$\frac{1}{\lambda^2}$	
Pascal distribution	$f_{Pas}(x)=\left(\frac{x+y-1}{y}\right)p^x q^y$ 	$R_{Pas}(x)=\sum_{i=x}^{n-1}\left(\frac{n-1}{i}\right)p^{n-i}q^i$ 	$\lambda_{Pas} = \frac{f_{Pas}}{R_{Pas}}$ 	$\frac{qy}{p}$	$\frac{qy}{p^2}$	
Gamma distribution	(x, α, β) 	$R_\Gamma(x)=\frac{\alpha}{\Gamma(\beta)}\int_x^\infty(\alpha t)^{\beta-1}e^{-\alpha t}dt$ 	$\lambda_\Gamma = \frac{f_\Gamma}{R_\Gamma}$ 	$\frac{\beta}{\alpha}$	$\frac{\beta}{\alpha^2}$	α: Scale parameter β: Shape parameter Refer to Figure D.8

Probability Distribution	Probability density function f(x)	Reliability function R(x)	Failure Rate λ(x)	Mean Value μ	Variance σ^2	Remarks
Poisson distribution	$f_{pois}(x) = \frac{1}{n!}x^n e^{-x}$ 	$R_{pois}(x) = \frac{1}{n!}\int_x t^n e^{-t} dt$ 	$\lambda_{Pois} = \frac{f_{Pois}}{R_{Pois}}$ 	x	x^2	Refer to Figure D.9
Weibull distribution	$f_{wbl}(x) = \frac{m(x-\gamma)^{m-1}}{t0} \bullet e^{-\frac{(x-\gamma)^m}{t0}}$ 	$R_{wbl}(x) = e^{-\frac{(x-\gamma)^m}{t0}}$ 	$\lambda_{Wdl}(x) = \frac{m}{t0}(x-\gamma)^{m-1}$ 	$\frac{1}{t0^m}\Gamma(1+\frac{1}{m})$	$\frac{2}{t0^m}\{\Gamma(1+\frac{2}{m}) - \Gamma^2(1+\frac{1}{m})\}$	m: Shape parameter γ: Position parameter t0: Scale parameter Refer to Figure D.11
Normal distribution	$f_{Norm}(x) = \frac{1}{\sigma\sqrt{2\pi}} e^{-\frac{(x-\mu)^2}{2\sigma^2}}$ 	$R_{Norm}(x) = \frac{1}{\sigma\sqrt{2\pi}}\int_x^\infty e^{-\frac{(t-\mu)^2}{2\sigma^2}} dt$ 	$\lambda_{Norm} = \frac{f_{Norm}}{R_{Norm}}$ 	μ	σ^2	Refer to Figure D.10
Logarithmic normal distribution	$f_{log-norm}(x) = \frac{1}{\sigma x\sqrt{2\pi}} e^{-\frac{(lix-lnxo)^2}{2\sigma^2}}$ 	$R_{log-norm}(x) = \int_x^\infty f_{log-norm}(t)dt$ 	$\lambda_{log-norm} = \frac{fl_{-norm}}{Rl_{-norm}}$ 	$e^{-(lnx0+\frac{\sigma^2}{2})}$	$e^{2lnx0+\sigma2\times(e^{\sigma^2}-1)}$	σ^2: Variance of normal distribution X_0: Medianvalue of probability distribution

REVISION HISTORY	Semiconductor Reliability Handbook

Rev.	Date	Description	
		Page	Summary
1.00	Mar. 21, 2013	—	First Edition issued
2.00	Nov. 25, 2016	xi	Using this Semiconductor Reliability Handbook: Section added.
		1	1. Quality Assurance for Semiconductor Devices: Title corrected.
		4	Table 1.1 Quality Grades for Renesas Semiconductor Devices: Title and description corrected.
		6	1.4 Quality Assurance at Mass Production Stage: Description of quality assurance inspection deleted.
		8	1.5 Change Control: Description corrected.
		11	2.1 Concept of Semiconductor Device Reliability: Description of wear-out failures corrected.
		12	2.2 Dependencies of Failure Rate Function (Bathtub Curve): Failure rate description corrected.
		13	2.2.3 Wear-out Failures: Description corrected.
		24	2.9.1 Fundamental Failure Model (1) Reaction Theory Model: Symbol description deleted.
		32	2.10.2 Example of Predicting the Random Failure Rate (Method of Estimating a Failure Rate at a 60% Confidence Level): Recommendation to refer to references added.
		48	3.2.1 Time Dependent Dielectric Breakdown (1) Failure Phenomena: Formulas corrected.
		53	3.2.3 NBTI (Negative Bias Temperature Instability) (1) Failure Phenomenon: Formulas corrected.
		55	3.2.4 Electromigration: Formulas corrected.
		61	3.2.7 Reliability of Non-Volatile Memory (2) Failure Mechanisms: Description deleted.
		62	Figure 3.32 Phase Diagram for Au-Al Alloy: Figure corrected.
		72	3.3.6 Moisture Resistance of Resin Mold Semiconductor Devices (3) Conditions for Practical Use and Acceleration: Formulas corrected.
		78	3.4.1 Cracks of the Surface-Mounted Packages in Reflow or Flow Soldering (5) Summary: Cautionary notes corrected.
		87	3.5.1 Electrostatic Breakdown and Electrical Overstress Breakdown (4) Actual Discharge and Test Methods (b) Machine Model Test Method: Description added
		96	3.5.3 Power MOS FET Damage (4) Secondary Breakdowns in Power Transistors: Description corrected.
		155-226	5. Basic Recommendations for Handling and Using Semiconductor Devices: Title and description corrected.
		263, 264	C.4.2 Cumulative Hazard Paper (d) Usage: Figure C.19 and Figure C.20 transposed.
2.50	Jan. 30, 2017	—	Notice: Amended.

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