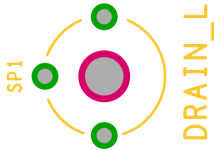
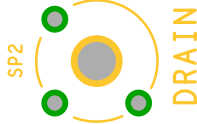
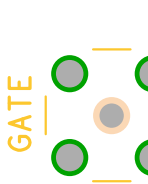
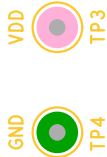




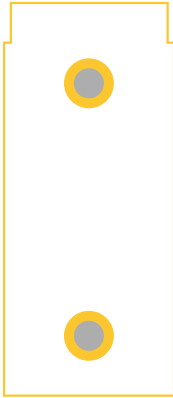
ISL70040SEH: Low Side GaN
FET Driver
ISL70020SEH: GaN FET



DRAIN_L



DRAIN



GND / SRC

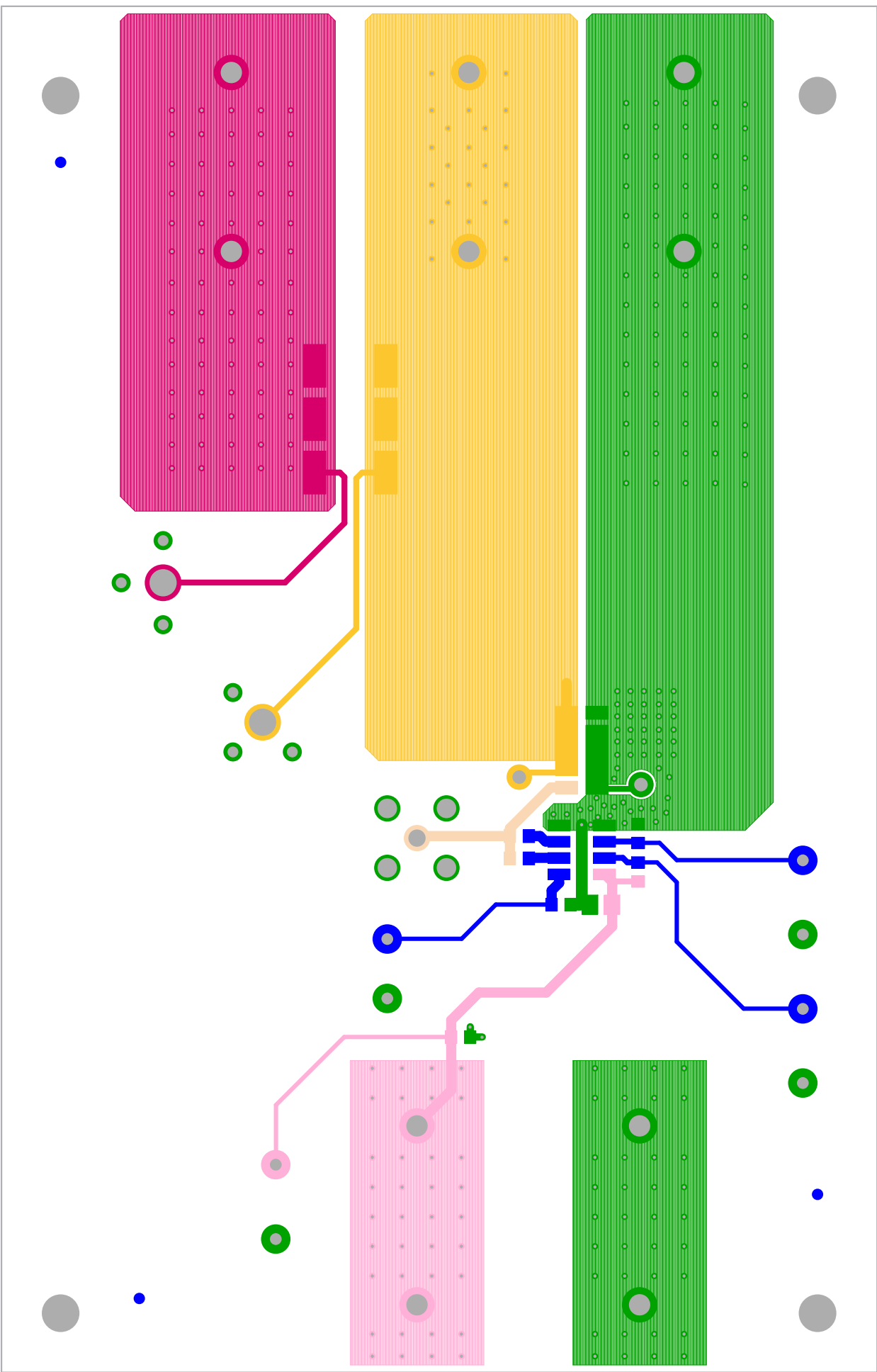


ISL70040SEHEV5Z REV.A

SILK SCREEN TOP

INTERSil CORPORATION

07-26-2019

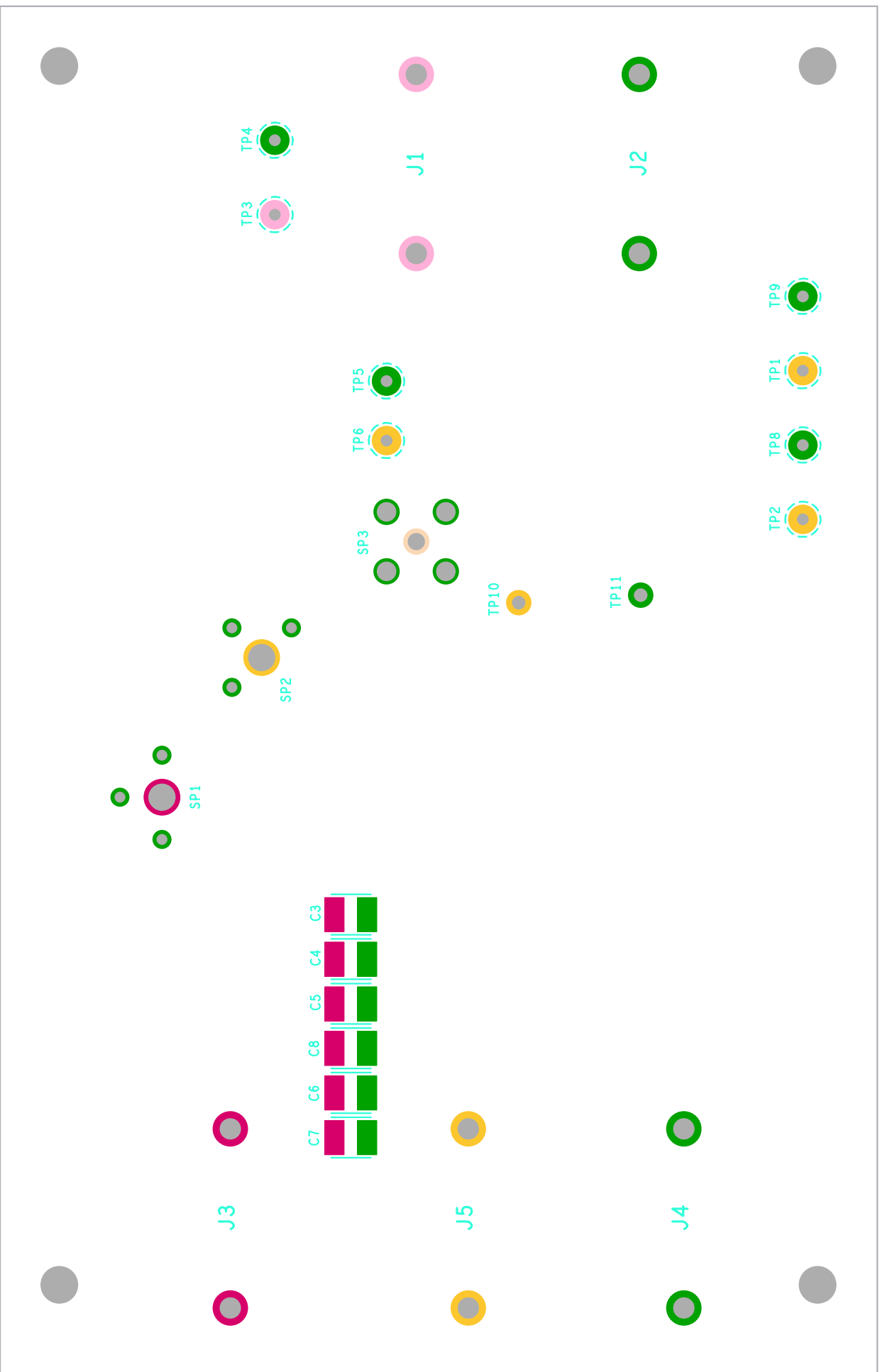


BOTTOM LAYER SOLDER SIDE
INTERSIL CORPORATION
07-26-2019



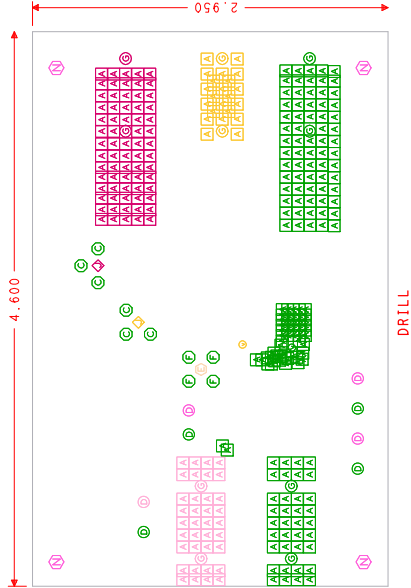
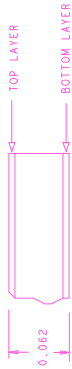
07-26-2019

01-S6-S010
INTERMIT COBORATION
2ITK SCREEN BOTTOM



01-50-5010
INTERIT CORPORATION
ASSEMBLY BOTTOM

	C3
	C4
	C5
	C8
	C6
C7	



DRILL CHART: TOP to BOTTOM			
ALL UNITS ARE IN MILS			
FIGURE	SIZE	PLATED	QTY
A	12.0	PLATED	287
C	37.0	PLATED	6
D	40.0	PLATED	8
E	46.0	PLATED	2
F	59.0	PLATED	1
G	67.0	PLATED	4
H	72.0	PLATED	10
I	93.0	PLATED	2
N	128.0	NON-PLATED	4

NOTES:

1. THIS BOARD IS RoHS COMPLIANT.
2. PRINTED WIRING BOARD DESIGN AND ACCEPTANCE CRITERIA SHALL BE IAW WITH THE REQUIREMENTS OF IPC-D-275 AND IPC-A-600.
3. MATERIAL: FR4 (RoHS COMPLIANT), 2 OZ COPPER.
4. APPLY SOLDER MASK. BOTH SIDES OVER BARE COPPER IAW IPC-SM-840. CLASS 2 (LPI) (BLUE MASK).
5. ALL PATTERNS ARE VIEWED FROM THE PRIMARY SIDE LOOKING THROUGH THE BOARD.
6. UNLESS OTHERWISE SPECIFIED ALL HOLE DIAMETERS ARE AFTER PLATING.
7. APPLY SILKSCREEN USING WHITE NON-CONDUCTIVE EPOXY BASED INK.
8. PWB MUST BE 100% ELECTRICALLY TESTED FOR SHORTS AND CONTINUITY. USE NETLIST PROVIDED ISL70040SEHEV5ZA_IPC356_IPC IAW IPC-D-356.
9. MARK DATE CODE AND MANUFACTURES IDENTIFICATION ON SOLDER SIDE PER IPC-6011 AND IPC-6012.
10. TOLERANCE ON ALL DRILL HOLES SHALL BE IAW IPC-D-2221 & 2222 UNLESS OTHERWISE SPECIFIED.

Drawn By: Tim Klemann	Date Drawn: 07/12/2019	Engineer: Kiran Bernard
Released By:	Date Released:	ISL70040SEH EVALUATION BOARD LAYOUT
Updated By:	Date Updated:	
MASK#		REV. A
HQR ID		
FILENAME: ~/ISL70040SEH/ISL70040SEHEV5ZA		
SHEET 1 of 1		

intersil
A Renesas Company