RENESAS   82P33714/33814 Evaluation Board

Introduction

The 82P33714/33814 evaluation board is designed to help the customer evaluate the IDT82P33714 and IDT82P33814 devices. This user guide will accomplish the following:

- Introduce the board on its power supply and jumper settings
- Describe the input and output connectors for normal operation
- How to bring up the board by using Timing Commander software GUI
- How to configure and program the board to generate standard-compliant frequencies

Board Overview

Use Figure 1 to identify various components of the board: Input and output SMA connectors; Power supply jacks and some jumper settings necessary for the board operations. Detailed descriptions are as follows:

- **Input SMA Connectors –** There are a total of 6 inputs, of which IN5 and IN6 are single-ended inputs; IN1, 2, 3, 4 are differential inputs.
- **Output SMA Connectors** – There are a total of 10 outputs, of which OUT1, 2, 7, 8, 9, 10 are single-ended outputs; OUT3, 4, 5, 6 are differential outputs. MFR_2K_1PPS and MFR_8K_1PPS are single-ended outputs providing 2KHz and 8KHz frame sync signals, respectively.
- **USB connector –** Type-B connector for GUI communications. No power is drawn from USB connector other than to power the FTDI USB chip.
- **Dip Switch SW6 –** Used to configure EEPROM write protection, master or slave selection and communication protocols between PC/GUI and the board. For typical I^2C mode, set MPU_MODE[1:0] = 00 ('I2C ON').
- **J76 –** This is a 2x12 pin header used to set communication mode between the PC and the board. Table 1 shows how to jump the header pairs for the intended mode. By default, I^2C mode will be selected with JP18 shunted (jumped).

Table 1:   Using the J76 Header to Set the Communication Between the PC and the Board

FTDI SPI	Aardvark SPI/I2C	FTDI I2C	Motherboard SPI/I2C	FTDI UART	FTDI to Aardvark
3-4 Jumper	1-3 Jumper	3-4 Jumper	3-5 Jumper	4-6 Jumper	1-2 Jumper
9-10 Jumper	7-9 Jumper	9-10 Jumper	9-11 Jumper	9-10 Jumper	7-8 Jumper
15-16 Jumper	13-15 Jumper	14-16 Jumper	15-17 Jumper	15-16 Jumper	13-14 Jumper
21-22 Jumper	19-21 Jumper		21-23 Jumper		19-20 Jumper

Figure 1. Board Overview
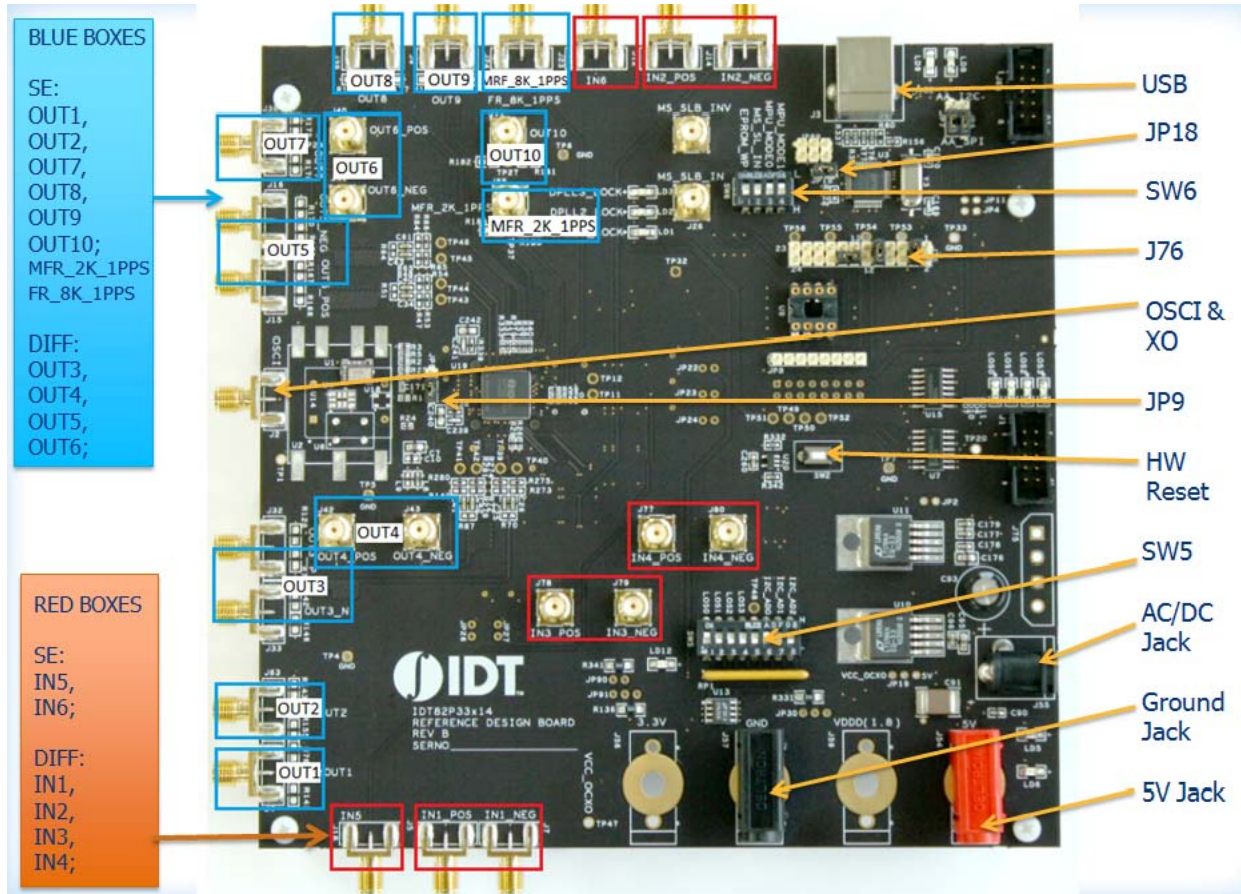
- **OSCI Input and XO –** System reference clock input. Refer to JP9 for clock source selection. The frequency of this input clock is selected by XO_FREQ[2:0] pins described in SW5.

- **HW Reset button –** Pressing this button will reset the device to default condition.

- **JP9 –** 3-pin header used to select the system reference clock to be from OSCI (jump UP) or XO (jump DOWN). Jumper default position is to jump DOWN to select XO.

- **Dip Switch SW5 –** This dip switch contains the following bit configurations:

  ○ **Input clock validation control LOS[3:0]**: Once these bits are set, the input clocks will be disqualified (invalid). Please note: there are other criteria for an input clock to be invalid.

  ○ **I²C address bits:** I2C_AD[2:1] sets the lower 3-bit address of 7-bit I2C address with the least significant bit, I2C_AD0 being ignored. Higher 4 bits is fixed at 4'b1010. This only applies to I²C mode (MPU_MODE[1:0] = 00 in SW6).

- **AC/DC Power Jack –** Using a wall adapter AC/DC power supply (output 5VDC/3A with center-positive jack) can power the board, if 5VDC Power Jack is not supplied with a 5VDC power source.

- **5VDC Power Jack –** If AC/DC power source is not used, a 5VDC power source can be plugged into the jack to power the board. Please note: Power Jacks labeled 3.3V and 1.8V are for other purposes. They can be left unused.

- **5VDC Ground Jack –** Paired with 5VDC Power Jack (above) to provide power return when 5VDC bench power supply is used.

Board Power Supply

There are two ways to power up the board:

- Use an AC/DC adapter which provides 5VDC to on-board voltage regulators to generate 3.3V and 1.8V.
- Connect a 5VDC power source (i.e., a bench power supply) to the power jack that is labeled s "5V".

USB connector is only used for communicating with the PC running Timing Commander. It is not used to provide any power source for the board. When plugged in to the PC's USB port, a green LED is lit.
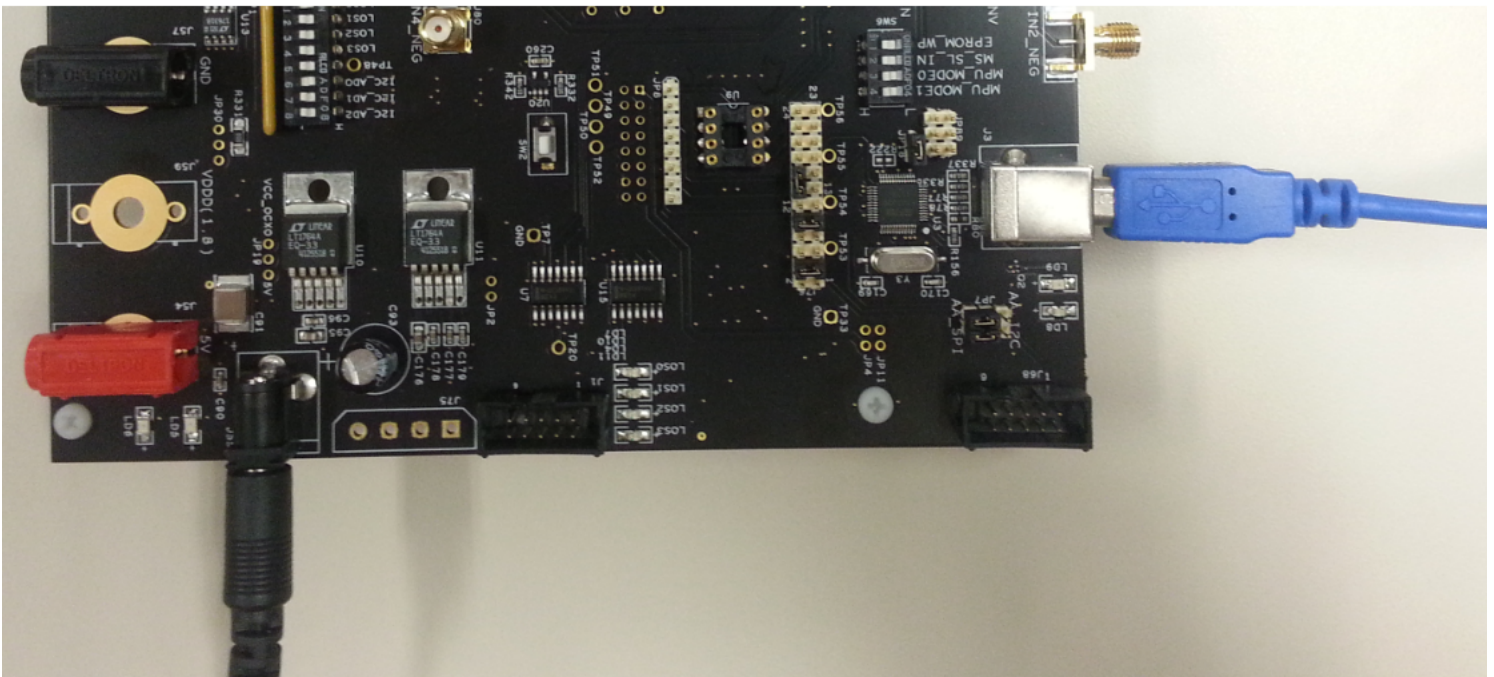
Connecting the Board

Other than input and output cables, the only connection you need to make to operate the board is a USB cable connecting to a PC USB port and a power supply connection (either an AC/DC adapter or a 5VDC power source, as described above). See Figure 2 below for different powering options.

Figure 2.   Connecting the Board to the Power Supply and USB Port
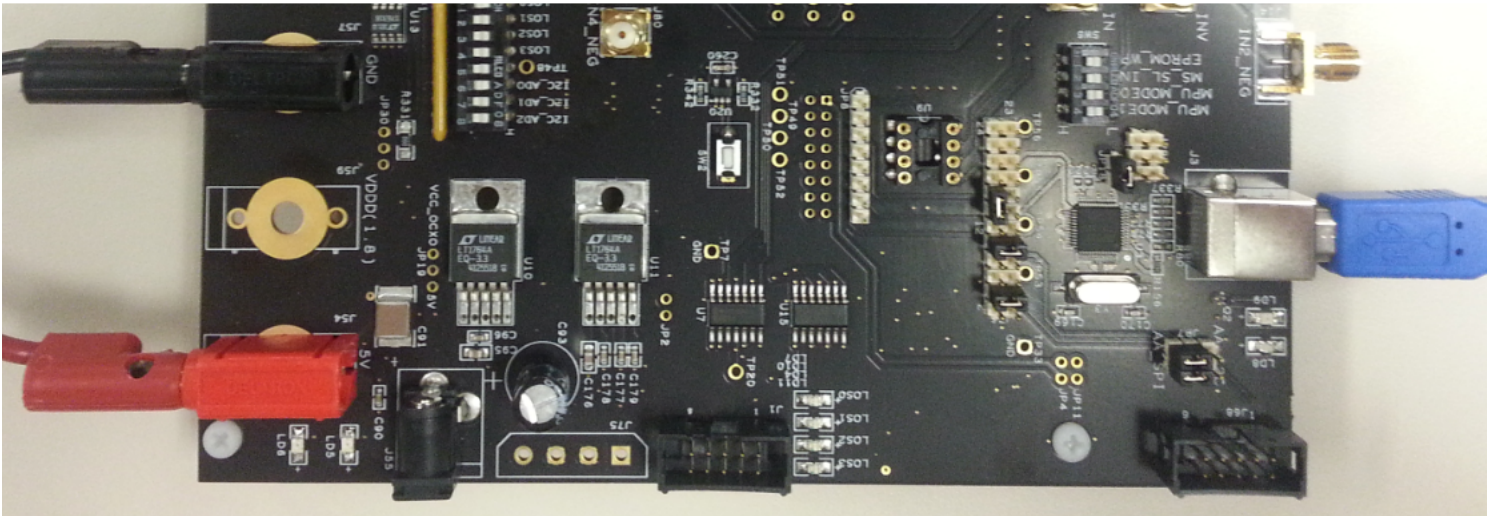
Board Default Frequency Output

Upon power-up, the following default frequencies will be available:

- OUT1 = 25MHz
- OUT2 = 125MHz
- OUT3 = 156.25MHz
- FRSYNC_8K_1PPS = 8kHz
- MFRSYNC_2K_1PPS = 2KHz

Working with TimingCommand for Configuration

Use the following steps to setup the board using I^2C and start the configuration of the board.

1. Connect the board as shown in Figure 2.

2. Press HW Reset button on the board to reset the device. This may not be necessary if the board is first powered up.

3. Start Timing Commander® software. You will see options of "New Setting File" and "Open Setting file". For a new configuration, select "New Setting File".

Figure 3. Starting up Timing Commander GUI

4. After selecting "New Settings File", a device selection window will pop up. In the window, choose the intended device in the list, click the button at the lower right corner of the window to browse and open a personality file, then click OK.

Figure 4. Selecting the Correct Device – 82P33814 is Selected. Open a Personality File
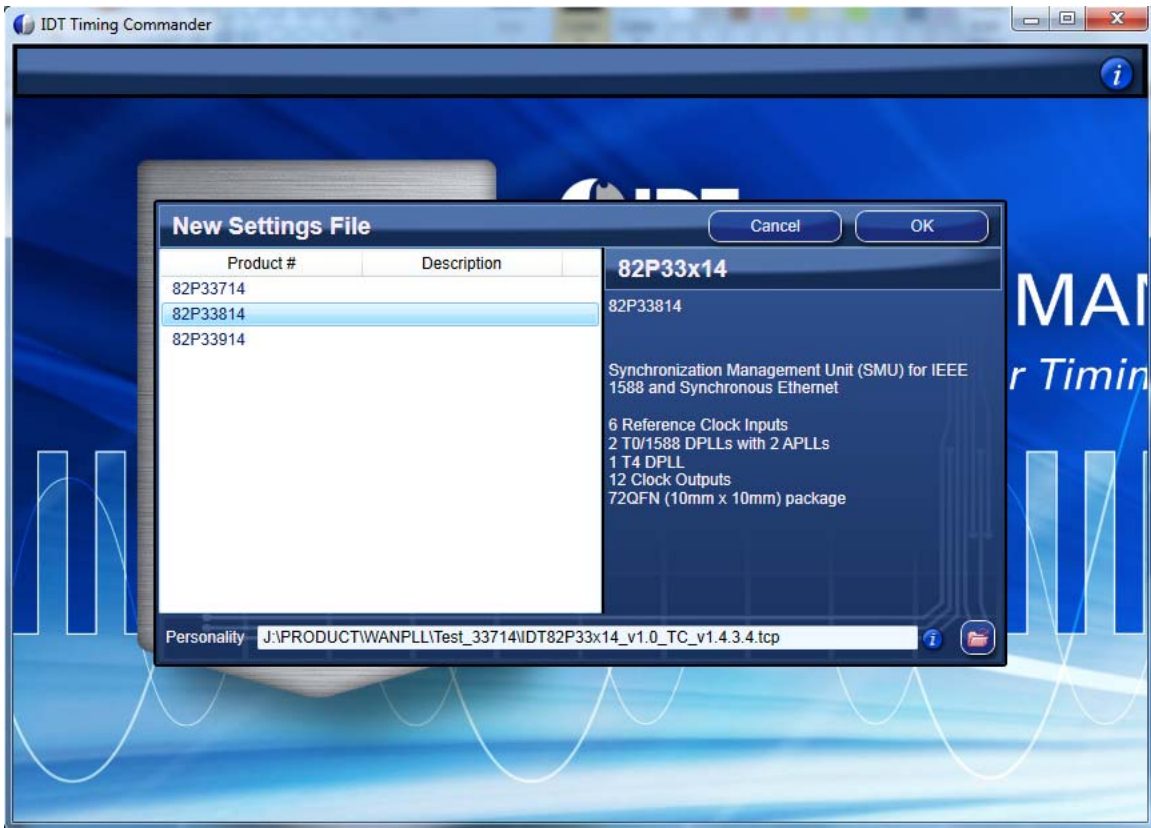
5. The GUI window is open for configurations. Overall, the configuration window shows 6 inputs on the left and 10 outputs are on the right side of the window. For Input configuration, most frequencies can be entered for IN01 ~ IN6 and they will be automatically configured to be available to both DPLLs.

For each frequency entry, click outside the entry box for it to take effect. In the example shown in Figure 5, 10MHz is entered in IN02. As you can see, IN02 is divided down to 8kHz and is available to all 3 DPLLs (if all 3 DPLLs are enabled).

**Figure 5. Enter Input and Output Frequencies**
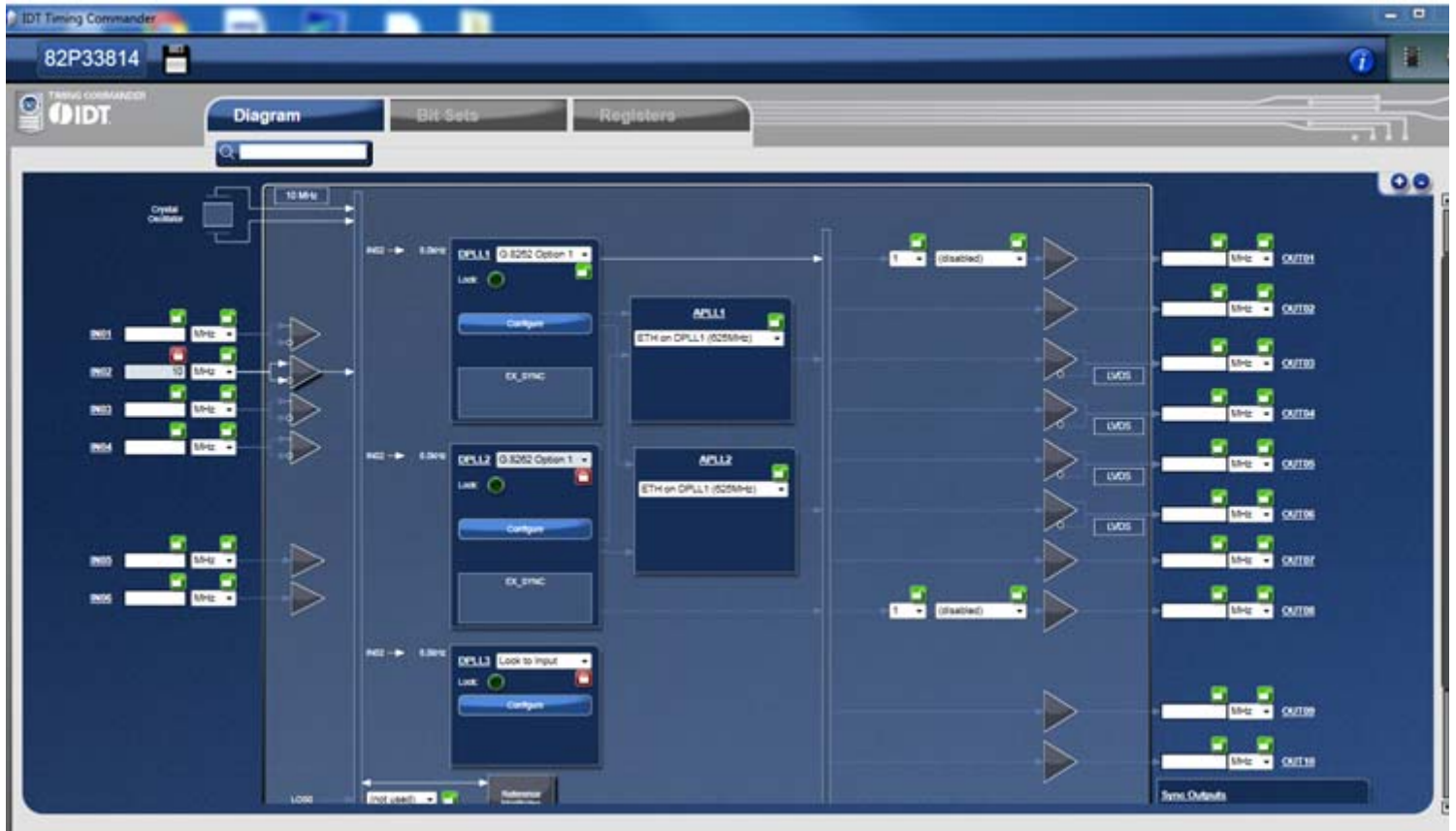
To associate an input clock with a sync signal (such as 1PPS, for e)xample, to associate a sync signal IN1 (1PPS) to IN02 (10MHz)), click on the Input Buffer of IN02 (the triangle symbol following frequency entry box), a sub-configuration window for IN02 is shown below. In the window, IN01 is selected as sync signal.

Figure 6. IN01 is Selected as Sync Signal for IN02 (green oval)
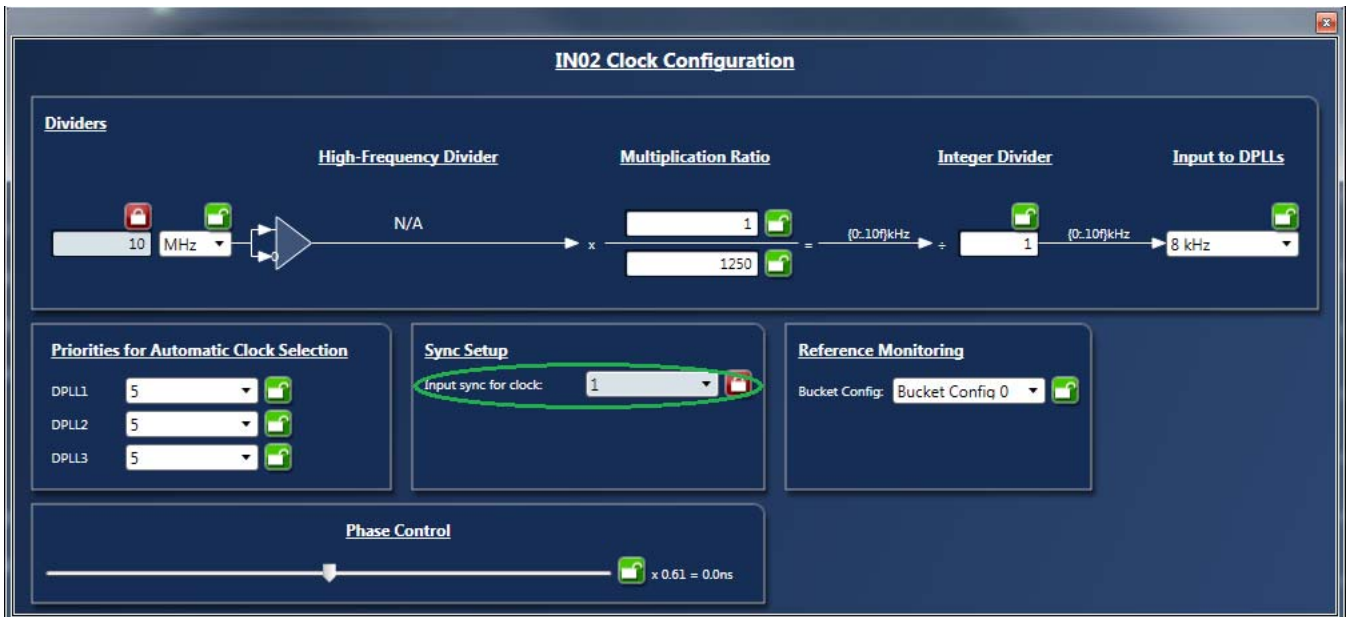

If IN10 is only used as a sync signal for IN09, then disable IN10 to the DPLL as an input in the Input Buffer window of IN10, as shown in Figure 7 below.

Figure 7. IN01 is Disabled as an Input Clock to DPLL (orange oval) because it's only used as a sync signal for IN02
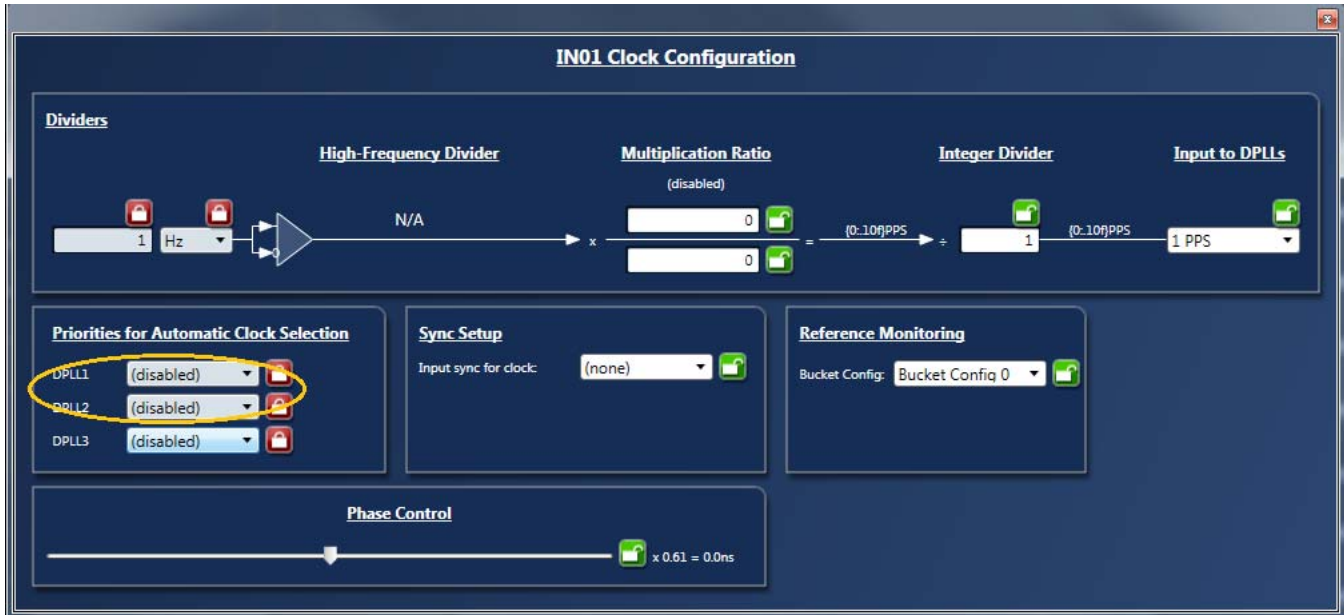
6. Each DPLL has Profile Selection and a "Configure" button. In general, the pull-down Profile Selection should be sufficient to automatically pre-configure the DPLL and reference monitor for the specific ITU-T recommendation. Click "Configure" button to open up configuration window for respective DPLL for additional or customized configuration. There are pull-down items for each configuration parameter. For example, in "Operation Mode" section, you can select:

   ○ Automatic, or Free-up to force Lock or Free-run;

   ○ Different base frequencies can be selected from pull-down items in Selector A or Select B;

   ○ Input reference can be set manually set to a particular input, or set it in "Automatic" mode, in which case an input reference is selected based on priority among multiple input references;

   ○ Feedback can be "Internal feedback mode" or use one of the input references as an "external feedback mode". When in external feedback mode, a clock source must be supplied to the input chosen at the same frequency as the input to the DPLL (typically, it is 8kHz).

**Figure 8. DPLL Configuration Window – Operation Mode Settings**
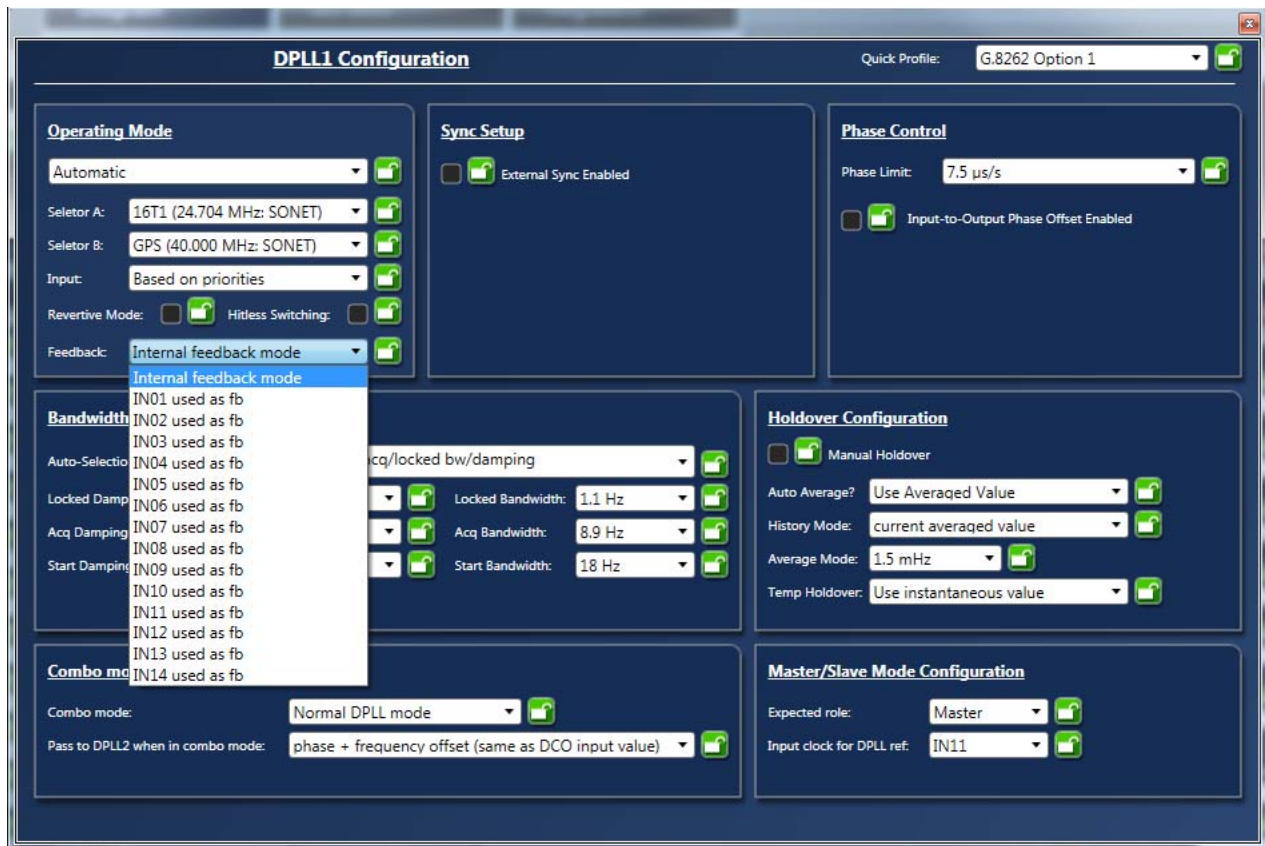
In "Bandwidth and Damping" section, there are two options to select DPLL's bandwidth and damping factors during start, acquisition and locked phases:

- Always use Locked bandwidth/damping. This option will use the bandwidth and damping factor that are available when DPLL is locked;

- Automatically select start/acq/locked bw/damping: preset bandwidth and damping factor values are used for the DPLL during start, acquisition and locked phases.

Figure 9. DPLL Configuration Window - Bandwidth/Damping Factor Settings
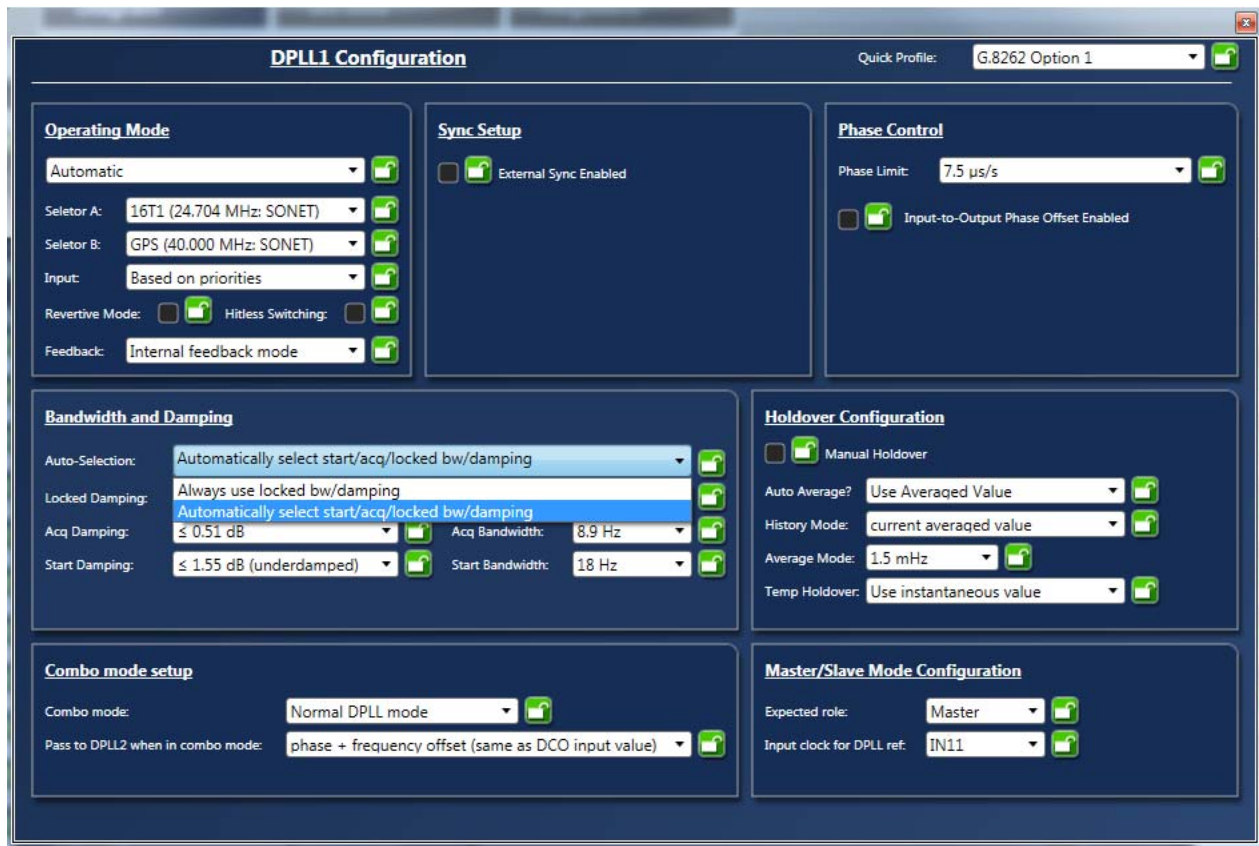
7. **Output Configuration.** Most output frequencies can be entered for OUT01~OUT11 and they will be automatically configured. However, 19.2MHz and 10MHz-based clocks are not supported by the default hardware profiles for the APLLs. Therefore, APLL1/APLL2 needs to be pre-configured to the applicable VCO frequency.
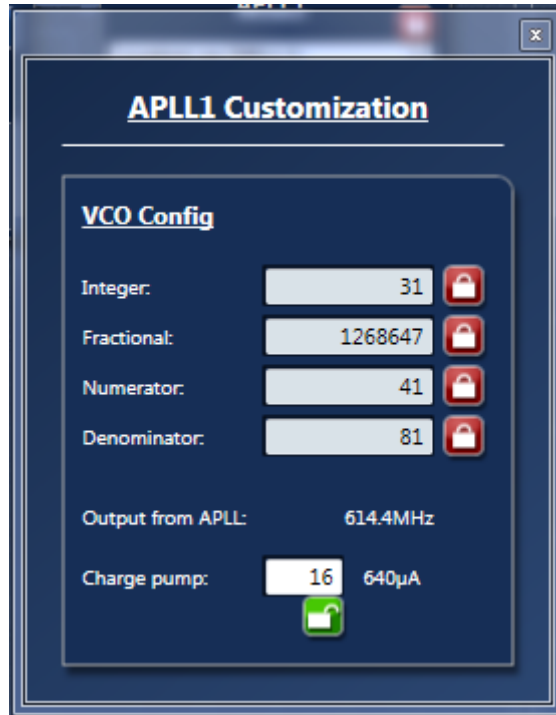
   ◦ To configure APLL1, select "(custom on DPLL1)" as shown in Figure 10.

Figure 10. APLL1 Parameters for VCO = 614.4MHz

Click on the "Customize" button and ignore the initial Timing Commander error. Enter the values as shown in Figure 11 below to get a VCO of 614.4MHz.

Figure 11. APLL1 Parameters for VCO = 614.4MHz

- ○ To configure APLL2, select "(custom on DPLL1)" as shown in Figure 10. Then click on "Customize" button and ignore the initial Timing Commander error. Enter the values as shown in Figure 12 below.

Figure 12. Configure APLL2 Parameters for VCO = 600.0MHz
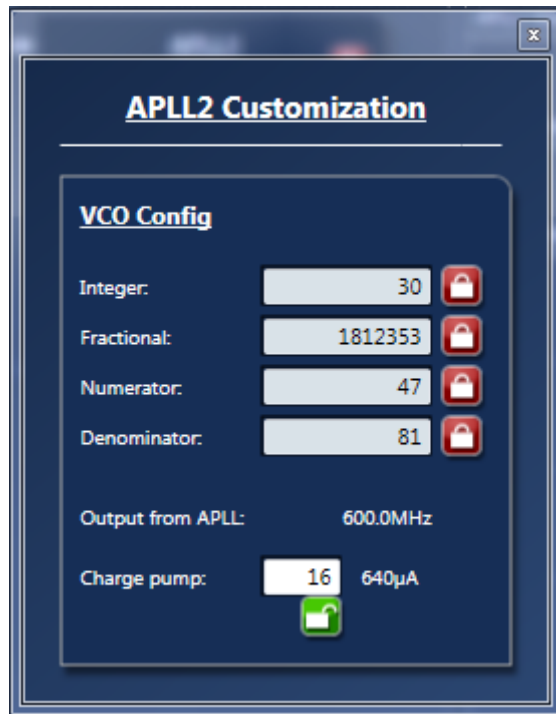
- ○ Once APLL1 and APLL2 have been configured, output frequencies can now be entered at OUT01 ~ OUT04, OUT07.

Figure 13. Output Frequencies Entered after APLL1/APLL2 Configured (example)
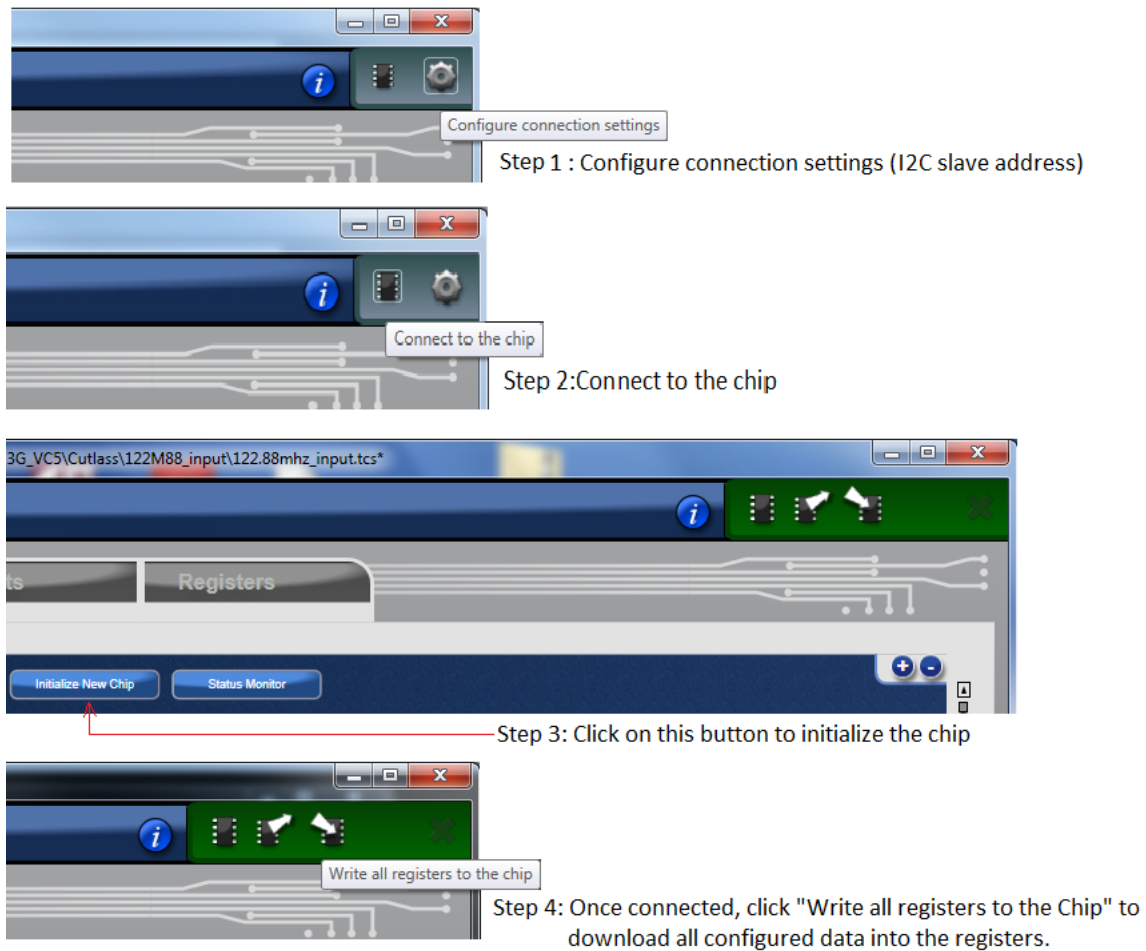

- ○ Finally, FRSYNC & MRFRSYNC can be configured, if needed. Change FRSYNC & MFRSYNC to 1PPS. By default, the duty cycle of sync outputs is 50/50. If a pulse is desired, click on the applicable check box. The pulse width is based on OUT01 clock period.

### Figure 14. Configure MRSYNC and MRFRSYNC

8. **Connecting to the Board**. Configurations can be done before making the USB/I^{2}C connection to the board. Or, connecting with the board can be established before configuring. It's recommended to complete initial configurations before making a USB/I^{2}C connection to the board and write registers into the chip. **Note:** after the board connection is established, any changes to the settings will be automatically written to the respective registers. Follow the steps below in Figure 15 to make a connection to the board.

Figure 15. Steps to Making Connections to the Board

Step 1 : Configure connection settings (I2C slave address)

Step 2: Connect to the chip

Step 3: Click on this button to initialize the chip

Step 4: Once connected, click "Write all registers to the Chip" to download all configured data into the registers.

9. For each DPLL, there are several frequency profiles to choose from by pull-down menu. These frequency profiles are (see Figure 16 below).

   ○ G.8262 Option 1: to configure the DPLL for SyncE for Europe

   ○ G.8262 Option 2: to configure the DPLL for SyncE for NA/Japan

   ○ G.8263: to configure the DPLL for PEC-S-F, which occurs when typically a IEEE-1588 algorithm is controlling the DCO with frequency offsets

   ○ G.8273.2: to configure the DPLL for T-BC (Telecom Boundary Clock), which occurs when a IEEE-1588 stack is directly controlling the DCO with phase offsets. It also puts the DPLL in combo mode to synchronize to the other PLL running G.8262-Option 1 profile

   ○ Lock to 1Hz: to configure the DPLL for GPS application and locking to 1PPS only.

   ○ Wideband: to configure the DPLL to operate in line card mode or lock to a 10MHz + 1PPS from GPS

Figure 16. Frequency Profiles for DPLL
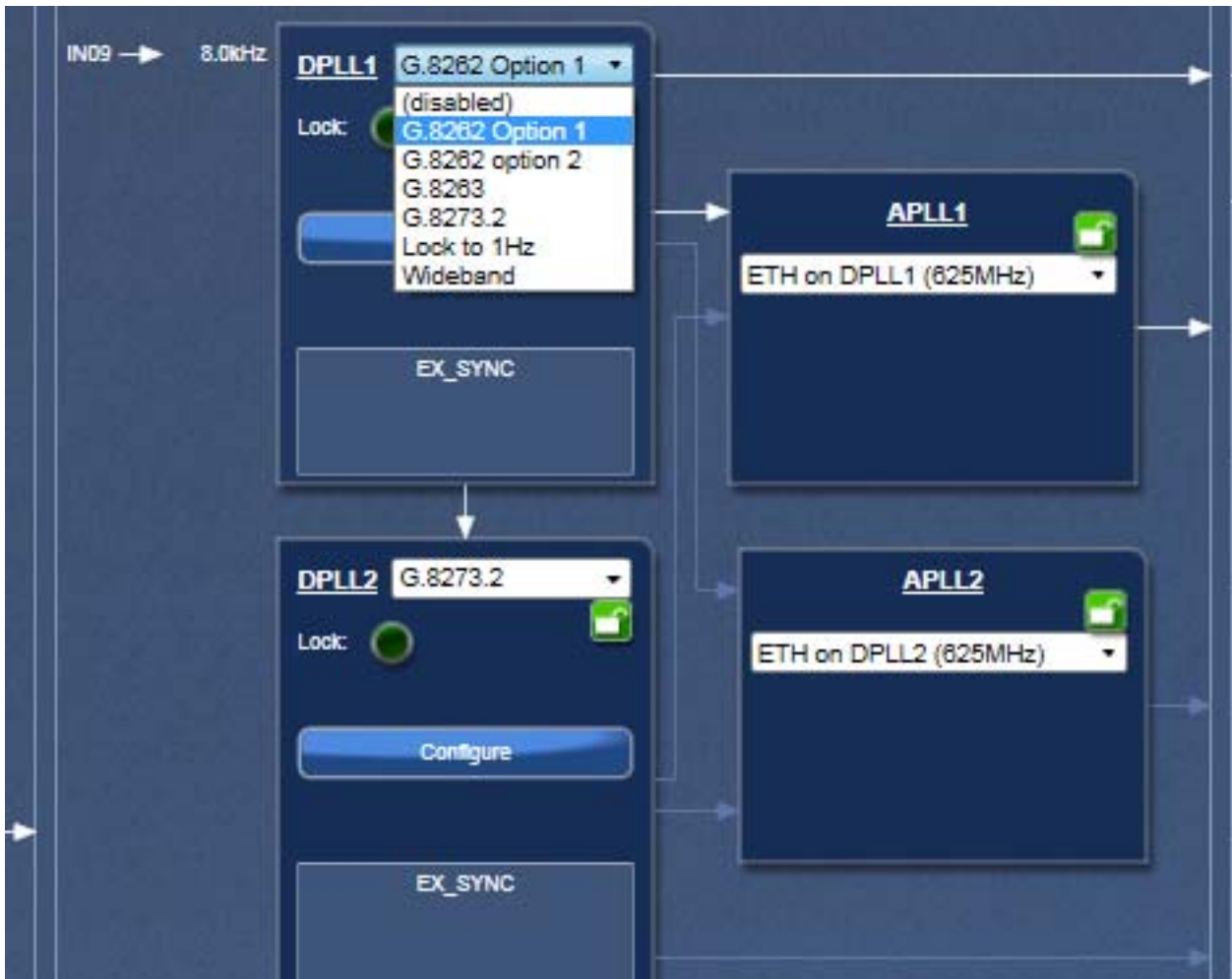
10. Viewing Status – After writing all registers, with configured input reference clocks available, the PLL is supposed to lock to the reference clock. The PLL operation status can be updated and viewed by clicking "View Status" button in GUI window. The status window looks like the following (Figure 17). Enabled input reference clock will show with a lit LED. Frequency offset will also be shown. Locking status of the DPLL will be indicated as "Locked" or otherwise as "Free-run" or "Holdover". The frequency and phase offset of the output clock with respect to the input reference will be indicated.

Figure 17. DPLL Status Window

Figure 17. DPLL Status Window
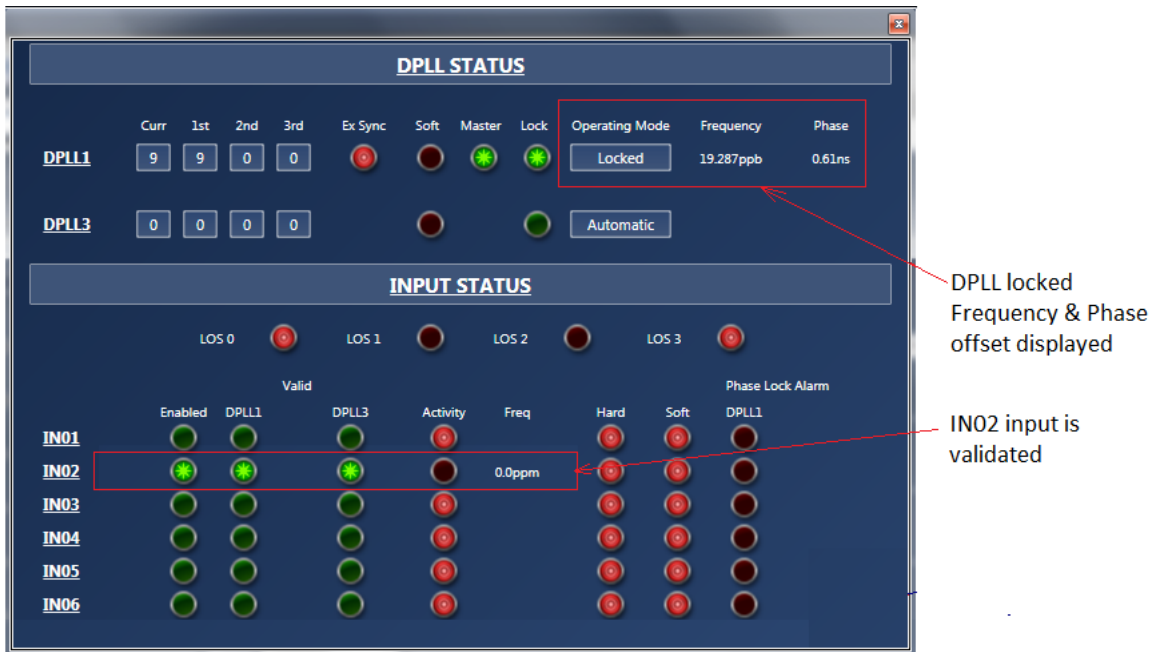
Board Schematics

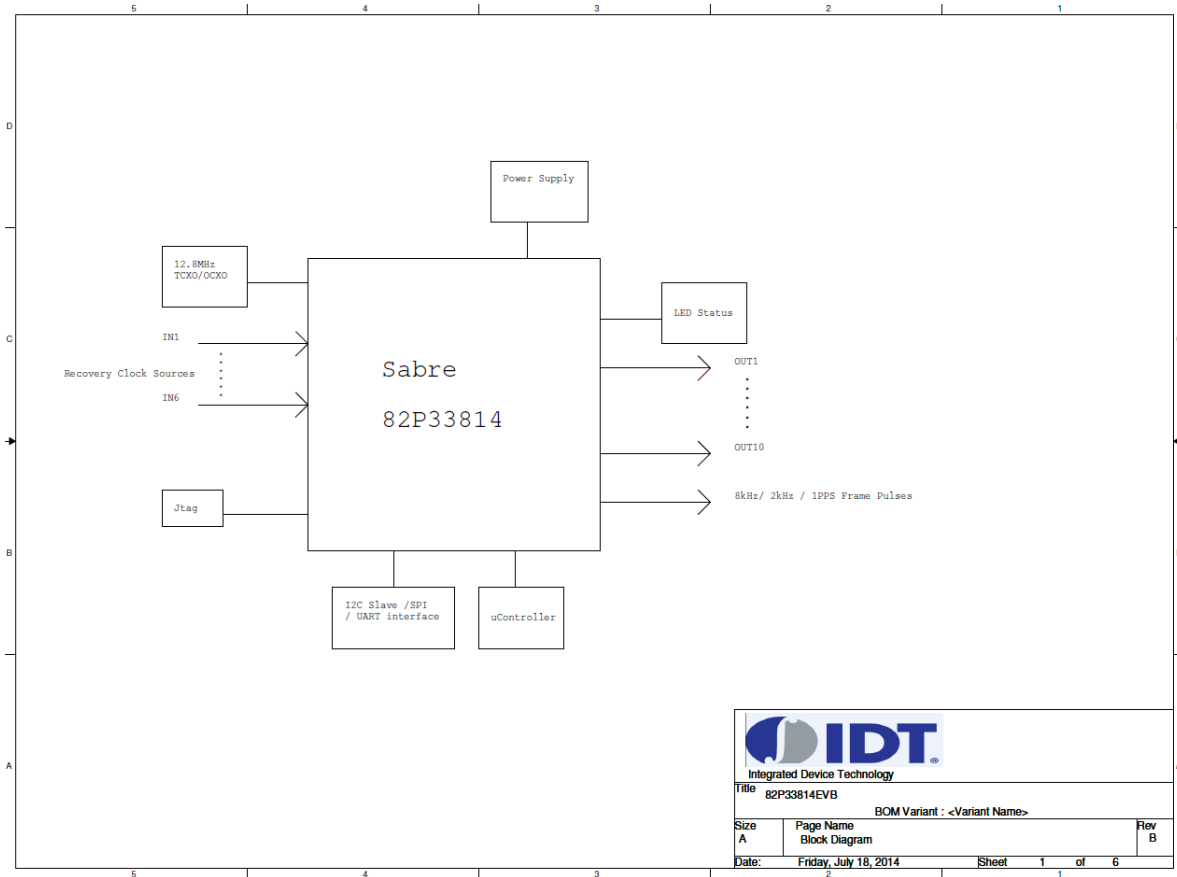## Figure 18. 82P33x14 Evaluation Board Schematics - Page 1: Block Diagram

Figure 19. 82P33x14 Evaluation Board Schematics - Page 2: Reference Selection
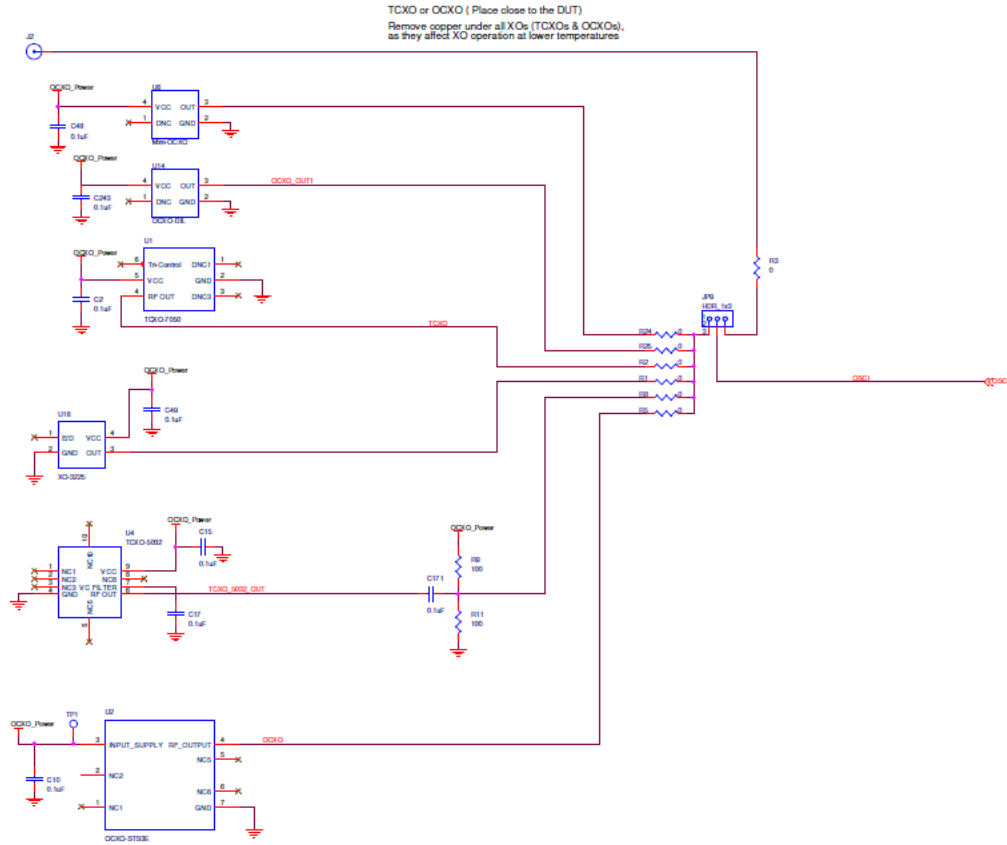
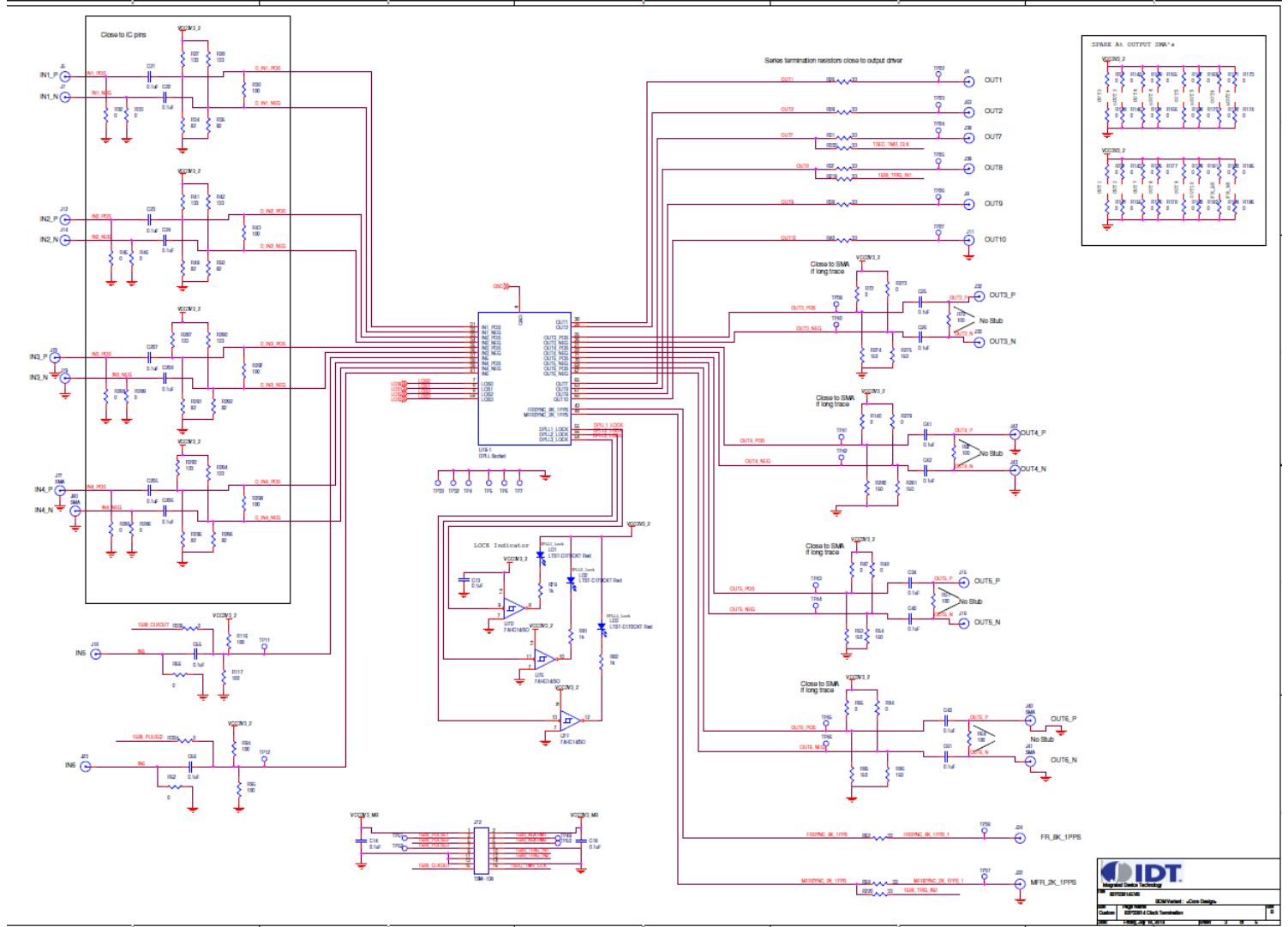**Figure 20. 82P33x14 Evaluation Board Schematics - Page 3: I/O Termination**

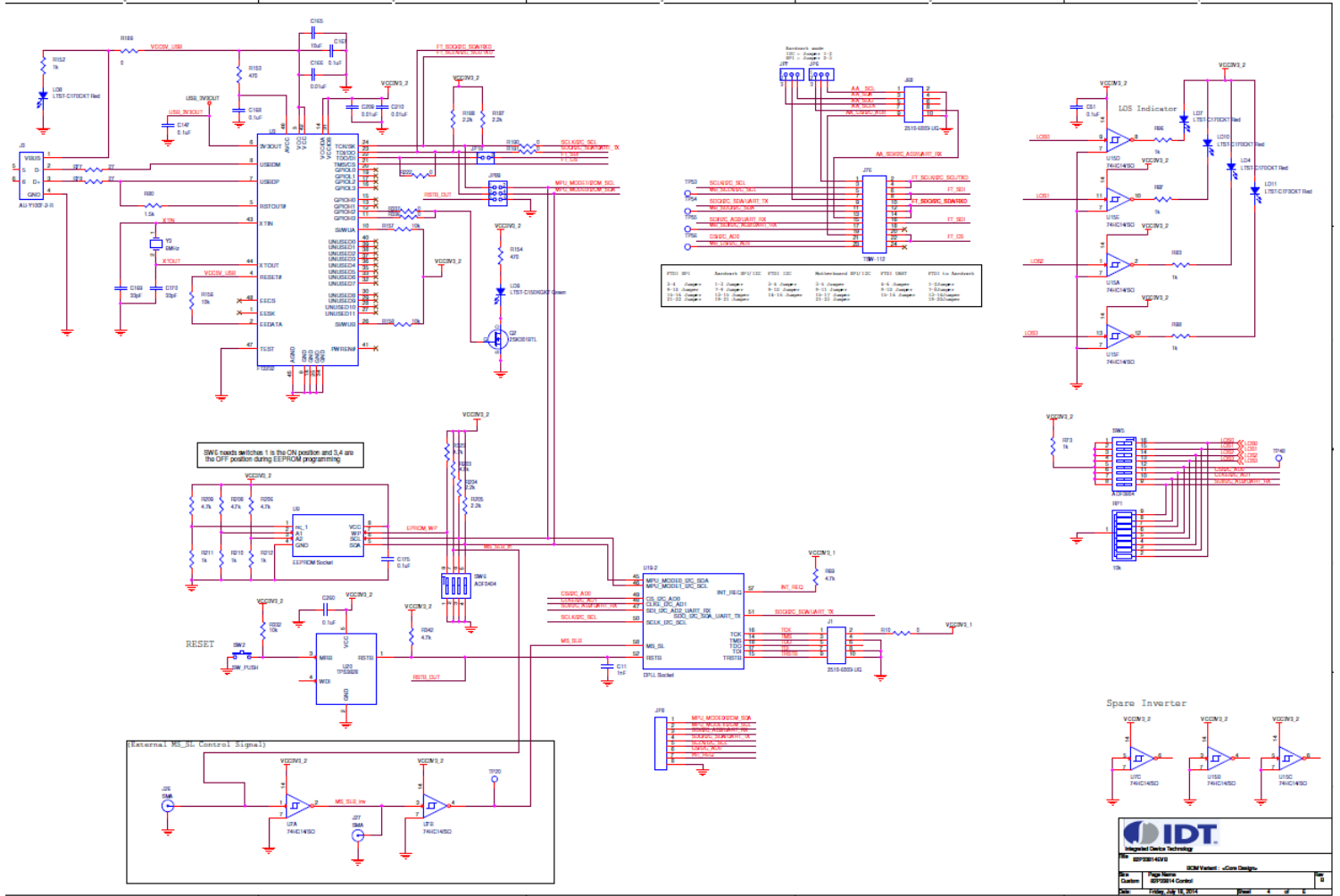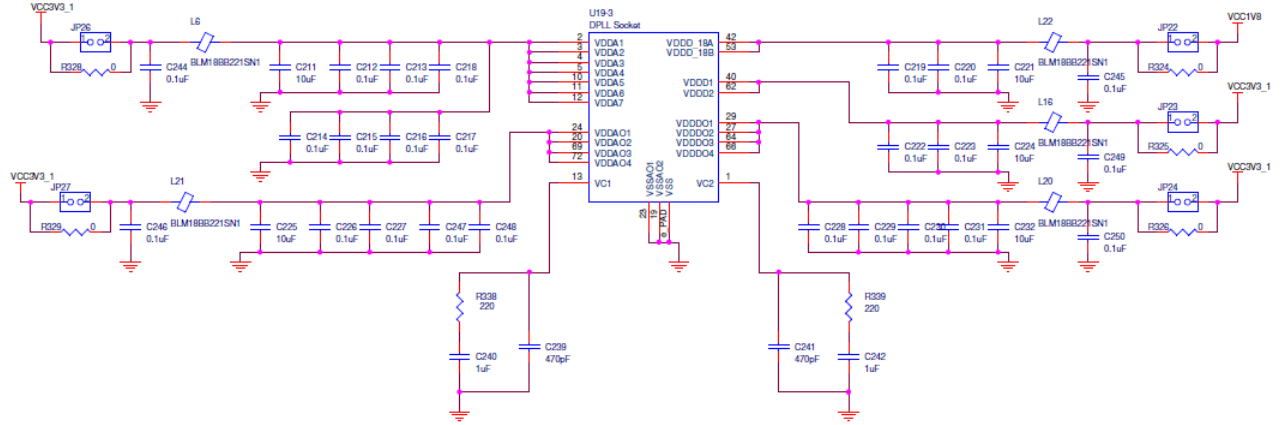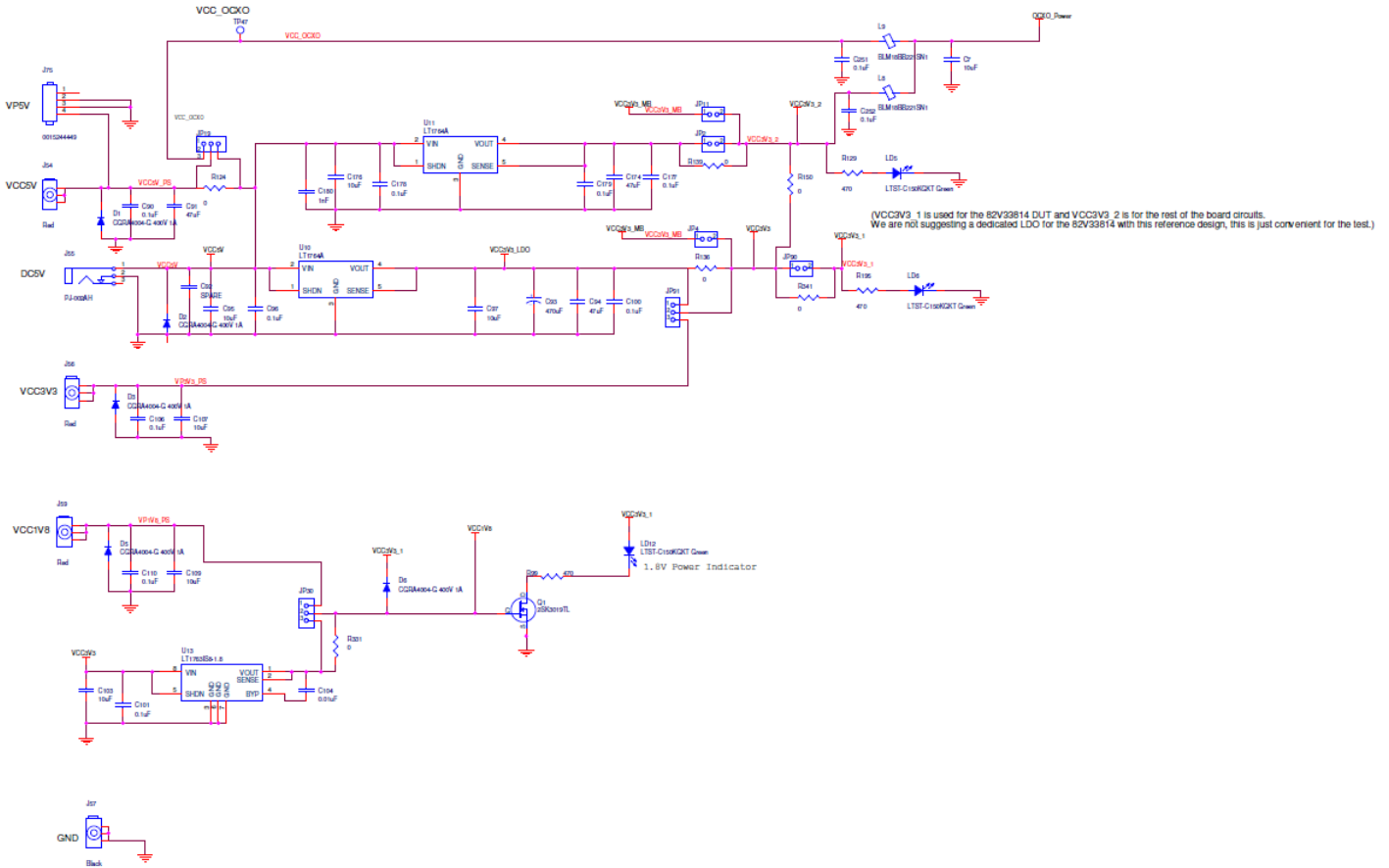# Figure 21. 82P33x14 Evaluation Board Schematics - Page 4: I2C/EEPROM

Figure 22. 82P33x14 Evaluation Board Schematics - Page 5: Power Supply 1

Figure 23. 82P33x14 Evaluation Board Schematics - Page 6: Power Supply 2

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES ("RENESAS") PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.