IDT® 89EBPES48H12G2 Evaluation Board Manual

(Eval Board: 18-677-000)

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Description of the EB48H12G2 Eval Board

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Introduction

The 89HPES48H12G2 switch (also referred to as PES48H12G2 in this manual) is a member of IDT's PCI Express® standard based line of products. It is a PCIe® Base Specification 2.0 compliant (Gen2) 12-port switch. There are twelve x4 lanes ports. Two x4 ports can be merged to form one x8 port in PES48H12G2. One upstream port is provided for connecting to the root complex (RC), and up to eleven downstream ports are available for connecting to PCIe endpoints or to another switch. More information on this device can be found in the 89HPES48H12G2 User Manual.

The 89EBPES48H12G2 Evaluation Board (also referred to as EB48H12G2 in this manual) provides an evaluation platform for the PES48H12G2 switch. It is also a cost effective way to add PCIe ports (slots) to an existing system with limited number of PCIe ports/slots. The EB48H12G2 board is designed to function as an add-on card to be plugged into a x8 PCIe slot available on a motherboard hosting an appropriate root complex and microprocessor(s). The EB48H12G2 is a vehicle to test and evaluate the functionality of the PES48H12G2 switch. It is also designed to work with the PES48H12 (Gen 1) switch. Refer to application note AN-550 for detail information on Designing Gen2-Ready boards for IDT's 48-lane, 12-port PCIe Switches. Customers can use this board to get a headstart on software development prior to the arrival of their own hardware. The EB48H12G2 is also used by IDT to reproduce system-level hardware or software issues reported by customers. Figure 1.1 illustrates the functional block diagram representing the main parts of the EB48H12G2 board.

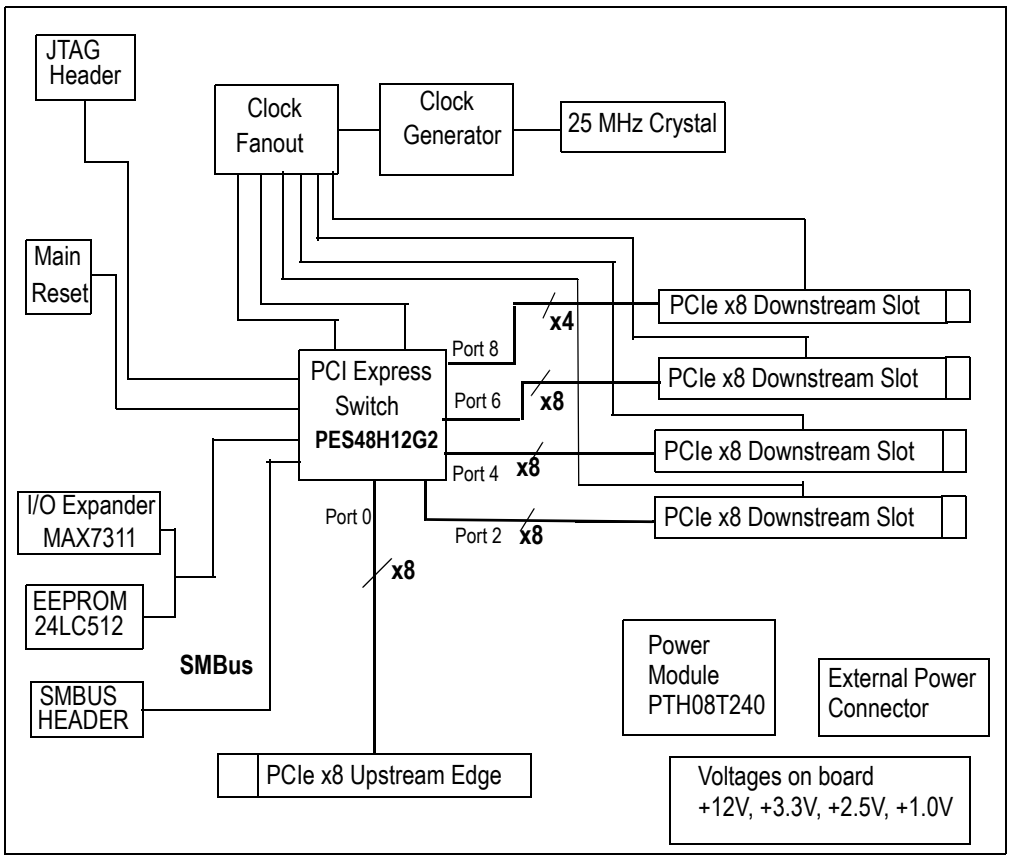


Figure 1.1 Function Block Diagram of the EB48H12G2 Eval Board

Notes

Board Features

Hardware

- **PES48H12G2 PCIe Gen2 switch**
  - *Up to twelve x4 or six x8 ports - 48 PCIe lanes*
  - *PCIe Base Specification Revision 2.0 compliant (Gen2 SerDes speeds of 5 GT/S)*
  - *Up to 2048 byte maximum Payload Size*
  - *Automatic lane reversal and polarity inversion supported on all lanes*
  - *Automatic per port link width negotiation to x8, x4, x2, x1*
  - *Load configuration from an optional serial EEPROM via SMBUS*
- **Upstream, Downstream Port**
  - *One edge connector on the upstream port, to be plugged into a slot with at least x8 capable on a host motherboard*
  - *Four slot connectors on the downstream ports, for PCIe endpoint add-on cards to be plugged in. These slot connectors are x8 mechanically and electrically connected as three x8 and one x4, but open-ended for card widths greater than x8 (e.g. x16).*
- **Numerous user selectable configurations set using onboard jumpers and DIP-switches**
  - *Source of clock - host clock or onboard clock generator*
  - *Two clock rates (100/125 MHz) from an onboard clock generator*
  - *Boot mode selection*
- **SMBUS Slave Interface (4 pin header)**
- **SMBUS Master Interface connected to the Serial EEPROMs through I/O expander**
- **"Attention" button for each downstream port to initiate a hot swap event on each port**
- **Four pin connector for optional external power supply**
- **Push button for Warm Reset**
- **Several LEDs to display status, reset, power, "Attention", etc.**
- **One 10-pin JTAG connector (pitch 2.54 mm x 2.54 mm)**

Software

There is no software or firmware executed on the board. However, useful software is provided along with the Evaluation Board to facilitate configuration and evaluation of the PES48H12G2 within host systems running popular operating systems.

- **Installation programs**
  - *Operating Systems Supported: Windows Server 2003, Windows Server 2008, WindowsXP, Vista, Linux*
- **GUI based application for Windows and Linux**
  - *Allows users to view and modify registers in the PES48H12G2*
  - *Binary file generator for programming the serial EEPROMs attached to the SMBUS.*

Other

- A metal bracket is provided to firmly hold in place three endpoints plugged into the EB48H12G2 board.
- An external power supply may be required under some conditions.
- SMBUS cable may be required for certain evaluation exercises.
- SMA connectors are provided on the EB48H12G2 board for clock outputs.

Revision History

January 5, 2009: Initial publication of eval board manual.

Notes

May 7, 2009: On page 2-2, changed reference to 25MHz oscillator (Y1) to (X1). In PCI Express Analog Power Voltage Converter section, changed DC-DC Converter (U4) to (U14). In PCI Express Transmitter Analog Power Voltage Converter section, changed DC-DC converter (U14) to (U4). In the SMBus Slave Interface section of Chapter 2, the slave interface default address was changed to **0b1110111.** In Table 2.6, signal S3[1] was changed from ON to OFF. In Table 2.11, locations were changed for the following signals: port 4: power-is-good; port 6 power-is-good; port 4: power indicator; port 6: power indicator; port 4: attention indicator; port 6: attention indicator.

Notes

Installation of the EB48H12G2 Eval Board

Notes

EB48H12G2 Installation

This chapter discusses the steps required to configure and install the EB48H12G2 evaluation board. All available DIP switches and jumper configurations are explained in detail.

The primary installation steps are:

1. Configure jumper/switch options suitable for the evaluation or application requirements.
2. Connect PCI Express endpoint cards to the downstream port PCIe slots on the evaluation board.
3. Make sure that the host system (motherboard with root complex chipset) is powered off.
4. Insert the evaluation board into the host system.
5. Apply power to the host system.

The EB48H12G2 board is typically shipped with all jumpers and switches configured to their default settings. In most cases, the board does not require further modification or setup.

Hardware Description

The PES48H12G2 is a 48-lane, 12-port PCI Express® switch. It is a peripheral chip that performs PCI Express based switching with a feature set optimized for high performance applications such as servers and storage. It provides switching functions between a PCI Express upstream port and downstream ports or peer-to-peer switching between downstream ports.

The EB48H12G2 has four PCI Express downstream ports, accessible through four x8 connectors. Three ports are capable of negotiating a x1, x2, x4 and x8 link width and one port is capable of negotiating a x1, x2, or x4 link width. All endpoint cards connected to the PES48H12G2 must support one of these link widths.

Basic requirements for the board to run are:

- Host system with a PCI Express root complex supporting at least x8 configuration through a PCI Express x8 or larger slot.
- x1, x2, x4 or x8 PCI Express Endpoint Cards.

Reference Clocks

The PES48H12G2 requires two differential reference clocks while the PES48H12 requires four. Also, AC coupling is not required on the PES48H12G2's reference input clocks, therefore capacitors C348, C350, C352, and C354 need to be removed and capacitors C347, C349, C351, and C353 should be replaced with 0 ohm resistors when the Gen2 part is installed. The EB48H12G2 derives these clocks from a common source which is user-selectable. The common source can be either the host system's reference clock or it can be the onboard clock generator. Selection is made by stuffing resistors as in Table 2.1.

Clock Configuration Stuffing Option	
W6 and W7	**Clock Source**
Pins 2 and 3	Onboard Reference Clock – Use onboard clock generator
Pins 1 and 2	Upstream Reference Clock – Host system provides clock **(Default)**

Table 2.1 Clock Source Selection

Notes

The source for the onboard clock is the ICS841484 clock generator device (U10) connected to a 25MHz oscillator (X1). When using the onboard clock generator, the output frequency is fixed at 100MHz, therefore FSEL0 (S2, pin 2) should be in the ON position as the default setting.

The outputs of the onboard clock generator and clock buffer (ICS9DB803) are accessible through two SMA connectors located on the Evaluation Board. See Table 2.2. This can be used to connect a scope for probing or capturing purposes and cannot be used to drive the clock from an external source.

Onboard Reference Clock Output (Differential) – J7, J9, J10-J15	
J7, J9, J12, J14	Positive Reference Clock
J10, J11, J13, J15	Negative Reference Clock

Table 2.2 SMA Connectors - Onboard Reference Clock

Power Sources

The EB48H12G2 and all downstream ports are powered from the upstream port slot power. If add-in cards require more power than the upstream slot can support, an external source is required to supply this extra power via an auxiliary 4-pin power connector on the board. Header W1, W2, and W3 (see Table 2.10) are used to select proper power source for the switch and all downstream ports.

External Power Source

If necessary, external power is supplied to the EB48H12G2 board through a 4-pin auxiliary power connector attached to J4. The external power supply provides +12V to the EB48H12G2 as described in Table 2.3. The +5V is unused.

Pin	Signal
1	+12V
2	GND
3	GND
4	+5V

Table 2.3 External Power Connector - J4

PCI Express Analog High Power Voltage Converter

A DC-DC converter (U5) provides a 2.5V PCI Express analog high power voltage (shown as V_{DD}PEHA) to the PES48H12G2. Install R224 (56 ohm resistor) to provide a 1.5V PCI Express serial data transmit termination voltage (shown as VTTPE) when the PES48H12 is installed.

PCI Express Analog Power Voltage Converter

A separate DC-DC converter (U14) provides a 1.0V PCI Express analog power voltage (shown as V_{DD}PEA) to the PES48H12G2.

PCI Express Transmitter Analog Voltage Converter

A separate DC-DC converter (U4) provides a 1.0V PCI Express transmitter analog voltage (shown as V_{DD}PETA) to the PES48H12G2.

Core Logic Voltage Converter

A separate DC-DC converter (U3) provides the 1.0V core voltage (V_{DD}CORE) to the PES48H12G2.

Notes

2.5V I/O Voltage Regulator

This evaluation board can be stuffed to host the PES48H12G2 (PCIe Gen2) device or the PES48H12 (PCIe Gen1) device. Depending on which device is populated on the board, appropriate settings can be made. A 12V to 3.3V voltage regulator (VR2) provides the 2.5V I/O voltage (V_{DD}I/O) to the PES48H12G2. Install R145 (2.49 ohm) to provide the 3.3V I/O voltage when the PES48H12 is installed instead.

Power-up Sequence for PES48H12G2 (PCIe Gen2 device)

During power supply ramp-up, V_{DD}CORE must remain at least 1.0V below V_{DD}I/O at all times. There are no other power-up sequence requirements for the various operating supply voltages.

Power-up Sequence for PES48H12 (PCIe Gen1 device)

The power -up sequence must be as following:

1. V_{DD}I/O — 3.3V
2. V_{DD}CORE, V_{DD}PE, V_{DD}APE — 1.0V
3. V_{TT}PE — 1.5V

When powering up, each voltage level must ramp up and stabilize prior to applying the next voltage in the sequence to ensure internal latch-up issues are avoided. There are no maximum time limitations between sequential valid power level requirements.

Reset

The PES48H12G2 supports two types of reset mechanisms as described in the PCI Express specification:

- Fundamental Reset: This is a system-generated reset that propagates along the PCI Express tree through a single side-band signal PERST# which is connected to the Root Complex, the PES48H12G2, and the endpoints.
- Hot Reset: This is an In-band Reset, communicated downstream via a link from one device to another. Hot Reset may be initiated by software. This is further discussed in the PES48H12G2 User Manual. The EB48H12G2 evaluation board provides seamless support for Hot Reset.

Fundamental Reset

There are two types of Fundamental Resets which may occur on the EB48H12G2 evaluation board:

- Cold Reset: During initial power-on, the onboard voltage monitor (TLC7733D) will assert the PCI Express Reset (PERSTN) input pin of the PES48H12G2.
- Warm Reset: This is triggered by hardware while the device is powered on. Warm Reset can be initiated by two methods:
  - Pressing a push-button switch (S1) located on EB48H12G2 board
  - The host system board IO Controller Hub asserting PERST# signal, which propagates through the PCIe upstream edge connector of the EB48H12G2. Note that one can bypass the onboard voltage monitor (TLC7733D) by moving the shunt from pin 1-2 to pin 2-3 (default) on W4.

  Both events cause the onboard voltage monitor (TLC7733D) to assert the PCI Express Reset (PERSTN) input of the PES48H12G2 while power is on.

Downstream Reset

The PES48H12G2 provides a a choice of either a software-controlled reset for each downstream port through GPIO pins or a fundamental reset through PERST#. Selection is made by jumpers described in Table 2.4.

Notes

Port #	Jumper	Selection
2	W9	[1-2] Software controlled reset through I/O Expander 0 [2-3] Fundamental reset PERST# (default)
4	W5	[1-2] Software controlled reset through I/O Expander 2 [2-3] Fundamental reset PERST# (default)
6	W19	[1-2] Software controlled reset through I/O Expander 2 [2-3] Fundamental reset PERST# (default)
8	W8	[1-2] Software controlled reset through I/O Expander 4 [2-3] Fundamental reset PERST# (default)

Table 2.4 Downstream Reset Selection

Boot Configuration Vector

A boot configuration vector consisting of the signals listed in Table 2.5 is sampled by the PES48H12G2 during a fundamental reset (while PERSTN is active). The boot configuration vector defines the essential parameters for switch operation and is set using DIP switches S3 and S13 as defined in Table 2.6.

Signal	Description
CCLKDS	**Common Clock Downstream (for 48H12).** The assertion of this pin indicates that all downstream ports are using the same clock source as that provided to downstream devices. This pin is used as the initial value of the Slot Clock Configuration bit in all of the Link Status Registers for downstream ports. The value may be overridden by modifying the SCLK bit in the downstream port's PCIELSTS register. **Default: 0x1**
CCLKUS	**Common Clock Upstream (for PES48H12).** The assertion of this pin indicates that the upstream port is using the same clock source as the upstream device. This pin is used as the initial value of the Slot Clock Configuration bit in the Link Status Register for the upstream port. The value may be overridden by modifying the SCLK bit in the P0_PCIELSTS register. **Default: 0x1**
CLKMODE[2:0]	**Initial Port Clocking mode (for PES48H12G2)**. **Default: 0x0** 0x0 - Global Clock mode on all ports. Port0/2/4/8 SCLK = 0 0x1 - Global Clock mode on all ports. Port0 SCLK =1, Port2 SCLK =0, Port4/8 SCLK =0 0x2 - Global Clock mode on all ports. Port0 SCLK =0, Port2 SCLK =1, Port4/8 SCLK =1 0x3 - Global Clock mode on all ports. Port0 SCLK =1, Port2 SCLK =1, Port4/8 SCLK =1 0x4 - Local Clock mode on Port0/1. Port0 SCLK =1, Port2 SCLK =1, Port4/8 SCLK =1 0x5 - Global Clock mode on Port0, Local Clock mode on Port1, Port0 SCLK =0, Port2 SCLK =1, Port4/8 SCLK =1 0x6 - Global Clock mode on Port0, Local Clock mode on Port1, Port0 SCLK =1, Port2 SCLK =1, Port4/8 SCLK =1 0x7 - Reserved
SWMODE[3:0]	**Switch Mode.** These configuration pins determine the PES48H12G2 switch operating mode. **Default: 0x0** 0x0 - Normal switch mode 0x1 - Normal switch mode with Serial EEPROM-based initialization 0x2 through 0xF - Reserved

Table 2.5 Boot Configuration Vector Signals

Notes

Signal	Description	Default
S13[1]	CLKMODE2	OFF
S13[2]	CLKMODE1/CCLKDS	OFF
S13[3]	CLKMODE0/CCLKUS	OFF
S3[1]	SWMODE[0]	OFF
S3[2]	SWMODE[1]	ON
S3[3]	SWMODE[2]	ON
S3[4]	SWMODE[3]	ON

Table 2.6 Boot Configuration Vector Switches S3 & S13 (ON=0, OFF=1)

SMBus Interfaces

The System Management Bus (SMBus) is a two-wire interface through which various system component chips can communicate. It is based on the principles of operation of I^2C. Implementation of the SMBus signals in the PCI Express connector is optional and may not be present on the host system. The SMBus interface consists of an SMBus clock pin and an SMBus data pin.

The PES48H12G2 contains two SMBus interfaces: a slave SMBus interface and a master SMBus interface. The slave SMBus interface allows a SMBus Master device full access to all software-visible registers. The Master SMBus interface provides connection to the external serial EEPROM used for initialization and the I/O expanders used for hot-plug signals.

SMBus Slave Interface

On the PES48H12G2 board, the slave SMBus interface is accessible through the PCI Express edge connector as well as a 4-pin header as described in Table 2.7.

Note: The SMBus signals to the PCI Express edge connector is disabled by default. To enable them, place 0-ohm resistors at locations R160 and R161.

.

Slave SMBus Interface Connector J8	
Pin	**Signal**
1	N/C
2	SCL
3	GND
4	SDA

Table 2.7 Slave SMBus Interface Connector

A fixed slave SMBus address specified by the SSMBADDR[5,2:1] pins is used. For a fixed address, the SMBus address of the PES48H12G2 slave interface is **0b1110111** by default.

The slave SMBus interface responds to the following SMBus transactions initiated by an SMBus master. Initiation of any SMBus transaction other than those listed above produces undefined results. See the SMBus 2.0 specification for a detailed description of the following transactions:

- Byte and Word Write/Read
- Block Write/Read

Notes

SMBus Master Interface

Connected to the master SMBus interface are seven 16-bit I/O Expanders (MAX7311) and a serial EEPROM (24LC512). Six I/O Expanders are used as the interface for the onboard hot-plug controllers (MIC2591B). The SMbus address for the I/O Expander0/2/4/8/12/13 are fixed as 0x20, 0x24, 0x22, 0x26, 0x28, 0x2A and 0x2C, respectively.

Note: Hot-plug is not implemented when PES48H12 is installed.

The seven bits address for the selected EEPROM device is fixed at `0b1010_000` by default.

JTAG Header

The PES48H12G2 provides a JTAG connector J5 for access to the PES48H12G2 JTAG interface. The connector is a 2.54 x 2.54 mm pitch male 10-pin connector. Refer to Table 2.8 for the JTAG Connector J5 pin out.

JTAG Connector J5					
Pin	**Signal**	**Direction**	**Pin**	**Signal**	**Direction**
1	/TRST - Test reset	Input	2	GND	—
3	TDI - Test data	Input	4	GND	—
5	TDO - Test data	Output	6	GND	—
7	TMS - Test mode select	Input	8	GND	—
9	TCK - Test clock	Input	10	GND	—

Table 2.8 JTAG Connector Pin Out

Attention Buttons

The PES48H12G2 features three attention buttons, shown in Table 2.9. Each button corresponds to a particular port and is used to initiate hot-swapping events.

Button	Description
S7	Port 2 Attention Button
S12	Port 4 Attention Button
S6	Port 6 Attention Button
S11	Port 8 Attention Button

Table 2.9 Attention Buttons

Notes

Miscellaneous Jumpers, Headers

Miscellaneous Jumpers, Headers			
Ref. Designator	**Type**	**Default**	**Description**
W1-W3	Header	1-2 Shunted	1-2: 12.0V source from Upstream Port **(Default)** 2-3: 12.0V source from external power connector
W38	Header	Shunted	Disable EEPROM Write protect feature **(Default)**
S9[1]	Switch	ON	ON: Port2, Force hot-plug controller on **(Default)** OFF: Port2, Power Enable bit controls hot-plug controller
S10[1]	Switch	ON	ON: Port4, Force hot-plug controller on **(Default)** OFF: Port4, Power Enable bit controls hot-plug controller
S10[2]	Switch	ON	ON: Port6, Force hot-plug controller on **(Default)** OFF: Port6, Power Enable bit controls hot-plug controller
S9[2]	Switch	ON	ON: Port8, Force hot-plug controller on **(Default)** OFF: Port8, Power Enable bit controls hot-plug controller
W45	Header	2-3 Shunted	2-3: Port 2, +12V source from Upstream port **(Default)** 1-2: Port 2, +12V source from hot-plug controller
W51	Header	2-3 Shunted	2-3: Port 4, +12V source from Upstream port **(Default)** 1-2: Port 4, +12V source from hot-plug controller
W52	Header	2-3 Shunted	2-3: Port 6, +12 source from Upstream port **(Default)** 1-2: Port 6, +12 source from hot-plug controller
W46	Header	2-3 Shunted	2-3: Port 8, +12 source from Upstream port **(Default)** 1-2: Port 8, +12 source from hot-plug controller
W47	Header	2-3 Shunted	2-3: Port 2, +3.3V source from Upstream port **(Default)** 1-2: Port 2, +3.3V source from hot-plug controller
W53	Header	2-3 Shunted	2-3: Port 4, +3.3V source from Upstream port **(Default)** 1-2: Port 4, +3.3V source from hot-plug controller
W54	Header	2-3 Shunted	2-3: Port 6, +3.3V source from Upstream port **(Default)** 1-2: Port 6, +3.3V source from hot-plug controller
W48	Header	2-3 Shunted	2-3: Port 8, +3.3V source from Upstream port **(Default)** 1-2: Port 8, +3.3V source from hot-plug controller
W49	Header	2-3 Shunted	2-3: Port 2, +3.3AUX source from upstream port **(Default)** 1-2: Port 2, +3.3V source from hot-plug controller
W55	Header	2-3 Shunted	2-3: Port 4, +3.3AUX source from upstream port **(Default)** 1-2: Port 4, +3.3V source from hot-plug controller
W56	Header	2-3 Shunted	2-3: Port 6, +3.3AUX source from upstream port **(Default)** 1-2: Port 6, +3.3V source from hot-plug controller
W50	Header	2-3 Shunted	2-3: Port 8, +3.3AUX source from upstream port **(Default)** 1-2: Port 8, +3.3V source from hot-plug controller

Table 2.10 Miscellaneous Jumpers, Headers

Notes

LEDs

There are several LED indicators on the EB48H12G2 which convey status feedback. A description of each is provided in Table 2.11.

Location	Color	Definition
DS14	Green	Port 2: Power-is-good Indicator
DS20	Green	Port 4: Power-is-good Indicator
DS17	Green	Port 6: Power-is-good Indicator
DS24	Green	Port 8: Power-is-good Indicator
DS16	Green	Port 2: Power Indicator
DS23	Green	Port 4: Power Indicator
DS19	Green	Port 6: Power Indicator
DS26	Green	Port 8: Power Indicator
DS15	Yellow	Port 2: Attention Indicator
DS21	Yellow	Port 4: Attention Indicator
DS18	Yellow	Port 6: Attention Indicator
DS25	Yellow	Port 8: Attention Indicator
DS27	Green	Port 0: Activity Indicator
DS28	Green	Port 2: Activity Indicator
DS29	Green	Port 4: Activity Indicator
DS30	Green	Port 6: Activity Indicator
DS31	Green	Port 8: Activity Indicator
DS8	Green	Port 0: Linkup Indicator
DS9	Green	Port 2: Linkup Indicator
DS10	Green	Port 4: Linkup Indicator
DS11	Green	Port 6: Linkup Indicator
DS12	Green	Port 8: Linkup Indicator
DS3	Red	Port 2/8: Power Fault Indicator
DS7	Red	Port 4/6: Power Fault Indicator
DS33	Green	GPIO7
DS34	Green	GPIO6
DS35	Green	GPIO5
DS36	Green	GPIO4
DS37	Green	GPIO3
DS38	Green	GPIO2
DS39	Green	GPIO1
DS40	Green	GPIO0

Table 2.11 LED Indicators

Notes

PCI Express Connectors

Pin	Side A		Side B	
1	+12V	12V power	PRSNT1#	Hot-Plug presence detect
2	+12V	12V power	+12V	12V power
3	RSVD	Reserved	+12V	12V power
4	GND	Ground	GND	Ground
5	SMCLK	SMBus clock	JTAG2	TCK (Test Clock) JTAG i/f clk i/p
6	SMDAT	SMBus Data	JTAG	TDI (Test Data Input)
7	GND	Ground	JTAG	TDO (Test Data Output)
8	+3.3V	3.3V power	JTAG	TMS (Test Mode Select)
9	JTAG1	TRST# (Test/Reset) resets JTAG i/f	+3.3V	3.3V power
10	3.3Vaux	3.3V auxiliary power	+3.3V	3.3V power
11	WAKE#	Signal for Link reactivation	PERST#	Fundamental Reset
Mechanical Key				
12	RSVD	Reserved	GND	Ground
13	GND	Ground	REFCLK+	REFCLK Reference clock
14	PETp0	Transmitter differential	REFCLK-	(differential pair)
15	PETn0	pair, Lane 0	GND	Ground
16	GND	Ground	PERp0	Receiver differential
17	PRSNT2#	Hot-Plug presence detect	PERn0	pair, Lane 0
18	GND	Ground	GND	Ground
19	PETp1	Transmitter differential	RSVD	Reserved
20	PETn1	pair, Lane 1	GND	Ground
21	GND	Ground	PERp1	Receiver differential
22	GND	Ground	PERn1	pair, Lane 1
23	PETp2	Transmitter differential	GND	Ground
24	PETn2	pair, Lane 2	GND	Ground
25	GND	Ground	PERp2	Receiver differential
26	GND	Ground	PERn2	pair, Lane 2
27	PETp3	Transmitter differential	GND	Ground
28	PETn3	pair, Lane 3	GND	Ground
29	GND	Ground	PERp3	Receiver differential
30	RSVD	Reserved	PERn3	pair, Lane 3
31	PRSNT2#	Hot-Plug presence detect	GND	Ground
32	GND	Ground	RSVD	Reserved
33	PETp4	Transmitter differential	RSVD	Reserved

Table 2.12 PCI Express x8 Connector Pinout (Part 1 of 2)

Notes

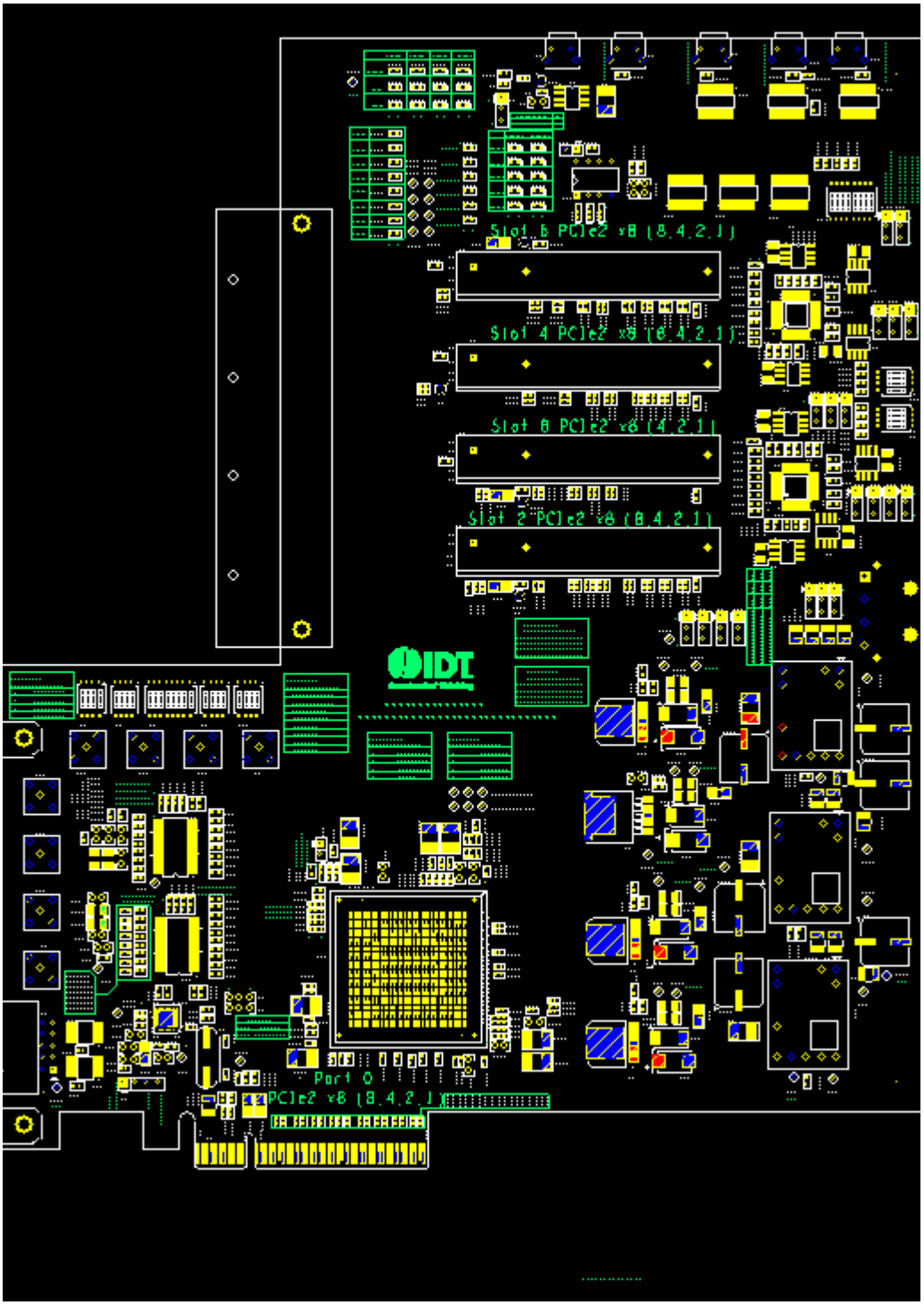
Pin	Side A		Side B	
34	PETn4	pair, Lane 4	GND	Ground
35	GND	Ground	PERp4	Receiver differential
36	GND	Ground	PERn4	pair, Lane 4
37	PETp5	Transmitter differential	GND	Ground
38	PETn5	pair, Lane 5	GND	Ground
39	GND	Ground	PERp5	Receiver differential
40	GND	Ground	PERn5	pair, Lane 5
41	PETp6	Transmitter differential	GND	Ground
42	PETn6	pair, Lane 6	GND	Ground
43	GND	Ground	PERp6	Receiver differential
44	GND	Ground	PERn6	pair, Lane 6
45	PETp7	Transmitter differential	GND	Ground
46	PETn7	pair, Lane 7	GND	Ground
47	GND	Ground	PERp7	Receiver differential
48	PRSNT2#	Hot-Plug presence detect	PERn7	pair, Lane 7
49	GND	Ground	GND	Ground

Table 2.12 PCI Express x8 Connector Pinout (Part 2 of 2)

Note: These x8 PCI Express connectors comply with the PCIe specification. According to the PCI Express specification, the PRSNT1# pin should be wired to the farthest available PRSNT2# pin on the connector. In the EB48H12G2, all PRSNT2# pins are tied together. This allows a board with a x1 or x4 width to be installed.

Notes

EB48H12G2 Board Figure



Software for the EB48H12G2 Eval Board

Notes

Introduction

This chapter discusses some of the main features of the available software to give users a better understanding of what can be achieved with the EB48H12G2 evaluation board using the device management software.

Device Management Software and related user documentation are available on a CD which is included in the Evaluation Board Kit. This information is also available on IDT's FTP site. For more information, contact IDT at ssdhelp@idt.com.

Device Management Software

The primary use of the Device Management Software package is to enable users of the evaluation board to access all the registers in the PES48H12G2 device. This access can be achieved using the PCI Express in-band configuration cycles through the upstream port on the PES48H12G2.

This software also enables users to save a snapshot of the current register set into a dump file which can be used for debugging purposes. An export/import facility is also available to create and use "Configuration" files which can be used to initialize the switch device with specific values in specific registers.

A conversion utility is also provided to translate a configuration file into an EEPROM programmable data structure. This enables the user to program an appropriate serial EEPROM with desirable register settings for the PES48H12G2, and then to populate that EEPROM onto the Evaluation Board. It is also possible to program the EEPROM directly on the Evaluation Board using a feature provided by the software package.

The front end of the Device Management Software is a user-friendly Graphical User Interface which allows the user to quickly read or write the registers of interest. The GUI also permits the user to run the software in "simulation" mode with no real hardware attached, allowing the creation of configuration files for the PES48H12G2 in the absence of the actual device.

Much of the Device Management Software is written with device-independent and OS-independent code. The software will be guaranteed to work on Linux (/sys interface) and MS Windows XP. It may function flawlessly on various flavors of MS Windows, but may not be validated on all. The fact that the software is device-independent assures its scalability to future PCIe parts from IDT. Once users are familiar with the GUI, they will be able to use the same GUI on all PCIe parts from IDT. This software is customized for each device through an XML device description file which includes information on the number of ports, registers, types of registers, information on bit-fields within each register, etc.

Notes

Schematics

Notes

Schematics

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2	Top Level Block Diagram
3	DUT Top
4	DUT Control, Misc
5	DUT Serial ports
6	DUT Power
7	DUT Ground
8	Clock Tree
9	Downstream Clock G1
10	DUT Clock G2 Reference
11	Upstream Port 0,1
12	Downstream Port 2, 4, 6, 8
13	Downstream Port 2
14	Downstream Port 4
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16	Downstream Port 8
17	Hot Swap Controller Port 2,4
18	Hot Swap Controller Port 6,8
19	Port Wake Buffers
20	I/O Expander Top / Port Status LEDS
21	I/O Expander Ports 0-7
22	Reset / Power Conectors
23	Power Regulators

P02_TOP_LEVEL_BLOCK_DIAGRAM

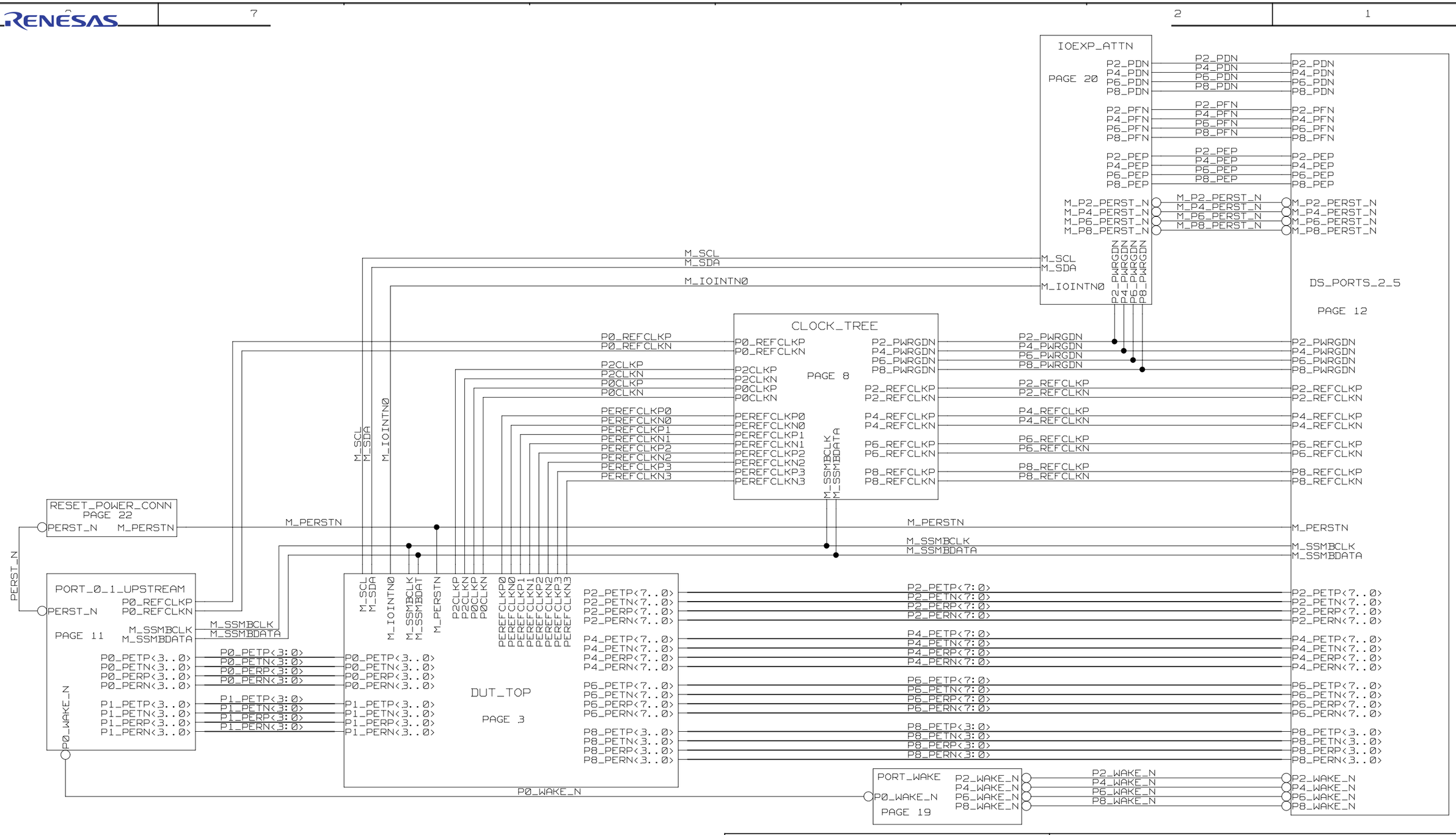
REVISIONS				
DCN	REV	DESCRIPTION	DATE	CHANGE BY
PCB-0171R01	1.0	89EBPES48H12G2 EVAL BOARD	JULY 31 2008	JHU

TITLE
89HPES48H12G2 Eval Board

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-00172	18-677-000	1.0

AUTHOR	CHECKED BY
JHU	B. Le

Tue Sep 23 14:23:33 2008 | SHEET 1 OF 23



TITLE 89HPES48H12G2 Eval Board

TOP LEVEL BLOCK DIAGRAM

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-00172	18-677-000	1.0

AUTHOR	CHECKED BY
JHU	B. Le

Mon Aug 11 11:41:08 2008 — SHEET 2 OF 23

DUT_CONTROL_MISC

4C5v 2B6^ IN P0CLKP → P0CLKP
4C5v 2B6^ IN P0CLKN → P0CLKN

4C5v 2B6^ IN P2CLKP → P2CLKP
4C5v 2B6^ IN P2CLKN → P2CLKN

4D5v 2B5^ IN PEREFCLKP3 → PEREFCLKP3
4D5v 2B5^ IN PEREFCLKN3 → PEREFCLKN3

4D5v 2B5^ IN PEREFCLKP2 → PEREFCLKP2
4D5v 2B5^ IN PEREFCLKN2 → PEREFCLKN2

4D5v 2B6^ IN PEREFCLKP1 → PEREFCLKP1
4C5v 2B6^ IN PEREFCLKN1 → PEREFCLKN1

4C5v 2B6^ IN PEREFCLKP0 → PEREFCLKP0
4C5v 2B6^ IN PEREFCLKN0 → PEREFCLKN0

M_PERSTN → M_PERSTN → IN 2B6^ 4C5v
M_SCL → M_SCL → IO 2B6^ 4A6v
M_SDA → M_SDA → IO 2B6^ 4A6v
M_SSMBCLK → M_SSMBCLK → IO 2B6^ 4B2v
M_SSMBDAT → M_SSMBDAT → IO 2B6^ 4B2v
M_IOINTN0 → M_IOINTN0 → IN 2B6^ 4D5v

PAGE 4

DUT_SERIAL_PORTS

5D4v 2B7^ OUT P0_PETP<3:0> → P0_PETP<3..0>
5D4v 2A7^ OUT P0_PETN<3:0> → P0_PETN<3..0>

5D5v 2A7^ IN P0_PERP<3:0> → P0_PERP<3..0>
5D5v 2A7^ IN P0_PERN<3:0> → P0_PERN<3..0>

5D4v 2A7^ OUT P1_PETP<3:0> → P1_PETP<3..0>
5D4v 2A7^ OUT P1_PETN<3:0> → P1_PETN<3..0>

5D5v 2A7^ IN P1_PERP<3:0> → P1_PERP<3..0>
5D5v 2A7^ IN P1_PERN<3:0> → P1_PERN<3..0>

5B4v 2B5^ OUT P2_PETP<7:0> → P2_PETP<7..0>
5B4v 2B5^ OUT P2_PETN<7:0> → P2_PETN<7..0>

5B5v 2B5^ IN P2_PERP<7:0> → P2_PERP<7..0>
5B5v 2B5^ IN P2_PERN<7:0> → P2_PERN<7..0>

5A4v 2B5^ OUT P4_PETP<7:0> → P4_PETP<7..0>
5A4v 2B5^ OUT P4_PETN<7:0> → P4_PETN<7..0>

5A5v 2B5^ IN P4_PERP<7:0> → P4_PERP<7..0>
5A5v 2A5^ IN P4_PERN<7:0> → P4_PERN<7..0>

PAGE 5

DUT_POWER

PAGE 6

DUT_GND

PAGE 7

LANE REVERSED FOR IMPROVED ROUTING

DOWNSTREAM PORTS

2A5^ IN P6_PERP<7:0> → P6_PERP<4> AC10 PE06RN3 … P6_PERP<7> AC6 PE06RN0 — PORT 6 — PE06RP0 … PE06TN0 AE6 P6_PERN<7:0> → OUT 2A5^

2A5^ IN P6_PERN<7:0> → P6_PERN<4> AB10 … P6_PERN<7> AB6 — PORT 6 — P6_PETP<7:0> → OUT 2A5^

P6_PERP<0> AC16 PE07RN3 … P6_PERP<3> AC12 PE07RN0 — PORT 7 — PE07RP0 … PE07TN0 AE12 P6_PERN<3:0> → OUT 2A5^

P6_PERN<0> AB16 … P6_PERN<3> AB12 — PORT 7 — P6_PETP<3:0> → OUT 2A5^

2A5^ IN P8_PERP<3:0> → P8_PERP<0> D5 PE08RN3 … P8_PERP<3> D9 PE08RN0 — PORT 8 — PE08RP0 … PE08TN0 B9 P8_PERN<3:0> → OUT 2A5^

2A5^ IN P8_PERN<3:0> → P8_PERN<0> E5 … P8_PERN<3> E9 — PORT 8 — P8_PETP<3:0> → OUT 2A5^

K4 K5 J4 J5 G4 G5 F4 F5 — PORT 9 — K1 K2 J1 J2 G1 G2 F1 F2

ALL AC CAPS ARE TO BE PLACED AT THE ASSOCIATED CONNECTORS

LANE REVERSED FOR IMPROVED ROUTING

AF10 AC_P6_PETP4 0.1UF C147 P6_PETP<4> 4 → P6_PETP<7:0> OUT 2A5^
AE10 AC_P6_PETN4 0.1UF C131 P6_PETN<4> 4
AF9 AC_P6_PETP5 0.1UF C146 P6_PETP<5> 5
AE9 AC_P6_PETN5 0.1UF C130 P6_PETN<5> 5
AF7 AC_P6_PETP6 0.1UF C145 P6_PETP<6> 6
AE7 AC_P6_PETN6 0.1UF C129 P6_PETN<6> 6
AF6 AC_P6_PETP7 0.1UF C144 P6_PETP<7> 7
AE6 AC_P6_PETN7 0.1UF C128 P6_PETN<7> 7

AF16 AC_P6_PETP0 0.1UF C151 P6_PETP<0> 0
AE16 AC_P6_PETN0 0.1UF C135 P6_PETN<0> 0
AF15 AC_P6_PETP1 0.1UF C150 P6_PETP<1> 1
AE15 AC_P6_PETN1 0.1UF C134 P6_PETN<1> 1
AF13 AC_P6_PETP2 0.1UF C149 P6_PETP<2> 2
AE13 AC_P6_PETN2 0.1UF C133 P6_PETN<2> 2
AF12 AC_P6_PETP3 0.1UF C148 P6_PETP<3> 3
AE12 AC_P6_PETN3 0.1UF C132 P6_PETN<3> 3 → P6_PETN<7:0> OUT 2A5^

A5 AC_P8_PETP0 0.1UF C380 P8_PETP<0> 0 → P8_PETP<3:0> OUT 2A5^
B5 AC_P8_PETN0 0.1UF C356 P8_PETN<0> 0
A6 AC_P8_PETP1 0.1UF C377 P8_PETP<1> 1
B6 AC_P8_PETN1 0.1UF C106 P8_PETN<1> 1
A8 AC_P8_PETP2 0.1UF C374 P8_PETP<2> 2
B8 AC_P8_PETN2 0.1UF C103 P8_PETN<2> 2
A9 AC_P8_PETP3 0.1UF C371 P8_PETP<3> 3
B9 AC_P8_PETN3 0.1UF C100 P8_PETN<3> 3 → P8_PETN<3:0> OUT 2A5^

AC22 AB22 AC21 AB21 AC19 AB19 AC18 AB18 — PORT 12 — AF22 AE22 AF21 AE21 AF19 AE19 AF18 AE18

U23 U22 V23 V22 Y23 Y22 AA23 AA22 — PORT 13 — U26 U25 V26 V25 Y26 Y25 AA26 AA25

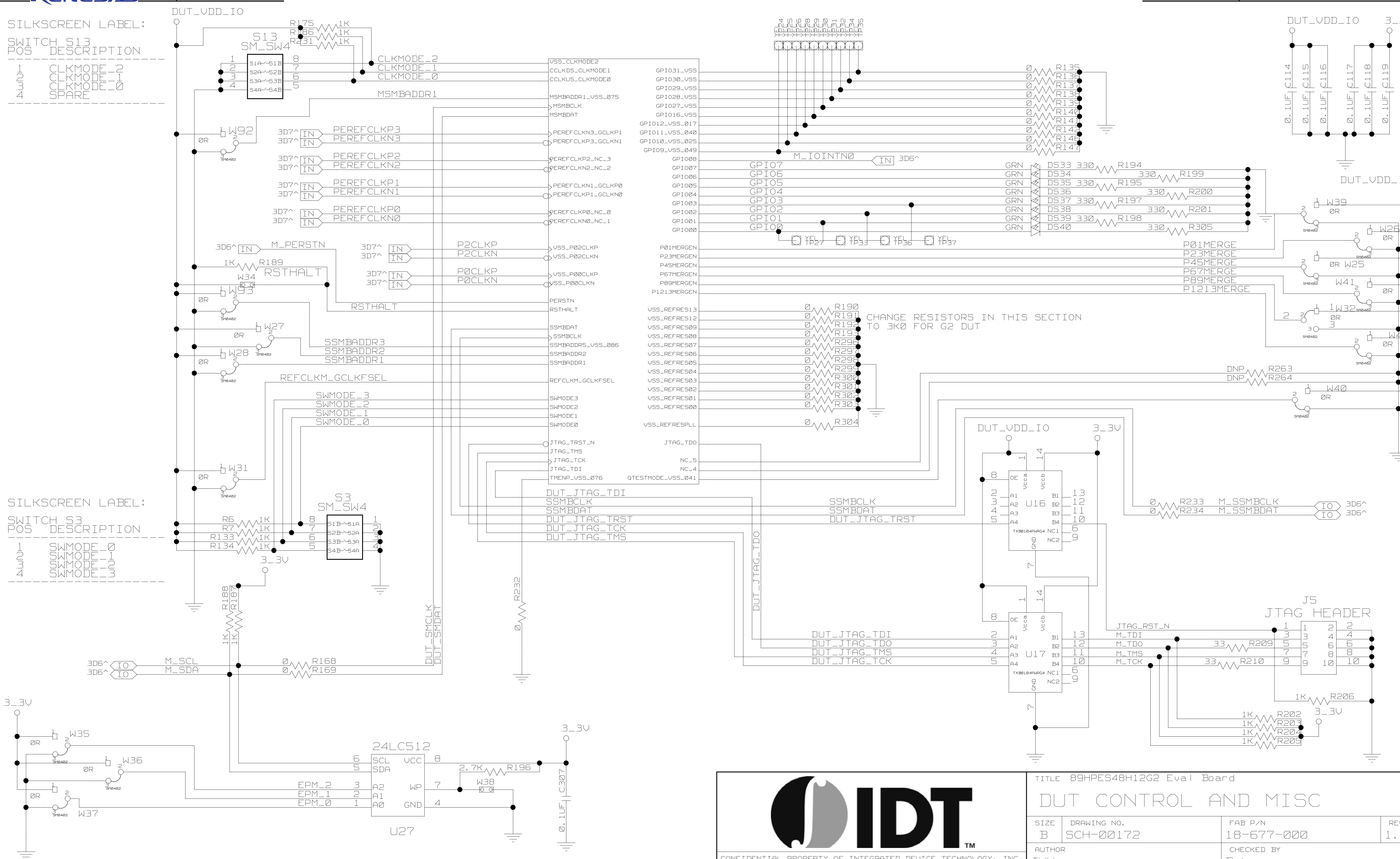
TITLE 89HPES48H12G2 Eval Board

DUT TOP

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-00172	18-677-000	1.0

AUTHOR	CHECKED BY
JHU	B.Le

Wed Sep 24 16:24:08 2008 SHEET 3 OF 23



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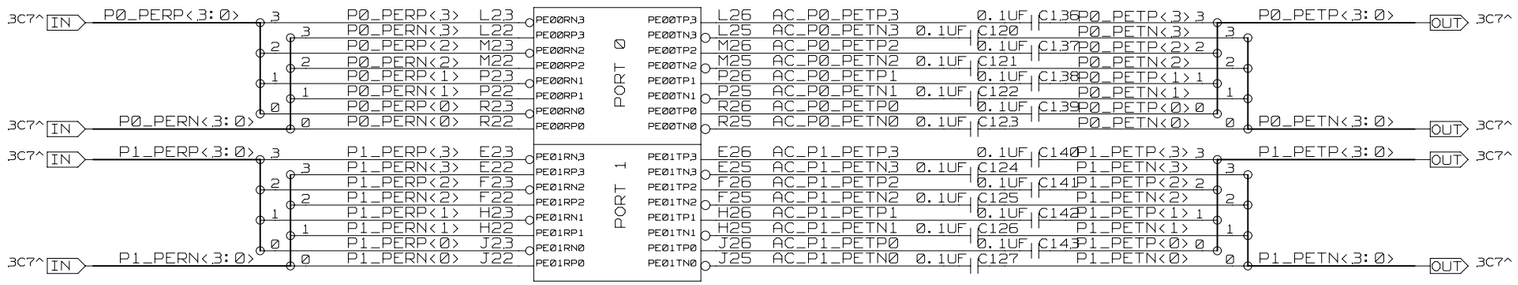
TITLE 89HPES48H12G2 Eval Board			
DUT CONTROL AND MISC			
SIZE B	DRAWING NO. SCH-00172	FAB P/N 18-677-000	REV. 1.0
AUTHOR JHU		CHECKED BY B.Le	
Wed Sep 24 16:24:13 2008		SHEET 4 OF 23	

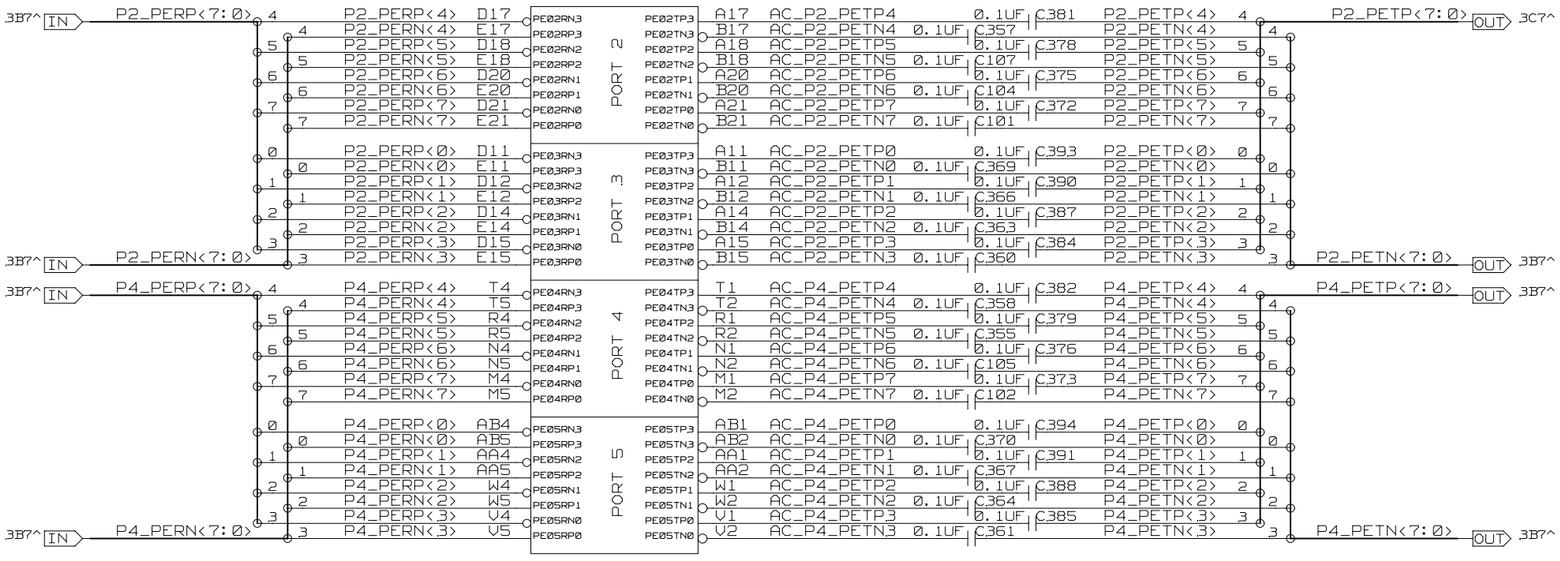
UPSTREAM PORTS



LANE REVERSED FOR IMPROVED ROUTING

ALL AC CAPS ARE TO BE PLACED AT THE ASSOCIATED CONNECTORS

LANE REVERSED FOR IMPROVED ROUTING



DOWNSTREAM PORTS

TITLE 89HPES48H12G2 Eval Board

DUT SERIAL PORTS

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-00172	18-677-000	1.0

AUTHOR	CHECKED BY
JHU	B. Le

Wed Sep 24 16:24:11 2008 SHEET 5 OF 23

DUT_VDDPEA

0.1UF C317 C318 C319 C320 C321 C322 C323 C324 C325 C326 C327 C328 C329 C330 C331 C332 C333 C334 C335 C336 C337 C338 C339 C340
47UF 47UF 1.0UF

DUT_VDDPETA

0.1UF C218 C227 C237 C246 C253 C260 C267 C271 C275 C278 C281 C284 C287 C290 C293 C296 C299 C302 C315
0.1UF C219 C228 C238 C247 C254 C261 C268 C272 C276 C279 C282 C285 C288 C291 C294 C297 C300 C303 C316
47UF 47UF 1.0UF

DUT_VDDPEHA

0.1UF C216 C225 C235 C244 C255 C262 C270 C274 C277 C280 C283 C286 C289 C292 C295 C298 C301 C314
0.1UF C217 C226 C236 C245
47UF 47UF

DUT_VDD_IO

0.1UF C214 C223 C232 C242 C250 C257 C264
0.1UF C215 C224 C233 C243 C251 C258 C265
1.0UF
0.1UF C211 C220 C229 C239

DUT_VDDCORE

0.1UF C153 C155 C157 C159 C161 C163 C165 C167 C169 C171 C173 C175 C177 C179 C181 C183 C185 C187 C189 C191 C193 C195 C197 C199 C201 C203 C205 C207 C209 C212 C221 C230 C240 C248 C255 C262 C273
0.1UF C152 C154 C156 C158 C160 C162 C164 C166 C168 C170 C172 C174 C176 C178 C180 C182 C184 C186 C188 C190 C192 C194 C196 C198 C200 C202 C204 C206 C208 C210 C213 C222 C231 C241 C249 C256 C263 C269
1.0UF
47UF 47UF

DUT_VDD_IO

A22 A3 AA3 AB24 AB3 AC1 AC2 AC24 AD24 AE24 B22 B3 D1 D2 D25 D26 AE4 AD1

DUT_VDDPEHA

AA13 AA18 AA9 F10 F19 F8 G10 G19 G8 L19 L6 L7 L8 M19 N19 T19 T20 T21 U6 U7 U8 Y13 Y18 Y9

DUT_VDDCORE

H11 H12 H15 H16 J11 J12 J15 J16 K11 K12 K15 K16 L11 L12 L15 L16 M11 M12 M15 M16 N11 N12 N15 N16 P11 P12 P15 P16 R11 R12 R15 R16 T11 T12 T15 T16 U11 U12 U15 U16 V11 V12 V15 V16 W11 W12

VDDCORE_00 VDDCORE_01 VDDCORE_02 VDDCORE_03 VDDCORE_04 VDDCORE_05 VDDCORE_06 VDDCORE_07 VDDCORE_08 VDDCORE_09 VDDCORE_10 VDDCORE_11 VDDCORE_12 VDDCORE_13 VDDCORE_14 VDDCORE_15 VDDCORE_16 VDDCORE_17 VDDCORE_18 VDDCORE_19 VDDCORE_20 VDDCORE_21 VDDCORE_22 VDDCORE_23 VDDCORE_24 VDDCORE_25 VDDCORE_26 VDDCORE_27 VDDCORE_28 VDDCORE_29 VDDCORE_30 VDDCORE_31 VDDCORE_32 VDDCORE_33 VDDCORE_34 VDDCORE_35 VDDCORE_36 VDDCORE_37 VDDCORE_38 VDDCORE_39 VDDCORE_40 VDDCORE_41 VDDCORE_42 VDDCORE_43 VDDCORE_44 VDDCORE_45 VDDCORE_46 VDDCORE_47

W15 W16

power

VDDIO_00 VDDIO_01 VDDIO_02 VDDIO_03 VDDIO_04 VDDIO_05 VDDIO_06 VDDIO_07 VDDIO_08 VDDIO_09 VDDIO_10 VDDIO_11 VDDIO_12 VDDIO_13 VDDIO_14 VDDIO_15 VDDIO_16 VDDIO_17

VDDPEHA_00 VDDPEHA_01 VDDPEHA_02 VDDPEHA_03 VDDPEHA_04 VDDPEHA_05 VDDPEHA_06 VDDPEHA_07 VDDPEHA_08 VDDPEHA_09 VDDPEHA_10 VDDPEHA_11 VDDPEHA_12 VDDPEHA_13 VDDPEHA_14 VDDPEHA_15 VDDPEHA_16 VDDPEHA_17 VDDPEHA_18 VDDPEHA_19 VDDPEHA_20 VDDPEHA_21 VDDPEHA_22 VDDPEHA_23

DUT_VDDPEA

VDDPEA_00 AA10 VDDPEA_01 AA17 VDDPEA_02 F14 VDDPEA_03 F17 VDDPEA_04 G14 VDDPEA_05 G17 VDDPEA_06 H19 VDDPEA_07 H20 VDDPEA_08 H21 VDDPEA_09 H6 VDDPEA_10 H7 VDDPEA_11 H8 VDDPEA_12 J19 VDDPEA_13 J20 VDDPEA_14 J21 VDDPEA_15 J6 VDDPEA_16 J7 VDDPEA_17 J8 VDDPEA_18 N6 VDDPEA_19 N7 VDDPEA_20 N8 VDDPEA_21 P19 VDDPEA_22 P20 VDDPEA_23 P21 VDDPEA_24 P8 VDDPEA_25 V19 VDDPEA_26 V20 VDDPEA_27 V21 VDDPEA_28 V6 VDDPEA_29 V7 VDDPEA_30 V8 VDDPEA_31 W19 VDDPEA_32 W20 VDDPEA_33 W21 VDDPEA_34 W6 VDDPEA_35 W7 VDDPEA_36 W8 VDDPEA_37 Y10 VDDPEA_38 Y17

VDDPETA_00 VDDPETA_01 VDDPETA_02 VDDPETA_03 VDDPETA_04 VDDPETA_05 VDDPETA_06 VDDPETA_07 VDDPETA_08 VDDPETA_09 VDDPETA_10 VDDPETA_11 VDDPETA_12 VDDPETA_13 VDDPETA_14 VDDPETA_15 VDDPETA_16 VDDPETA_17 VDDPETA_18 VDDPETA_19 VDDPETA_20 VDDPETA_21 VDDPETA_22 VDDPETA_23

AA11 AA12 AA19 AA8 F11 F18 G11 G18 K19 K20 K21 K6 K7 K8 L21 R19 R20 R21 R8 T6 T7 T8 Y19 Y8

DUT_VDDPETA

TITLE 89HPES48H12G2 Eval Board

DUT POWER SUPPLY

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-00172	18-677-000	1.0

AUTHOR	CHECKED BY
JHU	B. Le

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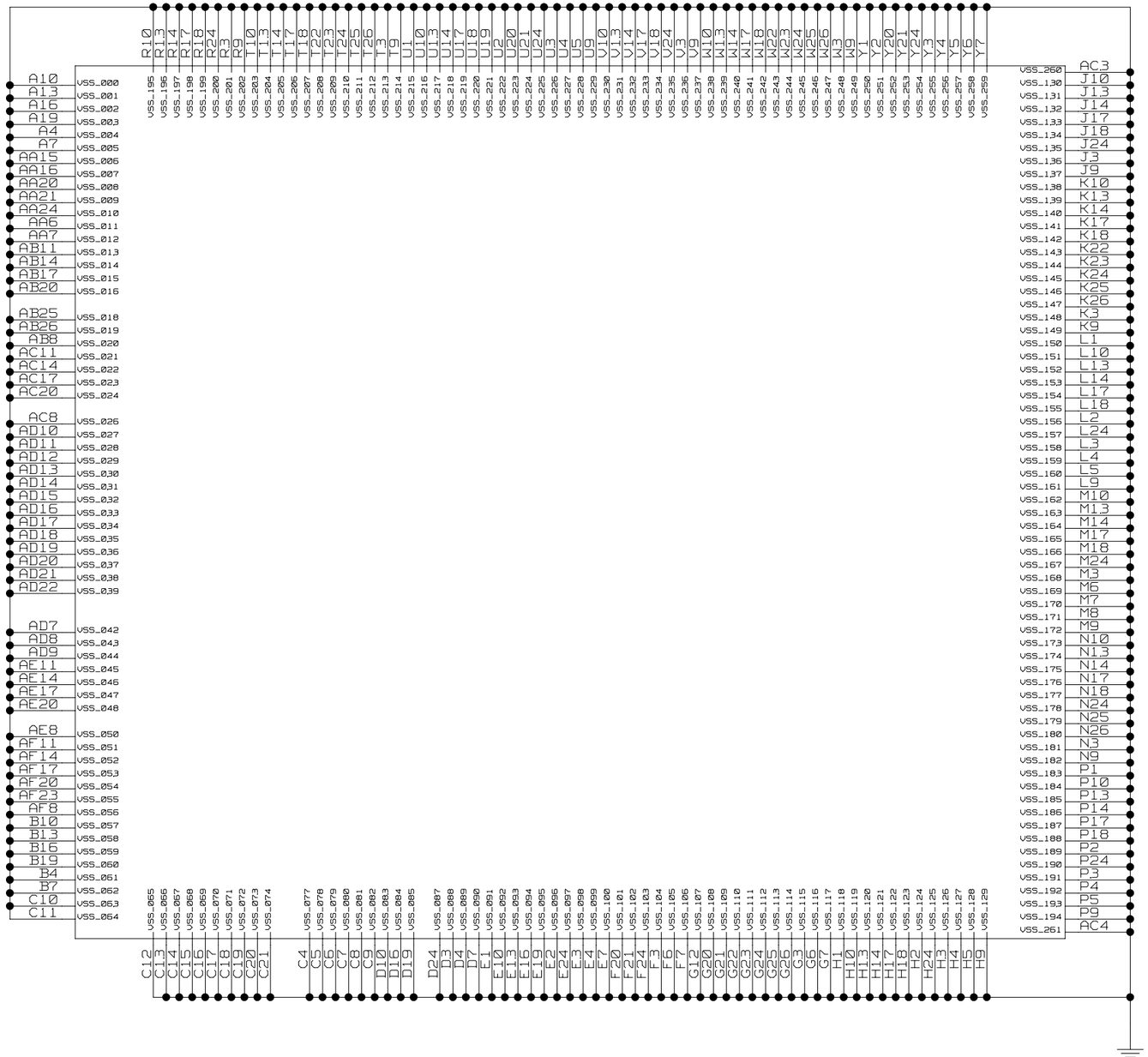

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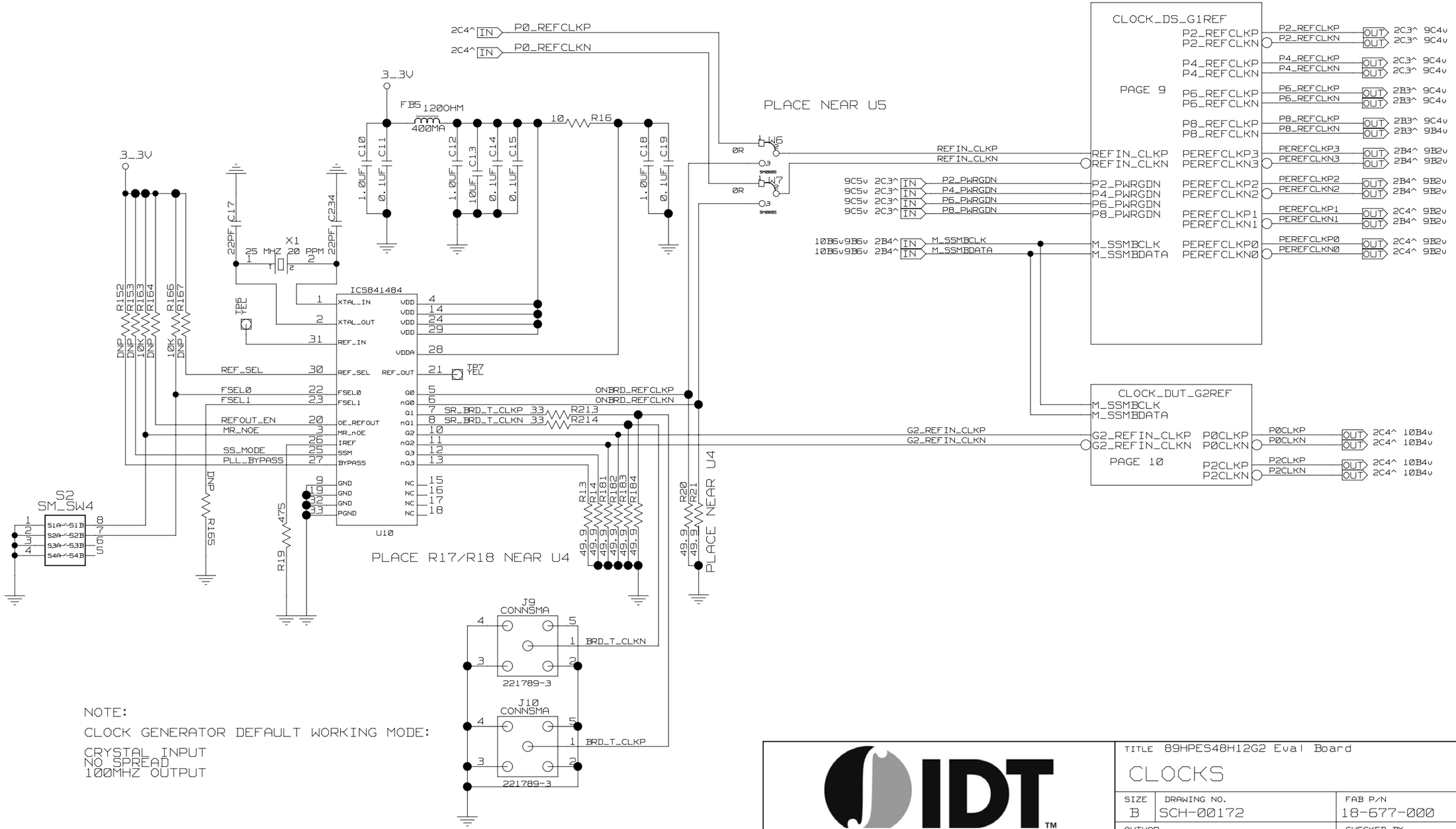
TITLE 89HPES48H12G2 Eval Board

DUT GROUND

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-00172	18-677-000	1.0

AUTHOR	CHECKED BY
JHU	B. Le

Wed Sep 24 16:24:34 2008 SHEET 7 OF 23

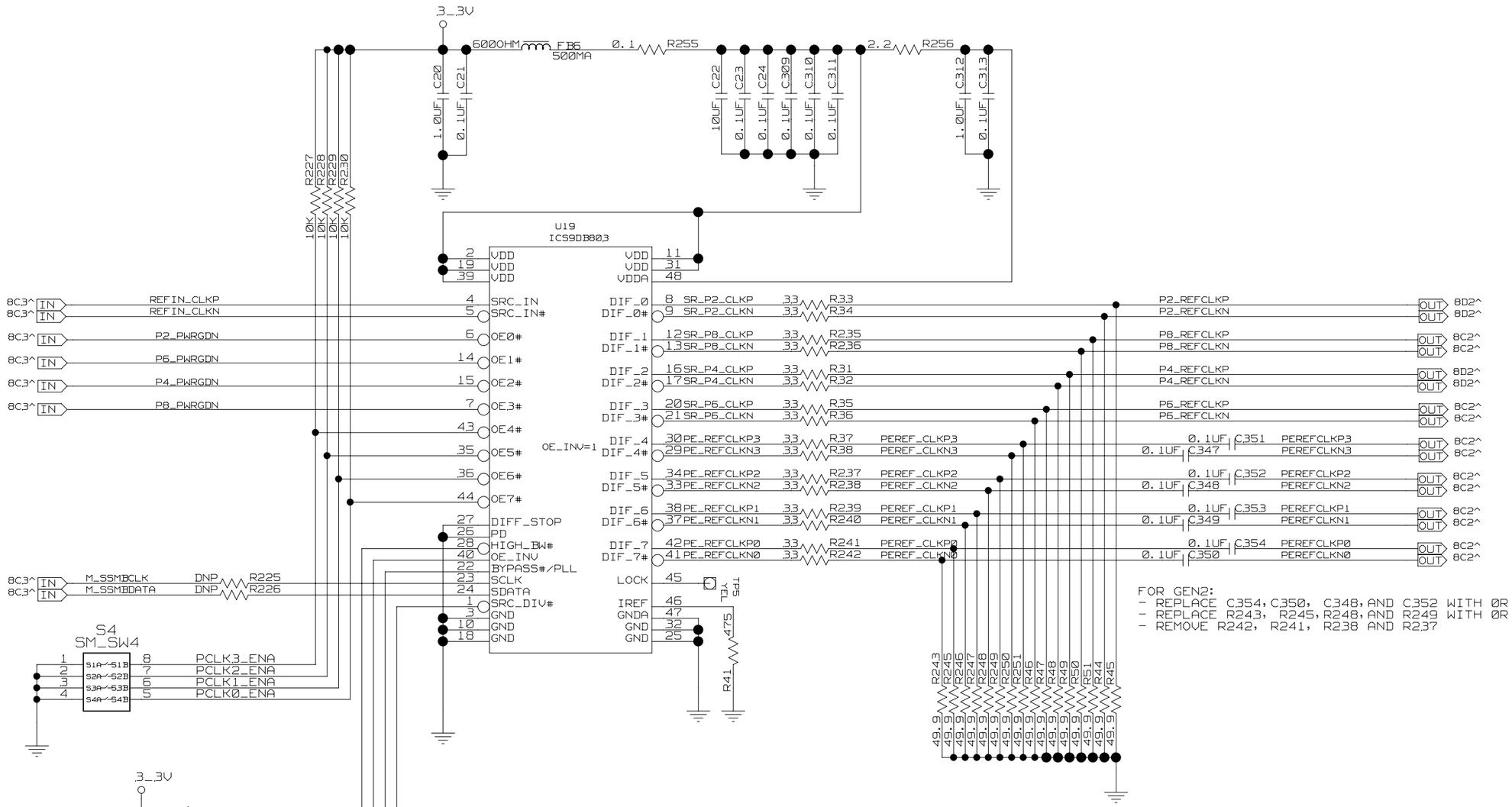


NOTE:

CLOCK GENERATOR DEFAULT WORKING MODE:

CRYSTAL INPUT
NO SPREAD
100MHZ OUTPUT

TITLE 89HPES48H12G2 Eval Board			
CLOCKS			
SIZE B	DRAWING NO. SCH-00172	FAB P/N 18-677-000	REV. 1.0
AUTHOR JHU		CHECKED BY B.Le	
Tue Aug 19 16:43:10 2008		SHEET 8 OF 23	



FOR GEN2:
- REPLACE C354, C350, C348, AND C352 WITH 0R
- REPLACE R243, R245, R248, AND R249 WITH 0R
- REMOVE R242, R241, R238 AND R237

SILKSCREEN LABEL:

SWITCH S4

POS	DESCRIPTION
1	PCLK3_ENA
2	PCLK2_ENA
3	PCLK1_ENA
4	PCLK0_ENA

SILKSCREEN LABEL:

W29 HIGHBW
W30 G1_OE
W33 BYPASS
W42 SRC_DIV

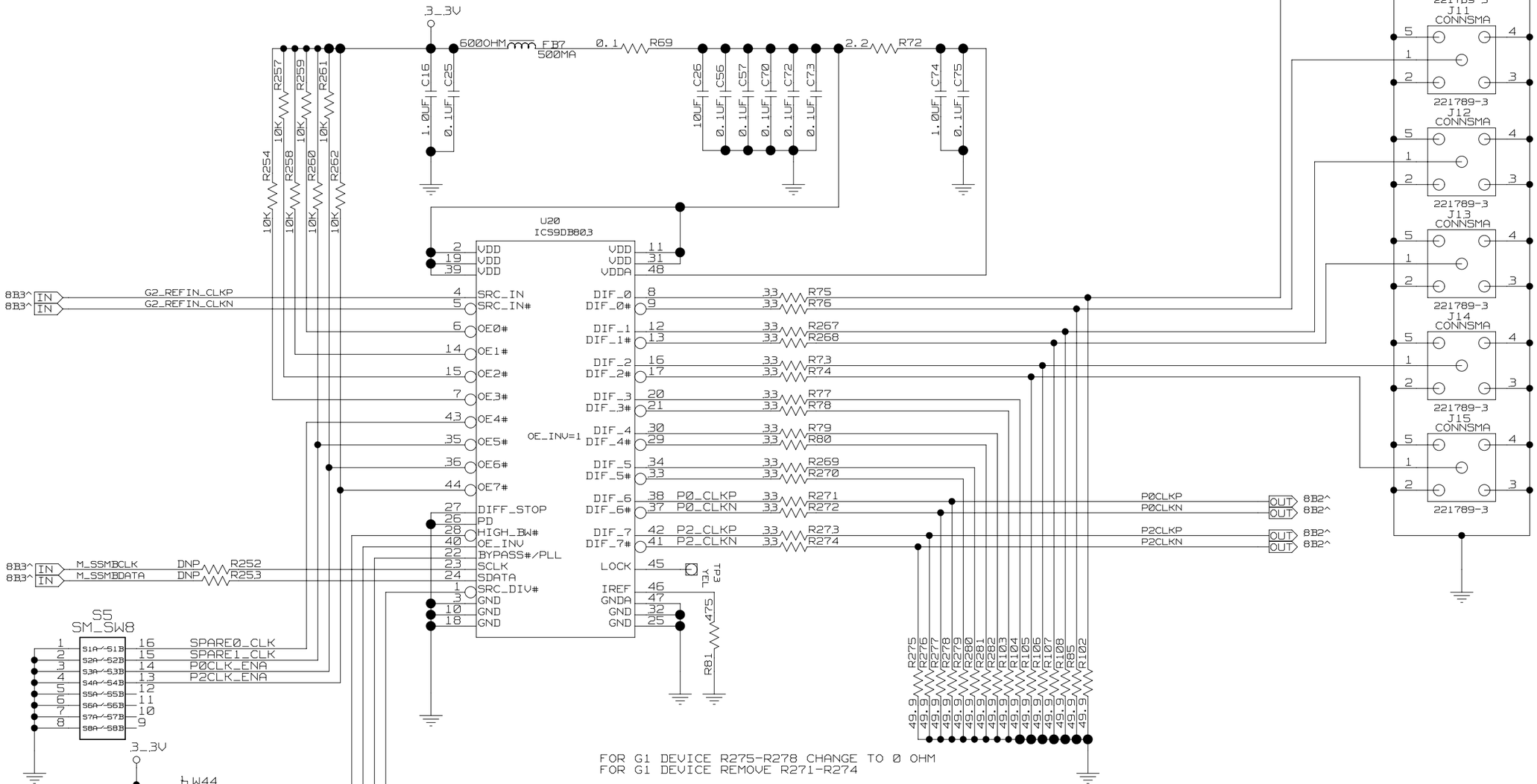
TITLE 89HPES48H12G2 Eval Board

CLOCK BUFFER DS, G1

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-00172	18-677-000	1.0

AUTHOR	CHECKED BY
JHU	B. Le

Tue Aug 19 16:43:16 2008 SHEET 9 OF 23



SILKSCREEN LABEL:

SWITCH S5

POS	DESCRIPTION
1	SPARECLK_0
2	SPARECLK_1
3	P0CLKENA
4	P2CLKENA
5	SPARE
6	SPARE
7	SPARE
8	SPARE

SILKSCREEN LABEL:

W44 HIGHBW
W82 G1_OE
W83 BYPASS
W84 SRC_DIV

FOR G1 DEVICE R275-R278 CHANGE TO 0 OHM
FOR G1 DEVICE REMOVE R271-R274

TITLE 89HPES48H12G2 Eval Board

CLOCK BUFFER G2

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-00172	18-677-000	1.0

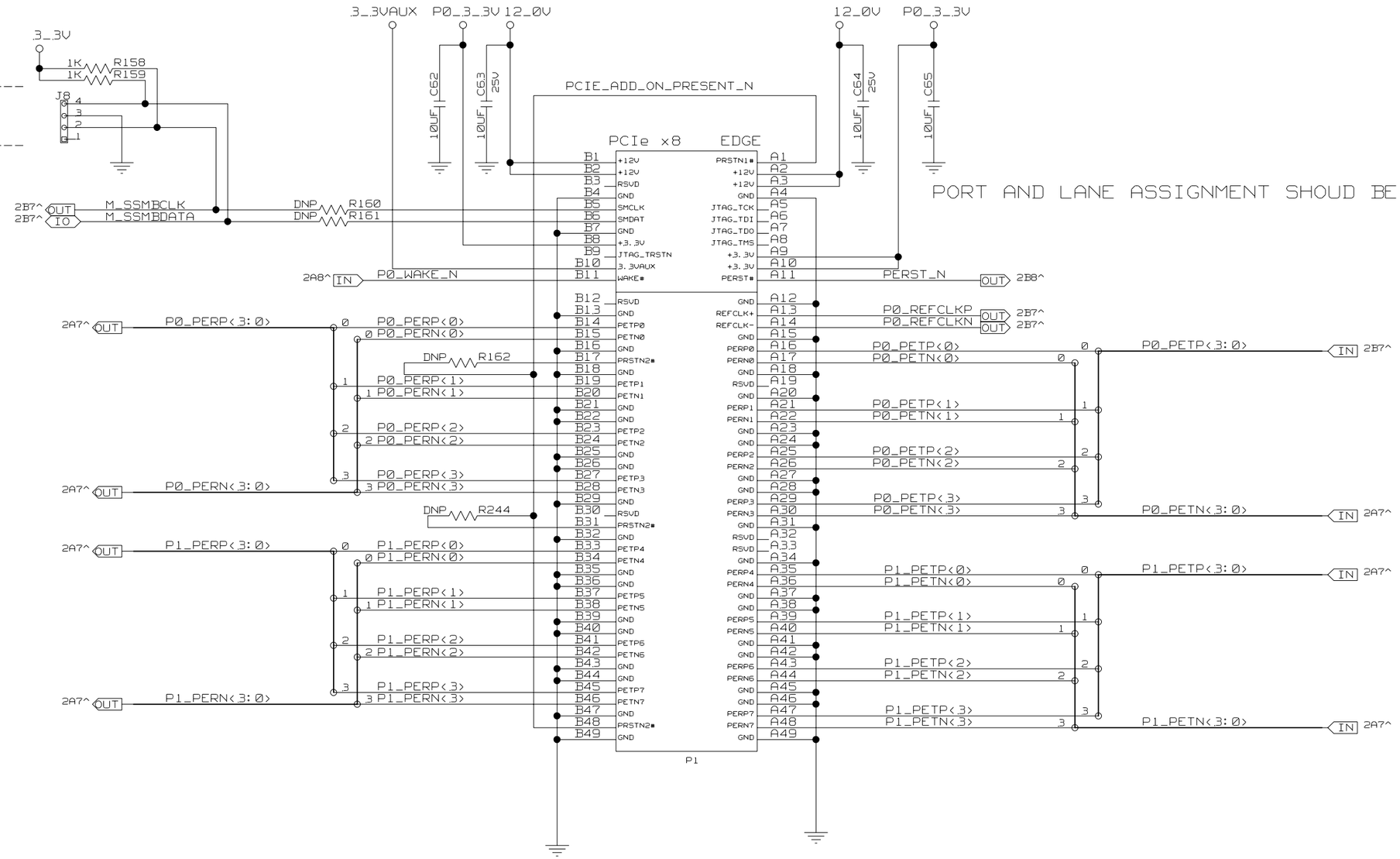
AUTHOR	CHECKED BY
JHU	B.Le

Tue Aug 19 16:43:20 2008 SHEET 10 OF 23

SILKSCREEN LABEL:

SWITCH J8

POS	DESCRIPTION
4	SMBDATA
3	GND
2	SMBCLK
1	NC



PORT AND LANE ASSIGNMENT SHOUD BE VERIFIED

SILKSCREEN LABEL:

CONECTOR P1

PORT 0 PCIE2 X8<8,4,2,1>

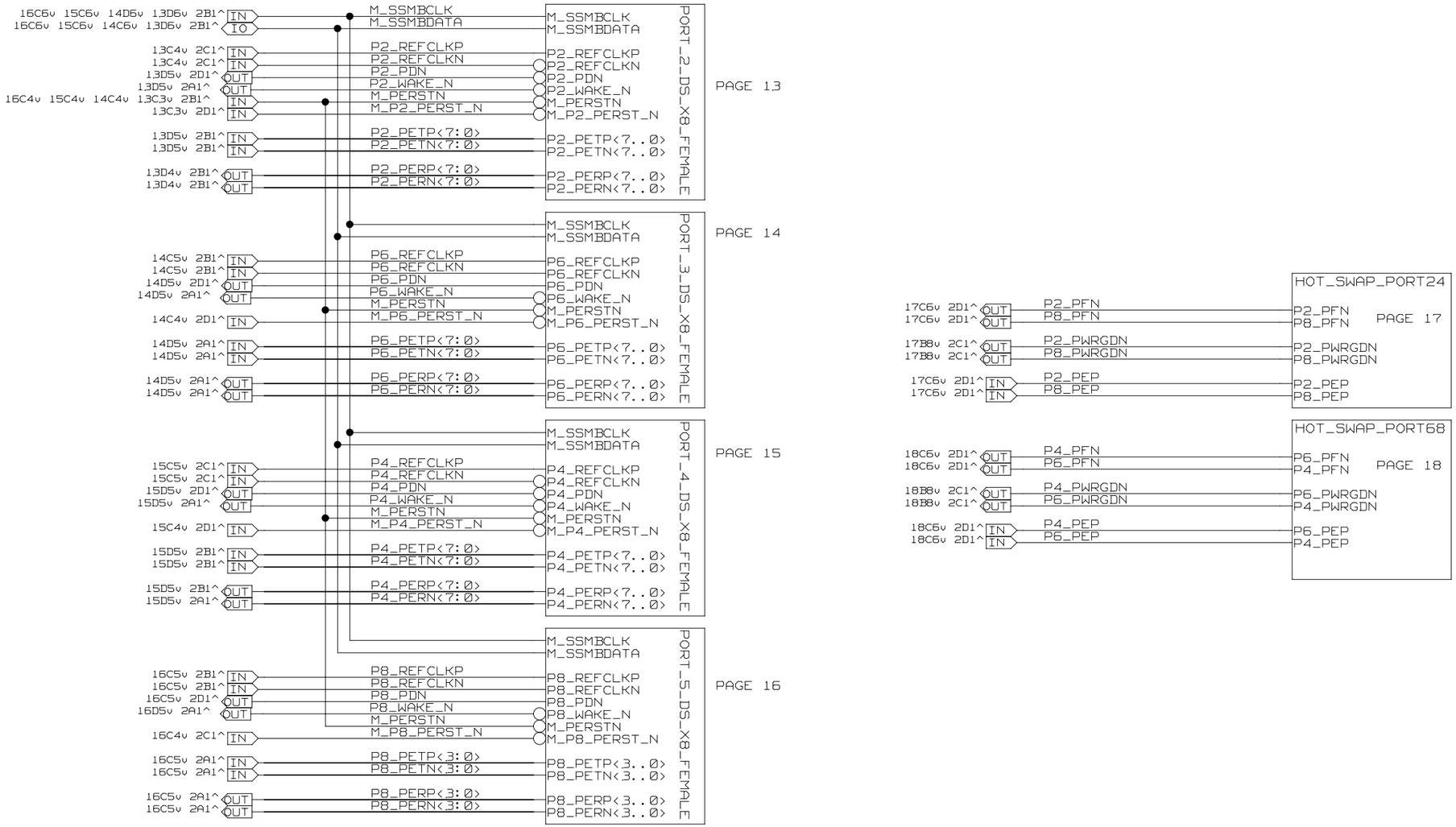
TITLE 89HPES48H12G2 Eval Board

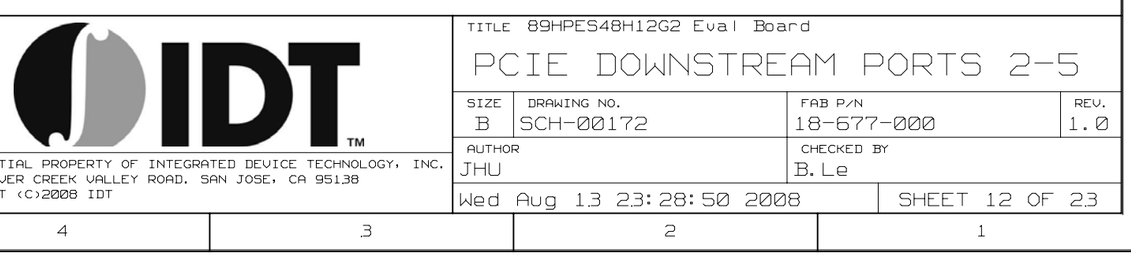
CONNECTOR EDGE US PCIE X8

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-00172	18-677-000	1.0

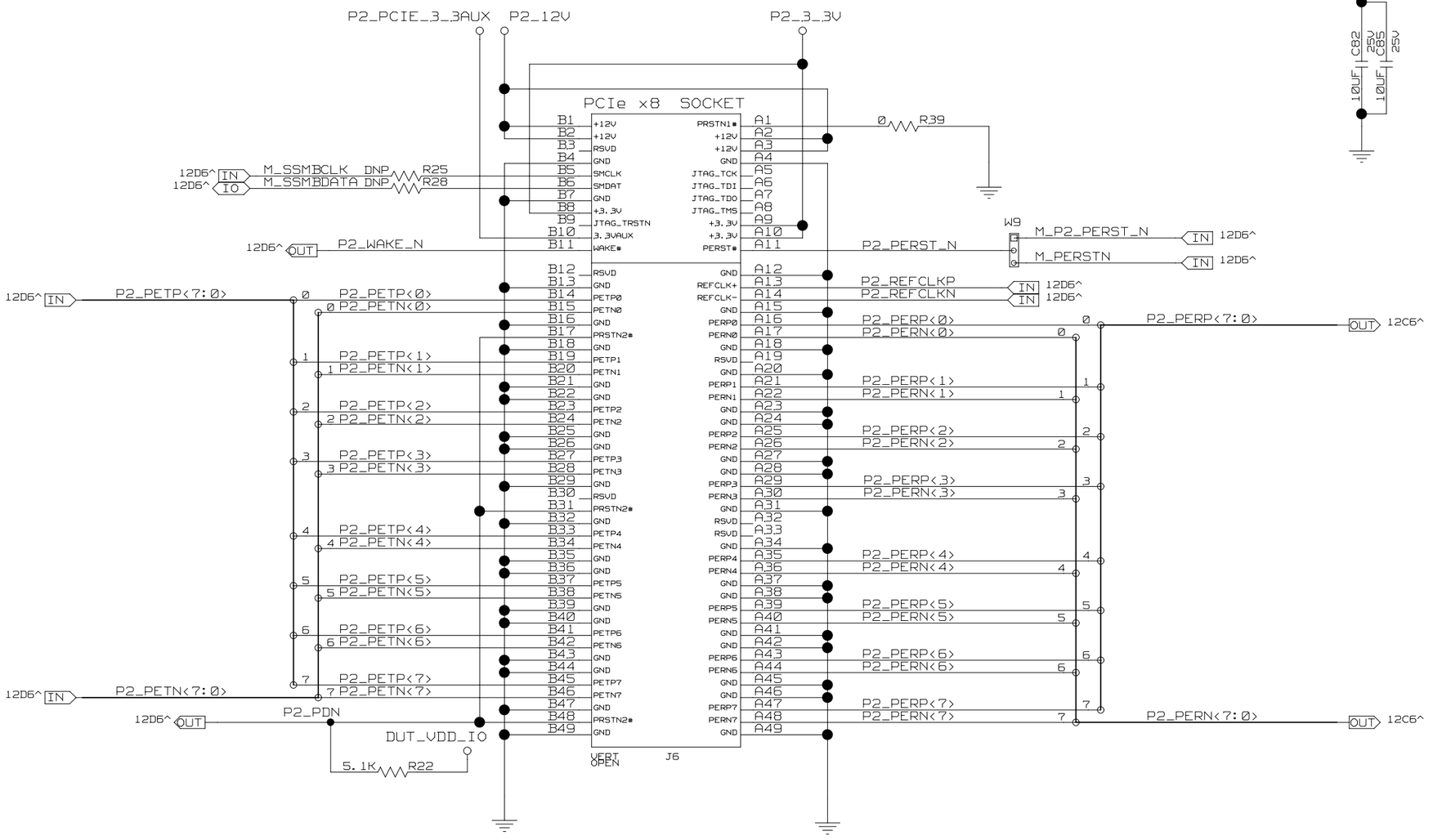
AUTHOR	CHECKED BY
JHU	B. Le

Tue Aug 19 16:43:28 2008 SHEET 11 OF 23





TITLE	89HPES48H12G2 Eval Board		
	PCIE DOWNSTREAM PORTS 2-5		
SIZE: B	DRAWING NO.: SCH-00172	FAB P/N: 18-677-000	REV.: 1.0
AUTHOR: JHU		CHECKED BY: B.Le	
Wed Aug 13 23:28:50 2008			SHEET 12 OF 23



SILKSCREEN LABEL:

CONECTOR J6

SLOT 2 PCIE2 X8(8,4,2,1)

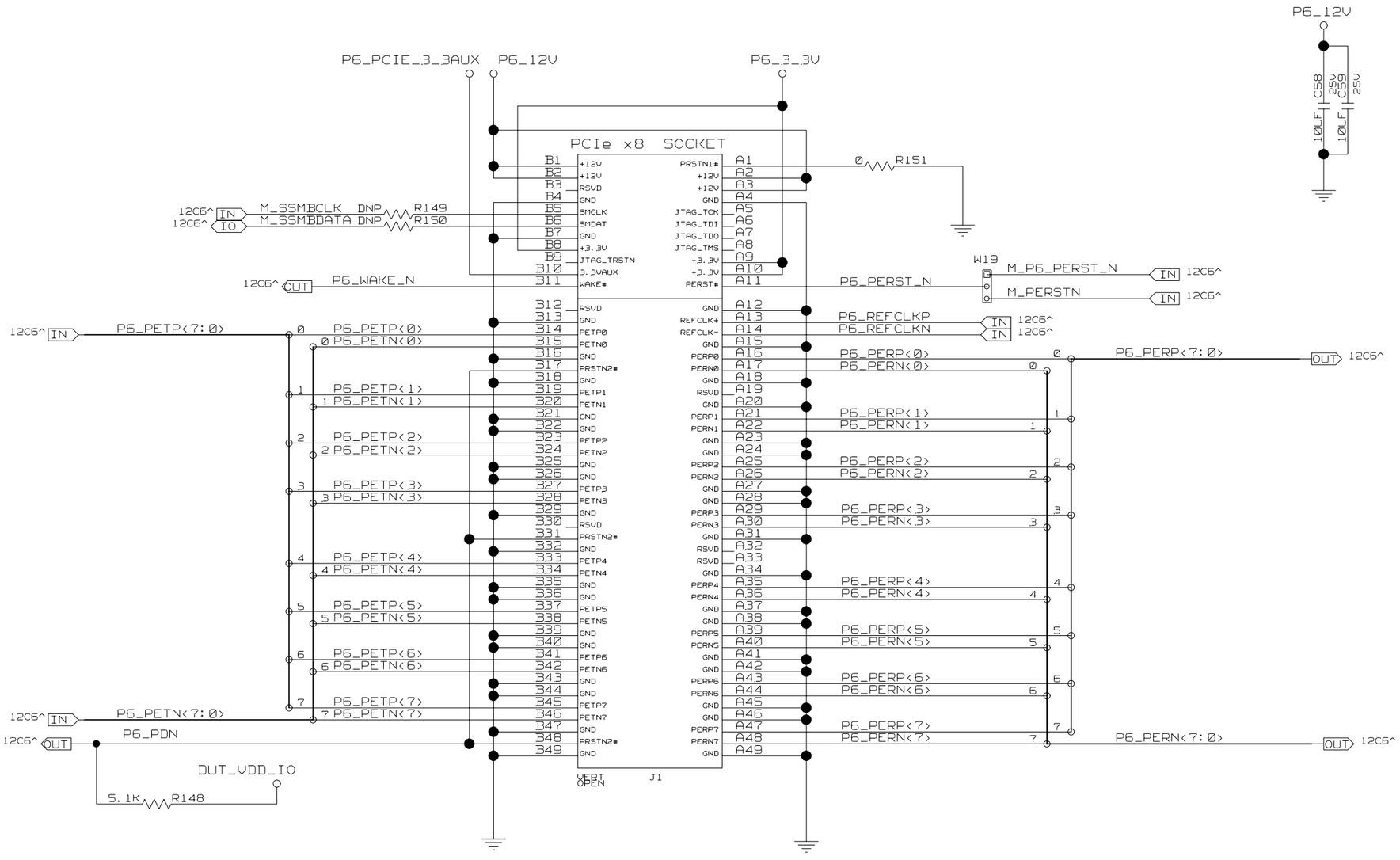
TITLE 89HPES48H12G2 Eval Board

PORT 2 PCIE X8 CONNECTOR

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-00172	18-677-000	1.0

AUTHOR	CHECKED BY
JHU	B.Le

Tue Aug 19 16:44:21 2008 SHEET 13 OF 23

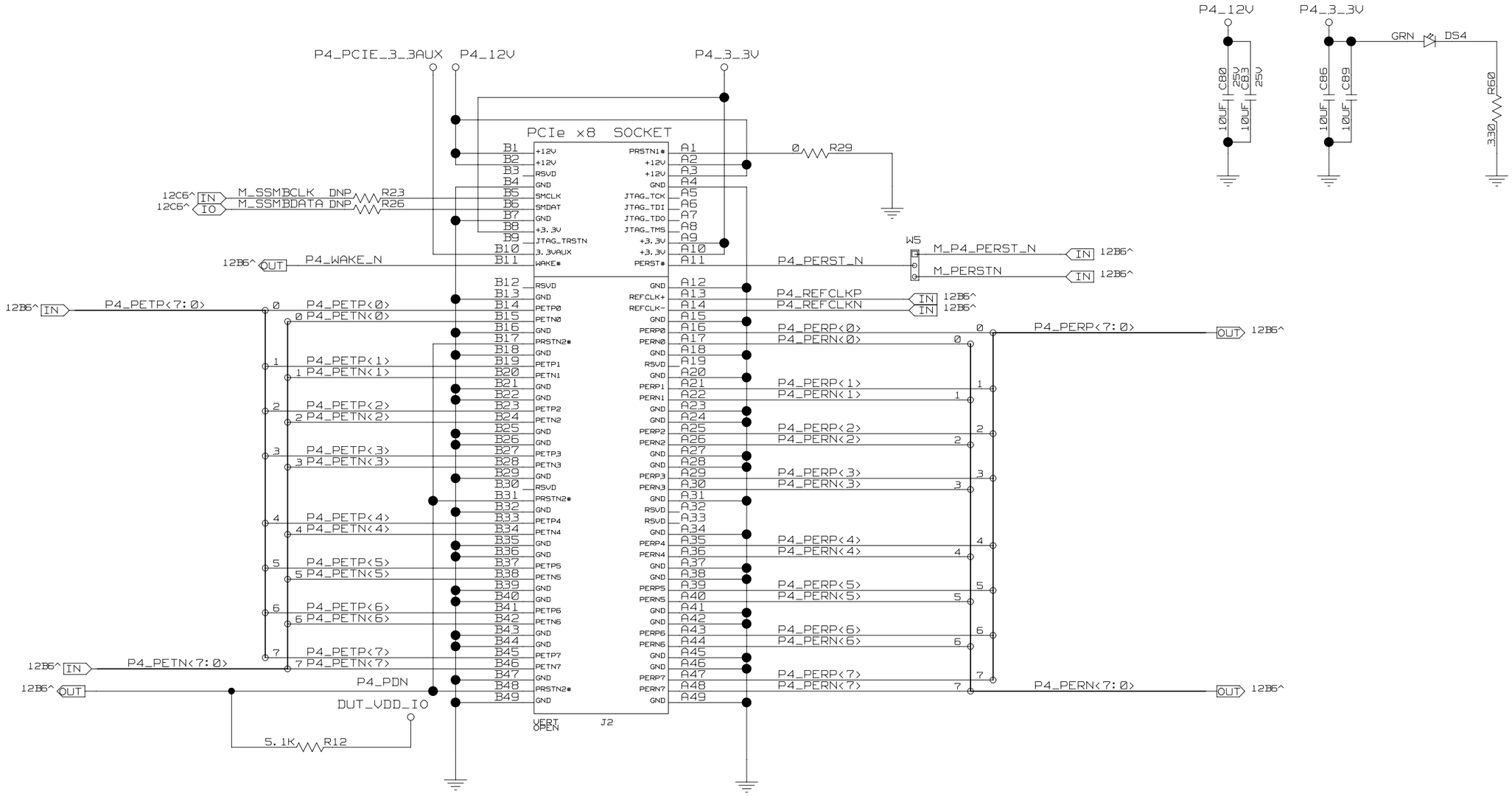


SILKSCREEN LABEL:

CONECTOR J1

SLOT 6 PCIE2 X8(8,4,2,1)

TITLE	89HPES48H12G2 Eval Board		
PORT 6 PCIE X8 CONNECTOR			
SIZE: B	DRAWING NO.: SCH-00172	FAB P/N: 18-677-000	REV.: 1.0
AUTHOR: JHU		CHECKED BY: B.Le	
Tue Aug 19 16:43:54 2008		SHEET 14 OF 23	

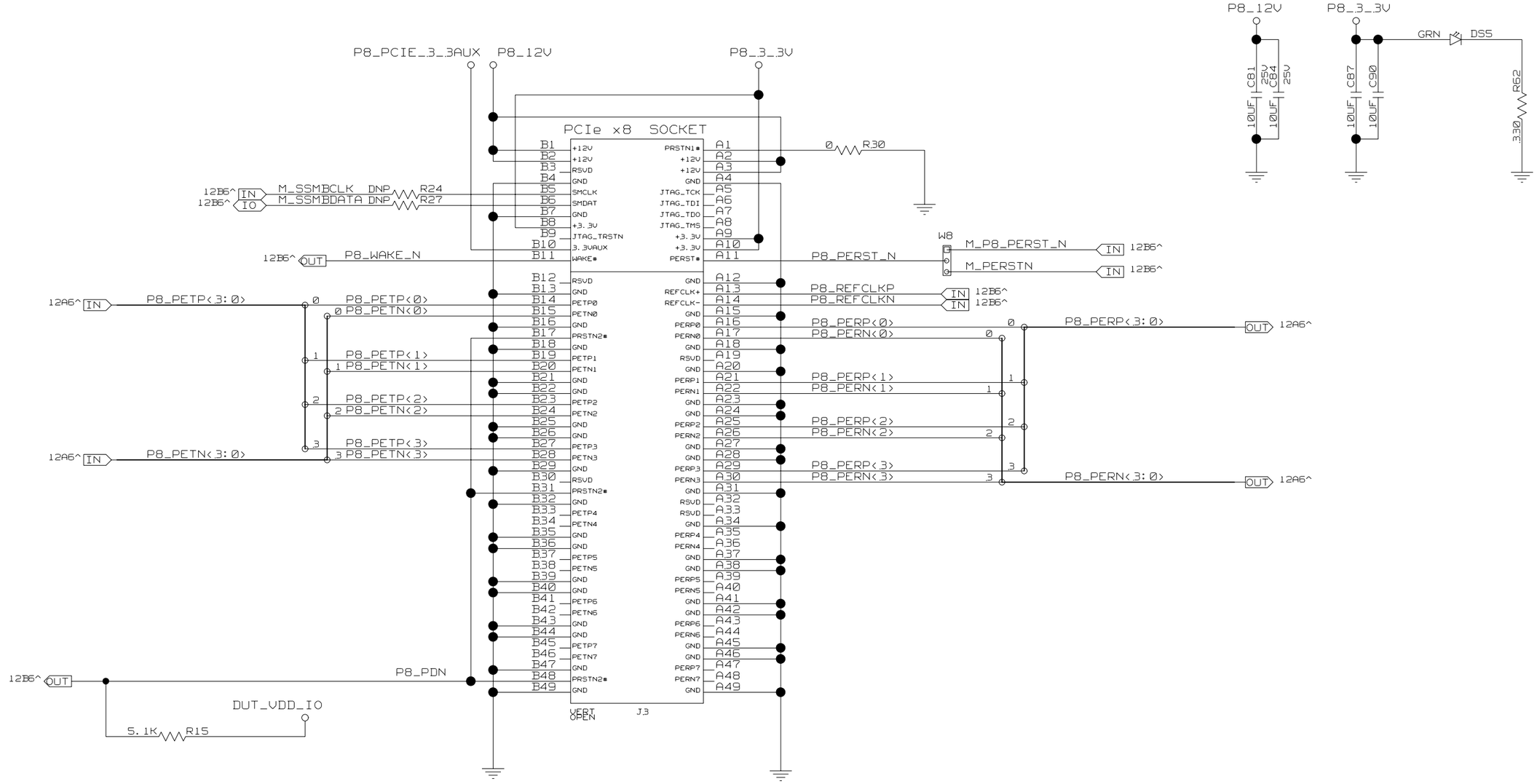


SILKSCREEN LABEL:

CONECTOR J2

SLOT 4 PCIE2 X8(8,4,2,1)

TITLE 89HPES48H12G2 Eval Board			
PORT 4 PCIE X8 CONNECTOR			
SIZE B	DRAWING NO. SCH-00172	FAB P/N 18-677-000	REV. 1.0
AUTHOR JHU		CHECKED BY B.Le	
Tue Aug 19 16:44:03 2008		SHEET 15 OF 23	



SILKSCREEN LABEL:

CONECTOR J3

SLOT 8 PCIE2 X8(4,2,1)

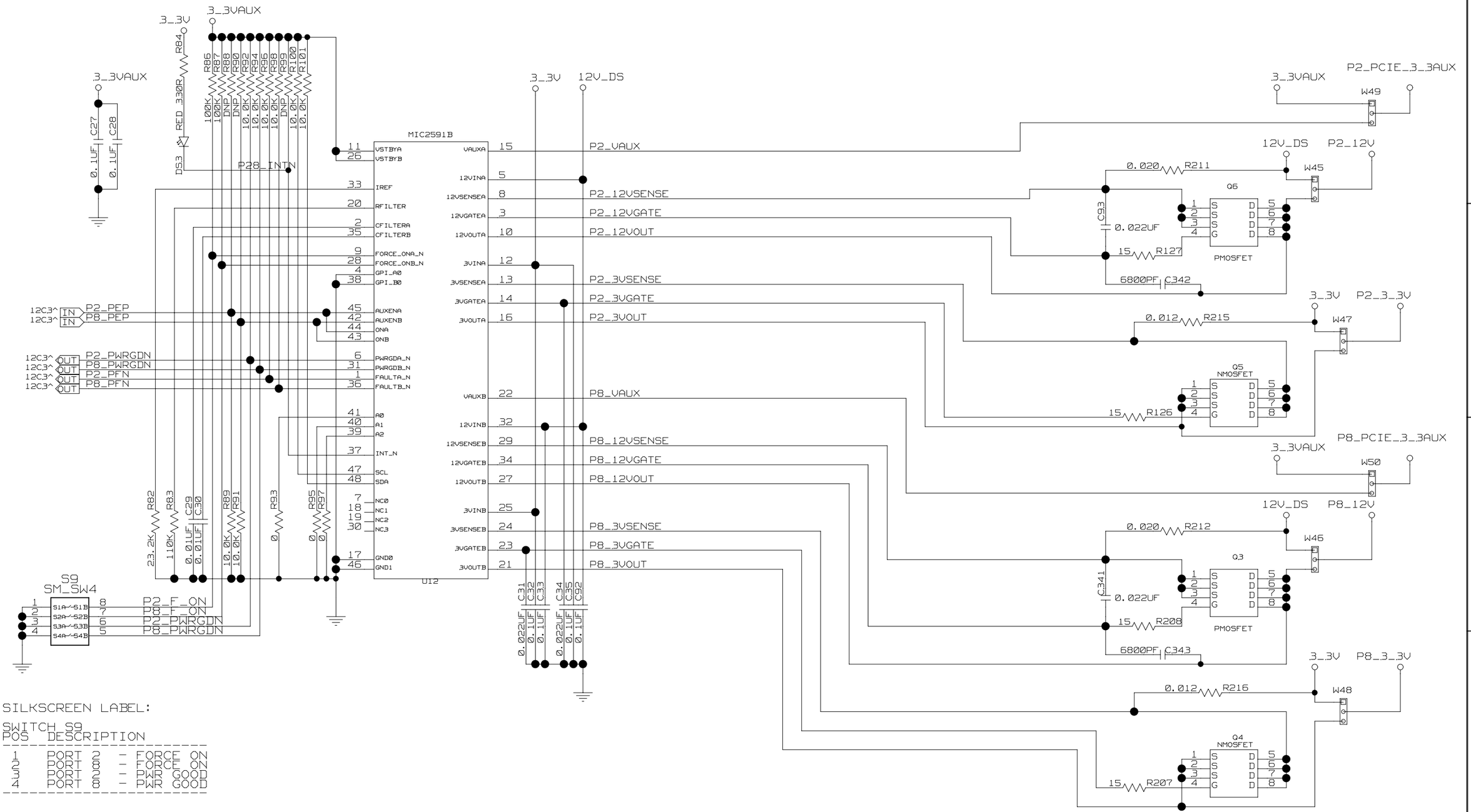
TITLE 89HPES48H12G2 Eval Board

PORT 8 PCIE X8 CONNECTOR

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-00172	18-677-000	1.0

AUTHOR	CHECKED BY
JHU	B.Le

Tue Aug 19 16:44:06 2008 SHEET 16 OF 23



SILKSCREEN LABEL:

SWITCH S9

POS	DESCRIPTION
1	PORT 2 - FORCE ON
2	PORT 8 - FORCE ON
3	PORT 2 - PWR GOOD
4	PORT 8 - PWR GOOD

TITLE 89HPES48H12G2 Eval Board

HOT SWAP PORT 2, 8

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-00172	18-677-000	1.0

AUTHOR	CHECKED BY
JHU	B. Le

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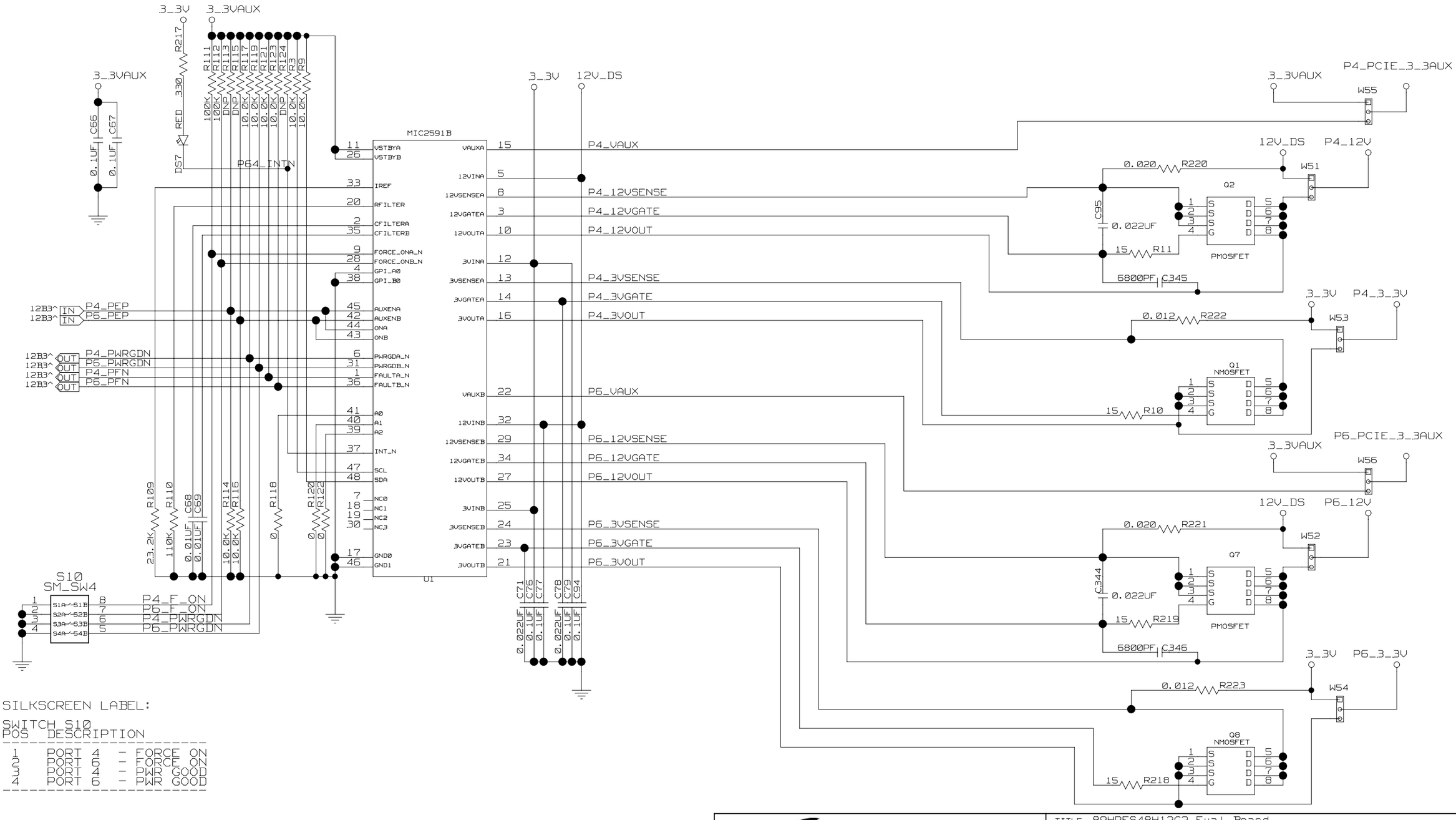


SILKSCREEN LABEL:

SWITCH S10

POS	DESCRIPTION
1	PORT 4 - FORCE ON
2	PORT 6 - FORCE ON
3	PORT 4 - PWR GOOD
4	PORT 6 - PWR GOOD

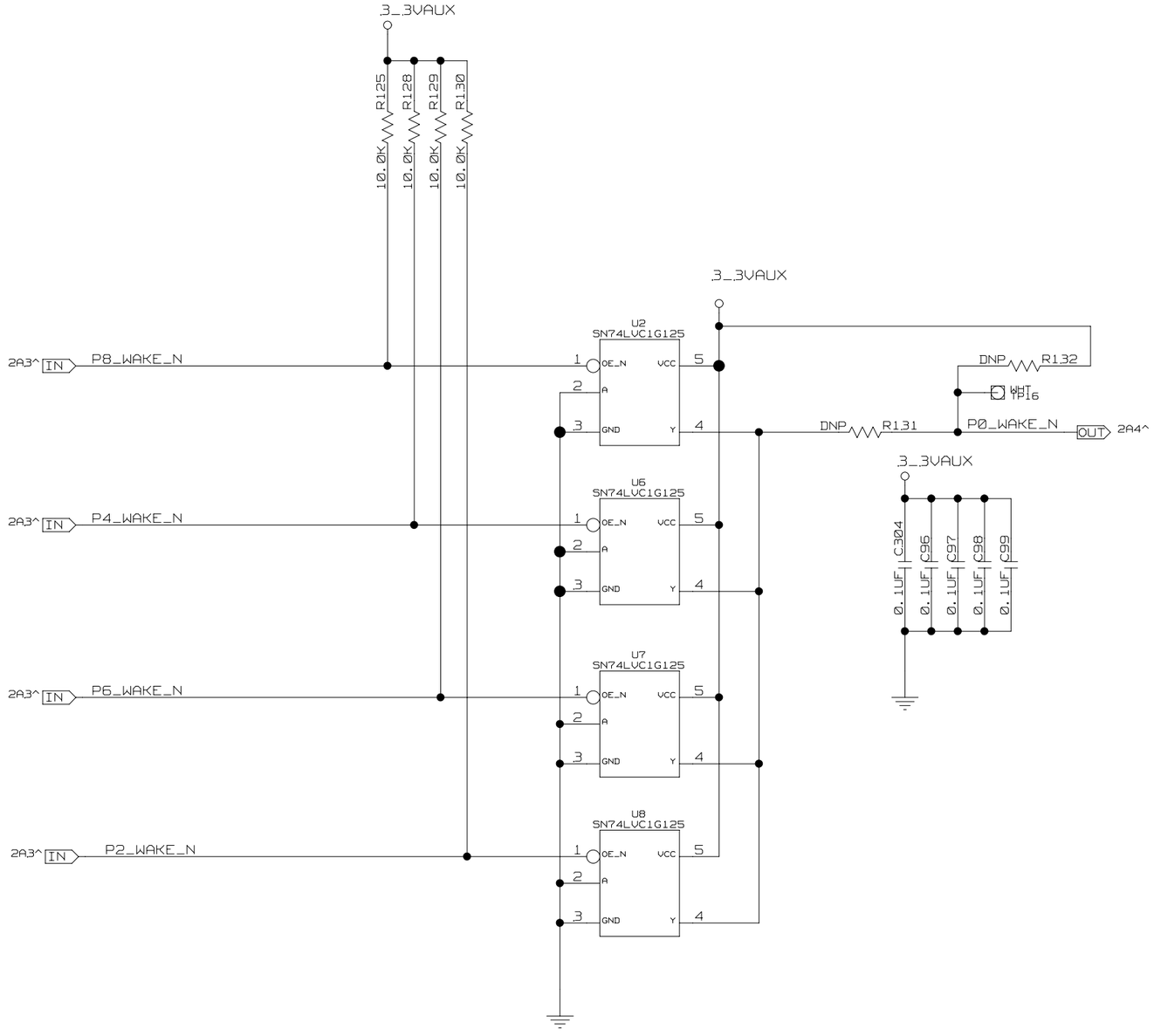
TITLE 89HPES48H12G2 Eval Board

HOT SWAP PORT 6, 4

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-00172	18-677-000	1.0

AUTHOR	CHECKED BY
JHU	B. Le

Tue Aug 19 16:44:13 2008 SHEET 18 OF 23



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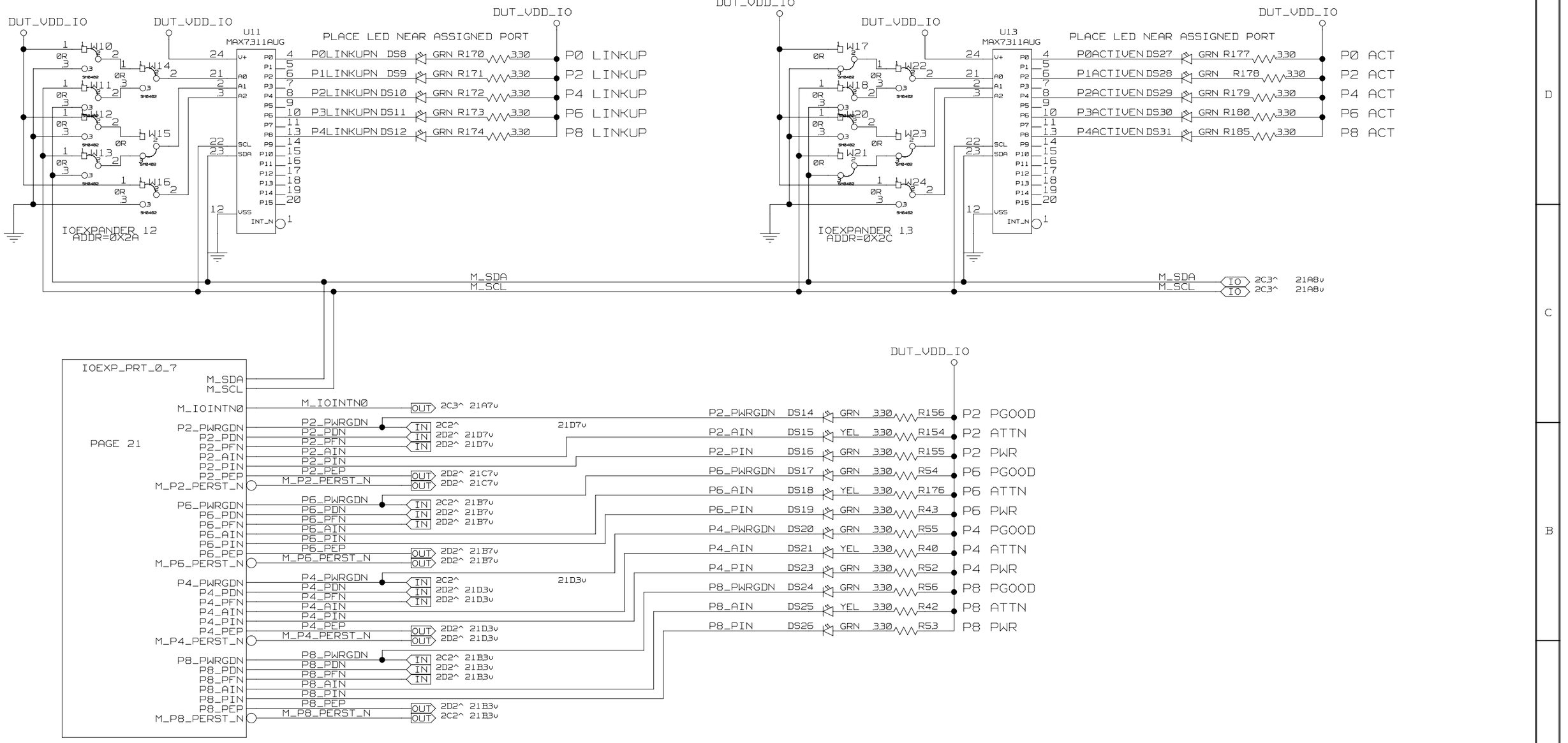
TITLE 89HPES48H12G2 Eval Board

PORT WAKE BUFFER

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-00172	18-677-000	1.0

AUTHOR	CHECKED BY
JHU	B. Le

Tue Aug 19 16:43:31 2008 SHEET 19 OF 23



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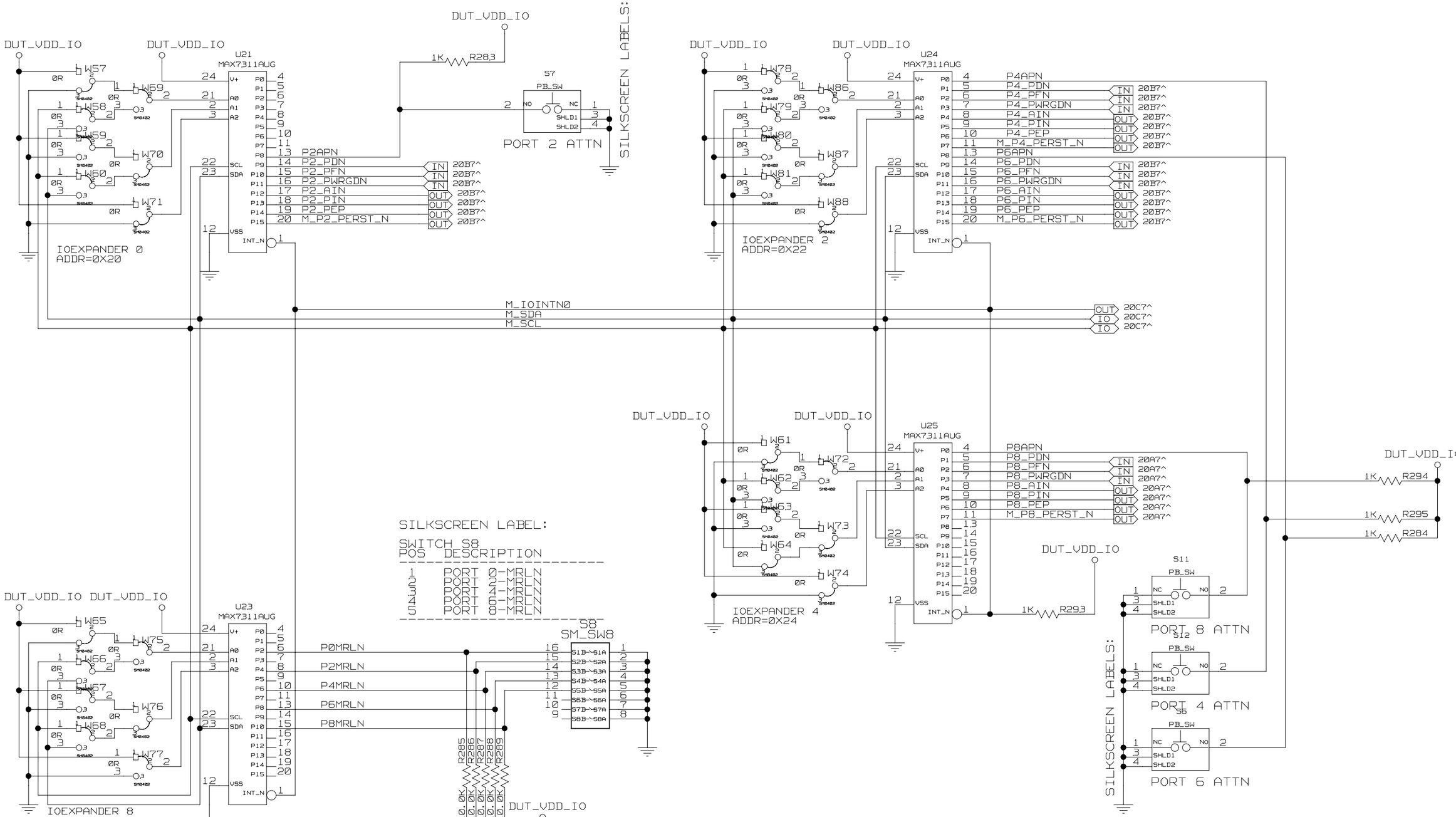
TITLE 89HPES48H12G2 Eval Board

IO EXP, WAKE, ATTN BUTTONS

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-00172	18-677-000	1.0

AUTHOR	CHECKED BY
JHU	B. Le

Tue Aug 19 16:43:23 2008 SHEET 20 OF 23



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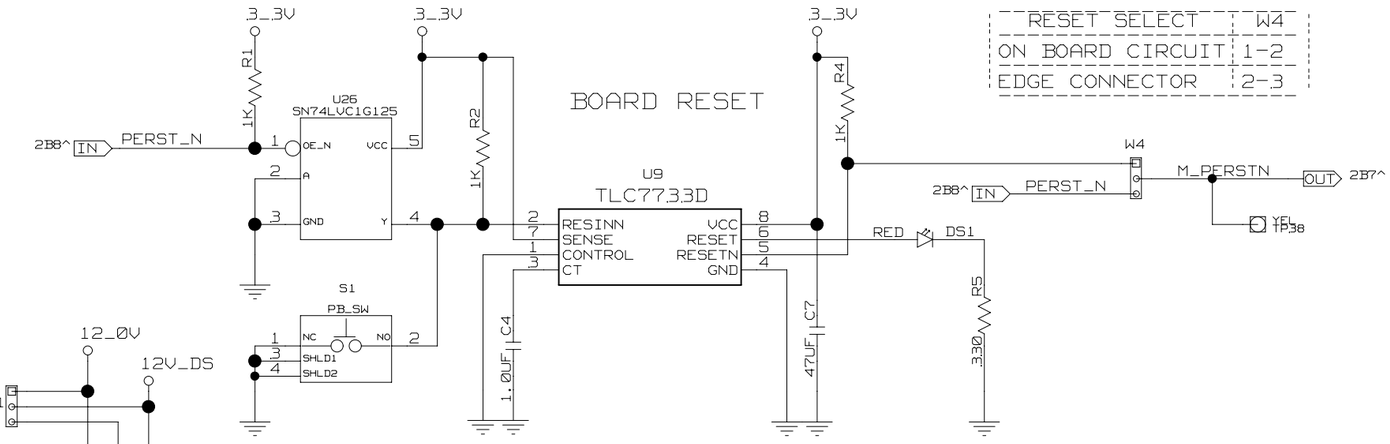
TITLE 89HPES48H12G2 Eval Board			
I/O EXPANDER 0-4			
SIZE B	DRAWING NO. SCH-00172	FAB P/N 18-677-000	REV. 1.0
AUTHOR JHU		CHECKED BY B. Le	
Tue Aug 19 16:43:26 2008		SHEET 21 OF 23	

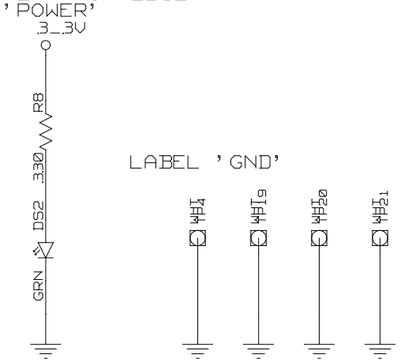
BOARD RESET



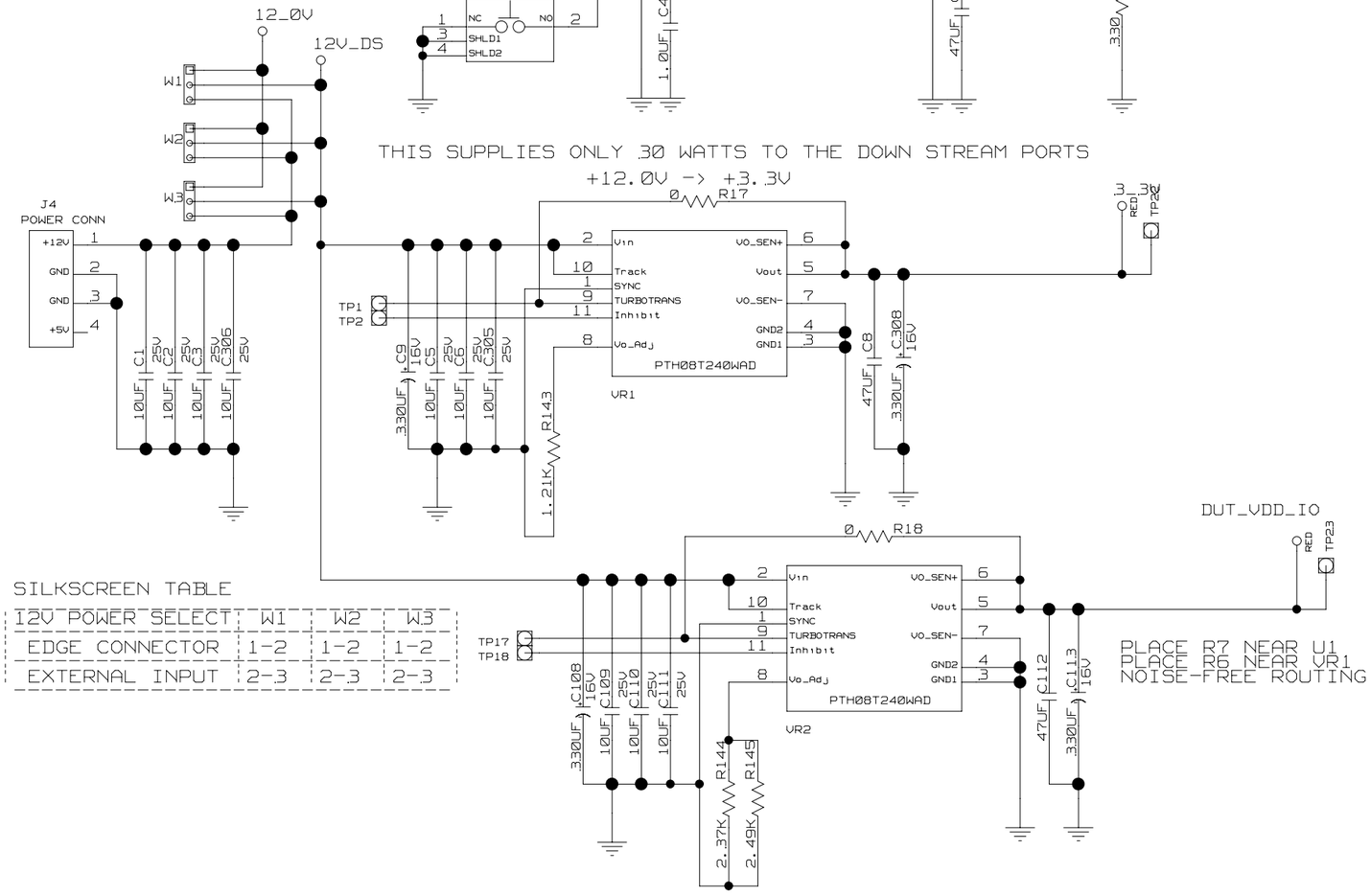
SILKSCREEN TABLE

RESET SELECT	W4
ON BOARD CIRCUIT	1-2
EDGE CONNECTOR	2-3

POWER INDICATOR PLACE NEAR TOP EDGE LABEL 'POWER'



THIS SUPPLIES ONLY 30 WATTS TO THE DOWN STREAM PORTS +12.0V -> +3.3V



SILKSCREEN TABLE

12V POWER SELECT	W1	W2	W3
EDGE CONNECTOR	1-2	1-2	1-2
EXTERNAL INPUT	2-3	2-3	2-3

PLACE R7 NEAR U1
PLACE R6 NEAR VR1
NOISE-FREE ROUTING

REMOVE 2.49K TO SET VDD_IO TO 2.5V

POWER_SUPPLIES
PAGE 23

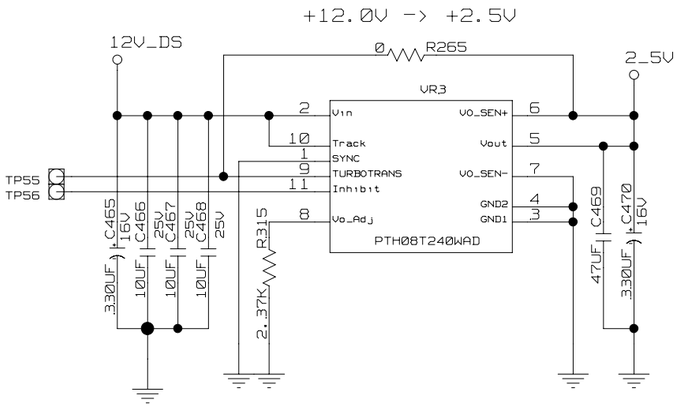
TITLE 89HPES48H12G2 Eval Board

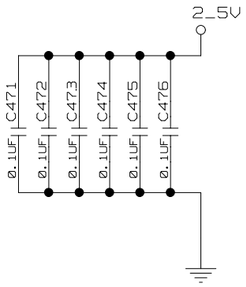
SWITCHING REGULATORS

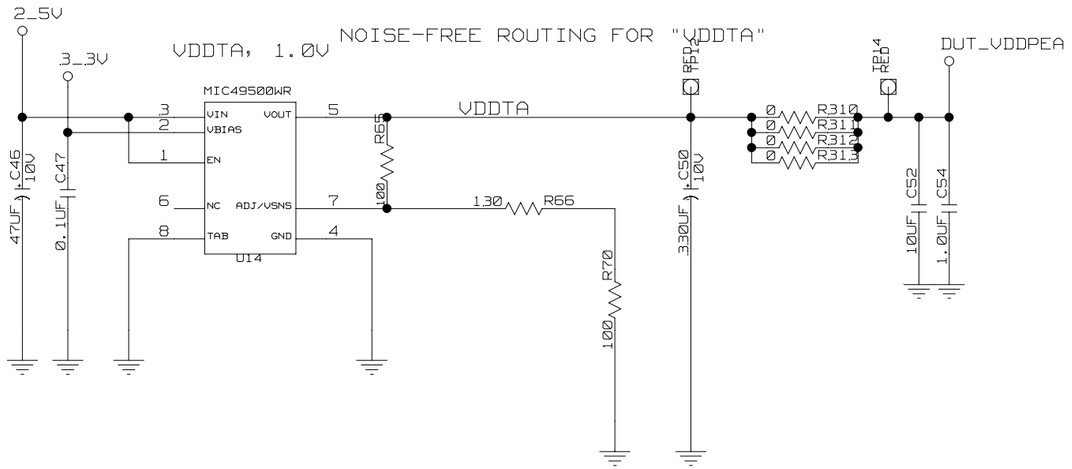
SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-00172	18-677-000	1.0

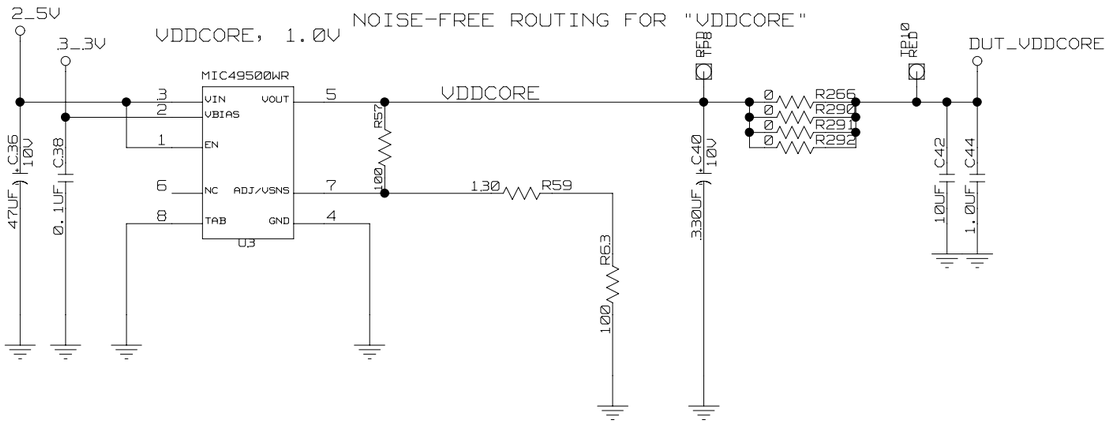
AUTHOR	CHECKED BY
JHU	B. Le

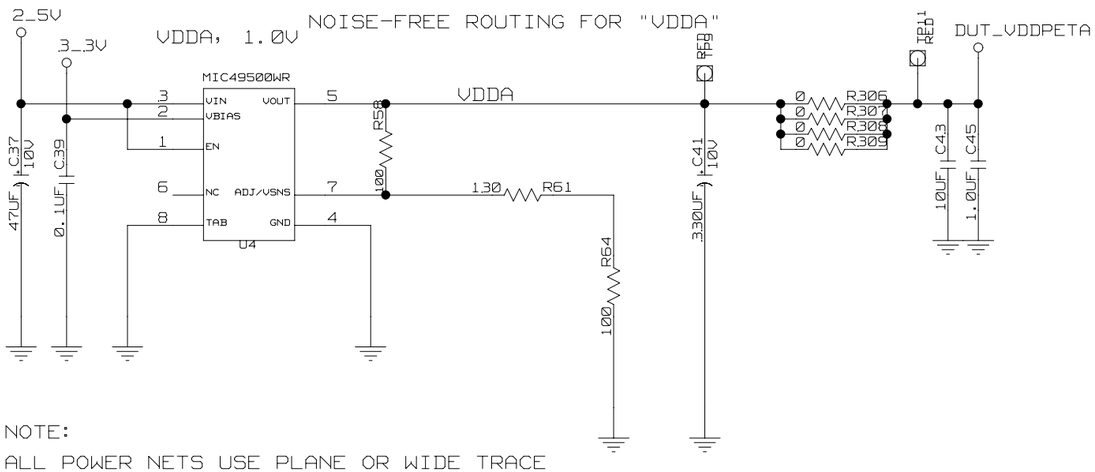
Tue Aug 19 16:43:02 2008 SHEET 22 OF 23



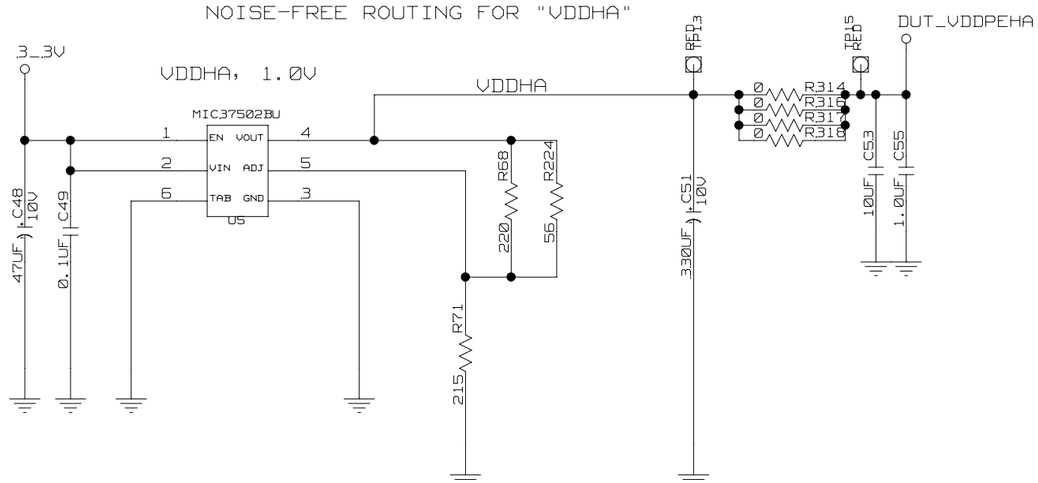








NOTE:
ALL POWER NETS USE PLANE OR WIDE TRACE



DEFAULT SUPPLY SET TO 1.5V REMOVE 56R RESISTOR FOR 2.5V

COPPER AREA AS LARGE AS POSSIBLE

NOTE:
ALL POWER NETS USE PLANE OR WIDE TRACE

TITLE 89HPES48H12G2 Eval Board			
SWITCHING REGULATORS			
SIZE B	DRAWING NO. SCH-00172	FAB P/N 18-677-000	REV. 1.0
AUTHOR JHU		CHECKED BY B. Le	
Tue Aug 19 16:43:06 2008		SHEET 23 OF 23	

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