

Description

The 8Axxxx 144BGA EVK is designed to help customers evaluate IDT ClockMatrix devices. This document discusses the following about the EVK:

- Introduces the board and its power supply and jumper settings
- Describes the input and output connectors for normal operation
- Explains how to bring up the board using the Timing Commander software GUI
- Discusses how to configure and program the board to generate standard-compliant frequencies

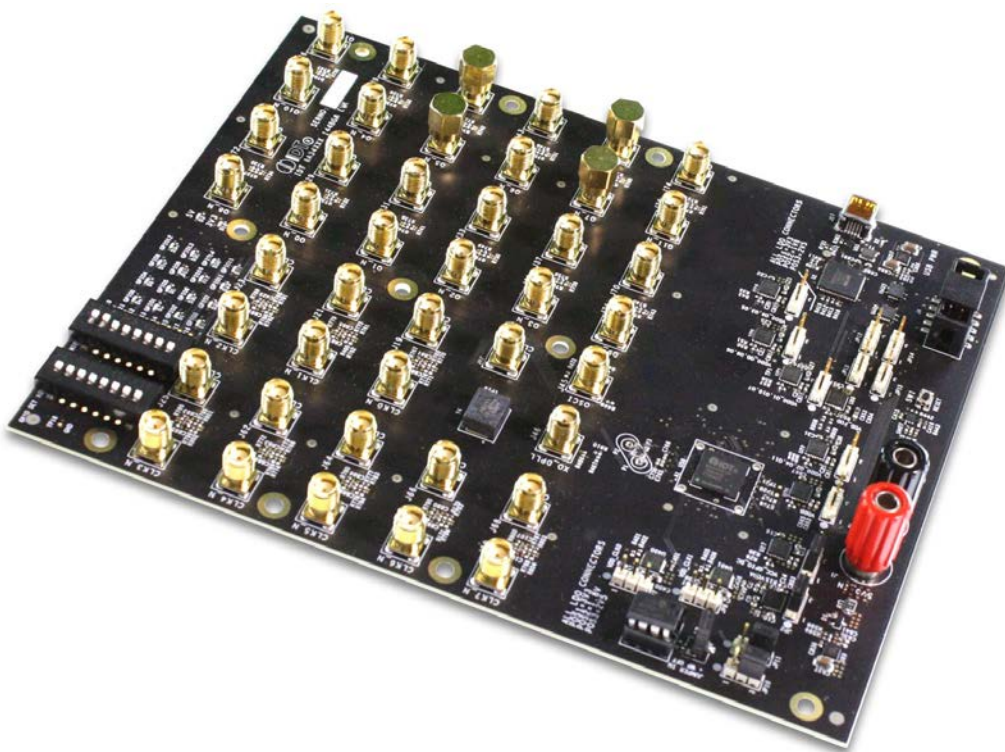
Requirements

- IDT Timing Commander Software Installed (available at www.idt.com/timingcommander)
- ClockMatrix GUI (available at www.idt.com/clockmatrix)
- USB 2.0 or USB 3.0 interface
- Windows XP SP3 or later
- Processor: Minimum 1GHz
- Memory: Minimum 512MB; recommended 1GB
- Available disk space: Minimum 600MB (1.5GB 64-bit); recommended 1GB (2GB 64-bit)
- Network access during installation if the .NET framework is not currently installed on the system

Kit Contents

- 8A34xxx 144BGA Evaluation Board
- USB Type A cable

8A3xxxx 144BGA EVK Board



Important Notes

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- (iii) misuse, abuse, use under abnormal conditions, or alteration by anyone other than IDT.

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Important Equipment Warning: Ensure the correct connection of all cables. Supplying the board using the wrong polarity could result in damage to the board and/or the equipment. Check that all jumpers have been removed from the board before applying power.

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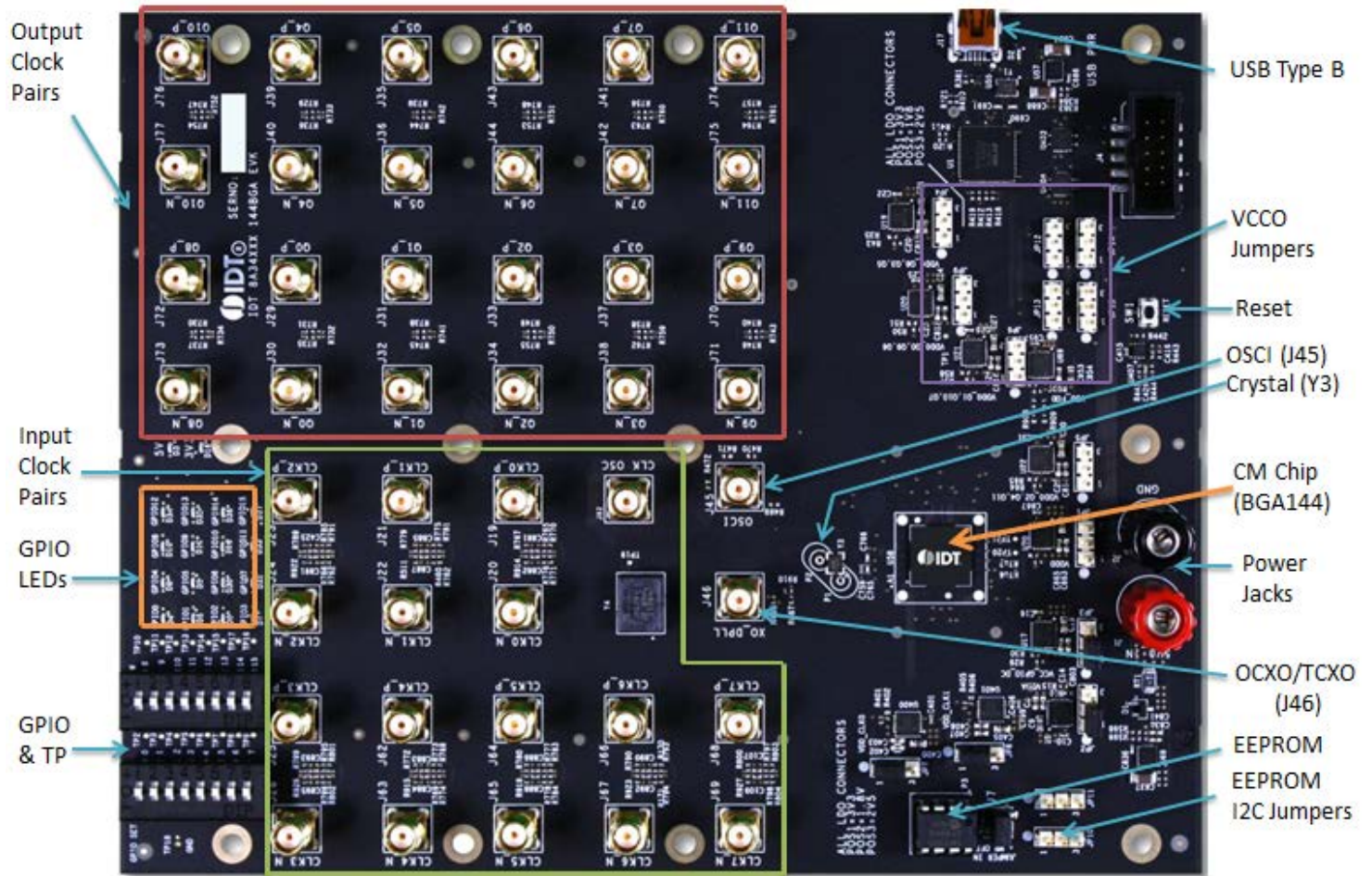
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1. Usage Guide

1.1 Board Overview

The following diagram identifies various components of the board: input and output SMA connectors, power supply jacks, and some jumper settings necessary for the board operations.

Figure 1. Overview of 144BGA ClockMatrix Evaluation Board



Detailed descriptions of the board are as follows.

- Input SMA Connectors – There are eight differential inputs labeled CLK0/nCLK0-CLK7/nCLK7. Each input clock can be configured differentially (LVDS, PECL 2.5V, and PECL 3.3V) or in single-ended format (CMOS).
- Output SMA Connectors – There are 12 outputs labeled as Q0/nQ0-Q11/nQ11. Each output clock can be configured differentially (LVDS, LVPECL, or user-defined amplitude), or in single-ended format (LVCMOS – in-phase or out-of-phase)
- GPIO switch, LEDs, and test points – There are 16 GPIOs available. Each GPIO can be set a “low” or “high” level (if input) or displayed with an LED (if output). Some GPIOs are used to set the chip in a certain working condition on power-up. For more information, see GPIO Switches, LEDs, and Test Points.
- USB connector – A USB mini-connector connects the evaluation board to a PC for GUI communications. No power is drawn from the USB connector other than to power the FTDI USB chip.

- VCCO voltage selection jumpers – Each output voltage can be individually supplied with 1.8V, 2.5V, or 3.3V. These jumpers are used to select the voltage for the output voltages.
- Reset button – A small button is used to reset the board.
- OSCI Input connector – An SMA connector, J45, can optionally supply a clock signal to overdrive the crystal.
- OCXO/TCXO reference – An SMA connector, J46, can supply a local OCXO/TCXO reference as an optional reference for System DPLL.
- Crystal – A crystal of various frequencies must be present for board operations. A 3225 footprint is provided for SMT crystals. For easy plug-in of a canned crystal, two through holes are also available.
- EEPROM – An SO-8 socket is provided to hold an EEPROM device of compatible package. EEPROM is used to store firmware and customer configuration data, if needed.

1.2 Board Power Supply

The board uses a single +5V supply for its power supplies. When running the board, set the bench power supply at 5V/2A. The red jack (J1) is positive; the black jack (J2) is the ground.

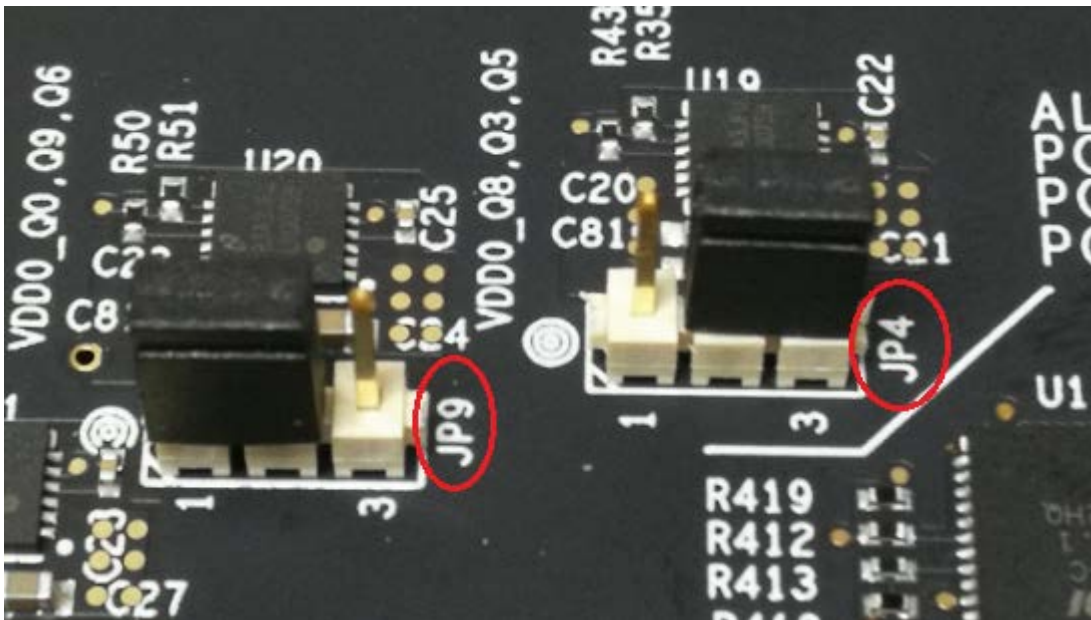
Multiple LDOs are used to generate 3.3V, 2.5V, and 1.8V from the +5V supply.

1.3 Voltage Selection Jumpers

There are nine headers/jumpers to select different voltages for different functional blocks of the chip. Each head is labeled pin 1 and pin 3 – jumping pin 1 and pin 2 will select 3.3V; jumping pin 2 and pin 3 will select 2.5V; no jumper will have 1.8V.

Please see the following example for JP4 and JP9 – JP4 will select 2.5V; JP9 will select 3.3V.

Figure 2. Example of Voltage Jumpers



The following list shows which head/jumper is used to select what voltage:

- JP1 – VDDD
- JP2 – VDDA
- JP3 – VCC_GPIO_DC
- JP4 – VDDO_Q8_3_5
- JP5 – VDDO_Q2_4_11
- JP6 – VDDO_1_10_7
- JP7 – VDD_CLK0
- JP8 – VDD_CLK1
- JP9 – VDDO_Q0_9_6



Important Equipment Warning: VDD_FOD voltage is selected by resistors R908 and R909. In order to prevent damage to the device, both R908 and R909 should not be stuffed, in which case VDD_FOD = 1.8V.

1.4 GPIO Switches, LEDs, and Test Points

Two 8-bit dip switches sets the logic levels for 16 GPIOs. The following table shows the GPIO levels for each setting and the corresponding LED state.

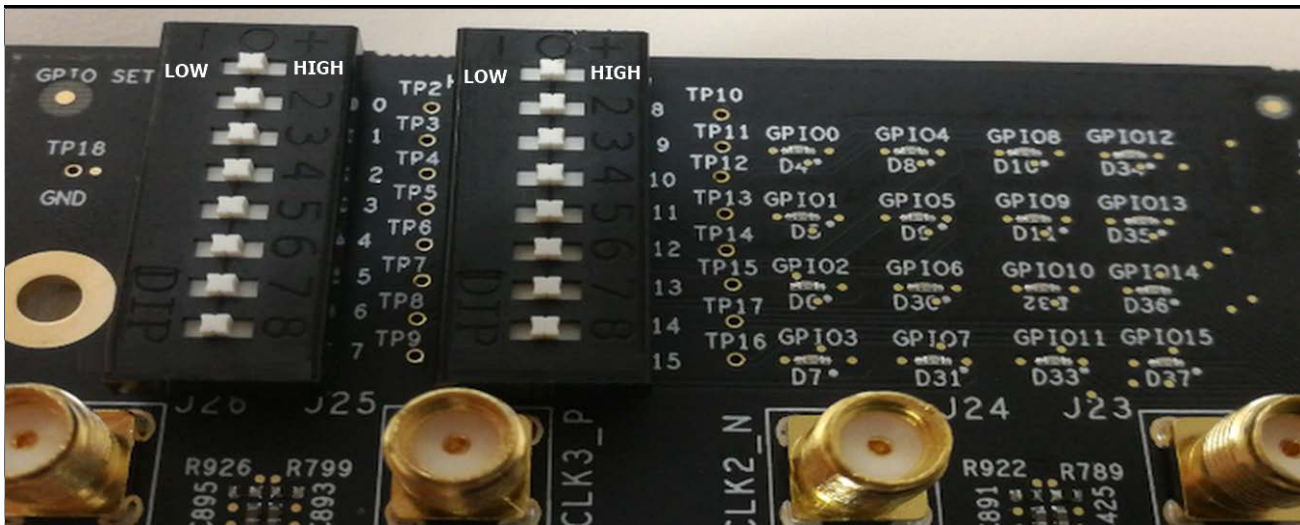
Table 1. GPIO Settings

Dip Switch Position	GPIO Logic Level	LED
Left	Low	On
Center	High if GPIO is configured as Input High or Low according to the GPIO output setting	High if GPIO is configured as Input High or Low according to the GPIO output setting
Right	High	Off

Please see the picture and labels in Figure 3.

When the GPIOs are configured as outputs (such as User-Controlled or LOL indicator), the dip switch for the corresponding GPIO should be placed in the center position. The LED will indicate the state of the GPIO.

Figure 3. GPIO Setting and Status Display Area



1.5 USB Jack

The board has a USB mini-connector. The other end of the USB cable is a USB Type A connector going to a PC.

1.6 Onboard EEPROM

An onboard EEPROM is used to store device firmware and/or customer's configuration data. There are two headers/jumpers, JP10 and JP11, used to select the I²C communication paths for the EEPROM.

Table 2. EEPROM I²C Connections

	JP10/JP11	JP10/JP11
Jumper Position	Both Pin 1 and 2	Both Pin 2 and 3
EEPROM I ² C Path	FDTI and EEPROM	EEPROM and CM Chip

2. Working with Timing Commander™ for Programming/Configuration

The following sections are best cross-referenced with the *ClockMatrix GUI Step-by-Step User Guide* which is available on www.idt.com.

2.1 Default Operation

The board can operate off an EEPROM that has stored all information including firmware and a default configuration data. A default operation provides a sanity check on the board before running the board through the IDT Timing Commander. Please set the board in the following default conditions (see Figure 4 for jumper and switch positions).

- Set all the GPIOs to the center position. This will ensure that GPIO8 and GPIO9 are high and that the serial port is configured for I²C 1-byte addressing.
- VDDA = 3.3V, VCC_GPIO_DC = 3.3V, and VDDO_Qx = 3.3V
- Crystal frequency = 50MHz
- CLK0 = 25MHz
- EEPROM is connected to ClockMatrix chip through an I²C bus by jumping Pin 2 and 3 of JP10 and JP11

With the above default conditions ready, connect the board to the PC using a USB type A to USB mini cable, and power up the board using a single +5V supply. On power-up, the ClockMatrix chip will read its firmware and configuration data from EEPROM and update all registers. When this process is completed, the following frequencies are available:

Q0 = 122.88MHz

Q1 = 122.88MHz

Figure 4. Board Setting for Default Operation

Crystal = 38.88MHz

Jump Pin 1 and 2 on JP2 and JP3

Jump Pin 2 and 3 on JP10 and JP11

+5V Power Supply



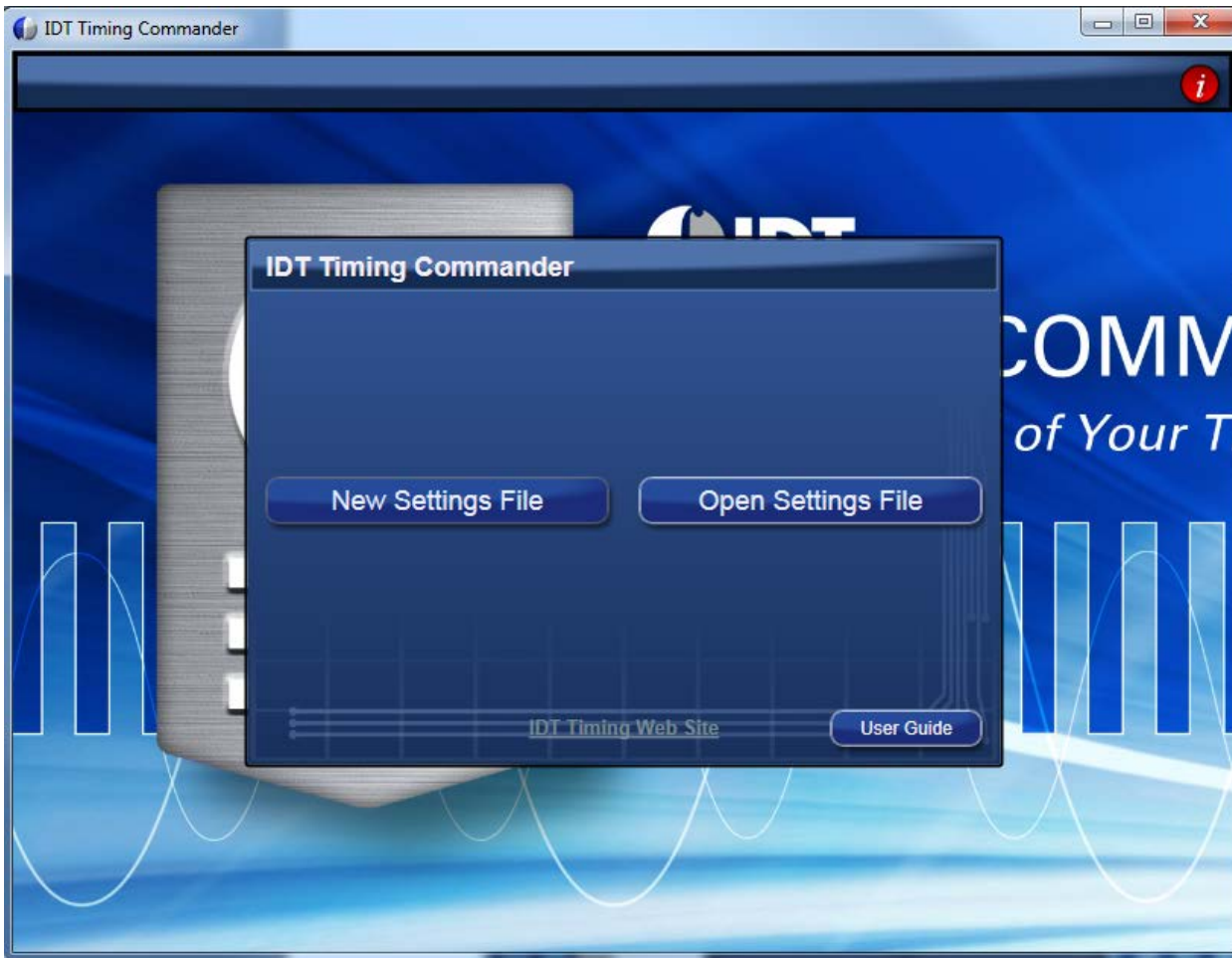
Important Equipment Warning: In order to set GPIO8 and GPIO9 to "High", the switches for GPIO8 and GPIO9 must be set either to the "+" (high) position or the center position.

2.2 Using Timing Commander to Control the Board

Once the default operation is successful, complete the following steps to configure and program the ClockMatrix device per your specific application requirements using Timing Commander GUI tools:

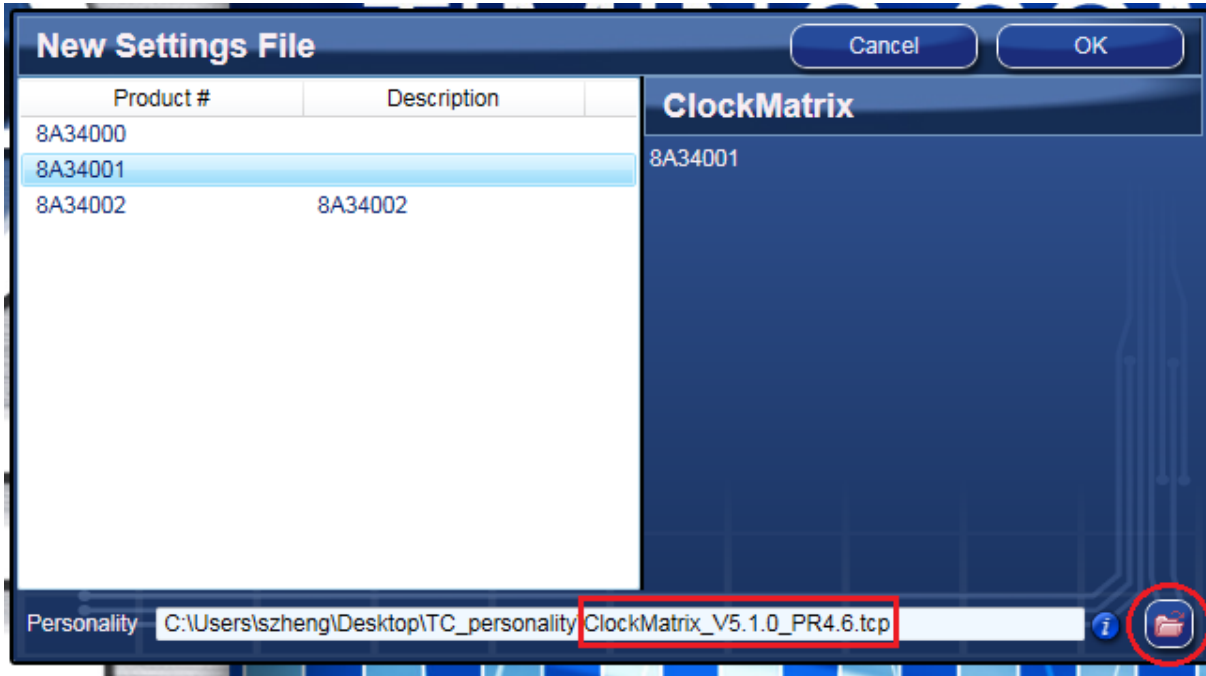
1. Power up the board and set the main serial port in I²C mode by GPIO9 = "high". Set GPIO8 = "High". Connect the board to the PC.
2. Start the Timing Commander software. You will see options of "New Setting File" and "Open Setting file". For a new configuration, select "New Setting File".

Figure 5. Starting Up Timing Commander GUI



- After selecting "New Settings File", a device selection window will pop up. In the window, choose the intended device in the list (in this example, 8A34001 is selected). Click the button at the lower right corner of the window (red circle) to browse and select the correct personality file (in this example, personality v4.6 is selected). Click OK.

Figure 6. Selecting 8A34001 using Personality File v4.6



- The GUI window with the 8A34001 block diagram will open for configurations; or if "Open Settings File" is selected in Step 3, you will be prompted to browse and select an existing .tcs file and the personality file. When the configuration file is open, all configured values will be displayed (see Figure 7).

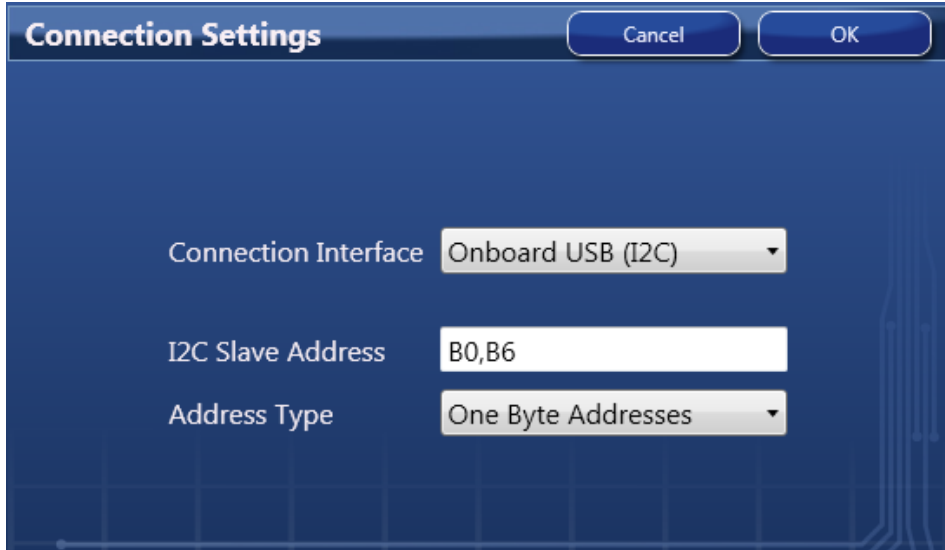
Figure 7. Timing Commander GUI with a Settings File Opened



- In order to connect the board with Timing Commander (PC), click the button (red circle) at the up-right corner of the GUI to set up the communication protocols (see Figure 7).

After I²C and one-byte addressing are selected, click OK to close the window.

Figure 8. Setting I²C for Connecting the Board with GUI



- Click on the chip symbol at the upper-right corner to initiate the connection. The connection is valid when a green band appears at the upper-right corner of the window, as shown below.

Figure 9. A Green Band appears when a Valid Connection is Made



- If ClockMatrix chip's firmware, or firmware loaded from EEPROM, has a different version from that in the Personality file, a firmware version mismatch warning message will appear. Click "Close" button to close the message window and a connection is made.

Figure 10. Firmware Version Mismatch Warning Message



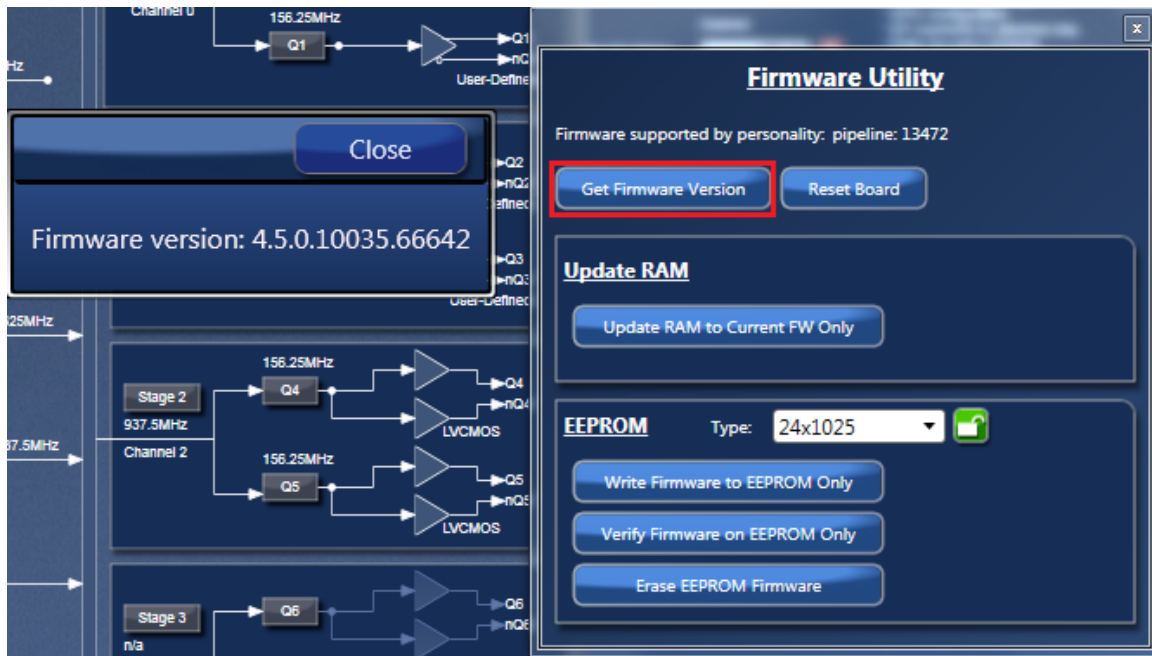
- Once the connection is made, the firmware version can be read within the GUI. Click the "Firmware Utility" button to bring up the Firmware Utility window, as shown below.

Figure 11. Reading Firmware Version



9. Within the Firmware Utility window, click the "Get Firmware Version" button to read the firmware version.


Figure 12. Read Firmware Version of ClockMatrix Chip



10. In the case where the firmware version mismatches each other, a firmware upgrade is necessary to update the chip's firmware. To do so, complete the steps in How to Upgrade the Firmware to update the chip's firmware.

2.3 Output Terminations and Rework to Take 1PPS Input

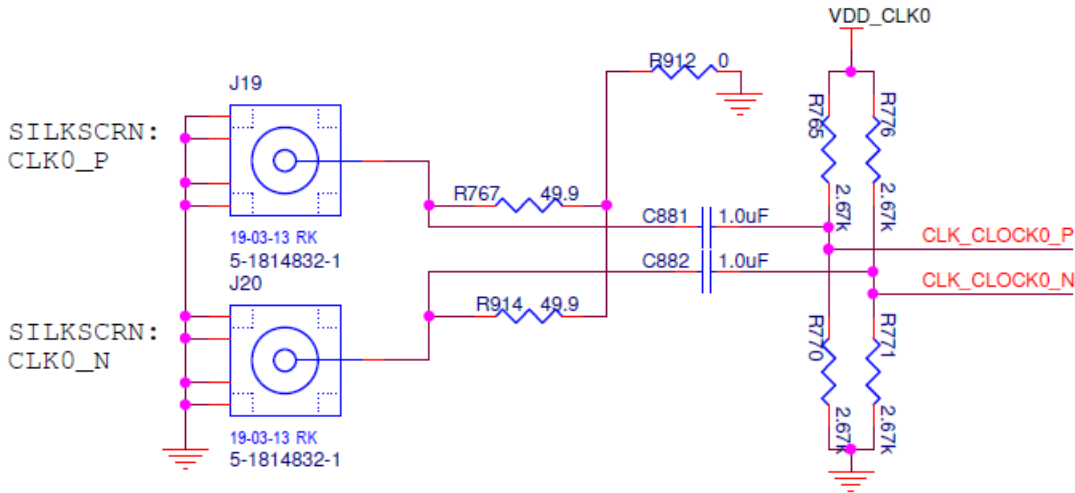
All outputs are terminated with a 100Ω resistor across the output pair. This is the recommended termination regardless of the Voffset and Vswing settings. Since the outputs are DC-coupled, they will support a 1PPS output without any need for rework.



Important Equipment Warning: When connecting the outputs to measurement equipment, use a DC-block to ensure that the output operates at its intended V_{offset} . Otherwise, the equipment may load the output down and cause degraded performance.

The following rework must be implemented in order to support a 1PPS input clock. All input clocks for this board are ac-coupled and terminated as in the following figure.

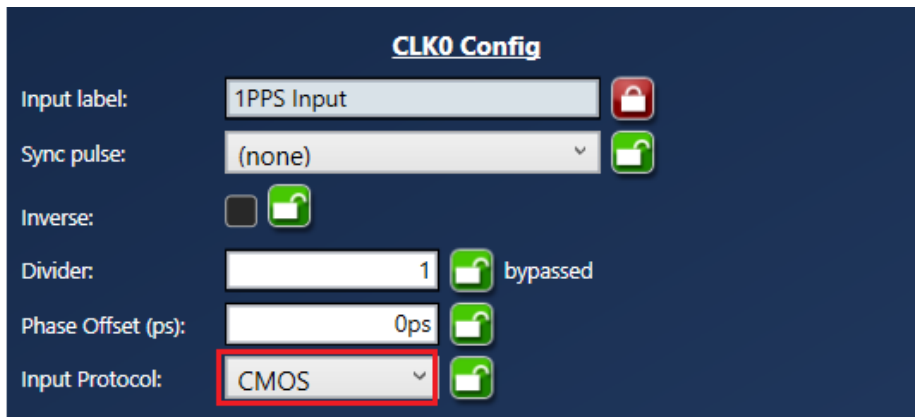
Figure 13. AC Coupling and Terminations for Input Clock



For a 1PPS input, a single-ended input with DC-coupling is recommended. As such, the populated AC-coupling capacitor must be removed and the input must be configured as LVCMOS, not differential.

1. In Figure 13, to make CLK0 supportive of 1PPS input, first configure CLK0 as LVCMOS in Timing Commander (see Figure 14).

Figure 14. Configuring CLK0 as CMOS to Receive a 1PPS Input

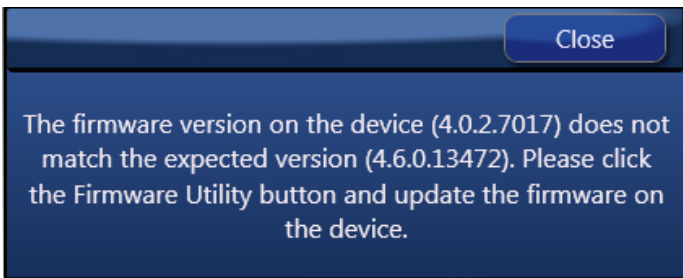


2. Once in LVCMOS mode, CLK0_P and CLK0_N will be two separate LVCMOS inputs instead of a differential pair. To make CLK0_P receive a 1PPS input, replace C881 with a 0Ω resistor; and at the same time, remove R765 and R770.

3. How to Upgrade the Firmware

3.1 Upload Firmware to the RAM

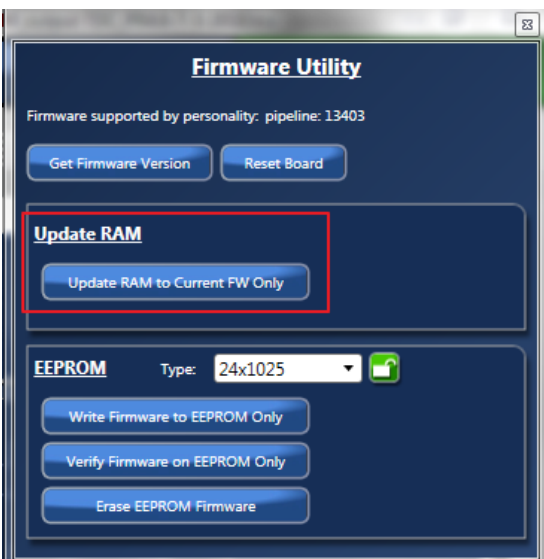
1. Connect to the EVK board.
2. Power up the board with no EEPROM present. This ensures the firmware is 4.0.2.7017, as displayed in the figure.
3. The GUI will indicate that the firmware on the chip does not match the GUI firmware. Press "Close".



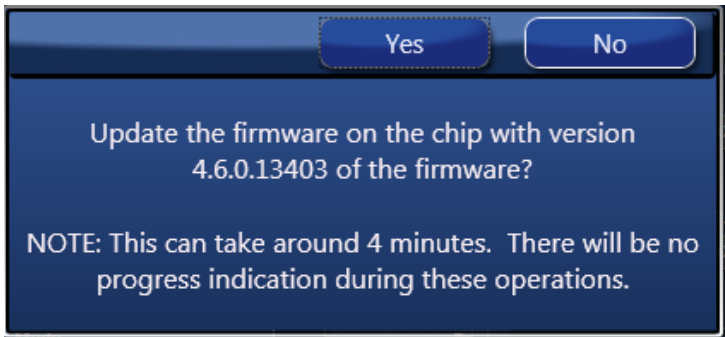
4. Open the "Firmware Utility" window by clicking on the button as follows.



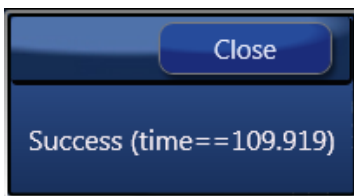
5. Update the Firmware first. Press "Update RAM to Current FW Only".



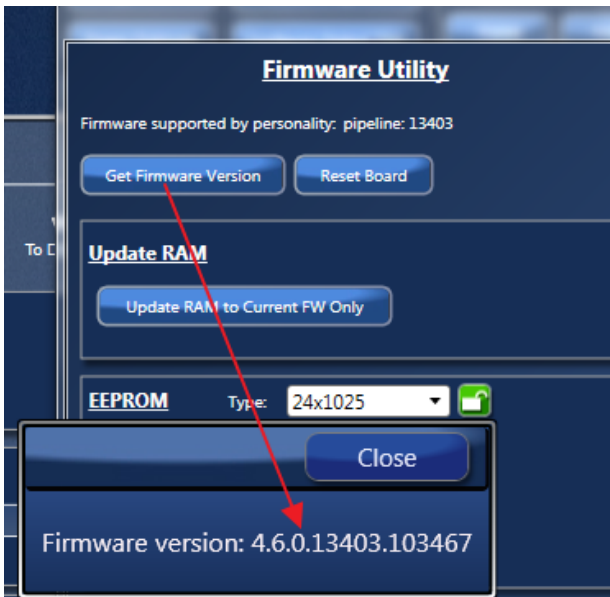
6. In the next window, press "Yes" and wait around 3-4 minutes.



7. Once the firmware is updated, the following window will indicate a successful update. Click "Close".

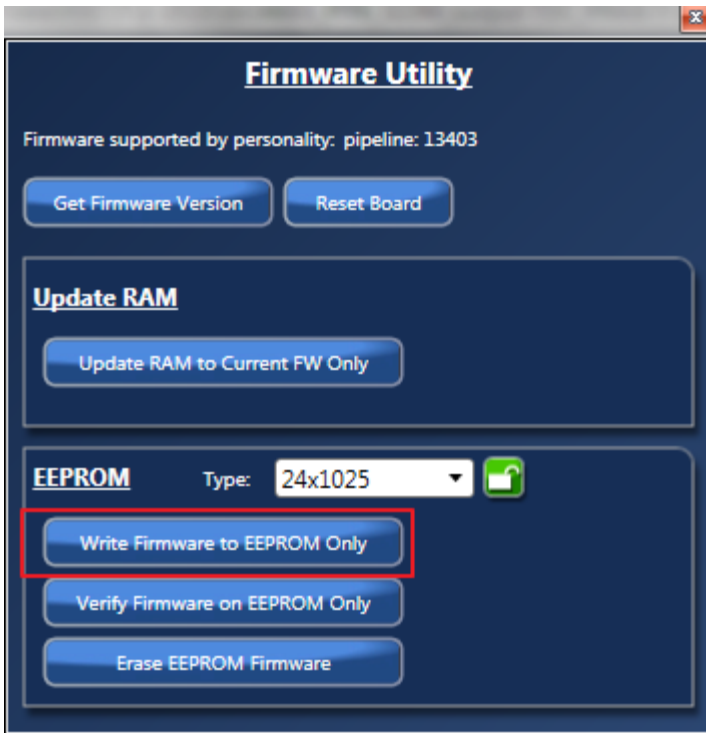


8. Press "Get Firmware Version" to verify that the RAM was updated correctly, then click "Close".

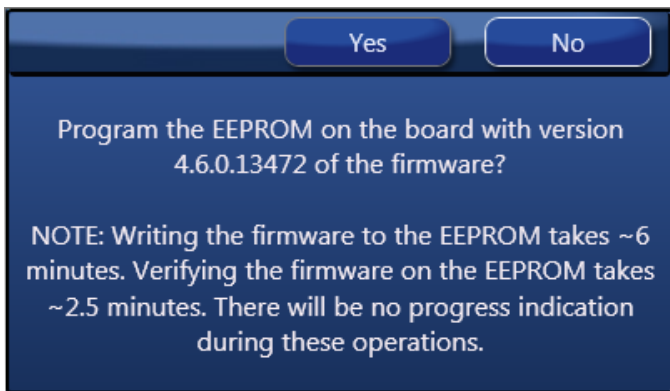


3.2 Upload Firmware into the EEPROM

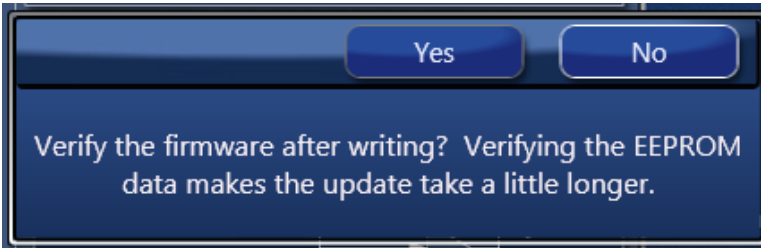
1. Once the firmware has been updated to the chip (steps 1 to 8), install the EEPROM on the EVK board.
2. Press "Write Firmware to EEPROM Only".



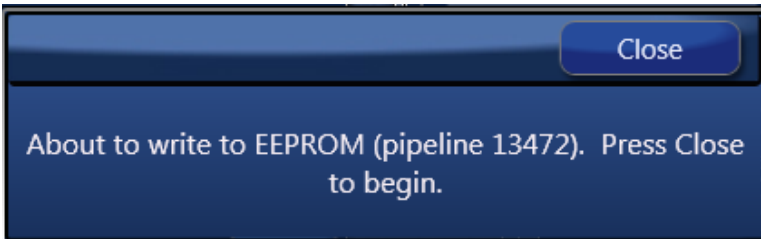
3. In the next window, press "Yes".



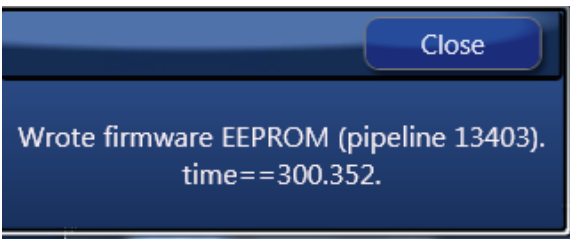
4. When asked to "Verify" the EEPROM, press "No".



5. In the next window, press "Close" to start the EEPROM write.



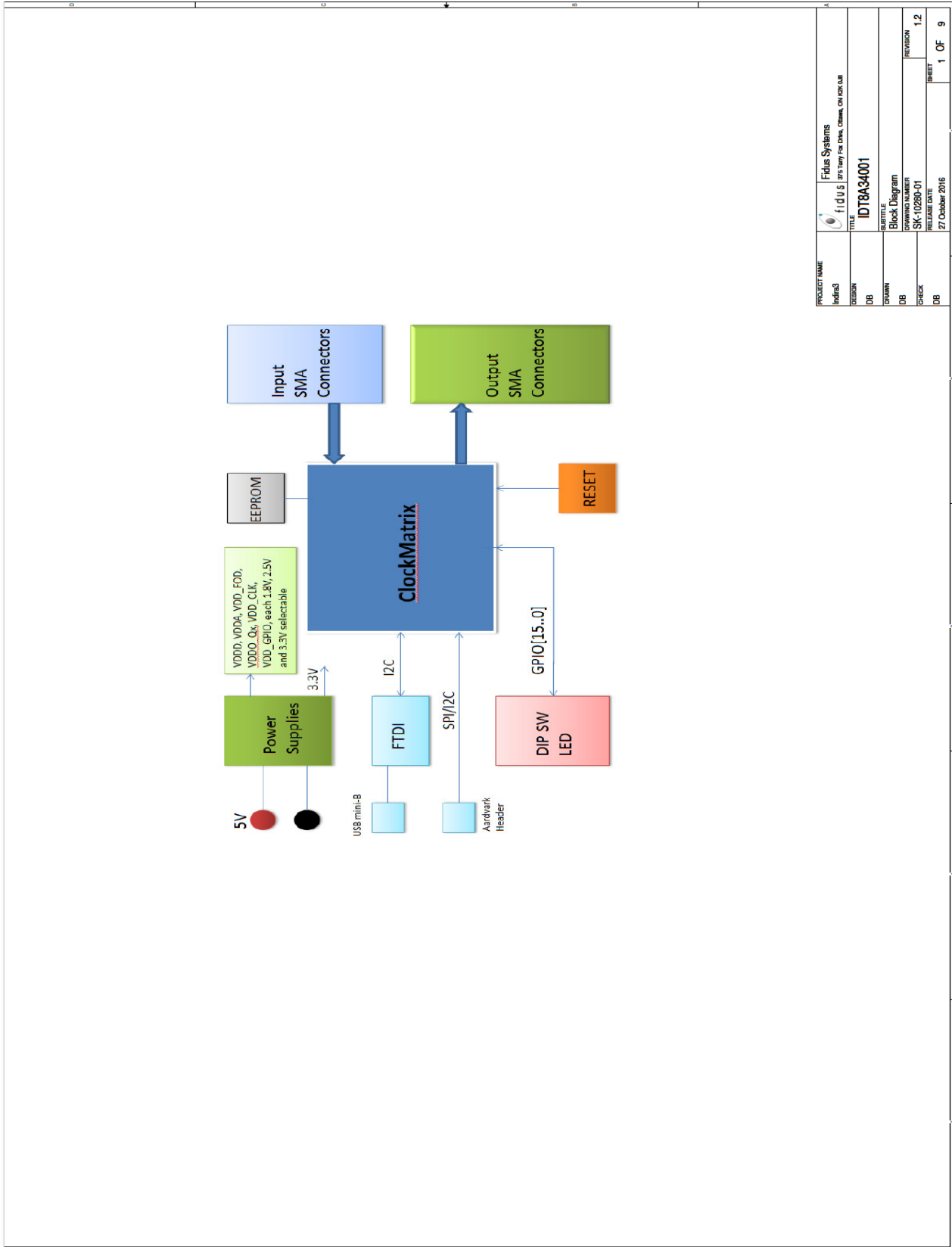
6. Wait about 5 minutes for the EEPROM write to complete. Click "Close" in the following window.

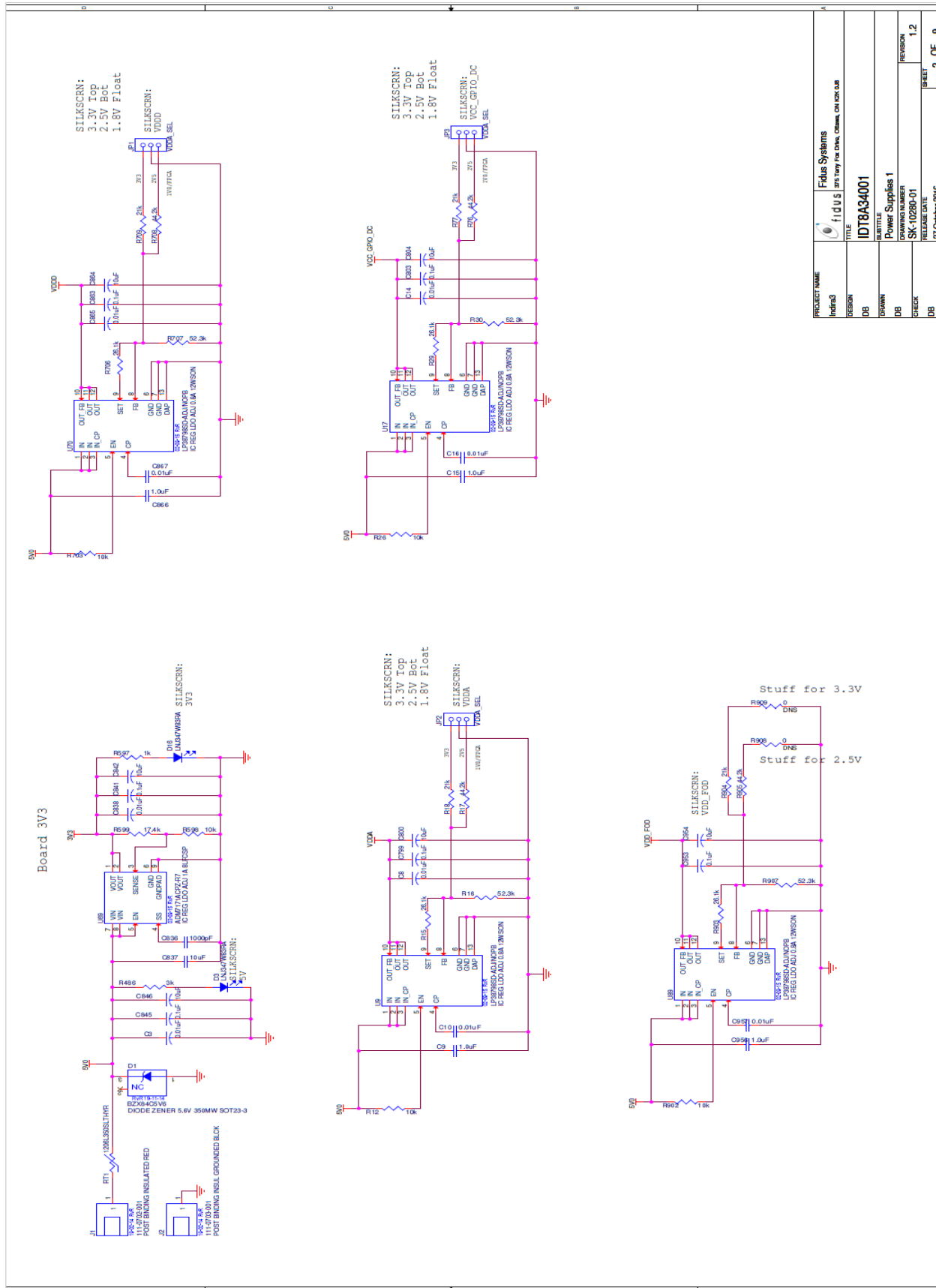


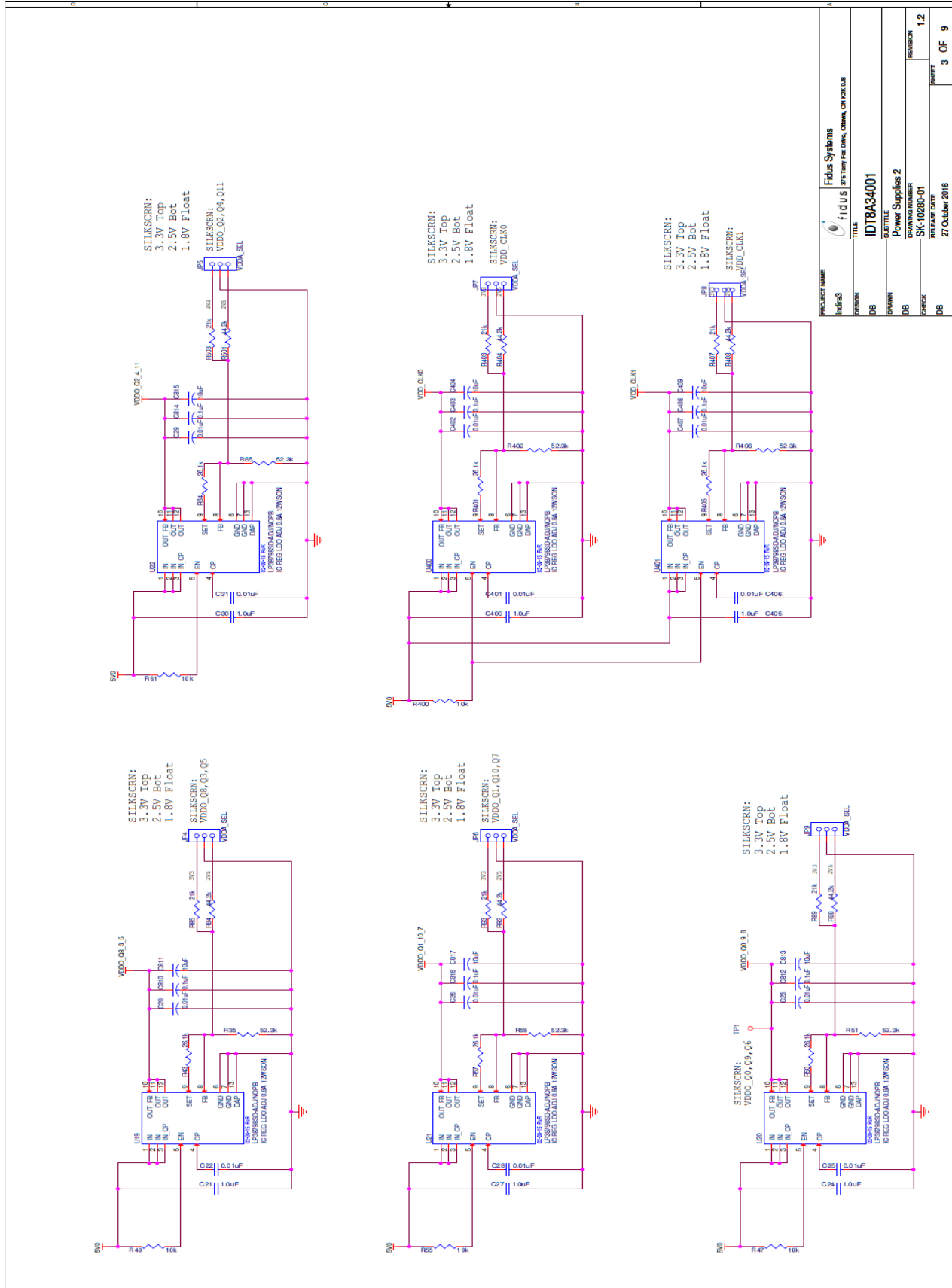
3.3 Verify the EEPROM Programming

7. Power cycle the board.
8. Disconnect and reconnect to the chip.
9. Read back the firmware version to ensure it is correct (see steps 3 to 7).

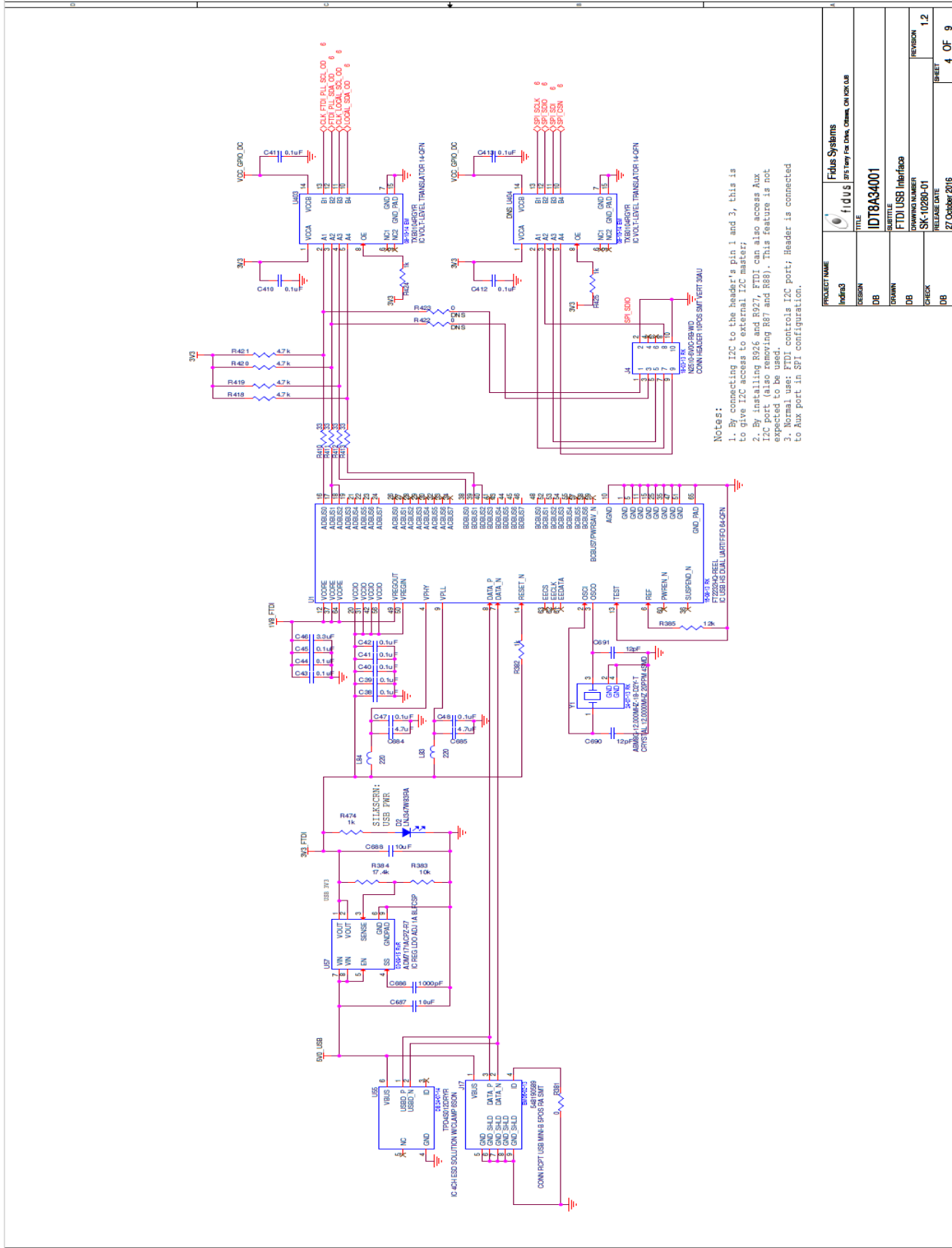
4. Schematics





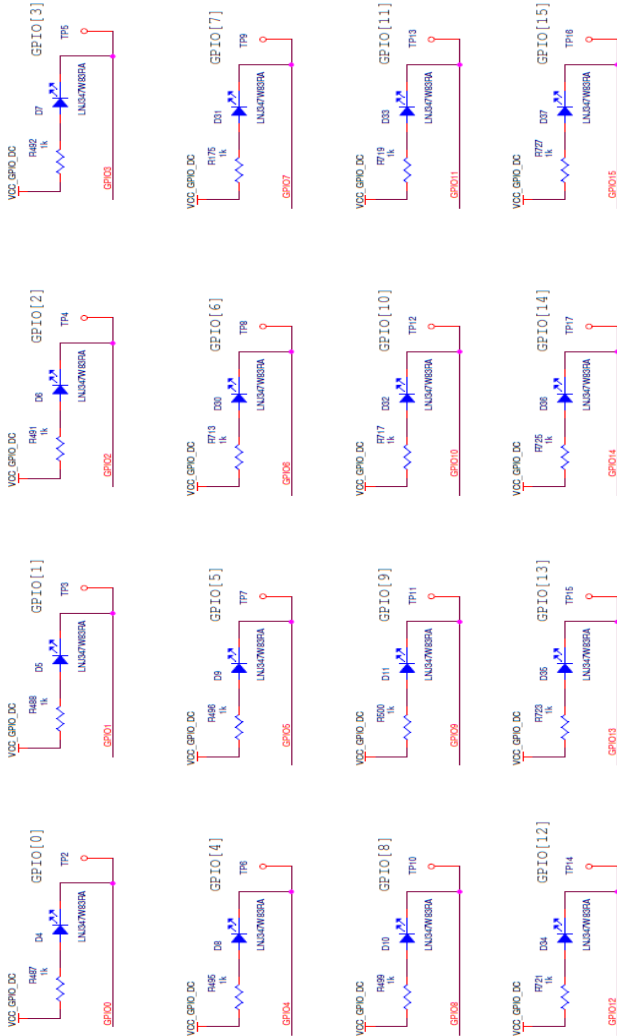


PROJECT NAME	fidus	Fidus Systems
DESIGN	IDT8A34001	875 Temp For Chm, ChmW, ON KICK-UB
DRAWN	Power Supplies 2	
CHECK	SK-10280-01	REVISION
DATE	27 October 2016	REVISION
		3 OF 9

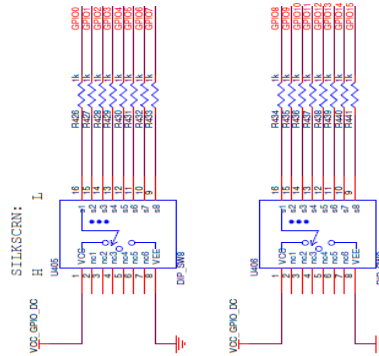


PROJECT NAME	Fidus Systems
INDIC3	fidus 185 Terry Fox Drive, Channah, ON K0C 1A0
DESIGN	IDT8A34001
DB	FTDI USB Interface
DESIGNER	SK-10280-01
DATE	27 October 2016
CHECK	DB
RELEASE DATE	27 October 2016
REVISION	1.2
DRW	4 OF 9

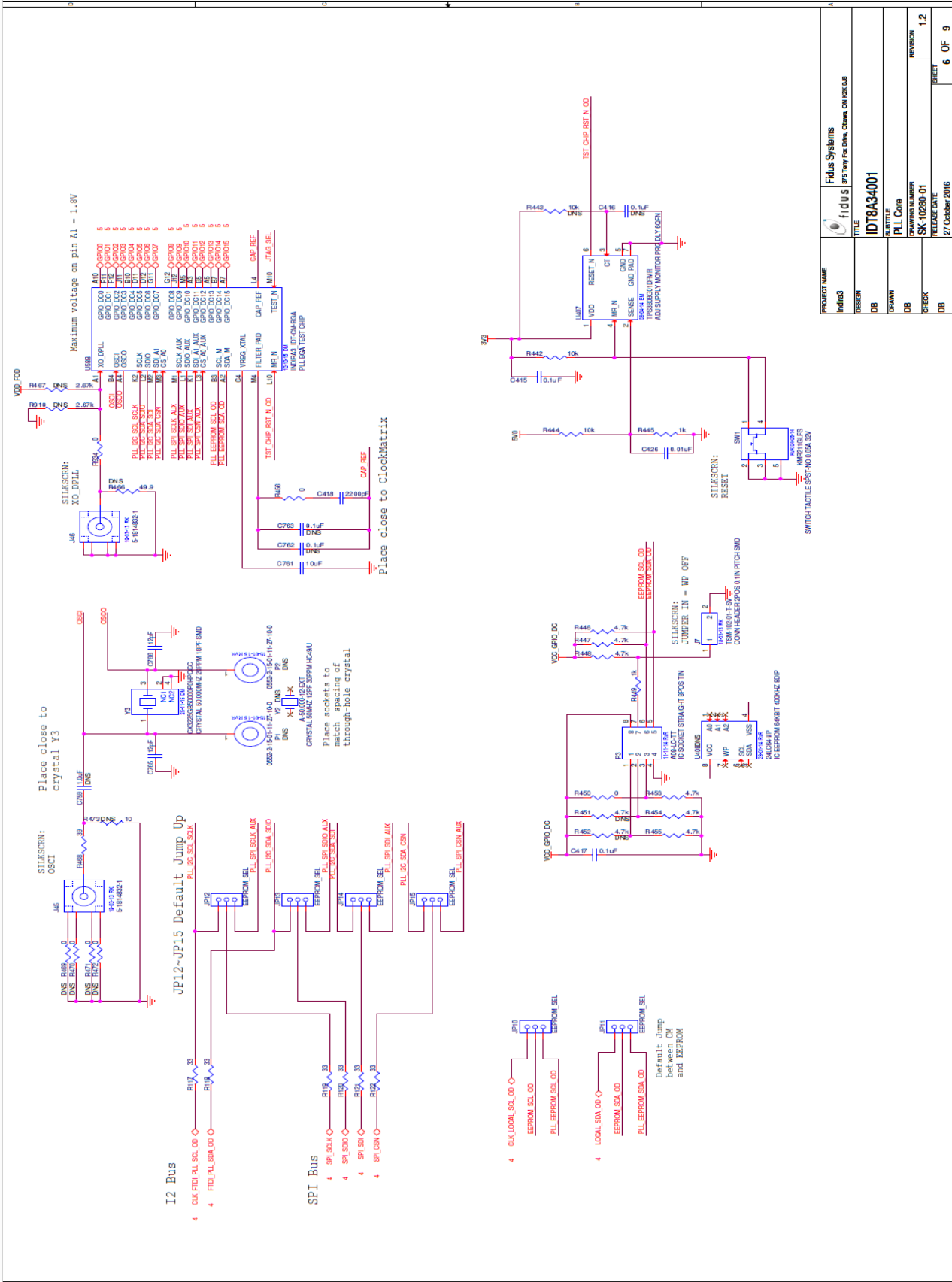
Note for Silkscreen:
Place GPIO[x] label close to each corresponding LED and Test point.



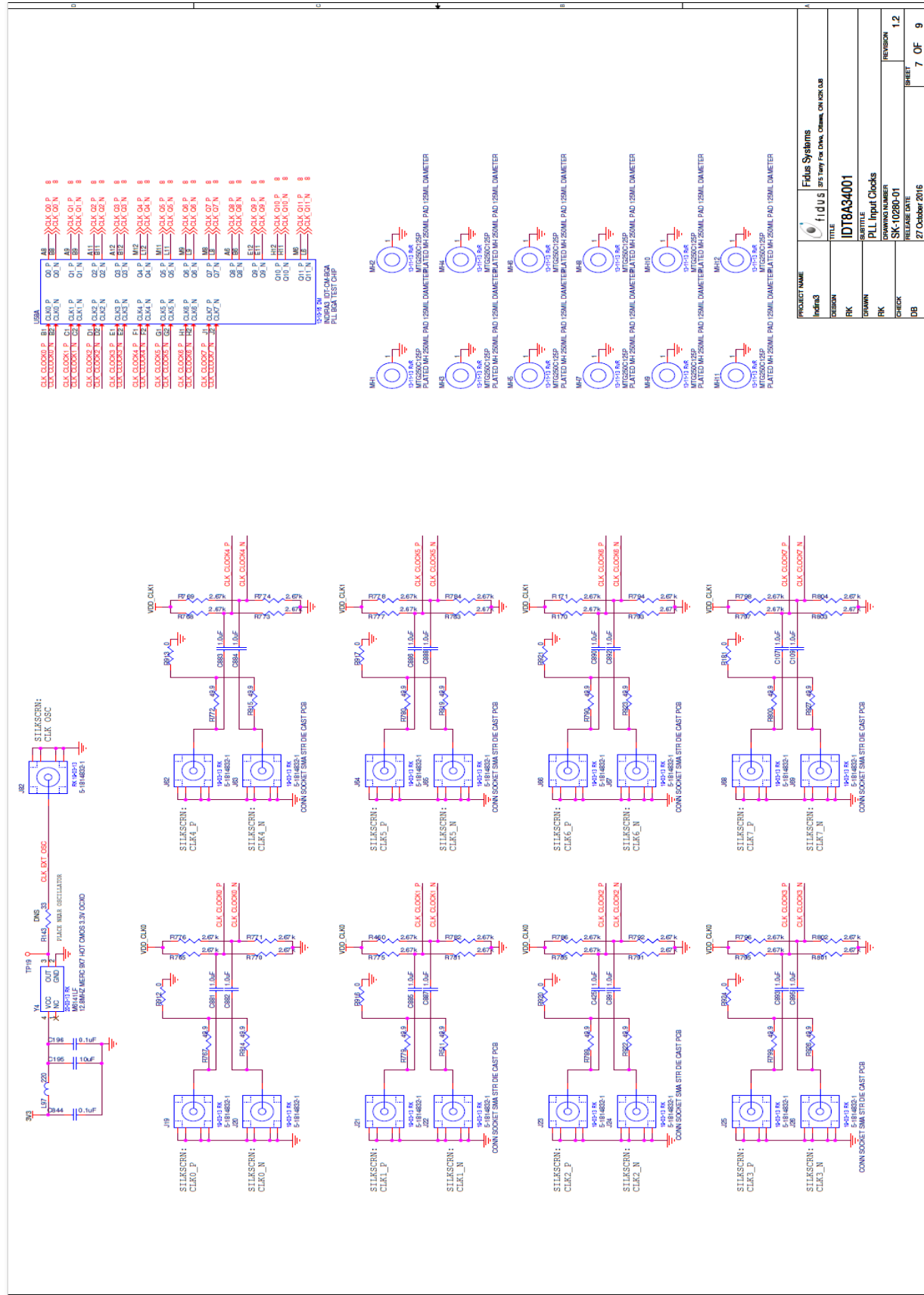
- 6 GPIO0
- 6 GPIO1
- 6 GPIO2
- 6 GPIO3
- 6 GPIO4
- 6 GPIO5
- 6 GPIO6
- 6 GPIO7
- 6 GPIO8
- 6 GPIO9
- 6 GPIO10
- 6 GPIO11
- 6 GPIO12
- 6 GPIO13
- 6 GPIO14
- 6 GPIO15



PROJECT NAME	fidius Fritius Systems
DESIGN	GPIO LEDs
RK	IDT8A34001
FRWNRN	GPIO LEDs
RK	SK-10280-01
CHECK	RELEASE DATE
DB	27 October 2016
	SHEET
	5 OF 9



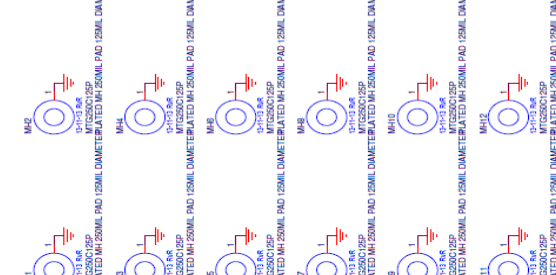
PROJECT NAME	fidus	File Systems
DESIGN	ID78A34001	PL Core
DRAWN	SK-10280-01	REVISION
CHECK	27 October 2016	1.2
DB		6 OF 9



U99A

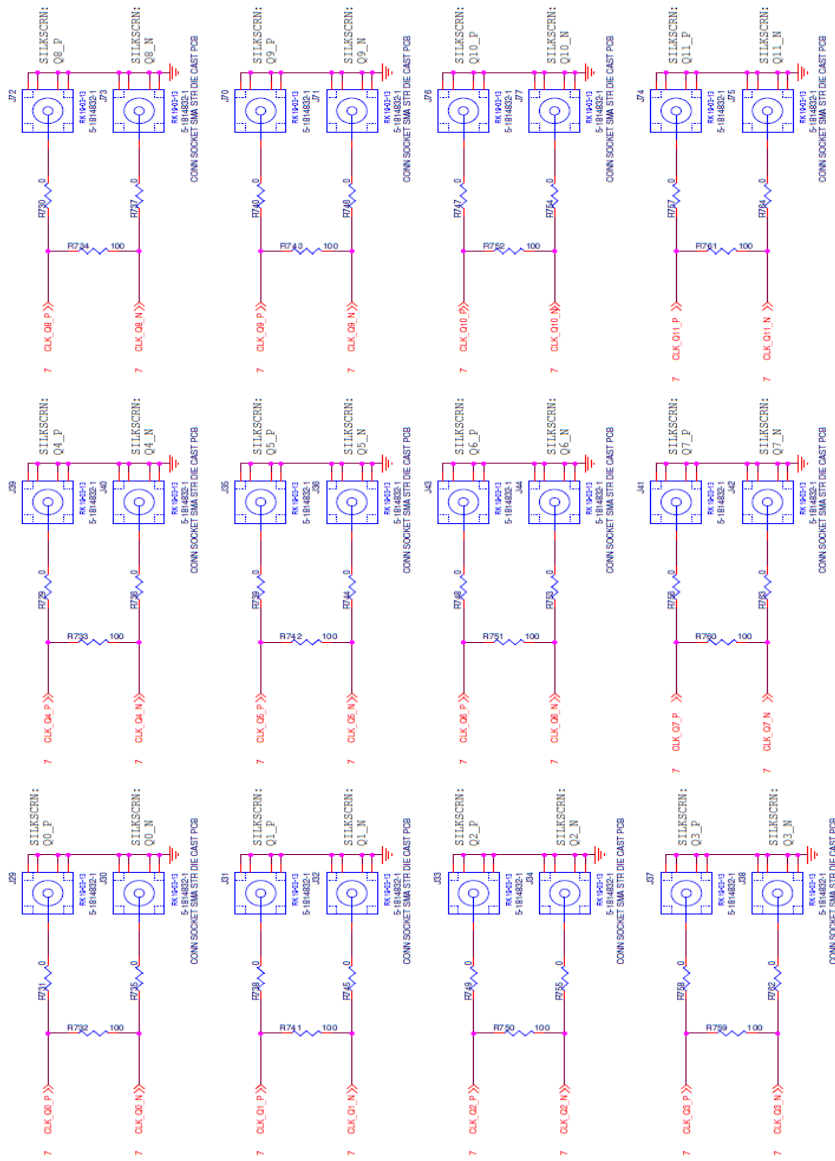
CLK_O0000_P	01_P	08	CLK_O0_P	8
CLK_O0000_N	01_N	08	CLK_O0_N	8
CLK_O0001_P	02_P	09	CLK_O1_P	9
CLK_O0001_N	02_N	09	CLK_O1_N	9
CLK_O0002_P	03_P	10	CLK_O2_P	10
CLK_O0002_N	03_N	10	CLK_O2_N	10
CLK_O0003_P	04_P	11	CLK_O3_P	11
CLK_O0003_N	04_N	11	CLK_O3_N	11
CLK_O0004_P	05_P	12	CLK_O4_P	12
CLK_O0004_N	05_N	12	CLK_O4_N	12
CLK_O0005_P	06_P	13	CLK_O5_P	13
CLK_O0005_N	06_N	13	CLK_O5_N	13
CLK_O0006_P	07_P	14	CLK_O6_P	14
CLK_O0006_N	07_N	14	CLK_O6_N	14
CLK_O0007_P	08_P	15	CLK_O7_P	15
CLK_O0007_N	08_N	15	CLK_O7_N	15
CLK_O0008_P	09_P	16	CLK_O8_P	16
CLK_O0008_N	09_N	16	CLK_O8_N	16
CLK_O0009_P	10_P	17	CLK_O9_P	17
CLK_O0009_N	10_N	17	CLK_O9_N	17
CLK_O0010_P	11_P	18	CLK_O10_P	18
CLK_O0010_N	11_N	18	CLK_O10_N	18
CLK_O0011_P	12_P	19	CLK_O11_P	19
CLK_O0011_N	12_N	19	CLK_O11_N	19

U100A-DT-0485A
PLL 624 TEST CHIP



PROJECT NAME	Fidus Systems
DESIGN	fidus 5FS Input Clocks
TITLE	PL Input Clocks
DATE	27 October 2016
DESIGNER	JK
DRAWN	JK
CHECK	JK
DB	JK
REVISION	1.2
SHEET	7 OF 9

PLACE PARALLEL TERMINATIONS CLOSE TO US



PROJECT NAME	Fidus Systems
DESIGN	515 Terry Fox Drive, Ottawa, ON K1H 1C8
REVISION	DB
TITLE	IDT8A34001
DRAWN	Benite
CHECK	PLL Output Clocks
RELEASE DATE	27 October 2016
REVISION	SK-10280-01
SHEET	8 OF 9

5. Ordering Information

Orderable Part Number	Description
8A34001-EVK	8A3xxxx 144BGA Evaluation Kit

6. Revision History

Revision Date	Description of Change
February 6, 2019	Initial release.

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