8V49NS0412 (Rev. C)

This document describes how to configure the 8V49NS0412 Rev. C evaluation board. The board can be configured through I2C, which offers complete control of the device features, or through tri-level pin selections, which offers the most popular configurations.

When the board is connected to a PC running Renesas Timing Commander software through USB, the device can be configured and programmed to generate frequencies with best-in-class performances.

Board Contents

The evaluation board ships with the following:

- 1 8V49NS0412 evaluation board
- 1 USB cable

Requirements

- Power supply with 3.3V and/or 5V output and 1000mA rating
- Two banana plug cables to connect the power supply to the board.
- Optional for I2C programming:
- PC requirements:
  - Renesas Timing Commander Software installed
  - Windows XP SP3 or later
  - Processor: minimum 1GHz
  - Memory: minimum 512MB; recommended 1GB
  - Available disk space: min. 600MB (1.5GB 64bit), recommended 1GB (2GB 64bit)
  - Network access during installation if the .NET framework is not currently installed on the system

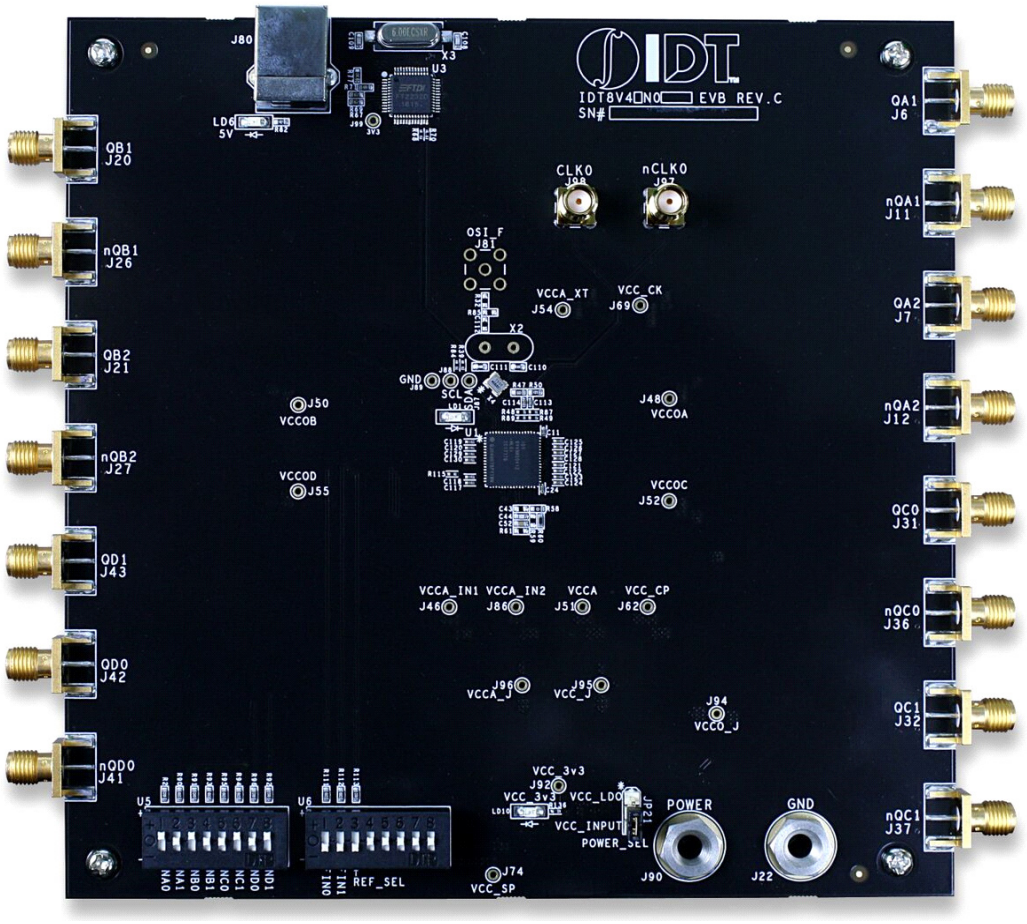

Figure 1. 8V49NS0412 Evaluation Board Diagram

Contents

1. Functional Description

1.1 Quick Start: Powering Up the Board

1. Configure the lab power supply to 3.3V with a 700mA limit. Turn off the output.
2. Set POWER_SEL (JP21) to select VCC_INPUT.
3. Remove all output terminations.
4. Set Dip Switch selectors to the positions shows in Figure 3.
5. Connect VEE to the GND jack (J22).
6. Connect the 3.3V source to POWER (J90).
7. Turn on the power supply. The current should measure ~503mA.

   Optional (for I2C programming through Timing Commander).
8. Connect a cable from a PC to the USB port.

When correct operation is verified, set the power supply limit for the number of outputs to be active.

The board ships with a 50MHz crystal and with the DIP Switch settings from Figure 3 it will be configured as follows:

- QA1 = QA2 = 156.25MHz, LVDS levels
- QB1 = QB2 = 156.25MHz, LVPECL levels
- QC0 = QC1 = 125MHz, LVDS levels
- QD0 = 125MHz, LVDS levels
- QD1 = High Impedance

When evaluating performance with the default hardware configuration, it is recommended that all active outputs be terminated 50Ω to GND by either terminator plugs or an instrument.

Bank A: This device supports four outputs for bank A, but only QA1 and QA2 have been routed. This bank's termination is configured for LVDS operation and will not switch if set to LVPECL levels unless the terminations are modified. For LVPECL operation, consult Output Configuration.

Bank B: This device supports four outputs for bank A, but only QB1 and QB2 have been routed. This bank's termination is configured for LVPECL operation. For LVDS operation, consult Output Configuration.

Bank C: This bank's termination is configured for LVDS operation and will not switch if set to LVPECL levels unless the terminations are modified. For LVPECL operation, consult Output Configuration.

Bank D: QD0 is terminated for LVDS operation and will not switch if set to LVPECL levels unless the terminations are modified. For LVPECL operation, consult Output Configuration.

1.2 Board Power Supply

This board offers the option to power the device from either a supply set to 5V and an LDO (U9), or the supply set to 3.3V and bypassing the LDO.

1.2.1 Bypass External LDO (Default Configuration)

Set JP21 jumper to VCC_INPUT. Provide 3.3V to the POWER jack (J90).

1.2.2 External LDO Configuration

Set JP21 jumper to VCC_LDO. Provide 5V to the POWER jack (J90).

1.3 Input Configuration

The inputs are configured with an AC-coupling termination scheme. This scheme allows flexibility for either differential or single-ended inputs. The default configuration is as follows:

Table 1. Default Input Configuration

Input	Default Termination
CLK0	50Ω to ground, AC-coupled into the device.

1.3.1 Differential Input

Connect the input signal to CLK0 and nCLK0.

1.3.2 Single-ended Input

Connect the input signal to CLK0 and float nCLK0.

1.4 Output Configuration

The differential outputs are AC-coupled, allowing for maximum flexibility for observation of the output whether configured for LVPECL or LVDS levels. The default termination scheme can be used to measure either of the two output level-types but is not optimal. The optimal termination circuits are tabulated below. To locate the components listed, see Figure 5.

Table 2. Termination Outputs for QA1

Signal Type	180Ω Pull-down: R124, R125	Series Capacitors: C125, C126	Resistor Network: R3, R4, R11, R12
LVPECL	Installed	0.1µF	Not Installed
LVDS (default)	Not Installed	0.1µF	Not Installed

Table 3. Termination Outputs for QA2

Signal Type	180Ω Pull-down: R126, R127	Series Capacitors: C127, C128	Resistor Network: R5, R6, R13, R14
LVPECL	Installed	0.1µF	Not Installed
LVDS (default)	Not Installed	0.1µF	Not Installed

Table 4. Termination Outputs for QB1

Signal Type	180Ω Pull-down: R118, R119	Series Capacitors: C119, C120	Resistor Network: R19, R20, R27, R28
LVPECL (default)	Installed	0.1µF	Not Installed
LVDS	Not Installed	0.1µF	Not Installed

Table 5. Termination Outputs for QB2

Signal Type	180Ω Pull-down: R128, R129	Series Capacitors: C129, C130	Resistor Network: R21, R20, R29, R30
LVPECL (default)	Installed	0.1µF	Not Installed
LVCMOS	Not Installed	33Ω	Not Installed
LVDS	Not Installed	0.1µF	Not Installed

Table 6. Termination Outputs for QD0

Signal Type	180Ω Pull-down: R116, R117	Series Capacitors: C118, C117	Resistor Network: R52, R53, R55, R56
LVPECL (default)	Installed	0.1µF	Not Installed
LVCMOS	Not Installed	33Ω	Not Installed
LVDS	Not Installed	0.1µF	Not Installed

As noted, the 4-resistor network is not installed in Table 2 to Table 7 because an oscilloscope with internal 50Ω termination is used for signal termination and measurement. If a DC-coupled, stand-alone LVPECL output is needed (without oscilloscope connections), the 4-resistor network must be installed accordingly. The following table provides the configuration for QA1.

Table 7. Resistor Network Termination for LVPECL for QA1

Signal Type	180Ω Pull-down: R39, R40	Series Capacitors: C123, C125	Resistor Network: R3, R4, R11, R12
LVPECL	Not Installed	0Ω	R3 = R4 = 125Ω R11 = R12 = 84Ω

1.5 DC Controls

The dip switches have three settings: 0V, Float, and VCC. For the location of the dip switches and their default configuration, see Figure 3, labels “E” and “F”.

1.6 Crystal Interface

By default, a 3.2 × 2.5 mm SMD 50MHz crystal is installed on the top side of the board. It provides the reference frequency for the device. This board supports other options for the XTAL_IN reference. If using one of the other options, the crystal on X4 must be removed.

1. **Through-hole crystal**. With this option, the device can be evaluated with different crystals without the need to solder each time the crystal is replaced:
   a. Remove the crystal from X4 on the top-side of the board (see Figure 3, “X4” for location of the component).
   b. Place a crystal into the crystal socket X2 (see Figure 2 for location of the component).

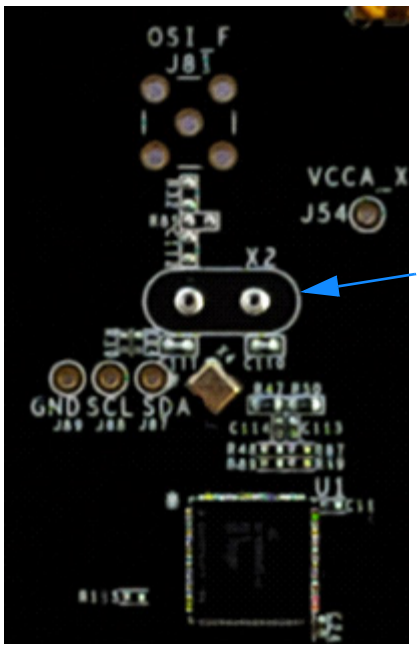

Figure 2. Crystal Interface PCB

2. **Crystal overdrive**. With this option, the device can be evaluated with different sources, such as frequency generators, XOs, or other devices. For identification of the components mentioned, see Figure 2 and Figure 6.
   a. Remove the crystal from X4 (see Figure 3, “X4” for location of the component).
   b. Populate SMA J81.
   c. Solder a 1µF capacitor onto C112.
      Note: The input must be AC-coupled.
   d. R85 can be populated with a 50Ω resistor for input sources requiring such termination.
   e. R32 must be populated. It can be a 0Ω resistor for input sources or 33Ω for CMOS inputs.

2. Board Design

Use Figure 3 and Table 8 to identify: power supply jacks, USB connector, input and output SMA connectors, DIP switches, and other board elements.

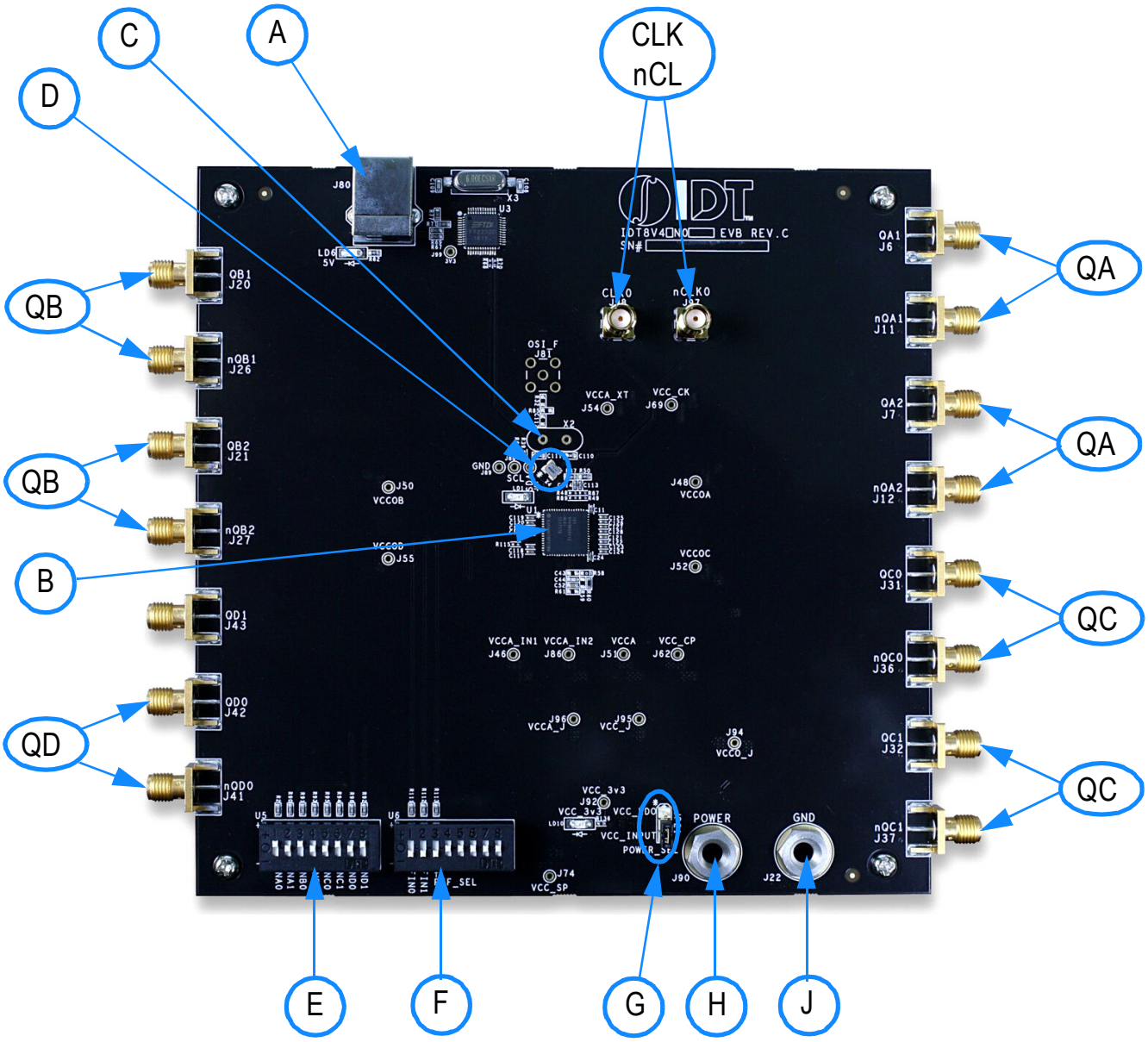

Figure 3. Evaluation Board Overview

Table 8. Evaluation Board Legend

Inputs	Description
CLK	Clock input line. Can be configured for differential or single-ended input.
nCLK	nClock input line.
Outputs	**Description**
QA1	Can be configured for either LVPECL or LVDS output levels.
QA2	Can be configured for either LVPECL or LVDS output levels.
QB1	Can be configured for either LVPECL or LVDS output levels.

Table 8. Evaluation Board Legend

Inputs	Description
QB2	Can be configured for either LVPECL or LVDS output levels.
QC0	Can be configured for either LVPECL or LVDS output levels.
QC1	Can be configured for either LVPECL or LVDS output levels.
QD0	Can be configured for either LVPECL or LVDS output levels.
QD1	Single-ended LVCMOS output.
Other	**Description**
A	USB connector.
B	8V49NS0412 – the device to be evaluated.
C	Through-hole HC-49 crystal socket (optional).
D	SMD 50MHz crystal.
E	Dip Switch for DC control signals (NAx, NBx, NCx, NDx).
F	Dip Switch for DC control signals (FINx, REF_SEL).
G	Power select (default is 3.3V input).
H	Power jack.
J	Ground jack.

2.1 Schematic Diagrams

The following figures are schematics that are applicable to specific sections of this document. The complete schematics are available in a separate document.

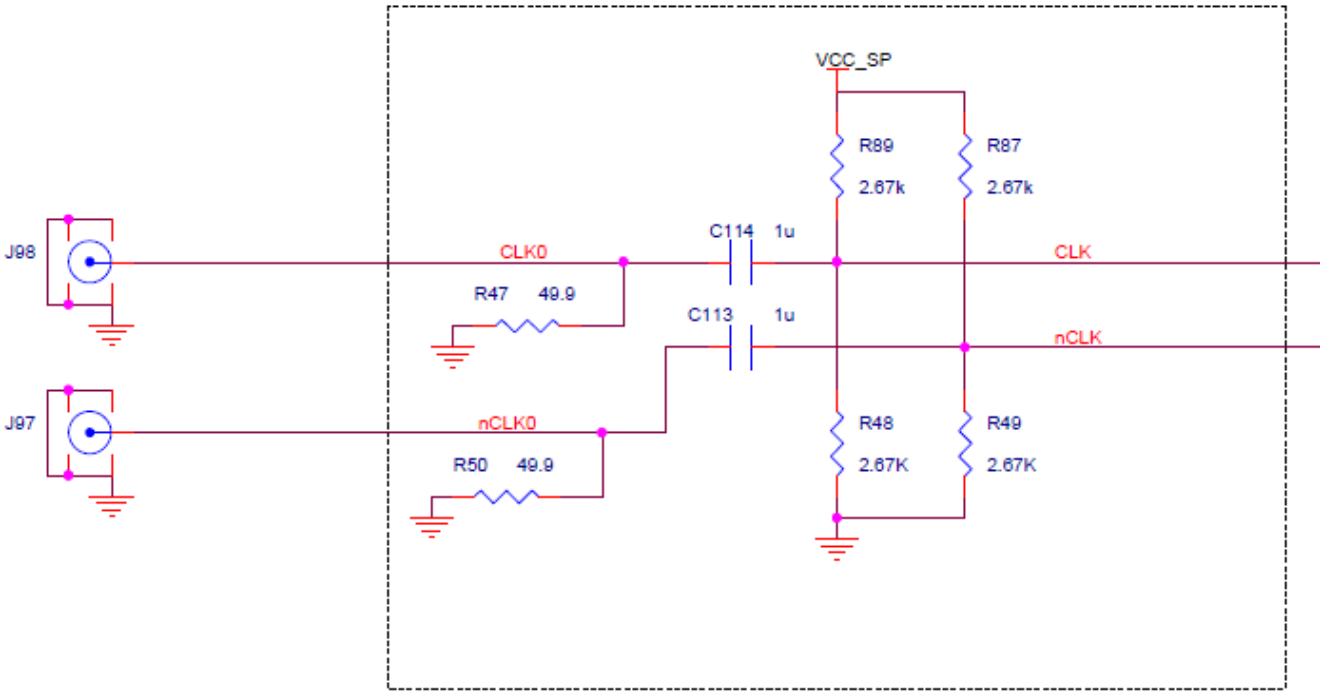

Figure 4. Input CLK Schematic

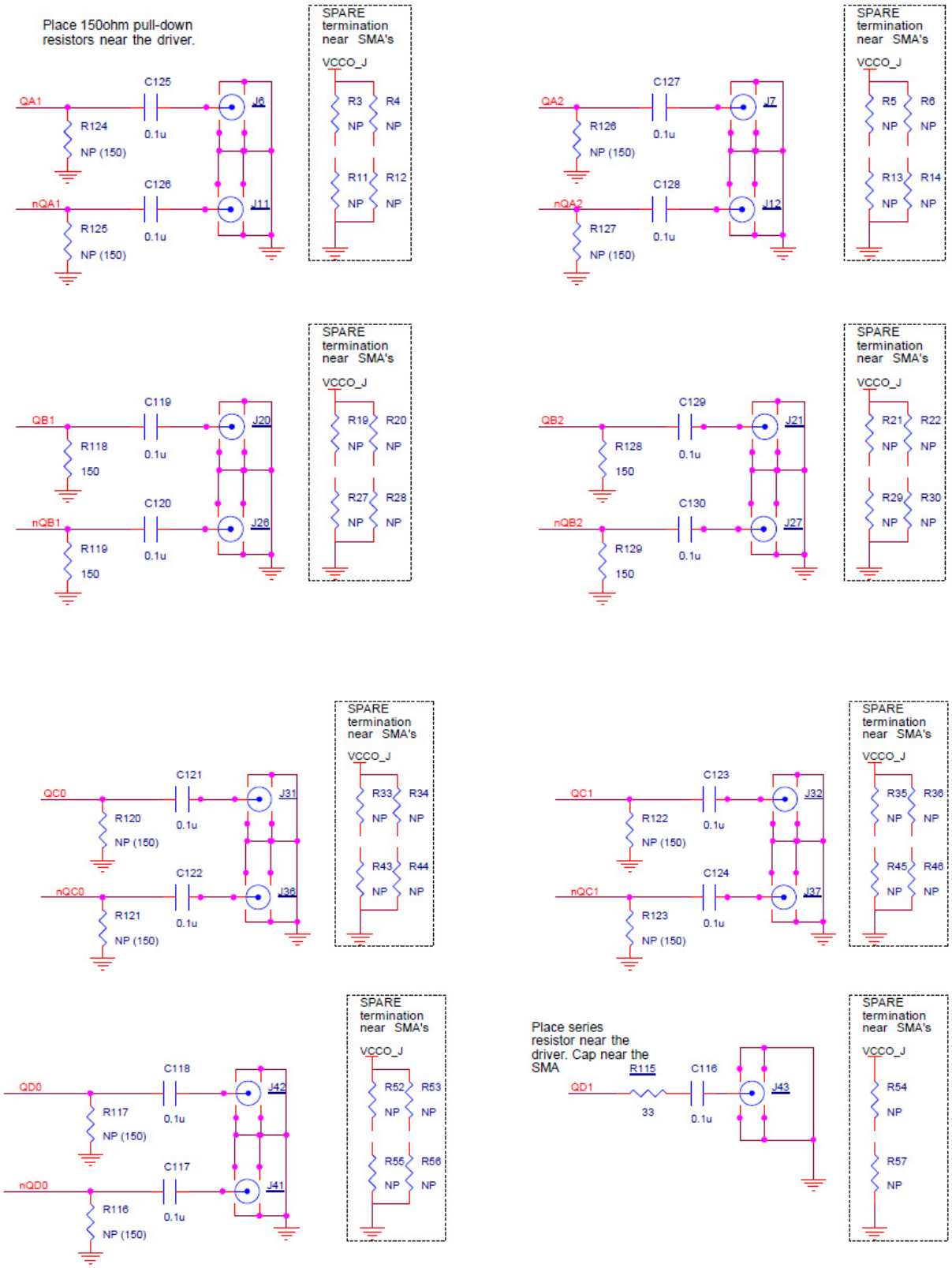

Figure 5. Output Termination Schematics

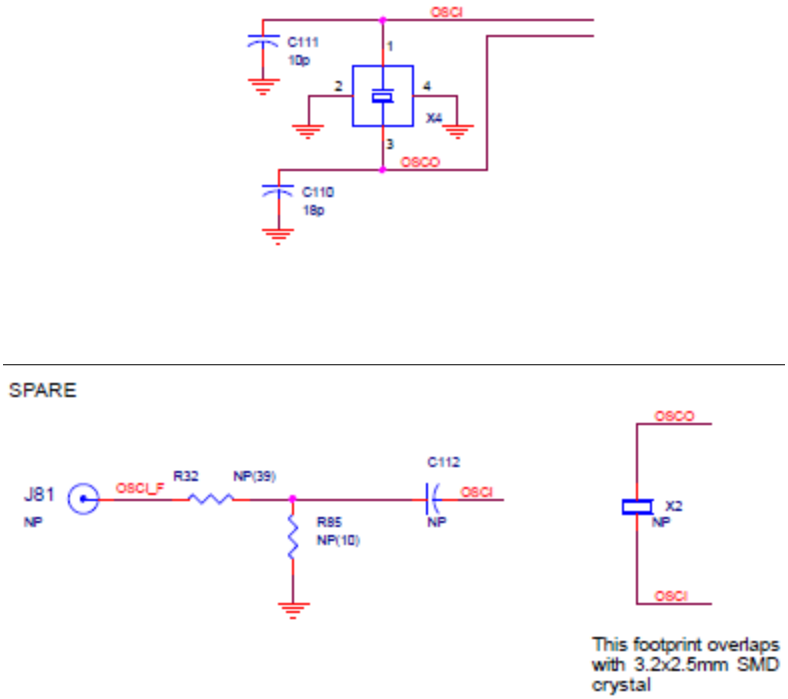

Figure 6. Crystal Interface Schematic

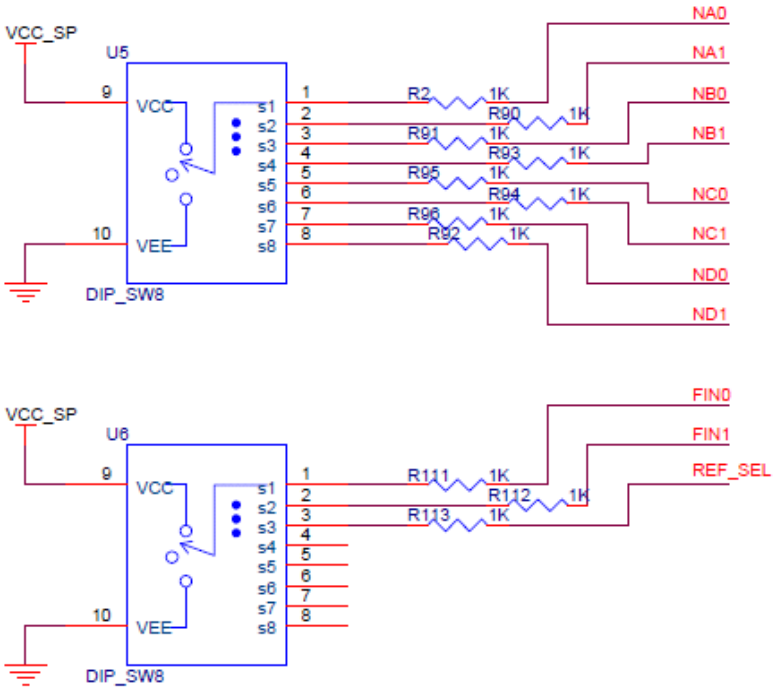

Figure 7. DC Control Schematic

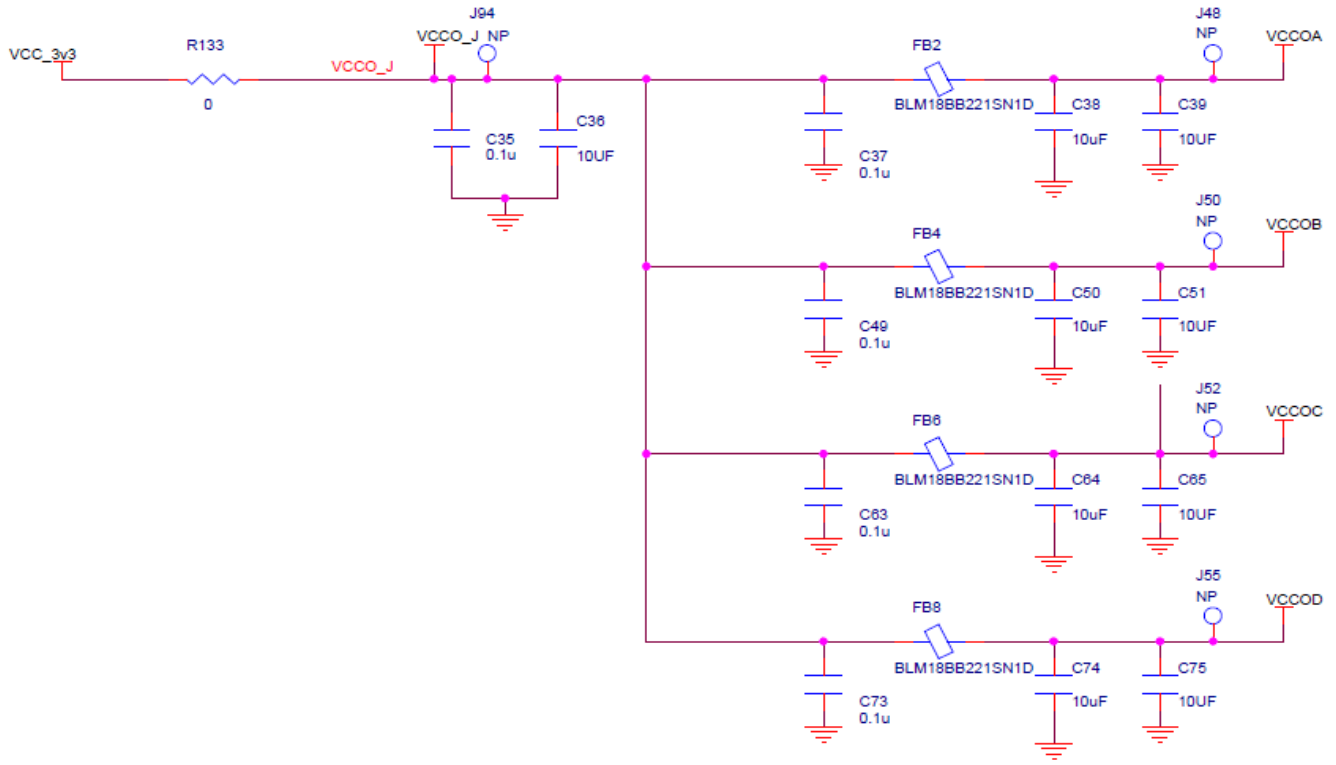

Figure 8. VCCO Power Filtering

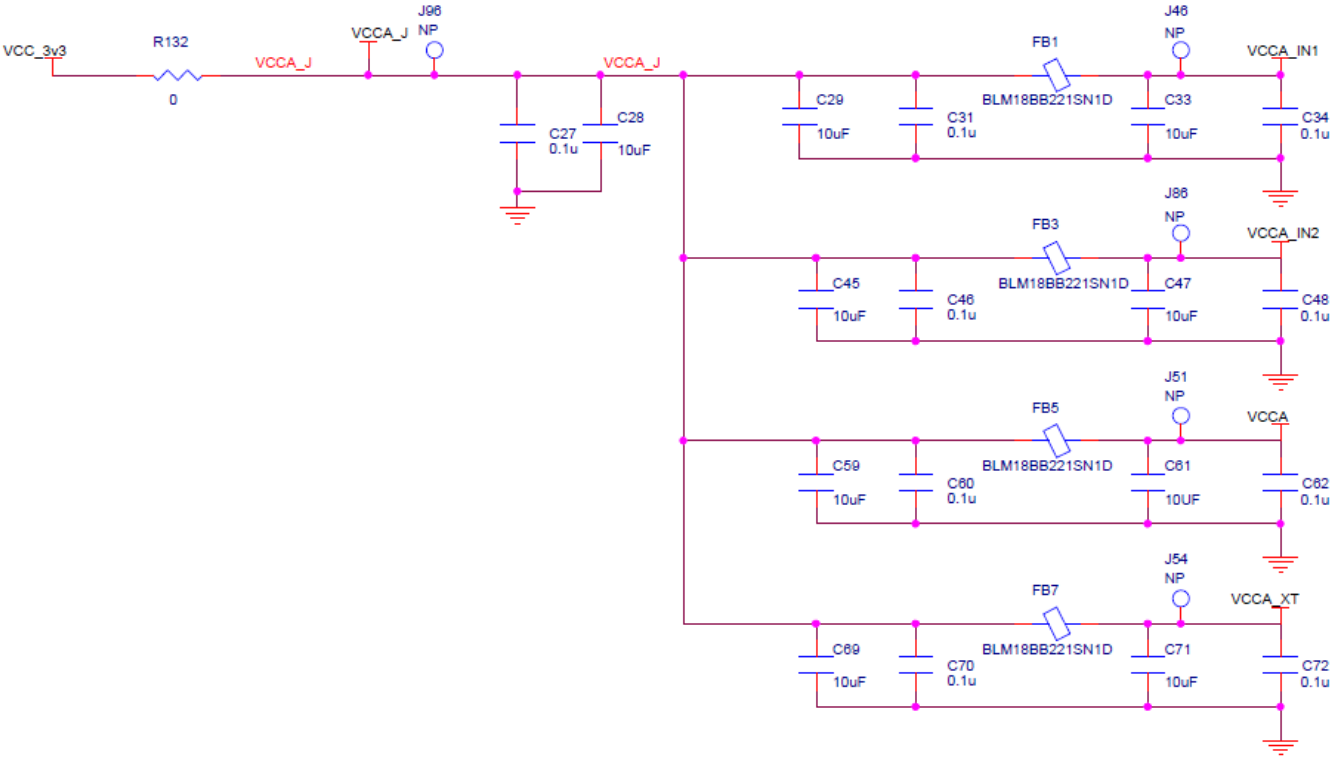

Figure 9. VCC Filtering

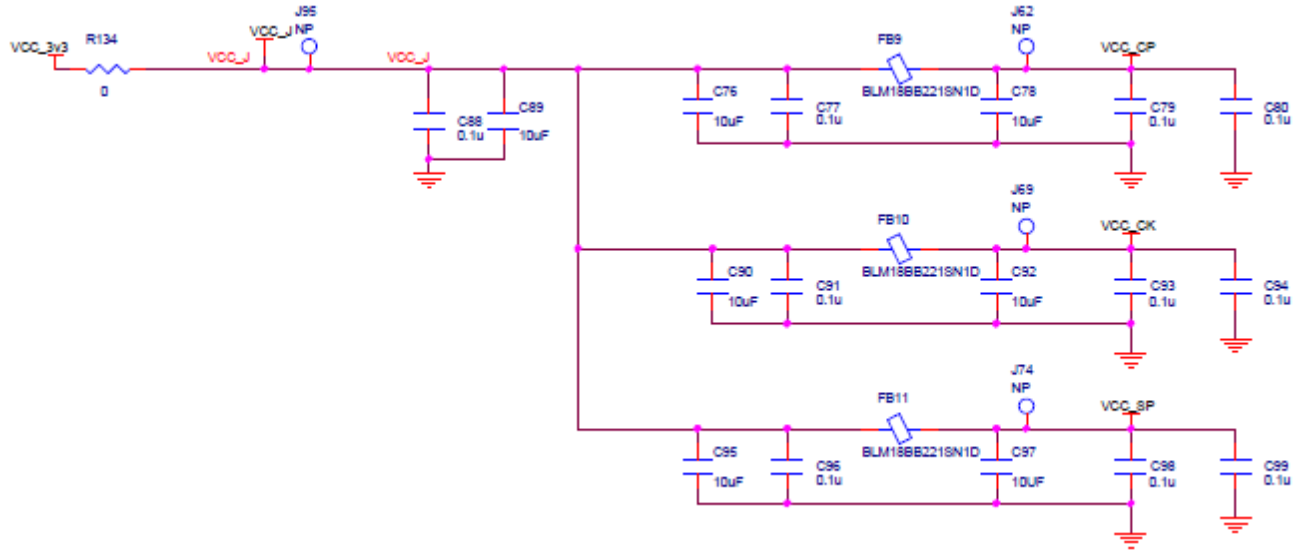

Figure 10. Digital and Core Power Filter

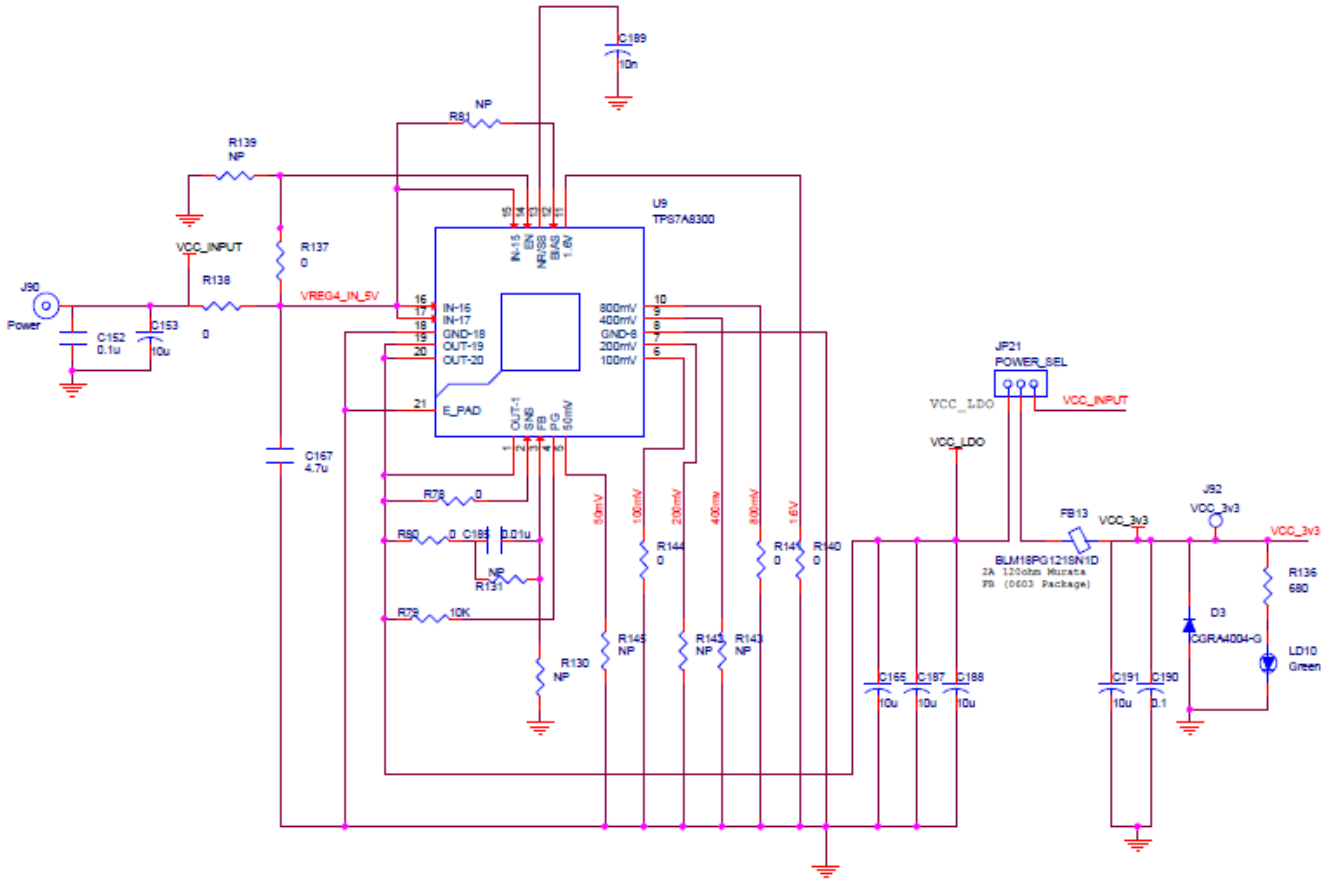

Figure 11. LDO and Power Scheme

2.2 Bill of Materials

Table 9. Bill of Materials

Item	Qty	Reference	Part	Footprint	Preferred Manufacturer	Preferred Part Number
1	3	C5,C42,C55	4.7u	402	Samsung	CL05A475MQ5NRNC
2	38	C7,C9,C11,C13,C15,C17,C19,C22,C24,C27,C31,C34,C35,C37,C41,C46,C48,C49,C54,C58,C60,C62,C63,C68,C70,C72,C73,C77,C79,C80,C88,C91,C93,C94,C96,C98,C99,C152	0.1u	402	TDK	C1005X7R1C104K
3	25	C28,C29,C33,C36,C38,C39,C45,C47,C50,C51,C59,C61,C64,C65,C69,C71,C74,C75,C76,C78,C89,C90,C92,C95,C97	10UF	402	TDK	C1005X5R0G106M050BB
4	1	C44	200p	603	Murata	GRM1885C1H201JA01D
5	5	C52,C102,C106,C107,C190	0.1u	603	Murata	GRM188R71H104KA93D
6	3	C56,C113,C114	1.0u	402	TDK	C1005X5R1C105K
7	1	C103	0.047uF	402	TDK	C1005X7R1C473K050BC
8	1	C104	10uF	805	Taiyo Yuden	EMK212BJ106KG-T
9	1	C105	10000PF	603	Murata	GRM188R71H103KA01D
10	2	C108,C109	33PF	603	Murata	GRM1885C2A330JA01D
11	1	C110	10p	0402-0603	Murata	GRM1555C1H100FA01D
12	1	C111	6.8p	0402-0603	Murata	GRM1555C1H6R8BA01D
13	1	C115	22u	603	Samsung	CL10A226MQ8NRNC
14	5	C153,C165,C187,C188,C191	10u	603	TDK	C1608X5R1A106M
15	1	C167	4.7u	603	Samsung	CL10A475KP8NNNC
16	1	C185	0.01u	402	Taiyo Yuden	EMK105B7103KV-F
17	1	C189	10n	603	Murata	GRM188R71H103KA01D
18	1	D3	CGRA4004-G	DIODE_DO_214AC	Comchip	CGRA4004-G
19	11	FB1,FB2,FB3,FB4,FB5,FB6,FB7,FB8,FB9,FB10,FB11	BLM18BB221SN1D	603	Murata	BLM18BB221SN1D
20	1	FB13	BLM18PG121SN1D	603	Murata	BLM18PG121SN1D
21	1	JP21	POWER_SEL	HDR_THVT_1x3_100	Samtec	HTSW-103-07-G-S
22	15	J6,J7,J11,J12,J20,J21,J26,J27,J31,J32,J36,J37,J41,J42,J43	SMA_STRAIGHT_pin	SMA_SMEL_373x312	LightHorse	LTI-SASF975ZGT
23	1	J22,J90	GND, Power	JACK_THVT_BANANA_260DIA	Cinch	108-0740-001
24	1	J80	USB PORT	CON_THRT_USB_B_F	Mill-Max	897-43-004-90-000000
25	2	J97,J98	SMA_STRAIGHT_pin	SMA_THVT_LTI-SASF54GT	LightHorse	LTI-SASF54G
26	1	LD1	LED_0603_1206_H	LED_1206	Visual CC	CMD15-21VRC/TR8
27	2	LD6,LD10	Green	LED_1206	Visual CC	CMD15-21VGC/TR8

Table 9. Bill of Materials

Item	Qty	Reference	Part	Footprint	Preferred Manufacturer	Preferred Part Number
28	1	L1	600 ohm 500mA	603	TDK	MMZ1608Y601B
29	11	R2,R90,R91,R92,R93,R94,R95,R96,R111,R112,R113	1K	603	Yageo	RC0603FR-071KL
30	1	R23	475	0603ss	Yageo	RC0603FR-07475RL
31	14	R39,R68,R70,R78,R80,R84,R132,R133,R134,R137,R138,R140,R141,R144	0	402	Yageo	RC0402JR-070RL
32	2	R41,R42	4.7K	603	Yageo	RC0603FR-074K7L
33	2	R47,R50	49.9	603	Yageo	RC0603FR-0749R9L
34	4	R48,R49,R87,R89	2.67k	402	Yageo	RC0402FR-072K67L
35	1	R51	2.8K	603	Yageo	RC0603FR-072K8L
36	1	R58	0	603	Yageo	RC0603JR-070RL
37	1	R60	150	603	Yageo	RC0603JR-07150RL
38	1	R64	470	603	Yageo	RC0603FR-07470RL
39	2	R67,R69	27	603	Yageo	RC0603FR-0727RL
40	1	R71	1.5K	603	Yageo	RC0603FR-071K5L
41	3	R72,R77,R83	10K	603	Yageo	RC0603FR-0710KL
42	1	R79	10K	402	Panasonic	ERJ-2RKF1002X
43	1	R82	680	603	Yageo	RC0603JR-07680RL
44	1	R114	1	402	Samsung	RC1005F1R0CS
45	1	R115	33	402	Panasonic	ERJ-2RKF33R0X
46	4	R118,R119,R128,R129	No Populate			
47	1	R136	680	402	Panasonic	ERJ-2RKF6800X
48	1	U1	8V49NS0312	QFN_64_9x9mm	IDT (Renesas)	8V49NS0312
49	1	U3	ft2232_chip	QFP_48_7x7mm_p0_5	FTDI	FT2232D
50	2	U5,U6	DIP_SW8	SW_THVT_TDS08	APEM	TDS08
51	1	U9	TPS7A8300	RGR_PVQFN_20	Texas Instruments	TPS7A8300RGRT
52	1	X3	6MHz	XTAL_2_SM_4p8x11p4mm	ECS	ECS-60-32-5P-TR
53	1	X4	50MHz	XTAL_4_SM_3p2x2p5mm	TXC	7M-50.000MAAE-T
54	15	C116,C117,C118,C119,C120,C121,C122,C123,C124,C125,C126,C127,C128,C129,C130	33ohm	402	Yageo	RC0402JR-0733RL

3. Typical Performance Graphs

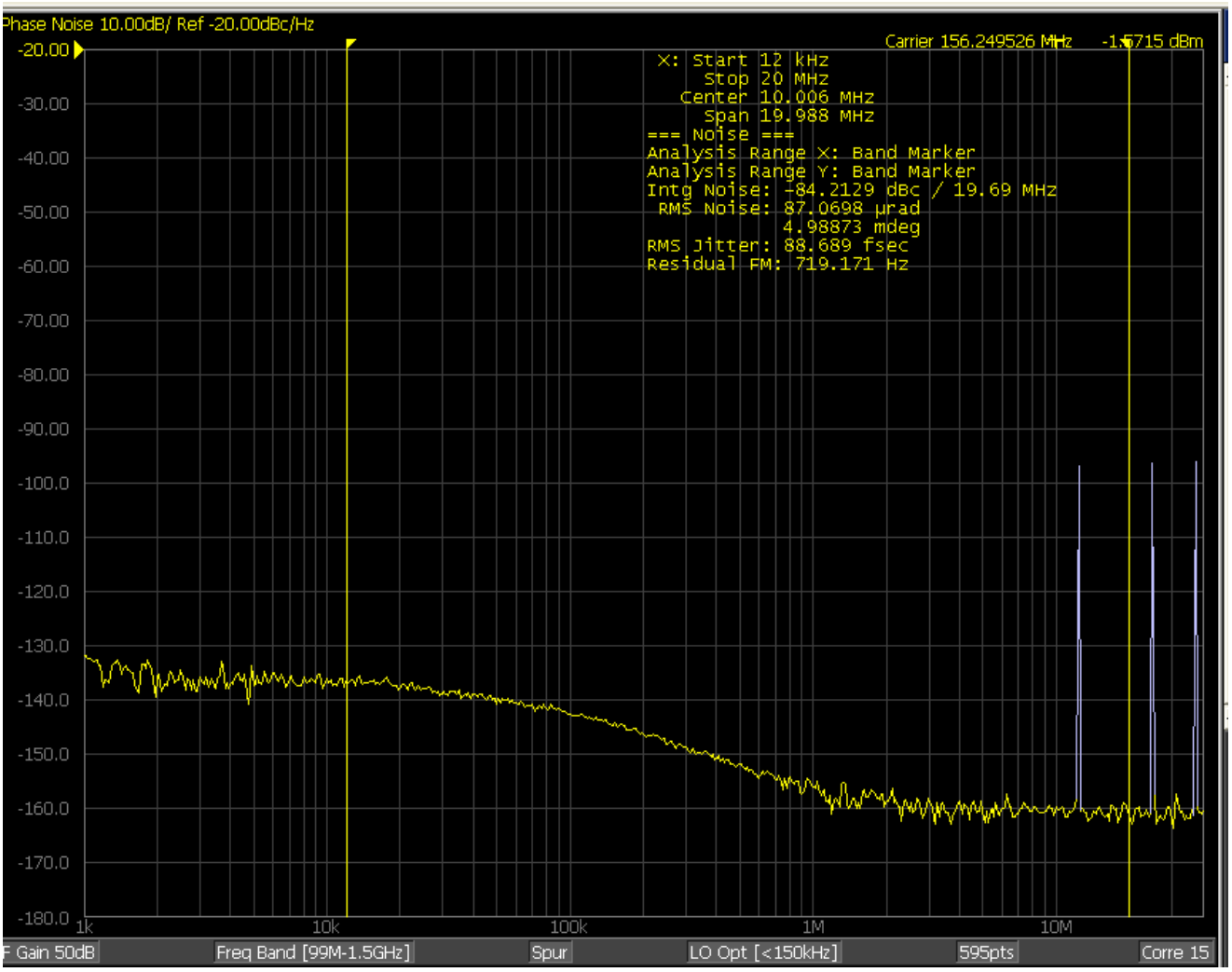

Figure 12. Default Configuration, Phase Noise on QA1

4. Ordering Information

Part Number	Description
EVK-8V49NS0412	8V49NS0412 (Rev. C) Evaluation Board

5. Revision History

Revision	Date	Description
1.00	Aug 23, 2021	▪ Rebranded as Renesas ▪ Completed other minor changes
-	Oct 24, 2018	Initial release.

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01 Jan 2024)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.