8V79S680/8V79S683/RC18016

The 8V79S680 Evaluation Board (EVB) is designed to evaluate the JESD Buffers 8V79S680, 8V79S683 and RC18016. This document describes the following:

- Basic hardware and GUI setup using Renesas IC Toolbox (RICBox™) software
- Board power-up instructions
- Instructions to get active output signals using a provided configuration file

A simplified block diagram for an 8V79S68x device is shown in Figure 1.

Board Contents

- 8V79S680/8V79S683/RC18016 evaluation board
- EVB manual
- Configuration software (installable plugin for RICBox)
- Configuration example file for device settings
- Board schematic and BOM

Features

- Distribution, fanout, phase-delay of clock and SYSREF signals
- Four output channels with a total of 16 differential outputs
- CLK/nCLK and REF/nREF inputs can use laboratory signal generator or driven by an RF-PLL Clock and Sysref generator (for example, 8V19N49x-xx Evaluation Board)
- Laboratory power supply connectors
- USB-C power supply
- Serial port for register configuration and register read back

Computer Requirements

- USB 2.0 or USB 3.0 interface
- Processor: minimum 1GHz
- Memory: minimum 512MB; recommended 1GB
- Available disk space: minimum 600MB (1.5GB 64-bit); recommended 1GB (2GB 64-bit)

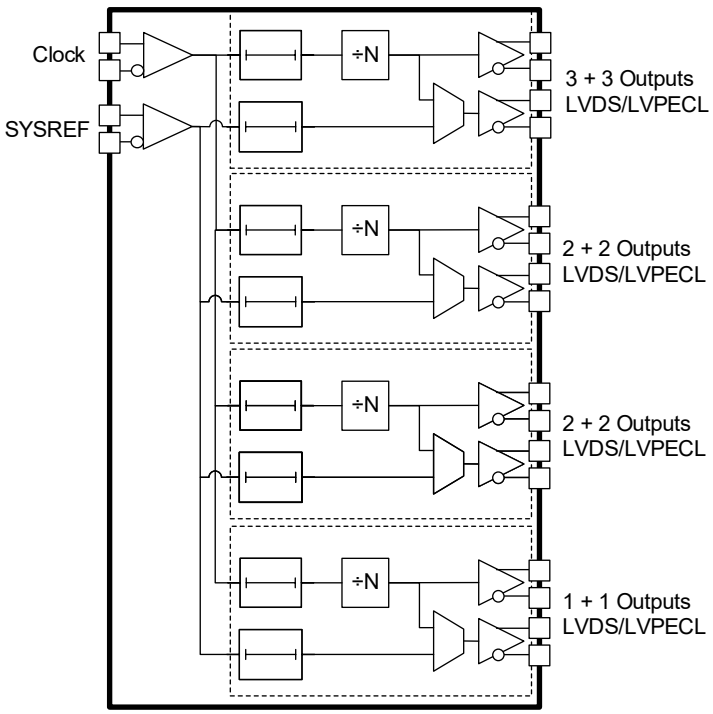

Figure 1. 8V79S68x Simplified Block Diagram

Contents

Figures

1. Functional Description

The evaluation kit is used for demonstrating the 8V79S680, 8V79S683 and RC18016, an integrated, clock and JESD204B SYSREF signal fanout buffer for JESD204B/C applications. The kit can be used to evaluate major parameters including phase noise, clock frequency, output skew, phase alignment, device timing, and the signal waveform. The device on the board accepts any input frequency up to 3GHz for clock input. The device under test distributes the input clock (CLK/nCLK) and JESD204B SYSREF signals (REF/nREF) to four fanout channels. Input clock signals can be frequency divided and are fanned-out to multiple clock (QCLKx) and SYSREF (QREFx) outputs. Configurable phase-delay circuits are available for both clock and SYSREF signals. The propagation delays in all signal paths are fully deterministic to support fixed phase relationships between clock and SYSREF signals within one device.

The board is equipped with on-board LDOs that require a 5V supply. If connecting to a USB C interface, the evaluation board may be powered directly from the USB 3.0 connection. The board is designed to operate over the industrial temperature range from -40°C to +85°C, ambient temperature.

It is recommended to use proper grounding during board operations to avoid ESD damage to the EVB.

1.1 Hardware Setup and Configuration

The following sections describe the crystal, input clock, serial, and output and power functions used for setting up device testing. The setup example is shown in Figure 2.

- **SPI Interface**

  SPI 3-wire interface in this example.

- **Power Supply**

Use 5V from a Power Supply or USB 3.0 with on-board LDO to generate 3.3V power rail. See Figure 3 for power select jumper settings.

- **CLKx Inputs**

  The CLK/nCLK inputs can be AC-coupled or DC coupling and can accept differential input.

  Assume the signal source (for example, lab equipment requires 50Ω to GND termination at the receiver); the **CLK/nCLK** inputs have on-chip terminations of 50Ω to VTC DC bias with AC-coupling.

  REF/nREF is SYSREF differential signal DC coupling with on chip termination.

- **Outputs**

  The outputs are AC-coupled without on-board pull-down or pull-up resistors.

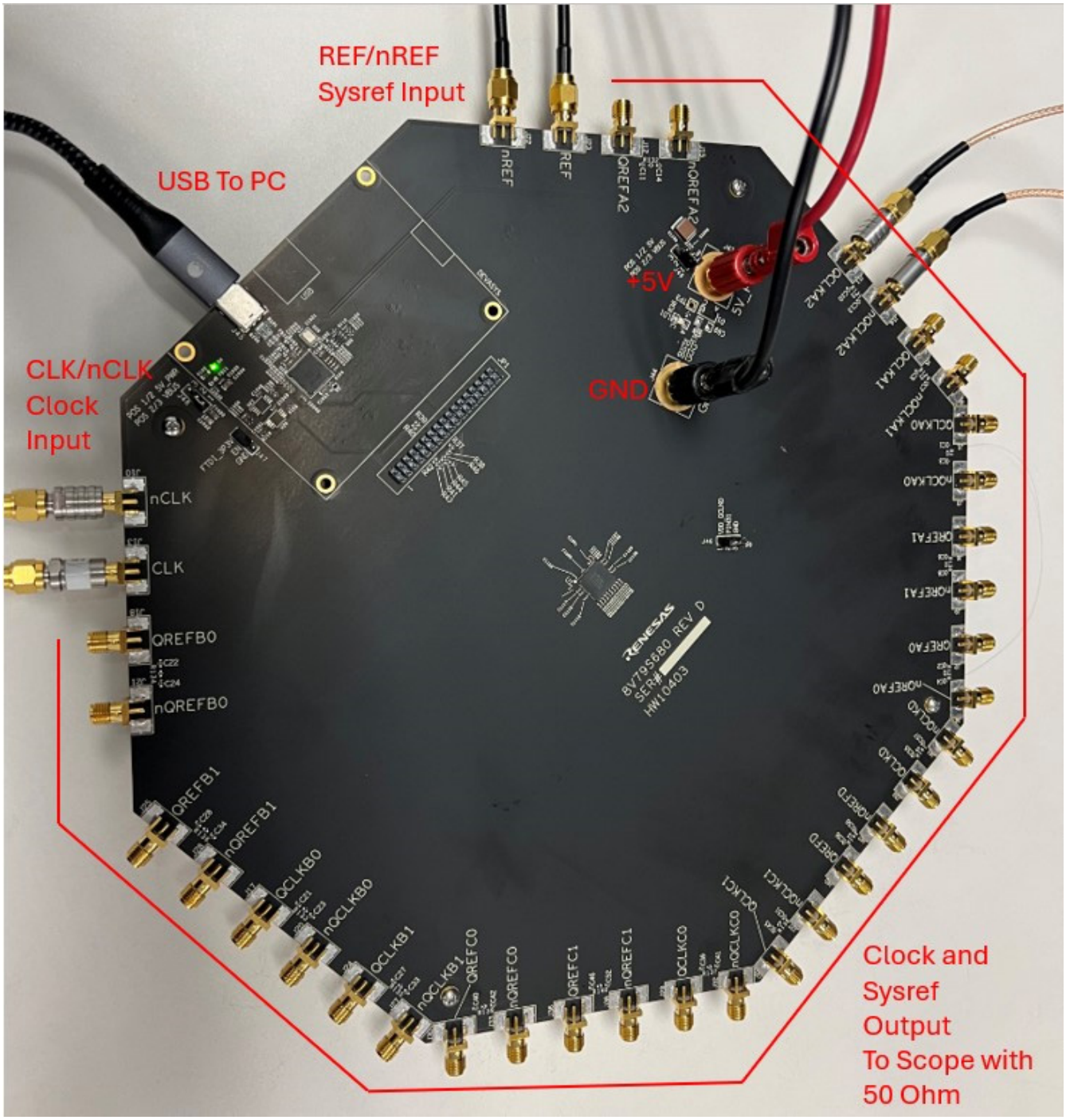

Figure 2. Evaluation Board – General Setup

1.1.1. Power and USB-C Connections to Computer Host

The EVB is connected to a computer host via the USB3.0 to USB-C cable. It is recommended that the cable is connected to a USB3.0 port. However, a USB2.0 port is acceptable for the DUT (8V79S680, 8V79S683 and RC18016) to SPI communications only. The USB 3.0 or external power supply provides +5V as power source to the on-board regulators. The on-board regulators support 3.3V voltages to the EVB.

The DUT voltage source is derived from the on-board voltage regulators for 3.3V. The USB connection will still be required to connect to RICBox.

- Power Connection:
  - Set the power supply voltage to +5V and the current limit to 1A
  - +5V (J43) = +5V
  - GND (J44) = GND
- Expected Current Draw:
  - ~ 0.7 to ~0.8A for 8V79S683 and RC18016
  - ~0.3A to 0.4A for 8V79S680
  - After programming the device, the current can be varied ~0.3A to ~1A during normal operation (device configuration dependent)

1.1.1.1. Power the Device with USB Connection

- Jumper J49 and J48 is used for selecting a +5V power supply from an external power supply or from USB 3.0. Figure 3 and Figure 4 show the schematics of jumper J49 and J48.
- Set jumper on J49 between pins 2 and 3
- Set jumper on J48 between pin 2 and 3
- Ensure that the EVB connects to a USB 3.0 (or newer) port

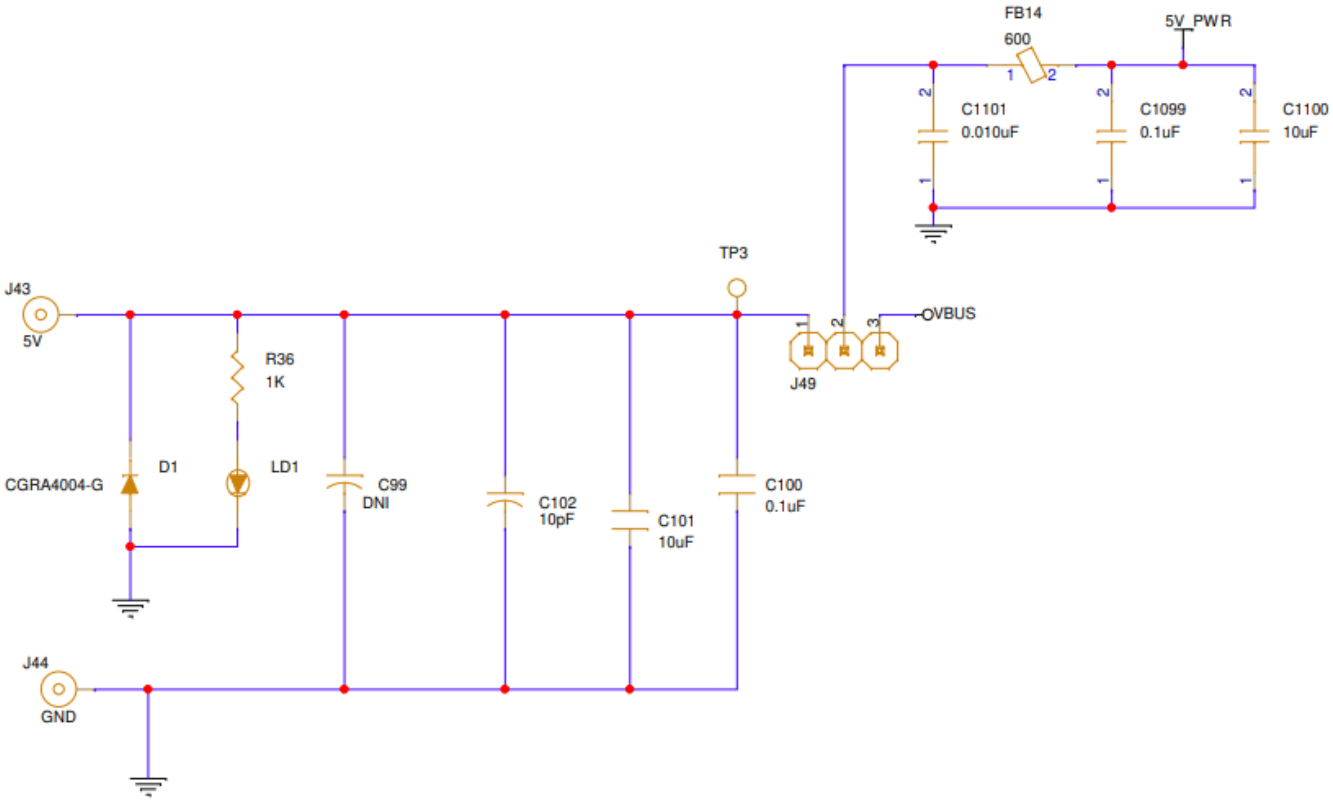

Figure 3. USB Power/External Power Select Jumpers J49

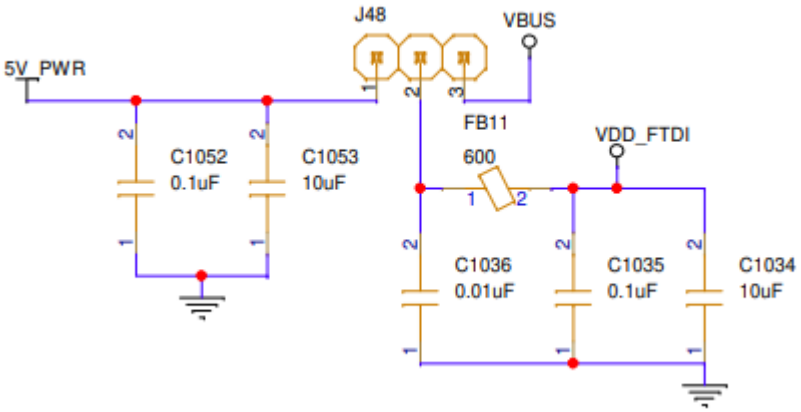

Figure 4. USB Power/External Power Select Jumpers J48

1.1.1.2. Power the Device with External Power Supply Connection and On-board Voltage Regulators

- Set jumper on J49 between pins 1 and 2
- Set jumper on J48 between pins 1 and 2
- Ensure 5V at banana jack J43 (5V) and J44 (GND) connection

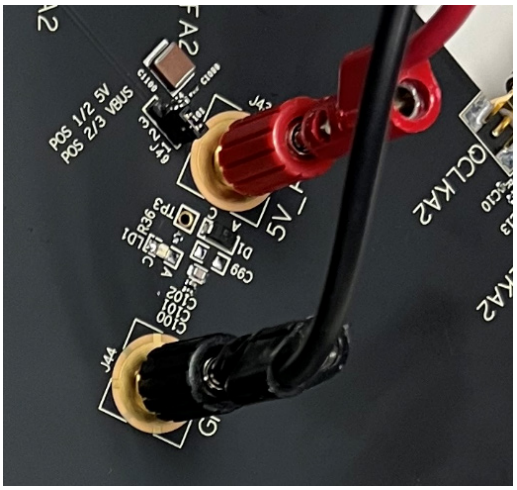

Figure 5. External 5V Board Input

Note: Allow for up to 1A of current with direct power supply.

1.1.2. Clock Inputs (CLK/nCLK) and SysRef Input (REF/nREF)

The Clock input CLK/nCLK and Sysref input REF/nREF can accept differential signals. The input can be AC coupling or DC coupling as shown in Figure 6 and Figure 7. For AC coupling, the DUT has built-in 50Ω to VTC and VTR. The board provides DC bias to VTC/VTR pin as shown in Figure 8.

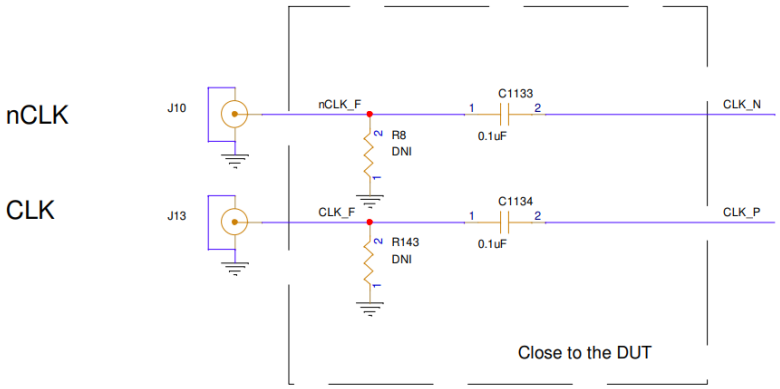

Figure 6. Input AC Coupling

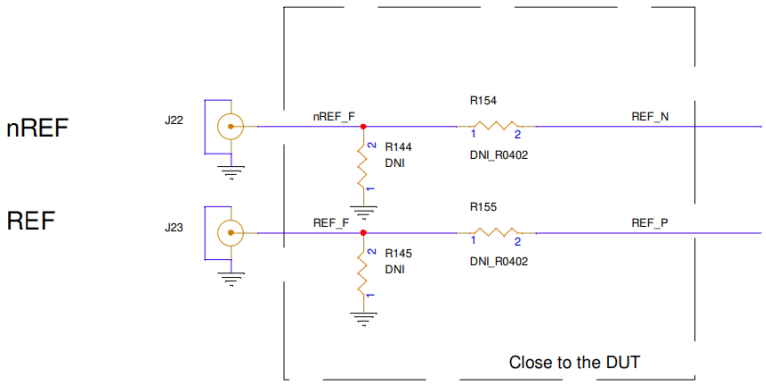

Figure 7. Input DC Coupling

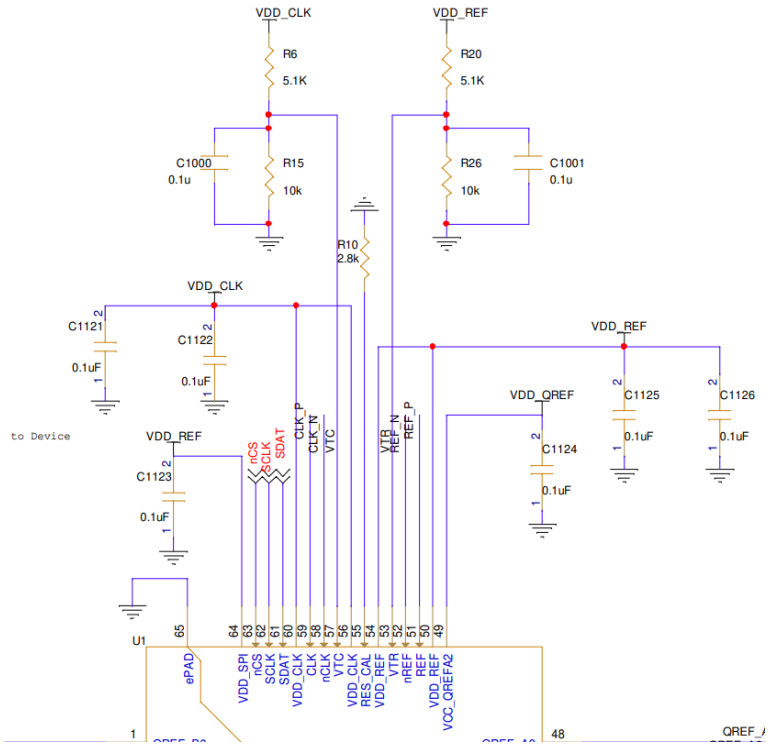

Figure 8. CLK Input VTC and REF Input VTR DC Bias Schematic

The input signal requirement for CLK/nCLK and REF/nREF is provided in the datasheet and is shown in Figure 9. For DC coupling, both amplitude (V_{IN} or V_{DIFF_IN}) and DC offset (V_{CMR}) requirement need to be met. For AC coupling, the DC offset is handled by on-board DC re-bias. Only the input amplitude requirement needs to be met.

V_{IN}	Input Voltage Amplitude[d]	CLK, nCLK REF, nREF		0.15	-	1.2	V
V_{DIFF_IN}	Differential Input Voltage Amplitude[d e]	CLK, nCLK REF, nREF		0.3	-	2.4	V
V_{CMR}	Common Mode Input Voltage			1	-	$V_{DD\_V} - (V_{IN} / 2)$	V

Figure 9. CLK/nCLK and REF/nREF Input Signal Requirements

1.1.3. Clock (QCLKx) and Sysref (QREFx) Outputs

The 8V79S680, 8V79S683 and RC18016 differential output pairs can be programmed to LVDS or LVPECL logic type as shown in Figure 10. In addition, RC18016 output pairs can also be programmed to AC-HCSL.

- The board's output pairs, by default, are AC-coupling as shown in Figure 11 and Figure 12.
- The LVPECL and AC-HCSL driver requires DC current path to switch. This board does not have pull-down resistors before AC-coupling to provide DC current path, therefore LVPECL and AC-HCSL driver cannot be used in this board as is.
- For an LVDS driver, the output will switch without board level termination. After the onboard AC-coupling, it only requires 50Ω termination to GND at the monitor equipment.
- LVDS outputs can be configured to 350mV or 750mV swing.
- Each output can also be disabled when not used.

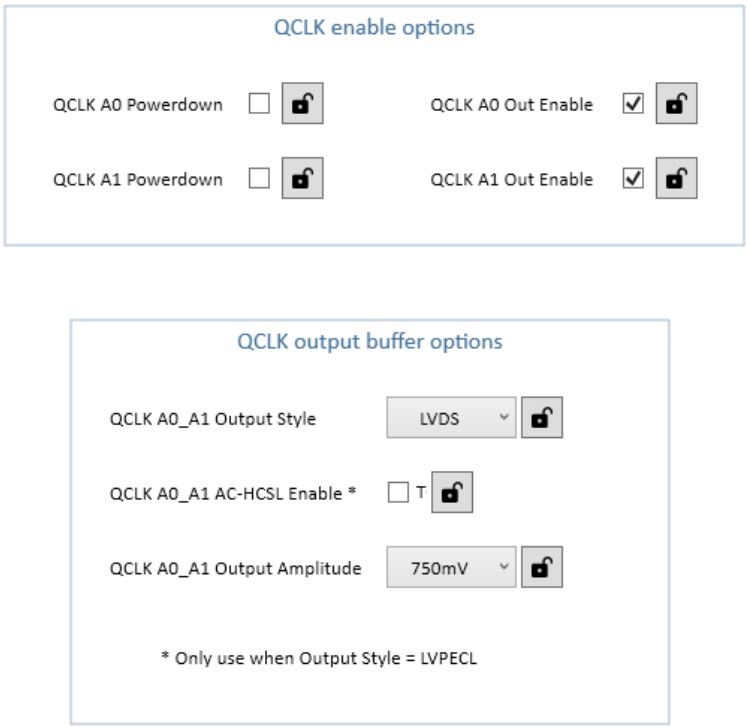

Figure 10. Output Type Options

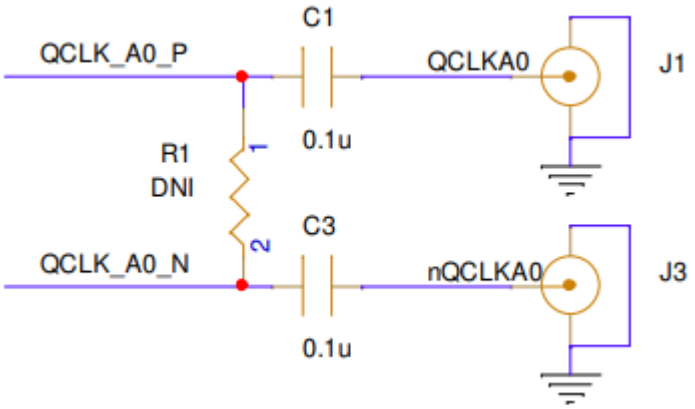

Figure 11. Output Clock AC-Coupling

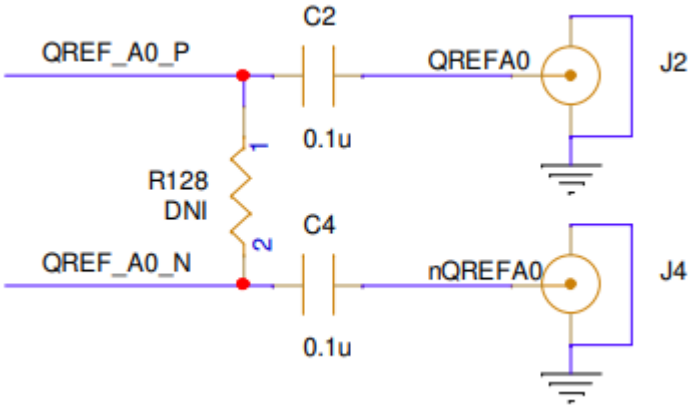

Figure 12. Output QREFx AC-Coupling

1.1.4. Serial Connection

The EVB can be connected to a computer via a USB3.0 to USB-C connector J45. The on-board USB-to-MPSSE Bridge (FTDI FT232HQ) handles the data communication. The bus will be 3-wire SPI.

2. Software Setup and Configuration

2.1.1. Prepare the Software

For software installation instructions, see the Renesas IC Toolbox Software Manual, sections 1 and 11.

2.1.2. Launch the GUI

After installing the Renesas IC Toolbox software, launch the software from the Windows *Start* menu at the bottom-left corner of the screen.

1. Click *Start* > *RICBox* to open the initial RICBox window (see Figure 13).
2. The GUI can create new register configuration from scratch or Open a previously saved existing configuration. In the example below, a new configuration is created for 8V79S683
3. Click *Create new project*.

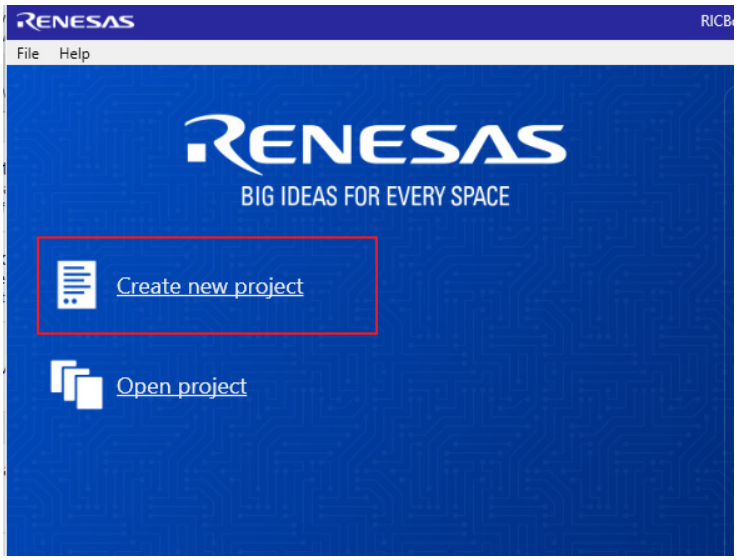

Figure 13. Create New Project in RICBox

4. Select *RC180xx* from the “Select a Product Family” list (see Figure 14).
5. Select the product variant to evaluate, then click *OK*. In this example, the 8V79S683 is selected.

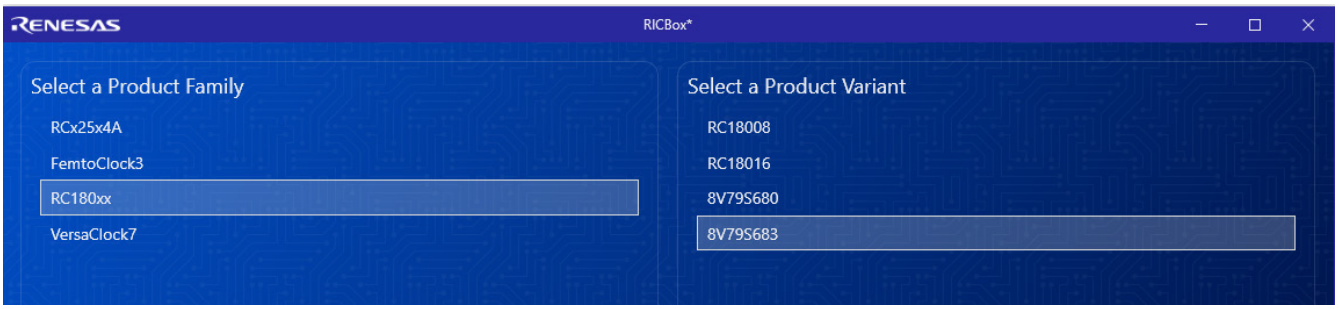

Figure 14. Selecting 8V79S683 Device GUI in RICBox

6. Click *Finish* and then the Block Diagram logo at side panel to go straight to the Block Diagram (see Figure 15).

Figure 15. RICBox GUI Menu Buttons

7. Enter the Clock and Sysref Input frequencies as shown in Figure 16.
8. Enter the values in the Delay Calibration Block (see Figure 17 for an example). This block is for setting Sysref delay step unit. For more details on setting the Delay Unit Multiplier, M_DCB, P_DCB and other parameters, refer to the 8V79S680 datasheet Delay Calibration Block (DCB) section.

   DCB_CAL setting: Activate DCB_CAL = 1 and check the DAC_CODE status for indicate successful calibration. Figure 18 displays the DAC_CODE on the GUI.
9. Set the clock output QCLKx output frequency and phase delay (see Figure 19 for an example). INIT_CLK is required to activate QCLKx divider and Phase Delay.
10. Set the clock output QCLKx output driver type and amplitude (see Figure 20 for an example).
11. Set the SysRef output QREFx output driver type, amplitude and phase delay (see Figure 21 for an example). For more details, refer to the 8V79S680 datasheet.

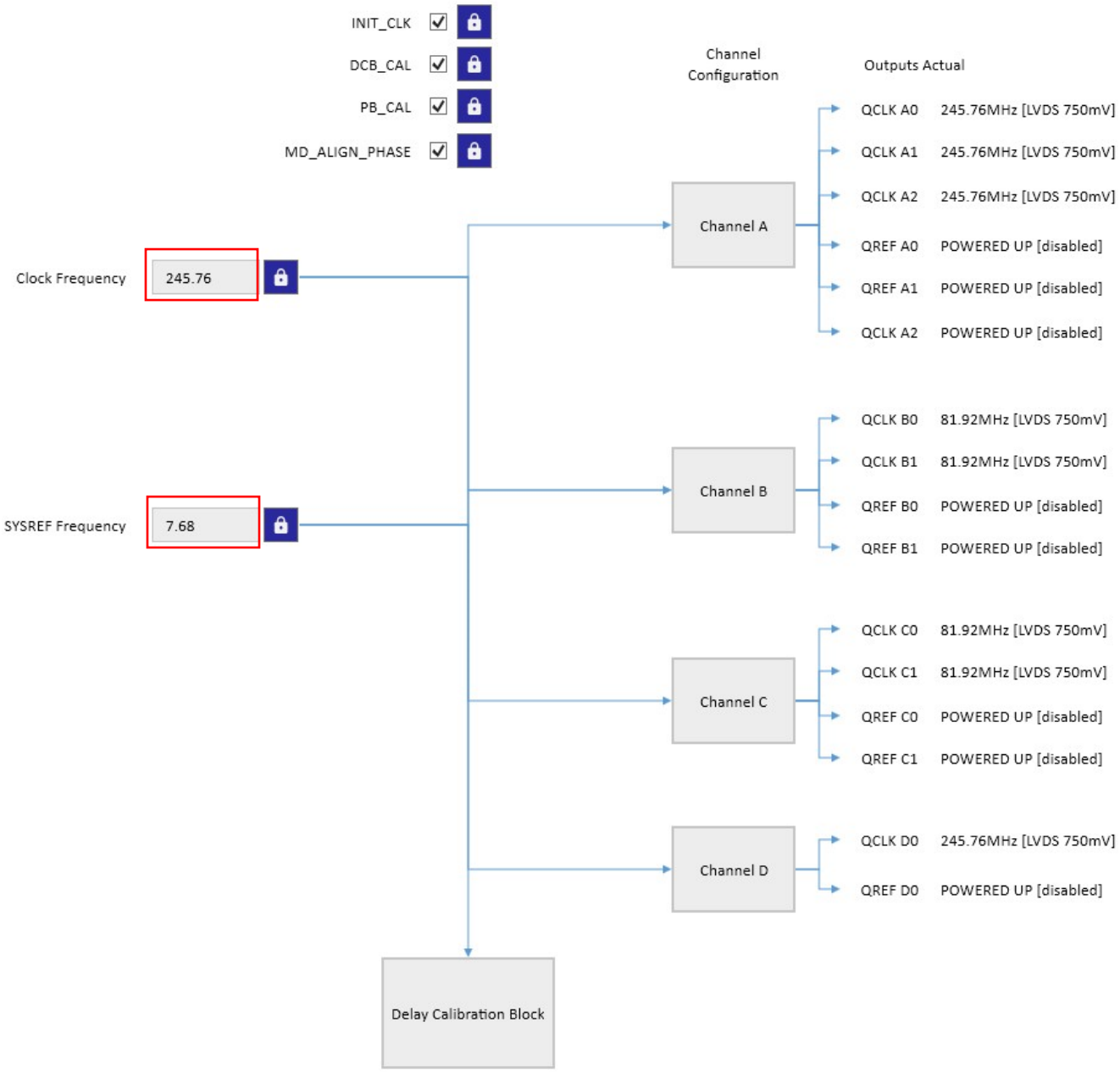

Figure 16. CLK/nCLK (Clock) and REF/nREF (Sysref) Input Frequency Setting

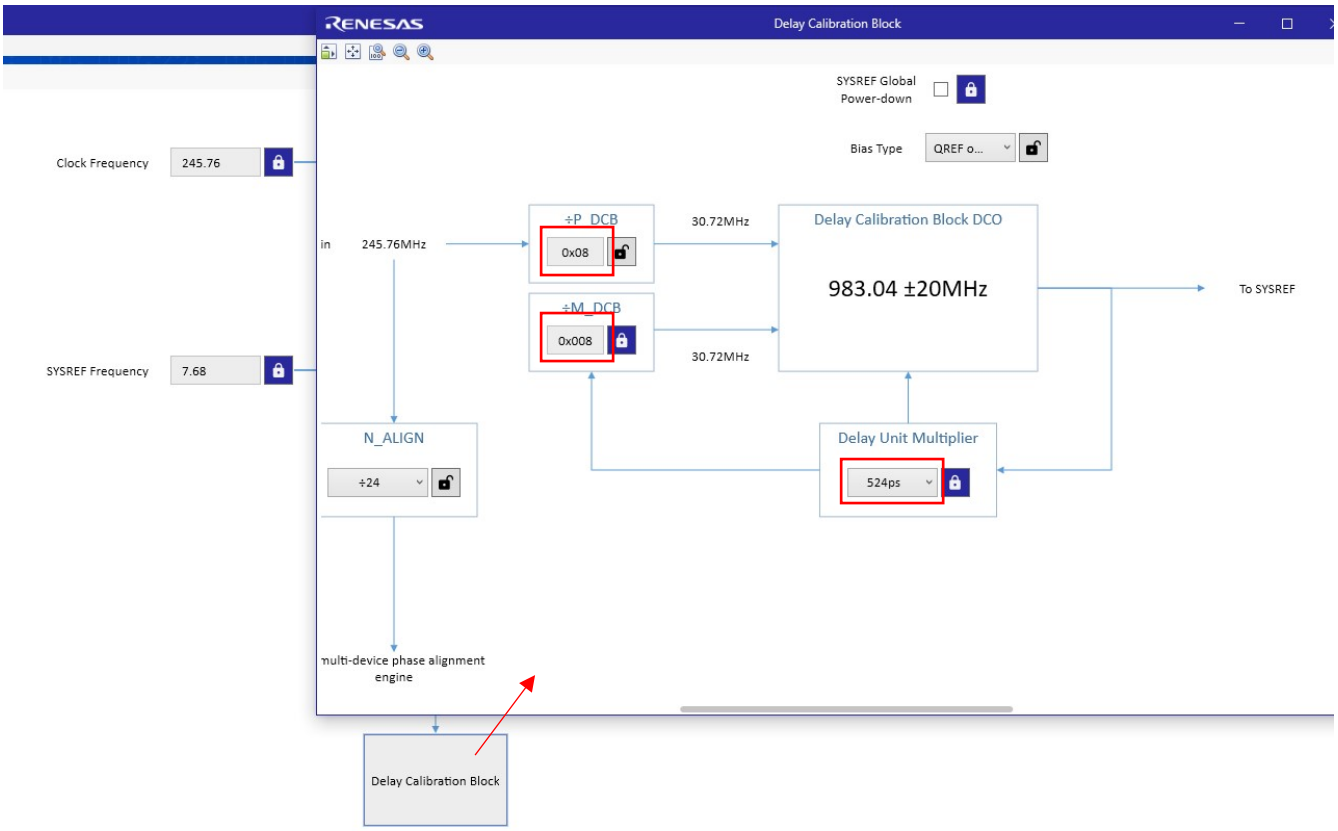

Figure 17. Delay Calibration Block

Note: Activate DCB_CAL to take effect.

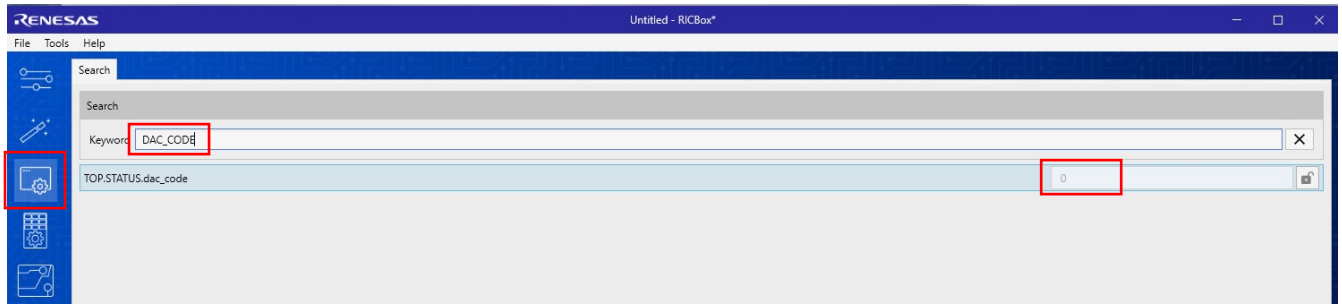

Figure 18. Activate DCB_CAL and Check DAC_CODE Value

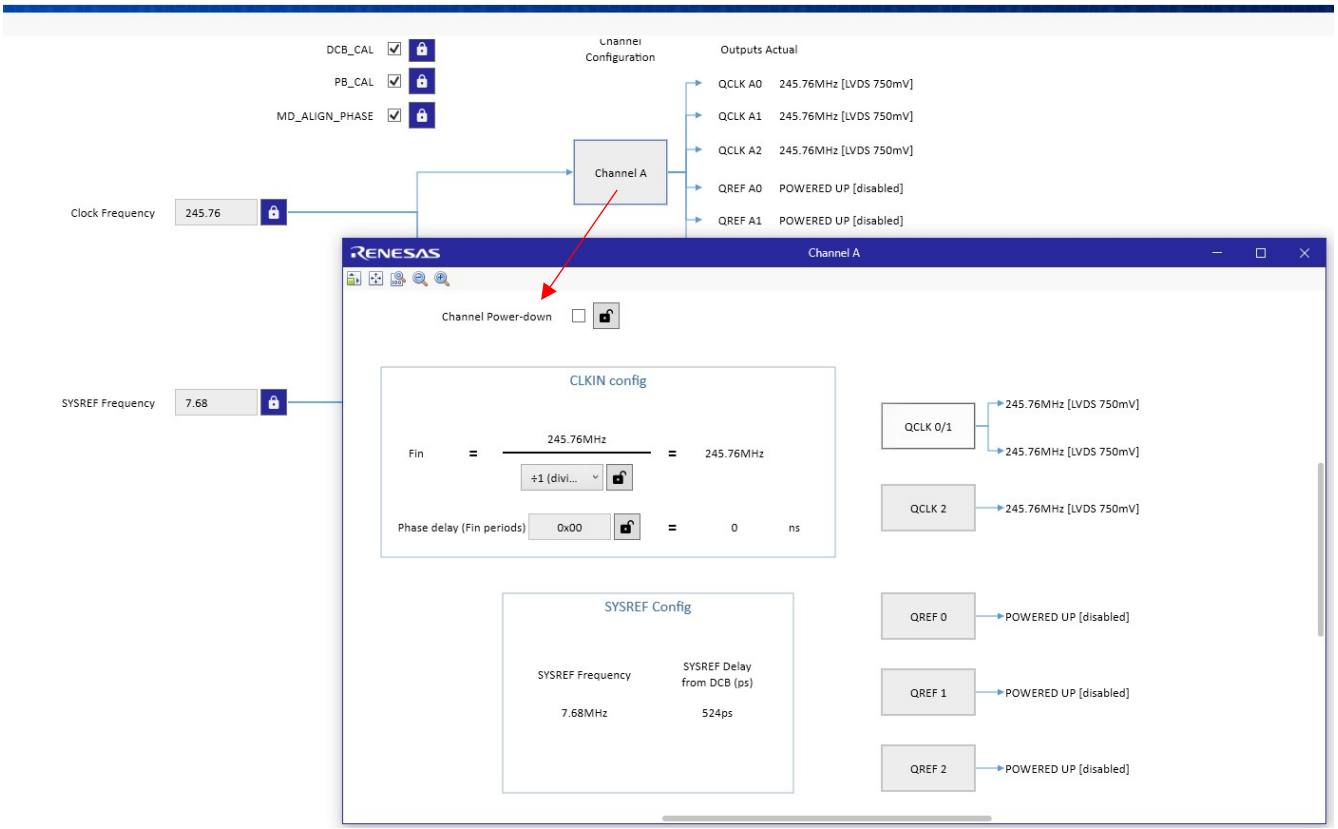

Figure 19. Output Channel Frequency and Phase Delay Setting

Note: Activate INIT_CLK to take effect.

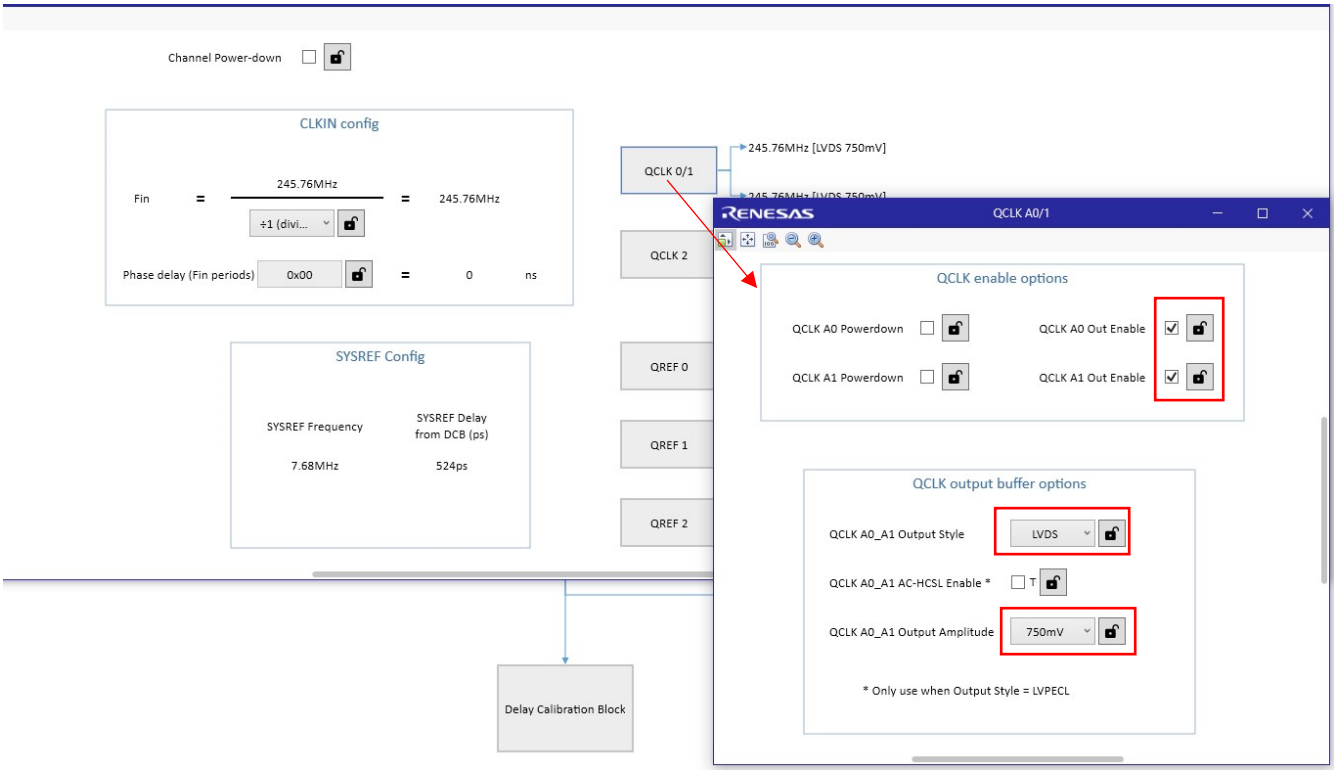

Figure 20. QCLKx Output Driver Type and Amplitude Setting

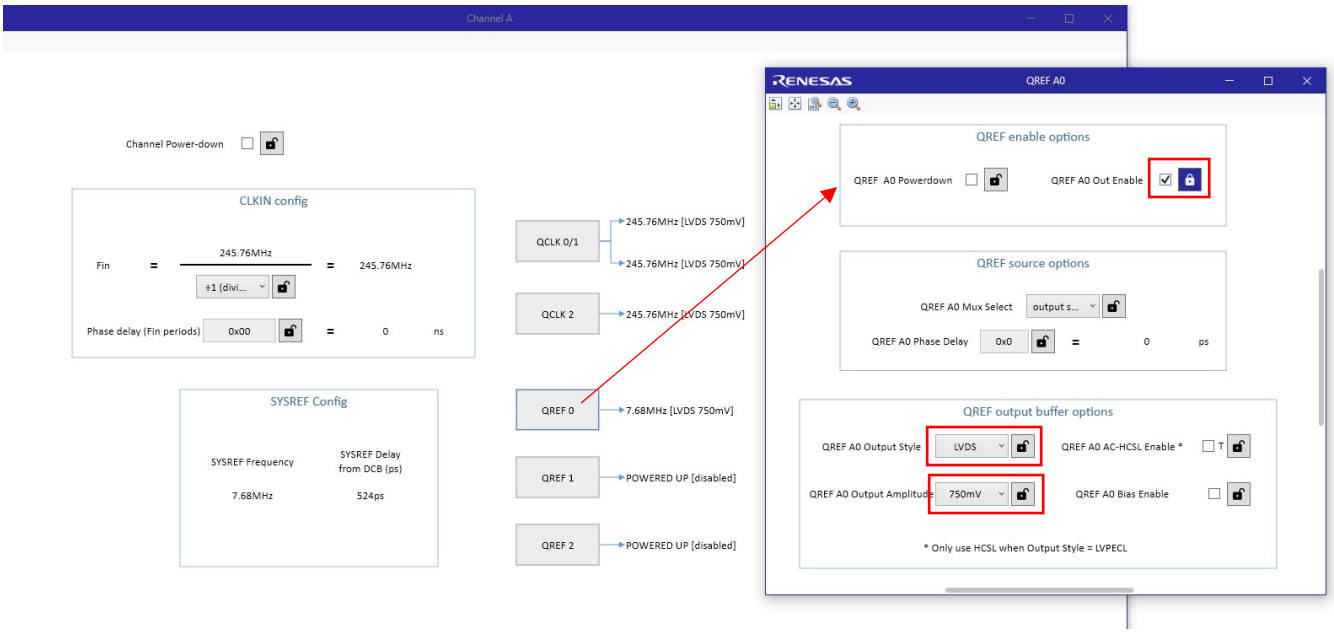

Figure 21. QREFx Output Driver Type and Phase Delay Setting

Note: QREF Phase Delay Adjust does not need to activate INIT_CLK to take effect.

2.1.3. Configure the Evaluation Board

1. To establish communication between the EVB and the GUI, click the *Not Connected* button (1) in the lower right corner, then click *Connect* (2) (see Figure 22).

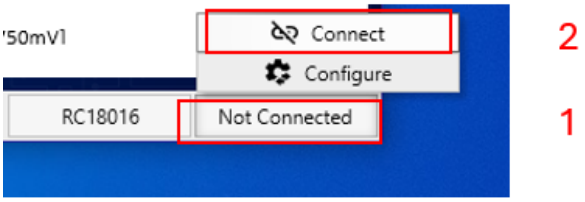

Figure 22. Connect to the Device in RICBox

2. Once the RICBox connection is established to the EVB, the *Not Connected* button will change to *Connected* (see Figure 23).

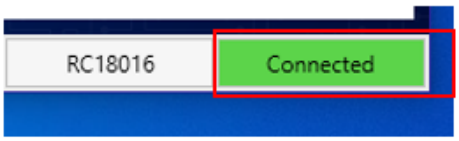

Figure 23. Connected Button

3. Click the *Program* button to write all the changed registers from the GUI to the on-board device. Any register changes made after clicking the *Program* button will occur in real-time and the device will update (see Figure 24).

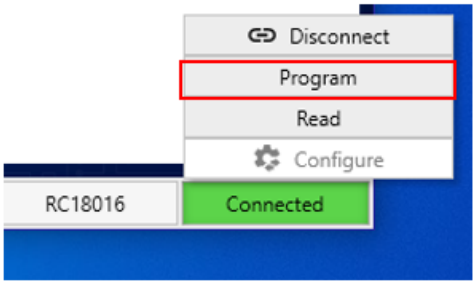

Figure 24. Program Button

3. Board Design

Note: The 8V79S680 EVB schematic and BOM is available upon request.

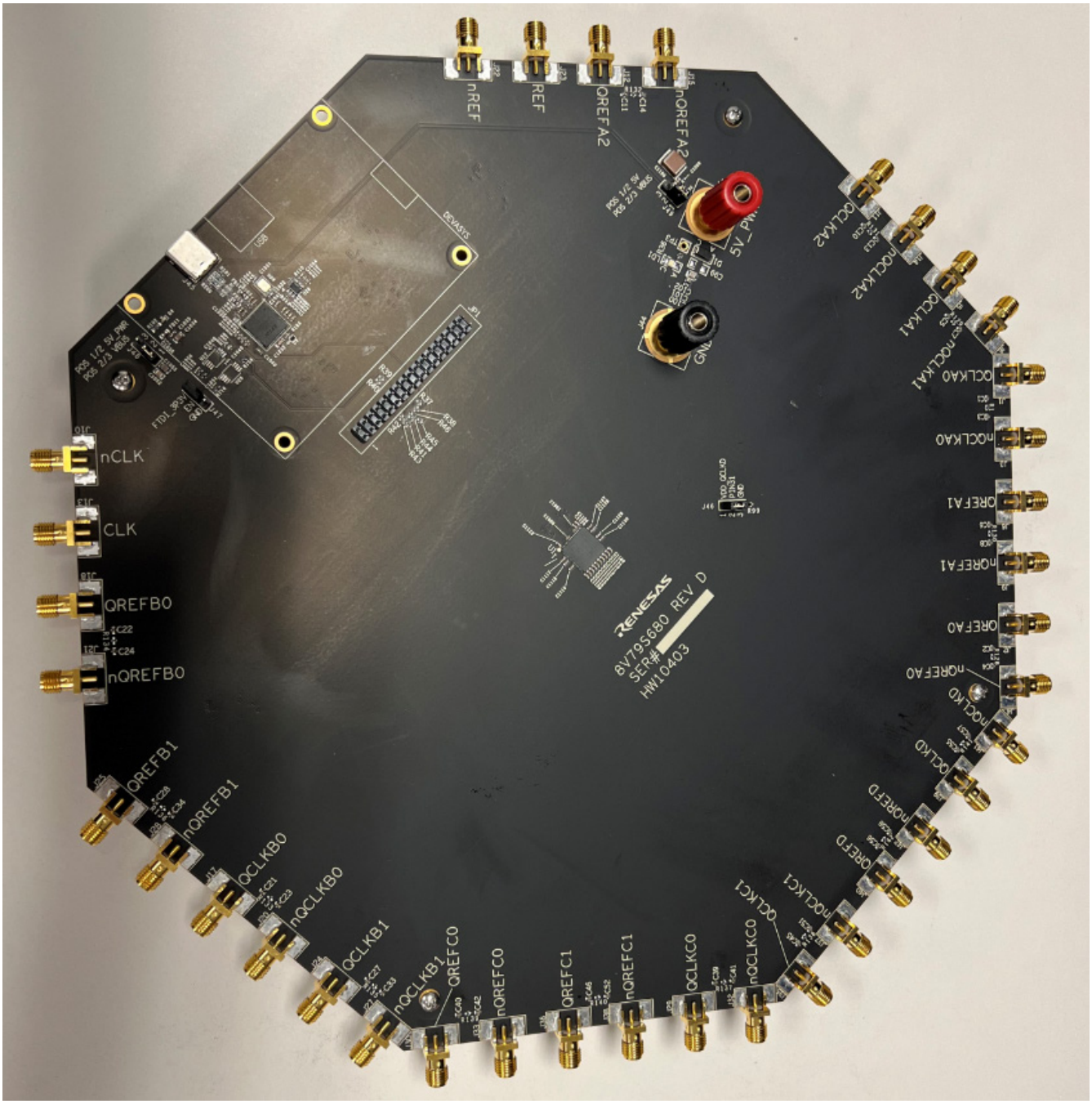

Figure 25. 8V79S680/8V79S683/RC18016 Evaluation Board (top)

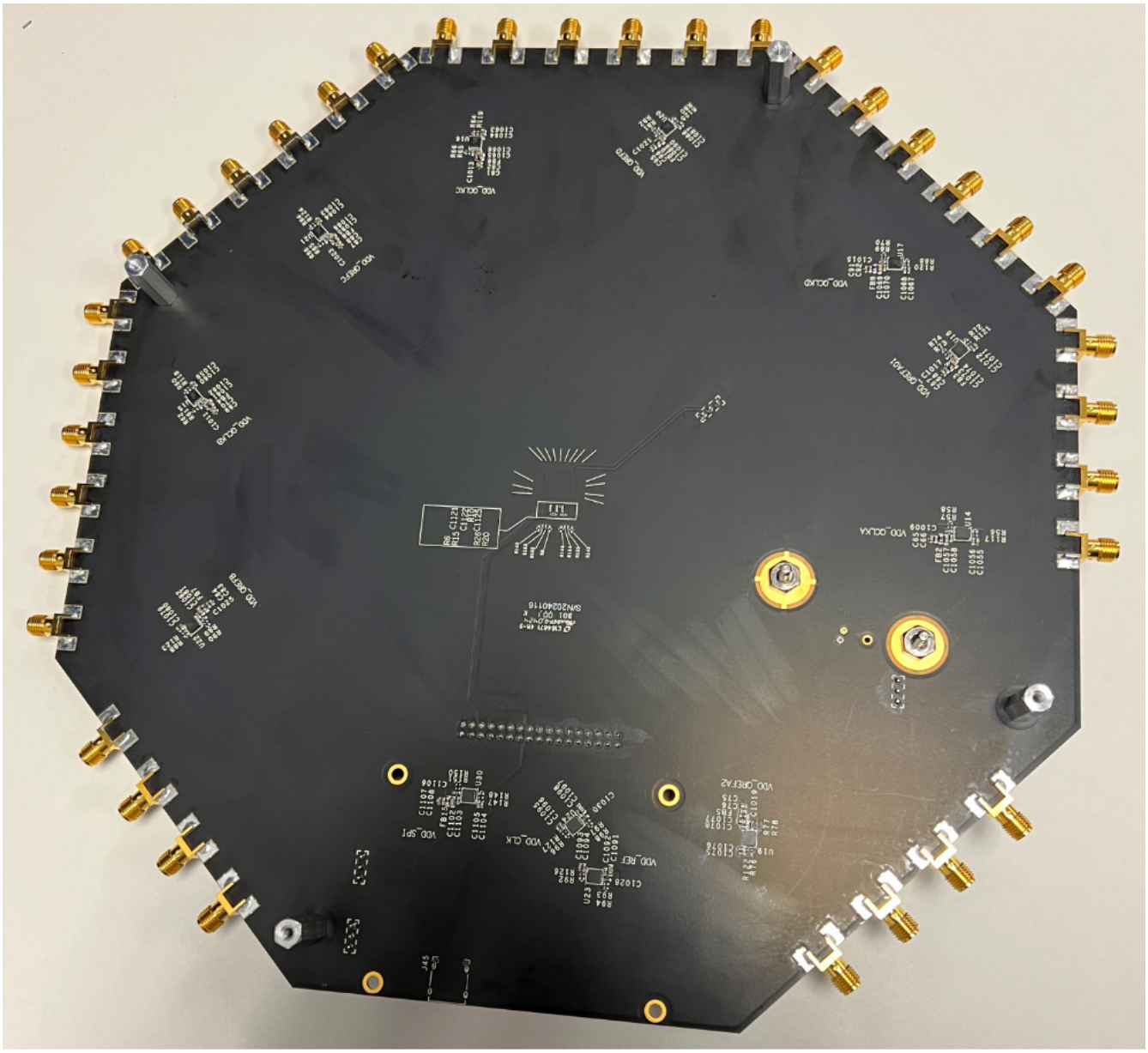

Figure 26. 8V79S680/8V79S683/RC18016 Evaluation Board (bottom)

4. Ordering Information

Part Number	Description
8V79S680-EVK	8V79S680 Evaluation Board
8V79S683-EVK	8V79S683 Evaluation Board
RC18016-EVK	RC18016 Evaluation Board

5. Revision History

Revision	Date	Description
1.00	Jul 5, 2024	Initial release.