CLK-104a/b Boards Using Renesas RF-PLL and RF-Synthesizer Solutions

Renesas collaborated with AMD to design a version of the CLK-104 board to work with AMD's platform for RF SoC solutions. The CLK-104 board uses an RF-PLL device to provide a reference for up to 12 RF clocks, including one for an onboard RF-synthesizer device, and the 8V97003 as a reference clock to generate two output clocks up to 18GHz for ADC/DAC applications. Two versions of the CLK-104 boards are available: the CLK-104a uses an RF-PLL device with the 8V19N491-24, and the CLK-104b uses the 8V19N882. The rest of the design is identical for both versions.

The CLK-104 is designed as a plug-in module to the AMD ZCU-1275 (16×16) platform. By plugging in to the mainboard socket, the CLK-104 acquires power supplies, an I2C/SPI interface, and input reference clocks. The following figure shows the bottom of the CLK-104 board with a male connector to match with ZCU-1275 board. For information on how to operate and access the CLK-104 board, see the *ZCU-1275 User Manual*.

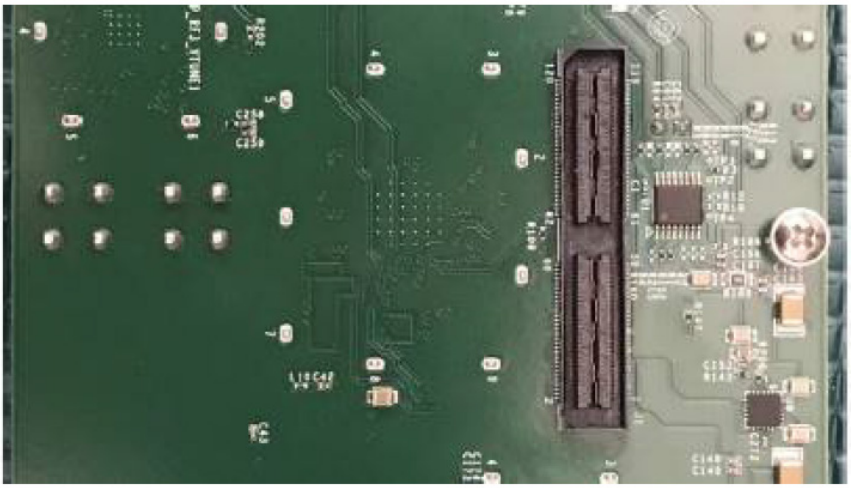


Figure 1. Back of CLK-104 Board with Mating Connector with AMD ZCU-1275

The CLK-104 board is designed to function as a standalone testing platform. For more information, see the following sections.

Contents

1. System Overview

The CLK-104 board consists an RF-PLL device (8V19N491-24 or 8V19N882) and two RF-synthesizer devices (2x 8V97003). RF-PLL device can take one of the following three reference clocks as inputs to its CLK0/nCLK0 and CLK1/nCLK1 (both are differential inputs):

- 156.25MHz from AMD RF SoC (ZCU-1275) board through above-mentioned connector
- An onboard 10MHz TCXO
- An external clock connected to SMA connectors

The RF-PLL devices generate the following output clocks:

- A differential output for RF-synthesizer #1
- A differential output for RF-synthesizer #1
- A differential output for RF-synthesizer #2
- A differential output to a pair of onboard SMA connectors for monitoring
- 6 differential outputs connecting to ZCU-1275 board (through the connector)

A diagram of the CLK-104 board is displayed below.

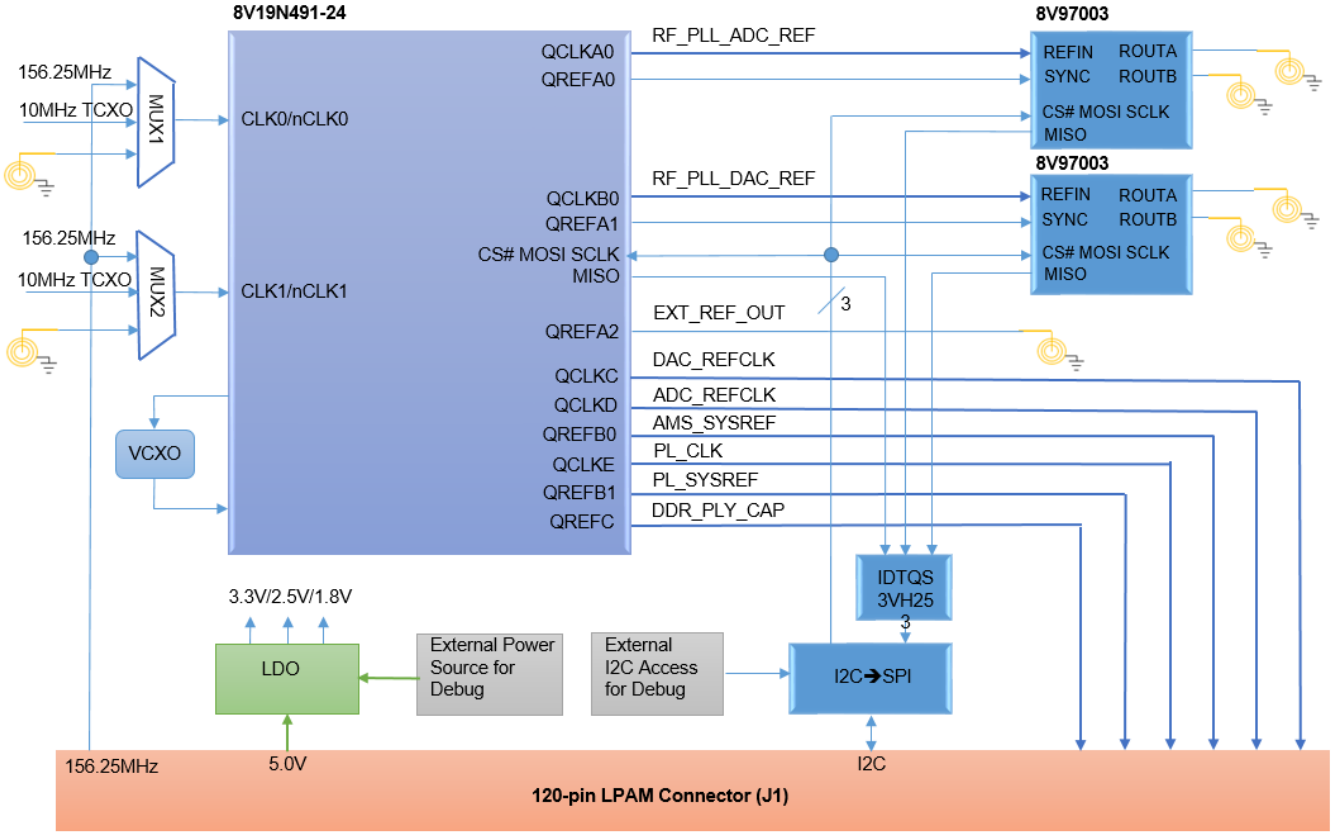


Figure 2. CLK-104 Board Diagram

The RF-PLL device and two RF-synthesizer devices are accessible by an SPI interface. As stated above, they can be accessed by an I2C-to-SPI converter from/to the ZCU-1275 board. The I2C signals are within the mating connector between the two boards. Please note that the SPI port has been connected to an onboard 5 × 2 header by which an external SPI master can access all devices on CLK-104 board.

The CLK-104 board can be powered locally or by plugging it into the ZCU-1275. For more information, see “Standalone Testing.”

2. Standalone Testing

If an AMD ZCU-1275 board is not available, the CLK-104 board can be tested standalone. To conduct a standalone test or evaluation, complete the following steps and information below.

2.1 Power Supply

The connector between the CLK-104 and ZCU-1275 contains +5V, +3.3V, and ground pins that provide power supplies to the CLK-104 board when plugged in. Copper pads are available on the CLK-104 board to facilitate the power supplies coming from a bench power supply. Solder a thick wire on these pads and connect +5V, +3.3V, and GND to a bench power supply. For the locations of these copper pads, see Figure 3.

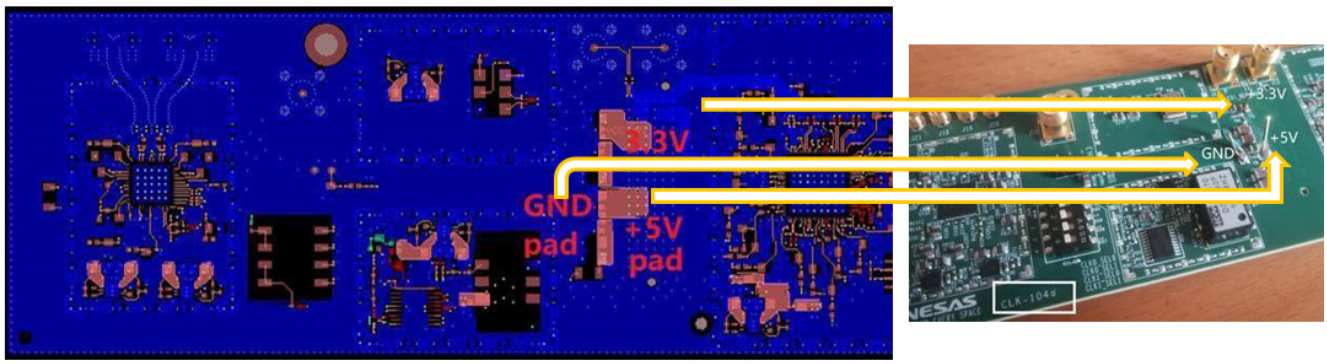


Figure 3. +5V, +3.3V, and GND Copper Pads are Provided for Local Power Supplies

3. SPI Interface

The 5 × 2 header is installed to make connections between an external SPI master to the devices on the CLK-104 board. Use an FTDI dangle (C232HM) to connect the SCLK, SDI, SDO, and nCS signals as labelled in the header below.

Note: Jump J4, J5, or J6 one at a time to access one of three devices on the board.

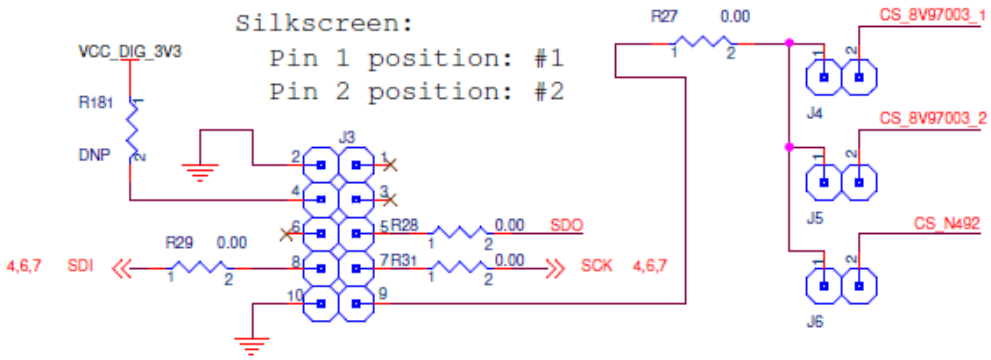


Figure 4. SPI Header for Connecting to 8V19N491-24 or 2x 8V19N882 One at a Time

4. Input Reference Selection

A 4-bit dip-switch (J11) is used to select one of three available reference clocks for the two input clocks of the RF-PLL (8V19N491-24 or 8V19N882). Two mux devices are used so the two input clocks going to the RF-PLL device can be selected individually (see Dipswitch selection pin allocation below).

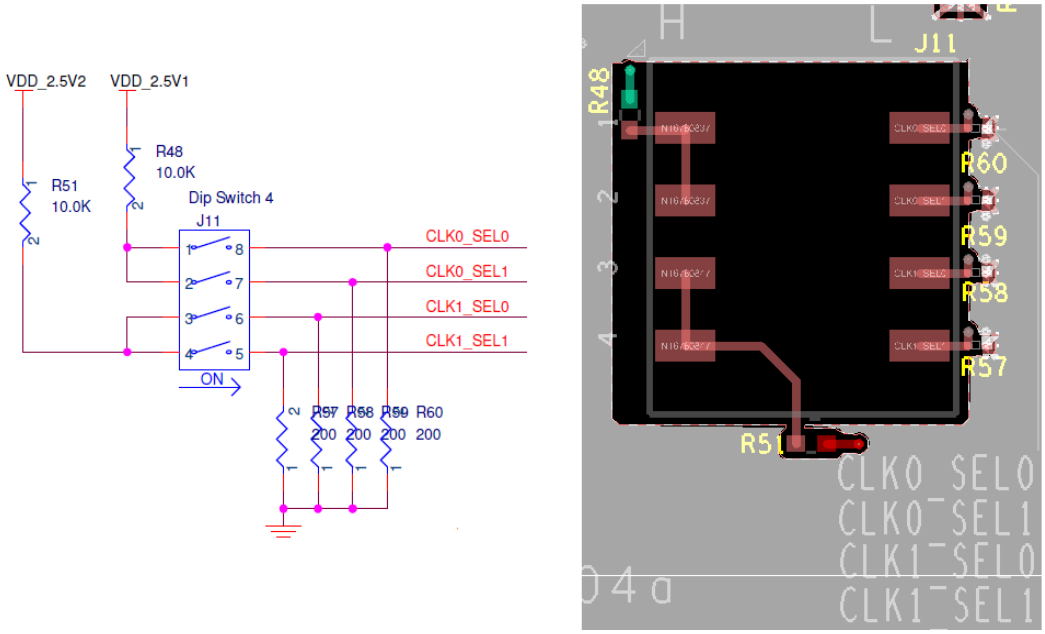


Figure 5. Dip-Switch to Individually Select an Input Reference for CLK0/nCLK0 and CLK1/nCLK1

Follow onboard silkscreen labels for “H” or “L” position (see Figure 5) for the Dipswitch (J11) pins. The reference selection table is as follows.

Table 1. Reference Selections for RF_PLL Inputs (CLK0/nCLK0 and CLK1/nCLK1)

Destination	CLK0_SEL0 Pin	CLK0_SEL1 Pin	Reference Selected
CLK0_P/N	H	H	X
	H	L	SMA_IN
	L	H	TCXO_IN
	L	L	SFP_RCV_CK_P/N
	CLK1_SEL0 Pin	**CLK1_SEL1 Pin**	
CLK1_P/N	H	H	SFP_RCV_CK_P/N
	H	L	TCXO_IN
	L	H	SMA_IN
	L	L	X

5. Using Timing Commander to Program the Devices

For ease of use, Renesas' free-of-charge software tool – Timing Commander is recommended to configure and program the CLK-104 board/devices (8V19N491-24, 8V19N882, and 8V97003). If you have any questions on the Timing Commander software download or TCP/TCS files, contact Renesas Timing Technical Support via Renesas.com

In the Timing Commander GUI, when the settings file (.tcs) is loaded:

1. Click on the button in the upper-right corner to display the Connection Settings window.

2. Select USB/SPI in the Connection Settings window.

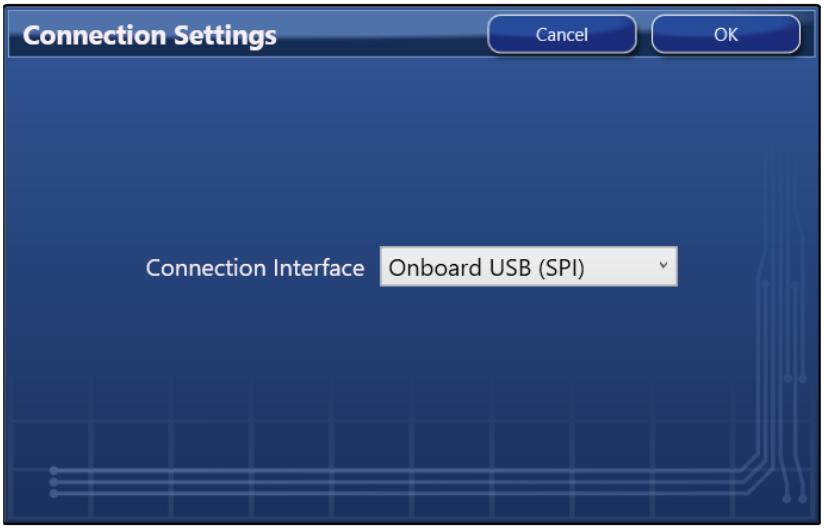


Figure 6. Connection Setting window to select SPI mode

3. Click the chip symbol button in the upper-right corner of the GUI to initiate the connection to the targeted device.

6. Output Clock Monitoring/Measurement

The following SMA connector pairs are available to monitor/measure the output frequencies from devices on the CLK-104 board:

- J15/J16 – 8V97001 #1 Output A
- J14/J17 – 8V97001 #1 Output B
- J19/J20 – 8V97001 #2 Output A
- J18/J21 – 8V97001 #2 Output B
- J12/J13 – 8V19N491-24 Output QREF_A2/nQREF_A2

Other outputs are connected to the connector, and therefore, are not accessible.

6.1 Example 1: Phase Noise Plot from J12/J13 (122.88MHz)

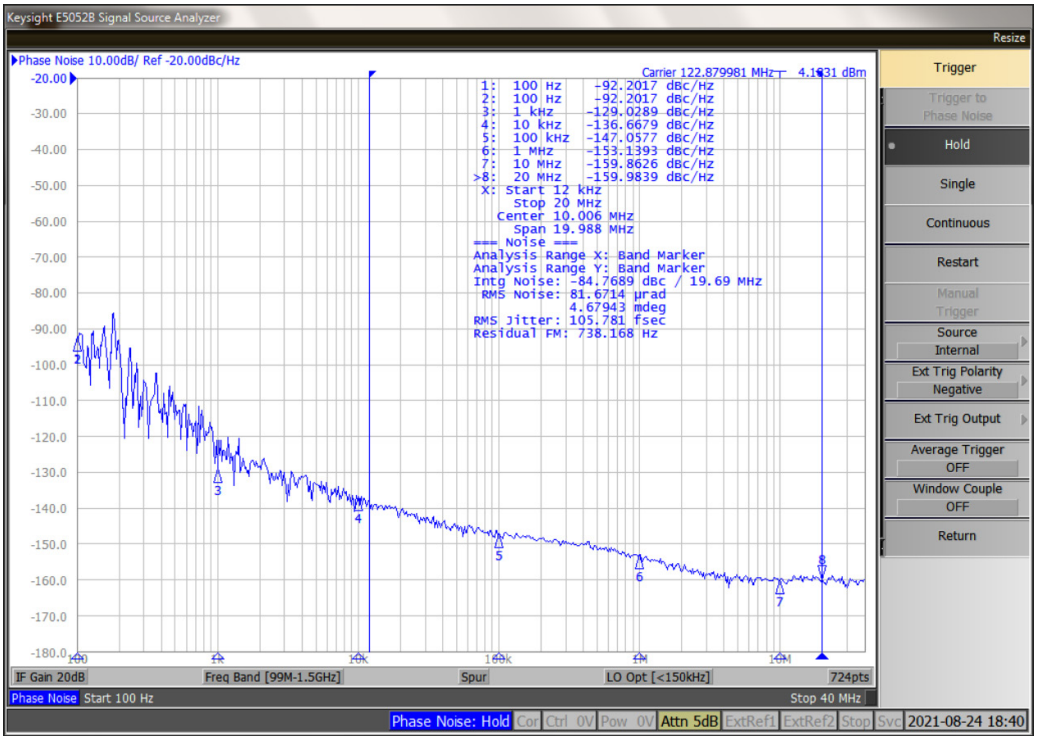


Figure 7. Phase Noise Plot of 122.88MHz Output from 8V19N491-24 QREF_A2/nQREF_A2

6.2 Example 2: Phase Noise Plot from 8V97003 #1 (1GHz)

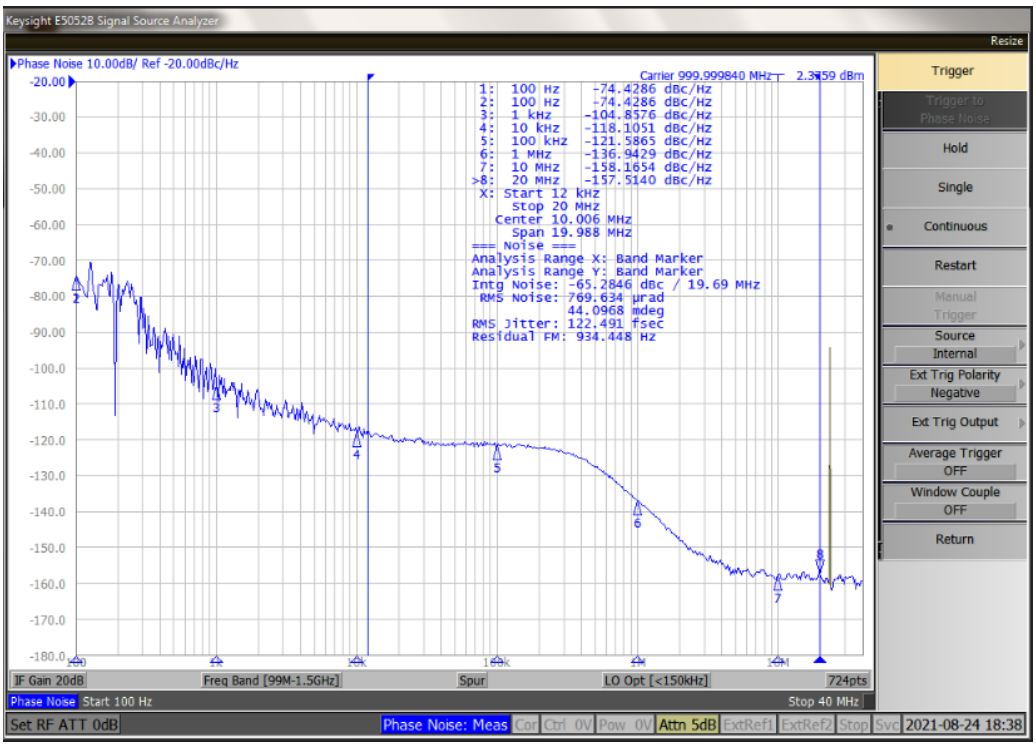


Figure 8. Phase Noise Plot of 1000MHz Output from 8V97002 #1 ROUT_A/nROUT_A

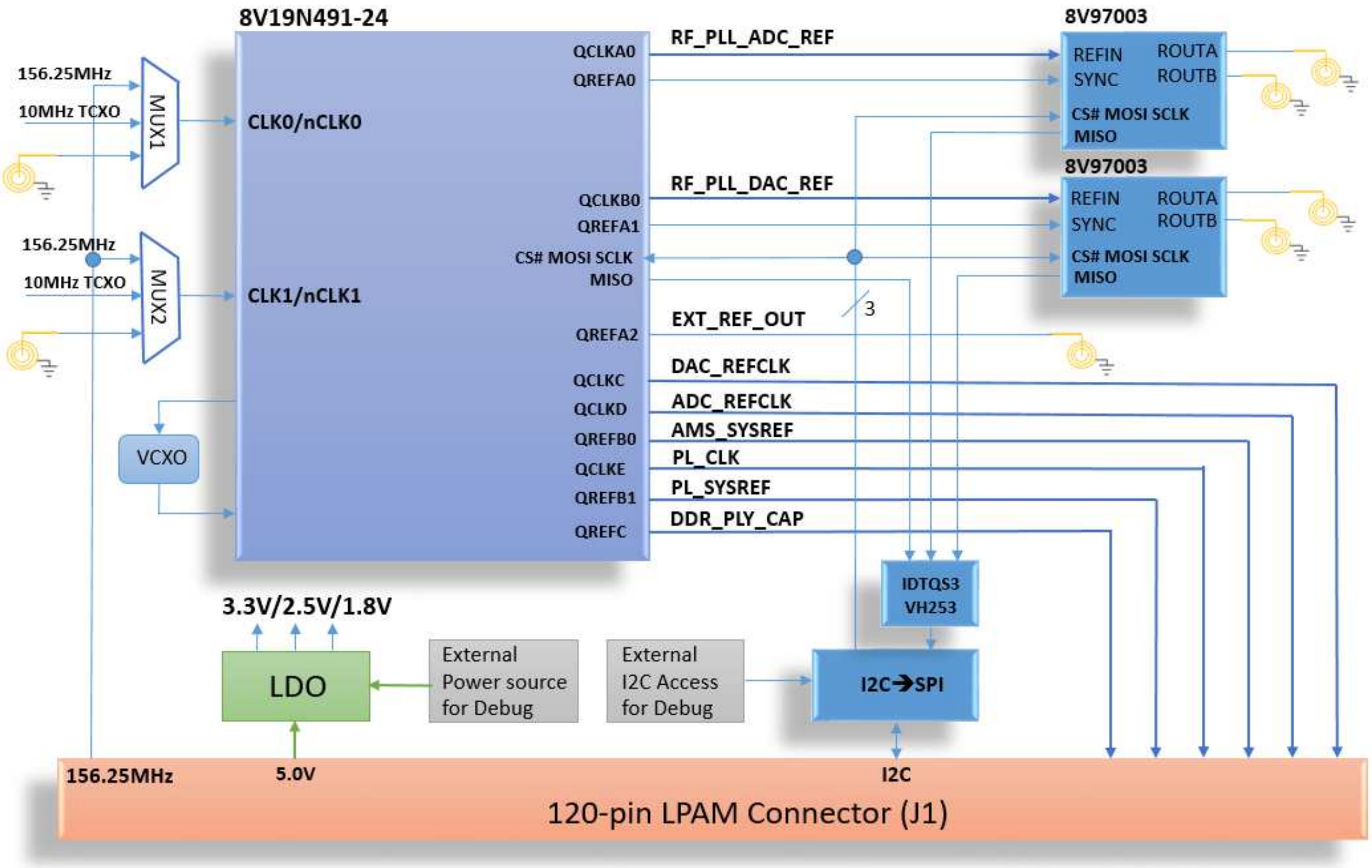
7. Board Schematics

The board schematics are located at the end of this document.

8. Revision History

Revision	Date	Description
1.01	Jul 22, 2024	▪ Replaced all instances of Xilinx with AMD. ▪ Updated schematics.
1.00	Nov 26, 2021	Initial release.

CLK-104 RF CLOCK BLOCK DIAGRAM



Renesas
1140 West Warner Rd.
Tempe, AZ 85284

Title: CLK-104			
Size: B	HW Number: 987456321587	Engineer: SZ	Rev.: A
	Date: 07/16/2024	Sheet: 1 of 11	

REV.	DESCRIPTION	DATE	ENGINEER
A	CLK-104 INITIAL DRAFT	12/10/2020	SZ
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-	----------	-------	--

Renesas
1140 West Warner Rd.
Tempe, AZ 85284

Title: CLK-104

Size	HW Number:	Engineer:	Rev.
B	987456321587	SZ	A
	Date: 07/16/2024	Sheet: 2 of 11	

J1A

LPAM-20-01.0-L-06-2-K-TR

J1B

B4 — SPI_MUX_SEL0
B5 — SPI_MUX_SEL1
B8 — AMS_SYSREF_P 5
B9 — AMS_SYSREF_N 5
B12 — PL_SYSREF_P 5
B13 — PL_SYSREF_N 5
B15 — PL_CLK_P 5
B16 — PL_CLK_N 5
B18 — DDR_PLY_CAP_P 5
B19 — DDR_PLY_CAP_N 5

LPAM-20-01.0-L-06-2-K-TR

J1C

LPAM-20-01.0-L-06-2-K-TR

VCC_DIG_3V3

R6 DNP, R7 DNP, R2 DNP, R3 DNP

CS_N492 — 4

U1 — SC18IS602B

SS0/GPIO0 1
SS1/GPIO1 2
RESET 3
VSS 4
MISO 5
MOSI 6
SDA 7
SCL 8
INT 9
SS2/GPIO2 10
SPICLK 11
VDD 12
SS3/GPIO3 13
A0 14
A1 15
A2 16

SDO — R12 0.00
SDI — R13 0.00
CLK104_SDA
CLK104_SCL

R4 0.1uF, R5 10.0K, R1 DNP DNP

CS_8V97003_2 — R11 0.00 — CS_8V97003_1

SCK

R8 10.0K, R9 10.0K, R10 10.0K
R14 DNP, R15 DNP, R16 DNP

Jumped to use local SPI header

J2

J1D

LPAM-20-01.0-L-06-2-K-TR

VCC_3V3
UTIL_5V0_A

J1E

LPAM-20-01.0-L-06-2-K-TR

E1 — DAC_REFCLK_P 5
E2 — DAC_REFCLK_N 5
E9 — SYNC_IN — SYNC_IN 5
E15 — SFP_RCV_CLK_P 5
E16 — SFP_RCV_CLK_N 5
E18 — CLK104_SCL
E19 — CLK104_SDA

VCC_3V3
UTIL_5V0_A

J1F

LPAM-20-01.0-L-06-2-K-TR

VCC_DIG_3V3

C2 10uF, C3 0.1uF

U2 — IDTQS3VH253QG8

VCC_16 16
YA_7 7
YB_9 9
EA_B_1 1
EB_B_15 15
S0_14 14
S1_2 2
GND_8 8
I0A_6 6
I1A_5 5
I2A_4 4
I3A_3 3
I0B_10 10
I1B_11 11
I2B_12 12
I3B_13 13

SDO
SPI_MUX_SEL0
SPI_MUX_SEL1

8V97003_MAXOUT1 6
8V97003_MAXOUT2 7
N492_MAXOUT 4

R17 DNP, R18 DNP, R19 DNP
R20 10.0K, R21 10.0K, R22 10.0K

VCC_DIG_3V3

R23 DNP, R24 DNP
R25 DNP, R26 DNP

SCK
SDI

UTIL_5V0_A — FB1 600 — VIN_5V

C4 1uF, C5 22uF, C6 47uF, C7 47uF, C8 1uF

VCC_3V3 — FB2 600 — VCC_DIG_3V3

C9 1uF, C10 22uF, C11 47uF, C12 47uF, C13 1uF

D1 LED Green

R30 1.00K

VCC_DIG_3V3

R181 DNP

J3

R28 0.00 SDO
R29 0.00 SDI — 4,6,7
R31 0.00 SCK — 4,6,7

Silkscreen:
Pin 1 position: #1
Pin 2 position: #2

R27 0.00

J4 — CS_8V97003_1
J5 — CS_8V97003_2
J6 — CS_N492

RENESAS

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1140 West Warner Rd.
Tempe, AZ 85284

Title: CLK-104

Size	HW Number:	Engineer:	Rev.
B	987456321587	SZ	A
	Date: 07/16/2024	Sheet: 3 of 11	

Silkscreen: LOCK
Silkscreen: nINT

J7
Headerstrip 1X2 SMD

SYNC_IN
R34 0.00
R33 2.70K
LFV
VDD_QCLKV
VDD_CPV
VDD_SPI
VDD_INP
CS_N492
SCK
N492_MAXOUT
SDI
CLK_1
nCLK_1
CLK_0
nCLK_0
OSC
nOSC

U4
EP

VDD_SPI
EXT_SYS
nCS
SCLK
SELSV
SDAT
nINT
LOCK
VDD_QCLKV
QCLK_V
nQCLK_V
OSC
nOSC
VDD_QCLKV
VDD_CPV
LFV
RES_CAL
CLK_1
nCLK_1
CLK_0
nCLK_0
VDD_INP

VDD_QREFB0
QREF_B0
nQREF_B0
QREF_B1
nQREF_B1
VDD_QREFB1
VDD_QCLKB
QCLK_B0
nQCLK_B0
QCLK_B1
nQCLK_B1
VDD_QCLKB
DNU-13
VDD_QREFC
QREF_C
nQREF_C
VDD_QREFC
DNU-18
VDD_QCLKC
QCLK_C
nQCLK_C
VDD_ QCLKC

VDD_QREFA2
QREF_A2
nQREF_A2
VDD_QCLKA
QCLK_A1
nQCLK_A1
QCLK_A0
nQCLK_A0
VDD_QREFA1
QREF_A1
nQREF_A1
QREF_A0
nQREF_A0
VDD_QREFA0
VDD_QCLKE
QCLK_E1
nQCLK_E1
QCLK_E0
nQCLK_E0
VDD_QCLKE

DNU-23
QREF_D
nQREF_D
VDD_QREFD
QCLK_D
nQCLK_D
VDD_QCLKD
VDD_SYNC
VDD_LCV1
DNU_32
CBIAS
VDD_LCV2
CR
CLD0
LFFR
LFF
VDD_LCF-39
VDD_LCF-40
NC-41
NC 42
VDD_CPF
ICPF

8V19N491-24

QCLK_D
nQCLK_D
VDD_QREFD
VDD_QCLKD
VDD_SYNC
VDD_LCV

C46 4.7uF
C47 10uF
C48 4.7uF
R43 1.00
VDD_CPF
VDD_LCF
R44 DNP
R45 100
C49 33pF
C50 0.1uF

Layout note: Place these RC close to the U4 pins
R39 33.0K
C14 0.027uF
C16 1uF

VDD_VCXO
J8
R32 1.00K
Layout note: Place these RC close to the U3 pin 1
R36 5.10K
C15 2700pF

U3
Cont Volt
E/D
GND
VCC
Comp Output
OUT
CVPD-037X-153.6
VCXO_VC
VCXO_OE
VCXO_Q_N
VCXO_Q_P

R37 0.00
R38 100
R40 0.00
R41 150
R42 150
nOSC
OSC
Place the 100-ohm resistor close to Receiver pins

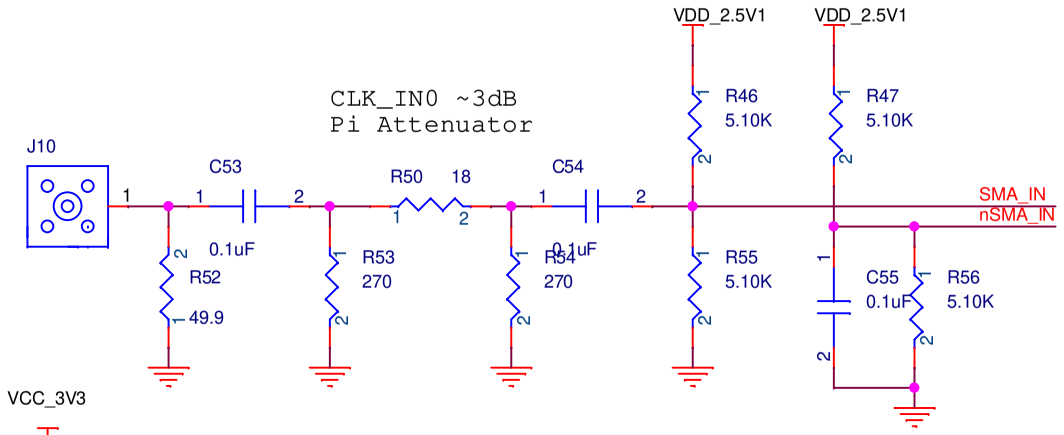
VDD_INP C17 0.1uF
VDD_SPI C18 0.1uF
VDD_LCF C19 1uF
VDD_CPF C20 0.1uF C21 0.1uF
VDD_LCV C22 0.1uF C23 100pF
VDD_SYNC C24 0.1uF
VDD_CPV C25 0.1uF
VDD_VCXO C26 0.1uF

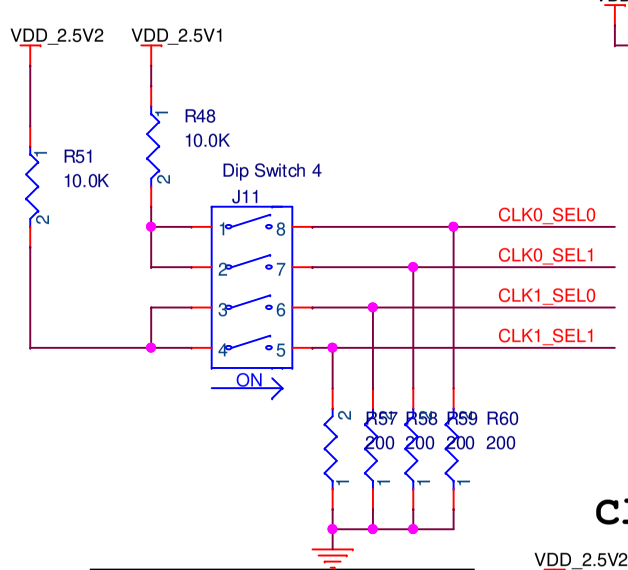
VDD_QCLKA C27 1uF C28 0.1uF
VDD_QCLKB C29 0.1uF
VDD_QCLKC C30 0.1uF
VDD_QCLKD C31 0.1uF
VDD_QCLKE C32 0.1uF
VDD_QCLKV C33 0.1uF C34 0.01uF C35 100pF

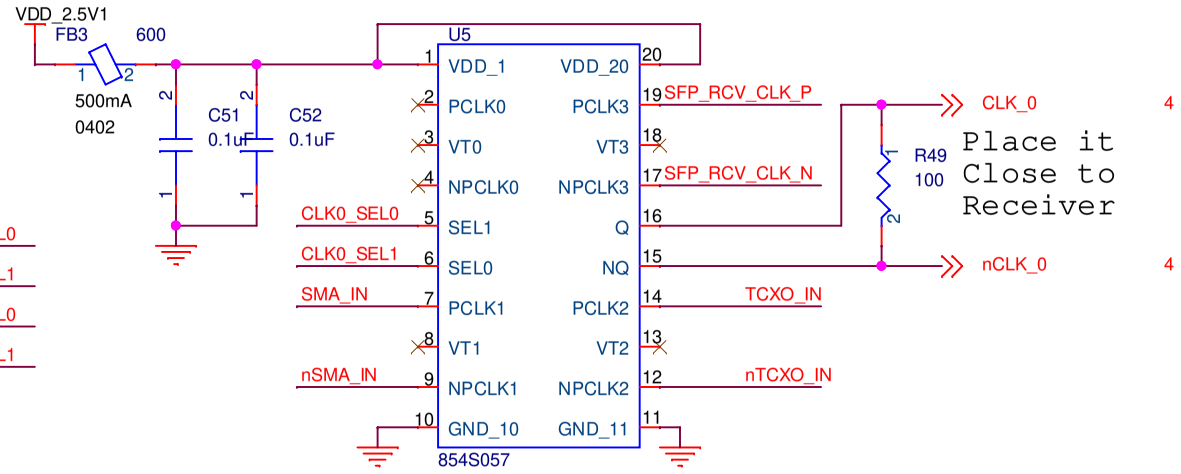
VDD_QREFA0 C36 0.1uF C37 0.01uF
VDD_QREFA1 C38 0.1uF
VDD_QREFA2 C39 0.1uF
VDD_QREFB0 C40 0.1uF C41 0.01uF
VDD_QREFB1 C42 0.1uF
VDD_QREFC C43 0.1uF C44 0.01uF
VDD_QREFD C45 0.1uF

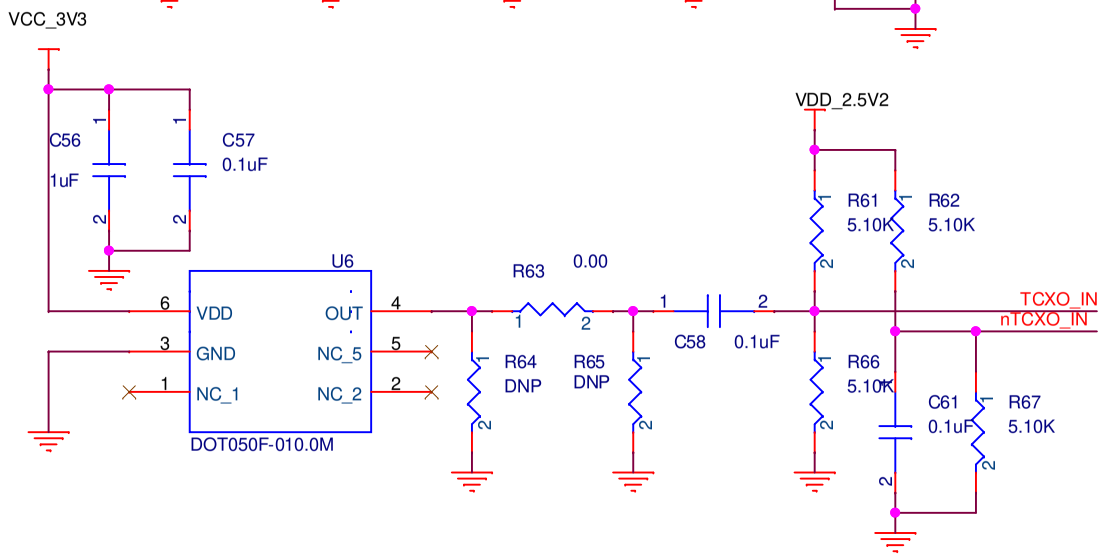
RENESAS
Renesas
1140 West Warner Rd.
Tempe, AZ 85284

Title: CLK-104
Size: B
HW Number: 987456321587
Engineer: SZ
Rev.: A
Date: 07/16/2024
Sheet: 4 of 11

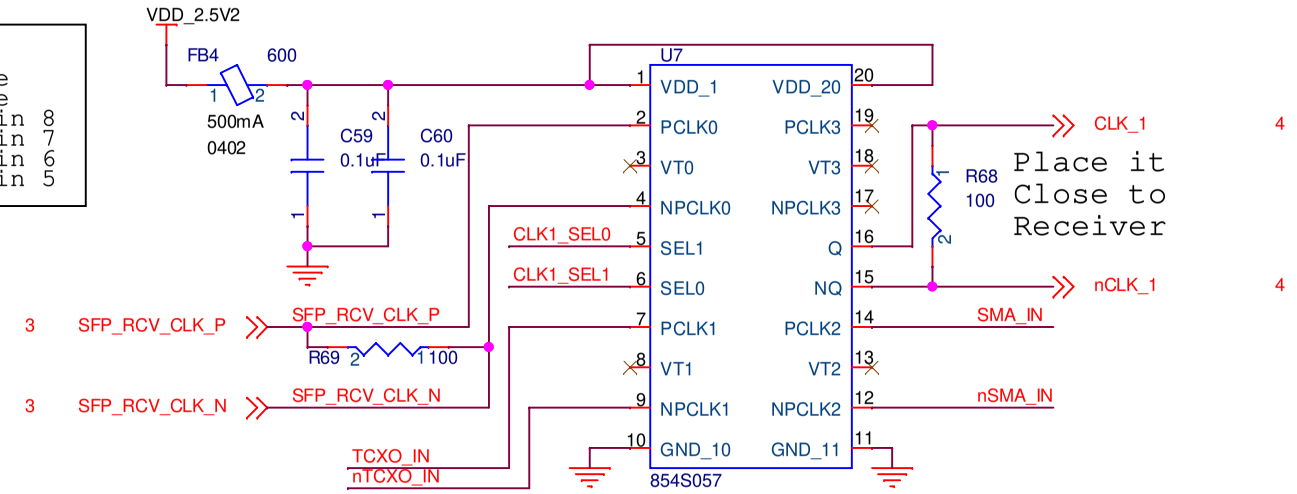




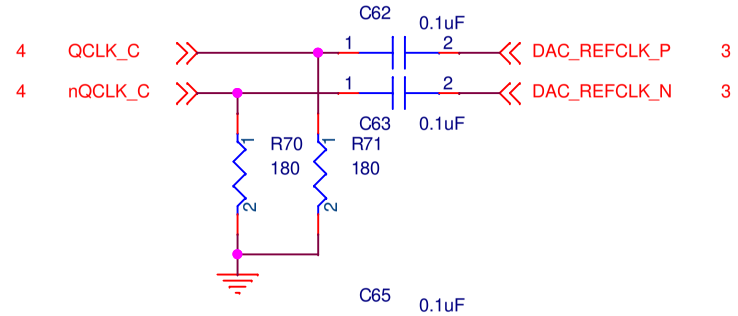


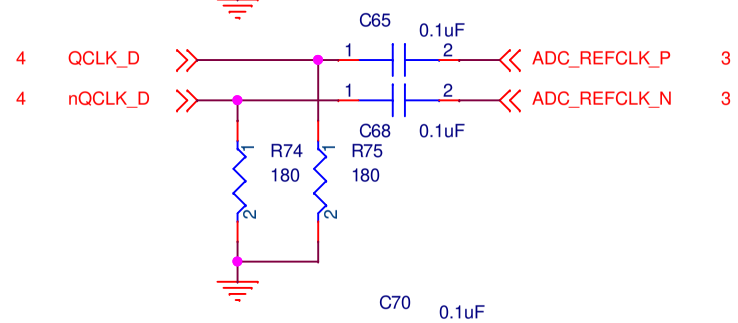


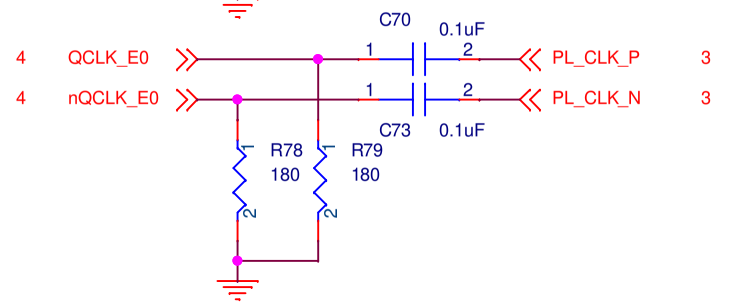
Clam-shell placement for the two MUX devices

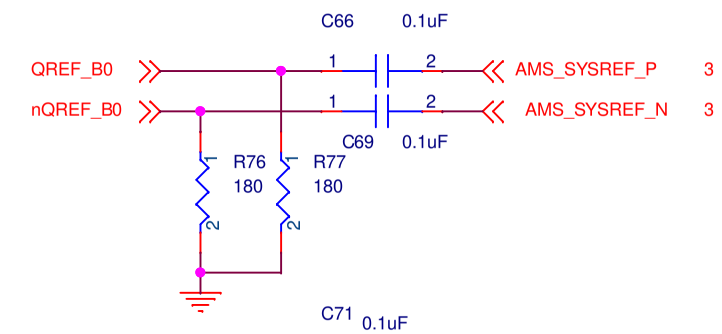


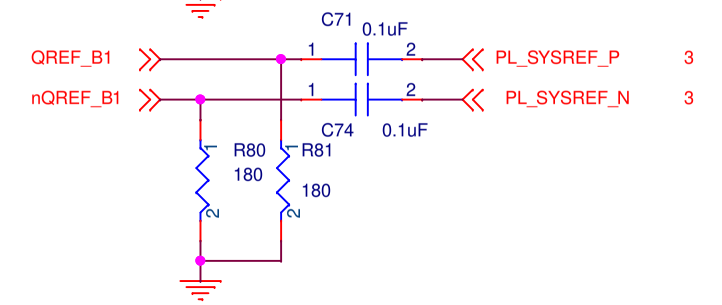
Silkscreen:
"H" at pin 1 side
"L" at pin 8 side
"CLK0_SEL0" at pin 8
"CLK0_SEL1" at pin 7
"CLK1_SEL0" at pin 6
"CLK1_SEL1" at pin 5

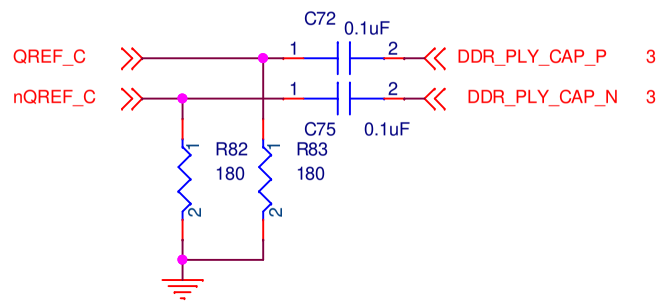




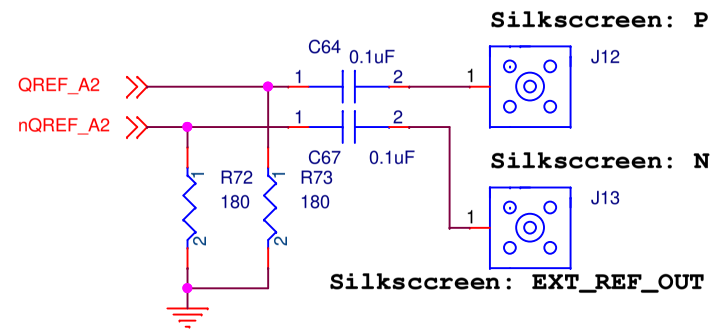








These 6 differential outputs (left and below) going to J1



Renesas
1140 West Warner Rd.
Tempe, AZ 85284

Title: CLK-104			
Size: B	HW Number: 987456321587	Engineer: SZ	Rev: A
	Date: 07/16/2024	Sheet: 5 of 11	

Silkscreen:
RF1_OUTB_P

J14
TM14-0084-00
C77 100pF
R84 49.9
R87 49.9
VDD_OUTB_1
L2 15nH
C80 0.01uF

Silkscreen:
RF1_OUTB_N

J17
TM14-0084-00
C83 100pF

C76 100pF
J15
TM14-0084-00
Silkscreen:
RF1_OUTA_P
R85 49.9
R86 49.9
VDD_OUTA_1
L1 15nH
C79 0.01uF
C82 100pF
J16
TM14-0084-00
Silkscreen:
RF1_OUTA_N

VDD_OUTB_1
C78 0.01uF
C81 0.1uF
VDD_VCO_1
C84 0.1uF
C85 0.01uF
VDD_OUTA_1
C86 0.1uF
C87 0.01uF
VDD_VCO_1
C88 0.1uF
C89 0.01uF
nRST_1
C242 0.1uF
R179 10.0K
VDD_DIG_1

pin42_1
pin43_1

U8
8V97003
EP
1 VREFVCO2
2 NC_2
3 VDDVCO2
4 VREGVCO2
5 VTUNE
6 RESERVED
7 MUTE
8 LD
9 NC_9
10 CPOUT
11 CPBIAS
12 VDDPDCP
13 VREGPDCP
14 VSSPDCP
15 VDDFB
16 VREGFB
17 VSSFB
18 VDDDIG
19 VSSDIG
20 VSSIN
21 VREGIN
22 REF_IN
23 NREF_IN
24 VDDIN
37 VSSOUTA_38
38 VDDOUTA
39 NRF_OUTA
40 RF_OUTA
41 VSSOUTA_41
42 VBIASOUTA
43 VBIASOUTB
44 VSSOUTB_44
45 RF_OUTB
46 NRF_OUTB
47 VSSOUTB_47
48 VDDOUTB
EP
NC_36 36
35 VREFVCO1
NC_34 34
33 VDDVCO1
32 VREGVCO1
31 NRESET
30 SYNC
29 CE
28 SDIO
27 SDO
26 SCLK
25 CSB

D2 LED Green
R91 20
C92 680pF
C93 2200pF
R94 62
C97 0.047uF
C94 22uF
C103 22uF
C105 22uF
C95 22uF
C96 22uF
R96 2.20K
R97 1.00K

nRST_1
R89 42.2
R88 2.20K
R90 2.20K
R92 0.00
R93 2.20K
R95 2.20K
VDD_DIG_1
SDI 3,4,7
8V97003_MAXOUT1 3
SCK 3,4,7
CS_8V97003_1 3
C91 22uF 35V
C90 22uF 35V

VDD_INPDFB_1
U9
83026I-01
VDD 8
NC_1 1
Q0 7
CLK 2
Q1 6
NCLK 3
GND 5
OE 4
SYNC_2 7
QREF_A0 4
nQREF_A0 4
QCLK_A0 4
nQCLK_A0 4
R98 82.0
R99 82.0
C99 0.1uF
C100 0.1uF
R105 130
R106 130
R107 180
R104 180
R100 49.9
R101 49.9
R102 2.20K
R103 49.9
0201

C98 0.1uF
C101 0.1uF
C102 0.1uF
C104 0.1uF

THe following Power/Ground pin-pairs are connected through a 0.1uF capacitor in a shortest trace through a via to the ground plane:

1. Pin 3, EPAD
2. Pin 12, Pin 14
3. Pin 15, Pin 17
4. Pin 18, Pin 19
5. Pin 24, Pin 20
6. Pin 33, EPAD
7. Pin 37, Pin 38, 41
8. Pin 48, Pin 44, 47

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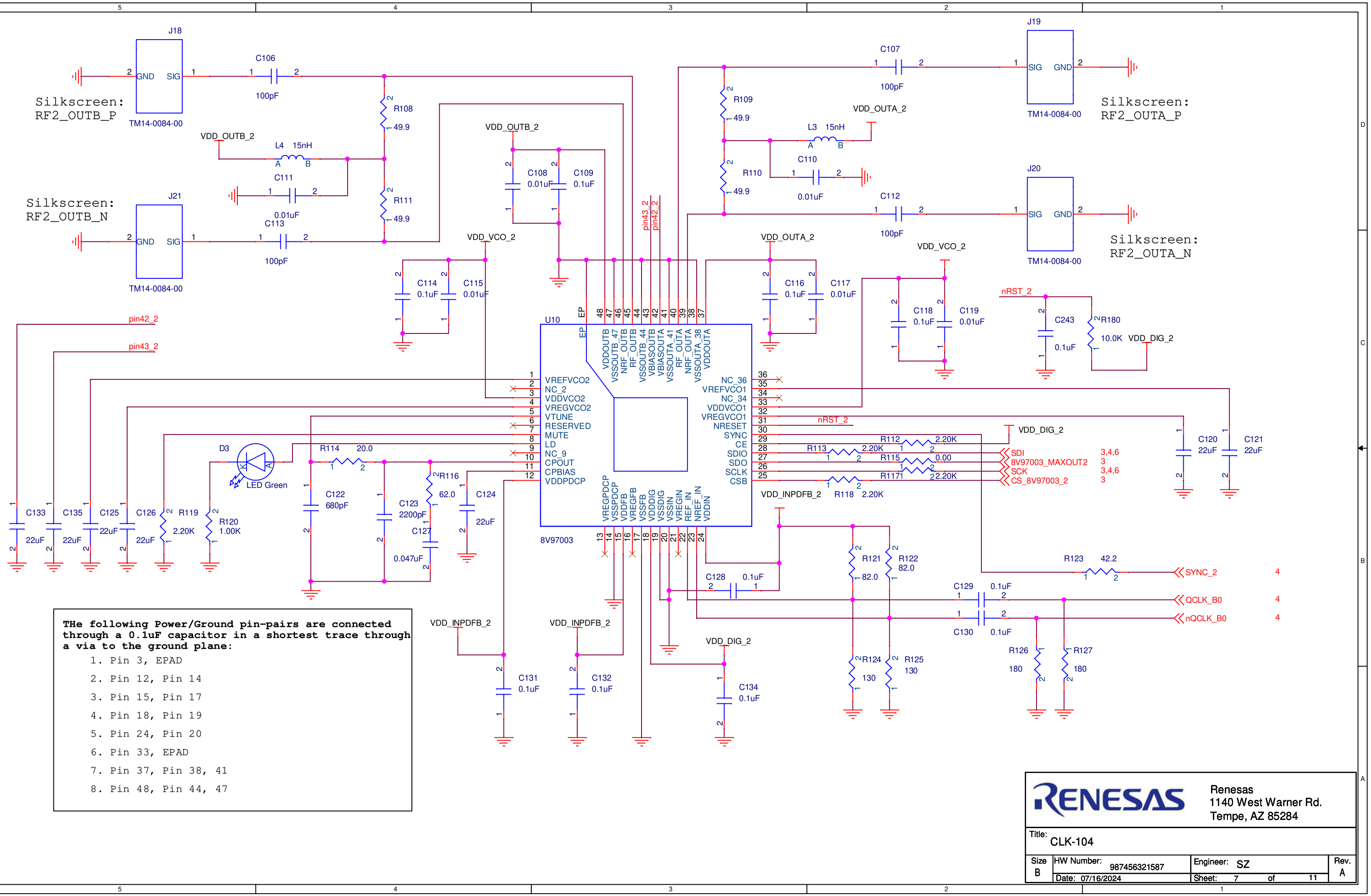

THe following Power/Ground pin-pairs are connected through a 0.1uF capacitor in a shortest trace through a via to the ground plane:

1. Pin 3, EPAD
2. Pin 12, Pin 14
3. Pin 15, Pin 17
4. Pin 18, Pin 19
5. Pin 24, Pin 20
6. Pin 33, EPAD
7. Pin 37, Pin 38, 41
8. Pin 48, Pin 44, 47

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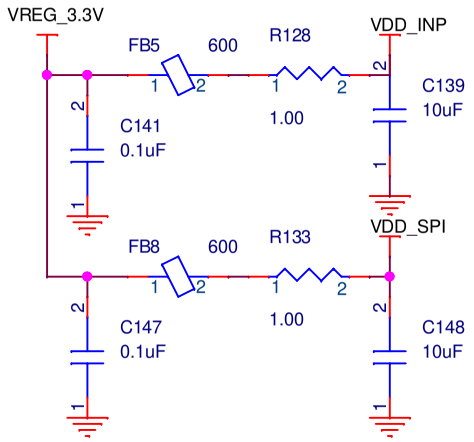

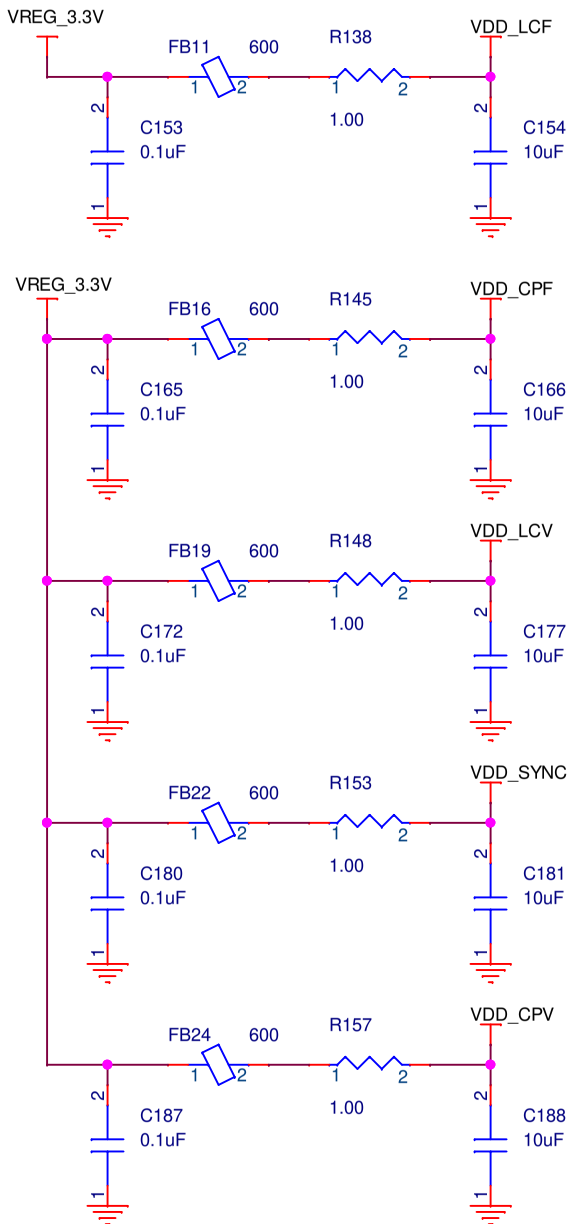

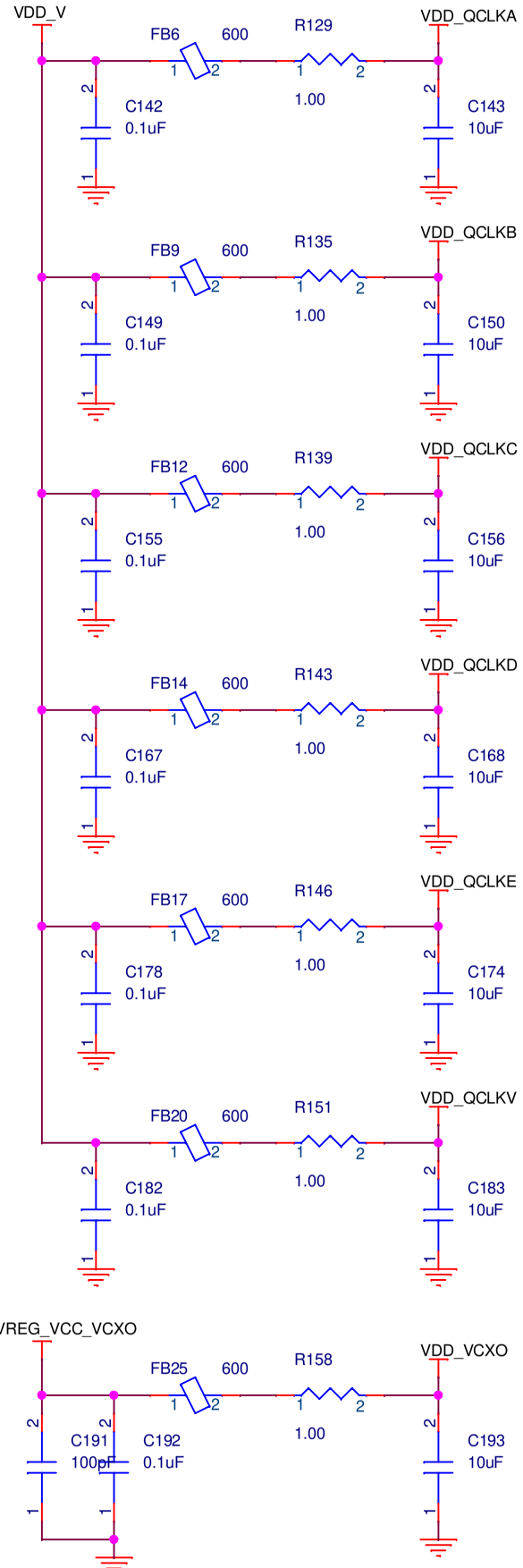

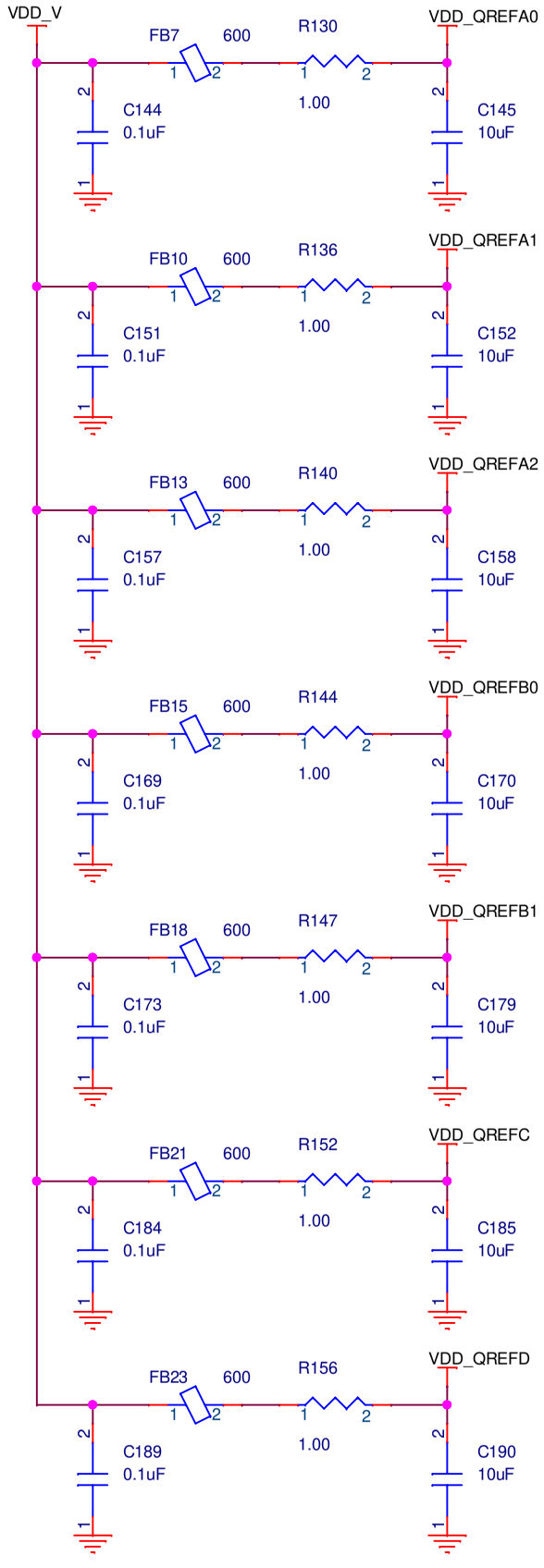

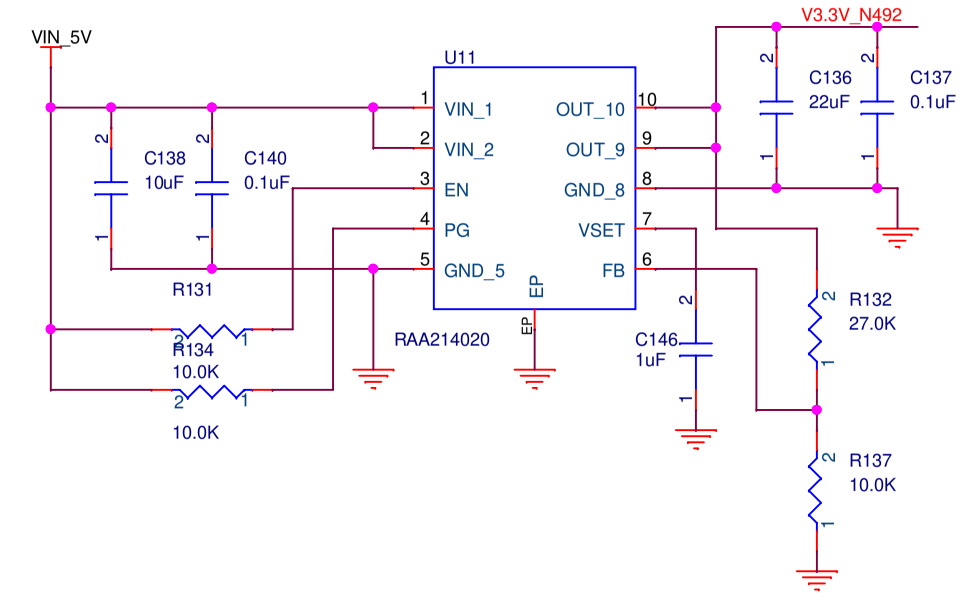

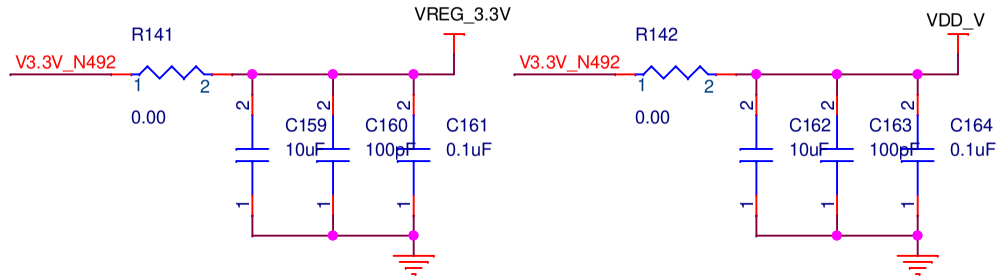

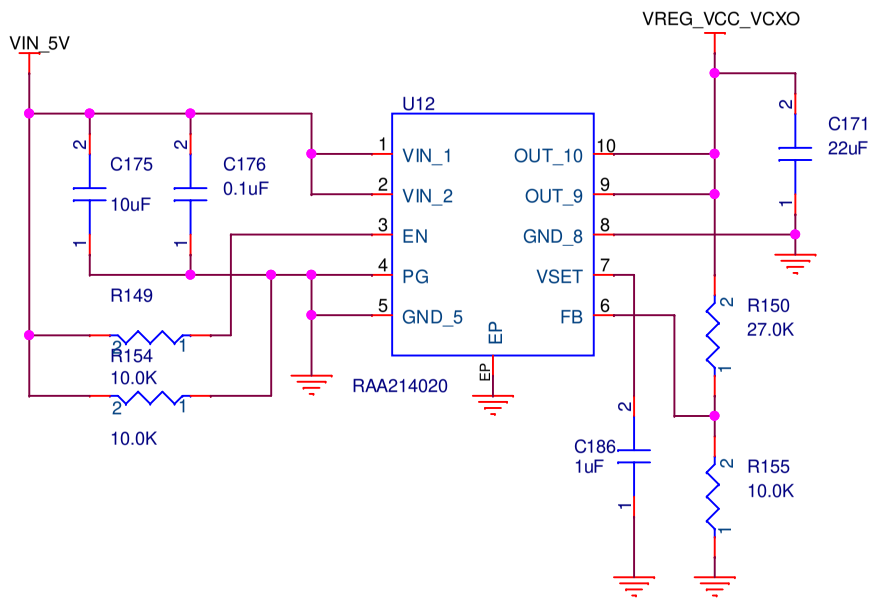

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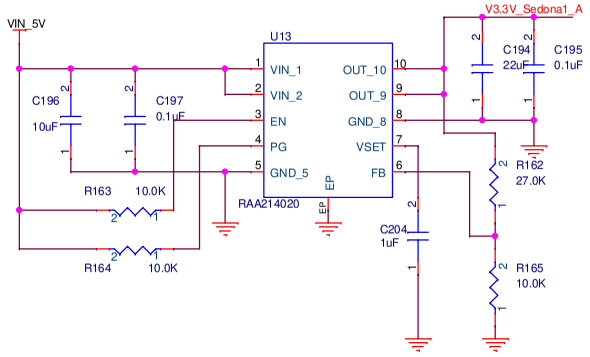
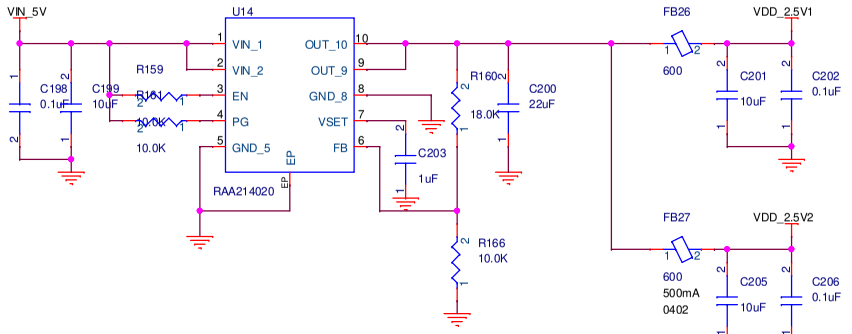
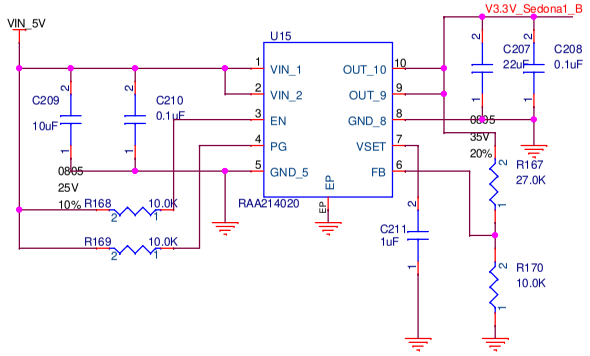
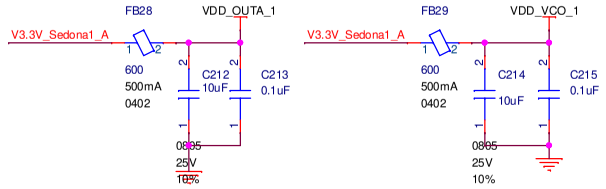
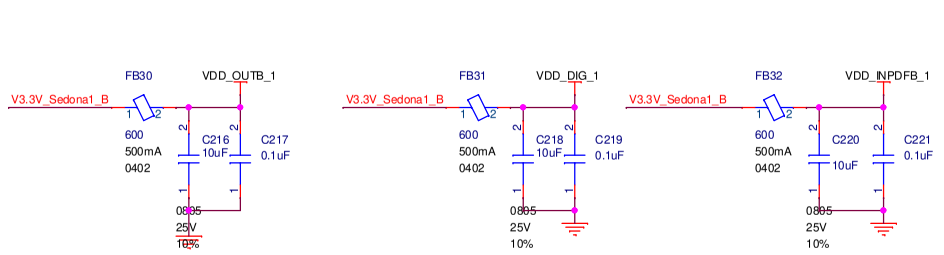


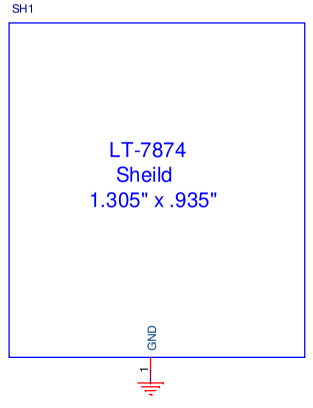








SH1 covers U8, U13, U15 and its filtering circuits



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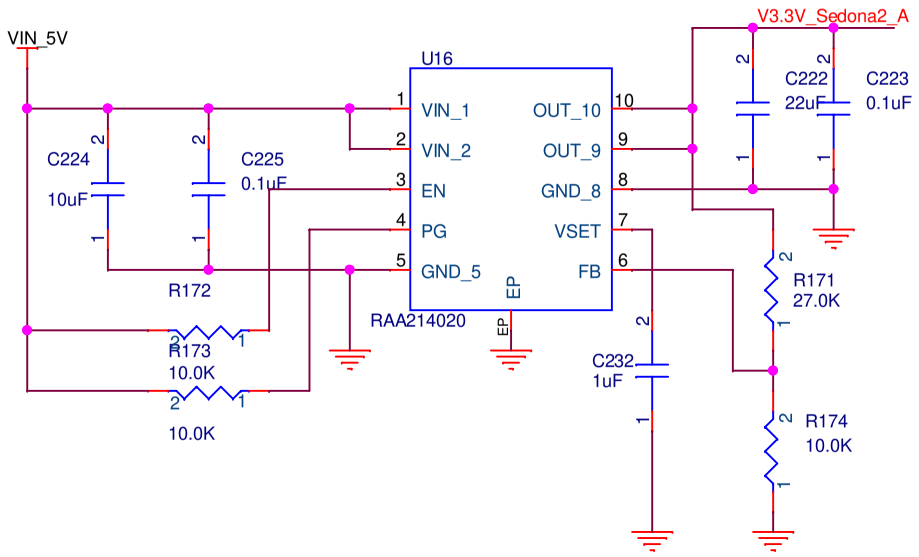
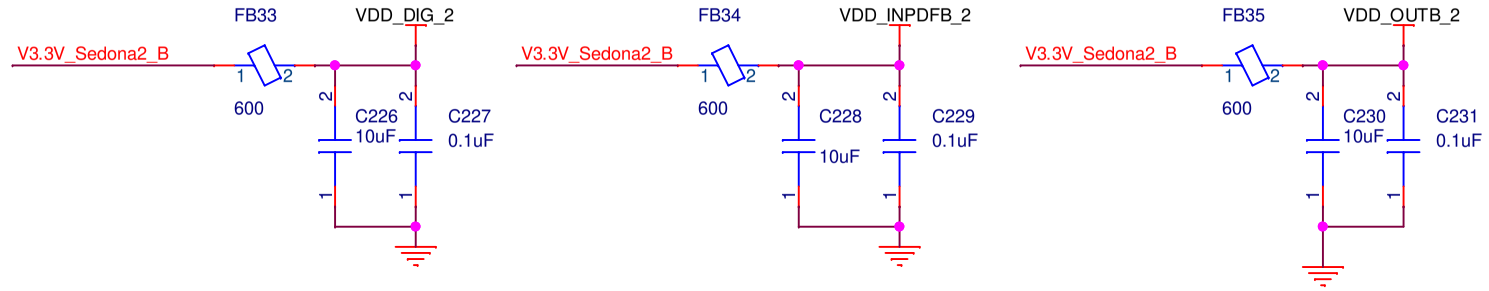
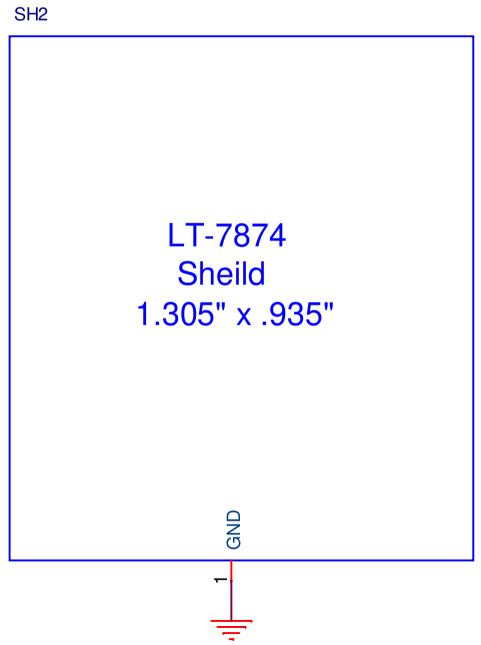
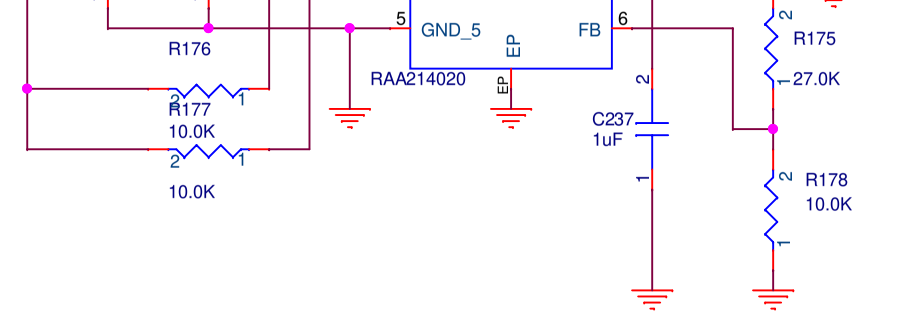
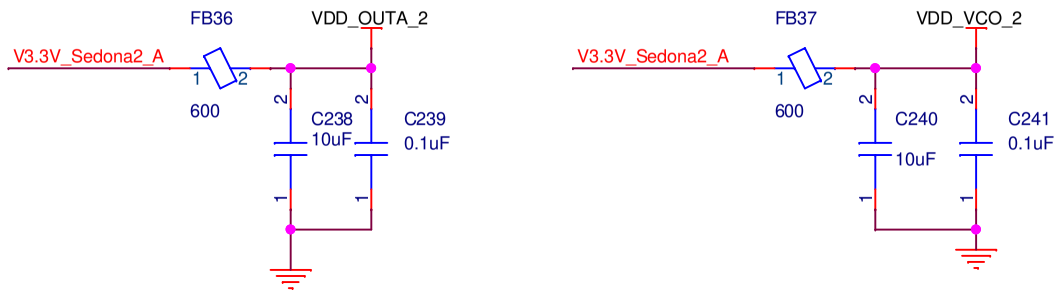




SH2 covers U10, U16, U17 and its filtering circuits







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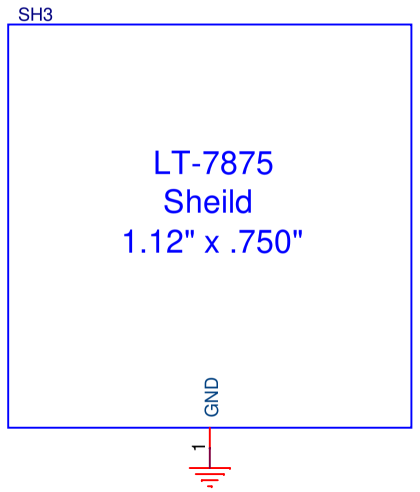
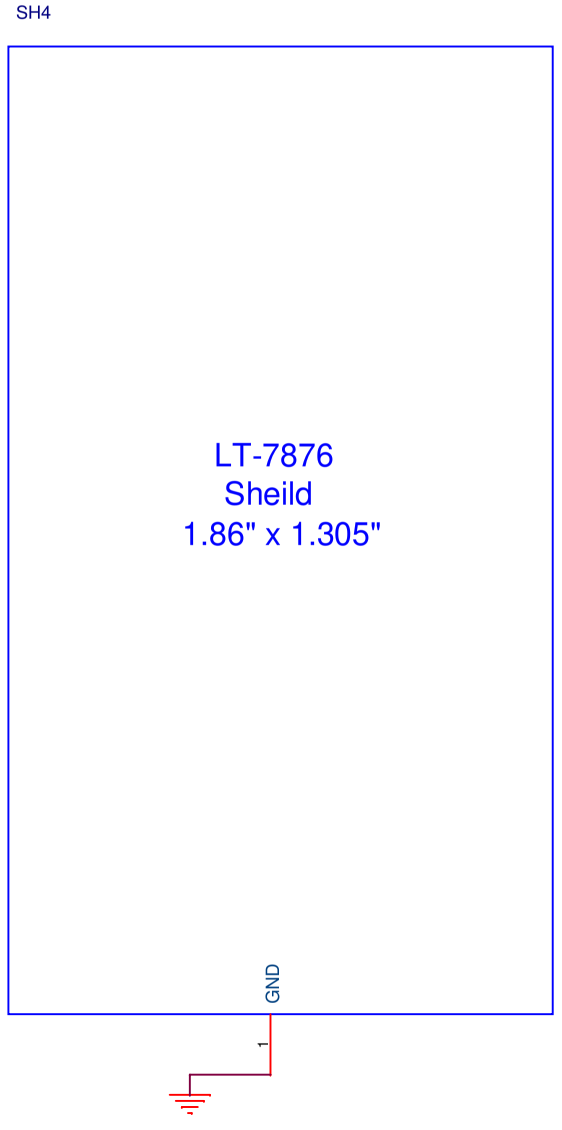
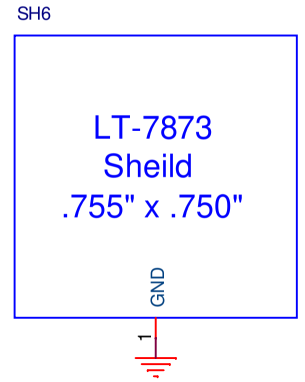
SH3 covers U3, and U12 and its surrounding cmoponents and circuits



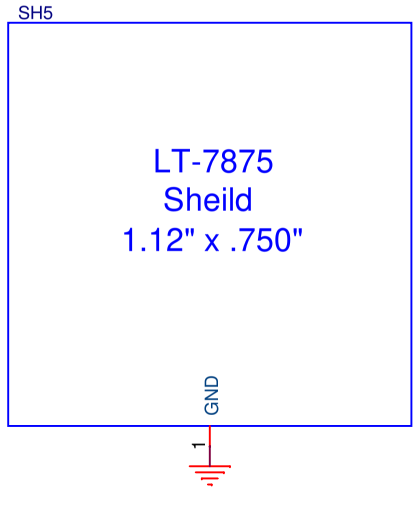
SH4 covers U4, U11 and its respective surrounding circuits



SH6 covers U1 its surrounding cmoponents and circuits



SH5 covers U6 its surrounding cmoponents and circuits



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