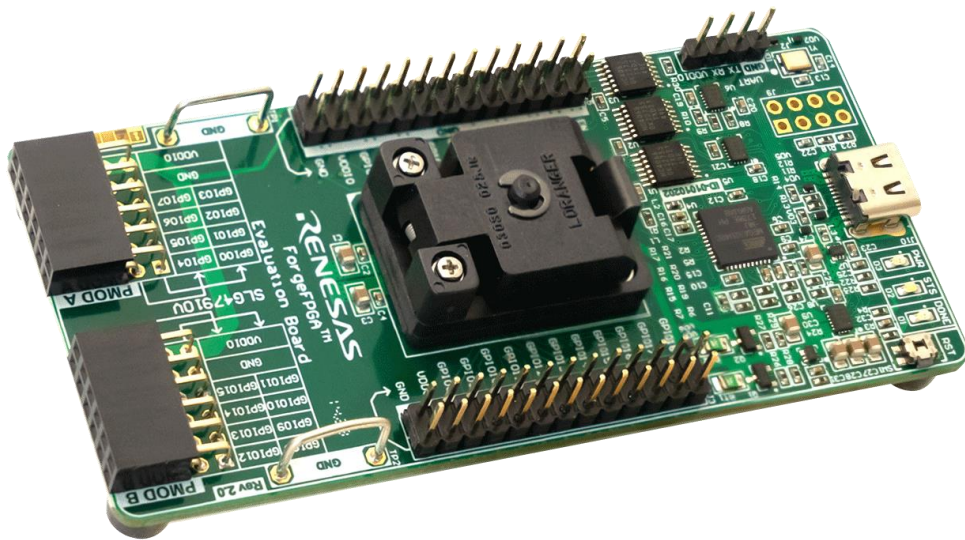


# User Manual



## ForgeFPGA™ Evaluation Board R2.0

## Contents

<b>1. Functional Description</b>	<b>4</b>
<b>2. Interaction Connectors and Specifications</b>	<b>5</b>
2.1 GPIO and PMOD Connectors	5
2.2 Power	6
2.3 UART Interface	7
<b>3. Working with ForgeFPGA Products</b>	<b>8</b>
<b>4. Additional Features</b>	<b>9</b>
4.1 Status Display and Controls	9
4.2 Firmware Update and RST Button	9
4.3 Initialization Error	9
<b>5. Board Schematic</b>	<b>11</b>
<b>6. Bill Of Materials</b>	<b>13</b>
<b>7. Ordering Information</b>	<b>14</b>
<b>8. Revision History</b>	<b>15</b>

## Figures

Figure 1. ForgeFPGA Evaluation Board R2.0	3
Figure 2. ForgeFPGA Evaluation Board R2.0 Overview	4
Figure 3. Board Structure	5
Figure 4. GPIO Connector Pinout	5
Figure 5. PMOD Connector Pinout	6
Figure 6. UART Connector Pinout	7
Figure 7. Debugging Setup for Socket Adapters	8
Figure 8. Indication	9
Figure 9. Reset Button	9

## ForgeFPGA Evaluation Board R2.0

ForgeFPGA Evaluation board is a compact, easy to use, USB powered hardware tool that provides SLG47910V IC hardware support for design emulation, programming, and real time testing. Evaluation board is controlled by Go Configure Hub software with emulation, VDDC/VDDIO regulation, IC programming and internal UART terminal options.

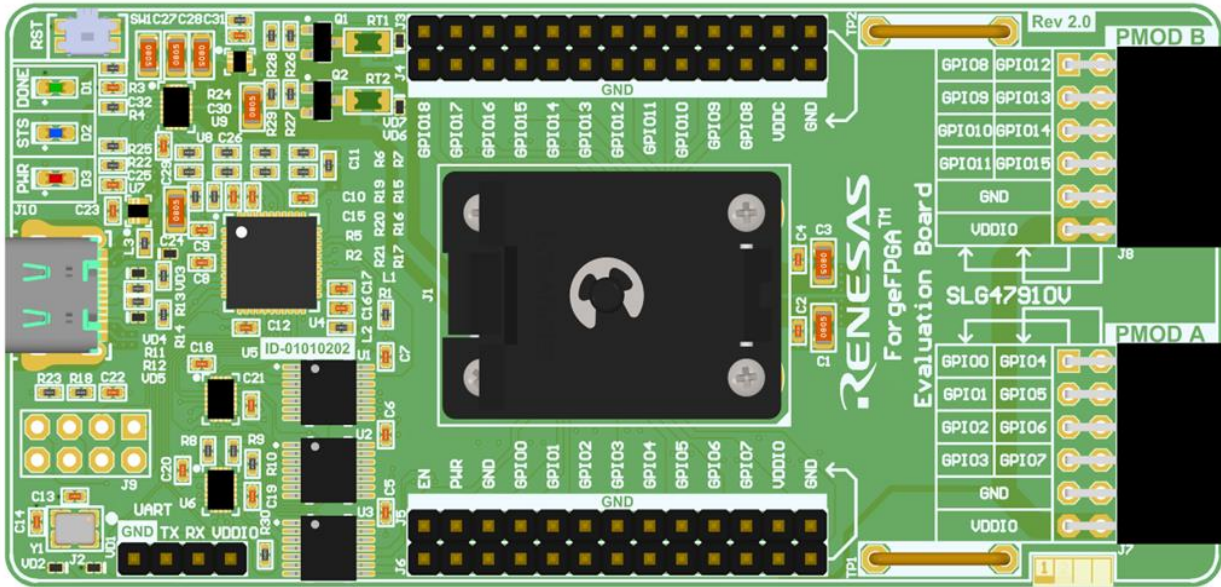


Figure 1. ForgeFPGA Evaluation Board R2.0

## Features

Driven by the Go Configure Software Hub, the ForgeFPGA Evaluation Board is configured to work with basic FPGA designs and provide such features:

- Configurable VDD and VDDIO Power Sources
- Zero-Force 24-pin Socket
- Emulation and programming options
- PMOD connectors
- UART Terminal Interface

# 1. Functional Description

The main components are shown in Figure 2.

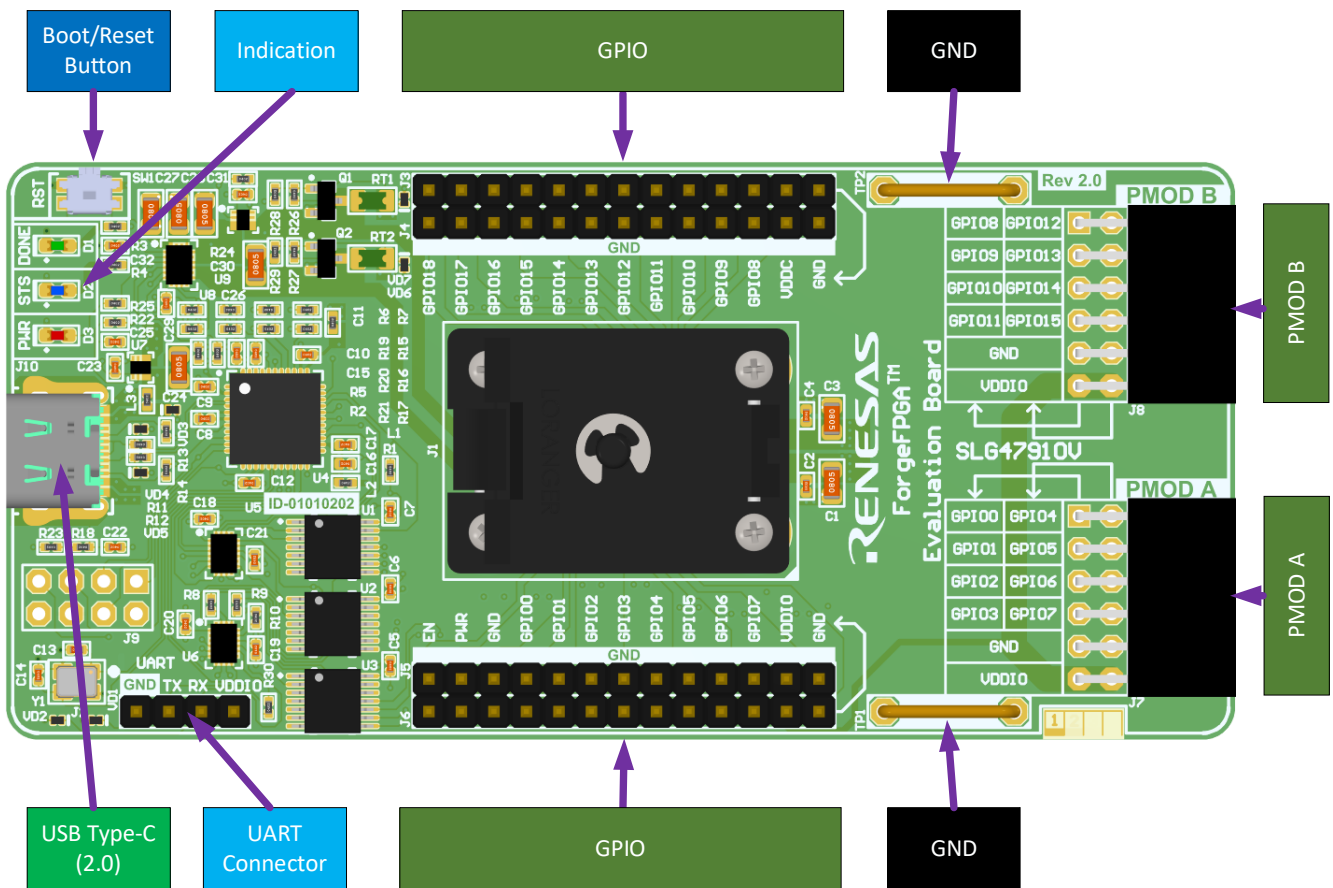


Figure 2. ForgeFPGA Evaluation Board R2.0 Overview

ForgeFPGA Evaluation Board provides support for basic FPGA operations for ForgeFPGA devices. By using this board, it is possible to emulate, test and program custom FPGA designs. This evaluation board can also be used for small quantity sample programming. User can access the ForgeFPGA GPIO provided by external connectors “J3” and “J6”. Almost all pins from Socket are also duplicated on PMOD connectors.

Table 1 shows general USB characteristics that are required for Evaluation Board stable functionality.

Table 1. General Specifications

Parameter	Description	Condition	Min	Typ	Max	Unit
V <sub>USB</sub>	USB Input Voltage	-	4.75	-	5.25	V
I <sub>USB</sub>	USB Input Current	-	-	-	500	mA
T <sub>A</sub>	Operating Ambient Temperature	-	10	-	45	°C
-	Board Dimensions	-	143 x 65			mm
-	Weight	-	35			g

ForgeFPGA Evaluation Board consists of 2 main blocks – Program Interface and Socket with external connectors. This evaluation board uses USB 2.0 Type-C connector for communications and power. Board dimensions are 143mm x 65mm.

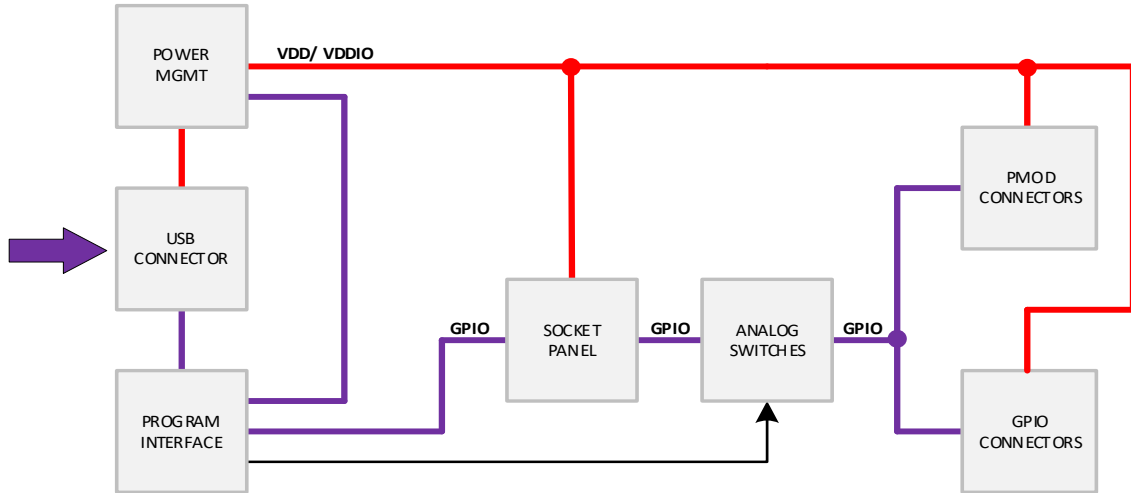


Figure 3. Board Structure

Analog switches are used to isolate external connections in programming or emulation sequences. When emulation entry is done, analog switches connect GPIO back to both GPIO and PMOD connectors and the programming interface sets all output states to Hi-Z.

## 2. Interaction Connectors and Specifications

### 2.1 GPIO and PMOD Connectors

All 24 pins of SLG47910V are distributed within GPIO, PMOD and Zero-Force socket connectors. Analog switches and programming interface add additional parasitic parameter to SLG47910V GPIOs. Table 2 shows GPIO characteristics including analog switches parameters.

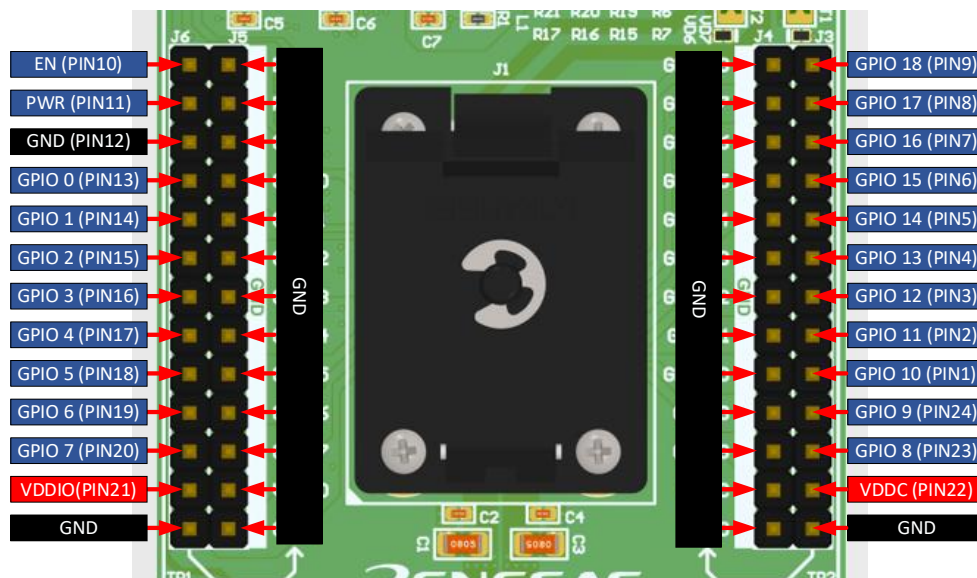


Figure 4. GPIO Connector Pinout

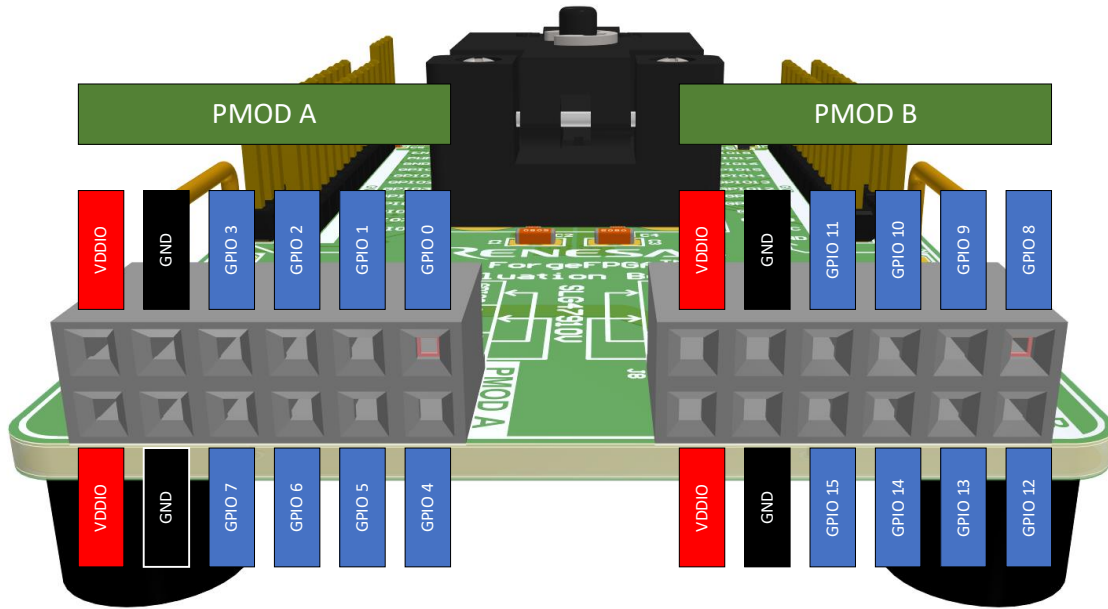


Figure 5. PMOD Connector Pinout

Table 2. GPIO and PMOD Connector characteristics

Parameter	Description	Condition	Min	Typ	Max	Unit
$I_L$	Input leakage current	-	-	2	-	$\mu\text{A}$
$C_{IO}$	Input-Output Pin Capacitance	-	-	7	-	$\text{pF}$
$R_{ON}$	Series Resistance	-	-	25	52	$\Omega$
$V_{IN}$	Input Voltage	-	-0.5	-	$V_{DDIO}+0.3$	V

## 2.2 Power

The board has  $V_{DD}$  and  $V_{DDIO}$  programmable power supplies. The maximum available output current is 150mA for each source. The same voltage is supplied to GPIOs, for keeping the logic level compatibility with the circuit under test. If Load current value exceeds  $I_{OUT(MAX)}$ ,  $V_{DD}$  output will go into OCP mode. All  $V_{DDIO}$  and  $V_{DDC}$  terminals on board are working only as output.

Table 3. Voltage Sources Characteristics ( $V_{DD}$ ,  $V_{DDIO}$ )

Parameter	Description	Condition	Min	Typ	Max	Unit
$V_{OUT(VDD)}$	Output Voltage on $V_{DD}$	$I_{OUT(MIN)} \leq I_{OUT} \leq I_{OUT(MAX)}$	1	-	1.2	V
$V_{OUT(VDDIO)}$	Output Voltage on $V_{DDIO}$	$I_{OUT(MIN)} \leq I_{OUT} \leq I_{OUT(MAX)}$	1.8	-	3.6	V
$V_{STEP}$	Output Voltage Regulation Step	$V_{OUT(MIN)} \leq V_{OUT} \leq V_{OUT(MAX)}$	100	-	170	mV
$\Delta V_{OUT}$	Output Voltage DC Error	$I_{OUT(MIN)} \leq I_{OUT} \leq I_{OUT(MAX)}$	-5	-	5	%
$I_{OUT}$	Output Load Current	$V_{OUT(MIN)} \leq V_{OUT} \leq V_{OUT(MAX)}$	0	-	150	mA
$V_{OUT(SR)}$	$V_{OUT}$ Slew Rate	$I_{OUT(MIN)} \leq I_{OUT} \leq I_{OUT(MAX)}$	7	10	13	V/ms
$C_L$	Load Capacitance	-	0	-	100	$\mu\text{F}$

## 2.3 UART Interface

UART terminal option is accessible with a UART Connector. Voltage level on “V<sub>DDIO</sub>”, “TX”, “RX” is equal to V<sub>DDIO</sub> selection voltage in Go Configure Software Hub. Supported baud rates are from 600 to 230400 bit/s.

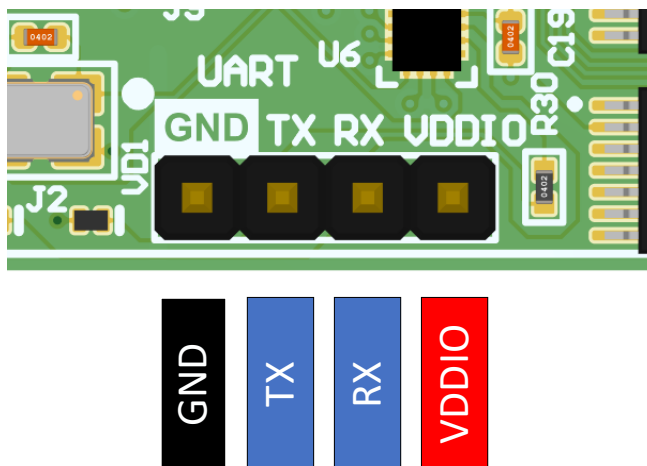


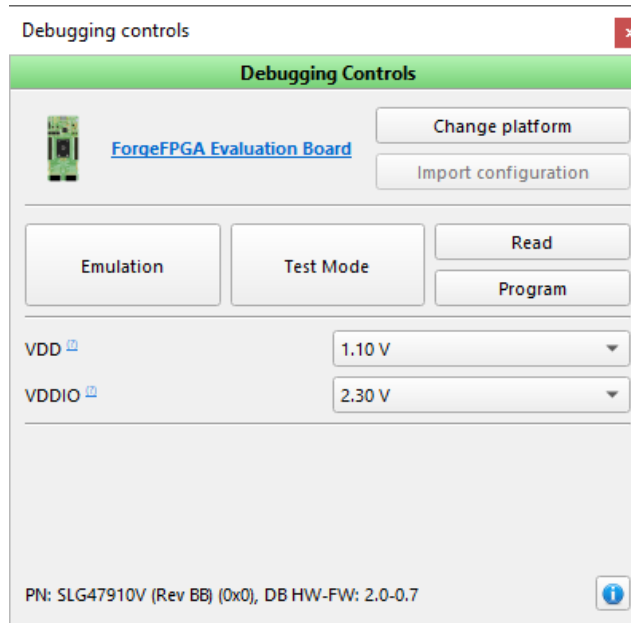
Figure 6. UART Connector Pinout

Table 4. UART Specifications

Symbol	Description	Condition	Min	Typ	Max	Unit
<b>TX:</b>						
V <sub>O</sub>	Output Voltage Level Range	-	1.8	-	3.6	V
V <sub>OH</sub>	Output High Voltage	VDD = 3.6V	3.5	-	-	V
V <sub>OL</sub>	Output Low Voltage	VDD = 3.6V	-	-	0.08	V
I <sub>OH</sub>	Output Current High	VDD = 3.6V	-	-	50	mA
I <sub>OL</sub>	Output Current Low	VDD = 3.6V	-	-	50	mA
<b>RX:</b>						
V <sub>I</sub>	Input Voltage Level Range	-	- 0.2	-	V <sub>DDIO</sub> + 0.2	V
V <sub>IH</sub>	Input High Voltage	-	0.7 x V <sub>DDIO</sub>	-	-	V
V <sub>IL</sub>	Input Low Voltage	-	-	-	0.3 x V <sub>DDIO</sub>	V
I <sub>I</sub>	Input Leakage Current	-	-	-	2	μA
C <sub>IN</sub>	Input capacitance	-	-	20	-	pF
-	Baud Rate	-	600	-	230400	bit/s

### 3. Working with ForgeFPGA Products

To start working with the FPGA products, connect the platform to the PC via a USB Type-C cable and connect the power supply. Important note, that USB cable should be connected directly to PC without any USB hubs and Docking stations. If all the connections are correct, then the red LED (PWR) will be automatically enabled. After Selecting “ForgeFPGA Evaluation Board” in Go Configure “Debug” tab – blue LED will blink several times and “HW-FW” version will be available in left bottom corner of debugging control window (Figure 7).



**Figure 7. Debugging Setup for Socket Adapters**

“Emulation” allows to debug the current project, it will only work after performing synthesis in FPGA Editor, “Test Mode” lets the user debug the programmed project. “Read” button lets the user read the programmed chip configuration and opens the project in the new software instance or in the “Project data” window of the current instance. “Program” button programs the chip with the current project. “TP Map” shows the test point map on the work area, reflecting the physical Test Points on the development platform.

The more detailed information about Go Configure software can be found in “ForgeFPGA Software User Guide.”



## 4. Additional Features

### 4.1 Status Display and Controls

There are three onboard LEDs whose functions are described in table below:



Figure 8. Indication

Table 5. LED Indication

PWR	STS	DONE	
OFF	X	X	USB in not connected / power fail / self test fail
ON	OFF	X	Standby mode
ON	BLINK	X	USB data transfer
ON	X	ON	ForgeFPGA configuration done

### 4.2 Firmware Update and RST Button

Firmware update will be performed automatically while ForgeFPGA Evaluation Board is connected to the PC with Go Configure Software Hub opened. If “RST” button pressed and released in interval less than 2s -board will perform hardware reset and disappear from USB device tree for 500us.

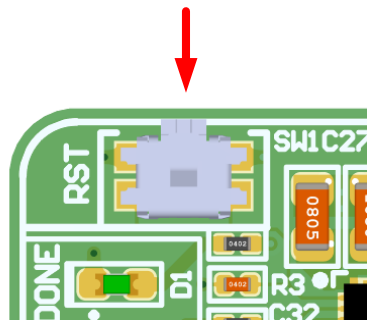
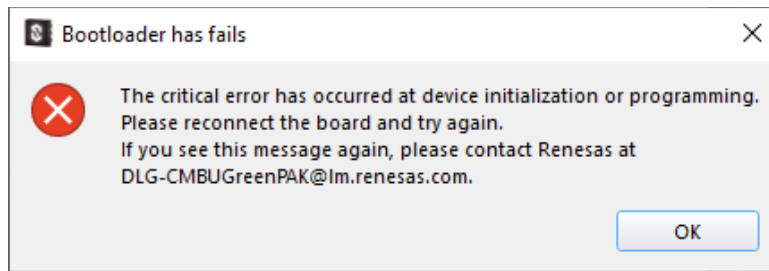


Figure 9. Reset Button

If button (SW1) pressed in interval with more than 2s duration then, the board performs BOOT sequence. Boot option from button is required in case the board is disconnected from USB while firmware update.

### 4.3 Initialization Error

When connecting the Evaluation Board to the software, it might display an error message as it is unable to initialize the board. You will see that the blue LED flashes briefly and then it disappears. This means there is an initialization error. The message displayed resembles this (see below)



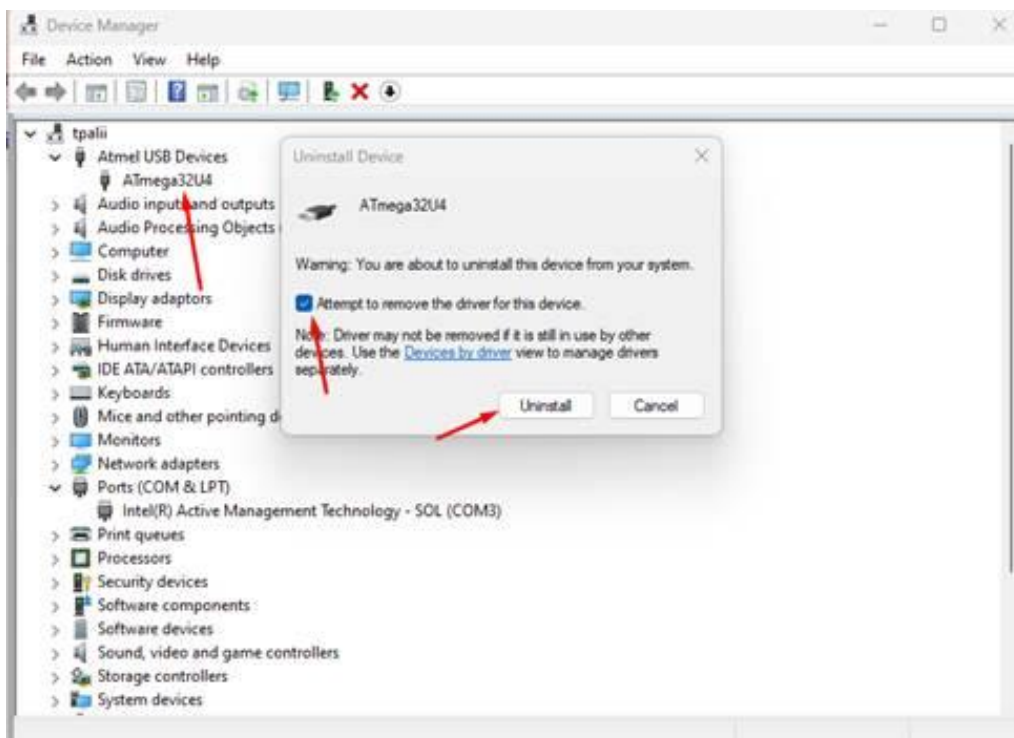
### **Solution:**

This is due to a missing or incorrect device driver. We have found that installing the latest Atmel driver for different devices would cause a conflict.

Typically, during the installation, the software avoids forcefully replacing any existing drivers in the user's system. If a different driver version had been installed before, our devices might be inoperable.

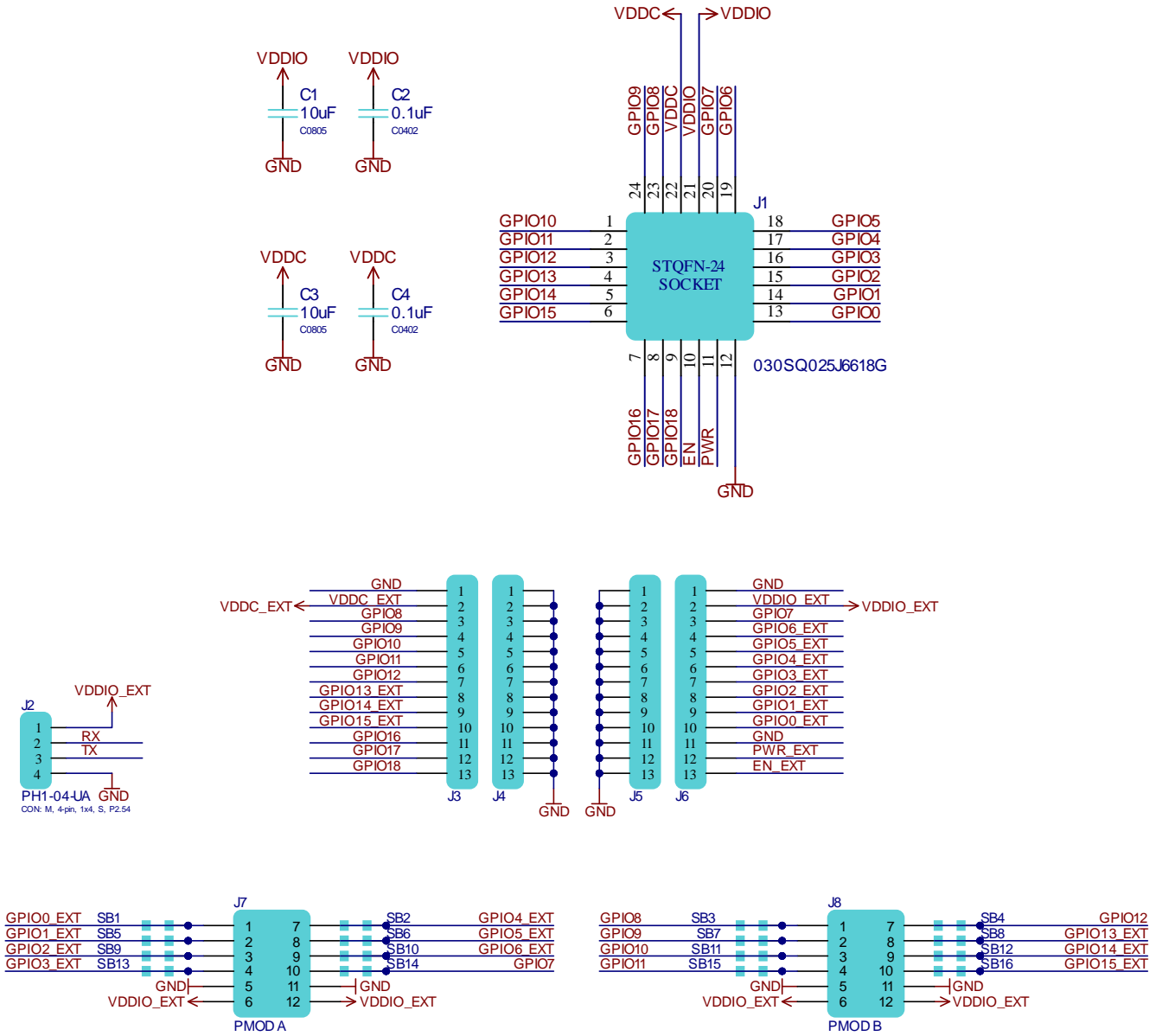
To fix the issue, a user must uninstall the conflicting driver and rerun our driver installation package.

1. Open Go Configure software -> press Debug -> select ForgeFPGA Evaluation Board.
2. Hold the 'RST' button on the board pressed for 5 seconds.
3. Open the Device Manager, find the 'ATm32U4DFU' or 'ATmega32U4' device, and uninstall the driver. If multiple driver versions were installed previously, this action might need to be done several times. Make sure the driver is removed.

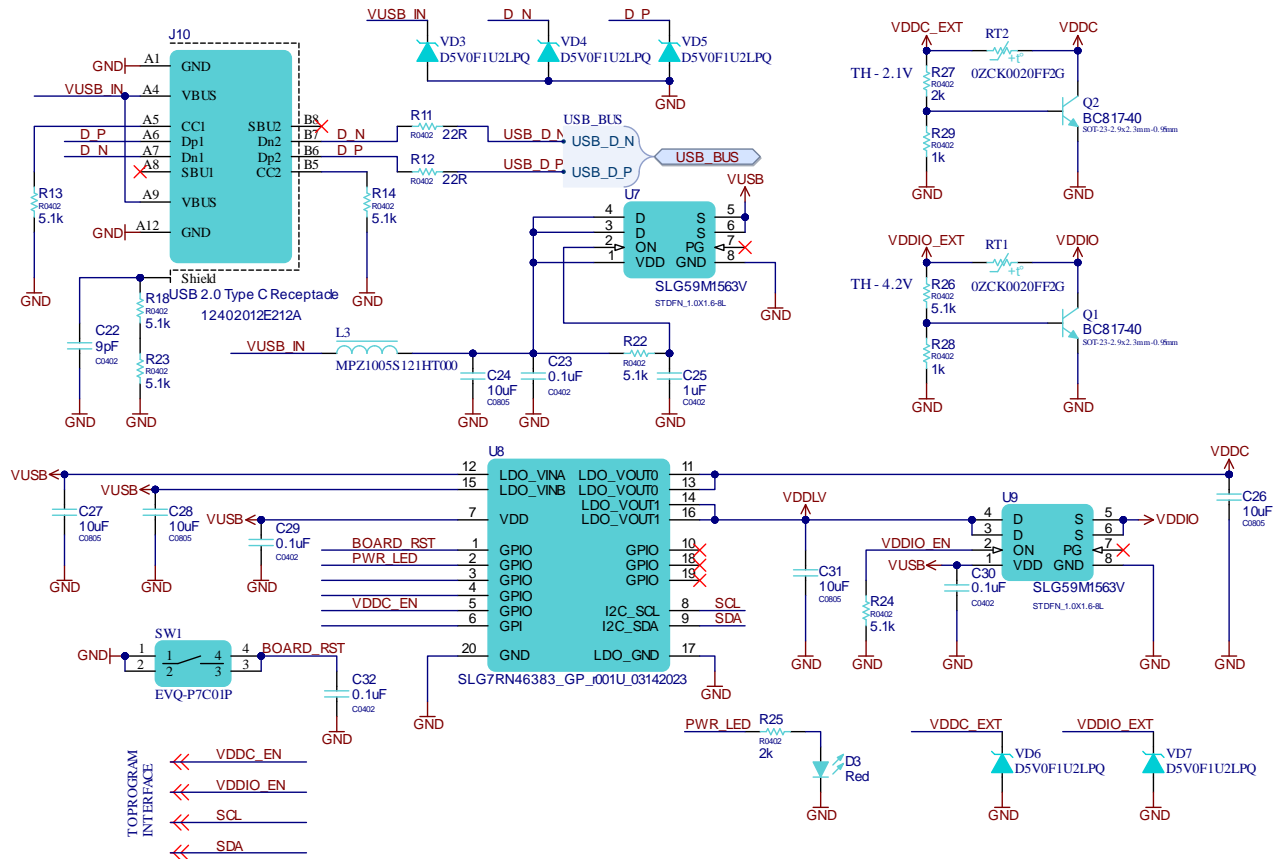
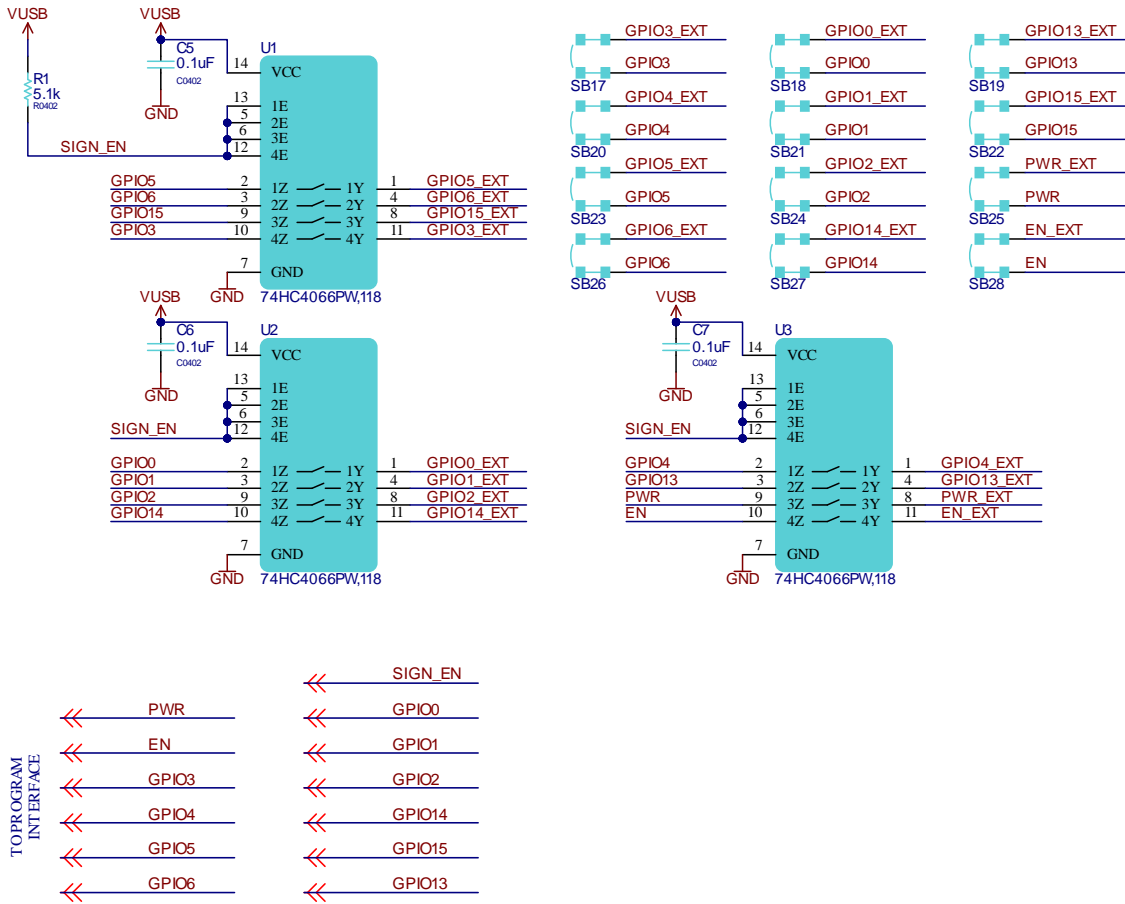


4. To install the drivers, a user must do one of the following:
  - Run 'Forcelnstallation.bat' as Administrator from the driver installer. Usually, it is provided with the software at 'C:\Program Files\Renesas Electronics\Go Configure Software Hub\driver'.
  - Alternatively, a user can reinstall the software, and the driver will be installed normally, provided there are no more conflicts. Repairing the software should also do the job.

## 5. Board Schematic



# ForgeFPGA Evaluation Board R2.0



## 6. Bill Of Materials

Designator	Manufacturer Part Number	Manufacturer	Quantity
BP1, BP2, BP3, BP4	SJ61A6	3M	4
C1, C3, C24, C26, C27, C28, C31	GRM21BR71A106KA73L	Murata	7
C2, C4-C7, C23, C29, C30, C32	GRM155R71C104KA88D	Murata	9
C22	GRM1555C1H9R0DA01D	Murata	1
C25	GRM155C81A105KA12D	Murata	1
D3	150060SS75000	Wurth Electronics	1
J1	030SQ025J6618G	Renesas	1
J2	PH1-04-UA	Adam Equipment	1
J3, J4, J5, J6	2PH1-13-UA	Adam Equipment	4
J7, J8	PPPC062LJBN-RC	Sullins	2
J10	12402012E212A	Amphenol	1
L3	MPZ1005S121HT000	TDK	1
Q1, Q2	BC817-40,215	Nexperia	2
R1, R13-R17, R18, R22-R24, R26	RC0402FR-075K1L	Yageo	11
R11, R12	RC0402FR-0722RL	Yageo	2
R19, R20, R21, R25, R27	RC0402FR-072KL	Yageo	5
R28, R29	RC0402FR-071KL	Yageo	2
RT1, RT2	0ZCK0020FF2G	Bel	2
SW1	EVQ-P7C01P	Panasonic	1
TP1, TP2	D3082-05	Harwin	2
U1, U2, U3	74HC4066PW,118	Nexperia	3
U7, U9	SLG59M1563V	Renesas	2
U8	SLG7RN46383	Renesas	1
VD3, VD4, VD5, VD6, VD7	D5V0F1U2LPQ-7B	Diodes	5

## 7. Ordering Information

Part Number	Description
SLG7EVBFORGE	ForgeFPGA SLG47910 Evaluation Board

## 8. Revision History

Revision	Date	Description
1.01	Jul 23, 2024	Added information about initialization error
1.00	May 10, 2024	Initial release.

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