

# ISL91302B22-EVZ

User's Manual: Evaluation Board

Core Power Solutions

## ISL91302B22-EVZ

Evaluation Board

UG141  
Rev.1.00  
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## 1. Overview

The ISL91302B22-EVZ platform allows quick evaluation of the high performance features of the [ISL91302B](#) multi-output PMIC, which has two controllers capable of configuring its power stages for 2+2 channel outputs. Each channel can deliver up to 5A continuous output current per phase. The ISL91302B uses the Renesas proprietary R5 modulator technology to maintain accurate voltage regulation, while providing excellent efficiency and transient response. It also supports the standard I<sup>2</sup>C and SPI communication protocols, ideal for systems using a single-cell battery.

### 1.1 Key Features

- Small, compact design
- Supports both I<sup>2</sup>C and SPI bus communication protocols
- Adjustable V<sub>OUT</sub> and independent DVS control for both channels
- Real-time fault protection and monitor (OC, UV, OV, OT)
- Six layer board design optimized for thermal performance and efficiency
- Connectors, test points, and jumpers for easy measurements
- Built-in load transient circuits for each output channel

### 1.2 Specifications

The board is designed to operate at the following operating conditions:

- Input voltage rating from 2.5V to 5.5V
- Programmable output voltage range of 0.3V to 2V
- 2+2 configuration with 5A maximum load current/phase
- 4MHz default switching frequency
- DVS slew rate of 2.5mV/μs
- Operating temperature range: -40°C to +85°C
- V<sub>OUT1</sub> = 0.65V and V<sub>OUT2</sub> = 0.75V

### 1.3 Related Literature

For a full list of related documents, visit our website

- [ISL91302B](#) product page

### 1.4 Ordering Information

Part Number	Description
ISL91302B22-EVZ	ISL91302B 2+2 evaluation board

## 1.5 Contents

- ISL91302B22-EVZ evaluation board
- Evaluation software
- Mini USB I<sup>2</sup>C dongle with USB cable (ISLUSBMINIEVAL1Z)
- All applicable documentation

## 1.6 Recommended Equipment

- 0V to 10V power supply with at least 10A current sourcing capability ( $V_{IN}$  supply bias)
- 0V to 10V power supply with at least 1A current sourcing capability ( $V_{CC\_6V}$  supply bias)
- Electronic loads capable of sinking current up to 10A
- Digital multimeter
- 500MHz quad-trace oscilloscope
- Dual edge slew rate controllable signal generator
- Differential probe (for load transient current measurement)

## 1.7 Block Diagram

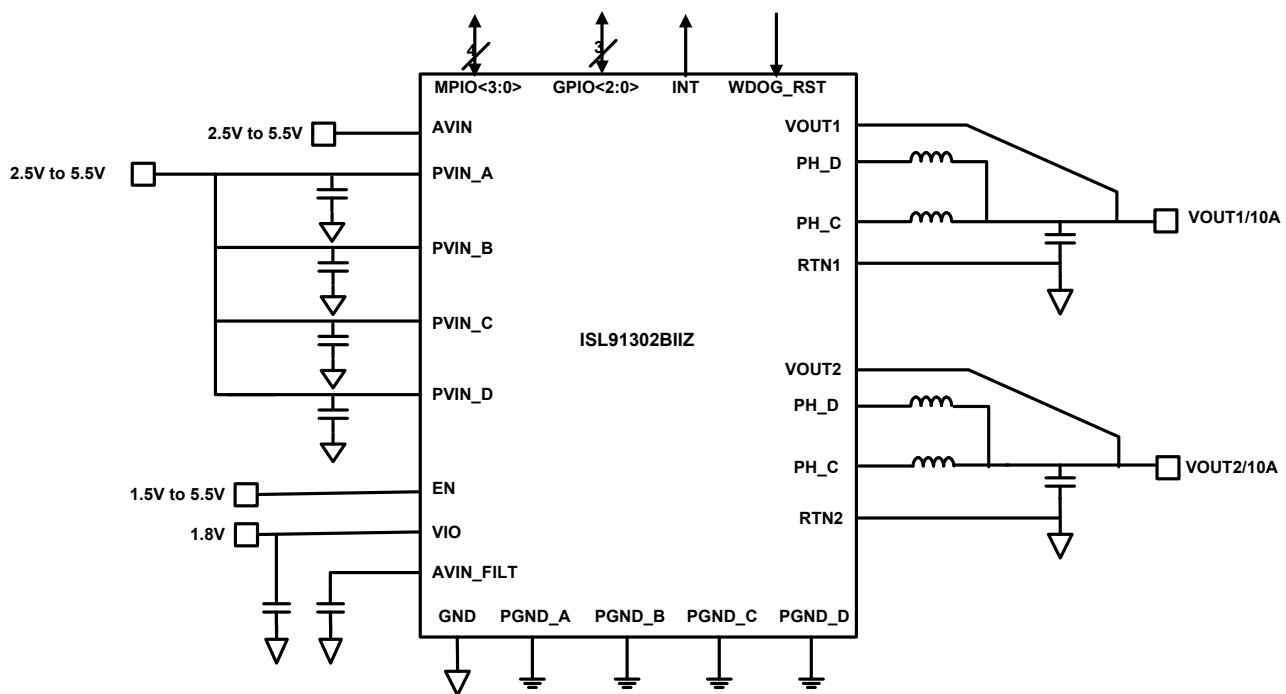


Figure 1. ISL91302B 2+2 Block Diagram

## 2. Functional Description

The ISL91302B22-EVZ evaluation board provides a simple platform to demonstrate the feature-rich ISL91302B PMIC. It has a 0.65V and 0.75V output (default) on each of its output channels after start-up and each output voltage can be programmed by I<sup>2</sup>C/SPI. The evaluation board has been functionally optimized for best performance, working harmoniously with the factory default tuning on the ISL91302B. The input power and load connections are provided through multi-pin connectors for high current operations.

The ISL91302B22-EVZ evaluation board is shown in [Figure 9 on page 9](#). The evaluation board's key test points and jumpers are listed in [Table 1](#). The ISL91302B's internal registers can be accessed by the I<sup>2</sup>C/SPI through the on-board headers J24 (SPI) and J60 (I<sup>2</sup>C).

**Table 1. Description of Important Test Points and Jumpers**

Test Point	Description
J6(+), J7(-)	Headers for connecting V <sub>IN</sub> supply
J35(+), J36(-)	Buck1 Headers for connecting external load
J37(+), J38(-)	Buck2 Headers for connecting external load
J3	V <sub>IN</sub> Kelvin connection for efficiency measurements
J15	Buck1 V <sub>OUT</sub> Kelvin connection for efficiency measurements
J18	Buck2 V <sub>OUT</sub> Kelvin connection for efficiency measurements
TP1	VCC_6V SUPPLY for VIO LDO and load transient circuits
J56	Buck1 driver input for load transient circuit
J57	Buck2 driver input for load transient circuit
J52	Load transient current sense, 1A/10mV
J55	Load transient current sense, 1A/10mV
J24	Header for connecting to SPI interface
J60	Header for connecting to I <sup>2</sup> C interface

The evaluation software GUI window for the ISL91302B is shown in [Figure 8 on page 8](#). The schematic of the ISL91302B22-EVZ evaluation board is shown in [Figure 13 on page 11](#). The PCB layout images for all layers are shown in [Figures 16 through 23](#). The bill of materials for the ISL91302B22-EVZ is shown in the [“Bill of Materials” on page 14](#).

### 2.1 Operating Range

The V<sub>IN</sub> range of the board is 2.5V to 5.5V. The adjustable V<sub>OUT</sub> range for the ISL91302B22-EVZ is 0.3V to 2.0V. The I<sub>OUT</sub> range of the board is 0A to 5A per phase. The operating ambient temperature range is -40°C to +85°C.

### 2.2 Quick Start Guide

For the ISL91302B22-EVZ evaluation board, the default output voltages for V<sub>OUT1</sub> and V<sub>OUT2</sub> are set at 0.65V and 0.75V, respectively. No jumper configurations are needed to power up the part into its default state. All the settings and features are instead loaded through the one-time programmable memory inside the IC, after the minimum bias conditions are met. Refer to the [“Setup Guide” on page 5](#) on how to power up the board for proper operation.

### 2.2.1 Setup Guide

- (1) Place scope probes on the  $V_{OUT}$  test point and other test points of interest.
- (2) Connect a power supply to J6 and J7 ( $V_{IN}$  supply), with a voltage setting between 2.5V and 5.5V. This will bias the PVIN and AVIN pins, but not initiate the startup sequence. The quiescent current should be less than 1mA.
- (3) Connect a second power supply to TP1 ( $VCC_{6V}$ ), with the voltage set to 6V. This will bias the VIO and Chip Enable pins as well as the on-board load transient circuits. The ISL91302B will boot up its internal reference, load the default register settings, and then initiate a power-on sequence. The two outputs should turn on in the Pulse Skipping mode if there are no external loads present, and  $V_{OUT1}$  and  $V_{OUT2}$  should default to 0.65V and 0.75V, respectively.
- (4) During the startup sequence, the two outputs should turn on sequentially, Buck1 then Buck2. Buck1 will turn on with a 1.4ms delay from the Chip Enable pin going high, and Buck2 will turn on 1ms later.
- (5) To initiate a shutdown sequence, short EN to GND at TP18, and the ISL91302B will turn off all the buck regulators at the same time.

### 2.2.2 I<sup>2</sup>C/SPI Communication

The ISL91302B supports I<sup>2</sup>C communication by default. A USB to I<sup>2</sup>C communication dongle (ISLUSBMINIEVAL1Z) is included with each ISL91302B22-EVZ board, and the Renesas Graphical User Interface (GUI) supports this tool across all operating systems.

To communicate with the ISL91302B using I<sup>2</sup>C, connect the Renesas USB to the I<sup>2</sup>C dongle to J60. Make sure R<sub>89</sub> is present on the board, because it provides the pull-up from SPI\_SS to 1.8V VIO supply.

Note: For the SPI communication option using the GUI, contact Renesas [support](#).

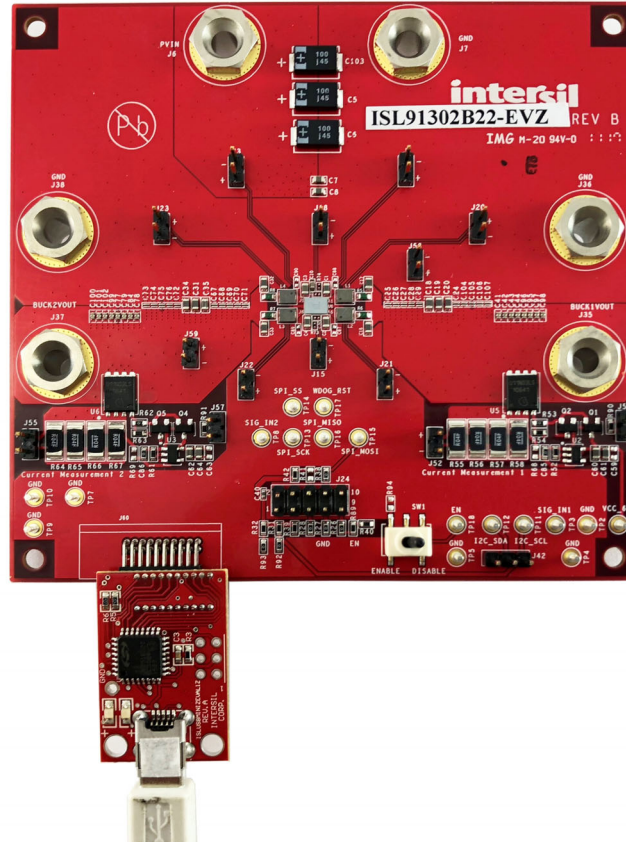


Figure 2. Communication Dongle Connection

### 2.2.3 Efficiency Measurement

- (1) Connect a power supply at J6 ( $V_{IN}$  supply), with the voltage setting between 2.5 and 5.5V. Set its current limit high enough to support the maximum load current with additional headroom. If the power supply supports remote sense lines, use a Kelvin connection on J3. Otherwise, connect a multimeter at J3.
- (2) Apply 6V to TP1 (VCC\_6V) to initiate the startup sequence and all three outputs will turn on. To get an accurate single channel measurement, disable the other two outputs using the GUI.
- (3) Turn on the electronic load at VOUTx. The connection should be made at J35 (VOUT1) or J37 (VOUT2). Make sure the load current does not exceed 5A per phase, and the correct wire size is used when attaching the electronic load.
- (4) Measure the output voltage with a multimeter. The voltage should regulate within datasheet spec limits.
- (5) To determine efficiency, measure input and output voltages at the Kelvin sense test points (S+ and S-), which are located at J3 ( $V_{IN}$  SENSE) and J15 (BUCK1 SENSE) or J18 (BUCK2 SENSE) headers. Measure the input and output currents from the  $V_{IN}$  power supply and the electronic load. Calculate efficiency based on these measurements. For detailed setup information, refer to [Figure 11 on page 10](#).

### 2.2.4 Load Transient Measurement

- (1) Go through the setup procedure (see [“Setup Guide” on page 5](#)). The ISL91302B22-EVZ should already be powered up with 2.5V to 5.5V at J6 ( $V_{IN}$  supply) and 6V at TP1 (VCC\_6V).
- (2) Connect a slew rate controllable signal generator to transient load circuit input, J56 (TRANSIENT 1 PULSE GEN) or J57 (TRANSIENT 2 PULSE GEN).
- (3) Program the signal generator to pulse mode, set the frequency to 100Hz, ON duration to 200 $\mu$ s, and signal amplitude from 0V to 2V. The load transient circuit starts to turn on when the input is  $\sim$ 2.6V. When in doubt, connect the signal generator output to an oscilloscope set to 1M $\Omega$  termination. The slew rate of the pulse, both rising and falling, should be conservatively slow, for example, 1 $\mu$ s.
- (4) Connect a differential probe to monitor load current across the sense resistors J52 (ISENSE1) or J55 (ISENSE2). The load current can be accurately converted to a voltage at 1A/10mV. Make sure the vertical scale of the oscilloscope is set properly to display the full amplitude of the load profile.
- (5) Connect a second differential probe at the VOUT sense points connected to the  $V_{OUT}$  decoupling capacitors, J58 (BUCK1 SENSE) or J59 (BUCK2 SENSE).
- (6) Set the oscilloscope to measure the rise and fall times and maximum level of the load current. Slowly increase the signal generator amplitude and slew rate until desired load profile is achieved. For detailed setup information, refer to [Figure 12 on page 10](#).

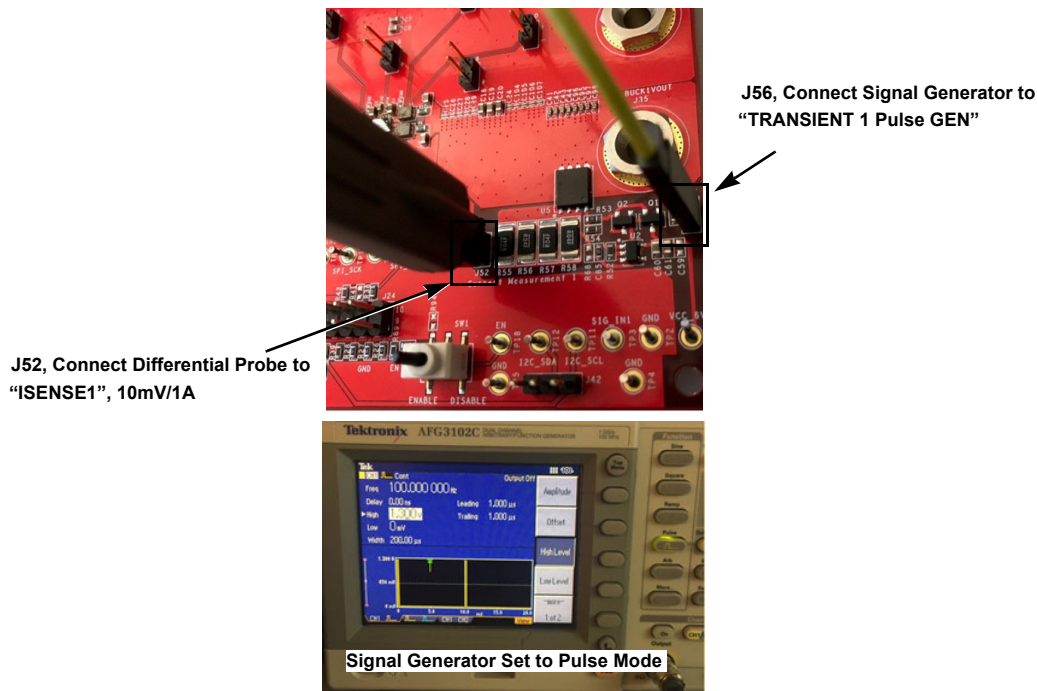


Figure 3. BUCK1 Transient Load Connection Example

### 2.3 Evaluation Software Installation and Use

- (1) On the evaluation CD, double-click AutoRun.exe. Follow the instructions to install the Multiphase PMIC I<sup>2</sup>C Control Tool software..
- (2) Attach the USB-I<sup>2</sup>C interface (ISLUSBMINIEVAL1Z) dongle to the computer using the supplied USB cable.
- (3) Attach the USB-I<sup>2</sup>C interface dongle to J60 on the ISL91302B22-EVZ evaluation board. Following the instructions in ["Setup Guide" on page 5](#), connect the power supplies, DC load, and other test equipment to the ISL91302B22-EVZ evaluation board, then apply power.
- (4) Start the Multiphase PMIC Control Tool software. Select Start > Programs > Renesas > Multiphase PMIC I<sup>2</sup>C Control Tool.
- (5) Select ISL91302B from the "Select Product" drop down menu. Click "Connect" button on the GUI to establish connection between GUI and the dongle . The LED light on the dongle will lit. If a connection is not detected, the software shows a red X next to I<sup>2</sup>C Communication. Press Reset to reconnect the dongle.

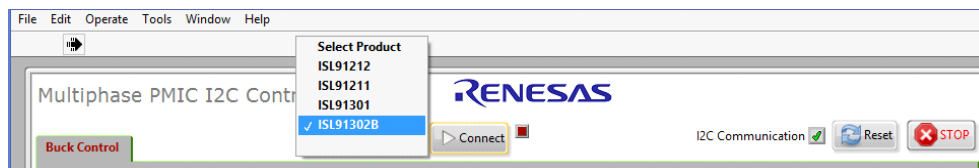


Figure 4. Product Selection Menu and I<sup>2</sup>C Communication OK Indicator

- (6) After the evaluation software establishes a connection to the USB-I<sup>2</sup>C interface dongle, the software loads a blank startup script by default and reads all the pertinent register values to show on screen.
- (7) The user should see Buck1 and Buck2 enabled, and the default DVS0 values should be 0.65V and 0.75V for Buck1 and Buck2, respectively. If no fault conditions occurred during the board power-up, all the fault indicators (UV, OV, OC) should be clear rather than red.
- (8) To change the output voltage, enter the desired value in voltages in the DVS0 control. There are also four default DVS values that are loaded as part of ISL91302B one time programmable memory space. The user can go to any of them and activate a DVS command by clicking on the DVS Pointer.

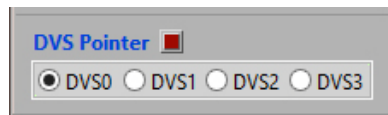


Figure 5. DVS Pointer Selection

- (9) Changing the ‘Max Voltage’ controls changes the internal feedback divider between ratios of 1 times, 0.8 times, and 0.6 times. This changes the maximum output voltage the ISL91302B can support, with the maximum being 2V. Keep in mind the smallest DVS resolution the IC and the software can support is no less than the maximum voltage divided by 1024.
- (10) After the evaluation software is up and running without hiccup, it polls all the registers at 2s intervals by default. The user can disable this feature by clearing the ‘Continuous Read’ option.



Figure 6. Continuous Read and Manual Read All Options

- (11) The fault indicators self clear when the software reads the register through Continuous Read or the fault is removed. Three additional replica fault indicators (UV, OV, and OC) latch the faults so they will clear only after the user clicks ‘Push To Clear’ in the event of a spurious fault condition.



Figure 7. Fault Indicators

Note: The default switching frequency of the ISL91302B is set to 4MHz and the slew rates for both DVS and power-up/down are set to 2.5mV/μs. These settings, along with many other features, are programmable only through OTP request or a Startup Script, and are not supported by the evaluation software. For more information, contact your local Renesas [support](#).

Figure 8. Multiphase PMIC (ISL91302B) I2C Control Tool Interface



### 3. PCB Layout Guidelines

The ISL91302B22-EVZ board is a 6-layer FR4 board. The main components are the ISL91302B, its passive filter components, test points, and connectors. A 220nH inductor is located close to each phase node of the ISL91302B, and 5x22 $\mu$ F plus 8x4.3 $\mu$ F capacitors are populated at the output of each inductor. PVIN is distributed using a power plane on an inner layer with a 10 $\mu$ F capacitor placed in close proximity to the PVIN and PGND balls of the power stage. In addition, there is a 10 $\mu$ F AVIN filter capacitor placed next to the ISL91302B referenced to a quiet ground plane.

The PCB layout is a critical design step in making sure the designed converter works under optimum conditions. For the ISL91302B, the power loop is composed of the inductor, output capacitors, phase node, and PGND pins. Keep this loop as short as possible and the connecting traces among them should be direct, short, and wide. The phase nodes of ISL91302B are very noisy, so keep remote sense signals away from traces coming out of the phase nodes, and do not route them under the inductor in an adjacent layer. The input capacitor should be placed as close as possible to the PVIN and PGND pins, and there should be a large unbroken ground plane that should connect all the decoupling capacitors together.

The heat of the ISL91302B is mainly dissipated through the GND and PHASE plane vias under the IC. To maximize thermal performance, use as much copper area as possible connecting to these vias. In addition, a solid ground plane is helpful for better EMI performance.

#### 3.1 Key Layout Strategies

- Place input capacitors as close as possible to their respective PVIN and PGND pins to minimize parasitic loop inductance.
- Route phase nodes with short, wide traces and avoid any sensitive nodes.
- Route the remote sense lines directly to the load using small, low inductance capacitors at the load for bypassing.
- Output capacitors should be close to the inductors and have a low impedance path to the PGND pins.
- Keep digital and phase nodes from intersecting AVIN\_FILT, VOUT, and RTN lines.
- Create a PGND plane on the second layer of the PCB below the power components and bumps carrying high switching currents.

#### 3.2 Evaluation Board

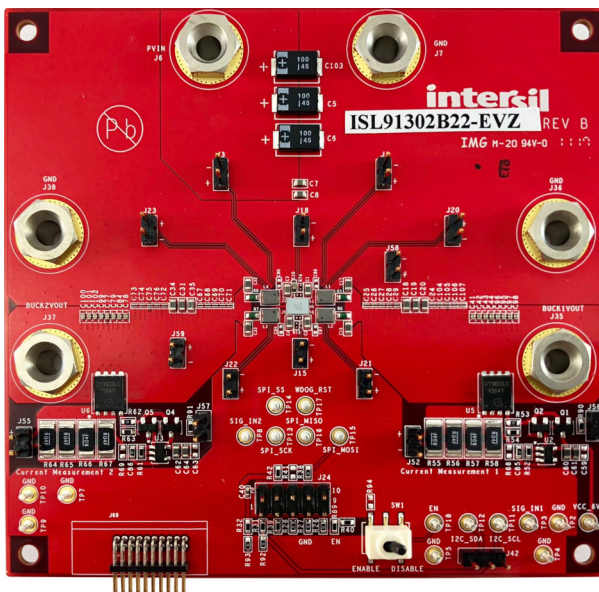


Figure 9. ISL91302B22-EVZ Top View

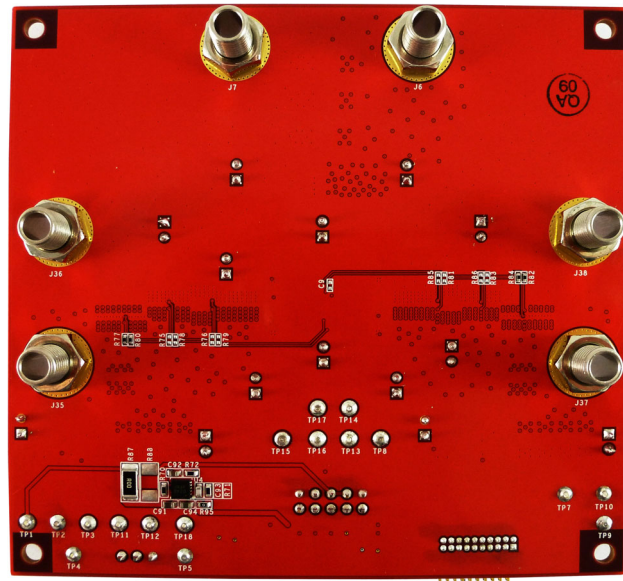


Figure 10. ISL91302B22-EVZ Bottom View

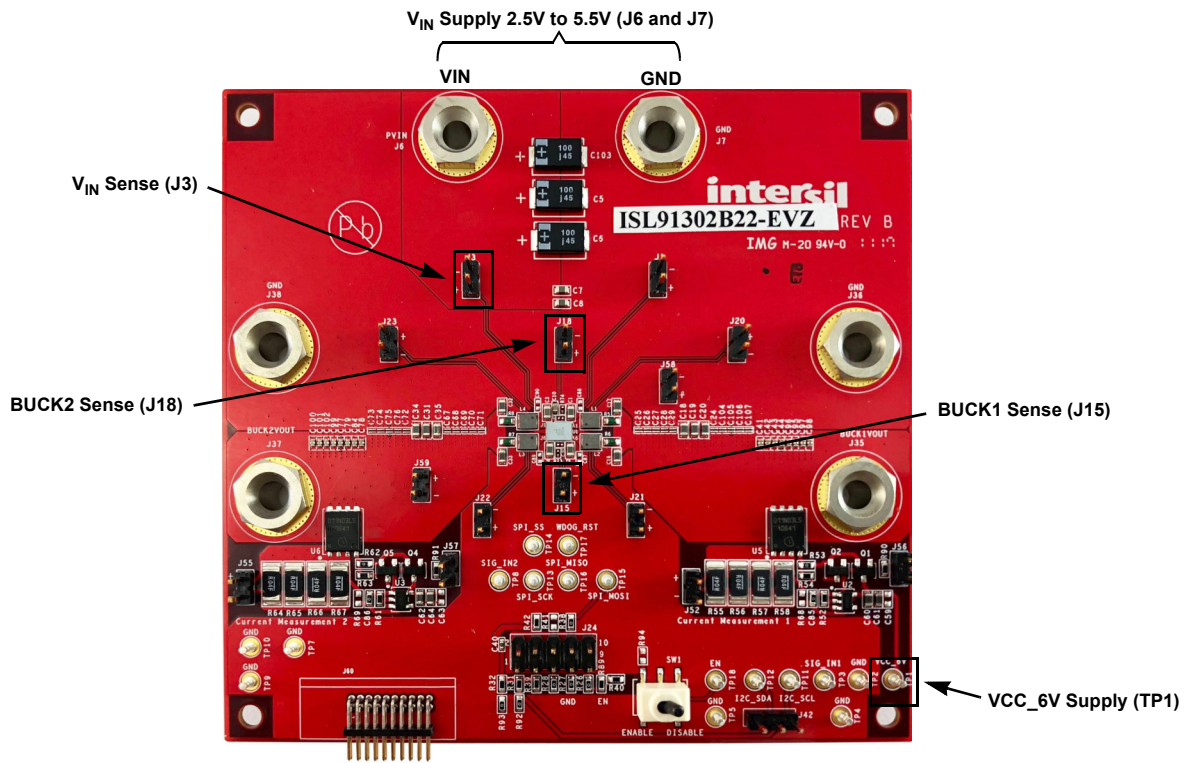


Figure 11. ISL91302B22-EVZ Efficiency Measurement Connections

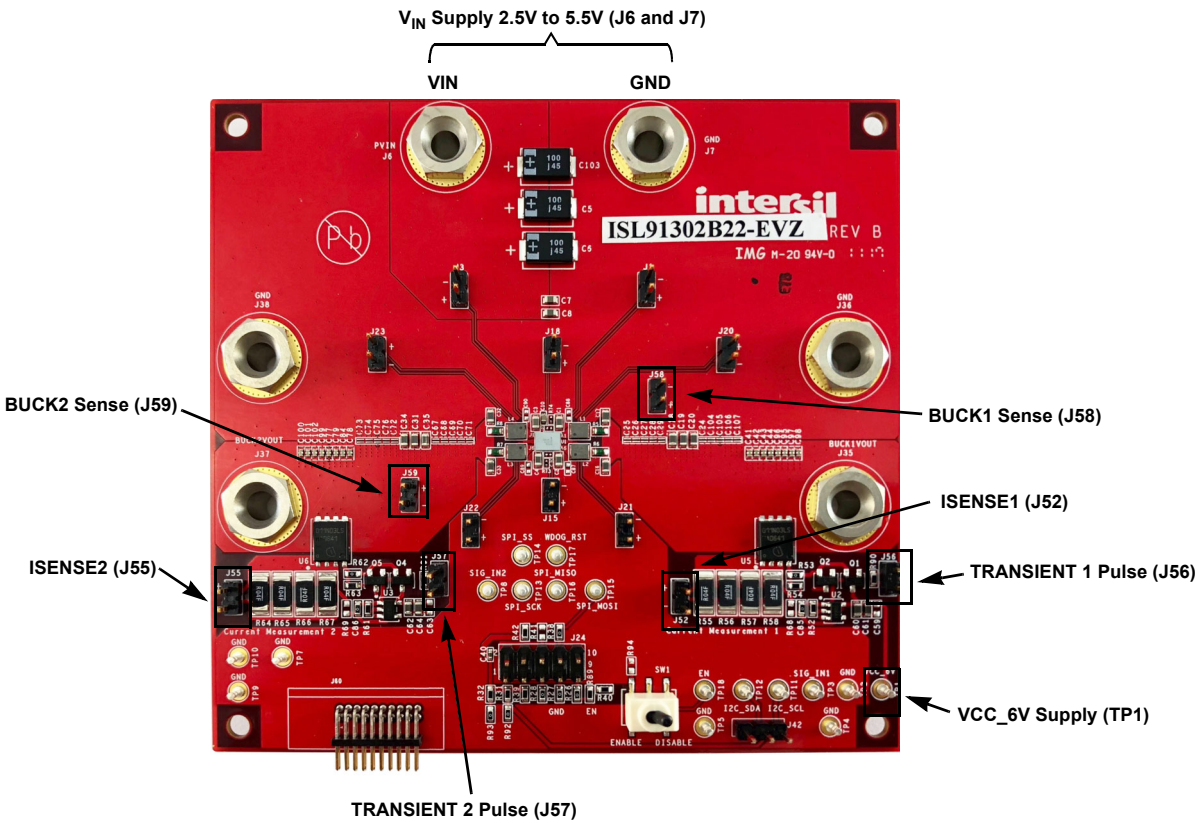


Figure 12. ISL91302B22-EVZ Load Transient Measurement Connections

### 3.3 Schematics

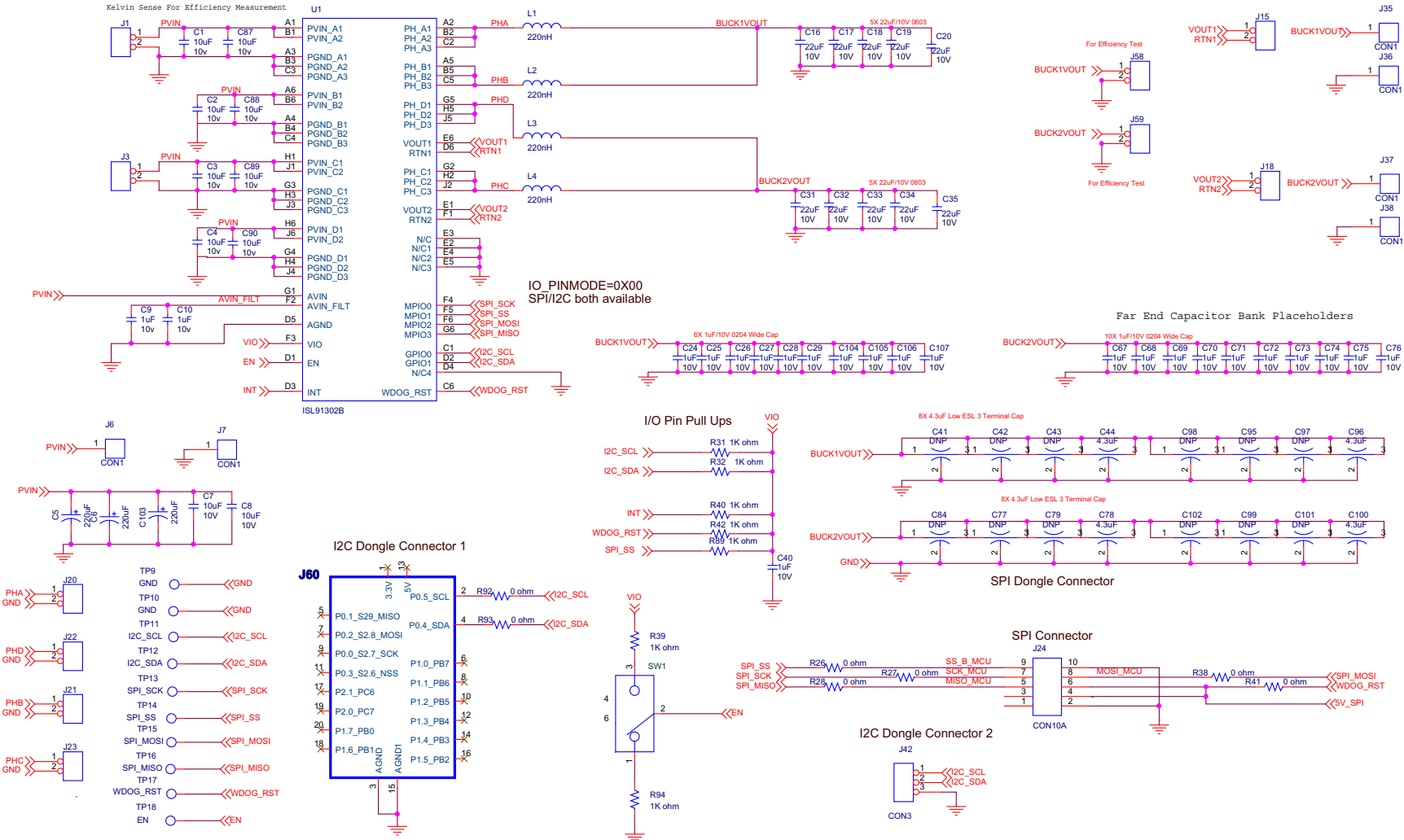
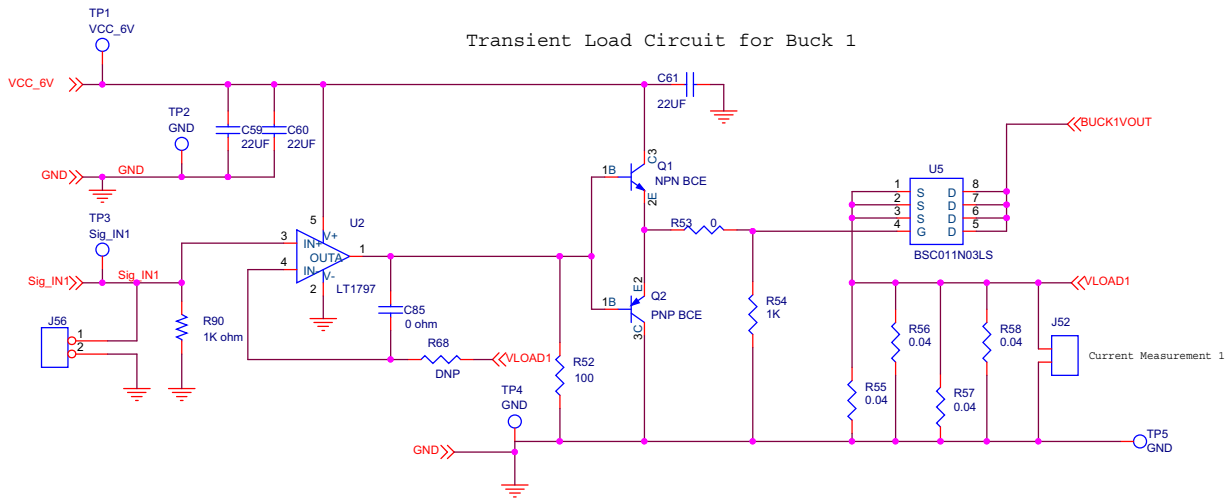
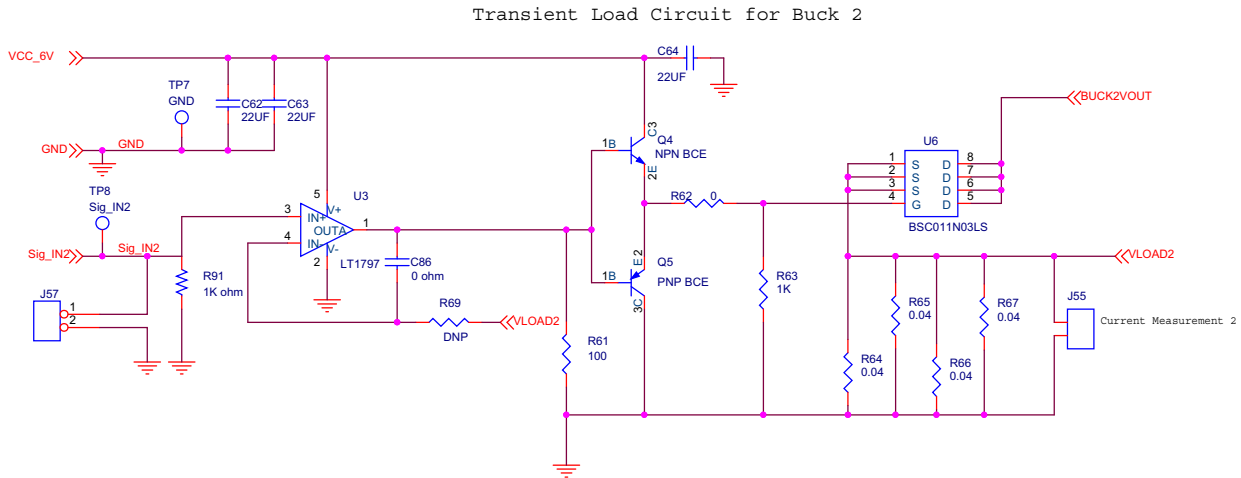


Figure 13. ISL91302B22-EVZ Schematic - Page 1

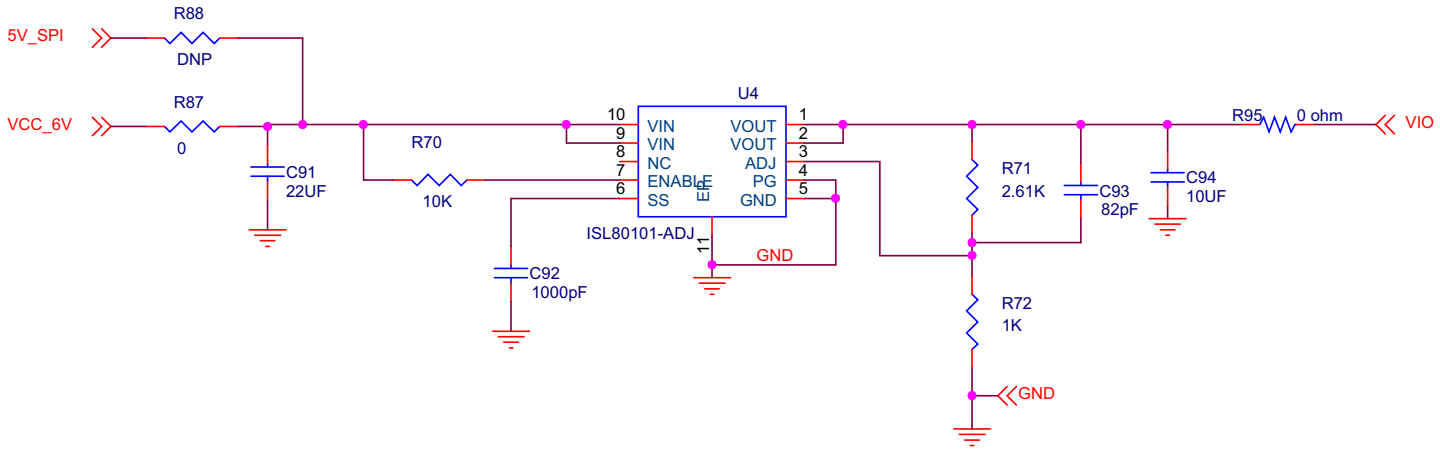


Magnitude of input signal sets load current.  
 To configure load trans circuit R68 = DNP, C85 = 0 Ohm.



Magnitude of input signal sets load current.  
 To configure load trans circuit R69 = DNP, C86 = 0 Ohm.

Figure 14. ISL91302B22-EVZ Schematic - Page 2



Output sense resistors for each rail.

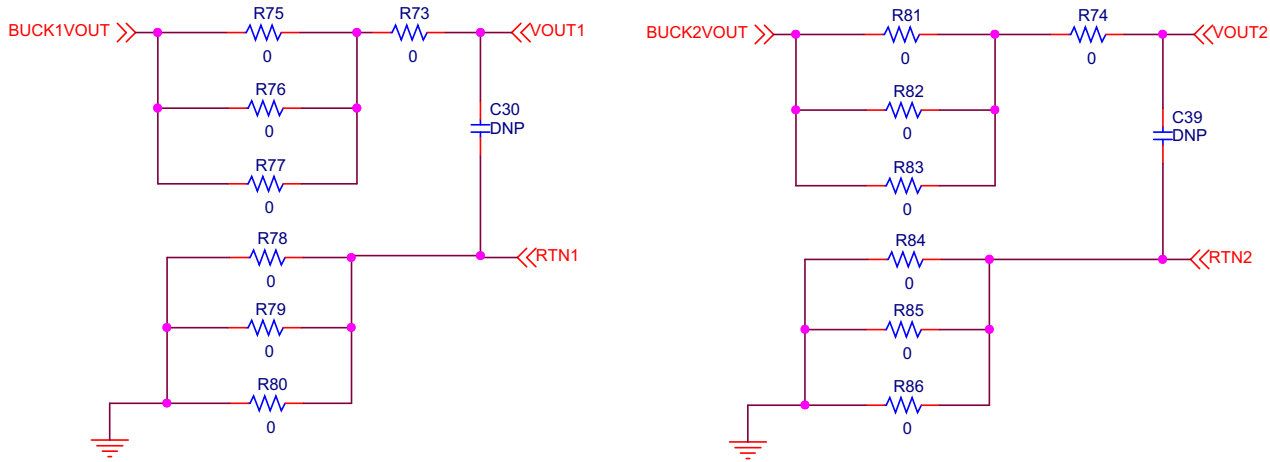


Figure 15. ISL91302B22-EVZ Schematic - Page 3

### 3.4 Bill of Materials

Qty	Reference Designator		Description	Digi-Key Part Number	Manufacturer	Manufacturer Part Number
	Top Components	Bottom Components				
1		C93	82pF, NP0, 0603	587-4437-1-ND	Taiyo Yuden	QVS107CG820JCHT
2	C85, C86		0Ω, 1/10W, 0603	P0.0GCT-NDD	Panasonic	ERJ-3GEY0R00V
1		C92	1000pF, 50V, X7R, 0603	587-1445-1-ND	Taiyo Yuden	HMK107B7102KA-T
1	C40		1μF, 10V, X5R, 0402	587-1454-1-ND	Taiyo Yuden	LMK105BJ105KV-F
16	C41, C42, C43, C44, C77, C78, C79, C84, C95, C96, C97, C98, C99, C100, C101, C102		4.3μF Multi-Terminal, 4V, X5R, 0402	n/a	Murata	LLD154R60G435ME01
7	C1, C2, C3, C4, C7, C8	C94	10μF, 10V, X5R, 0603	587-3412-1-ND	Taiyo Yuden	LMK107BBJ106MAHT
1	C10		10μF, 10V, X5R, 0402	1276-1450-1-ND	Samsung Electronics	CL05A106MP5NUNC
15	C16, C17, C18, C19, C20, C31, C32, C33, C34, C35, C60, C61, C62, C64	C91	22μF, 10V, X5R, 0603	445-9077-1-ND	TDK	C1608X5R1A226M080AC
3	C5, C6, C103		100μF, 6.3V, Polymer Tant, D2 Case	P16620CT-ND	Panasonic	6TPC100M
2	R73, R74		0Ω, 1/20W, 0201	P15979CT-ND	Panasonic	ERJ-1GN0R00C
4		R77, R80, R82, R84	0Ω, 1/10W, 0402	P0.0JCT-ND	Panasonic	ERJ-2GE0R00X
9	R26, R27, R28, R38, R53, R62, R92, R93, R95		0Ω, 1/10W, 0603	P0.0GCT-ND	Panasonic	ERJ-3GEY0R00V
1		R87	RES SMD 0.0Ω Jumper 3/4W 2010	RMCF2010ZT0R00CT-ND	Stackpole	RMCF2010ZT0R00
8	R55, R56, R57, R58, R64, R65, R66, R67		0.04Ω, 1%, 1W, 2010	WSLF-.04CT-ND	Vishay	WSL2010R0400FEA18
2	R52, R61		100Ω, 1%, 1/10W, 0603	P100HCT-ND	Panasonic	ERJ-3EKF1000V
11	R31, R32, R39, R40, R42, R89, R90, R91, R54, R63	R72	1.0kΩ, 1%, 1/10W, 0603	P1.00KHCT-ND	Panasonic	ERJ-3EKF1001V
1		R71	2.61kΩ, 1%, 1/10W, 0603	P2.61KHCT-ND	Panasonic	ERJ-3EKF2611V
1		R70	10kΩ, 1%, 1/10W, 0603	P10.0KHCT-ND	Panasonic	ERJ-3EKF1002V
4	L1, L2, L3, L4		0.22μH, 10mΩ, 6.6Asat, 2520 Inductor	n/a	Cyntec	PIFE25201T-R22MS
2	Q1, Q4		TRANS NPN 40V 0.2A SOT-23	MMBT3904FSCT-ND	Fairchild	MMBT3904
2	Q2, Q5		TRANS PNP 40V 0.2A SOT-23	MMBT3906FSCT-ND	Fairchild	MMBT3906
6	J6, J7, J36, J36, J37, J38		Conn Banana Jack Threaded 12AWG	J10138-ND	Cinch Connectivity	108-0740-102

Qty	Reference Designator		Description	Digi-Key Part Number	Manufacturer	Manufacturer Part Number
	Top Components	Bottom Components				
17	TP1, TP2, TP3, TP4, TP5, TP7, TP8, TP9, TP10, TP11, TP12, TP13, TP14, TP15, TP16, TP17, TP18		Conn-Gen, Compact Test Point, Vertical, White	36-5002-ND	Keystone	5002
14	J1, J3, J15, J18, J20, J21, J22, J23, J52, J55, J56, J57, J58, J59		2 Pin Header, 100 mil spacing	609-4434-ND	FCI	77311-118-02LF
1	J42		3 Pin Header, 100 mil spacing	952-1312-ND	Harwin	M22-2510305
1	J24		10 Pin Header, 100 mil spacing	609-3243-ND	FCI	67997-410HLF
1	J60		Right angle connector	952-1398-ND	Harwin Inc.	M50-3901042
1	SW1		Switch-Toggle, SMD, 6 Pin, SPDT, 2POS, On-None-On,RoHS	CKN1784CT-ND	ITT INDUSTRIES/ C&K DIVISION	GT11MSCBE
1	U1		ISL91302, 0.4mm Pitch WLCSP	n/a	Intersil	ISL91302B
2	U2, U3		IC OPAMP VFB 200MHZ RRO SOT23-5	296-32191-1-ND	Texas Instruments	OPA356AIDBVR
1		U4	IC REG LDO ADJ 1A 10DFN	ISL80101IRAJZ-TKCT-ND	Intersil	ISL80101IRAJZ
2	U5, U6		MOSFET N-CH 30V 100A 8TDSO	BSC011N03LS	Infineon	BSC011N03LSCT-ND
5	C87, C88, C89, C90	C9	Capacitor, 0402, DNP		any	any
20	C24, C25, C26, C27, C28, C29, C67, C68, C69, C70, C71, C72, C73, C74, C75, C76, C104, C105, C106, C107		Capacitor, 0204, DNP		any	any
2	C59, C63		Capacitor, 0603, DNP		any	any
2	C30, C39		Capacitor, 0201, DNP		any	any
9	R41	R75, R76, R78, R79, R81, R83, R85, R86	Resistor, 0603, DNP		any	any
2	R68, R69		Resistor, 0603, DNP		any	any
1		R88	Resistor, 2010, DNP		any	any

Note:

1. Components highlighted in red are DNP

### 3.5 Board Layout

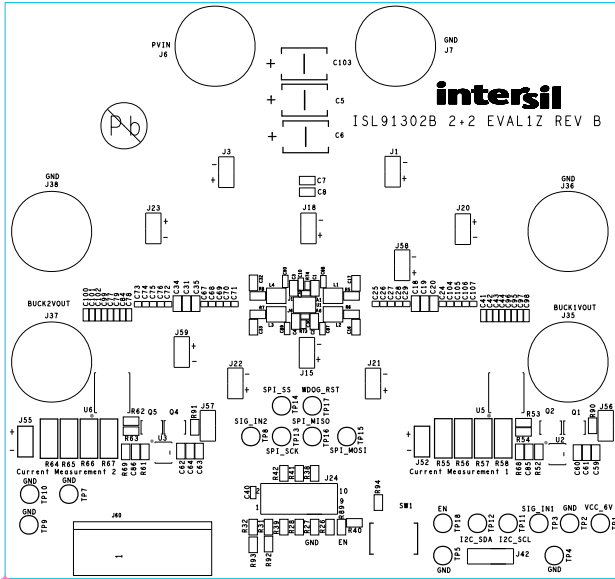


Figure 16. Top Silkscreen Layer

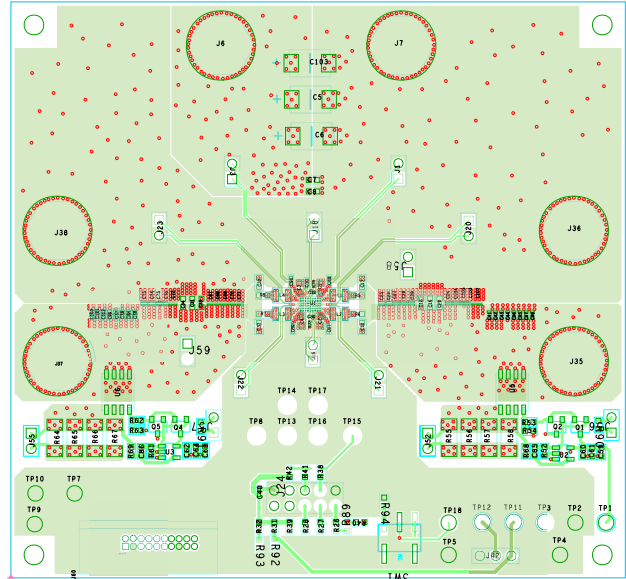


Figure 17. Top Layer

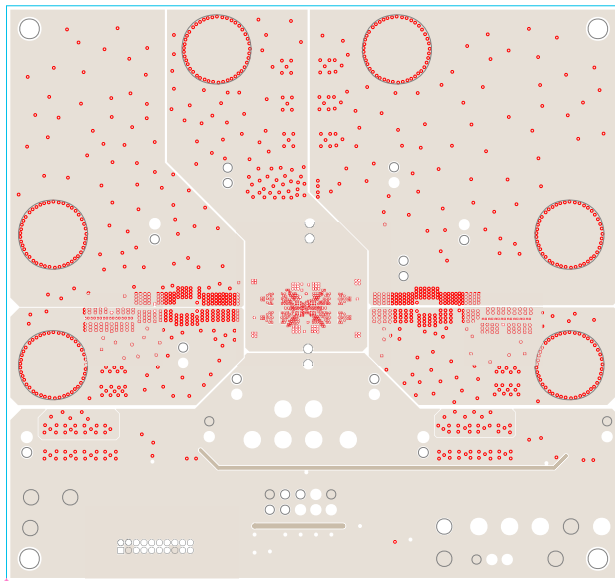


Figure 18. Layer 2 (PVIN Plane)

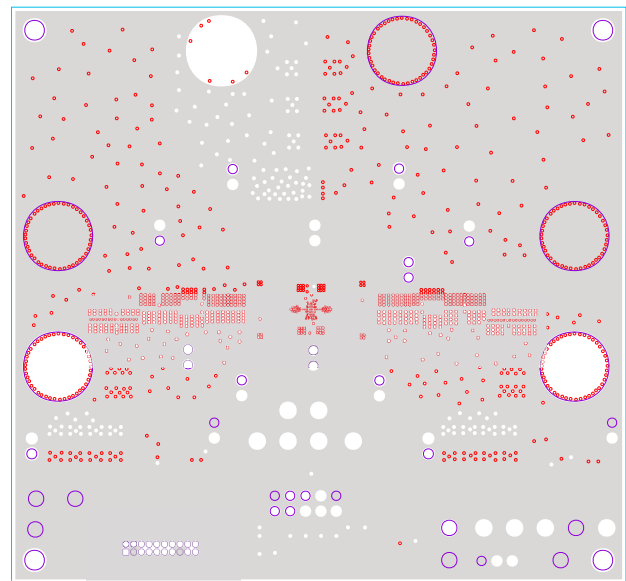


Figure 19. Layer 3 (GND Plane)



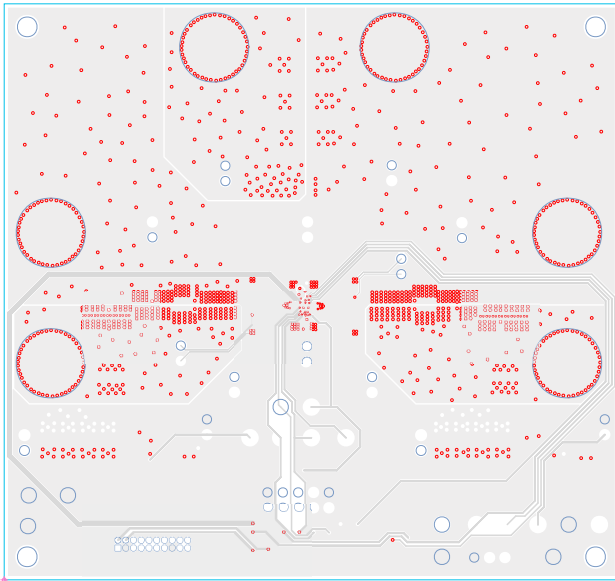


Figure 20. Layer 4 (IO Communications)

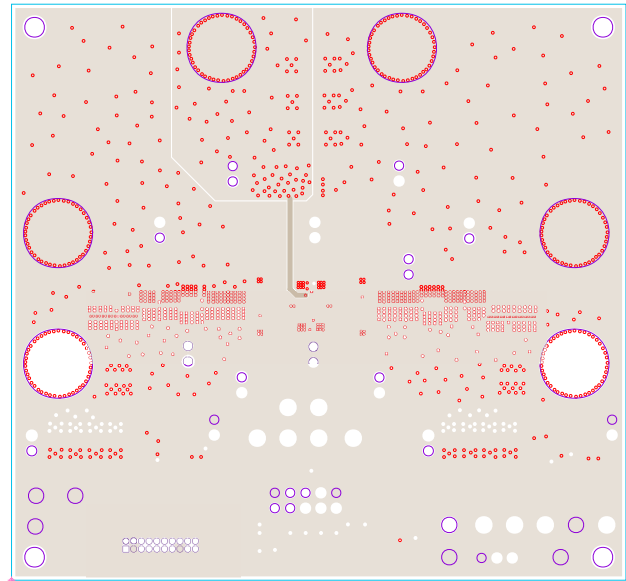


Figure 21. Layer 5 (GND Plane)

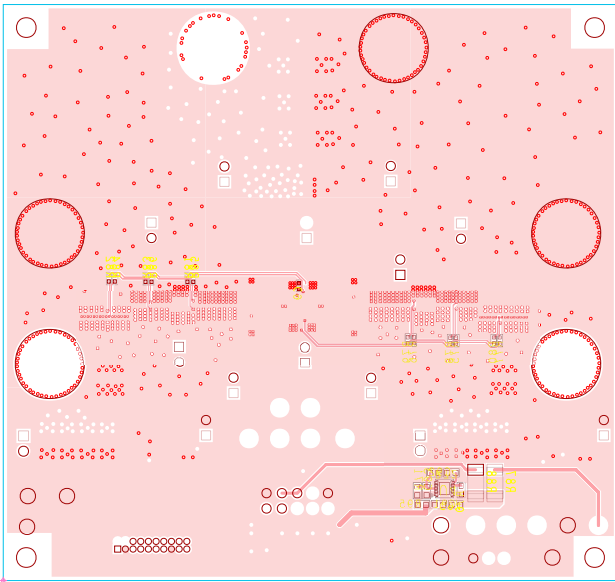


Figure 22. Bottom Layer (Remote Sense Lines)

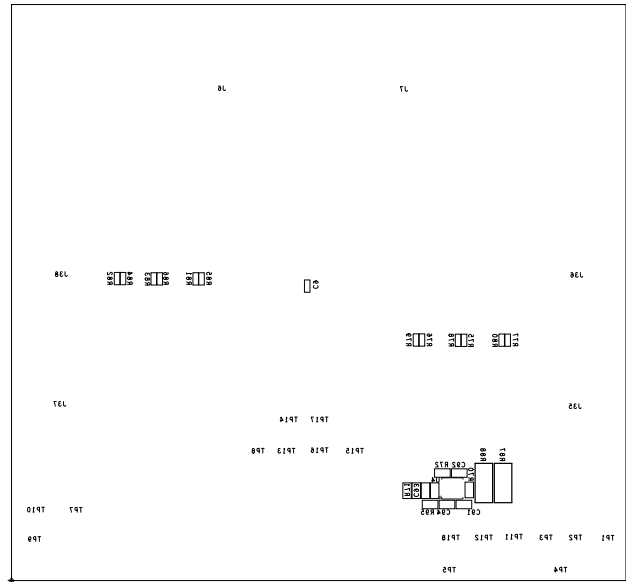
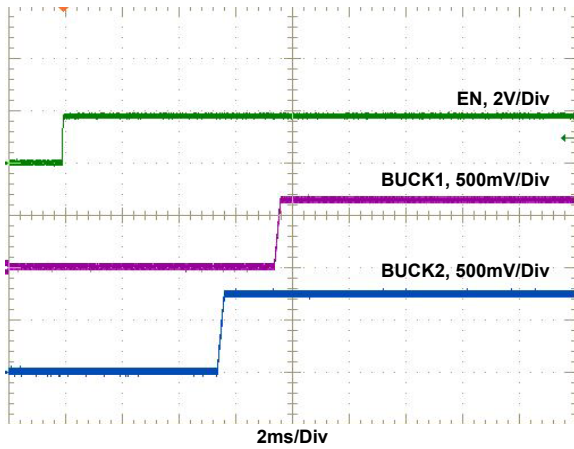


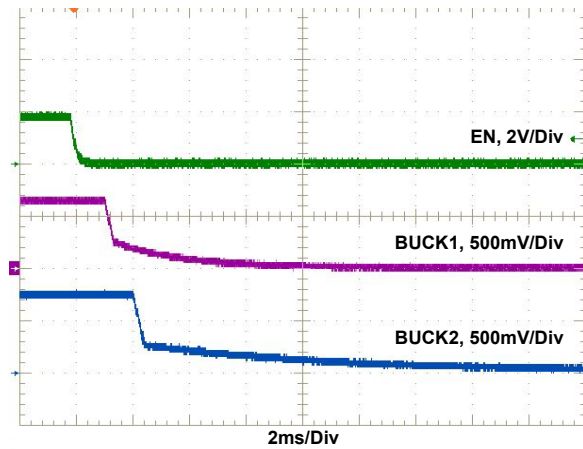
Figure 23. Bottom Silk Screen Layer

### 4. Typical Performance Curves



Note: Delay times are not the default values (modified by OTP change)

Figure 24. Startup by EN,  $V_{OUT1} = 0.65V$ ,  $V_{OUT2} = 0.75V$



Note: Delay times are not the default values (modified by OTP change)

Figure 25. Shutdown by EN,  $V_{OUT1} = 0.65V$ ,  $V_{OUT2} = 0.75V$

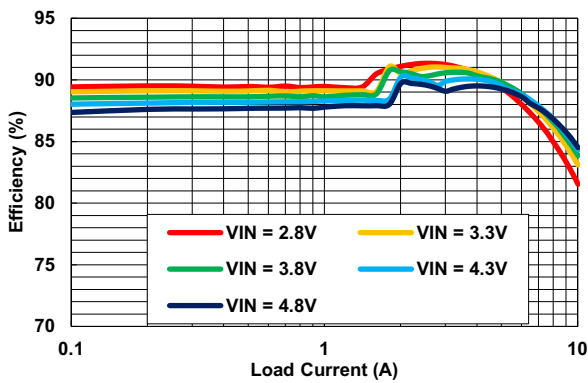


Figure 26. Dual-Phase Efficiency ( $V_{OUT} = 1V$ ), Continuous Load Sweep (0.1A to 10A),  $f_{SW} = 2MHz$

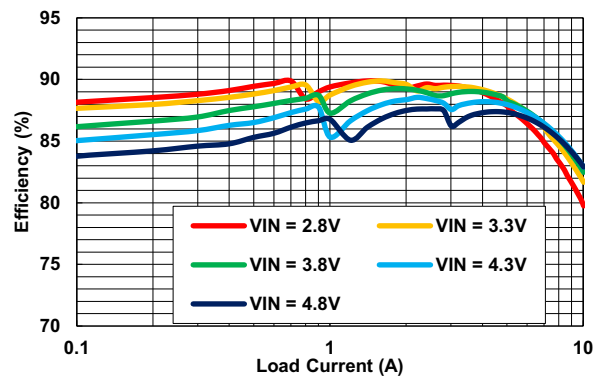
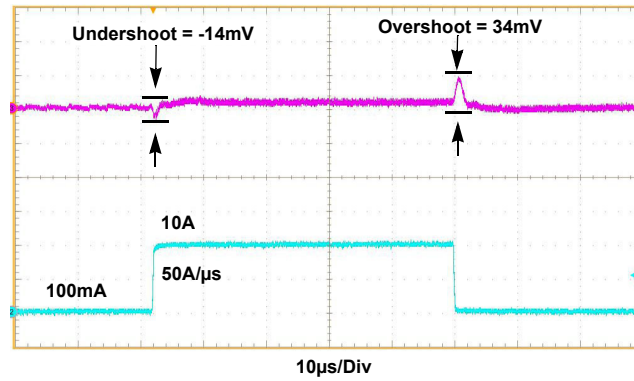


Figure 27. Dual-Phase Efficiency ( $V_{OUT} = 1V$ ), Continuous Load Sweep (0.1A to 10A),  $f_{SW} = 4MHz$



$V_{IN} = 3.8V$ ,  $V_{OUT} = 1V$ ,  $f_{SW} = 4MHz$   
Load Step Slew Rate =  $50A/\mu s$ , 0.1A to 10A  
220nH Inductor (Cyntec)  
2x10μF Capacitor (0603 Taido Yuden), 5x22μF Capacitor (0603 TDK)  
8x4.3μF Capacitor (Low ESL 0402 Murata)

**Figure 28. Dual-Phase Load Transient**

## 5. Revision History

Rev.	Date	Description
1.00	Apr 4, 2018	Removed "kit" and "ISL91302BEVAL1Z" throughout. Updated Figures 2, 9, 12, 13, 14, 15, 16, 25, 26, 27, 28 Page 6 - updated sections 2.2.3 and 2.2.4 Updated Bill of Materials on page 15. Updated Board layout images
0.00	Oct 31, 2017	Initial release

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