RENESAS

ISL91302B40-EVZ

User's Manual: Evaluation Board

Core Power Solutions

Rev.1.00   Aug 2019

ISL91302B40-EVZ
Evaluation Board

1. Overview

The ISL91302B40-EVZ platform allows quick evaluation of the ISL91302B high performance features, which is capable of providing a 4-phase single output. The output can deliver up to 5A continuous output current per phase, giving a total output of 20A. The ISL91302B uses the proprietary Renesas R5 modulator technology to maintain accurate voltage regulation, while providing excellent efficiency and transient response. It also supports the standard I^2C and SPI communication protocols, ideal for systems using a single-cell battery.

1.1 Key Features

- Small, compact design
- Supports both I^2C and SPI bus communication protocols
- Adjustable V_{OUT} and independent DVS control
- Real-time fault protection and monitor (OC, UV, OV, OT)
- Six layer board design optimized for thermal performance and efficiency
- Connectors, test points, and jumpers for easy measurements
- Built-in load transient circuit

1.2 Specifications

The board is designed to operate at the following operating conditions:

- Input voltage rating from 2.5V to 5.5V
- Programmable output voltage range of 0.3V to 2V
- 4-phase configuration with 5A maximum load current/phase
- 2MHz default switching frequency
- DVS slew rate of 3mV/μs
- Operating temperature range: -40°C to +85°C
- V_{OUT} = 0.6V

1.3 Related Literature

For a full list of related documents, visit our website:

- ISL91302B device page

1.4 Ordering Information

| Part Number	Description
ISL91302B40-EVZ	ISL91302B40-EVZ 4+0 evaluation board

1.5 Kit Contents

The evaluation kit contains:

- ISL91302B40-EVZ (Quad Phase) evaluation board
- Evaluation software
- Renesas mini USB I^{2}C dongle with USB cable (ISLUSBMINIEVAL1Z)
- All applicable documentation

1.6 Recommended Equipment

- 0V to 10V power supply with at least 10A current sourcing capability (VIN SUPPLY BIAS)
- 0V to 10V power supply with at least 1A current sourcing capability (VCC_6V SUPPLY BIAS)
- Electronic loads capable of sinking current up to 20A
- Digital multimeter
- 500MHz quad-trace oscilloscope
- Dual edge slew rate controllable signal generator
- Differential probe (for load transient current measurement)

1.7 Block Diagram

Figure 1. ISL91302B Block Diagram
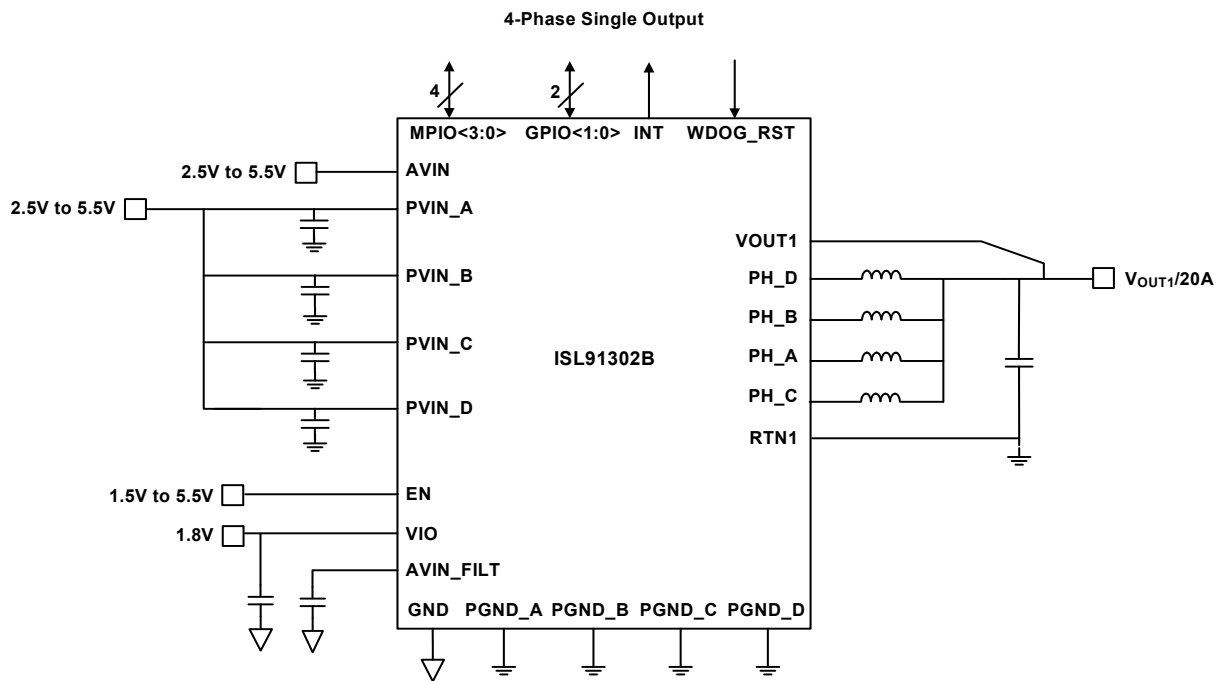
2. Functional Description

The ISL91302B40-EVZ evaluation board provides a simple platform to evaluate the feature-rich ISL91302B PMIC. It has a 0.6V output (default) after start-up that can be programmed by an I^{2}C or SPI. The evaluation board is functionally optimized for best performance, working harmoniously with the factory default tuning on the ISL91302B. The input power and load connections are provided through multi-pin connectors for high current operations.

The ISL91302B40-EVZ evaluation board is shown in Figure 9 on page 10. The evaluation board's key test points and jumpers are listed in Table 1. The ISL91302B's internal registers can be accessed by the I^{2}C or SPI through the on-board header J$_{24}$ (SPI) and J$_{60}$ (I^{2}C).

Table 1. Description of Important Test Points and Jumpers

Test Point	Description
J$_6$(+), J$_7$(-)	Header for connecting VIN supply
J$_{35}$(+), J$_{36}$(-)	Buck1 header for connecting external load
J$_3$	VIN Kelvin connection for efficiency measurements
J$_{15}$	Buck1 VOUT Kelvin connection for efficiency measurements
TP$_1$	VCC_6V SUPPLY for VIO LDO and load transient circuits
J$_{56}$	Buck1 driver input for load transient circuit
J$_{52}$	Load transient current sense, 1A/10mV
J$_{24}$	Header for connecting to SPI interface
J$_{60}$	Header for connecting to I^{2}C interface

The evaluation software GUI window for the ISL91302B is shown in Figure 8 on page 9. The schematic of the ISL91302B40-EVZ evaluation board is shown in Figure 13 on page 12. The PCB layout images for all layers are shown in Figures 16 through 23. The bill of materials of the ISL91302B40-EVZ is shown in "Bill of Materials" on page 15.

2.1 Operating Range

The V$_{IN}$ range of the board is 2.5V to 5.5V. The adjustable V$_{OUT}$ range for the ISL91302B40-EVZ is 0.3V to 2.0V. The I$_{OUT}$ range of the board is 0A to 5A per phase. The operating ambient temperature range is -40°C to +85°C.

2.2 Quick Start Guide

For the ISL91302B40-EVZ evaluation board, the default output voltage is set at 0.6V. No jumper configurations are needed to power up the part into its default state. All the settings and features are instead loaded through the one-time programmable memory inside the IC, after the minimum bias conditions are met. See "Setup Guide" on page 5 on how to power up the board for proper operation.

2.2.1   Setup Guide

(1)   Place scope probes on the VOUT test point and other test points of interest.

(2)   Connect a power supply to J_6 and J_7 (VIN SUPPLY), with a voltage setting between 2.5V and 5.5V. This biases the PVIN and AVIN pins, but does not initiate the startup sequence. The quiescent current should be less than 1mA.

(3)   Connect a second power supply to TP_1 (VCC_6V), with the voltage set to 6V. This biases the VIO and Chip Enable pins and the on-board load transient circuits. The ISL91302B boots up its internal reference, loads the default register settings, and then initiates a power-on sequence. The output should turn on in Pulse Skipping mode if no external load is present and V_{OUT1} should default to 0.6V.

(4)   During the startup sequence, the output should turn on with a 1.4ms delay from the Chip Enable pin going high.

(5)   To initiate shutdown, flip switch SW_1 to the disable position and the ISL91302B turns off the Buck.

2.2.2   I^{2}C and SPI Communication

The ISL91302B supports I^{2}C communication by default. A USB to I^{2}C communication dongle (ISLUSBMINIEVAL1Z) is included with each ISL91302B40-EVZ, and the Renesas Graphical User Interface (GUI) supports this tool across all operating systems.

To communicate with ISL91302B using I^{2}C, connect the Renesas USB to an I^{2}C dongle to J_{60}. Make sure R_{89} is present on the board, because it provides the pull-up from SPI_SS to the 1.8V VIO supply.

Note: For the SPI communication option using the GUI, contact Renesas support.

Figure 2. Communication Dongle Connection
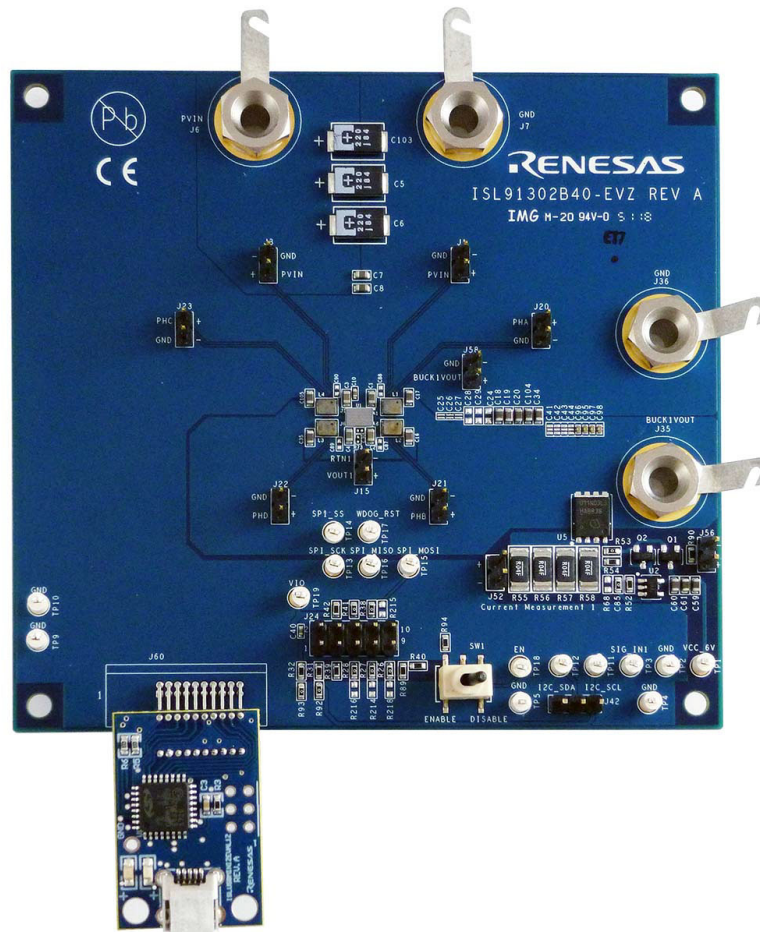
2.2.3   Efficiency Measurement

(1)   Connect a power supply at J_6 (VIN supply), with the voltage setting between 2.5V and 5.5V. Set its current limit high enough to support the maximum load current with additional headroom. If the power supply supports remote sense lines, use a Kelvin connection on J_3. Otherwise, connect a multimeter at J_3.

(2)   Apply 6V to TP_1 (VCC_6V) to initiate the startup sequence.

(3)   Turn on the electronic load at VOUT1. The connection should be made at J_{35} (VOUT1). Make sure the load current does not exceed 5A per phase, and the correct wire gauge is used when attaching the electronic load.

(4)   Measure the output voltage with a multimeter. The voltage should regulate within datasheet specification limits.

(5)   To determine efficiency, measure input and output voltages at the Kelvin sense test points (S+ and S-), which are located at J_3 (VIN SENSE) and J_{15} (BUCK1 SENSE). Measure the input and output currents from the VIN power supply and the electronic load. Calculate efficiency based on these measurements. For detailed setup information, refer to <u>Figure 11 on page 11</u>.

2.2.4   Load Transient Measurement

(1)   Go through the setup procedure (see <u>"Setup Guide" on page 5</u>). The ISL91302B40-EVZ should already be powered up with 2.5V to 5.5V at J_6 (VIN supply) and 6V at TP_1 (VCC_6V).

(2)   Connect a slew rate controllable signal generator to the transient load circuit input, J_{56} (TRANSIENT 1 PULSE GEN).

(3)   Program the signal generator to pulse mode, set the frequency to 100Hz, ON duration to 200µs, and signal amplitude from 0V to 2V. The load transient circuit starts to turn on when the input is ~2.6V. When in doubt, connect the signal generator output to an oscilloscope set to 1MΩ termination. The rising and falling time of the pulse should be conservatively slow, for example, 1µs.

(4)   Connect a differential probe to monitor load current across the sense resistors J_{52} (ISENSE1). The load current can be accurately converted to a voltage at 1A/10mV. Make sure the vertical scale of the oscilloscope is set properly to display the full amplitude of the load profile.

(5)   Connect a second differential probe at the VOUT sense points connected to the VOUT decoupling capacitors, J_{15} (BUCK1 SENSE).

(6)   Set the oscilloscope to measure the rise and fall times and maximum level of the load current. Slowly increase the signal generator amplitude and slew rate until desired load profile is a achieved. For detailed setup information, see <u>Figure 12 on page 11</u>.

J_52, Connect Differential Probe to "ISENSE1", 10mV/1A

J_56, Connect Signal Generator to "TRANSIENT 1 PULSE GEN"
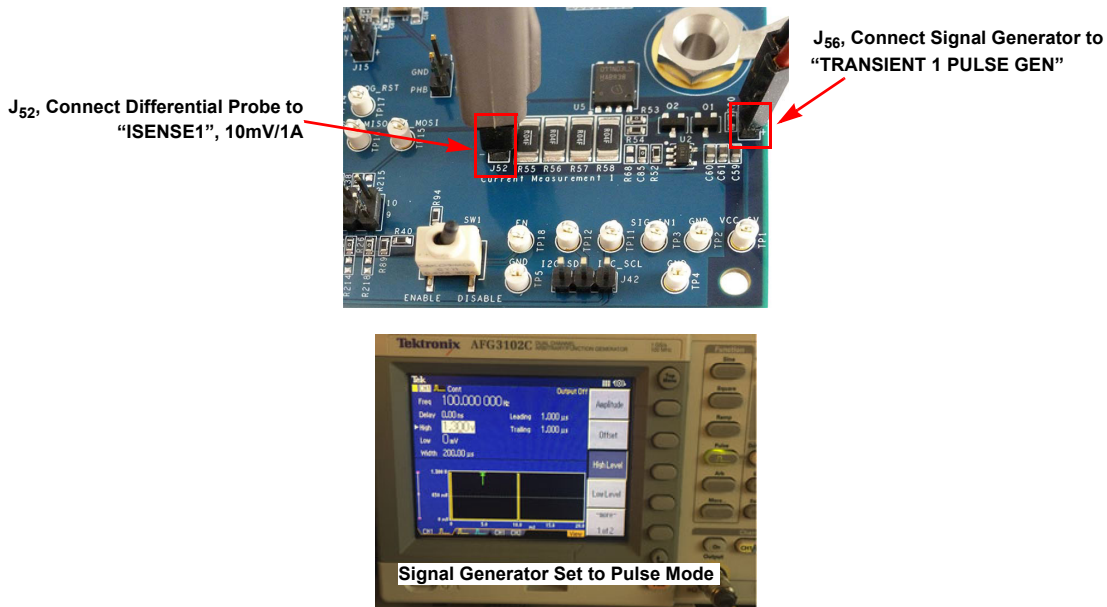
Signal Generator Set to Pulse Mode

Figure 3. BUCK1 Transient Load Connection Example

2.3   Evaluation Software Installation and Use

(1)   Extract the package and double-click AutoRun.exe. Follow the instructions to install the Multiphase PMIC I^{2}C Control Tool software.

(2)   Attach the USB-I^{2}C interface (ISLUSBMINIEVAL1Z) dongle to the computer using the supplied USB cable.

(3)   Attach the USB-I^{2}C interface dongle to J$_{60}$ on the ISL91302B40-EVZ evaluation board. Following the instructions in "Setup Guide" on page 5, connect the power supplies, DC load, and other test equipment to the ISL91302B40-EVZ evaluation board, then apply power.

(4)   Start the Multiphase PMIC Control Tool software. Select **Start > Programs > Renesas > Multiphase PMIC I2C Control Tool**.

(5)   Select **ISL91302B** from the Select Product drop down menu. Click the **Connect** button on the GUI to establish connection between GUI and the dongle . The LED on the dongle lights up. If a connection is not detected, the software shows a red X next to I2C Communication. Press **Reset** to reconnect the dongle.
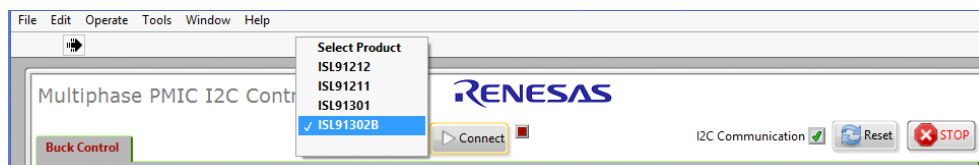

Figure 4. Product Selection Menu and I^{2}C Communication OK Indicator

(6)   After the evaluation software establishes a connection to the USB-I^{2}C interface dongle, the software loads a blank startup script by default and reads all the pertinent register values to show on screen.

(7)   You should see Buck1 enabled, and the default DVS0 values should be 0.6V. If no fault conditions occurred during the board power-up, all the fault indicators (UV, OV, and OC) should be clear rather than red.

(8) To change the output voltage, enter the desired value in voltages in the DVS0 control. There are also four default DVS values that are loaded as part of ISL91302B one time programmable memory space. You can go to any of them and activate a DVS command by clicking on the **DVS Pointer**.
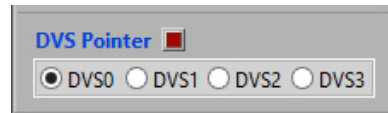
Figure 5. DVS Pointer Selection

(9) Changing the Max Voltage controls changes the internal feedback divider between ratios of 1x, 0.8x, and 0.6x. This changes the maximum output voltage the ISL91302B can support, with the maximum being 2V. Keep in mind the smallest DVS resolution the IC and the software can support is no less than the maximum voltage divided by 1023.

(10) After the evaluation software is up and running without hiccup, it polls all the registers at 2s intervals by default. You can disable this feature by clearing the **Continuous Read** option.

Figure 6. Continuous Read and Manual Read All Options

(11) The fault indicators self clear when the software reads the register through Continuous Read or the fault is removed. Three additional replica fault indicators (UV, OV, and OC) latch the faults so they clear only after you click **Push To Clear** in the event of a spurious fault condition.

Figure 7. Fault Indicators

Note: The default switching frequency of the ISL91302B is set to 2MHz and the slew rates for both DVS and power-up/down are set to 3mV/µs. These settings, along with many other features, are programmable only through OTP request or a Startup Script, and are not supported by the evaluation software. For more information, contact your local Renesas support.
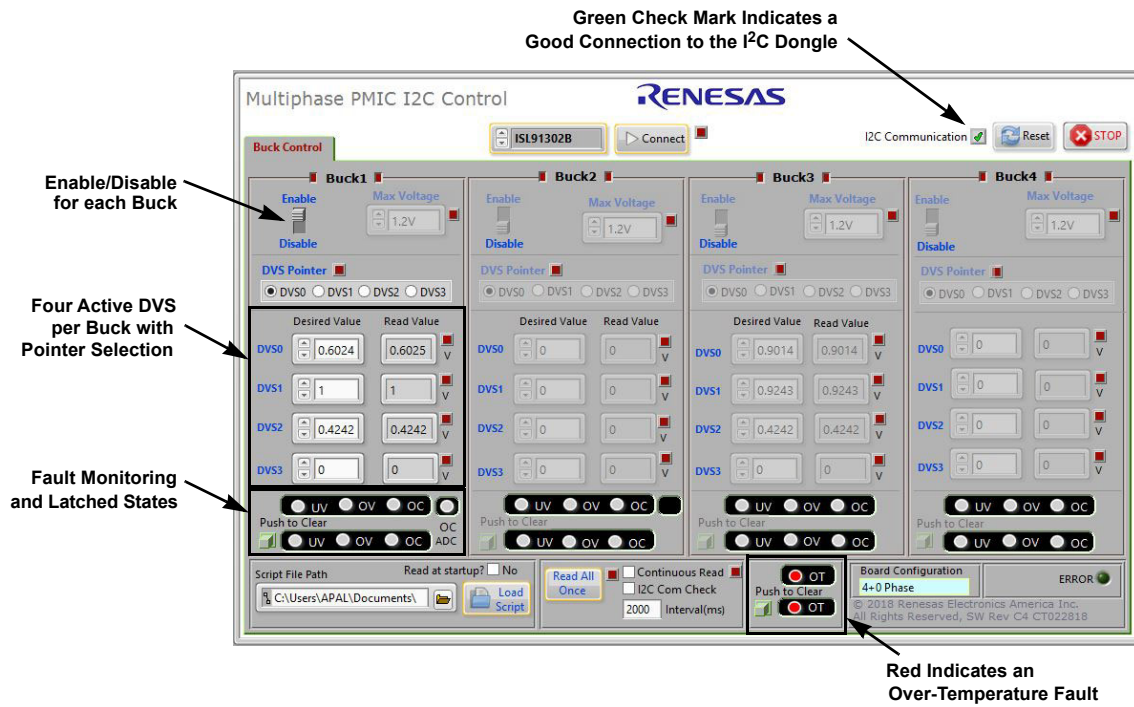
Figure 8. Multiphase PMIC (ISL91302B) I^{2}C Control Tool Interface

3.   PCB Layout Guidelines

The ISL91302B40-EVZ board is a 6-layer FR4 board. The main components are the ISL91302B, its passive filter components, test points, and connectors. A 220nH inductor is located close to each phase node of the ISL91302B, and 9x22µF plus 4x4.3µF capacitors are populated at the output of each inductor. PVIN is distributed using a power plane on an inner layer with a 10µF capacitor placed in close proximity to the PVIN and PGND balls of the power stage. In addition, a 10µF AVIN filter capacitor is placed next to the ISL91302B referenced to a quiet ground plane.

The PCB layout is a critical design step in making sure the designed converter works under optimum conditions. For the ISL91302B, the power loop is composed of the inductor, output capacitors, phase node, and PGND pins. Keep this loop as short as possible. The connecting traces among them should be direct, short, and wide. The ISL91302B's phase nodes are very noisy, so keep remote sense signals away from traces coming out of the phase nodes, and do not route them under the inductor in an adjacent layer. Place the input capacitor as close as possible to the PVIN and PGND pins. There should be a large unbroken ground plane that should connect all the decoupling capacitors together.

The heat of the ISL91302B is mainly dissipated through the GND and PHASE plane vias under the IC. To maximize thermal performance, use as much copper area as possible connecting to these vias. In addition, a solid ground plane is helpful for better EMI performance.

3.1   Key Layout Strategies

- Place input capacitors as close as possible to their respective PVIN and PGND pins to minimize parasitic loop inductance.
- Route phase nodes with short, wide traces and avoid any sensitive nodes.
- Route the remote sense lines directly to the load using small, low inductance capacitors at the load for bypassing.
- Output capacitors should be close to the inductors and have a low impedance path to the PGND pins.
- Keep digital and phase nodes from intersecting the AVIN_FILT, VOUT, and RTN lines.
- Create a PGND plane on the second layer of the PCB below the power components and bumps carrying high switching currents.
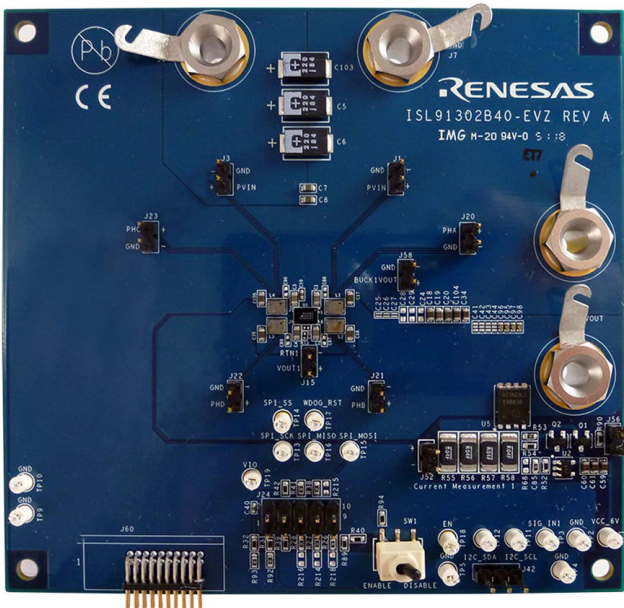
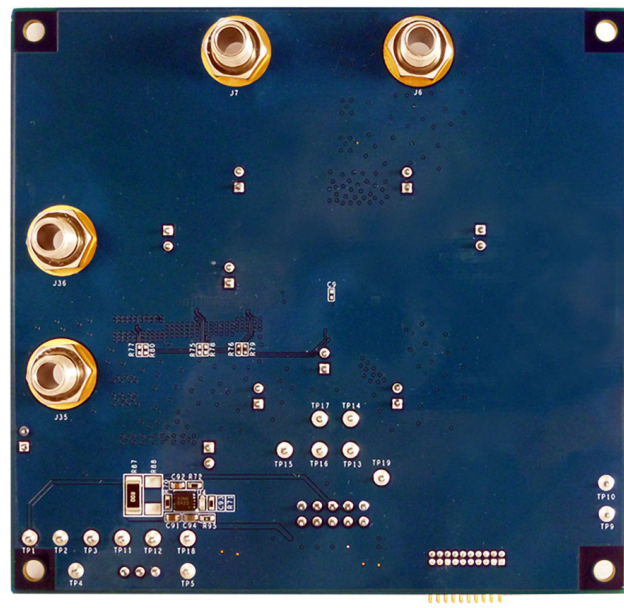## 3.2   Evaluation Board

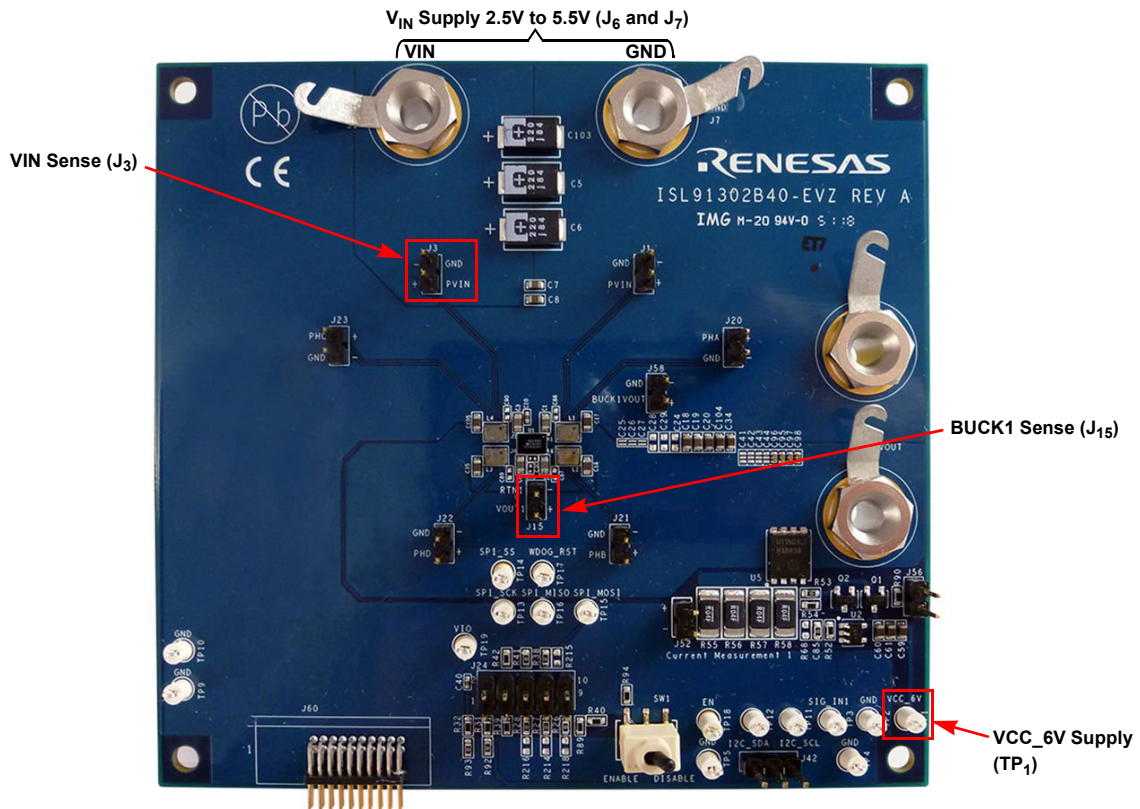Figure 9. ISL91302B40-EVZ Top View

Figure 10. ISL91302B40-EVZ Bottom View

Figure 11. ISL91302B40-EVZ Efficiency Measurement Connections
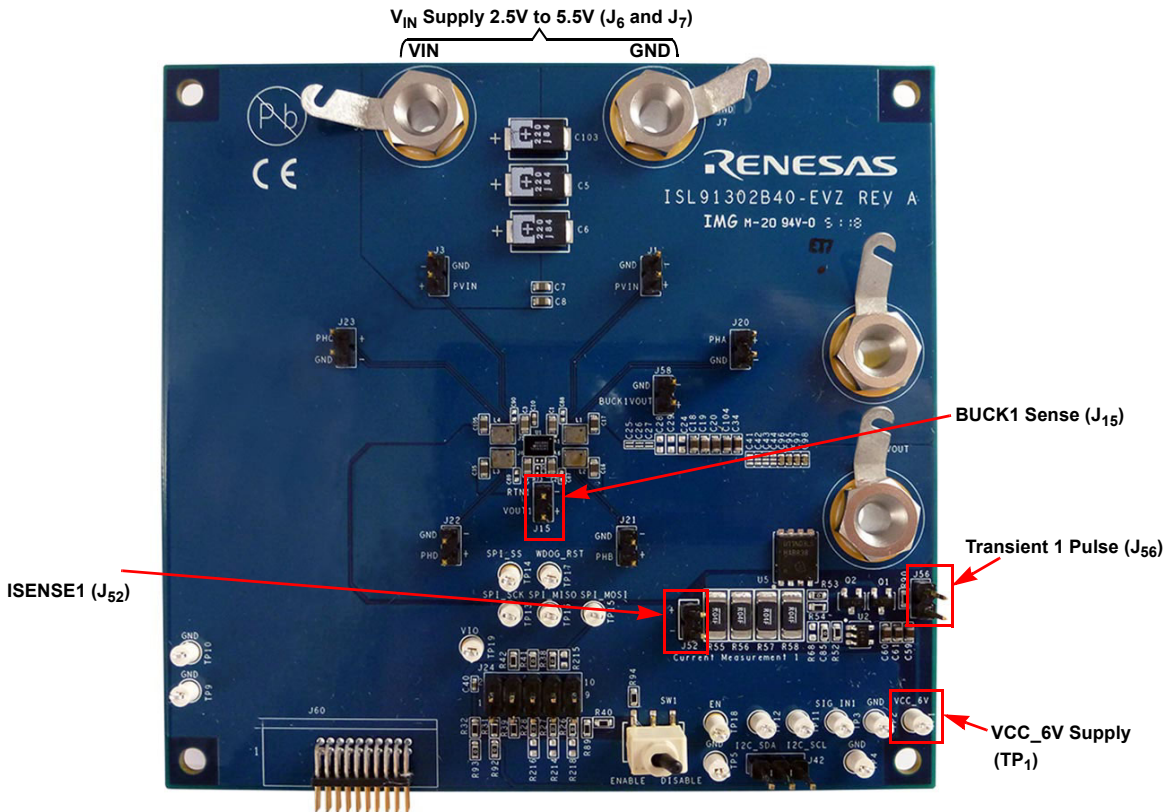

Figure 12. ISL91302B40-EVZ Load Transient Measurement Connections

3.3   Schematics

Figure 13. ISL91302B40-EVZ Schematic - Page 1

Transient Load Circuit for Buck 1

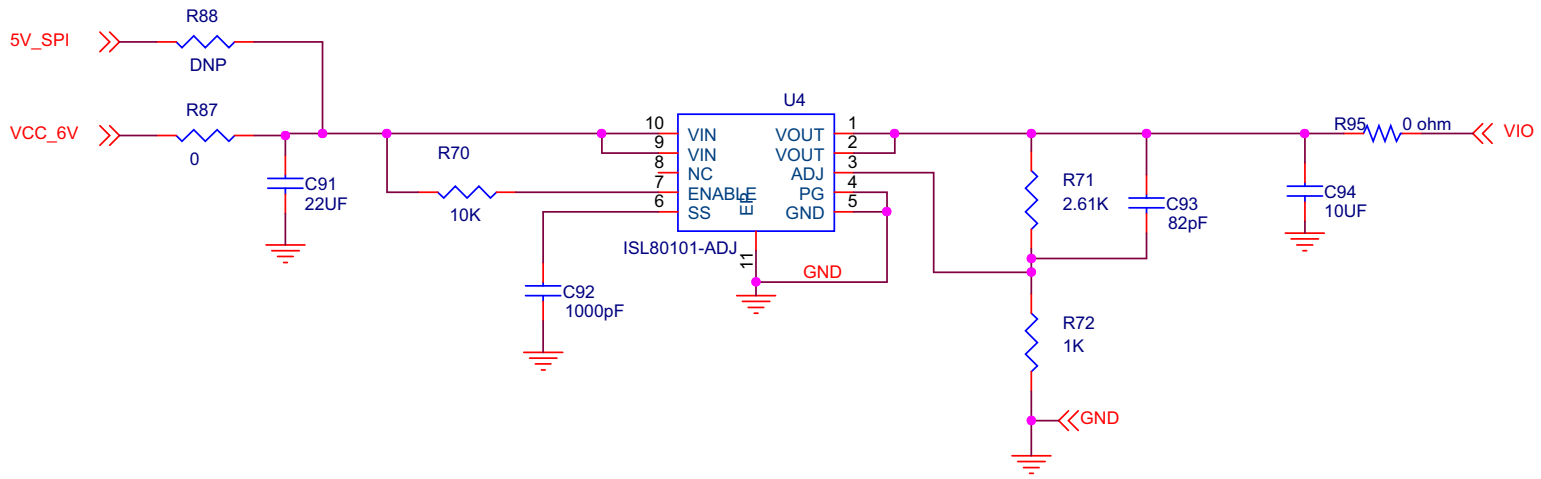**Figure 14. ISL91302B40-EVZ Schematic - Page 2**
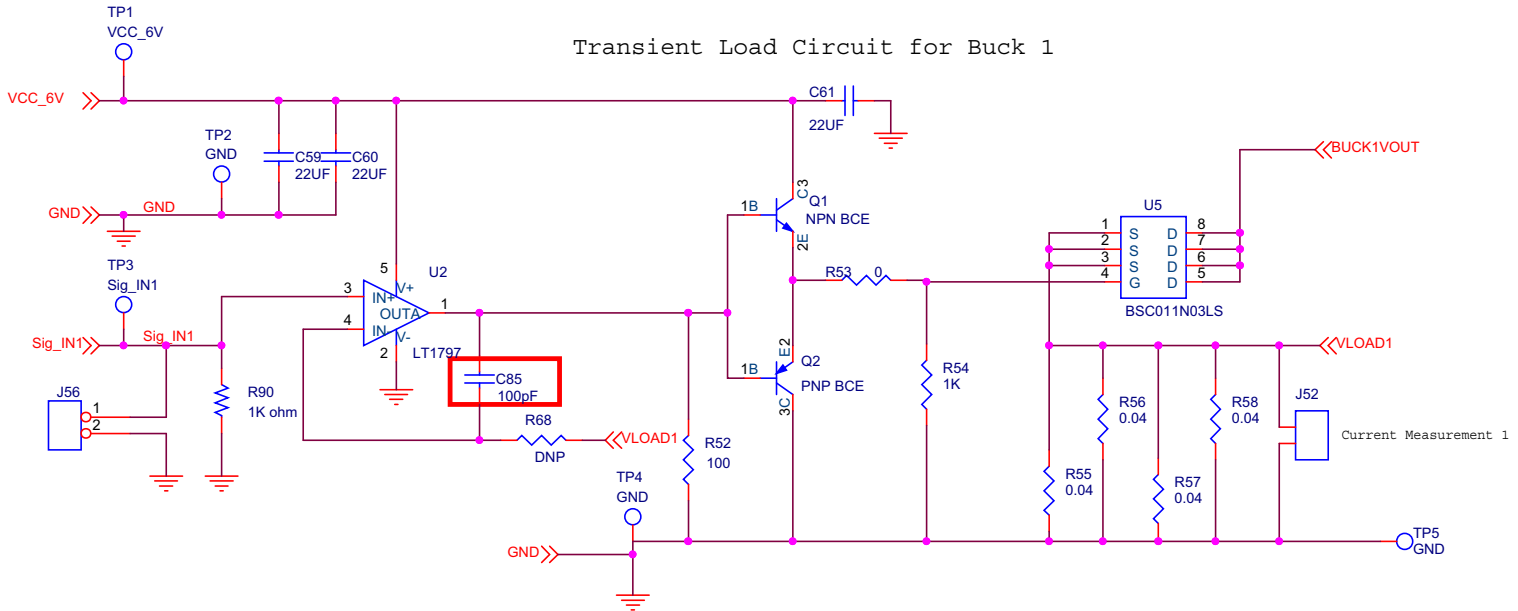
Magnitude of input signal sets load current.
To configure load transient circuit R68 = DNP, C85 = 0Ohm.

Ouput sense resistors for each rail.
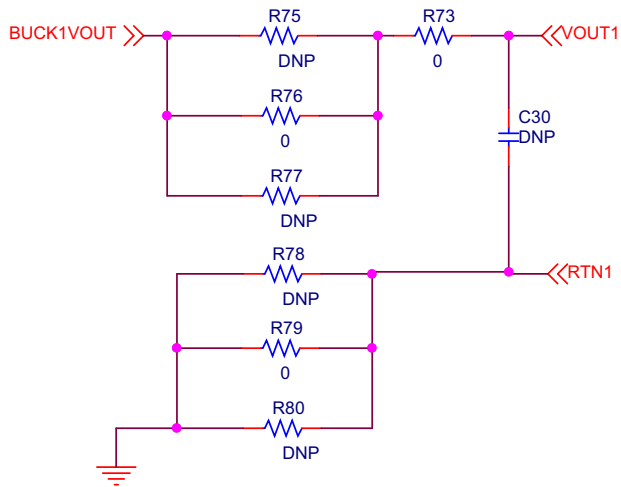
Figure 15. ISL91302B40-EVZ Schematic - Page 3

3.4 Bill of Materials

Qty	Reference Designatior — Top Components	Bottom Components	Description	Digi-Key PN	Manufacturer	Manufacturer Part Number
1		C93	82pF, NP0, 0603	587-4437-1-ND	Taiyo Yuden	QVS107CG820JCHT
1	C85		0Ω, 1/10W, 0603	P0.0GCT-ND	Panasonic	ERJ-3GEY0R00V
1		C92	1000pF, 50V, X7R, 0603	587-1445-1-ND	Taiyo Yuden	HMK107B7102KA-T
1	C40		1µF, 10V, X5R, 0402	587-1454-1-ND	Taiyo Yuden	LMK105BJ105KV-F
3	C96, C97, C98		3-terminal, 0402, 4.3V, 2.5V, X5R	n/a	Murata	NFM15PC435R0E3D
7	C1, C2, C3, C4, C7, C8	C94	10µF, 10V, X5R, 0603	587-3412-1-ND	Taiyo Yuden	LMK107BBJ106MAHT
1	C10		10µF, 10V, X5R, 0402	1276-1450-1-ND	Samsung Electronics	CL05A106MP5NUNC
13	C16, C17, C18, C19, C20, C34, C35, C59, C60, C61, C104, C105	C91	22µF, 10V, X5R, 0603	445-9077-1-ND	TDK	C1608X5R1A226M080AC
3	C5, C6, C103		220µF, 6.3V, Polymer Tant, D2 Case	P16625CT-ND	Panasonic	6TPE220MAP
1	R73		0Ω, 1/20W, 0201	P15979CT-ND	Panasonic	ERJ-1GN0R00C
2		R76, R79	0Ω, 1/10W, 0402	P0.0JCT-ND	Panasonic	ERJ-2GE0R00X
9	R26, R27, R28, R38, R41, R53, R92, R93, R95		0Ω, 1/10W, 0603	P0.0GCT-ND	Panasonic	ERJ-3GEY0R00V
1		R87	RES SMD 0.0Ω JUMPER 3/4W 2010	RMCF2010ZT0R00CT-ND	Stackpole	RMCF2010ZT0R00
4	R55, R56, R57, R58		0.04Ω, 1%, 1W, 2010	WSLF-.04CT-ND	Vishay	WSL2010R0400FEA18
1	R52,		100Ω, 1%, 1/10W, 0603	311-100HRCT-ND	Yageo	RC0603FR-07100RL
9	R31, R32, R39, R40, R42, R54, R89, R90, R94	R72	1.0kΩ, 1%, 1/10W, 0603	311-1.00KHRCT-ND	Yageo	RC0603FR-071KL
1		R71	2.61kΩ, 1%, 1/10W, 0603	311-2.61KHRCT-ND	Yageo	RC0603FR-072K61L
1		R70	10kΩ, 1%, 1/10W, 0603	311-10.0KHRCT-ND	Yageo	RC0603FR-0710KL
4	L1, L2, L3, L4		0.22µH, 9.6mΩ, 7Asat, 2520 Inductor	n/a	Cyntec	HMLB25201T-R22MSR-01
1	Q1		TRANS NPN 40V 0.2A SOT-23	MMBT3904FSCT-ND	Fairchild	MMBT3904
1	Q2		TRANS PNP 40V 0.2A SOT-23	MMBT3906FSCT-ND	Fairchild	MMBT3906
4	J6, J7, J35, J36		CONN BANANA JACK THREADED 12AWG	J10138-ND	Cinch Connectivity	108-0740-102

Qty	Reference Designatior		Description	Digi-Key PN	Manufacturer	Manufacturer Part Number
	Top Components	Bottom Components				
16	TP1, TP2, TP3, TP4, TP5, TP9, TP10, TP11, TP12, TP13, TP14, TP15, TP16, TP17, TP18, TP19		Conn-Gen, Compact Test Point, Vertical, White	36-5002-ND	Keystone	5002
10	J1, J3, J15, J20, J21, J22, J23, J52, J56, J58		2 Pin Header, 100 mil spacing	609-4434-ND	FCI	77311-118-02LF
1	J42		3 Pin Header, 100 mil spacing	952-1312-ND	Harwin	M22-2510305
1	J24		10 Pin Header, 100 mil spacing	952-2380-ND	FCI	67997-410HLF
1	J60		Right angle connector	952-1398-ND	Harwin Inc.	M50-3901042
1	SW1		SWITCH-TOGGLE, SMD, 6PIN, SPDT, 2POS, ON-NONE-ON, ROHS	CKN1784CT-ND	ITT Industries /C&K Division	GT11MSCBE
1	U1		ISL91302 6x9 0.4mm Pitch WLCSP	n/a	Renesas	ISL91302B
1	U2		IC OPAMP VFB 200MHZ RRO SOT23-5	296-32191-1-ND	Texas Instruments	OPA356AIDBVR
1		U4	IC REG LDO ADJ 1A 10DFN	ISL80101IRAJZ-TKCT-ND	Renesas	ISL80101IRAJZ
1	U5		MOSFET N-CH 30V 100A 8TDSON	BSC011N03LS	Infineon	BSC011N03LSCT-ND
5	C9, C87, C88, C89, C90	C9	Capacitor, 0402, DNP		any	any
6	C24, C25, C26, C27, C28, C29		Capacitor, 0204, DNP		any	any
2	C59, C63		Capacitor, 0603, DNP		any	any
2	C30, C39		Capacitor, 0201, DNP		any	any
4	C41, C42, C43, C44,		3-terminal, 0402, 9.1µF, 4V, X5R		Murata	NFM15PC915R0G3
9	R41	R75, R76, R78, R79, R81, R83, R85, R86	Resistor, 0603, DNP		any	any
1	R88		100Ω, 1%, 1/10W, 0603	P100HCT-ND	Panasonic	ERJ-3EKF1000V
1		R88	Resistor, 2010, DNP		any	any
	R68		Resistor DNP			

Note: Components highlighted in blue are DNP.
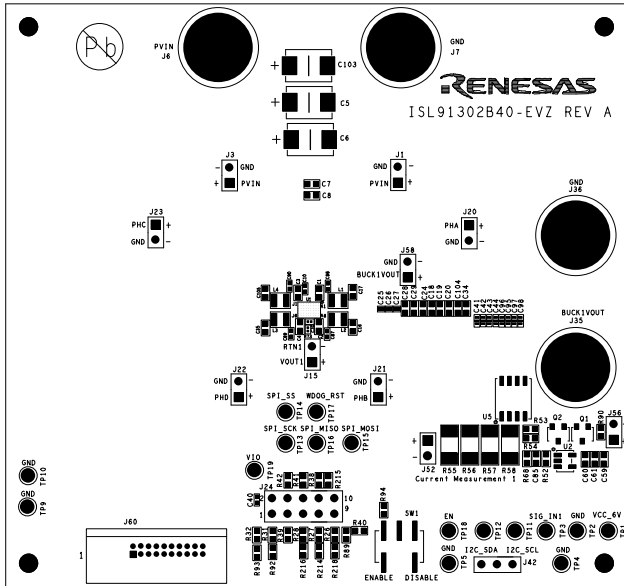
3.5   Board Layout
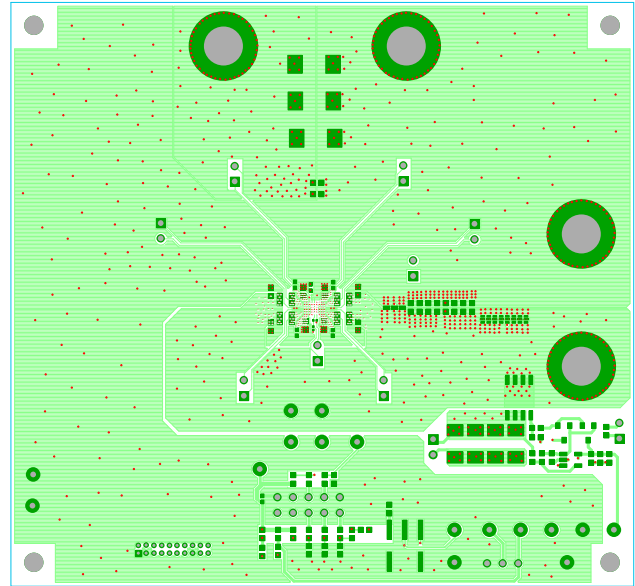

Figure 16. Top Silkscreen Layer
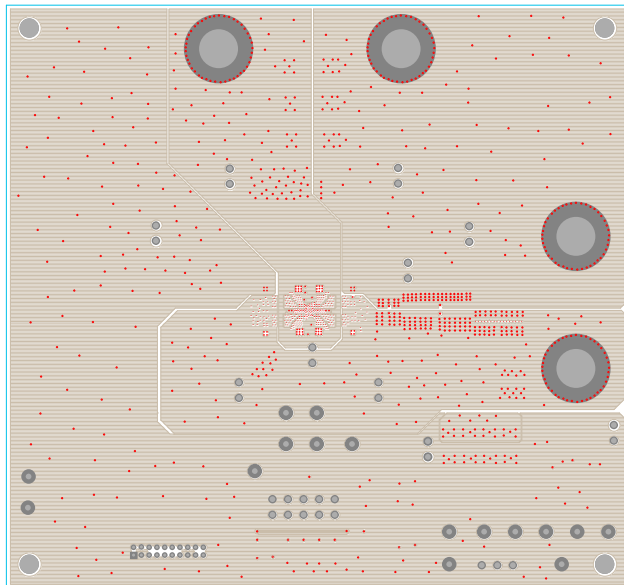

Figure 17. Top Layer
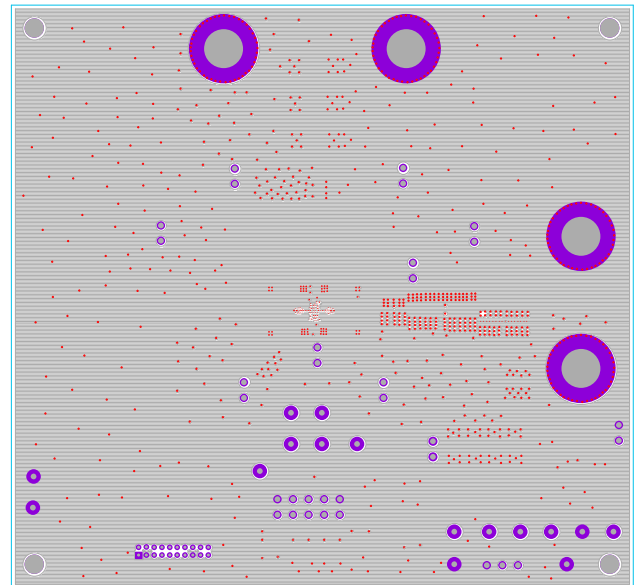

Figure 18. Layer 2 (PVIN Plane)
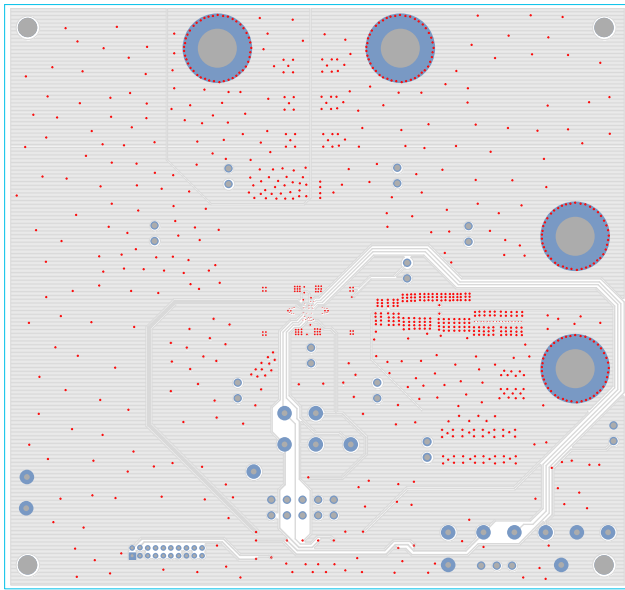

Figure 19. Layer 3 (GND Plane)

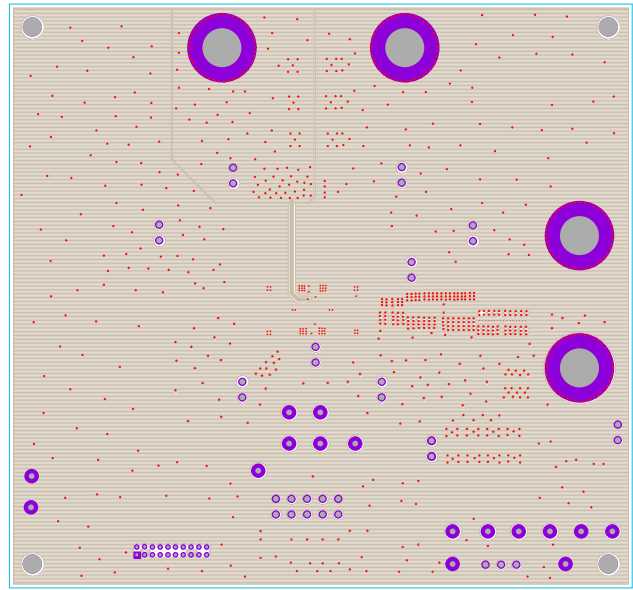**Figure 20. Layer 4 (IO Communications)**
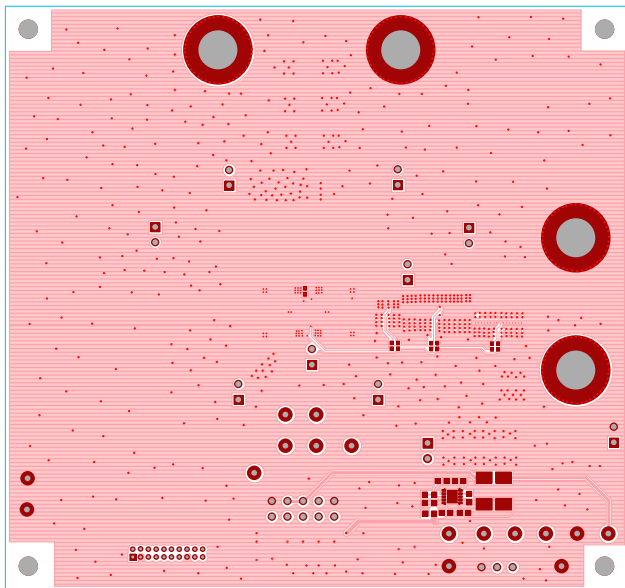

Figure 21. Layer 5 (GND Plane)

Figure 22. Bottom Layer (Remote Sense Lines)
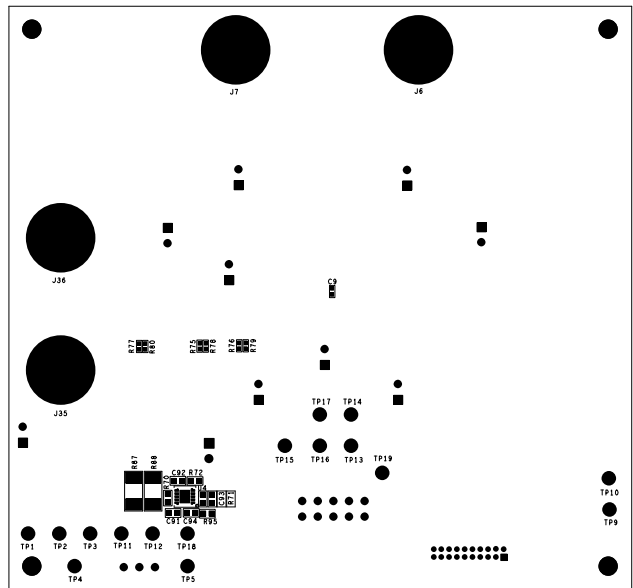

Figure 23. Bottom Silk Screen Layer
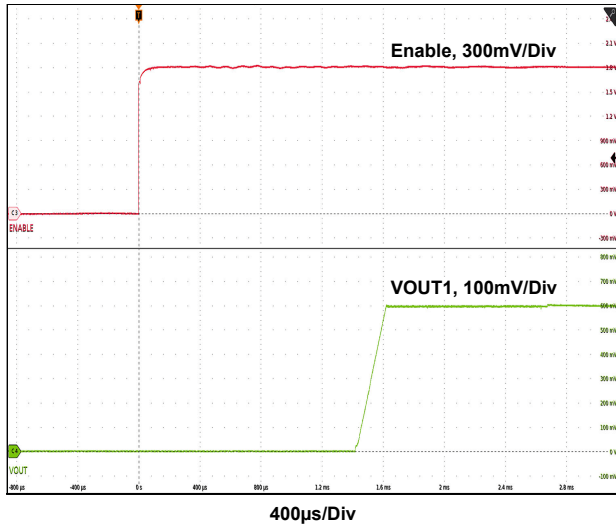
4. Typical Performance Curves

Figure 24. Startup by EN, V$_{OUT}$ = 0.6V
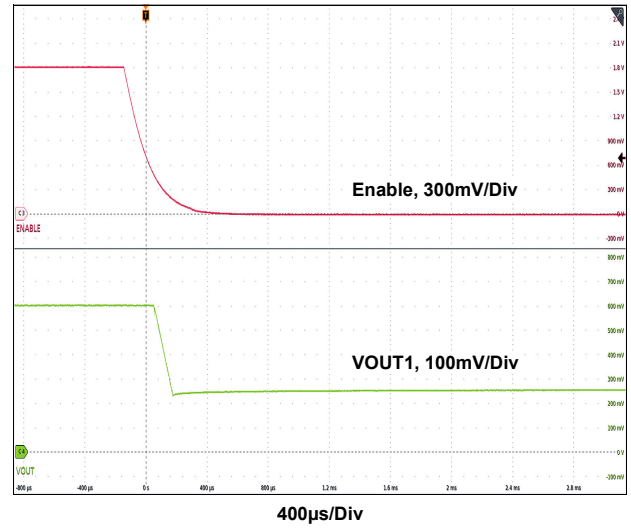

Figure 25. Shutdown by EN, V$_{OUT}$ = 0.6V

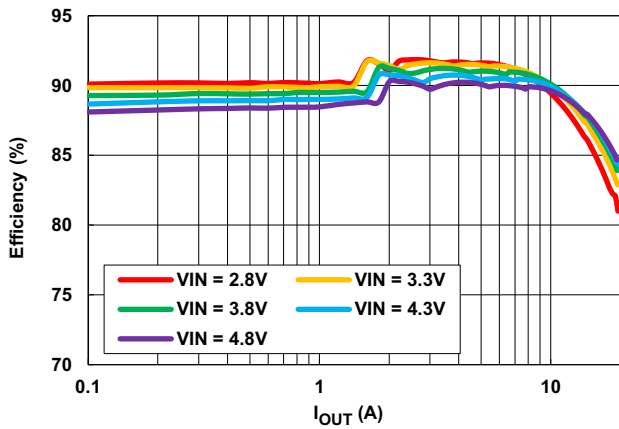**Figure 26. ISL91302B40-EVZ Efficiency, V$_{OUT}$ = 1V, f$_{SW}$ = 2MHz**
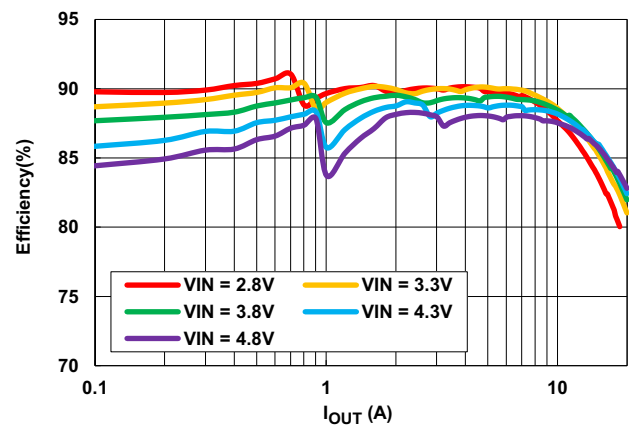
Figure 27. ISL91302B40-EVZ Efficiency, V$_{OUT}$ = 1V, f$_{SW}$ = 4MHz

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Figure 28. Load Transient
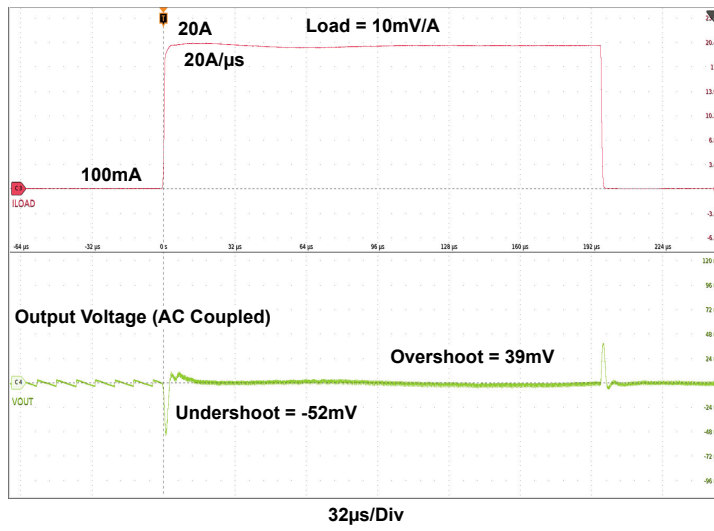
V_{IN} = 3.8V, V_{OUT} = 1V, f_{SW} = 2MHz   9x22µF Capacitor (0603 TDK)
Load Step Slew Rate = 20A/µs, 0.1A to 20A   4x4.3µF Capacitor (Low ESL 0402 Murata)
220nH Inductor (Cyntec)

5.   Revision History

Rev.	Date	Description
1.00	Aug 9, 2019	Updated default switching frequency from 4MHz to 2MHz. Updated power-up/down slew rate from 2.5mV/µs to 3mV/µs. Page 3 - Recommended Equipment - changed "Electronic loads capable of sinking current up to 10A" to Electronic loads capable of sinking current up to 20A". Updated board photos. Page 6 Efficiency Measurement - updated step 2. Page 15 - Bill of Materials updated. Updated Board Layout images. Page 19 - updated titles for Figures 26 and 27. Updated Figures 24, 25, and 28. Updated disclaimer.
0.00	Apr 5, 2018	Initial release

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(Rev.4.0-1 November 2017)

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