Description

The P9222-R-EVK Wireless Power Evaluation Board can be used to demonstrate the features and performance of the P9222-R 5W Wireless Power Receiver in low power 2.5W applications such as in earbuds charging cases. The P9222-R-EVK can also supply up to 5W power. IDT's P9235A-RB-EVK Evaluation Board or any other Qi certified transmitter can be used as the power transmitter for P9222-R-EVK evaluation board testing.

The P9222-R-EVK demonstrates a high-efficiency, turnkey reference design and is supported by comprehensive online, digital resources to significantly expedite the design-in effort and enable rapid prototyping. The printed circuit board (PCB) has four layers. The total solution area (excluding coil) is approximately 70 mm^2 out of which 37 mm^2 is occupied by the components. A small 30×30mm power receiver coil is used in the design to meet small form-factor device requirements.

Using the P9222-R Windows GUI and the P9222-R-EVK, customers can quickly customize operating parameters for their applications. Operating parameters such as foreign object detection (FOD) parameters can be configured by either writing to internal SRAM registers via the I2C interface, or by loading the user configuration generated by the P9222-R Windows GUI into an external EEPROM. The P9222-R-EVK has an on-board external EEPROM and connectors to plug-in the USB to an I2C programming dongle.

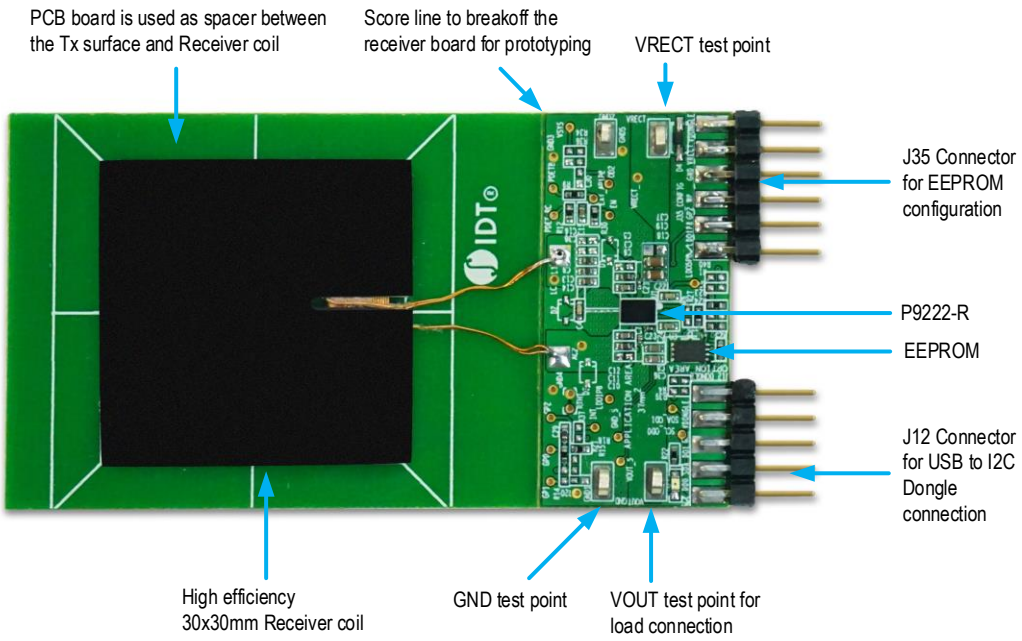
Features

- WPC1.2.4 Baseline Power Profile (5W) compatible
- Design optimized for low power (2.5W) applications with 30×30mm coil
- Approximately 70mm^2 solution area
- Schematic and layout files are available online
- Works with the P9222-R Windows GUI
- Easy configuration of design parameters through I2C interface
- On-board external EEPROM for flexible design parameter updates
- J12 connector compatible with the "USB-FTDI-V2-1" (FTDI) and ARM60 USB-to-I2C dongles
- 4-layer PCB with 1oz copper

Kit Contents

- P9222-R-EVK Evaluation board including the coil assembly

P9222-R-EVK MM EV Board (Top View)



Important Notes

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(i) delivered hardware or software

(ii) non-observance of instructions contained in this manual and in any other documentation provided to user, or

(iii) misuse, abuse, use under abnormal conditions, or alteration by anyone other than IDT.

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Restrictions in Use

IDT's P9222-R-EVK is designed for evaluation purpose only. It must not be used for module or mass production purposes.

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1. Setup

1.1 Required or Recommended User Equipment

The following additional lab equipment is required when using the kit:

- P9235A-RB-EVK Evaluation Board or any WPC certified transmitter.
- 5V DC power source or adapter that power transmitter
- Electronic load that can be connected to P9222-R-EVK

1.2 Required Software on Computer

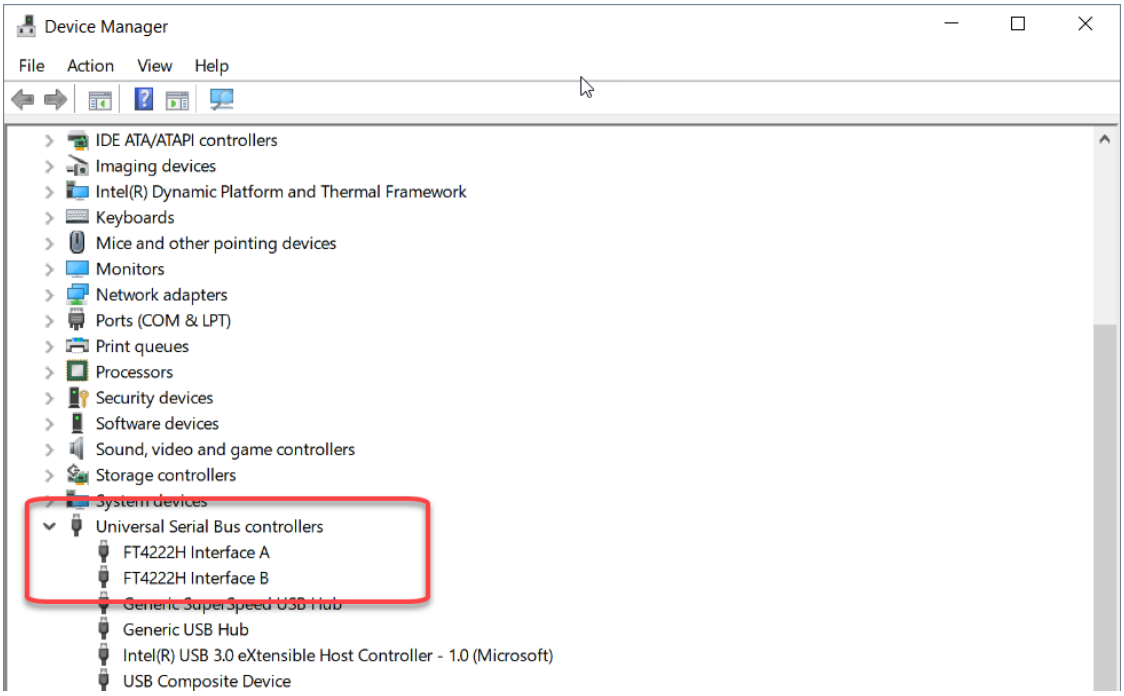
To download latest version of the *P9222-R Windows GUI* and USB drivers, visit the P9222-R-EVK webpage on the IDT website. The software provides an intuitive graphical user interface for reading and writing to P9222-R's SRAM registers. It can also be used to generate custom user configurations for the external EEPROM.

1.2.1 Software Installation

To install the software, complete the following procedure:

1. Do not connect the USB-to-I2C dongle before installing the software.
2. Run the downloaded *USB Drivers Setup* executable file and follow the user prompts to install the USB drivers.
3. After finishing the setup of the USB drivers, connect one of the USB-to-I2C dongles to the USB port. Wait for a few moments to let Windows® map the drivers for the dongle.
4. Open the Device Manager from the Windows control panel and check the devices listed under the "Universal Serial Bus controllers" section. "FT4222H Interface A" and "FT4222H Interface B" should appear in this section as shown in Figure 1.
5. Run the *P9222-R Setup* file and follow the user prompts to install the *P9222-R* software.

Figure 1. Windows Device Manager Display for Troubleshooting the USB Connection

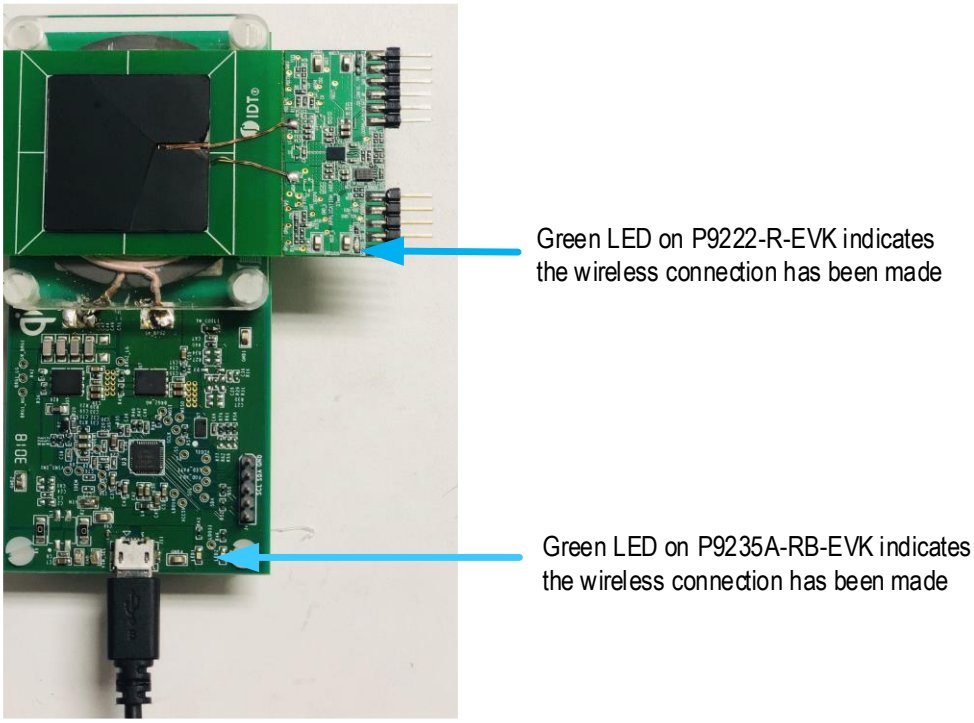


1.3 Kit Hardware Connections

To set up the kit as shown in Figure 2, complete the following procedure:

1. Set up the P9235A-RB-EVK Evaluation Board (or other transmitter board) according to the board's user manual and apply power.
2. Place the P9222-R-EVK Board on the transmitter coil surface with the coil back facing upwards. P9222-R-EVK PCB boards acts as a spacer between Tx surface and Rx coil.
3. Verify that the green LEDs on both kits are illuminated, which indicates that power transfer has been established.

Figure 2. Evaluation Kit Connections



1.4 Hardware Connections to Customize P9222-R-EVK Operating Parameters

The P9222-R firmware provides great flexibility to customize operating parameters for custom applications. Default values of the P9222-R operating parameters such as output voltage, FOD parameters, and current limit, are set in the firmware programmed into the internal one-time programmable (OTP) memory. Based on the end application, the P9222-R operating parameters can be configured by either writing to internal SRAM registers via the I2C interface, or by loading the user configuration generated by the P9222-R GUI into an external EEPROM.

To customize P9222-R-EVK operating parameters, a USB-to-I2C dongle must be connected to J12 Header and appropriate jumpers must be populated on J35 header.

Figure 3. USB-to-I2C Dongle Header of "USB-FTDI-V2-1" (FTDI) Dongle

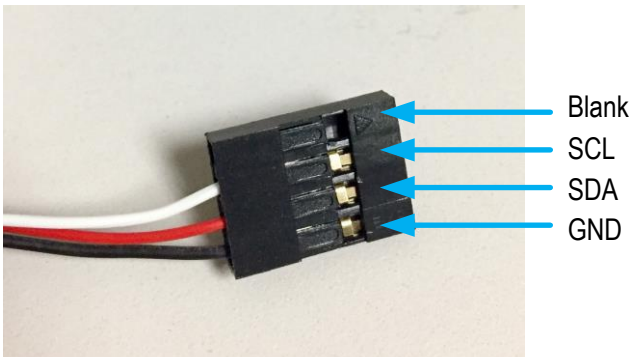


Figure 4. USB-to-I2C Dongle Connections to J12 Header

Table 1. J12 Header Pin Descriptions

Pin Number	Name	Type	Description
1	SCL	Input	I2C Interface Clock signal
2	SDA	Input /Output	I2C Interface Data signal
3	GND	Power	Ground reference
4	VDONGLE	Power	Dongle power supply from USB Dongle cable (optional)
5	/INT	Output	Interrupt Signal from P9222-R. Connect /INT to AP GPIO with PU (optional).

Figure 5. Jumper Connections on J35 Header

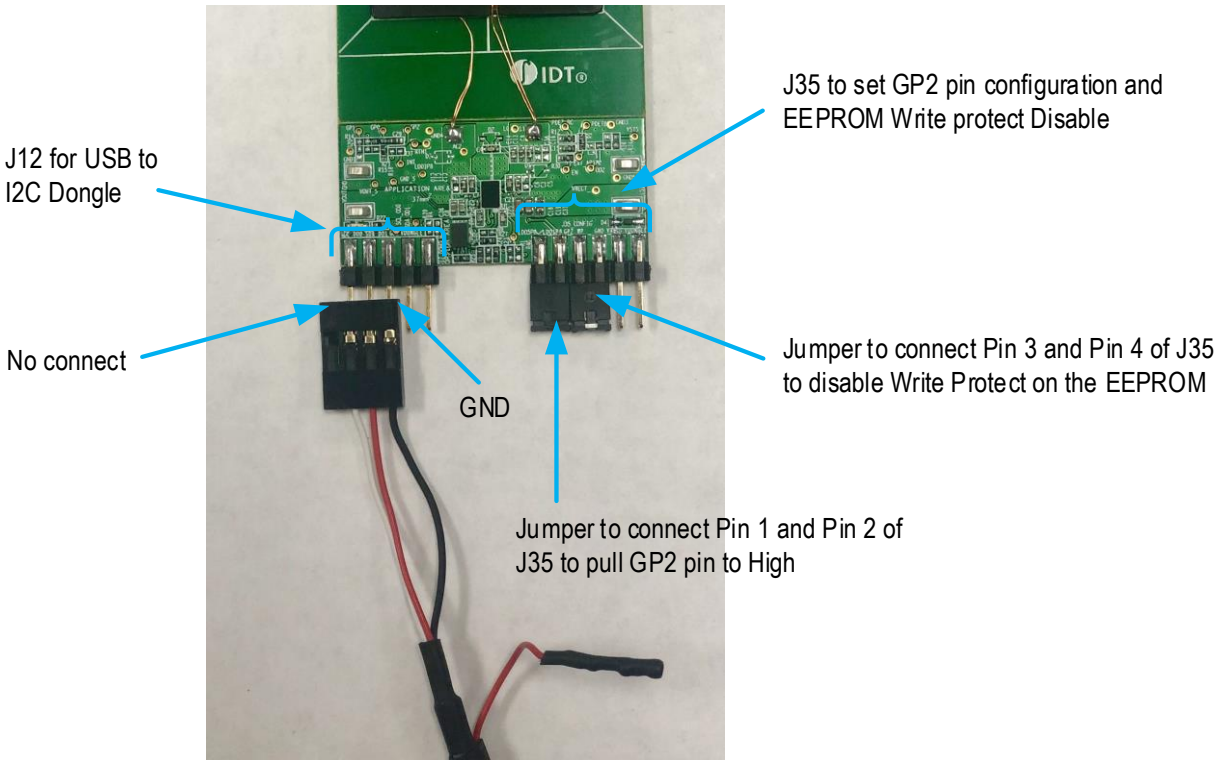


Table 2. J35 Header Pin Descriptions[a][b]

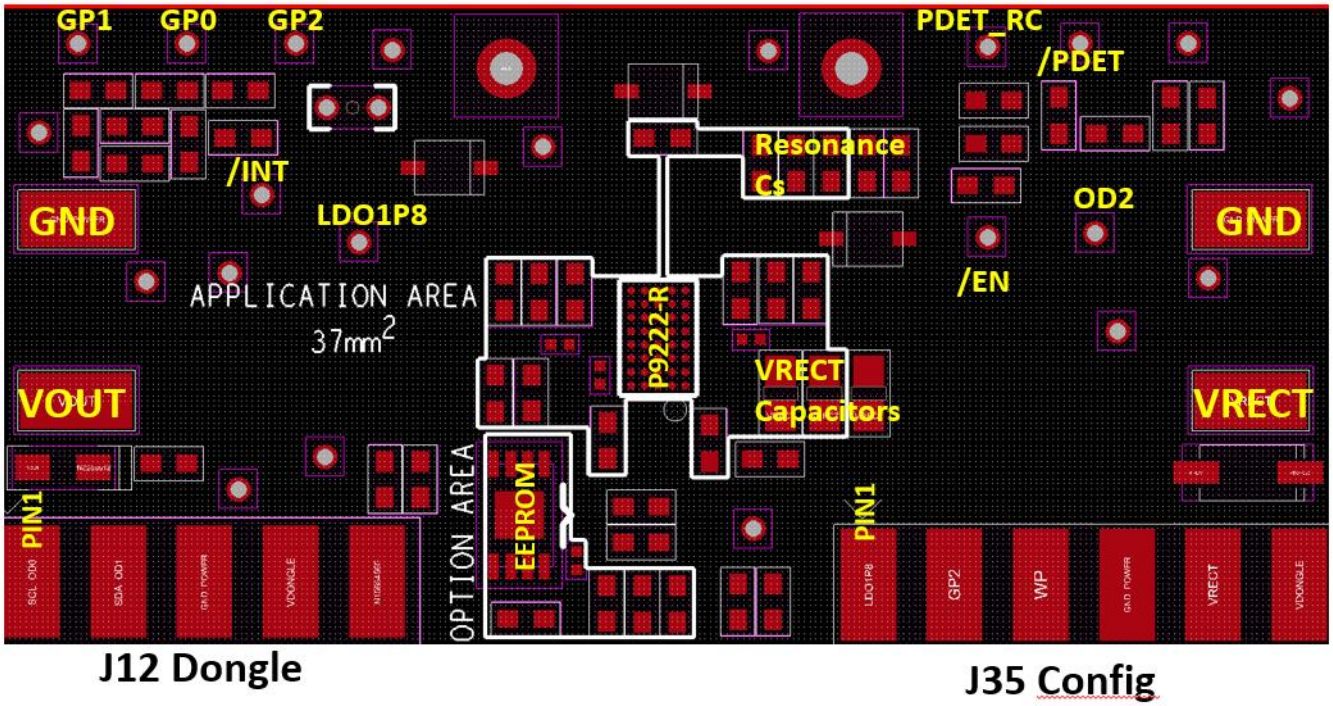
Pin Number	Name	Type	Description
1	LDO1P8	Power	LDO 1.8V IO power from P9222-R
2	GP2	Input	GPIO. If GP2 is low, the P9222-R loads the default configuration from internal OTP. If GP2 is high, the P9222-R loads the user configuration from an external EEPROM.
3	WP	Input	EEPROM Write Protection. If WP is high, EEPROM write protection is enabled. If WP is low, EEPROM write protection is disabled.
4	GND	Power	Ground reference
5	VRECT	Power	VRECT pin of P9222-R
6	VDONGLE	Power	Dongle power supply from USB-to-I2C dongle

[a] For loading a user configuration from the EEPROM, place the jumper header on J35 Pin 1 and Pin 2 before placing the P9222-R-EVK on the WPC TX pad. By connecting Pin 1 and Pin 2 of J35, the P9222-R GP2 GPIO pin is pulled high. If P9222-R GP2 is high during startup, the P9222-R becomes an I2C master during startup and loads 100 bytes of user configuration from the external EEPROM.

[b] Using the P9222-R GUI, a custom user configuration can be generated and loaded into the external EEPROM. Before programming the EEPROM, place the jumper header on Pin 3 and Pin 4 of the J35 header to disable EEPROM Write Protection. A new configuration will be effective after the P9222-R-EVK is power cycled and GP2 pin of the P9222-R is pulled high.

1.5 Test Point Placement for Advanced Evaluation

Figure 6. P9222-R-EVK Test Point Placement



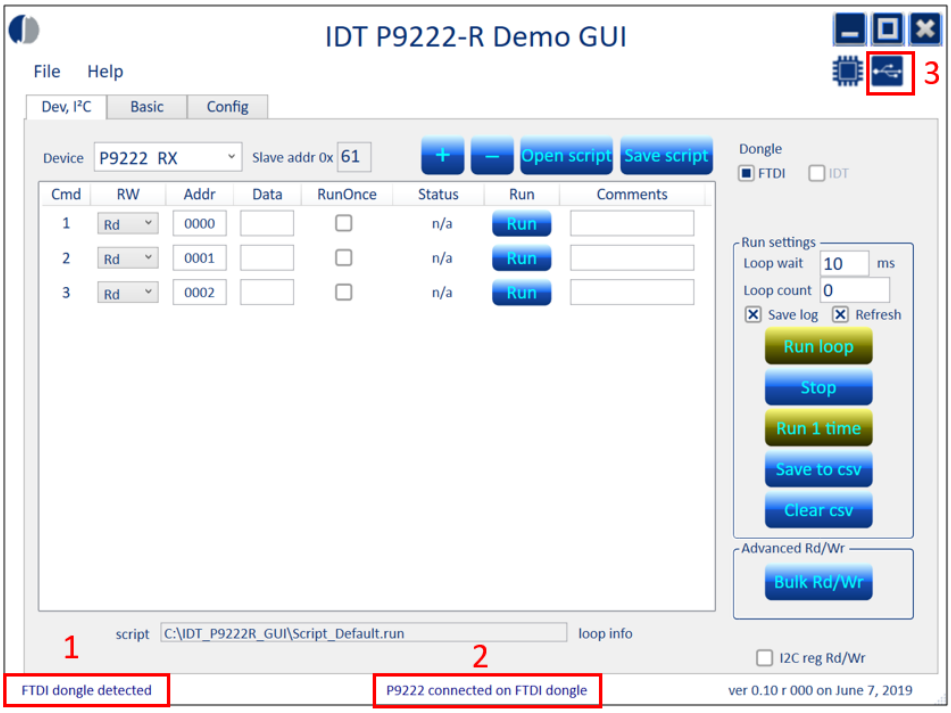
2. Connecting P9222-R-EVK to P9222-R Windows GUI

Connect the USB-to-I2C dongle to the computer USB port and attach the USB-to-I2C dongle header to the P9222-R-EVK J12 connector bridge as shown in Figure 4. The dongle should only be plugged-in in one direction extending away from the P9222-R-EVK PCB.

1. Make sure that latest USB drivers and P9222-R Windows GUI are installed (from the P9222-R-EVK webpage).
2. Place the IDTP9222-R EVK on the WPC TX, or apply 5V DC from any GND connection to the Vrect test point without placing the P9222-R-EVK on the transmitter.
3. Open the P9222-R Windows GUI program from the start menu.
4. If the IDT ARM60 Dongle is available, check the IDT box. If FTDI Dongle is available, check the FTDI box.

   The GUI launches and shows the connection status of the USB-to-I2C Dongle and P9222-R connection.

Figure 7. Initial Screen of P9222-R Windows GUI with FTDI Dongle



Notes:

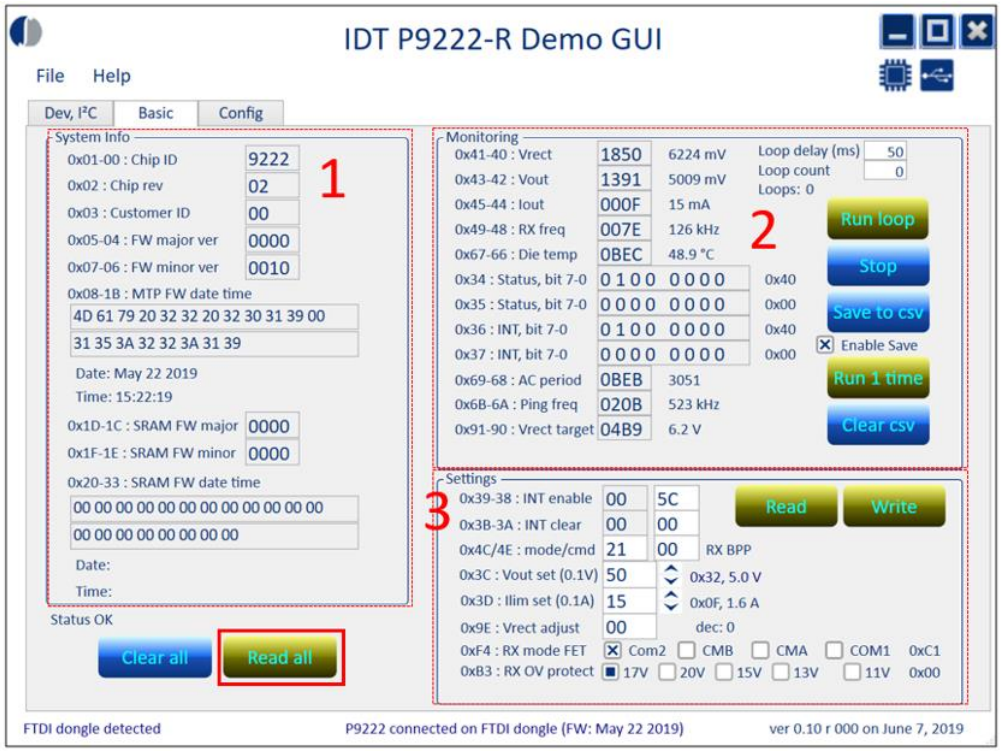
- A Dongle detection message will be displayed when a USB-to-Bridge dongle is connected to the PC. If it is not displayed, unplug and plug USB dongle again.
- A P9222 connection message will be displayed when the P9222-R EVK is powered on the WPC TX pad and connected to the USB dongle. If it is not displayed, click the USB Icon in #3 and close, re-open GUI (see Figure 7).

The Command window allows user to read and write the registers one time, continuously, and save the result in a csv file.

1. Select the mode (Read or Write) and enter the target register address you want to access and click the run mode setting (see Figure 8).

   For detailed register information, refer to Rx register tables. The screen in Figure 8 shows the BASIC tab of the GUI.
2. Click READ ALL to see System information, operation status, and default FW configuration setting.

Figure 8. P9222-R Basic System Information and Settings



Command window information:

- **System Info in section 1** shows the P9222-R FW version and IC information.
- **Monitoring in section 2** updates the P9222-R system operation information during wireless charging. Vrect voltage, Vout voltage, Output current, Operating frequency, Die temperature, System status, and Interrupt status are updated. If "Run loop" is clicked, status information will be updated in regular time base set in loop delay and counts.
- **Settings in section 3** shows the system configuration value. Interrupt enable/clear, operation mode, Vout voltage, ILim current limit, Vrect adjust, Rx modulation FET selection, and Overvoltage setting are configurable. If the "Write" button is clicked after setting the configuration value in section 3, a new value will be applied automatically in next operating cycle by the P9222-R FW.

2.1 Making EEPROM Configuration Changes for the First Time

If the EEPROM is blank, download the "Golden EEPROM configuration" from the P9222-R-EVK webpage and use it as a starting point.

3. Customizing P9222-R_EVK Operating Parameters

3.1 LDO Output Voltage (VOUT) Configuration

The default VOUT voltage of the P9222-R-EVK is 5.0V. The user can change the default Vout voltage in accordance with specific user design requirements and store the modified configuration in the external EEPROM, or an external Applications Processor (AP) can adjust VOUT voltage continuously via the I2C interface. In addition, an external MCU can continuously read the battery voltage and change VOUT to lower the losses in the battery charger to optimize the total system efficiency. The P9222-R configurable Vout voltage range is from 3.5V to 12V.

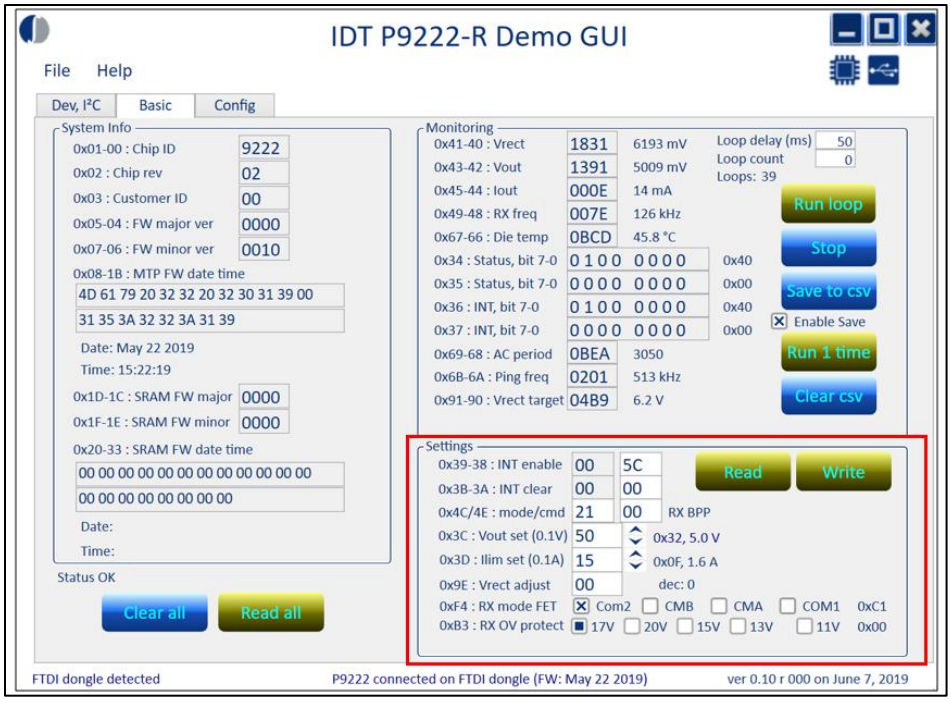
3.1.1 VOUT Adjustment via the I2C Interface

The P9222-R output voltage can be changed by writing to the Vout_Set register (0x3C). The P9222-R firmware reads the internal register value in regular time base and updates the Vout voltage. The output voltage can be incremented in steps of 100mV.

$$Output\ Voltage\ (VOUT) = \text{Decimal Value of 0x3C register} * 0.1\ (\text{V}) \qquad \textbf{Equation 1}$$

To change the 0x3C register using the P9222-R Windows GUI, go to the VOUT set box in the GUI "Basic" tab (see Figure 9).

Figure 9. Writing to the Vout_Set Register using P9222-R Windows GUI



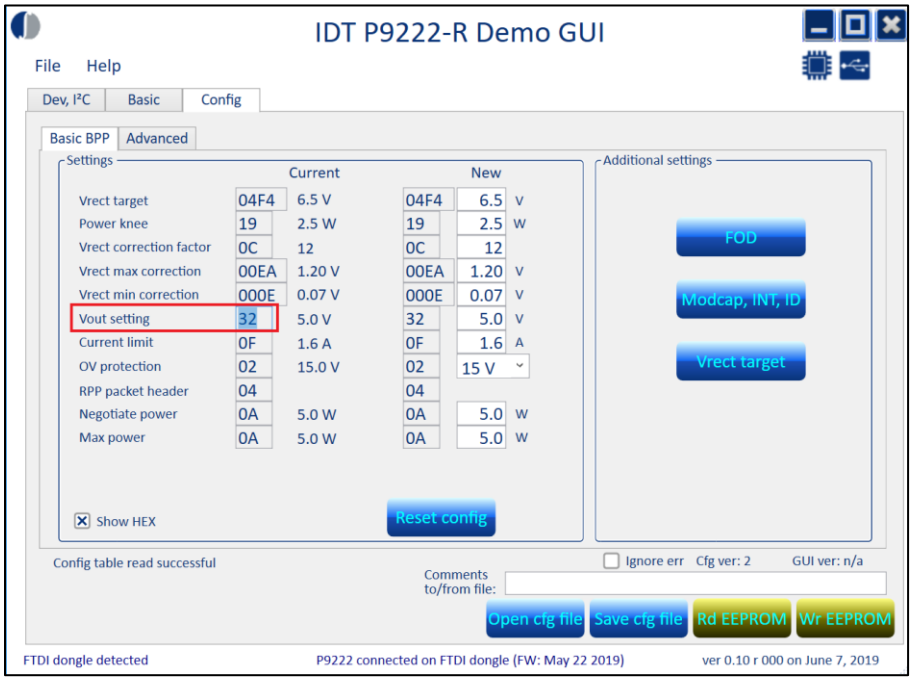
3.1.2 VOUT Configuration Change Using an External EEPROM

The default output voltage can be configured by writing a configuration file into the external EEPROM. The configuration file can be generated using the P9222-R Windows GUI. To generate a new configuration file using the P9222-R Windows GUI:

1. Place the receiver with the P9222-R-EVK on the WPC transmitter or apply 5V from an external power supply on the VRECT node.
2. Launch the P9222-R GUI, go to the "Config" tab, and then click on the "Rd EEPROM" button. The current EEPROM configuration values will be displayed. If the EEPROM is blank, download the "Golden EEPROM configuration" from the P9222-R-EVK webpage and use it as a starting point.
3. Enter a new VOUT value and generate a new configuration by clicking on "Save cfg file".
4. The Configuration can also be directly written to the external EEPROM by clicking "Wr EEPROM".

   Note: Write Protect on the EEPROM must be disabled before writing to the EEPROM.
5. After saving the new configuration into the EEPROM, the P9222-R must be power cycled for the output voltage to change to the new value.

Figure 10. Changing the Default VOUT Value using the P9222-R Windows GUI



3.2 Current Limit (ILIM) Configuration

The current limit threshold value is used to limit the output current of main LDO on the VOUT pin. If the output current reaches the target limit value, the VOUT voltage level will decrease due to the current limit setting if the output load is over the current limit level. The default ILIM value of the P9222-R-EVK is 1.6A. The user can change the default current limit value in accordance with specific user design requirements and store the modified configuration into an external EEPROM. In addition, after the P9222-R enters the power transfer phase, an external AP can adjust the ILIM value by writing to the ILIM_Set register (0x3D) via the I2C interface. The P9222-R firmware reads the internal register value in regular time base and updates the current limit value. The current limit can be incremented in steps of 100mA.

$$Current\ Limit\ (ILIM) = \text{Decimal Value of 0x3D register} * 0.1\ (A) \qquad \textbf{Equation 2}$$

The default Current Limit value can be configured by writing a configuration file into the external EEPROM. The configuration file can be generated using the P9222-R Windows GUI. For information on how the configuration file can be generated using the P9222-R Windows GUI, see "VOUT Configuration Change Using an External EEPROM."

3.3 Overvoltage (OV) Protection Configuration

The wireless charging receivers are vulnerable to external high voltage condition (> 20V) caused by coupling factor changes or other abnormal behavior of rogue wireless power transmitters. The overvoltage protection function should be carefully configured to protect the receiver from worst cases. The overvoltage protection limit sets the maximum allowable Vrect voltage. If Vrect reaches the voltage limit (default OV voltage is 15V), the P9222-R will do the following:

1. Turn on the internal clamping circuit
2. Enable an additional DC load when Vrect reaches 90% of the set level
3. Send an End Power Transfer packet (OV) to TX

The default OV protection limit value can be configured by writing a configuration file into the external EEPROM. The configuration file can be generated using the P9222-R Windows GUI. For information on how the configuration file can be generated using the P9222-R Windows GUI, see "VOUT Configuration Change Using an External EEPROM."

In addition, an external AP can adjust overvoltage protection limit by writing to the OV Set register (0x4C) via the I2C interface.

3.4 Configuring FOD Parameters

FOD parameters consist of various sections. Each section is divided by output current and consists of gain and offset to compensate for Rx internal power loss. Each section is also adjusted for Reported Rx power. The following comprises the mA ranges for the FOD sections:

- FOD section [0] is from 0mA to 191mA
- FOD section [1] is from 192mA to 351mA
- FOD section [2] is from 352mA to 511mA
- FOD section [3] is from 512mA to 671mA
- FOD section [4] is from 672mA to 819mA
- FOD section [5] is more than 820mA

The formula of Rx Reported Power is:

$$Rx\ Reported\ Power[0..5] = Power(Rx\ delivered\ power) * FOD\ Gain[0 \dots 5] + Offset[0..5] \qquad \textbf{Equation 3}$$

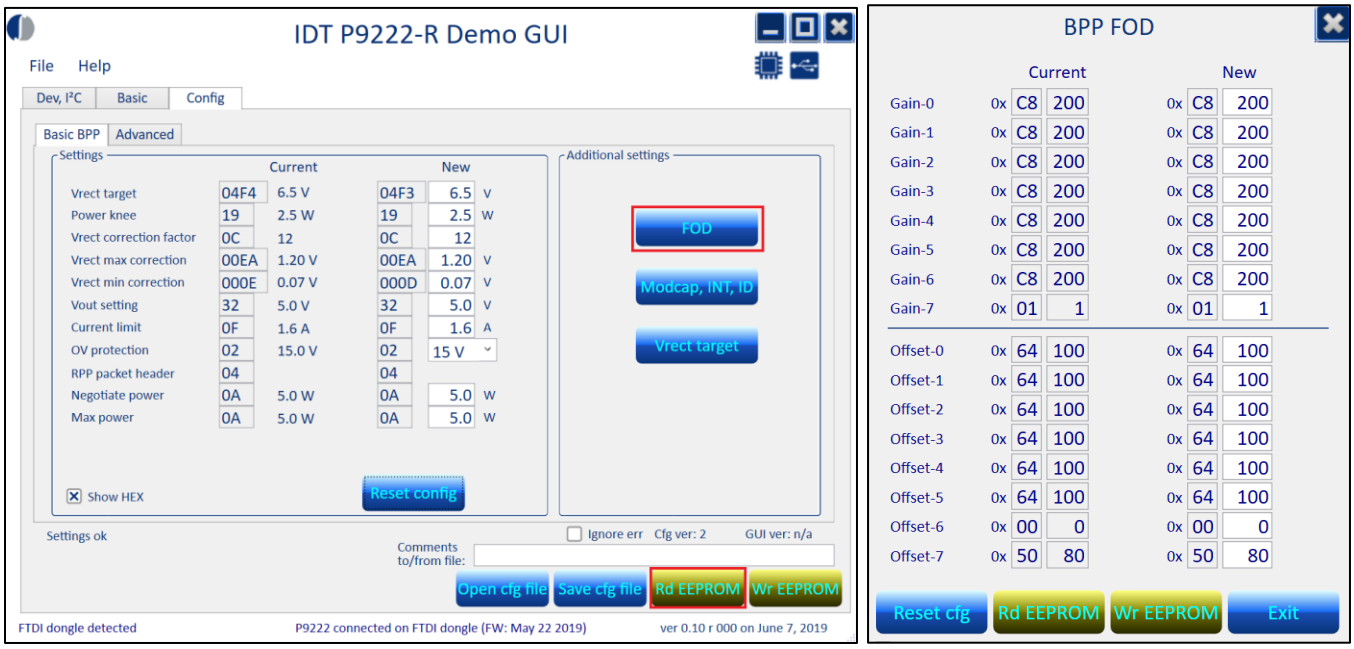
Place the P9222-R-EVK on the Nok9 FOD transmitter. Ramp the current on the output of the P9222-R-EVK in steps of 50mA to 100mA, and monitor power difference between the Nok9 transmitted power and the receiver reported power value. The difference should be within 0-350mW. If the difference exceeds -350mW, adjust the FOD gain or FOD offset of that particular output current section in order to bring the difference back into the 0-350mW range. The AP can modify the FOD gain and FOD offset by writing to the Foreign Object Detection Registers (0x70-0x7E). In the final product, the AP can use the VRECTON interrupt or battery charger interrupt as a trigger to update the FOD registers.

The default values of the FOD registers can also be configured by writing a configuration file into the external EEPROM. To generate the configuration file using the P9222-R Windows GUI:

1. Place the receiver with the P9222-R onto the WPC transmitter or apply 5V from an external power supply on the VRECT node.
2. Launch the P9222-R GUI, go to the "Config" tab, click the "Rd EEPROM" button, and then click the "FOD" button. A new popup window with the current FOD values stored in the external EEPROM will be displayed.
3. Enter new FOD values and click on the "Save cfg file" to generate a new configuration. The configuration can also be directly written into the external EEPROM by clicking the "Wr EEPROM" button.

   Note: The Write Protect function on the EEPROM must be disabled before writing to the EEPROM.

Figure 11. Changing the Default FOD Registers using the P9222-R Windows GUI



3.4.1 Modulation Capacitor and Interrupt Enables

The P9222-R sends the communication packets to the transmitter using ASK modulation of the coil voltage. For ASK modulation, the P9222-R switches the capacitors on and off that are on the COM1, COM2, CMA, and CMB pins using internal MOSFETs. By default, the P9222-R switches only the MOSFETs on the COM1 and COM2 pins. ASK modulation depth can be increased by enabling the switches on the CMA and CMB pins. Measure the modulation depth on the transmitter demodulation circuitry, and if too small, adjust the ASK modulation depth by enabling the CMA and CMB switches. Modulation depth can also be increased by increasing the capacitor value. The AP can also change the ASK modulation depth by writing to the ASK modulation depth Registers (0xF4).

Using the /INT pin, the P9222-R can interrupt the AP when there is a fault condition such as overcurrent, or when there is a major state change such as when the VRECT is turned on. The AP can enable or disable the interrupt conditions by writing to the Interrupt Enable Registers, INT_Enable_L (0x38) and INT_Enable_H (0x39).

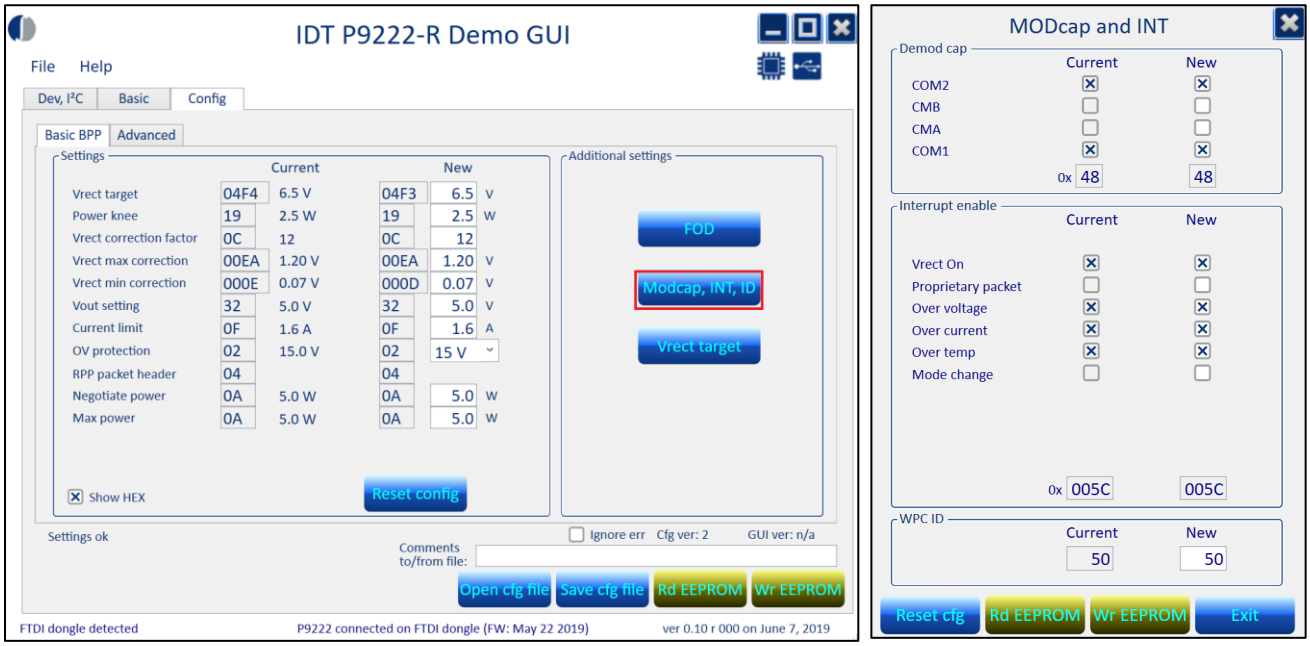
The default values of the ASK modulation depth and the interrupt enable registers can also be configured by writing a configuration file into the external EEPROM.

To generate the configuration file using the P9222-R Windows GUI, complete the following:

1. Place the receiver with the P9222-R-EVK onto the WPC transmitter or apply 5V from an external power supply on the VRECT node.
2. Launch the P9222-R GUI, go to the “Config” tab, click the “Rd EEPROM” button, and then click the “MODcap,INT,ID” button. A new popup window with the current values stored in the external EEPROM will be displayed.
3. Enter new values and click on the “Save cfg file” to generate a new configuration. The configuration can also be directly written to the external EEPROM by clicking the “Wr EEPROM” button.

   Note: The Write Protect function on the EEPROM must be disabled before writing to the EEPROM.

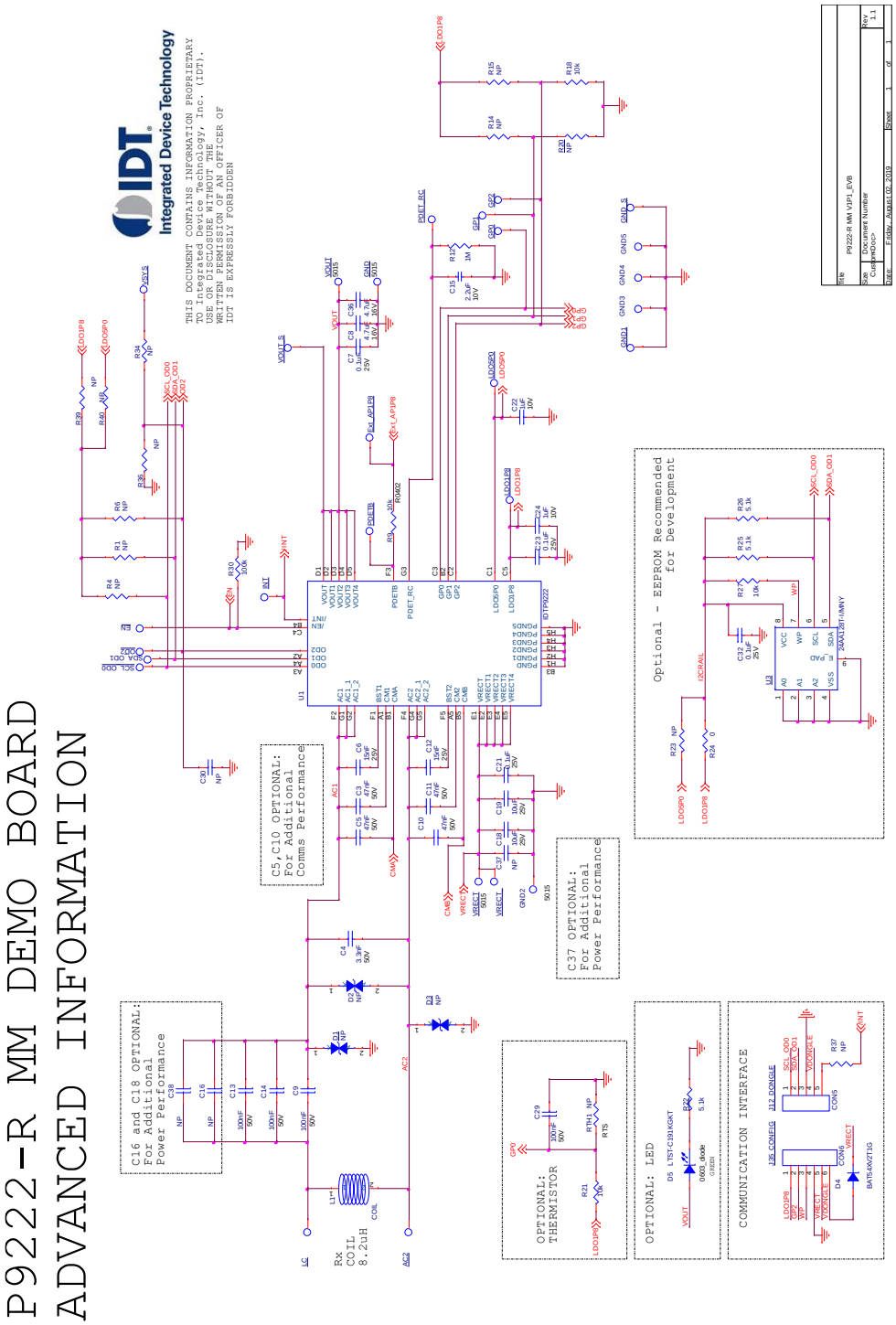
Figure 12. Modulation and INT Settings Tab



4. Hardware Information

4.1 Evaluation Board Schematic

Figure 13. Evaluation Board Schematic



4.2 Receiver Coil

The following coils are recommended for use in 5W or 3W applications in order to achieve optimum performance with the P9222-R receiver.

Table 3. Recommended Coil Manufacturer

Output Power	Vendor	Part Number	Inductance at 100kHz	Resonant Caps (Cs)	DC Resistance at 20℃
5W	SUNLORD	MQQRR303008S8R2	8.2µH ± 10%	300nF	180mΩ max
3W	TDK	WR303050-12F5-ID	8.2µH ± 10%	300nF	280mΩ max

4.3 Bill of Materials (BOM)

Table 4. P9222-R-EVK BOM

Item	Qty	Reference	Value	Description	Part Number	PCB Footprint
1	23	SDA_OD1, GP1, GND1, OD2, GP2, AC2, GND3, GND4, GND5, LDO1P8, Ext_AP1P8, LDO5P0, VSYS, VRECT_, VOUT_S, SCL_OD0, PDET_RC, PDETB, LC, INT, GP0, GND_S, EN	PTH_TP	Test Pad		10mil_35pad_1
2	2	C3, C11	47nF	CAP CER 0.047UF 50V X5R 0402	GRM155R61H473KE19D	C0402
3	1	C4	3.3nF	CAP CER 3300PF 50V X7R 0402	CL05B332KB5NNNC	C0402
4	2	C5, C10	NP	CAP CER 0.047UF 50V X5R 0402	GRM155R61H473KE19D	C0402
5	2	C6,C12	15nF	CAP CER 0.015UF 25V X7R 0402	GRM155R71E153KA61D	C0402
6	4	C7, C21, C23, C32	0.1uF	CAP CER 0.1UF 25V X5R 0201	CL03A104KA3NNNC	201
7	2	C8, C36	4.7uF	CAP CER 4.7UF 16V X5R 0402	CL05A475MO5NUNC	C0402
8	4	C9, C13, C14, C29	100nF	CAP CER 0.1UF 50V X5R 0402	GRM155R61H104KE19D	C0402
9	1	C15	2.2uF	CAP CER 2.2UF 10V X5R 0402	GRM155R61A225KE95D	C0402
10	2	C16, C38	NP	CAP CER 0.1UF 50V X5R 0402	GRM155R61H104KE19D	C0402
11	2	C18, C19	10uF	CAP CER 10UF 25V X5R 0603	GRM188R61E106MA73D	C0402_0603
12	2	C22, C24	1uF	CAP CER 1UF 10V X5R 0402	GRM155R61A105KE15D	C0402
13	1	C30	NP			C0402
14	1	C37	NP	CAP CER 10UF 25V X5R 0603	GRM188R61E106MA73D	C0402_0603
15	3	D1, D2, D3	NP	TVS DIODE 18V 45V SOD323	CDSOD323-T18C	SOD323

Item	Qty	Reference	Value	Description	Part Number	PCB Footprint
16	1	D4	DB2J31000L	DIODE SCHOTTKY 30V 200MA SOD-323F	DB2J31000L	SC-90, SOD-323F
17	1	D5	LTST-C191KGKT	LED GREEN CLEAR SMD	LTST-C191KGKT	0603_diode
18	4	GND2, VRECT, VOUT, GND	TP_SM	PC TEST POINT MINIATURE	5015	test_pt_sm_135x70
19	1	J12_DONGLE	CON5	CONN HEADER VERT 5POS 2.54MM	68000-105HLF	header_1x5_SMD
20	1	J35_CONFIG	CON6	CONN HEADER VERT 6POS 2.54MM	68000-106HLF	header_1x6_SMD
21	1	L1	COIL		8.2uH	P9222_COIL_PAIR
22	1	RTH1	NP			RTS
23	12	R1, R4, R6, R14, R15, R20, R23, R34, R36, R37, R39, R40	NP		NP	R0402
24	4	R9, R18, R21, R27	10k	RES SMD 10K OHM 5% 1/16W 0402	RC0402JR-0710KL	R0402
25	1	R12	1M	RES SMD 1M OHM 1% 1/16W 0402	RC0402FR-071ML	C0402
26	3	R22, R25, R26	5.1k	RES SMD 5.1K OHM 5% 1/16W 0402	MCR01MRTJ512	R0402
27	1	R24	0	RES SMD 0 OHM JUMPER 1/10W 0402	ERJ-2GE0R00X	R0402
28	1	R30	100k	RES SMD 100K OHM 1% 1/16W 0402	RC0402FR-07100KL	R0402
29	1	U1	IDTP9222		P9222	P9270CSP_0p4mm
30	1	U3	24AA128T-I/MNY	IC MEM TDFN08 64KBYTE EEPROM 400KHZ I2C	24AA128T-I/MNY	TDFN08

* NP: Non Populate.

4.4 P9222-R-EVK PCB Layout

Figure 14. Top Layer

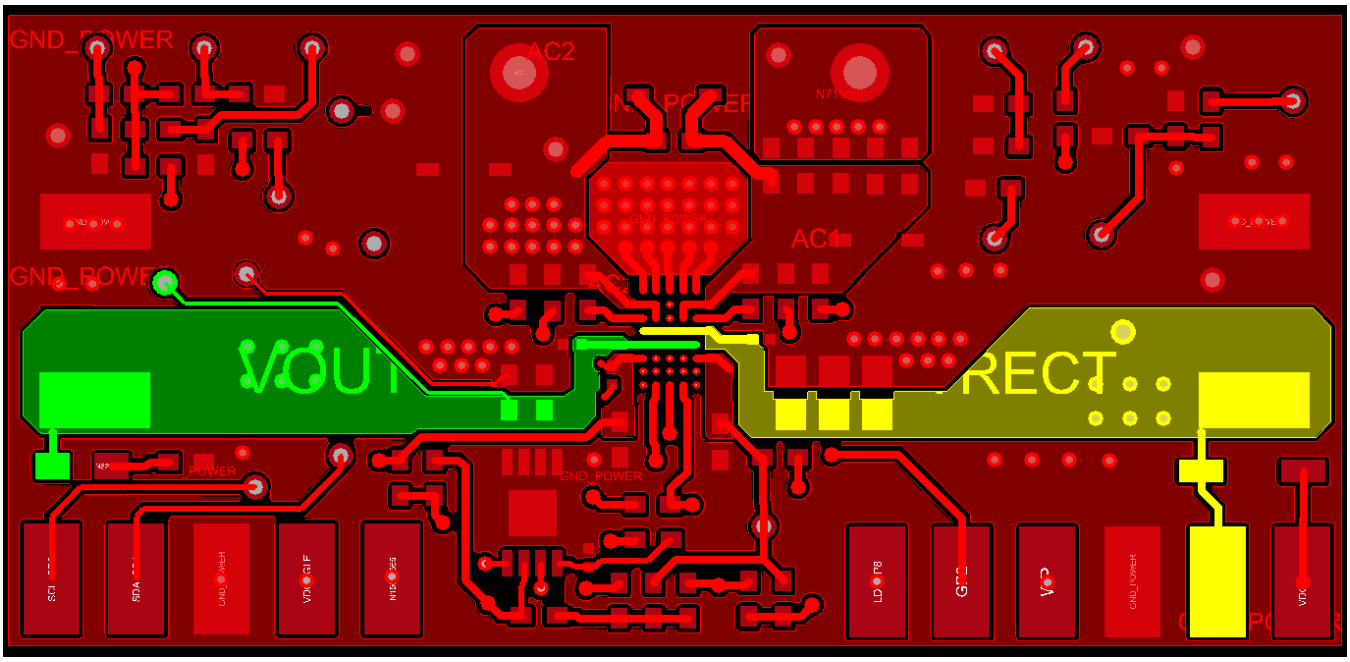


Figure 15. Inner1 GND Layer

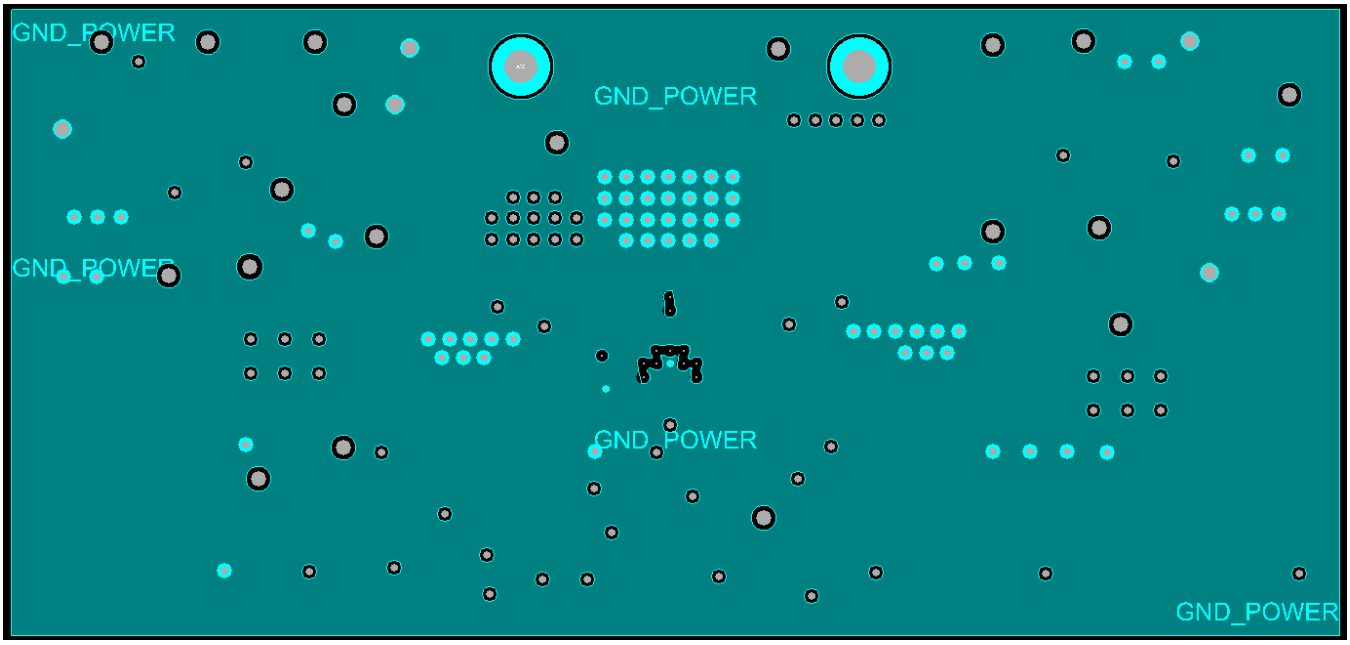


Figure 16. Inner2 POWER/Signal/GND Layer

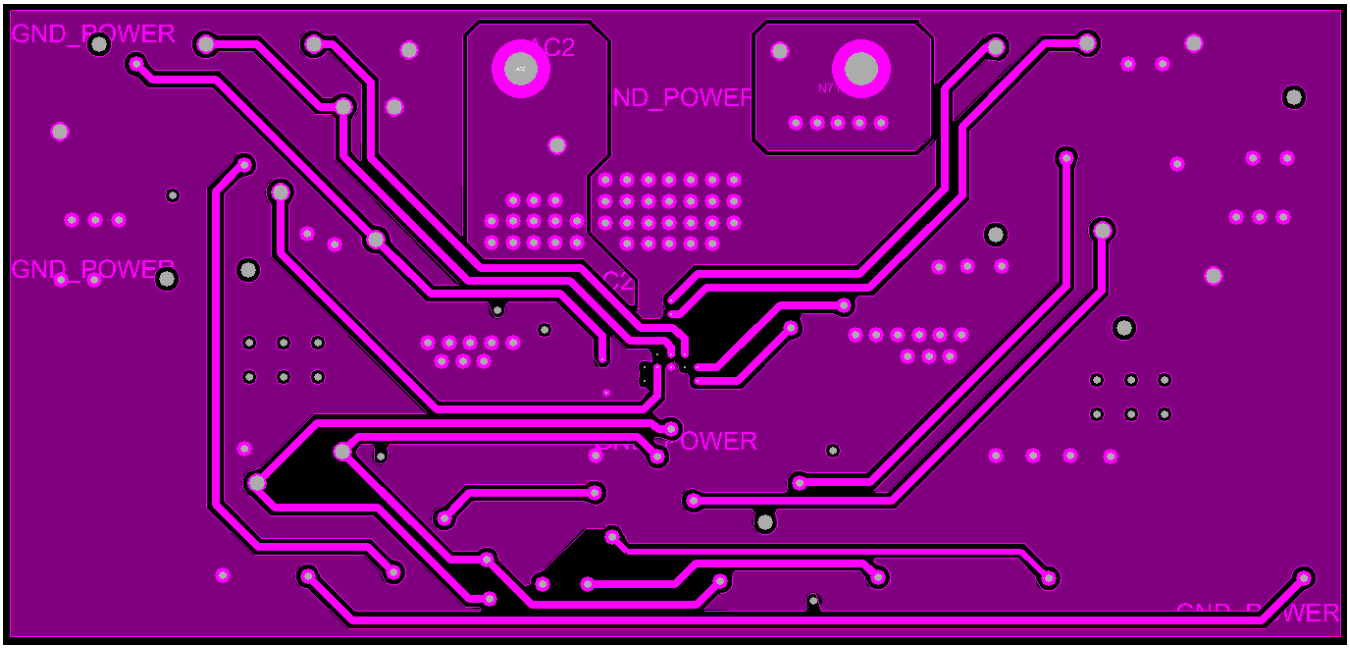


Figure 17. Bottom Layer

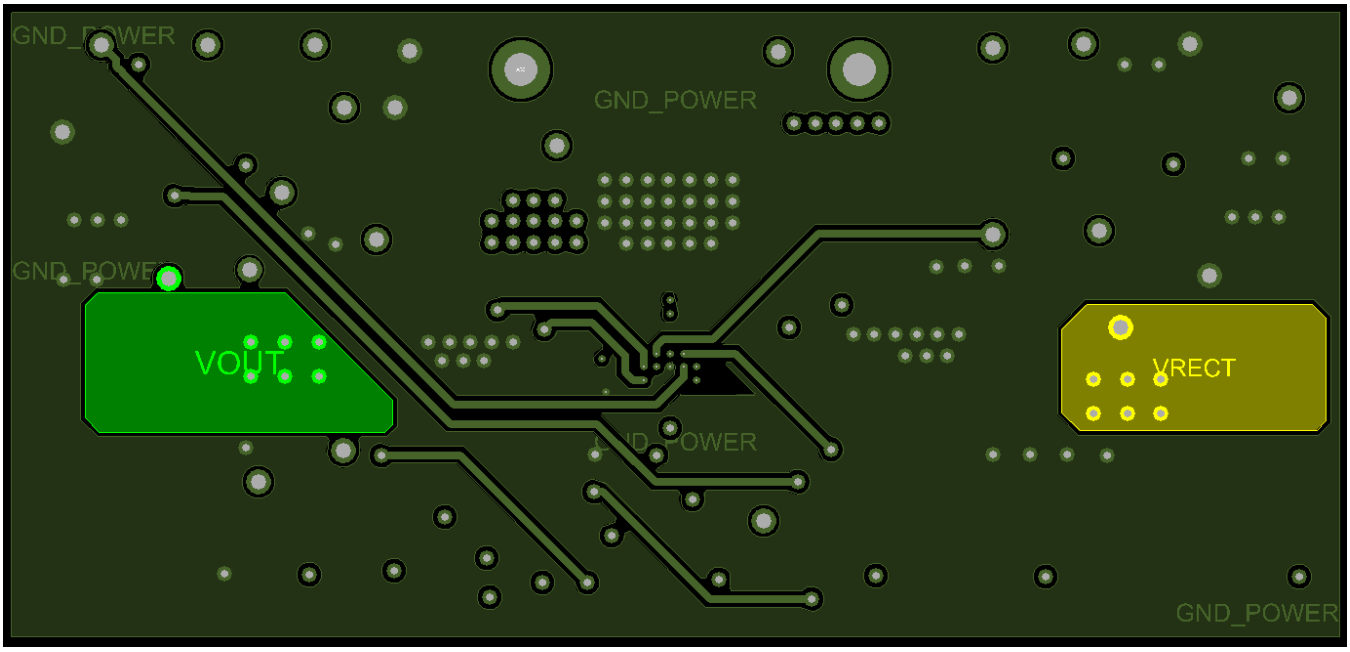
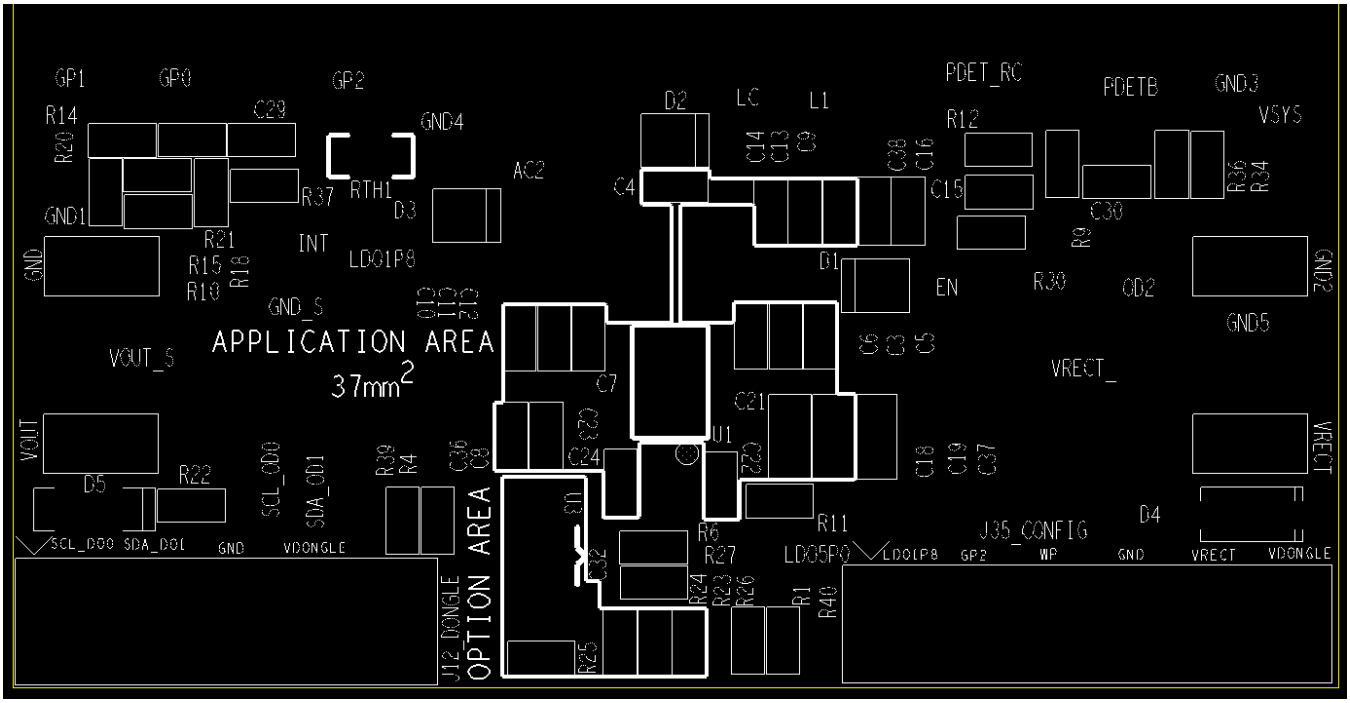


Figure 18. Top Silkscreen Layer



5. List of Registers

The P9222-R uses the standard I²C slave implementation protocol to communicate with a host AP or other I2C peripherals. The communication protocol is implemented using 8 bits for data and 16 bits for addresses. The default slave address of the P9222-R is 0x61.

The following tables list address locations, field names, available operations (R or RW), default values, and functional descriptions of internally accessible registers contained within the P9222-R. The OTP registers are loaded each time the device is powered and cannot be changed except by new firmware programmed into a blank device. The SRAM registers are available to make setting changes after the device is powered. These changes are reset to default when the power is cycled or the device is reset.

Table 5. Chip Part Number ID Register, Chip_ID_L (0x00), Chip_ID_H (0x01)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x00 [7:0]	Chip_ID_L	R	0x22	Chip ID low byte
0x01 [7:0]	Chip_ID_H	R	0x92	Chip ID high byte

Table 6. Chip Revision Register, Chip_Rev (0x02)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x02 [7:0]	Chip_Rev	R	0x02	Chip main revision. Latest chip revision is 0x02 (default).

Table 7. OTP Firmware Revision Registers, OTP_FW_Major (0x04), OTP_FW_Minor (0x06)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x04 [15:0]	OTP_FW_Major	R	0x0000	Major revision of firmware in OTP low byte
0x06 [15:0]	OTP_FW_Minor	R	0x0011	Minor revision of firmware in OTP low byte

Table 8. Status Registers, Status_L (0x34), Status_H (0x35)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x34 [7]	Reserved	R	0x0	Reserved
0x34 [6]	VRECTON	R	0x0	1 = Indicates AC power is applied. The flag is set before the Configuration Packet. It is cleared on system reset or when power is removed. Interrupt event is generated on SET event. This bit can be used for turning on the charging indicator on the receiver.
0x34 [5]	TX Data Received	R	0x0	0 = Indicates no TX data is received. 1 = Indicates TX data is received and is ready to be read
0x34 [4]	Over voltage	R	0x0	0 = Indicates no such a condition exists. 1 = Indicates Over Voltage condition exists
0x34 [3]	Over current	R	0x0	0 = Indicates no such a condition exists 1 = Indicates Over Current condition exists
0x34 [2]	Over temperature	R	0x0	0 = Indicates no such a condition exists 1 = Indicates Over Temperature condition exists
0x34 [1:0]	Reserved	R	0x0	Reserved
0x35 [7:0]	Reserved	R	0x0	Reserved

Table 9. Interrupt Registers, INT_L (0x36), INT_H (0x37)[a]

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x36 [7]	Reserved	R	0x0	Reserved.
0x36 [6]	VRECTON_INT	R	0x0	AC power applied and stable interrupt.
0x36 [5]	TX Data Received	R	0x0	1 = Indicates a pending interrupt for TX Data Received. (No received data state change to data received state).
0x36 [4]	Over voltage	R	0x0	1 = Indicates a pending interrupt for Over voltage event
0x36 [3]	Over current	R	0x0	1 = Indicates a pending interrupt for Over current event
0x36 [2]	Over temperature	R	0x0	1 = Indicates a pending interrupt for Over temperature event
0x36 [1]	Reserved	R	0x0	Reserved
0x36 [0]	Mode_Changed	R	0x0	1 = Indicates a pending interrupt for mode or state change. For reading the current state, refer to Sys_Op_Mode (0x4C).
0x37 [7:0]	Reserved	R	0x00	Reserved

[a] If any bit in the two INT status registers is 1, and the corresponding bit in the two INT Enable registers is set to 1, /INT pad will be pulled down to indicate an interrupt event to AP.

Table 10. Interrupt Enable Registers, INT_Enable_L (0x38), INT_Enable_H (0x39)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x38 [6]	VRECTON_EN	R/W	0x1	AC power applied and stable interrupt enable.
0x38 [5]	TX Data Received	R/W	0x0	0 = Disable the interrupt. 1 = AP writes 1 to enable the interrupt from Interrupt Registers' corresponding bit.
0x38 [4]	Over voltage	R/W	0x1	0 = Disable the interrupt. 1 = AP writes 1 to enable the interrupt from Interrupt Registers' corresponding bit.
0x38 [3]	Over current	R/W	0x1	0 = Disable the interrupt. 1 = AP writes 1 to enable the interrupt from Interrupt Registers' corresponding bit.
0x38 [2]	Over temperature	R/W	0x1	0 = Disable the interrupt. 1 = AP writes 1 to enable the interrupt from Interrupt Registers' corresponding bit.
0x38 [1]	Reserved	R	0x0	Reserved
0x38 [0]	Mode Changed	R/W	0x0	0 = Disable the interrupt. 1 = AP writes 1 to enable the interrupt from Interrupt Registers' corresponding bit.
0x39 [7:0]	Reserved	R	0x00	Reserved

Table 11. Interrupt Clear Registers, INT_Clear_L (0x3A), INT_Clear_H (0x3B)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x3A [6]	VRECTON_CLR	R/W	0x0	AC power applied and stable interrupt clear.
0x3A [5]	TX Data Received	R/W	0x0	AP writes 1 to clear the corresponding Interrupt Registers' bit. This bit is self-cleared to 0 (by M0) afterward.
0x3A [4]	Over voltage	R/W	0x0	AP writes 1 to clear the corresponding Interrupt Registers' bit. This bit is self-cleared to 0 (by M0) afterward.
0x3A [3]	Over current	R/W	0x0	AP writes 1 to clear the corresponding Interrupt Registers' bit. This bit is self-cleared to 0 (by M0) afterward.
0x3A [2]	Over temperature	R/W	0x0	AP writes 1 to clear the corresponding Interrupt Registers' bit. This bit is self-cleared to 0 (by M0) afterward.
0x3A [1]	Reserved	R	0x0	Reserved.
0x3A [0]	Stat_Mode_Changed	R/W	0x0	AP writes 1 to clear the corresponding Interrupt Registers' bit. This bit is self-cleared to 0 (by M0) afterward.
0x3B [7:0]	Reserved	R	0x00	Reserved

Clearing all interrupts:

Clear all the interrupts that were generated using the INT_Clear_L (0x3A) and COM (0x4E) registers:

1. Write 0xFF to the INT_Clear_L (0x3A) register.
2. Write 0x20 to the COM (0x4E) register (set bit 5) to instruct the processor to clear the interrupt.

Clearing a single interrupt:

Clearing a single interrupt is a two-step process using the INT_Clear_L (0x3A) and COM (0x4E) registers:

1. In the INT_Clear_L (0x3A) register, set the bit that corresponds to the interrupt that will be cleared.
2. In the COM (0x4E) register, set bit 5 to instruct the processor to clear the interrupt.

   Note: Only the interrupt(s) that are selected with the INT_Clear_L (0x3A) register will be cleared.

Table 12. Vout Set Register, Vout_Set (0x3C)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x3C [7:0]	Vout_Set	R/W	0x32	Set the output voltage of the main LDO in 0.1V units. BPP default value: 0x32. Example: To set Vout to 5.5V, write 0d55 (0x37).

Table 13. ILIM Set Register, ILIM_Set (0x3D)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x3D [7:0]	ILIM_Set[7:0]	R/W	0x0F	Main LDO output current limit (by which LDO will behave as a constant current source) set value. 100mA step, 0.1A-1.3A 0x00-0x0F: ILim = value * 0.1 (A)

Table 14. Battery Charge Status Register, CHG_Status (0x3E)[a]

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x3E [7:0]	Charge status	R/W	0x00	A WPC charge status packet will be sent based on the following: 0x0 = Reserved 0x1 = Charge status packet sent with parameter = 1 (1%) 0x2 = Charge status packet send with parameter = 2 (2%) … 0x64 = Charge status packet send with parameter = 100 (100%) 0x65-0xFE = Reserved 0xFF = No battery charge device or not providing charge status packet

[a] After writing to this register, Send Charge Status bit of Command Register (0x4E) needs to be set for transmission to begin.

Table 15. End of Power Transfer Register, EPT (0x3F)[a]

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x3F [7:0]	EPT/EOC/EOP Reason	R/W	0x00	A WPC End of Power Transfer packet/message will be sent based on the following: 0 = WPC mode, unknown EPT should be sent. 1 = WPC mode, End of Charge EPT packet should be sent. 2 = WPC mode, Internal Fault EPT packet should be sent. 3 = WPC mode, Over Temperature EPT packet should be sent. 4 = WPC mode, Over Voltage EPT packet should be sent. 5 = WPC mode, Over Current EPT packet should be sent. 6 = WPC mode, Battery Failure EPT packet should be sent. 7 = WPC mode, Reconfiguration EPT packet should be sent. 8 = WPC mode, No Response EPT packet should be sent. 9-254 = Reserved

[a] After writing to this register, the Send End of Power bit Command of Register (0x4E) must be set for transmission to begin.

Table 16. Vrect ADC Value Registers, ADC_Vrect_L (0x40), ADC_Vrect_H (0x41)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x40 [15:0]	ADC_Vrect [15:0]	R	0x0	Vrect ADC value in mV.

Table 17. Vout ADC Value Registers, ADC_Vout_L (0x42), ADC_Vout_H (0x43)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x42 [15:0]	ADC_Vout [15:0]	R	0x0	Vout ADC value in mV.

Table 18. Iout Value Registers, Iout_L (0x44), Iout_H (0x45)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x44 [15:0]	Iout [15:0]	R	0x0	Iout value in mA.

Table 19. Operating Frequency Registers, Op_Freq_L (0x48), Op_Freq_H (0x49) (RX Only)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x48 [15:0]	Op_Freq[7:0]	R	0x0	Operating frequency (AC signal frequency on the coil) in kHz.

Table 20. System Operating Mode Register, Sys_Op_Mode (0x4C)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x4C [7]	Reserved	R	0	Reserved.
0x4C [6:5]	Operational Mode	R	0x0	Indicates current operational mode. No Default Value, depends on power source that is detected. 00 = AC Missing mode 01 = WPC mode 10 = Reserved 11 = Reserved
0x4C [4:1]	Reserved	R	0	Reserved.
0x4C [0]	LDOONMODE	R/W	0	Indicates output on VOUT.

Table 21. (AP to P9222-R) Command Register, COM (0x4E)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x4E [7:6]	Reserved	R	0x0	Reserved.
0x4E [5]	Clear Interrupt	R/W	0x0	If the AP sets this bit to 1 then the P9222 M0 clears the interrupt corresponding to the bit(s) that have a value of 1 in Interrupt Clear Registers, and also sets the bit(s) in Interrupt Clear Registers to 0, as well as sets this bit to 0.
0x4E [4]	Send Charge Status	R/W	0x0	If the AP sets this bit to 1 then the P9222 the M0 sends the Charge Status packet (defined in the Battery Charge Status Register) to TX, and then sets this bit to 0 after execution.
0x4E [3]	Send End of Power	R/W	0x0	If the AP sets this bit to 1 then the P9222 M0 sends the End of Power packet (defined in the End of Power Transfer Register) to TX and then sets this bit to 0.
0x4E [2]	Reserved	R/W	0x0	Reserved.
0x4E [1]	Toggle LDO On/OFF	R/W	0x0	If the AP sets this bit to 1 then the P9222 M0 toggles LDO output once (from on to off, or from off to on), and then sets this bit to 0.
0x4E [0]	SEND RX Data	R/W	0x0	If the AP sets this bit to 1 then the P9222 M0 sends Data Command + Value to TX on Header and Payload of WPC Proprietary Packet, and then sets this bit to 0 after execution.

The P9222-R will prioritize packets when sending commands and data to the Tx. Packets are prioritized as follows:

1. Received Power Packet (RPP)
2. Charge Status Packet (CSP)
3. Proprietary Packet (PPP)
4. Control Error Packet (CEP)

When using the AP to send CSP and PPP messages, care should be taken not to send them too frequently because they will delay the CEP transmission. It is not recommended to send CSP or PPP packets more than once every 250ms to avoid extended periods of time without allowing the P9222-R to transmit a CEP.

Table 22. Die Temperature ADC Value Registers, ADC_Die_Temp_L (0x66), ADC_Die_Temp_H (0x67)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x66 [15:12]	Reserved	R	0x0	Reserved
0x66 [11:0]	ADC_Die_Temp_L	R	0x0	8 LSB of current Die Temperature ADC value. Formula converting ADC value to Die Temperature in Celsius Degree is: T_{DIE} = (DieTemp(adc) * 10/107) - 247

Table 23. Overvoltage Protection Set Register (0xB3, 8-bit)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0xB3 [7:3]	Reserved	R	0	Reserved.
0xB3 [2:0]	OV Set	R/W	0x02	Set Overvoltage Protection level. The hardware enables an additional DC Load when Vrect reaches 90% of the set level. The possible combinations are: 0x0 = 17V 0x1 = 20V 0x2 = 15V 0x3 = 13V 0x4-0x7 = 11V

Table 24. ASK Modulation Depth Register (0xB2, 16-bit)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0xB2 [7]	Reserved	R	0	Reserved.
0xB2 [6]	CM2EN	R/W	0x1	Enable CM2 pin to generate ASK modulation signal.
0xB2 [5]	CMBEN	R/W	0x0	Enable CMB pin to generate ASK modulation signal.
0xB2 [4]	CMAEN	R/W	0x0	Enable CMA pin to generate ASK modulation signal.
0xB2 [3]	CM1EN	R/W	0x1	Enable CM1 pin to generate ASK modulation signal
0xB2 [2:0]	Reserved	R	0	Reserved.

Table 25. Foreign Object Detection Registers, FOD (0x70-0x7E)[a]

The FOD registers are divided into eight pairs. Each pair has one byte for gain setting and one byte for offset setting. The first six pairs control the Received Power calculation for six power sectors during the Power Transfer phase. The seventh pair calibrates the internal DC Load. The set values of the FOD registers are found with the help of an IDT developed calibration procedure using the nok9 tester.

The firmware initializes the FOD registers for BPP mode. The correct set is loaded at completion of the ID and Configuration Phase. The AP can modify the registers at any time if needed to update the values.

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x70 [7:0]	GAIN_0	R/W	0xBC	FOD coefficients for Power Region 0: Gain (slope settings).
0x71 [7:0]	OFFSET_0	R/W	0x14	FOD coefficients for Power Region 0: Offset settings.
0x72 [7:0]	GAIN_1	R/W	0x98	FOD coefficients for Power Region 1: Gain (slope settings).
0x73 [7:0]	OFFSET_1	R/W	0x18	FOD coefficients for Power Region 1: Offset settings.
0x74 [7:0]	GAIN_2	R/W	0x9F	FOD coefficients for Power Region 2: Gain (slope settings).
0x75 [7:0]	OFFSET_2	R/W	0x0A	FOD coefficients for Power Region 2: Offset settings.
0x76 [7:0]	GAIN_3	R/W	0x94	FOD coefficients for Power Region 3: Gain (slope settings).
0x77 [7:0]	OFFSET_3	R/W	0x12	FOD coefficients for Power Region 3: Offset settings.
0x78 [7:0]	GAIN_4	R/W	0x97	FOD coefficients for Power Region 4: Gain (slope settings).
0x79 [7:0]	OFFSET_4	R/W	0x05	FOD coefficients for Power Region 4: Offset settings.
0x7A [7:0]	GAIN_5	R/W	0xA7	FOD coefficients for Power Region 5: Gain (slope settings).
0x7B [7:0]	OFFSET_5	R/W	0xCB	FOD coefficients for Power Region 5: Offset settings.
0x7C [7:0]	GAIN_6	R/W	0x14	FOD coefficients for Power Region 6: Gain (slope settings).
0x7D [7:0]	OFFSET_6	R/W	0x00	FOD coefficients for Power Region 6: Offset settings.
0x7E [7:0]	GAIN_7	R/W	0x01	FOD coefficients for Power Region 7: Gain (slope settings).
0x7F[7:0]	OFFSET_7	R/W	0x50	FOD coefficients for Power Region 7: Offset settings.

[a] These default FOD coefficients are calculated to PASS Nok9 CATS1 tester FOD tests using the P9222-R reference design. FOD coefficients must be changed if the receiver design uses a different coil compared to the P9222-R reference design, or if there is a large amount of friendly metal around the receiver coil.

Table 26. ADC Result Register (0xD4, 16-bit, OD2 in Default Config)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0xD4 [15:0]	AdcResult[0]	R	0	Configurable for GPIO, Temperature, Vout, Iout, or Vrect. By default it is configured to OD2. The value is always in ADC counts and therefore must be converted to the desired units. For GPIOs the conversion is: ***AdcResult[0] * 2100 / 4096 = Voltage on OD2 in mV***

Table 27. ADC Result Register (0xD6, 16-bit, GP1 in Default Config)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0xD6 [15:0]	AdcResult[1]	R	0	Configurable for GPIO, Temperature, Vout, Iout, or Vrect. By default it is configured to GP1. The value is always in ADC counts and therefore must be converted to the desired units. For GPIOs the conversion is: ***AdcResult[1] * 2100 / 4096 = Voltage on GP1 in mV***

Table 28. ADC Result Register (0xD8, 16-bit, GP2 in Default Config)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0xD8 [15:0]	AdcResult[2]	R	0	Configurable for GPIO, Temperature, Vout, Iout, or Vrect. The value is always in ADC counts and therefore must be converted to the desired units. For GPIOs the conversion is: ***AdcResult[2] * 2100 / 4096 = Voltage on GP2 in mV***

Table 29. ADC Result Register (0xDA, 16-bit, Die Temperature in Default Config)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0xDA [15:0]	AdcResult[3]	R	0	Configurable for GPIO, Temperature, Vout, Iout, or Vrect. The value is always in ADC counts and therefore must be converted to the desired units. For the conversion is: ***AdcResult[3] * (2.1*200 / 4096) - 280 = Temperature in degC***

Table 30. External Thermistor Voltage on GP0 (0xB0, 16-bit)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0xB0 [15:12]	Reserved	R	0	Reserved
0xB0 [11:0]	ExtTemp	R	0xFFF	12-bit raw data of the thermistor ADC reading on GP0 pin.

Table 31. VRECT Target Register (0x90, 16-bit)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x90 [15:0]	VrectTarget	R	0x4F3	Current value of VrectTarget in ADC codes. The ADC code to Voltage conversion formula is: Vrect(V) = Vrect(adc code) * 21(V) / 4095

Table 32. VRECT Knee Register (0x92, 8-bit)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x92 [7:0]	PwrKnee	R/W	0x0F	Threshold in units of 0.1W output power at which minimal window is applied.

Table 33. VRECT Correction Factor Register (0x93, 8-bit)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x93 [7:0]	VrCorrFactor	R/W	0x19	Coefficient used in the Vrect Target calculation algorithm.

Table 34. VRECT Maximum Correction Register (0x94, 16-bit)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x94 [15:0]	VrMaxCorr	R/W	0xEA	Maximum width of the window in ADC codes.

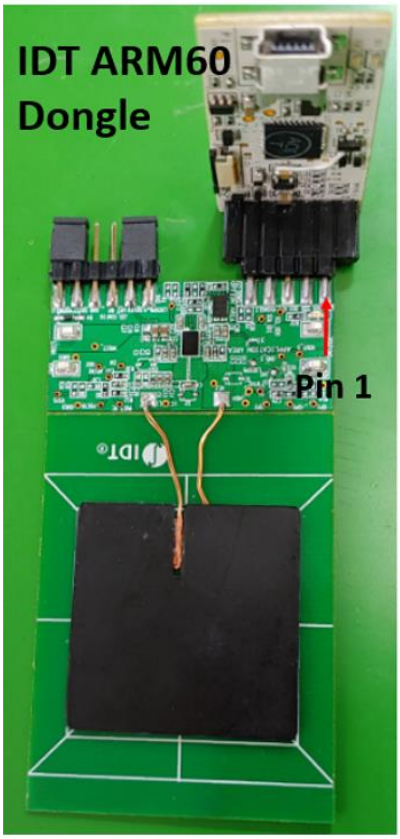
Table 35. VRECT Minimum Correction Register (0x96, 16-bit)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x96 [15:0]	VrMinCorr	R/W	0x0D	Minimum width of the window in ADC codes.

Appendix A – IDT ARM60 Dongle Driver Install

An IDT internal ARM60 USB-to-I2C is an alternative to the “USB-FTDI-V2-1” (FTDI) USB-to-I2C dongle. The following figure shows the hardware connection of the ARM60 dongle to the P9222-R-EVK.

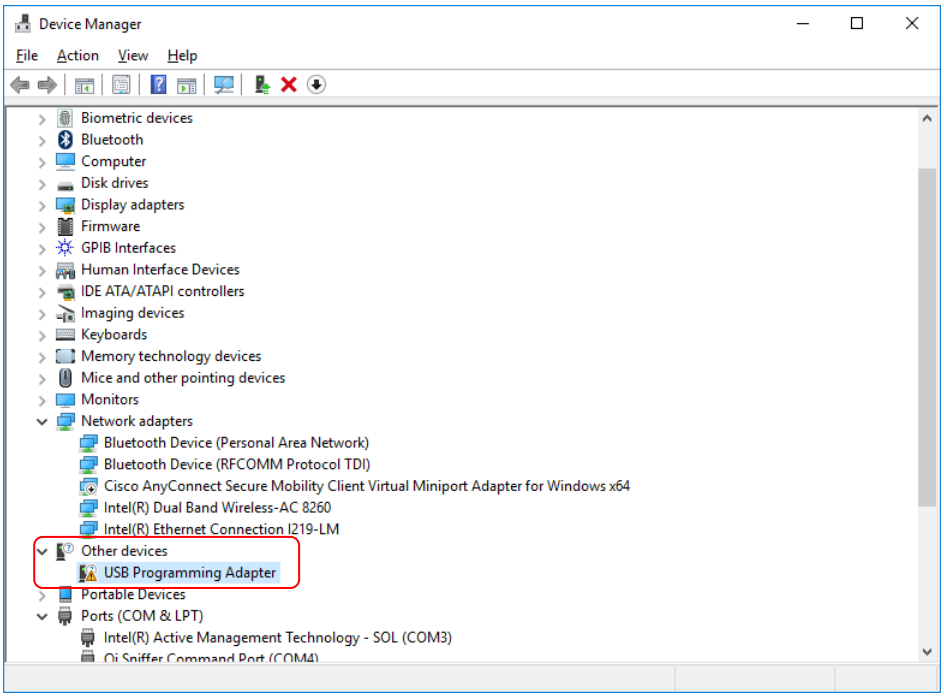
Figure 19. ARM60 Dongle



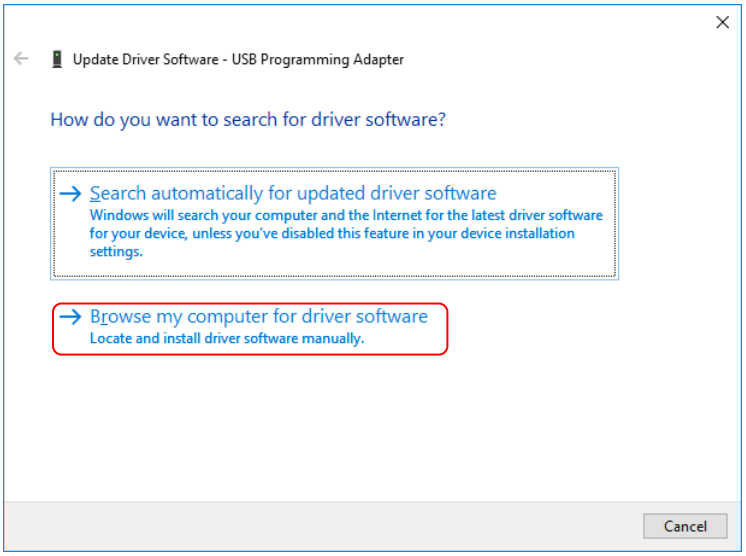
Installing USB Drivers

Install one at a time (9000, then 9001) if using two dongles simultaneously (for Windows 10 instructions, see “Disabling Driver Signature Enforcement in Windows 10):

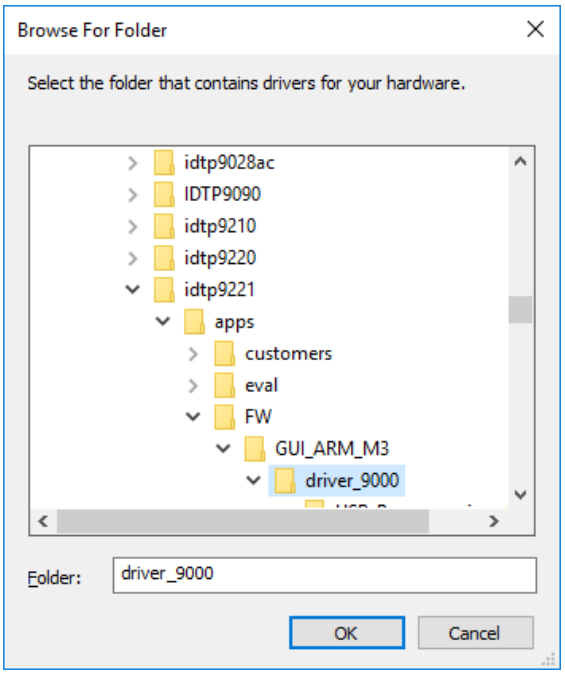
1. Go to the Control Panel and locate the USB Programming Adaptor.



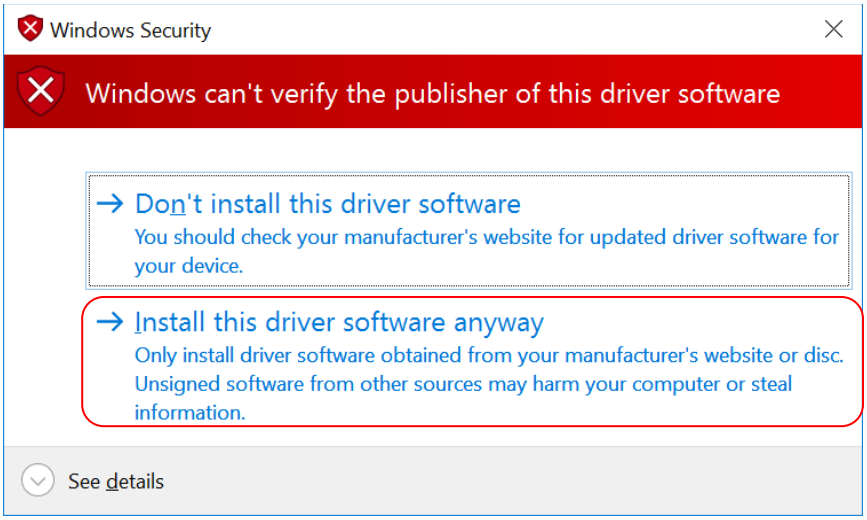
2. Right-click the USB Programming Adaptor and Select “Update Device Software…”
3. Choose “Browse My Computer for driver software”.



4. Browse to the folder driver9000 and select OK (the driver should install).



Note: Install this driver anyway:



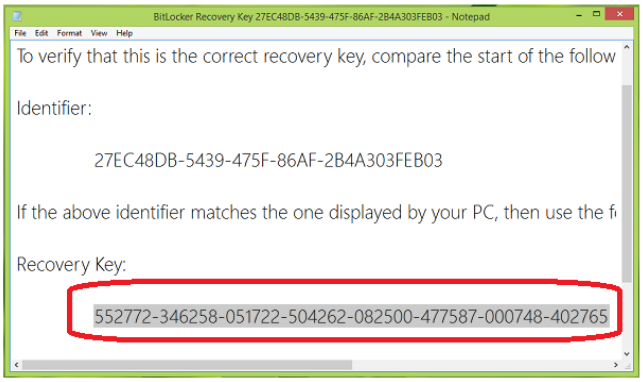
The driver will install, click 'Close' when successfully updated.

5. Repeat steps 1 to 4 for the driver9001 (or driver9000 if the driver9001 was installed first).

Disabling Driver Signature Enforcement in Windows 10

Windows 10 does not allow driver installation without a Driver Signature. The ARM M3 9000 and 9001 dongles do not have this signature, so the Driver Signature Enforcement must be disabled prior to installing the driver (one time is suggested and the instructions are below):

1. Locate and write down or print your PC recovery key (48 # numeric key):
   a. Backup BitLocker Drive Encryption Recovery Key.
      i. Press **Windows Key + Q** and type "**bitlocker"**. From search results, pick **Manage BitLocker** entry.
      ii. In the *BitLocker Drive Encryption* window, look for the drive whose recovery key is required at the moment. Click on **Back up your recovery key.**
      iii. Select the most convenient method to save the recovery key (e.g., Save to file (must be on drive other than current CPU drive) or Print the recovery key).
      iv. Open the file or view the recovery key (example):



2. Disable the Driver Signature Enforcement:
   a. Press the **Windows key + R** to bring up the Run box. Type "**shutdown /r /o**" and hit Enter.
   b. Windows informs you that you are about to be signed off. Click **Close**.
   c. Once your computer has rebooted you will need to choose the **Troubleshoot** option, then click on **Advanced options.**
   d. In the Advanced Options window, choose **Startup Settings**.
   e. Click the **Restart** button on the Startup Settings screen to reboot your computer again.
   f. After restart in Startup Settings windows, press the **F7** key on your keyboard to select "**Disable driver signature enforcement**".
   g. Enter the **Recovery Key** for your computer located in Step 1 when prompted.
   h. After the computer reboots again, install the ARM M3 9000 and 9001 drivers.
   i. After rebooting the computer again, Driver Signature Enforcement will be automatically enabled.

Ordering Information

Orderable Part Number	Description
P9222-R-EVK	P9222-R Evaluation Kit
USB-FTDI-V2-1	USB-to-I2C dongle (FTDI). It is not included in the P9222-R-EVK evaluation kit and needs to be ordered separately.

Revision History

Revision Date	Description of Change
September 27, 2019	Initial release.

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