

PTX105R-EB-ST-QFN56-POS_IoT (v2.0)

This document describes how the PTX105R demonstration (demo) board can be operated with two selectable voltage settings by moving the jumper from JMP_VBUS to JMP_DCDC. The board also provides easy interfacing options to a PC via USB or to a microcontroller board via PMOD.

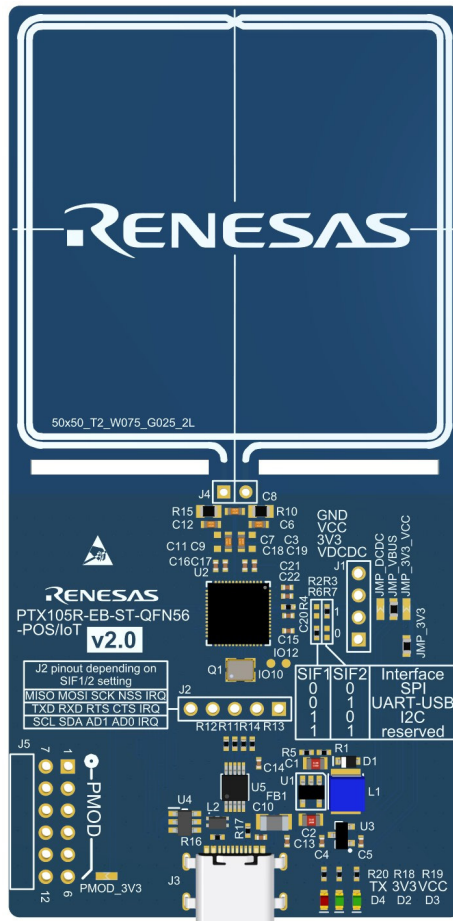


Figure 1. PTX105R-EB-ST-QFN56-POS_IoT Demo Board

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1. Power Supply

The board is powered via a USB-C connection.

The PTX105R can be operated in two voltage settings which can be selected by moving the jumper from JMP_VBUS to JMP_DCDC:

- VBUS (5V)
- or
- VDCDC (5.4V)

The board's default is VBUS which is also the setting that the compliance tests were performed in.



Current consumption in continuous field mode is ~360mA with VBUS and ~450mA with VDCDC.

2. USB Interface

The USB Interface is handled by a CH340E USB to UART bridge.

Drivers can be downloaded from the manufacturer's [webpage](#).

3. Interface Switching

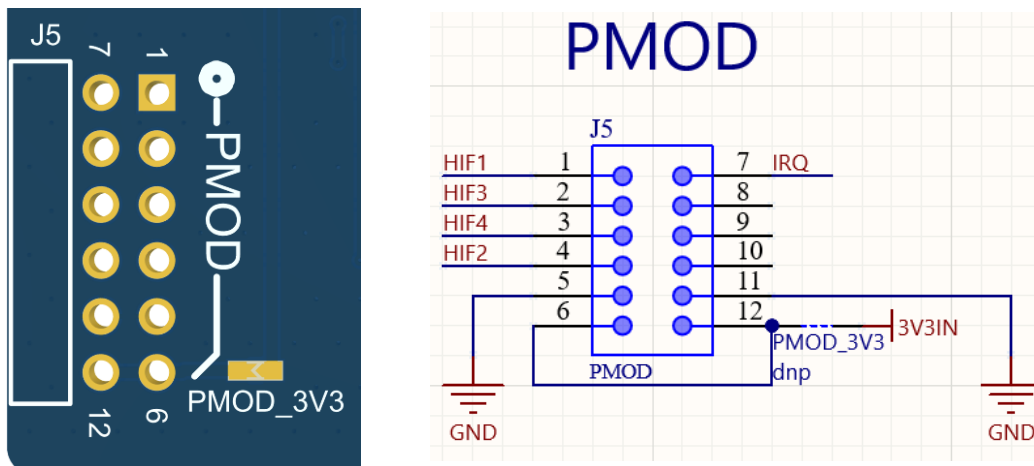
The evaluation board allows the user to switch between three interfaces supported by the PTX105R IC using the SIF1 / SIF2 jumpers:

SIF1	SIF2	Interface	Jumpers Used
0	0	SPI	
0	1	UART to USB	
1	0	I ² C	

The UART Interface is connected to the USB bridge and can be accessed via the USB-C plug.

4. PMOD

All interfaces are also available via a PMOD 2 × 6 pin connector (must be soldered manually). The pinout follows the PMOD recommendation for an SPI Interface. The PMOD connector allows connecting to a multitude of MCU demo boards. Example firmware is available for the Renesas [TB-S3A1 board](#).



The 3.3V supply for the host MCU can also be provided by the demo board if jumper PMOD_3V3 is placed

5. Clocking

The PTX105R device's default clock source is a 27.12MHz crystal (Q1).

6. Debugging

The PCB has three debug LEDs:

- Two for supply (green)
- One for UART communication (red)



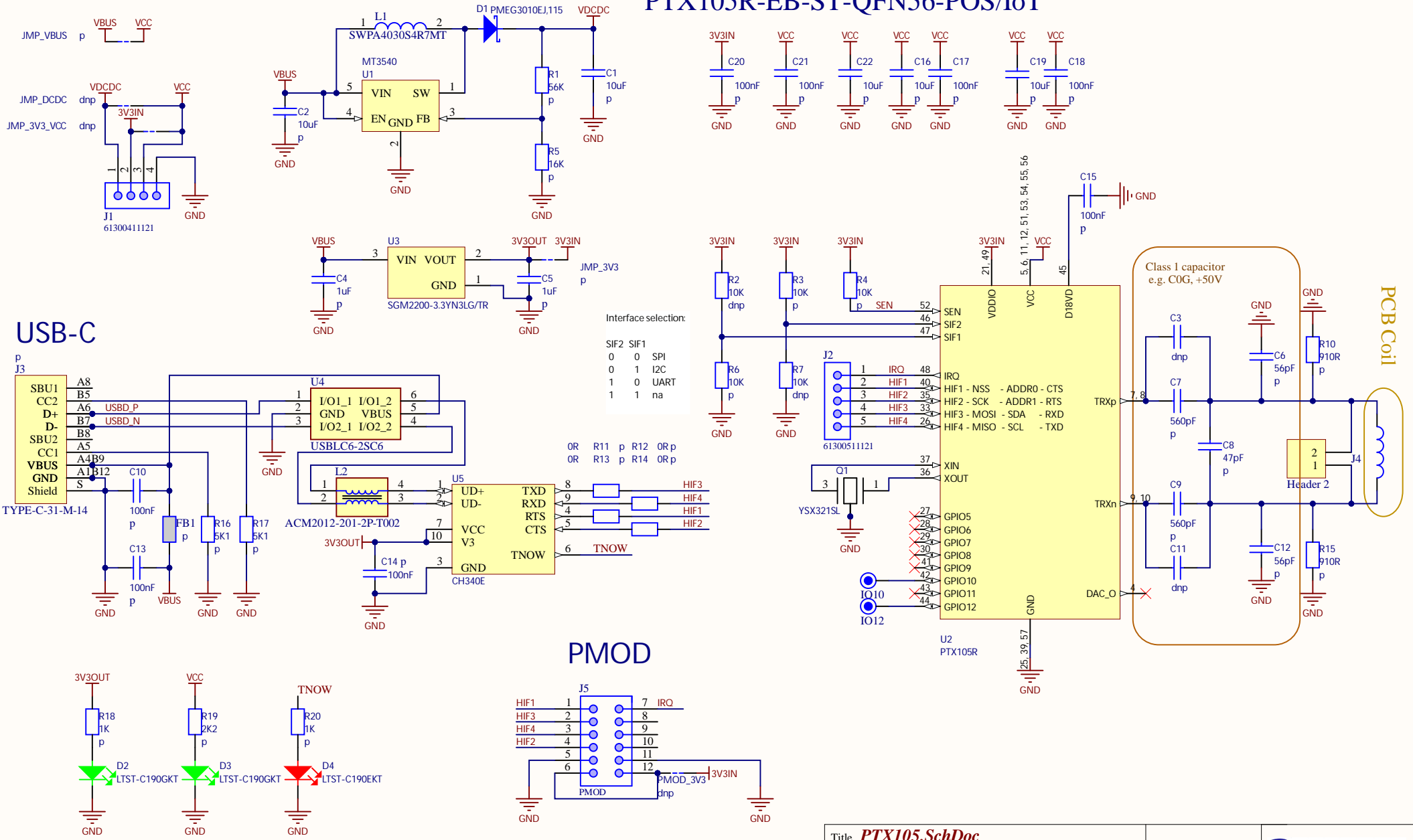
7. Schematics

The PTX105R-EB-ST-QFN56-POS_IoT schematics and layout diagrams are located at the end of this document.

8. Revision History

Revision	Date	Description
1.00	Apr 9, 2024	Initial release.

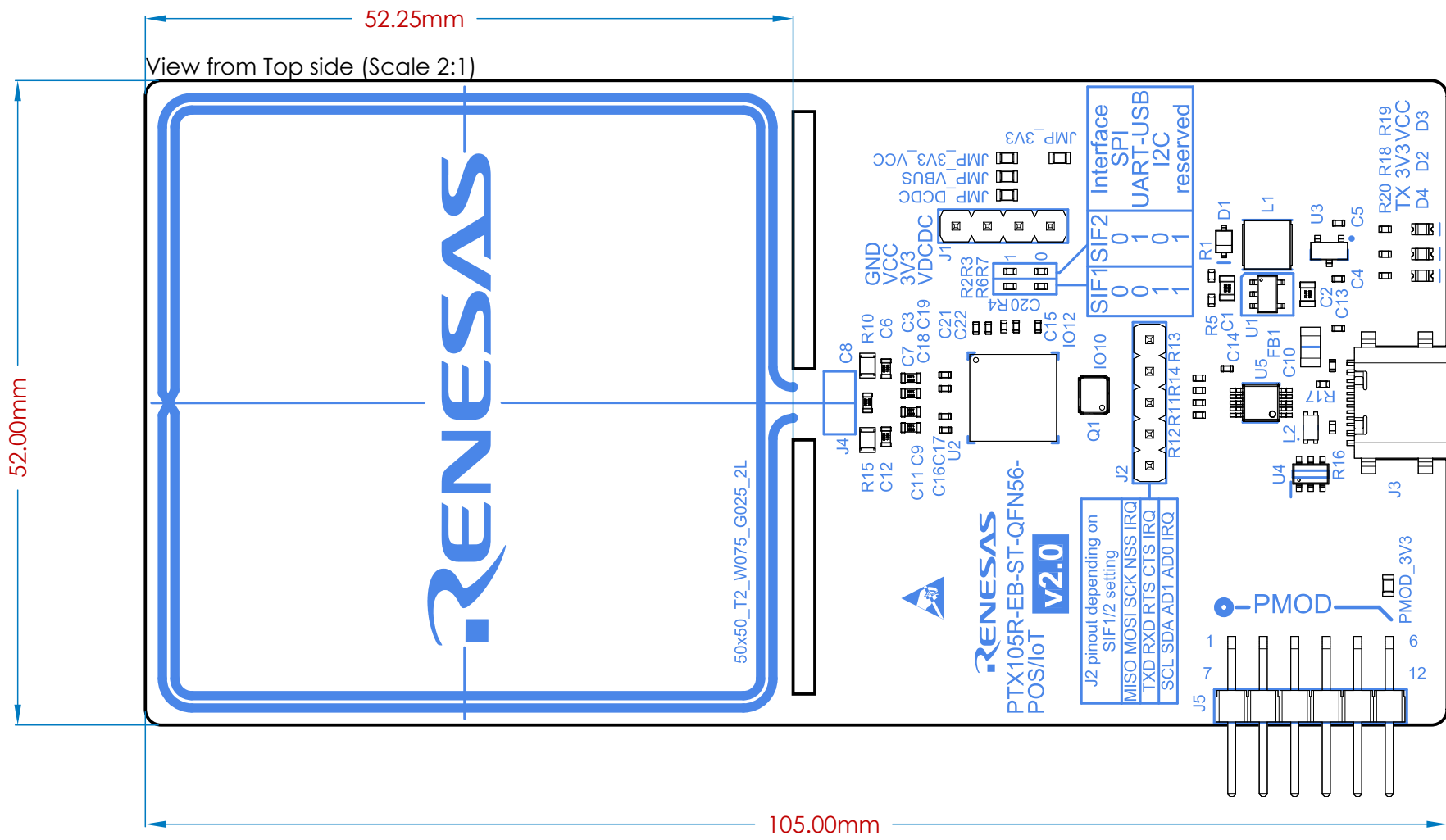
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Interface selection:

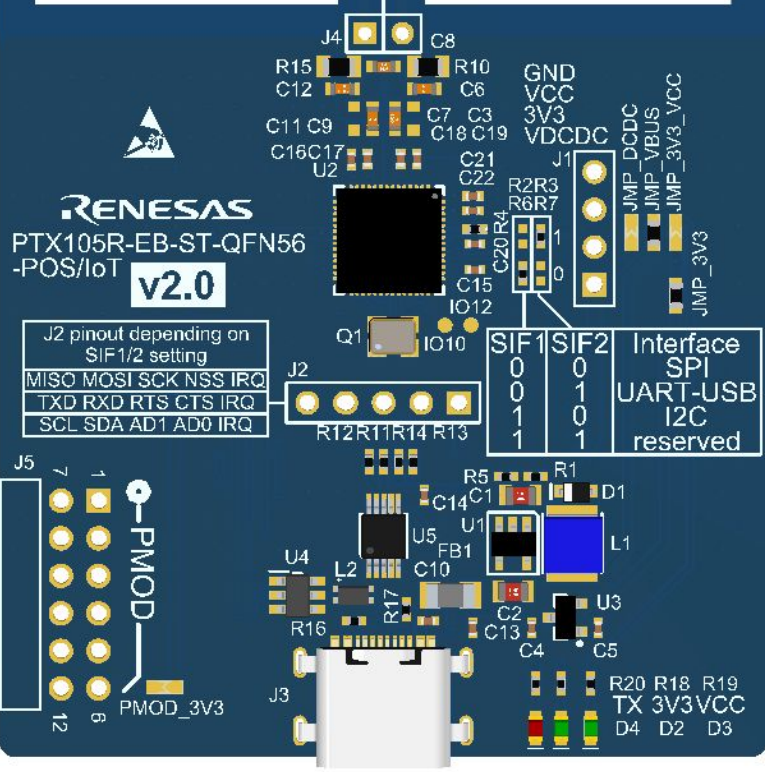
SIF2	SIF1	
0	0	SPI
0	1	I2C
1	0	UART
1	1	na

Title PTX105.SchDoc		Revision: v2.0	EPSPG/CSD	RENESAS
Size: A4	Drawn by: gheh			
Date: 23/11/2023	Time: 15:47:54	Sheet 1 of 1	www.renesas.com	
File: PTX105.SchDoc				



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50x50_T2_W075_G025_2L

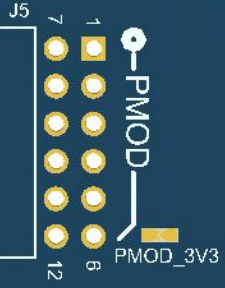


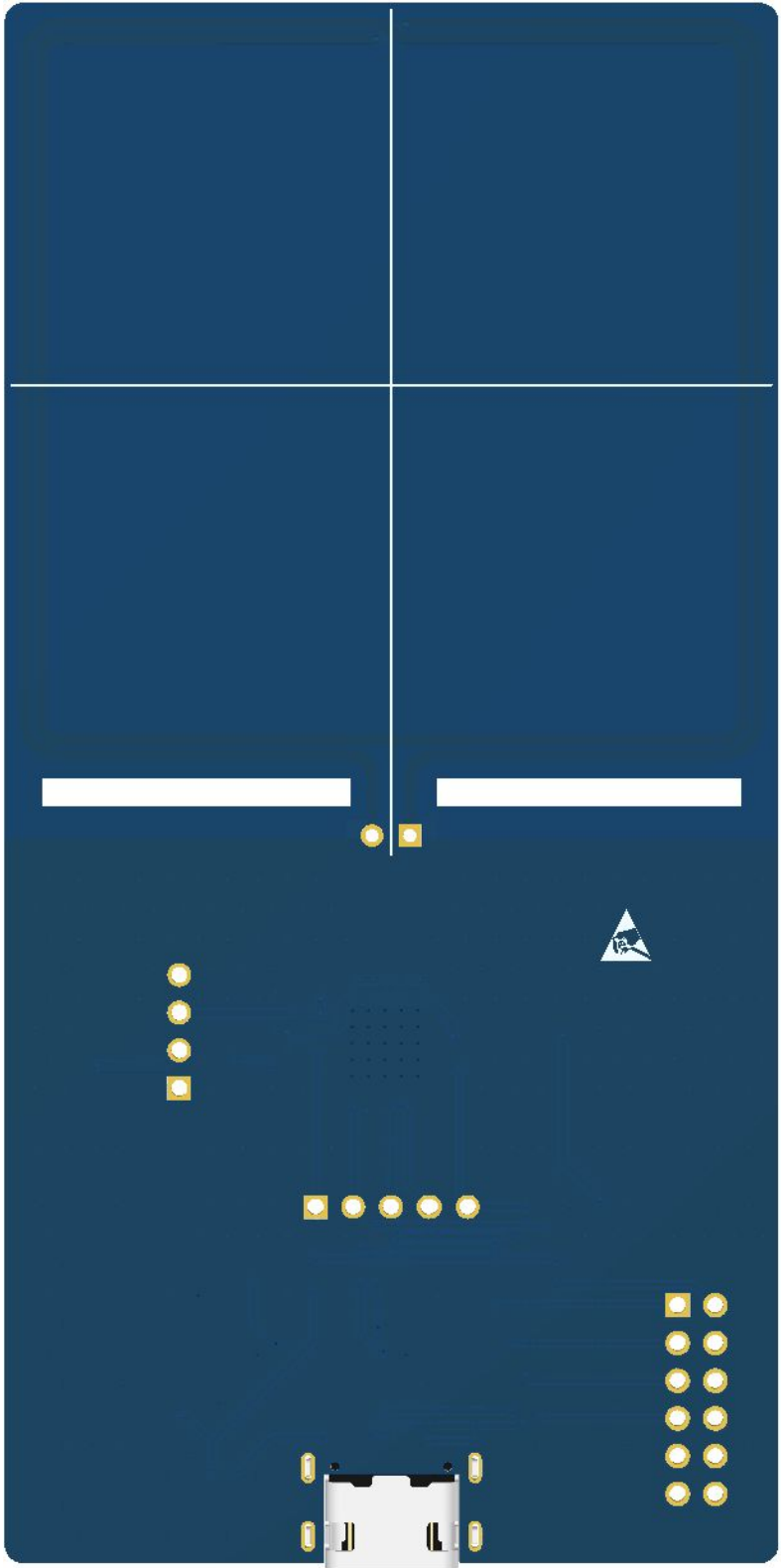
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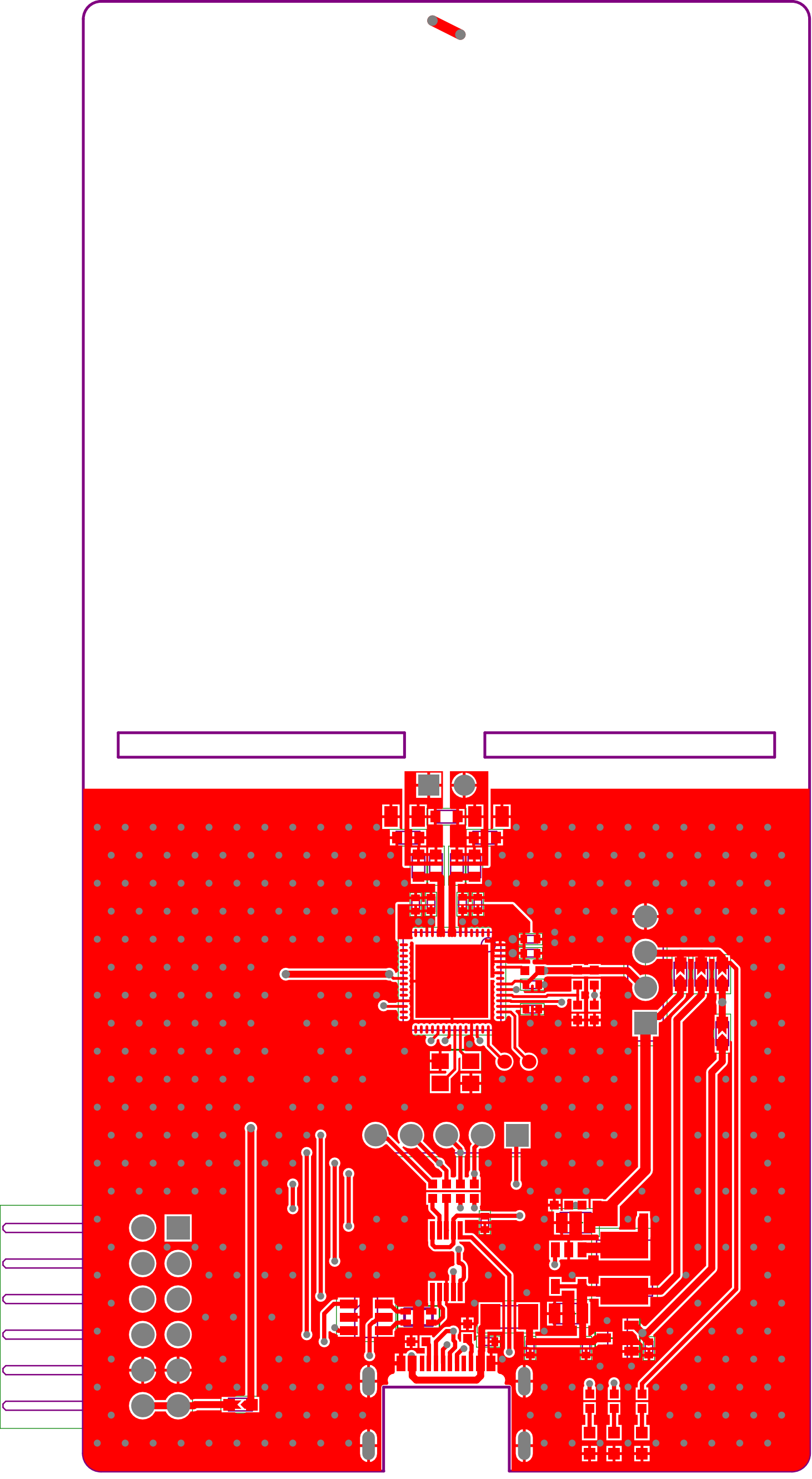
J2 pinout depending on SIF1/2 setting

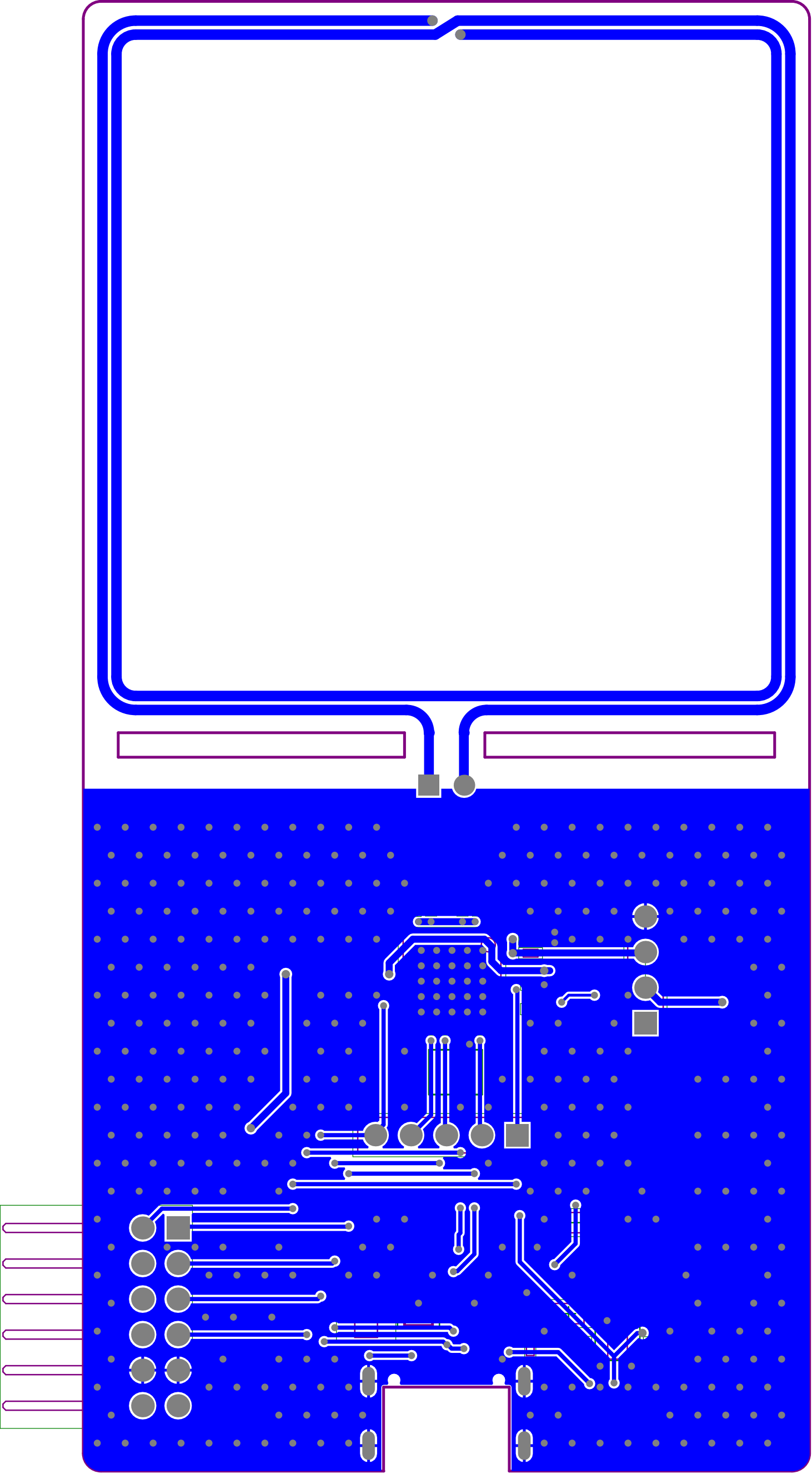
MISO	MOSI	SCK	NSS	IRQ
TXD	RXD	RTS	CTS	IRQ
SCL	SDA	AD1	AD0	IRQ

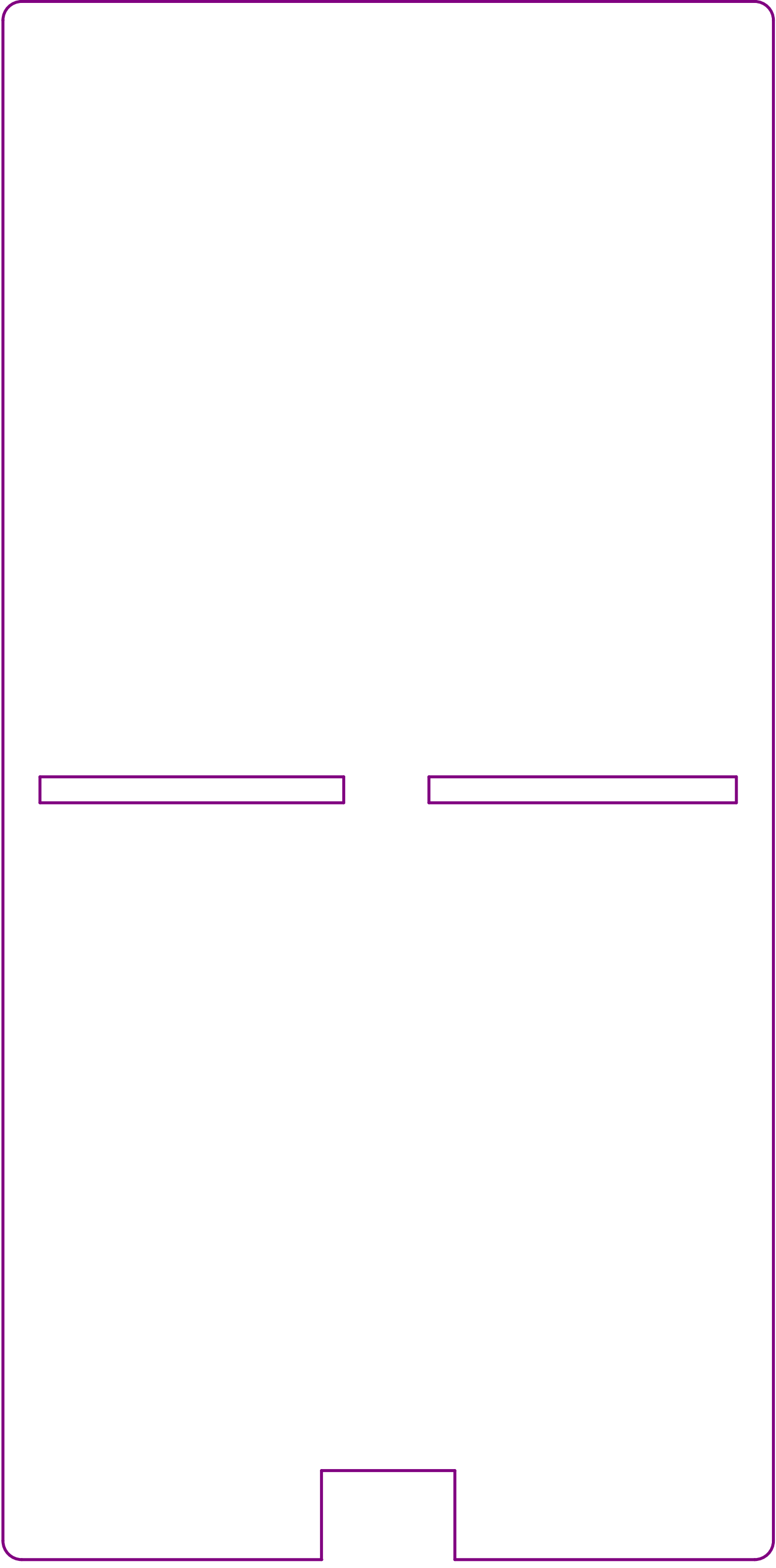
SIF1	SIF2	Interface
0	0	SPI
0	1	UART-USB
1	0	I2C
1	1	reserved











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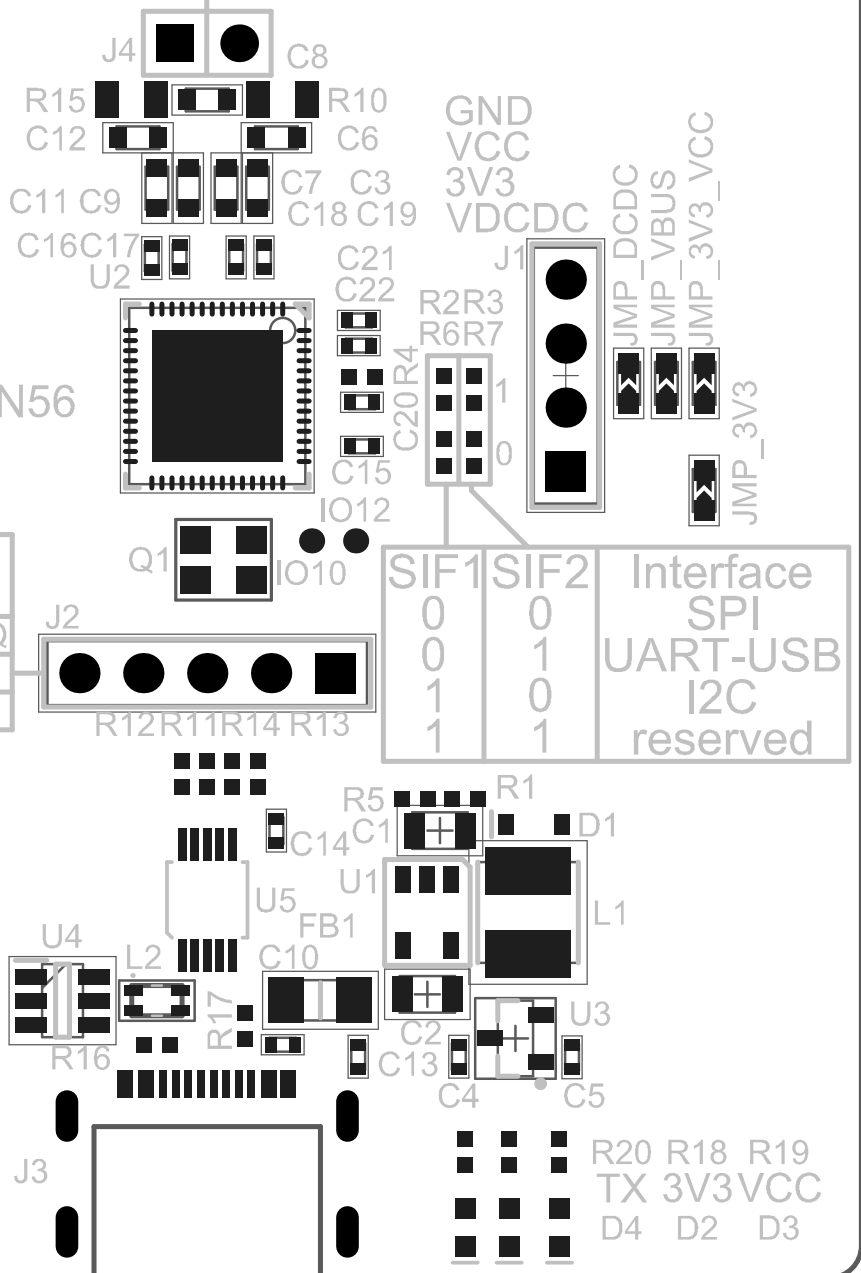
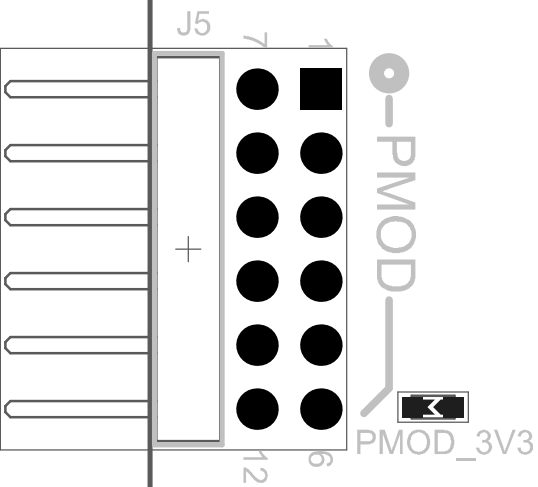
50x50_T2_W075_G025_2L

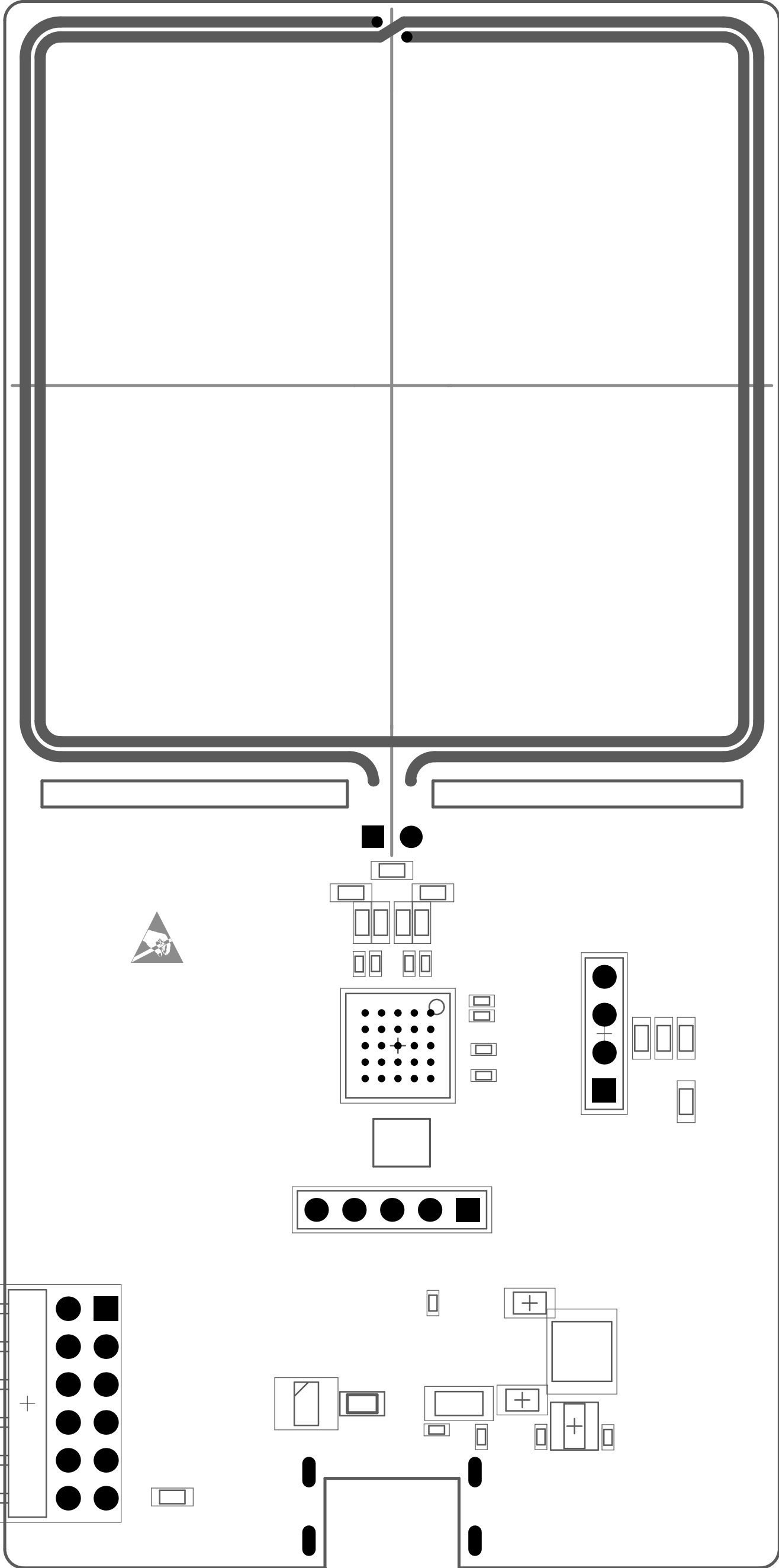

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J2 pinout depending on SIF1/2 setting

MISO	MOSI	SCK	NSS	IRQ
TXD	RXD	RTS	CTS	IRQ
SCL	SDA	AD1	AD0	IRQ

SIF1	SIF2	Interface SPI UART-USB I2C reserved
0	0	
0	1	
1	0	
1	1	





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