

PTX130R-EB-ST-QFN56-POS/IoT v1.1Ren

This document provides an overview of the hardware comprising the PTX130R-EB-ST-QFN56-POS/IoT v1.1Ren (PTX130R-EB) evaluation board.

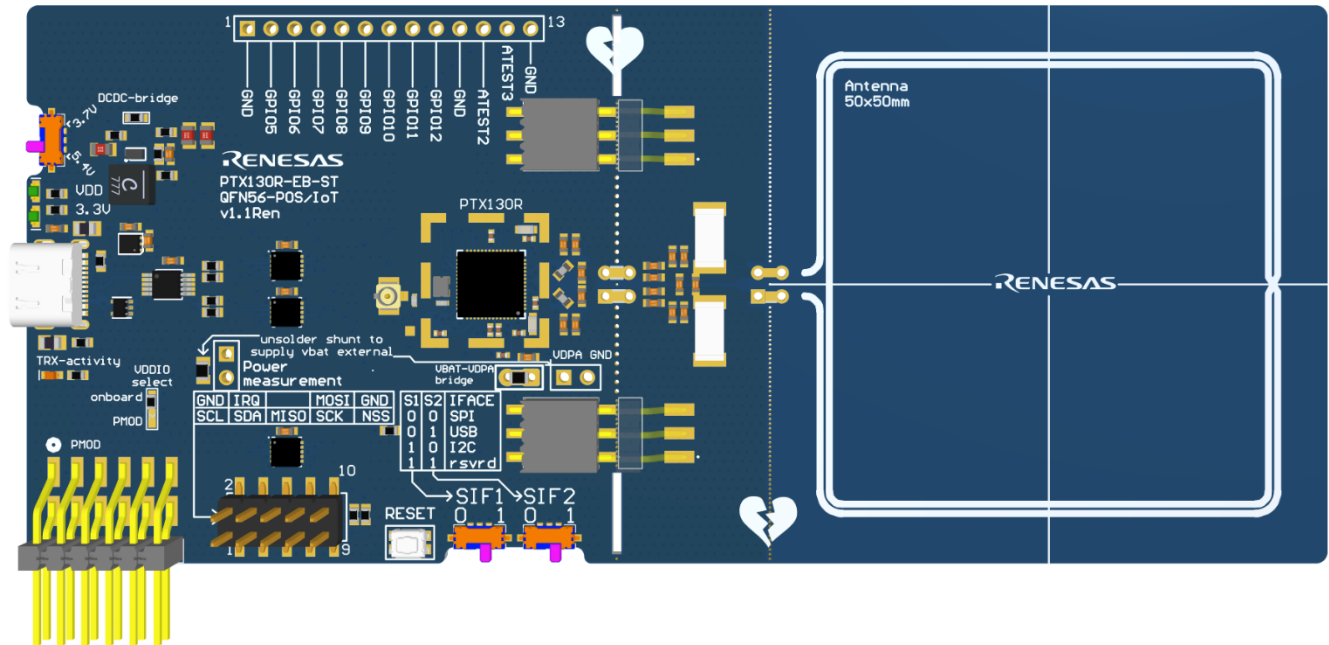


Figure 1. PTX130R-EB-ST-QFN56-POS/IoT v1.1Ren Board

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1. Power Supply

The PTX130R-EB board is powered via a USB-C connection. The board can be operated in two voltage settings (3.7V and 5.4V) that are selected by SW200 on the left side of the board.



The board's default is 5.4V, which is also the setting used for all compliance tests.

2. USB Interface

The USB Interface is handled by an CH340E USB <-> UART bridge. Driver installation is automatic on Windows® 10.

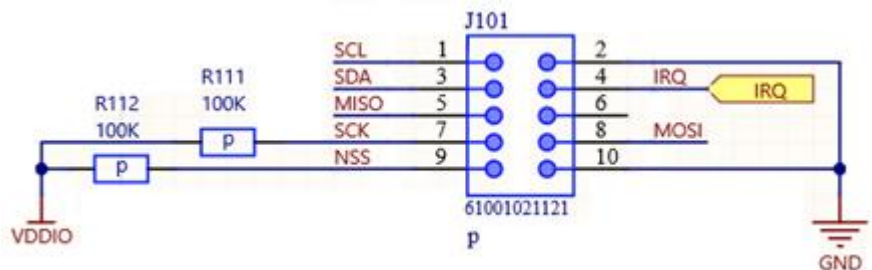
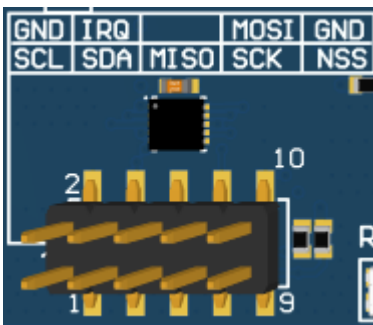
If automatic installation fails or you have an older version of Windows, download the drivers from the manufacturer's [website](#).

3. Interface Switching

The PTX130R-EB board allows to switch between the three interfaces supported by the PTX130R device using the SIF1 / SIF2 switches.

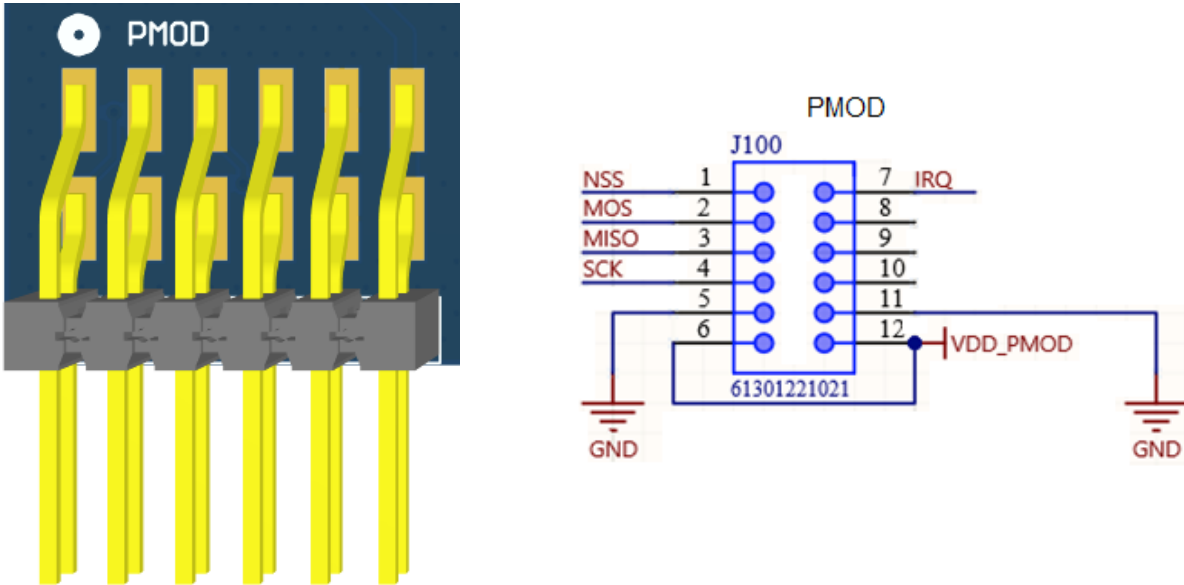
SIF1	SIF2	Interface	Picture of switches to be used:
0	0	SPI	
0	1	UART → USB	
1	0	I ² C	

The UART Interface is connected to the USB bridge and can be accessed via the USB-C plug. SPI and I²C are connected to a 2 x 5-pin header on the low side of the board:



4. PMOD

SPI is also available via a PMOD 2 x 6-pin connector. The PMOD connector allows connecting to a multitude of MCU demo boards. Example firmware is available for the TB-S3A1 board from Renesas.



5. Logic Level

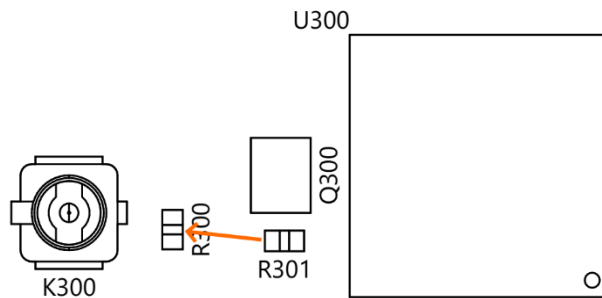
By default, the chip logic level is set to the on-board generated 3.3V (JMP302 in the “onboard” position).

However, it can also be defined from the PMOD connector. If JMP302 is in the PMOD position the voltage level on pins 6 and 12 of the PMOD connector will define the communication logic level.

Values between 1.8V and 5.5V are acceptable.

6. Clocking

The PTX130R device’s default clock source is a 27MHz crystal (Q300). The board gives the possibility to use an external clock source instead. For this, the 0R jumper R301 must be moved to position R300.



When completed, an external clock can be supplied via the U.FL plug K300.

7. Debugging

The PCB has three debug LEDs.

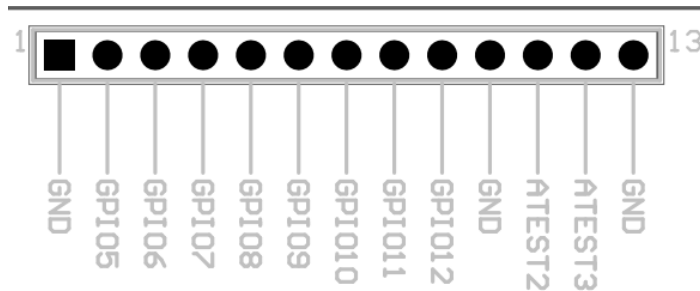


Two above the USB plug for supply.



One below the USB plug for UART communication.

In addition, GPIO5 to GPIO12 and ATEST2/3 are accessible via a pin header on the top of the board.



8. Power Consumption

Component	Typical Consumption [mA]
CH340E	12
NX3L4684TK	0.0003
TLV75533	0.025
TPS63036	0.025
PTX130 (0% sine)	43
PTX130 (100% sine)	372

Total consumption on USB port:

- Differential mode: 436mA, 2.066W
- Single ended mode: 346mA, 1.71W

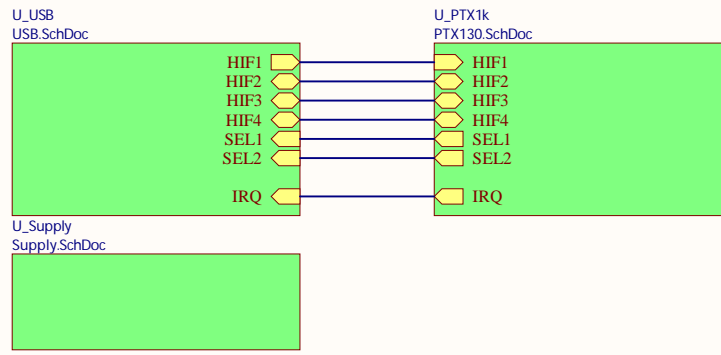
9. Schematics


See the schematics located at the end of this document.

10. Revision History

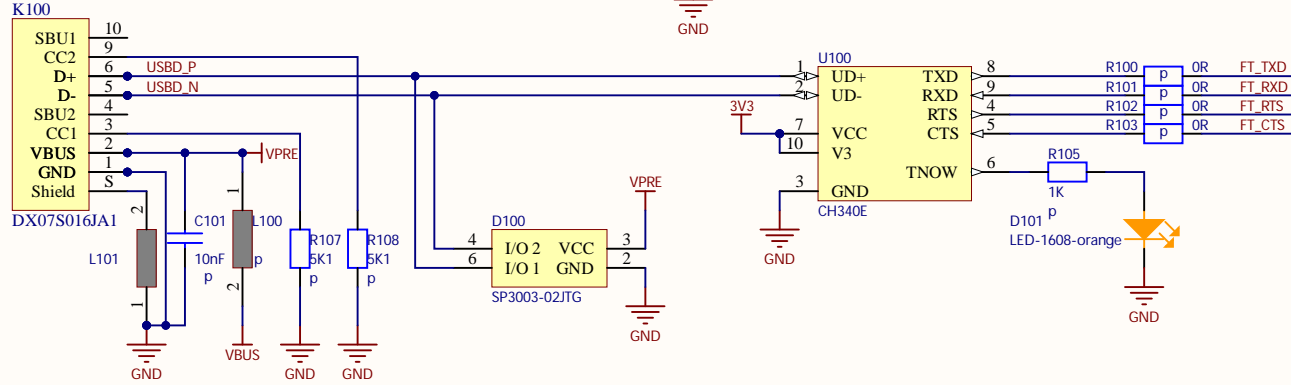
Revision	Date	Description
1.00	Oct 3, 2024	Initial release.

PTX130R-EB-ST-QFN56-POS/IoT

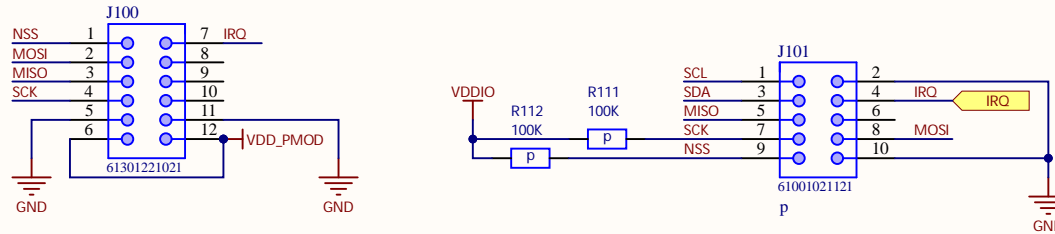


Title Top.SchDoc			EPSPG/CSD	 www.renesas.com
Size: A4	Drawn by: gheh	Revision: v1.1Ren		
Date: 24/11/2023	Time: 11:26:18	Sheet 1 of 4		
File: Top.SchDoc				

USB-C

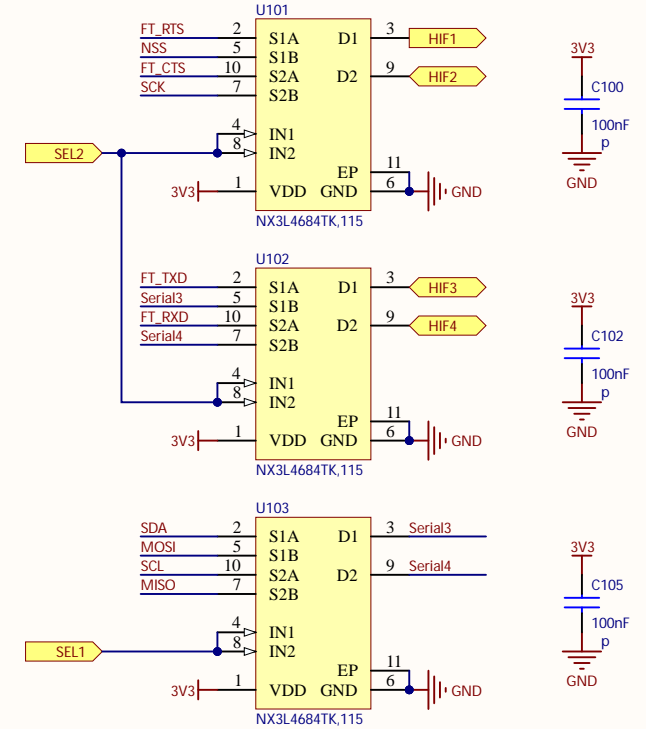


PMOD



PIN - SPI - I2C - UART
 HIF1 - NSS - ADDR0 - CTS
 HIF2 - SCK - ADDR1 - RTS
 HIF3 - MOSI - SDA - RXD
 HIF4 - MISO - SCL - TXD

1) LSBs of I2C address, evaluated at boot



Title **USB.SchDoc**

Size: **A4**

Drawn by: **gheh**

Revision: **v1.1Ren**

EPSPG/CSD **RENESAS**

Date: **24/11/2023**

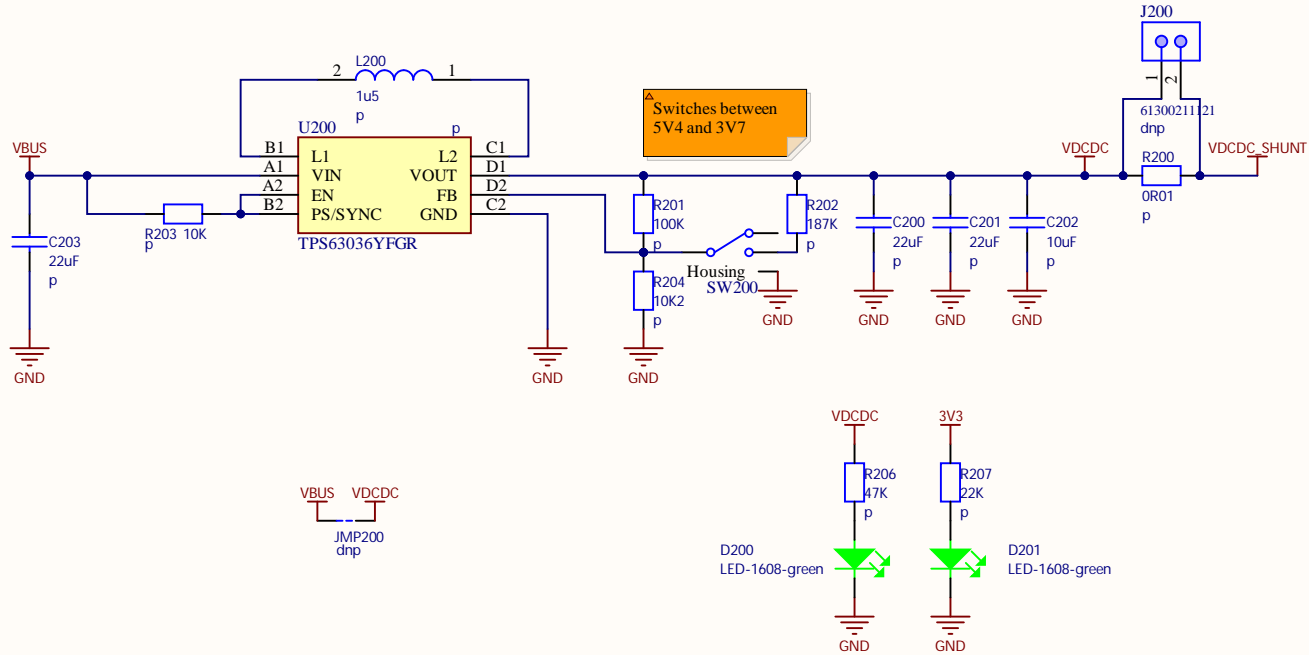
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Sheet **2** of **4**

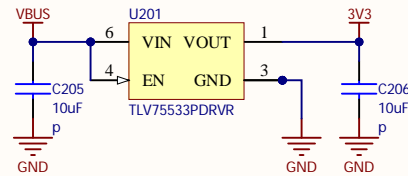
www.renesas.com

File: **USB.SchDoc**

5V Supply

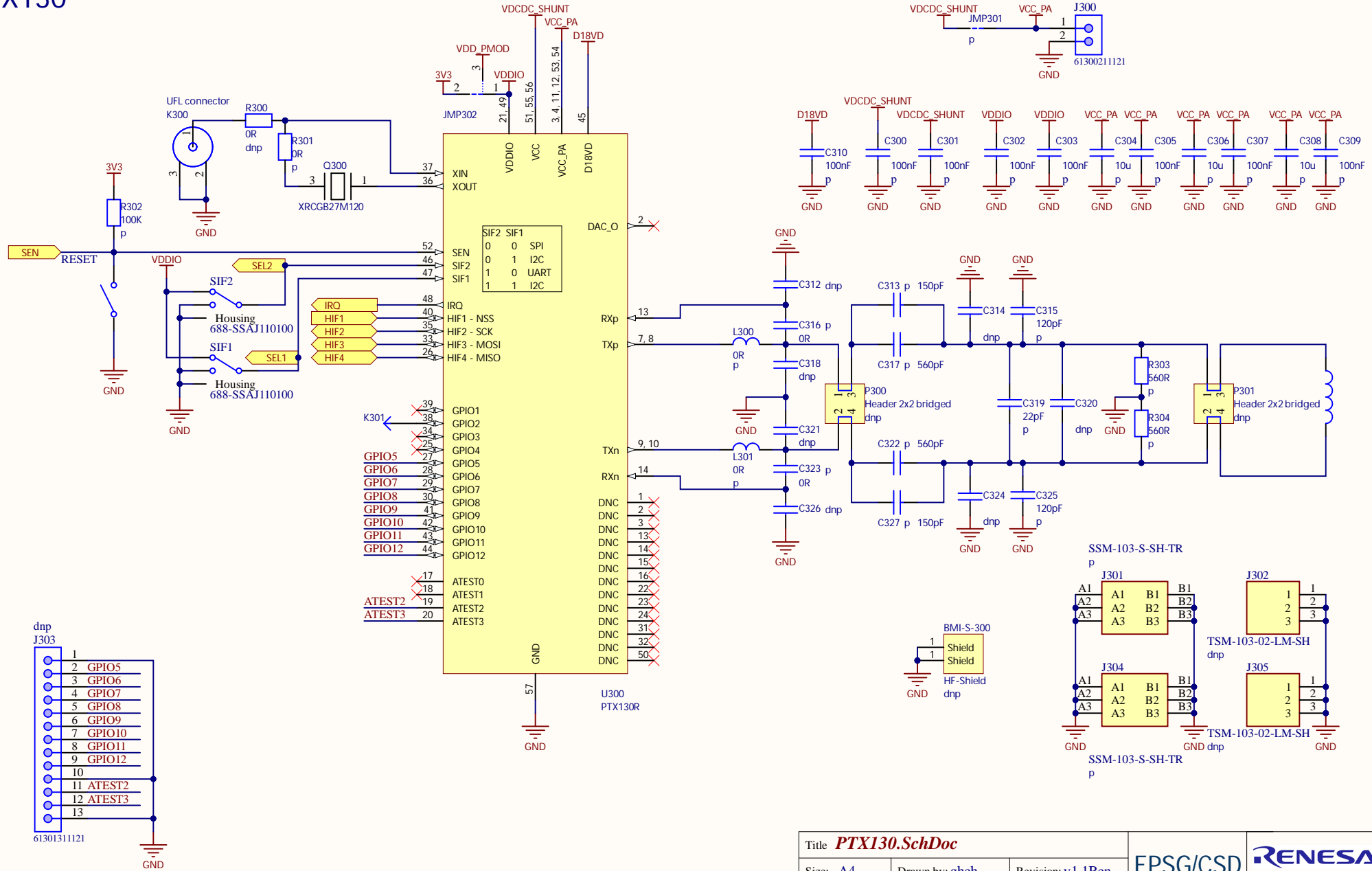


3V3 Supply



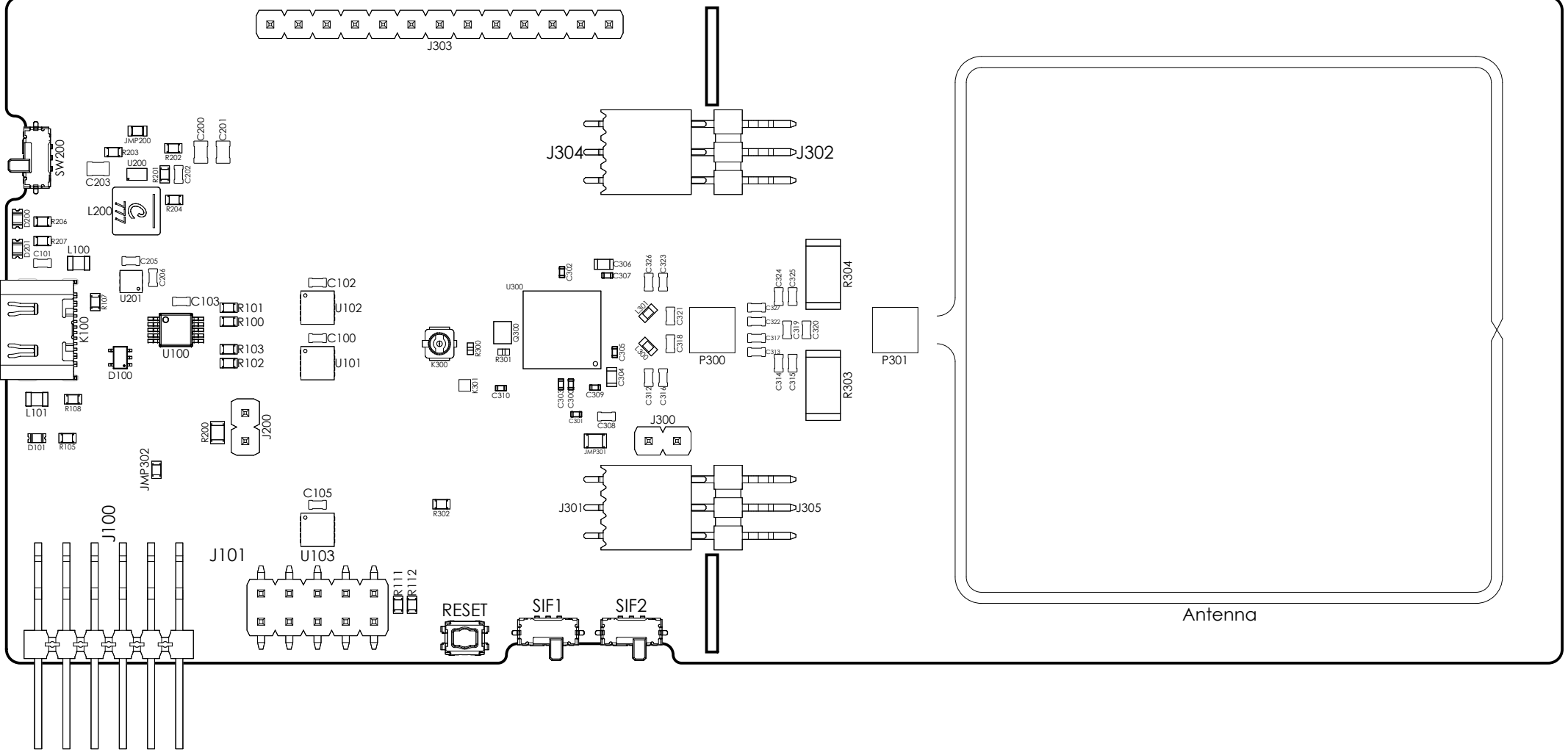
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Size: A4	Drawn by: gheh	Revision: v1.1Ren		
Date: 24/11/2023	Time: 11:26:19	Sheet 3 of 4		
File: Supply.SchDoc				


PTX130



Title PTX130.SchDoc			EPSPG/CSD	RENESAS
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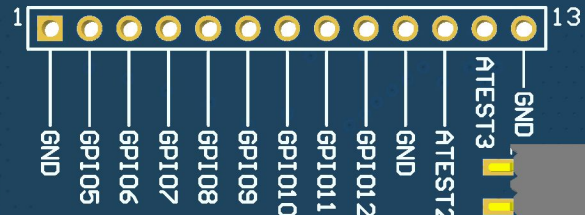
View from Top side (Scale 2:1)



Title: Assembly Top		Size: A4	 www.renesas.com
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File: Assembly.PCBDwf			

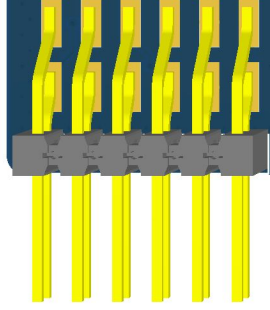
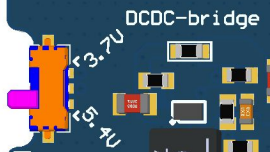
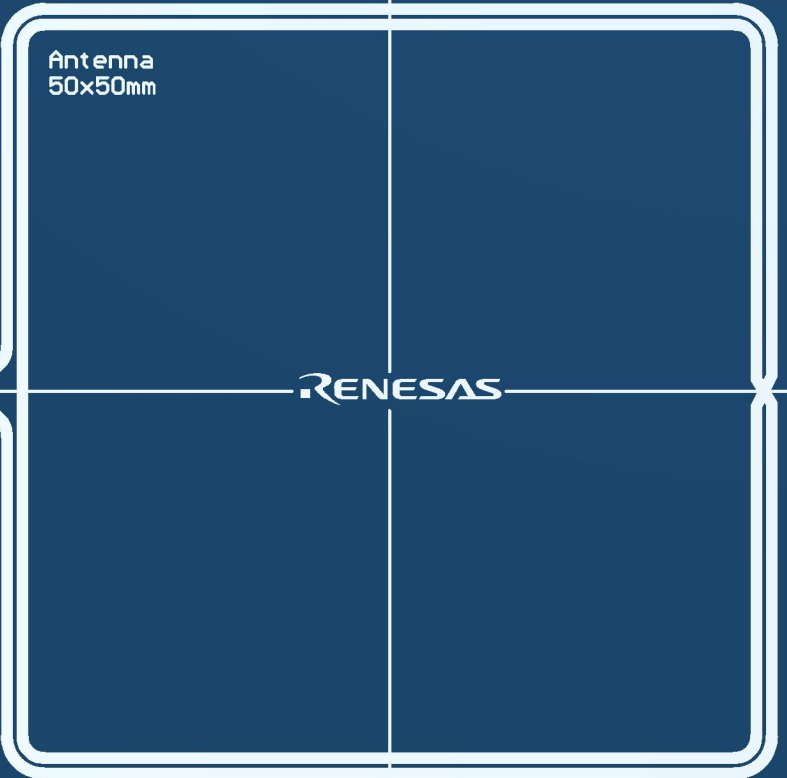
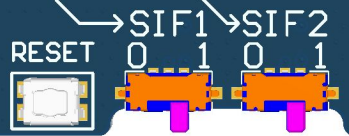
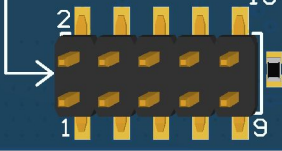
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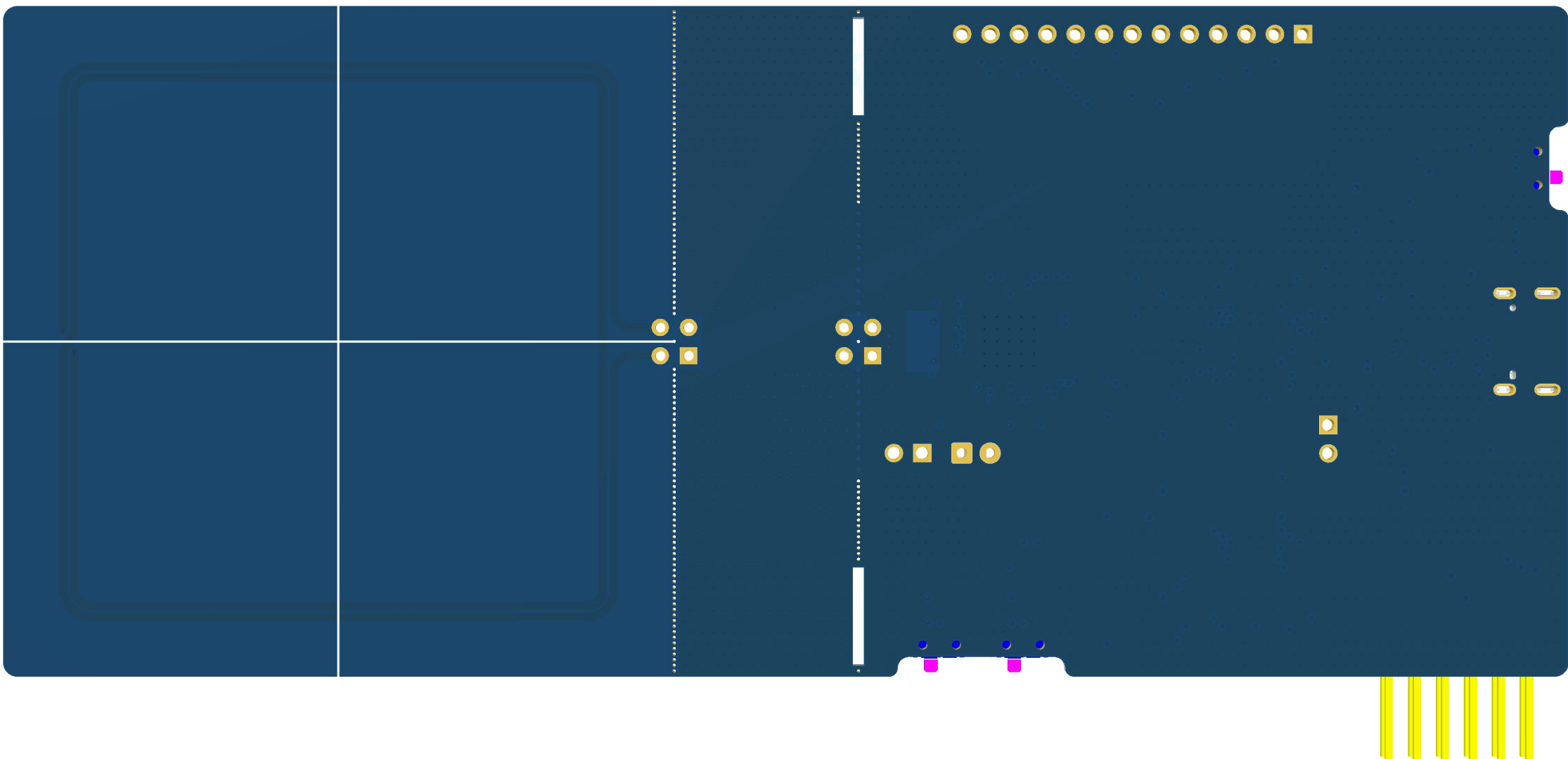
PTX130R



GND	IRQ	MOSI	GND
SCL	SDA	MISO	SCK
		NSS	

S1	S2	IFACE
0	0	SPI
0	1	USB
1	0	I2C
1	1	rsvrd





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