User's Manual

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R5R0C0B Group

User's Manual: Hardware

RENESAS MCU
R8C Family / R8C/3x Series

Renesas Electronics
www.renesas.com

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(2012.4)

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

How to Use This Manual

1. Purpose and Target Readers

This manual is designed to provide the user with an understanding of the hardware functions and electrical characteristics of the MCU. It is intended for users designing application systems incorporating the MCU. A basic knowledge of electric circuits, logical circuits, and MCUs is necessary in order to use this manual.
The manual comprises an overview of the product; descriptions of the CPU, system control functions, peripheral functions, and electrical characteristics; and usage notes.

Particular attention should be paid to the precautionary notes when using the manual. These notes occur within the body of the text, at the end of each section, and in the Usage Notes section.

The revision history summarizes the locations of revisions and additions. It does not list all revisions. Refer to the text of the manual for details.

The following documents apply to the R5R0C0B Group. Make sure to refer to the latest versions of these documents. The newest versions of the documents listed may be obtained from the Renesas Electronics Web site.

Document Type	Description	Document Title	Document No.
Datasheet	Hardware overview and electrical characteristics	R5R0C0B Group Datasheet	—
User's manual: Hardware	Hardware specifications (pin assignments, memory maps, peripheral function specifications, electrical characteristics, timing charts) and operation description Note: Refer to the application notes for details on using peripheral functions.	R5R0C0B Group User's Manual: Hardware	This User's manual
User's manual: Software	Description of CPU instruction set	R8C/Tiny Series Software Manual	REJ09B0001
Application note	Information on using peripheral functions and application examples Sample programs Information on writing programs in assembly language and C	Available from Renesas Electronics Web site.	
Renesas technical update	Product specifications, updates on documents, etc.		

2. Notation of Numbers and Symbols

The notation conventions for register names, bit names, numbers, and symbols used in this manual are described below.

(1) Register Names, Bit Names, and Pin Names
Registers, bits, and pins are referred to in the text by symbols. The symbol is accompanied by the word “register,” “bit,” or “pin” to distinguish the three categories.
Examples the PM03 bit in the PM0 register
P3_5 pin, VCC pin

(2) Notation of Numbers
The indication “b” is appended to numeric values given in binary format. However, nothing is appended to the values of single bits. The indication “h” is appended to numeric values given in hexadecimal format. Nothing is appended to numeric values given in decimal format.
Examples Binary: 11b
Hexadecimal: EFA0h
Decimal: 1234

3. Register Notation

The symbols and terms used in register diagrams are described below.

x.x.x XXX Register (Symbol)

Address XXXXh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	XXX7	XXX6	XXX5	XXX4	—	—	XXX1	XXX0
After Reset	0	0	0	0	0	0	0	0

*1

Bit	Symbol	Bit Name	Function	R/W
b0	XXX0	XXX bit	b1 b0 0 0: XXX 0 1: XXX 1 0: Do not set. 1 1: XXX	R/W
b1	XXX1			R/W
b2	—	Nothing is assigned. If necessary, set to 0. When read, the content is undefined.		—
b3	—	Reserved bit	Set to 0.	R/W
b4	XXX4	XXX bit	Function varies according to the operating mode.	R/W
b5	XXX5			W
b6	XXX6			R/W
b7	XXX7	XXX bit	0: XXX 1: XXX	R

*2 *3

*1

R/W: Read and write.
R: Read only.
W: Write only.
—: Nothing is assigned.

*2

- Reserved bit

  Reserved bit. Set to specified value.

*3

- Nothing is assigned.

  Nothing is assigned to the bit. As the bit may be used for future functions, if necessary, set to 0.
- Do not set to a value.

  Operation is not guaranteed when a value is set.
- Function varies according to the operating mode.

  The function of the bit varies with the peripheral function mode. Refer to the register diagram for information on the individual modes.

4. List of Abbreviations and Acronyms

Abbreviation	Full Form
ACIA	Asynchronous Communication Interface Adapter
bps	bits per second
CRC	Cyclic Redundancy Check
DMA	Direct Memory Access
DMAC	Direct Memory Access Controller
GSM	Global System for Mobile Communications
Hi-Z	High Impedance
IEBus	Inter Equipment Bus
I/O	Input/Output
IrDA	Infrared Data Association
LSB	Least Significant Bit
MSB	Most Significant Bit
NC	Non-Connection
PLL	Phase Locked Loop
PWM	Pulse Width Modulation
SIM	Subscriber Identity Module
UART	Universal Asynchronous Receiver/Transmitter
VCO	Voltage Controlled Oscillator

Table of Contents

SFR Page Reference

Address	Register	Symbol	Page
0000h			
0001h			
0002h			
0003h			
0004h	Processor Mode Register 0	PM0	28
0005h	Processor Mode Register 1	PM1	161
0006h	System Clock Control Register 0	CM0	94
0007h	System Clock Control Register 1	CM1	95
0008h	Module Standby Control Register	MSTCR	229
0009h	System Clock Control Register 3	CM3	96
000Ah	Protect Register	PRCR	121
000Bh	Reset Source Determination Register	RSTFR	28
000Ch	Oscillation Stop Detection Register	OCD	97
000Dh	Watchdog Timer Reset Register	WDTR	161
000Eh	Watchdog Timer Start Register	WDTS	161
000Fh	Watchdog Timer Control Register	WDTC	162
0010h			
0011h			
0012h			
0013h			
0014h			
0015h	High-Speed On-Chip Oscillator Control Register 7	FRA7	97
0016h			
0017h			
0018h			
0019h			
001Ah			
001Bh			
001Ch	Count Source Protection Mode Register	CSPR	162
001Dh			
001Eh			
001Fh			
0020h			
0021h			
0022h			
0023h	High-Speed On-Chip Oscillator Control Register 0	FRA0	98
0024h	High-Speed On-Chip Oscillator Control Register 1	FRA1	98
0025h	High-Speed On-Chip Oscillator Control Register 2	FRA2	99
0026h			
0027h			
0028h	Clock Prescaler Reset Flag	CPSRF	99
0029h	High-Speed On-Chip Oscillator Control Register 4	FRA4	100
002Ah	High-Speed On-Chip Oscillator Control Register 5	FRA5	100
002Bh	High-Speed On-Chip Oscillator Control Register 6	FRA6	100
002Ch			
002Dh			
002Eh			
002Fh	High-Speed On-Chip Oscillator Control Register 3	FRA3	100
0030h	Voltage Monitor Circuit Control Register	CMPA	41
0031h	Voltage Monitor Circuit Edge Select Register	VCAC	42
0032h			
0033h	Voltage Detect Register 1	VCA1	42
0034h	Voltage Detect Register 2	VCA2	43, 101
0035h			
0036h	Voltage Detection 1 Level Select Register	VD1LS	44
0037h			
0038h	Voltage Monitor 0 Circuit Control Register	VW0C	45
0039h	Voltage Monitor 1 Circuit Control Register	VW1C	46
003Ah	Voltage Monitor 2 Circuit Control Register	VW2C	47
003Bh			
003Ch			
003Dh			
003Eh			
003Fh			

Address	Register	Symbol	Page
0040h			
0041h	Flash Memory Ready Interrupt Control Register	FMRDYIC	128
0042h			
0043h			
0044h			
0045h			
0046h			
0047h	Timer RC Interrupt Control Register	TRCIC	128
0048h			
0049h			
004Ah			
004Bh			
004Ch			
004Dh	Key Input Interrupt Control Register	KUPIC	127
004Eh			
004Fh			
0050h			
0051h	UART0 Transmit Interrupt Control Register	S0TIC	127
0052h	UART0 Receive Interrupt Control Register	S0RIC	127
0053h			
0054h			
0055h	INT2 Interrupt Control Register	INT2IC	129
0056h	Timer RA Interrupt Control Register	TRAIC	127
0057h			
0058h	Timer RB Interrupt Control Register	TRBIC	127
0059h	INT1 Interrupt Control Register	INT1IC	129
005Ah	INT3 Interrupt Control Register	INT3IC	129
005Bh			
005Ch			
005Dh	INT0 Interrupt Control Register	INT0IC	129
005Eh			
005Fh			
0060h			
0061h			
0062h			
0063h			
0064h			
0065h			
0066h			
0067h			
0068h			
0069h			
006Ah	Sensor Control Unit Interrupt Control Register	SCUIC	127
006Bh			
006Ch			
006Dh			
006Eh			
006Fh			
0070h			
0071h			
0072h	Voltage Monitor 1 Interrupt Control Register	VCMP1IC	127
0073h	Voltage Monitor 2 Interrupt Control Register	VCMP2IC	127
0074h			
0075h			
0076h			
0077h			
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0079h			
007Ah			
007Bh			
007Ch			
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Note:
1. The blank regions are reserved. Do not access locations in these regions.

Address	Register	Symbol	Page
0080h	DTC Activation Control Register	DTCTL	173
0081h			
0082h			
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0088h	DTC Activation Enable Register 0	DTCEN0	172
0089h	DTC Activation Enable Register 1	DTCEN1	172
008Ah	DTC Activation Enable Register 2	DTCEN2	172
008Bh	DTC Activation Enable Register 3	DTCEN3	172
008Ch			
008Dh	DTC Activation Enable Register 5	DTCEN5	172
008Eh	DTC Activation Enable Register 6	DTCEN6	172
008Fh			
0090h			
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0097h			
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0099h			
009Ah			
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009Ch			
009Dh			
009Eh			
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00A1h	UART0 Bit Rate Register	U0BRG	278
00A2h	UART0 Transmit Buffer Register	U0TB	279
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00A5h	UART0 Transmit/Receive Control Register 1	U0C1	280
00A6h	UART0 Receive Buffer Register	U0RB	281
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00A8h			
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00AAh			
00ABh			
00ACh			
00ADh			
00AEh			
00AFh			
00B0h			
00B1h			
00B2h			
00B3h			
00B4h			
00B5h			
00B6h			
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00B8h			
00B9h			
00BAh			
00BBh			
00BCh			
00BDh			
00BEh			
00BFh			

Address	Register	Symbol	Page
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00C3h			
00C4h			
00C5h			
00C6h			
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00C8h			
00C9h			
00CAh			
00CBh			
00CCh			
00CDh			
00CEh			
00CFh			
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00D1h			
00D2h			
00D3h			
00D4h			
00D5h			
00D6h			
00D7h			
00D8h			
00D9h			
00DAh			
00DBh			
00DCh			
00DDh			
00DEh			
00DFh			
00E0h	Port P0 Register	P0	64
00E1h	Port P1 Register	P1	64
00E2h	Port P0 Direction Register	PD0	63
00E3h	Port P1 Direction Register	PD1	63
00E4h			
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00E6h			
00E7h	Port P3 Direction Register	PD3	63
00E8h	Port P4 Register	P4	64
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00EBh			
00ECh			
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00F9h			
00FAh			
00FBh			
00FCh			
00FDh			
00FEh			
00FFh			

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0100h	Timer RA Control Register	TRACR	190
0101h	Timer RA I/O Control Register	TRAIOC	190, 193, 196, 198, 200, 203
0102h	Timer RA Mode Register	TRAMR	191
0103h	Timer RA Prescaler Register	TRAPRE	191
0104h	Timer RA Register	TRA	192
0105h			
0106h			
0107h			
0108h	Timer RB Control Register	TRBCR	207
0109h	Timer RB One-Shot Control Register	TRBOCR	207
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010Bh	Timer RB Mode Register	TRBMR	208
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Address	Register	Symbol	Page
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014Eh			
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0150h			
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0152h			
0153h			
0154h			
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0160h			
0161h			
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016Bh			
016Ch			
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0176h			
0177h			
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Address	Register	Symbol	Page
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01A3h			
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01C1h			
01C2h			
01C3h	Address Match Interrupt Enable Register 0	AIER0	145
01C4h	Address Match Interrupt Register 1	RMAD1	145
01C5h			
01C6h			
01C7h	Address Match Interrupt Enable Register 1	AIER1	145
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01C9h			
01CAh			
01CBh			
01CCh			
01CDh			
01CEh			
01CFh			
01D0h			
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01D2h			
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01D4h			
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01D6h			
01D7h			
01D8h			
01D9h			
01DAh			
01DBh			
01DCh			
01DDh			
01DEh			
01DFh			

Note:
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02C7h	SCU Channel Control Counter	SCUCHC	313
02C8h	SCU Flag Register	SCUFR	314
02C9h	SCU Status Counter Register	SCUSTC	315
02CAh	SCU Secondary Counter Set Register	SCSCSR	315
02CBh	SCU Secondary Counter Register	SCUSCC	315
02CCh			
02CDh			
02CEh	SCU Destination Address Register	SCUDAR	316
02CFh			
02D0h	SCU Data Buffer Register	SCUDBR	317
02D1h			
02D2h	SCU Primary Counter Register	SCUPRC	318
02D3h			
02D4h	SCU Random Value Store Register 0	SCRVR0	319
02D5h	SCU Random Value Store Register 1	SCRVR1	319
02D6h	SCU Random Value Store Register 2	SCRVR2	319
02D7h	SCU Random Value Store Register 3	SCRVR3	320
02D8h	SCU Random Value Store Register 4	SCRVR4	320
02D9h	SCU Random Value Store Register 5	SCRVR5	320
02DAh	SCU Random Value Store Register 6	SCRVR6	321
02DBh	SCU Random Value Store Register 7	SCRVR7	321
02DCh	SCU Input Enable Register 0	TSIER0	322
02DDh			
02DEh			
02DFh			

Note:
1. The blank regions are reserved. Do not access locations in these regions.

Address	Register	Symbol	Page
2C00h	DTC Transfer Vector Area		
2C01h	DTC Transfer Vector Area		
2C02h	DTC Transfer Vector Area		
2C03h	DTC Transfer Vector Area		
2C04h	DTC Transfer Vector Area		
2C05h	DTC Transfer Vector Area		
2C06h	DTC Transfer Vector Area		
2C07h	DTC Transfer Vector Area		
2C08h	DTC Transfer Vector Area		
2C09h	DTC Transfer Vector Area		
2C0Ah	DTC Transfer Vector Area		
:	DTC Transfer Vector Area		
:	DTC Transfer Vector Area		
2C3Ah	DTC Transfer Vector Area		
2C3Bh	DTC Transfer Vector Area		
2C3Ch	DTC Transfer Vector Area		
2C3Dh	DTC Transfer Vector Area		
2C3Eh	DTC Transfer Vector Area		
2C3Fh	DTC Transfer Vector Area		
2C40h	DTC Control Data 0	DTCD0	
2C41h			
2C42h			
2C43h			
2C44h			
2C45h			
2C46h			
2C47h			
2C48h	DTC Control Data 1	DTCD1	
2C49h			
2C4Ah			
2C4Bh			
2C4Ch			
2C4Dh			
2C4Eh			
2C4Fh			
2C50h	DTC Control Data 2	DTCD2	
2C51h			
2C52h			
2C53h			
2C54h			
2C55h			
2C56h			
2C57h			
2C58h	DTC Control Data 3	DTCD3	
2C59h			
2C5Ah			
2C5Bh			
2C5Ch			
2C5Dh			
2C5Eh			
2C5Fh			
2C60h	DTC Control Data 4	DTCD4	
2C61h			
2C62h			
2C63h			
2C64h			
2C65h			
2C66h			
2C67h			
2C68h	DTC Control Data 5	DTCD5	
2C69h			
2C6Ah			
2C6Bh			
2C6Ch			
2C6Dh			
2C6Eh			
2C6Fh			
2C70h	DTC Control Data 6	DTCD6	
2C71h			
2C72h			
2C73h			
2C74h			
2C75h			
2C76h			
2C77h			

Address	Register	Symbol	Page
2C78h	DTC Control Data 7	DTCD7	
2C79h			
2C7Ah			
2C7Bh			
2C7Ch			
2C7Dh			
2C7Eh			
2C7Fh			
2C80h	DTC Control Data 8	DTCD8	
2C81h			
2C82h			
2C83h			
2C84h			
2C85h			
2C86h			
2C87h			
2C88h	DTC Control Data 9	DTCD9	
2C89h			
2C8Ah			
2C8Bh			
2C8Ch			
2C8Dh			
2C8Eh			
2C8Fh			
2C90h	DTC Control Data 10	DTCD10	
2C91h			
2C92h			
2C93h			
2C94h			
2C95h			
2C96h			
2C97h			
2C98h	DTC Control Data 11	DTCD11	
2C99h			
2C9Ah			
2C9Bh			
2C9Ch			
2C9Dh			
2C9Eh			
2C9Fh			
2CA0h	DTC Control Data 12	DTCD12	
2CA1h			
2CA2h			
2CA3h			
2CA4h			
2CA5h			
2CA6h			
2CA7h			
2CA8h	DTC Control Data 13	DTCD13	
2CA9h			
2CAAh			
2CABh			
2CACh			
2CADh			
2CAEh			
2CAFh			
2CB0h	DTC Control Data 14	DTCD14	
2CB1h			
2CB2h			
2CB3h			
2CB4h			
2CB5h			
2CB6h			
2CB7h			
2CB8h	DTC Control Data 15	DTCD15	
2CB9h			
2CBAh			
2CBBh			
2CBCh			
2CBDh			
2CBEh			
2CBFh			

Address	Register	Symbol	Page
2CC0h	DTC Control Data 16	DTCD16	
2CC1h			
2CC2h			
2CC3h			
2CC4h			
2CC5h			
2CC6h			
2CC7h			
2CC8h	DTC Control Data 17	DTCD17	
2CC9h			
2CCAh			
2CCBh			
2CCCh			
2CCDh			
2CCEh			
2CCFh			
2CD0h	DTC Control Data 18	DTCD18	
2CD1h			
2CD2h			
2CD3h			
2CD4h			
2CD5h			
2CD6h			
2CD7h			
2CD8h	DTC Control Data 19	DTCD19	
2CD9h			
2CDAh			
2CDBh			
2CDCh			
2CDDh			
2CDEh			
2CDFh			
2CE0h	DTC Control Data 20	DTCD20	
2CE1h			
2CE2h			
2CE3h			
2CE4h			
2CE5h			
2CE6h			
2CE7h			
2CE8h	DTC Control Data 21	DTCD21	
2CE9h			
2CEAh			
2CEBh			
2CECh			
2CEDh			
2CEEh			
2CEFh			
2CF0h	DTC Control Data 22	DTCD22	
2CF1h			
2CF2h			
2CF3h			
2CF4h			
2CF5h			
2CF6h			
2CF7h			
2CF8h	DTC Control Data 23	DTCD23	
2CF9h			
2CFAh			
2CFBh			
2CFCh			
2CFDh			
2CFEh			
2CFFh			
2D00h			
:			
2FFFh			
:			
FFDBh	Option Function Select Register 2	OFS2	30, 157, 164
:			
FFFFh	Option Function Select Register	OFS	29, 48, 156, 163, 345

Note:
1. The blank regions are reserved. Do not access locations in these regions.

1. Overview

1.1 Features

The R5R0C0B Group of single-chip MCUs incorporates the R8C CPU core, employing sophisticated instructions for a high level of efficiency. With 1 Mbyte of address space, and it is capable of executing instructions at high speed. In addition, the CPU core boasts a multiplier for high-speed operation processing.
Power consumption is low, and the supported operating modes allow additional power control. These MCUs are designed to maximize EMI/EMS performance.
Integration of many peripheral functions, including multifunction timer and serial interface, reduces the number of system components.

1.1.1 Applications

Electronic household appliances, office equipment, audio equipment, consumer equipment, etc.

1.1.2 Specifications

Tables 1.1 and 1.2 outline the Specifications for R5R0C0B Group.

Table 1.1 Specifications for R5R0C0B Group (1)

Item	Function	Specification
CPU	Central processing unit	R8C CPU core • Number of fundamental instructions: 89 • Minimum instruction execution time: 50 ns (f(XIN) = 20 MHz, VCC = 2.7 V to 5.5 V) 200 ns (f(XIN) = 5 MHz, VCC = 1.8 V to 5.5 V) • Multiplier: 16 bits × 16 bits → 32 bits • Multiply-accumulate instruction: 16 bits × 16 bits + 32 bits → 32 bits • Operation mode: Single-chip mode (address space: 1 Mbyte)
Memory	ROM, RAM	Refer to **Table 1.3 Product List for R5R0C0B Group**.
Power Supply Voltage Detection	Voltage detection circuit	• Power-on reset • Voltage detection 3 (detection level of voltage detection 0 and voltage detection 1 selectable)
I/O Ports	Programmable I/O ports	• CMOS I/O ports: 20, selectable pull-up resistor • High current drive ports: 20
Clock	Clock generation circuits	• 3 circuits: XIN clock oscillation circuit, High-speed on-chip oscillator (with frequency adjustment function), Low-speed on-chip oscillator • Oscillation stop detection: XIN clock oscillation stop detection function • Frequency divider circuit: Dividing selectable 1, 2, 4, 8, and 16 • Low power consumption modes: Standard operating mode (high-speed clock, high-speed on-chip oscillator, low-speed on-chip oscillator), wait mode, stop mode
Interrupts		• Number of interrupt vectors: 69 • External Interrupt: 7 ($\overline{\text{INT}}$ × 4, Key input × 4) • Priority levels: 7 levels
Watchdog Timer		• 14 bits × 1 (with prescaler) • Reset start selectable • Low-speed on-chip oscillator for watchdog timer selectable
DTC (Data Transfer Controller)		• 1 channel • Activation sources: 17 • Transfer modes: 2 (normal mode, repeat mode)
Timer	Timer RA	8 bits × 1 (with 8-bit prescaler) Timer mode (period timer), pulse output mode (output level inverted every period), event counter mode, pulse width measurement mode, pulse period measurement mode
	Timer RB	8 bits × 1 (with 8-bit prescaler) Timer mode (period timer), programmable waveform generation mode (PWM output), programmable one-shot generation mode, programmable wait one-shot generation mode
	Timer RC	16 bits × 1 (with 4 capture/compare registers) Timer mode (input capture function, output compare function), PWM mode (output 3 pins), PWM2 mode (PWM output pin)

Table 1.2 Specifications for R5R0C0B Group (2)

Item	Function	Specification
Serial Interface	UART0	Clock synchronous serial I/O/UART
Sensor Control Unit		System CH × 3, electrostatic capacitive touch detection × 8
Flash Memory		• Programming and erasure voltage: VCC = 2.7 V to 5.5 V • Programming and erasure endurance: 1,000 times (program ROM) • Program security: ROM code protect, ID code check • Debug functions: On-chip debug, on-board flash rewrite function
Operating Frequency/Supply Voltage		f(XIN) = 20 MHz (VCC = 2.7 V to 5.5 V) f(XIN) = 5 MHz (VCC = 1.8 V to 5.5 V)
Current Consumption		Typ. 6.5 mA (VCC = 5.0 V, f(XIN) = 20 MHz) Typ. 3.5 mA (VCC = 3.0 V, f(XIN) = 10 MHz) Typ. 3.5 μA (VCC = 3.0 V, wait mode) Typ. 2.0 μA (VCC = 3.0 V, stop mode)
Operating Ambient Temperature		–20 to 85°C
Package		24-pin TSSOP Package code: PTSP0024KB-A (previous code: 024P2X-D)

1.2 Product List

Table 1.3 lists Product List for R5R0C0B Group. Figure 1.1 shows a Part Number, Memory Size, and Package of R5R0C0B Group.

Table 1.3 Product List for R5R0C0B Group **Current of May 2012**

Part No.	ROM Capacity	RAM Capacity	Package Type	Remarks
R5R0C0B4SP	16 Kbytes	1 Kbyte	PTSP0024KB-A	

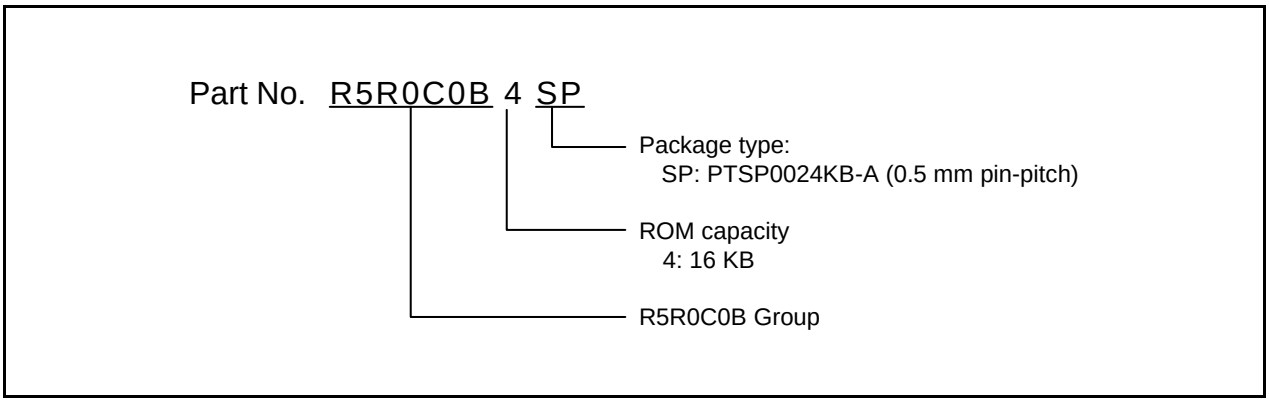


Figure 1.1 Part Number, Memory Size, and Package of R5R0C0B Group

1.3 Block Diagram

Figure 1.2 shows a Block Diagram.

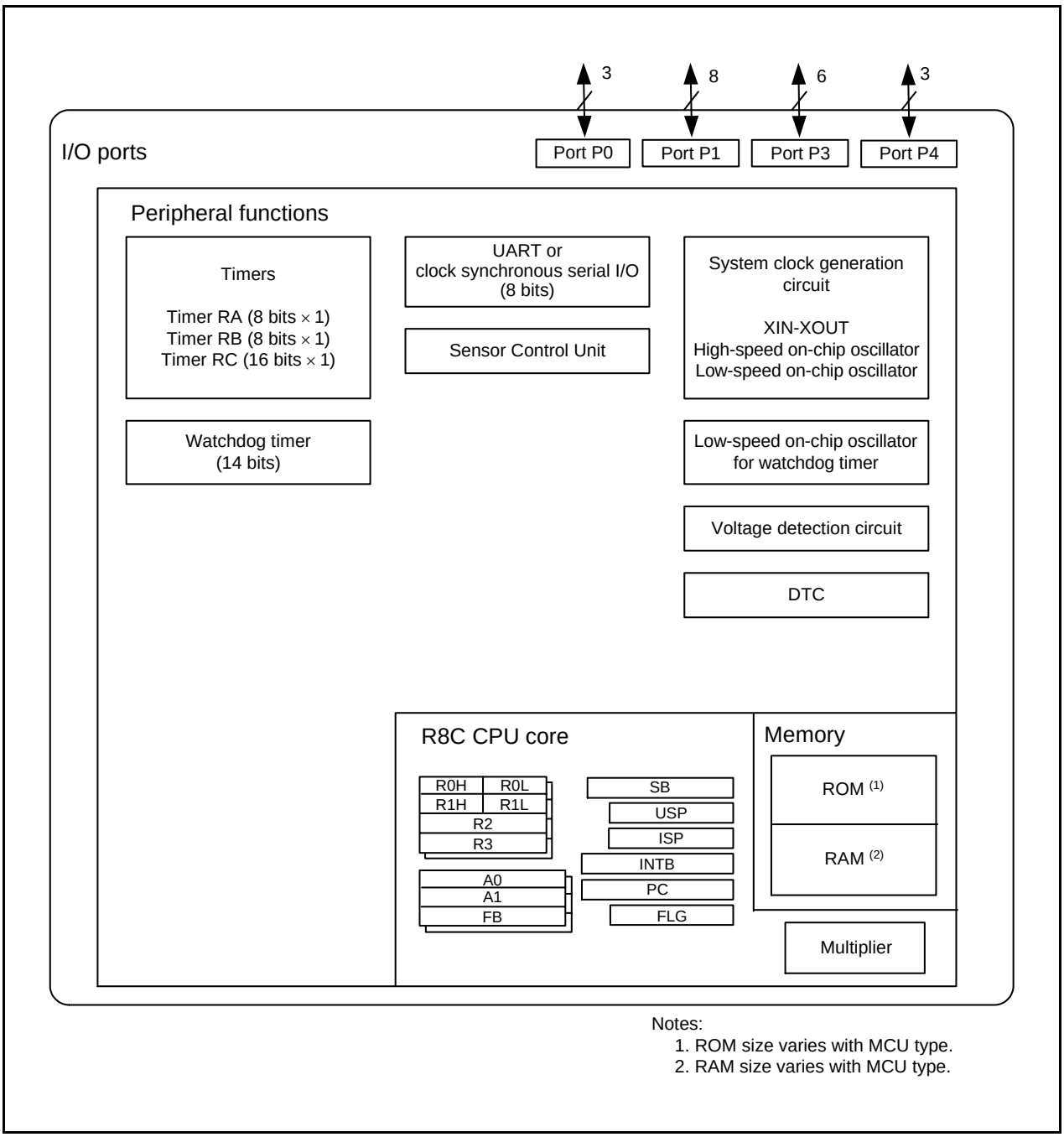


Figure 1.2 Block Diagram

1.4 Pin Assignment

Figure 1.3 shows Pin Assignment (Top View). Table 1.4 outlines the Pin Name Information by Pin Number.

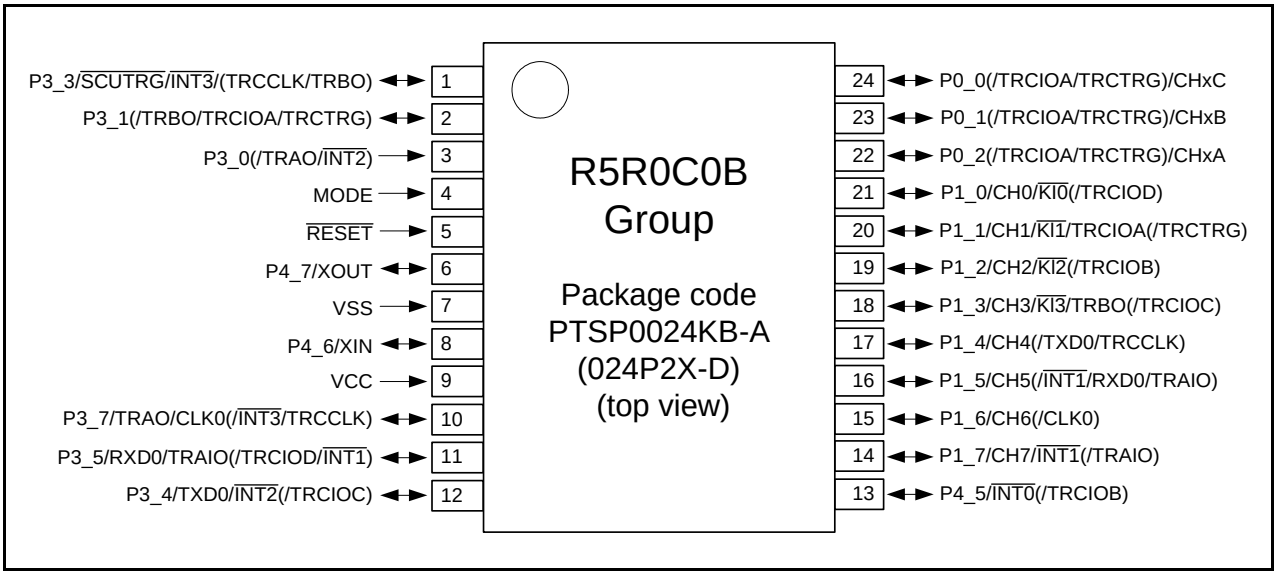


Figure 1.3 Pin Assignment (Top View)

Table 1.4 Pin Name Information by Pin Number

Pin Number	Control Pin	Port	I/O Pin Functions for Peripheral Modules			
			Interrupt	Timer	Serial Interface	Sensor Control Unit
1		P3_3	$\overline{\text{INT3}}$	TRBO/(TRCCLK)		$\overline{\text{SCUTRG}}$
2		P3_1		TRBO/(TRCTRG/ TRCIOA)		
3		P3_0	($\overline{\text{INT2}}$)	(TRAO)		
4	MODE					
5	$\overline{\text{RESET}}$					
6	XOUT	P4_7				
7	VSS					
8	XIN	P4_6				
9	VCC					
10		P3_7	($\overline{\text{INT3}}$)	TRAO/(TRCCLK)	CLK0	
11		P3_5	($\overline{\text{INT1}}$)	TRAIO/(TRCIOD)	RXD0	
12		P3_4	$\overline{\text{INT2}}$	(TRCIOC)	TXD0	
13		P4_5	$\overline{\text{INT0}}$	(TRCIOB)		
14		P1_7	$\overline{\text{INT1}}$	(TRAIO)		CH7
15		P1_6			(CLK0)	CH6
16		P1_5	($\overline{\text{INT1}}$)	(TRAIO)	(RXD0)	CH5
17		P1_4		(TRCCLK)	(TXD0)	CH4
18		P1_3	$\overline{\text{KI3}}$	TRBO/(TRCIOC)		CH3
19		P1_2	$\overline{\text{KI2}}$	(TRCIOB)		CH2
20		P1_1	$\overline{\text{KI1}}$	TRCIOA/ (TRCTRG)		CH1
21		P1_0	$\overline{\text{KI0}}$	(TRCIOD)		CH0
22		P0_2		(TRCIOA/ TRCTRG)		CHxA
23		P0_1		(TRCIOA/ TRCTRG)		CHxB
24		P0_0		(TRCIOA/ TRCTRG)		CHxC

Note:
1. Can be assigned to the pin in parentheses by a program.

1.5 Pin Functions

Table 1.5 lists Pin Functions.

Table 1.5 Pin Functions

Item	Pin Name	I/O Type	Description
Power supply input	VCC, VSS	—	Apply 1.8 V to 5.5 V to the VCC pin. Apply 0 V to the VSS pin.
Reset input	$\overline{\text{RESET}}$	I	Input “L” on this pin resets the MCU.
MODE	MODE	I	Connect this pin to VCC via a resistor.
XIN clock input	XIN	I	These pins are provided for XIN clock generation circuit I/O. Connect a ceramic resonator or a crystal oscillator between the XIN and XOUT pins. (1) To use an external clock, input it to the XOUT pin and leave the XIN pin open.
XIN clock output	XOUT	I/O	
$\overline{\text{INT}}$ interrupt input	$\overline{\text{INT0}}$ to $\overline{\text{INT3}}$	I	$\overline{\text{INT}}$ interrupt input pins. $\overline{\text{INT0}}$ is timer RB, and RC input pin.
Key input interrupt	$\overline{\text{KI0}}$ to $\overline{\text{KI3}}$	I	Key input interrupt input pins
Timer RA	TRAIO	I/O	Timer RA I/O pin
	TRAO	O	Timer RA output pin
Timer RB	TRBO	O	Timer RB output pin
Timer RC	TRCCLK	I	External clock input pin
	TRCTRG	I	External trigger input pin
	TRCIOA, TRCIOB, TRCIOC, TRCIOD	I/O	Timer RC I/O pins
Serial interface	CLK0	I/O	Transfer clock I/O pin
	RXD0	I	Serial data input pin
	TXD0	O	Serial data output pin
Sensor control unit	CHxA, CHxB, CHxC	I/O	Control pins for electrostatic capacitive touch detection
	CH0 to CH7	I	Electrostatic capacitive touch detection pins
	$\overline{\text{SCUTRG}}$	I	Sensor control unit external trigger input
I/O port	P0_0 to P0_2, P1_0 to P1_7, P3_0, P3_1, P3_3 to P3_5, P3_7, P4_5 to P4_7	I/O	CMOS I/O ports. Each port has an I/O select direction register, allowing each pin in the port to be directed for input or output individually. Any port set to input can be set to use a pull-up resistor or not by a program. All ports can be used as LED drive ports.

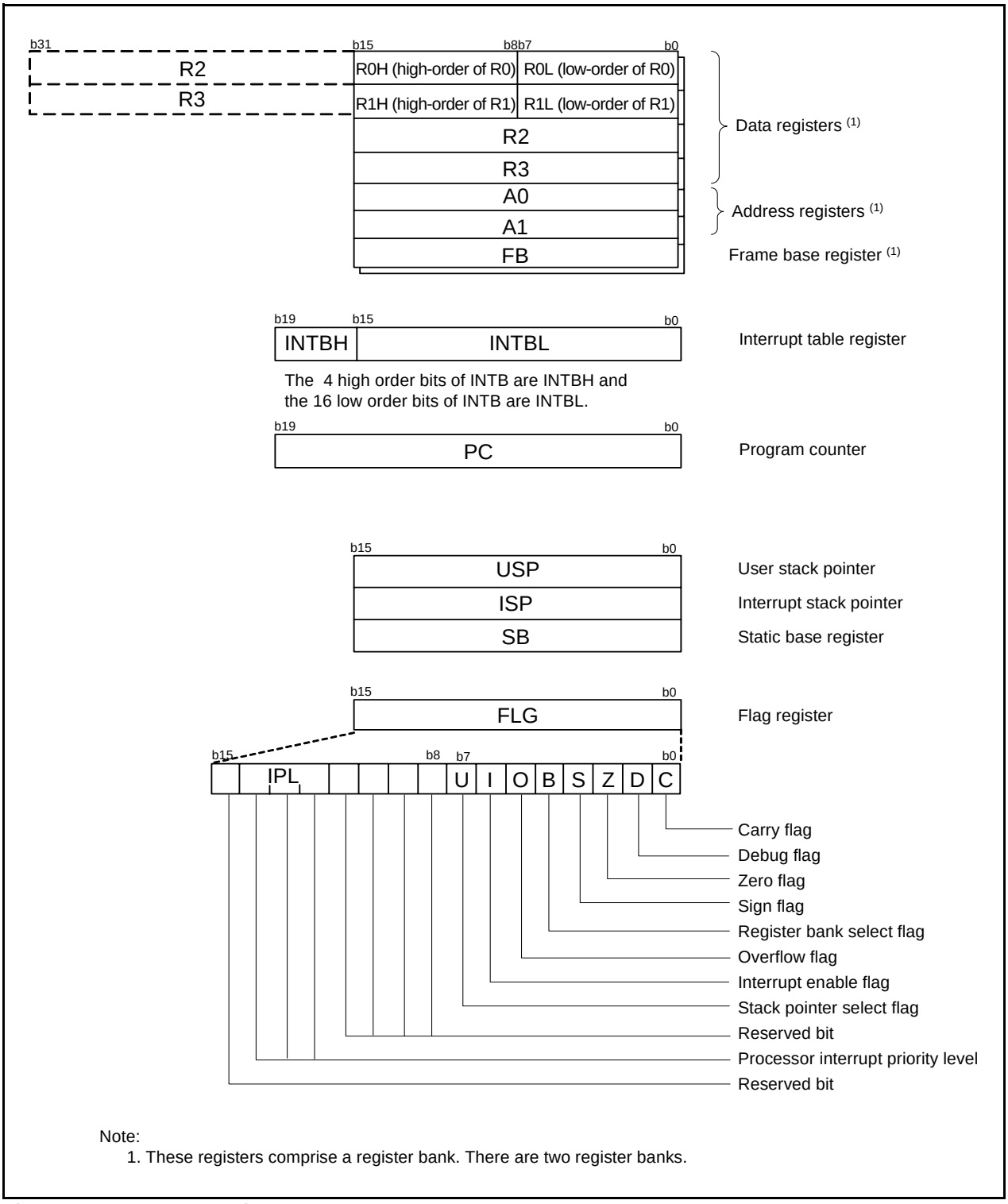
I: Input O: Output I/O: Input and output

Note:

1. Refer to the oscillator manufacturer for oscillation characteristics.

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU Registers. The CPU contains 13 registers. R0, R1, R2, R3, A0, A1, and FB configure a register bank. There are two sets of register bank.



Note:
1. These registers comprise a register bank. There are two register banks.

Figure 2.1 CPU Registers

2.1 Data Registers (R0, R1, R2, and R3)

R0 is a 16-bit register for transfer, arithmetic, and logic operations. The same applies to R1 to R3. R0 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R1H and R1L are analogous to R0H and R0L. R2 can be combined with R0 and used as a 32-bit data register (R2R0). R3R1 is analogous to R2R0.

2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. It is also used for transfer, arithmetic, and logic operations. A1 is analogous to A0. A1 can be combined with A0 and as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the starting address of an interrupt vector table.

2.5 Program Counter (PC)

PC is 20 bits wide and indicates the address of the next instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP and ISP, are each 16 bits wide. The U flag of FLG is used to switch between USP and ISP.

2.7 Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

2.8 Flag Register (FLG)

FLG is an 11-bit register indicating the CPU state.

2.8.1 Carry Flag (C)

The C flag retains carry, borrow, or shift-out bits that have been generated by the arithmetic and logic unit.

2.8.2 Debug Flag (D)

The D flag is for debugging only. Set it to 0.

2.8.3 Zero Flag (Z)

The Z flag is set to 1 when an arithmetic operation results in 0; otherwise to 0.

2.8.4 Sign Flag (S)

The S flag is set to 1 when an arithmetic operation results in a negative value; otherwise to 0.

2.8.5 Register Bank Select Flag (B)

Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is set to 1.

2.8.6 Overflow Flag (O)

The O flag is set to 1 when an operation results in an overflow; otherwise to 0.

2.8.7 Interrupt Enable Flag (I)

The I flag enables maskable interrupts.
Interrupts are disabled when the I flag is set to 0, and are enabled when the I flag is set to 1. The I flag is set to 0 when an interrupt request is acknowledged.

2.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to 0; USP is selected when the U flag is set to 1.
The U flag is set to 0 when a hardware interrupt request is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is 3 bits wide and assigns processor interrupt priority levels from level 0 to level 7.
If a requested interrupt has higher priority than IPL, the interrupt is enabled.

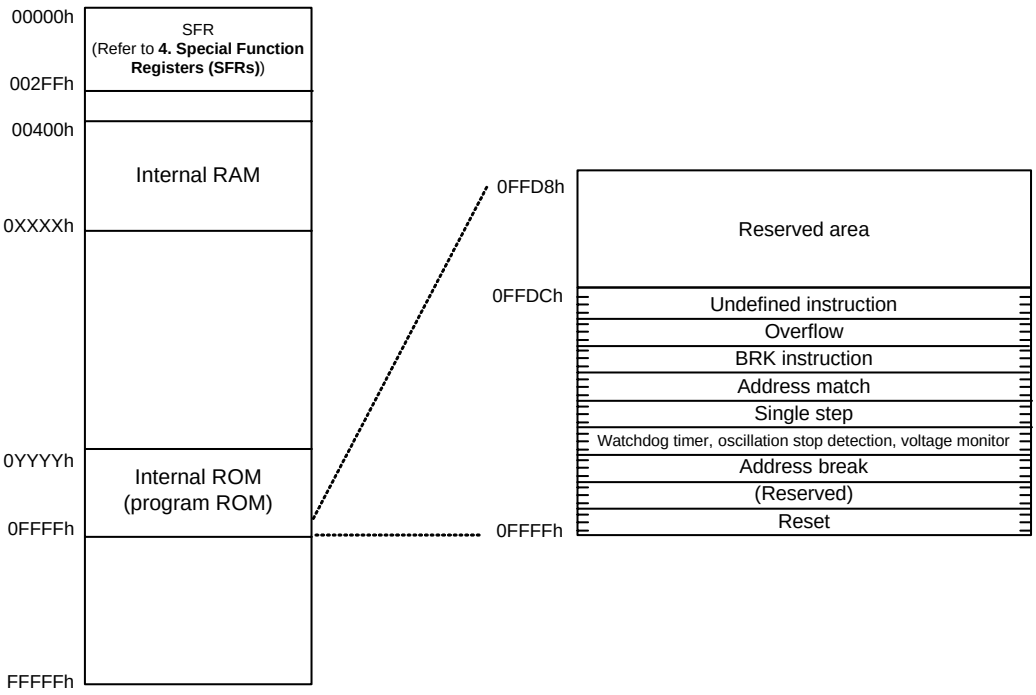
2.8.10 Reserved Bit

If necessary, set to 0. When read, the content is undefined.

3. Memory

3.1 R5R0C0B Group

Figure 3.1 is a Memory Map of R5R0C0B Group. The R5R0C0B Group has a 1-Mbyte address space from addresses 00000h to FFFFFh. A 16-Kbyte internal ROM area is allocated addresses 0C000h to 0FFFFh.
The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. The starting address of each interrupt routine is stored here.
The internal RAM is allocated higher addresses, beginning with address 00400h. A 1-Kbyte internal RAM area is allocated addresses 00400h to 007FFh. The internal RAM is used not only for data storage but also as a stack area when a subroutine is called or when an interrupt request is acknowledged.
Special function registers (SFRs) are allocated addresses 00000h to 002FFh and 02C00h to 02FFFh. Peripheral function control registers are allocated here. All unallocated spaces within the SFRs are reserved and cannot be accessed by users.



Note:
1. The blank areas are reserved and cannot be accessed by users.

Part Number	Internal ROM		Internal RAM	
	Size	Address 0YYYYh	Size	Address 0XXXXh
R5R0C0B4SP	16 Kbytes	0C000h	1 Kbyte	007FFh

Figure 3.1 Memory Map of R5R0C0B Group

4. Special Function Registers (SFRs)

An SFR (special function register) is a control register for a peripheral function. Tables 4.1 to 4.12 list the special function registers. Table 4.13 lists the ID Code Areas and Option Function Select Area.

Table 4.1 SFR Information (1) [1]

Address	Register	Symbol	After Reset
0000h			
0001h			
0002h			
0003h			
0004h	Processor Mode Register 0	PM0	00h
0005h	Processor Mode Register 1	PM1	00h
0006h	System Clock Control Register 0	CM0	00101000b
0007h	System Clock Control Register 1	CM1	00100000b
0008h	Module Standby Control Register	MSTCR	00h
0009h	System Clock Control Register 3	CM3	00h
000Ah	Protect Register	PRCR	00h
000Bh	Reset Source Determination Register	RSTFR	0XXXXXXXb [2]
000Ch	Oscillation Stop Detection Register	OCD	00000100b
000Dh	Watchdog Timer Reset Register	WDTR	XXh
000Eh	Watchdog Timer Start Register	WDTS	XXh
000Fh	Watchdog Timer Control Register	WDTC	00111111b
0010h			
0011h			
0012h			
0013h			
0014h			
0015h	High-Speed On-Chip Oscillator Control Register 7	FRA7	When shipping
0016h			
0017h			
0018h			
0019h			
001Ah			
001Bh			
001Ch	Count Source Protection Mode Register	CSPR	00h 10000000b [3]
001Dh			
001Eh			
001Fh			
0020h			
0021h			
0022h			
0023h	High-Speed On-Chip Oscillator Control Register 0	FRA0	00h
0024h	High-Speed On-Chip Oscillator Control Register 1	FRA1	When shipping
0025h	High-Speed On-Chip Oscillator Control Register 2	FRA2	00h
0026h			
0027h			
0028h	Clock Prescaler Reset Flag	CPSRF	00h
0029h	High-Speed On-Chip Oscillator Control Register 4	FRA4	When shipping
002Ah	High-Speed On-Chip Oscillator Control Register 5	FRA5	When shipping
002Bh	High-Speed On-Chip Oscillator Control Register 6	FRA6	When shipping
002Ch			
002Dh			
002Eh			
002Fh	High-Speed On-Chip Oscillator Control Register 3	FRA3	When shipping
0030h	Voltage Monitor Circuit Control Register	CMPA	00h
0031h	Voltage Monitor Circuit Edge Select Register	VCAC	00h
0032h			
0033h	Voltage Detect Register 1	VCA1	00001000b
0034h	Voltage Detect Register 2	VCA2	00h [4] 00100000b [5]
0035h			
0036h	Voltage Detection 1 Level Select Register	VD1LS	00000111b
0037h			
0038h	Voltage Monitor 0 Circuit Control Register	VW0C	1100X010b [4] 1100X011b [5]
0039h	Voltage Monitor 1 Circuit Control Register	VW1C	10001010b

X: Undefined

Notes:

1. The blank areas are reserved and cannot be accessed by users.
2. The CWR bit in the RSTFR register is set to 0 after power-on and voltage monitor 0 reset. Hardware reset, Software reset, or watchdog timer reset does not affect this bit.
3. The CSPROINI bit in the OFS register is set to 0.
4. The LVDAS bit in the OFS register is set to 1.
5. The LVDAS bit in the OFS register is set to 0.

Table 4.2 SFR Information (2) (1)

Address	Register	Symbol	After Reset
003Ah	Voltage Monitor 2 Circuit Control Register	VW2C	10000010b
003Bh			
003Ch			
003Dh			
003Eh			
003Fh			
0040h			
0041h	Flash Memory Ready Interrupt Control Register	FMRDYIC	XXXXX000b
0042h			
0043h			
0044h			
0045h			
0046h			
0047h	Timer RC Interrupt Control Register	TRCIC	XXXXX000b
0048h			
0049h			
004Ah			
004Bh			
004Ch			
004Dh	Key Input Interrupt Control Register	KUPIC	XXXXX000b
004Eh			
004Fh			
0050h			
0051h	UART0 Transmit Interrupt Control Register	S0TIC	XXXXX000b
0052h	UART0 Receive Interrupt Control Register	S0RIC	XXXXX000b
0053h			
0054h			
0055h	INT2 Interrupt Control Register	INT2IC	XX00X000b
0056h	Timer RA Interrupt Control Register	TRAIC	XXXXX000b
0057h			
0058h	Timer RB Interrupt Control Register	TRBIC	XXXXX000b
0059h	INT1 Interrupt Control Register	INT1IC	XX00X000b
005Ah	INT3 Interrupt Control Register	INT3IC	XX00X000b
005Bh			
005Ch			
005Dh	INT0 Interrupt Control Register	INT0IC	XX00X000b
005Eh			
005Fh			
0060h			
0061h			
0062h			
0063h			
0064h			
0065h			
0066h			
0067h			
0068h			
0069h			
006Ah	Sensor Control Unit Interrupt Control Register	SCUIC	XXXXX000b
006Bh			
006Ch			
006Dh			
006Eh			
006Fh			
0070h			
0071h			
0072h	Voltage Monitor 1 Interrupt Control Register	VCMP1IC	XXXXX000b
0073h	Voltage Monitor 2 Interrupt Control Register	VCMP2IC	XXXXX000b
0074h			
0075h			
0076h			
0077h			
0078h			
0079h			
007Ah			
007Bh			
007Ch			
007Dh			
007Eh			
007Fh			

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.3 SFR Information (3) (1)

Address	Register	Symbol	After Reset
0080h	DTC Activation Control Register	DTCTL	00h
0081h			
0082h			
0083h			
0084h			
0085h			
0086h			
0087h			
0088h	DTC Activation Enable Register 0	DTCEN0	00h
0089h	DTC Activation Enable Register 1	DTCEN1	00h
008Ah	DTC Activation Enable Register 2	DTCEN2	00h
008Bh	DTC Activation Enable Register 3	DTCEN3	00h
008Ch			
008Dh	DTC Activation Enable Register 5	DTCEN5	00h
008Eh	DTC Activation Enable Register 6	DTCEN6	00h
008Fh			
0090h			
0091h			
0092h			
0093h			
0094h			
0095h			
0096h			
0097h			
0098h			
0099h			
009Ah			
009Bh			
009Ch			
009Dh			
009Eh			
009Fh			
00A0h	UART0 Transmit/Receive Mode Register	U0MR	00h
00A1h	UART0 Bit Rate Register	U0BRG	XXh
00A2h	UART0 Transmit Buffer Register	U0TB	XXh
00A3h			XXh
00A4h	UART0 Transmit/Receive Control Register 0	U0C0	00001000b
00A5h	UART0 Transmit/Receive Control Register 1	U0C1	00000010b
00A6h	UART0 Receive Buffer Register	U0RB	XXh
00A7h			XXh
00A8h			
00A9h			
00AAh			
00ABh			
00ACh			
00ADh			
00AEh			
00AFh			
00B0h			
00B1h			
00B2h			
00B3h			
00B4h			
00B5h			
00B6h			
00B7h			
00B8h			
00B9h			
00BAh			
00BBh			
00BCh			
00BDh			
00BEh			
00BFh			

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.4 SFR Information (4) (1)

Address	Register	Symbol	After Reset
00C0h			
00C1h			
00C2h			
00C3h			
00C4h			
00C5h			
00C6h			
00C7h			
00C8h			
00C9h			
00CAh			
00CBh			
00CCh			
00CDh			
00CEh			
00CFh			
00D0h			
00D1h			
00D2h			
00D3h			
00D4h			
00D5h			
00D6h			
00D7h			
00D8h			
00D9h			
00DAh			
00DBh			
00DCh			
00DDh			
00DEh			
00DFh			
00E0h	Port P0 Register	P0	XXh
00E1h	Port P1 Register	P1	XXh
00E2h	Port P0 Direction Register	PD0	00h
00E3h	Port P1 Direction Register	PD1	00h
00E4h			
00E5h	Port P3 Register	P3	XXh
00E6h			
00E7h	Port P3 Direction Register	PD3	00h
00E8h	Port P4 Register	P4	XXh
00E9h			
00EAh	Port P4 Direction Register	PD4	00h
00EBh			
00ECh			
00EDh			
00EEh			
00EFh			
00F0h			
00F1h			
00F2h			
00F3h			
00F4h			
00F5h			
00F6h			
00F7h			
00F8h			
00F9h			
00FAh			
00FBh			
00FCh			
00FDh			
00FEh			
00FFh			

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.5 SFR Information (5) (1)

Address	Register	Symbol	After Reset
0100h	Timer RA Control Register	TRACR	00h
0101h	Timer RA I/O Control Register	TRAIOC	00h
0102h	Timer RA Mode Register	TRAMR	00h
0103h	Timer RA Prescaler Register	TRAPRE	FFh
0104h	Timer RA Register	TRA	FFh
0105h			
0106h			
0107h			
0108h	Timer RB Control Register	TRBCR	00h
0109h	Timer RB One-Shot Control Register	TRBOCR	00h
010Ah	Timer RB I/O Control Register	TRBIOC	00h
010Bh	Timer RB Mode Register	TRBMR	00h
010Ch	Timer RB Prescaler Register	TRBPRE	FFh
010Dh	Timer RB Secondary Register	TRBSC	FFh
010Eh	Timer RB Primary Register	TRBPR	FFh
010Fh			
0110h			
0111h			
0112h			
0113h			
0114h			
0115h			
0116h			
0117h			
0118h			
0119h			
011Ah			
011Bh			
011Ch			
011Dh			
011Eh			
011Fh			
0120h	Timer RC Mode Register	TRCMR	01001000b
0121h	Timer RC Control Register 1	TRCCR1	00h
0122h	Timer RC Interrupt Enable Register	TRCIER	01110000b
0123h	Timer RC Status Register	TRCSR	01110000b
0124h	Timer RC I/O Control Register 0	TRCIOR0	10001000b
0125h	Timer RC I/O Control Register 1	TRCIOR1	10001000b
0126h	Timer RC Counter	TRC	00h
0127h			00h
0128h	Timer RC General Register A	TRCGRA	FFh
0129h			FFh
012Ah	Timer RC General Register B	TRCGRB	FFh
012Bh			FFh
012Ch	Timer RC General Register C	TRCGRC	FFh
012Dh			FFh
012Eh	Timer RC General Register D	TRCGRD	FFh
012Fh			FFh
0130h	Timer RC Control Register 2	TRCCR2	00011000b
0131h	Timer RC Digital Filter Function Select Register	TRCDF	00h
0132h	Timer RC Output Master Enable Register	TRCOER	01111111b
0133h	Timer RC Trigger Control Register	TRCSCUCR	00h
0134h			
0135h			
0136h			
0137h			
0138h			
0139h			
013Ah			
013Bh			
013Ch			
013Dh			
013Eh			
013Fh			

Note:
1. The blank areas are reserved and cannot be accessed by users.

Table 4.6 SFR Information (6) (1)

Address	Register	Symbol	After Reset
0140h			
0141h			
0142h			
0143h			
0144h			
0145h			
0146h			
0147h			
0148h			
0149h			
014Ah			
014Bh			
014Ch			
014Dh			
014Eh			
014Fh			
0150h			
0151h			
0152h			
0153h			
0154h			
0155h			
0156h			
0157h			
0158h			
0159h			
015Ah			
015Bh			
015Ch			
015Dh			
015Eh			
015Fh			
0160h			
0161h			
0162h			
0163h			
0164h			
0165h			
0166h			
0167h			
0168h			
0169h			
016Ah			
016Bh			
016Ch			
016Dh			
016Eh			
016Fh			
0170h			
0171h			
0172h			
0173h			
0174h			
0175h			
0176h			
0177h			
0178h			
0179h			
017Ah			
017Bh			
017Ch			
017Dh			
017Eh			
017Fh			

Note:
1. The blank areas are reserved and cannot be accessed by users.

Table 4.7 SFR Information (7) (1)

Address	Register	Symbol	After Reset
0180h	Timer RA Pin Select Register	TRASR	00h
0181h	Timer RB/RC Pin Select Register	TRBRCSR	00h
0182h	Timer RC Pin Select Register 0	TRCPSR0	00h
0183h	Timer RC Pin Select Register 1	TRCPSR1	00h
0184h			
0185h			
0186h			
0187h			
0188h	UART0 Pin Select Register	U0SR	00h
0189h			
018Ah			
018Bh			
018Ch			
018Dh			
018Eh	INT Interrupt Input Pin Select Register	INTSR	00h
018Fh	I/O Function Pin Select Register	PINSR	00h
0190h	Low-Voltage Signal Mode Control Register	TSMR	00h
0191h			
0192h			
0193h			
0194h			
0195h			
0196h			
0197h			
0198h			
0199h			
019Ah			
019Bh			
019Ch			
019Dh			
019Eh			
019Fh			
01A0h			
01A1h			
01A2h			
01A3h			
01A4h			
01A5h			
01A6h			
01A7h			
01A8h			
01A9h			
01AAh			
01ABh			
01ACh			
01ADh			
01AEh			
01AFh			
01B0h			
01B1h			
01B2h	Flash Memory Status Register	FST	10000X00b
01B3h			
01B4h	Flash Memory Control Register 0	FMR0	00h
01B5h	Flash Memory Control Register 1	FMR1	00h
01B6h	Flash Memory Control Register 2	FMR2	00h
01B7h			
01B8h			
01B9h			
01BAh			
01BBh			
01BCh			
01BDh			
01BEh			
01BFh			

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.8 SFR Information (8) (1)

Address	Register	Symbol	After Reset
01C0h	Address Match Interrupt Register 0	RMAD0	XXh
01C1h			XXh
01C2h			0000XXXXb
01C3h	Address Match Interrupt Enable Register 0	AIER0	00h
01C4h	Address Match Interrupt Register 1	RMAD1	XXh
01C5h			XXh
01C6h			0000XXXXb
01C7h	Address Match Interrupt Enable Register 1	AIER1	00h
01C8h			
01C9h			
01CAh			
01CBh			
01CCh			
01CDh			
01CEh			
01CFh			
01D0h			
01D1h			
01D2h			
01D3h			
01D4h			
01D5h			
01D6h			
01D7h			
01D8h			
01D9h			
01DAh			
01DBh			
01DCh			
01DDh			
01DEh			
01DFh			
01E0h	Pull-Up Control Register 0	PUR0	00h
01E1h	Pull-Up Control Register 1	PUR1	00h
01E2h			
01E3h			
01E4h			
01E5h			
01E6h			
01E7h			
01E8h			
01E9h			
01EAh			
01EBh			
01ECh			
01EDh			
01EEh			
01EFh			
01F0h	Port P1 Drive Capacity Control Register	P1DRR	00h
01F1h			
01F2h	Drive Capacity Control Register 0	DRR0	00h
01F3h	Drive Capacity Control Register 1	DRR1	00h
01F4h			
01F5h	Input Threshold Control Register 0	VLT0	00h
01F6h	Input Threshold Control Register 1	VLT1	00h
01F7h			
01F8h			
01F9h			
01FAh	External Input Enable Register 0	INTEN	00h
01FBh			
01FCh	INT Input Filter Select Register 0	INTF	00h
01FDh			
01FEh	Key Input Enable Register 0	KIEN	00h
01FFh			

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.9 SFR Information (9) (1)

Address	Register	Symbol	After Reset
02C0h	SCU Control Register 0	SCUCR0	00h
02C1h	SCU Mode Register	SCUMR	00h
02C2h	SCU Timing Control Register 0	SCTCR0	00000011b
02C3h	SCU Timing Control Register 1	SCTCR1	00000001b
02C4h	SCU Timing Control Register 2	SCTCR2	00010000b
02C5h	SCU Timing Control Register 3	SCTCR3	00h
02C6h	SCU Channel Control Register	SCHCR	00h
02C7h	SCU Channel Control Counter	SCUCHC	00h
02C8h	SCU Flag Register	SCUFR	00h
02C9h	SCU Status Counter Register	SCUSTC	00h
02CAh	SCU Secondary Counter Set Register	SCSCSR	00000111b
02CBh	SCU Secondary Counter Register	SCUSCC	00000111b
02CCh			
02CDh			
02CEh	SCU Destination Address Register	SCUDAR	00h
02CFh			00001100b
02D0h	SCU Data Buffer Register	SCUDBR	00h
02D1h			00h
02D2h	SCU Primary Counter Register	SCUPRC	00h
02D3h			00h
02D4h	SCU Random Value Store Register 0	SCRVR0	00h
02D5h	SCU Random Value Store Register 1	SCRVR1	00h
02D6h	SCU Random Value Store Register 2	SCRVR2	00h
02D7h	SCU Random Value Store Register 3	SCRVR3	00h
02D8h	SCU Random Value Store Register 4	SCRVR4	00h
02D9h	SCU Random Value Store Register 5	SCRVR5	00h
02DAh	SCU Random Value Store Register 6	SCRVR6	00h
02DBh	SCU Random Value Store Register 7	SCRVR7	00h
02DCh	SCU Input Enable Register 0	TSIER0	00h
02DDh			
02DEh			
02DFh			
:			
2C00h	DTC Transfer Vector Area		XXh
2C01h	DTC Transfer Vector Area		XXh
2C02h	DTC Transfer Vector Area		XXh
2C03h	DTC Transfer Vector Area		XXh
2C04h	DTC Transfer Vector Area		XXh
2C05h	DTC Transfer Vector Area		XXh
2C06h	DTC Transfer Vector Area		XXh
2C07h	DTC Transfer Vector Area		XXh
2C08h	DTC Transfer Vector Area		XXh
2C09h	DTC Transfer Vector Area		XXh
2C0Ah	DTC Transfer Vector Area		XXh
:	DTC Transfer Vector Area		XXh
:	DTC Transfer Vector Area		XXh
2C3Ah	DTC Transfer Vector Area		XXh
2C3Bh	DTC Transfer Vector Area		XXh
2C3Ch	DTC Transfer Vector Area		XXh
2C3Dh	DTC Transfer Vector Area		XXh
2C3Eh	DTC Transfer Vector Area		XXh
2C3Fh	DTC Transfer Vector Area		XXh
2C40h	DTC Control Data 0	DTCD0	XXh
2C41h			XXh
2C42h			XXh
2C43h			XXh
2C44h			XXh
2C45h			XXh
2C46h			XXh
2C47h			XXh
2C48h	DTC Control Data 1	DTCD1	XXh
2C49h			XXh
2C4Ah			XXh
2C4Bh			XXh
2C4Ch			XXh
2C4Dh			XXh
2C4Eh			XXh
2C4Fh			XXh

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.10 SFR Information (10) (1)

Address	Register	Symbol	After Reset
2C50h	DTC Control Data 2	DTCD2	XXh
2C51h			XXh
2C52h			XXh
2C53h			XXh
2C54h			XXh
2C55h			XXh
2C56h			XXh
2C57h			XXh
2C58h	DTC Control Data 3	DTCD3	XXh
2C59h			XXh
2C5Ah			XXh
2C5Bh			XXh
2C5Ch			XXh
2C5Dh			XXh
2C5Eh			XXh
2C5Fh			XXh
2C60h	DTC Control Data 4	DTCD4	XXh
2C61h			XXh
2C62h			XXh
2C63h			XXh
2C64h			XXh
2C65h			XXh
2C66h			XXh
2C67h			XXh
2C68h	DTC Control Data 5	DTCD5	XXh
2C69h			XXh
2C6Ah			XXh
2C6Bh			XXh
2C6Ch			XXh
2C6Dh			XXh
2C6Eh			XXh
2C6Fh			XXh
2C70h	DTC Control Data 6	DTCD6	XXh
2C71h			XXh
2C72h			XXh
2C73h			XXh
2C74h			XXh
2C75h			XXh
2C76h			XXh
2C77h			XXh
2C78h	DTC Control Data 7	DTCD7	XXh
2C79h			XXh
2C7Ah			XXh
2C7Bh			XXh
2C7Ch			XXh
2C7Dh			XXh
2C7Eh			XXh
2C7Fh			XXh
2C80h	DTC Control Data 8	DTCD8	XXh
2C81h			XXh
2C82h			XXh
2C83h			XXh
2C84h			XXh
2C85h			XXh
2C86h			XXh
2C87h			XXh
2C88h	DTC Control Data 9	DTCD9	XXh
2C89h			XXh
2C8Ah			XXh
2C8Bh			XXh
2C8Ch			XXh
2C8Dh			XXh
2C8Eh			XXh
2C8Fh			XXh

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.11 SFR Information (11) (1)

Address	Register	Symbol	After Reset
2C90h	DTC Control Data 10	DTCD10	XXh
2C91h			XXh
2C92h			XXh
2C93h			XXh
2C94h			XXh
2C95h			XXh
2C96h			XXh
2C97h			XXh
2C98h	DTC Control Data 11	DTCD11	XXh
2C99h			XXh
2C9Ah			XXh
2C9Bh			XXh
2C9Ch			XXh
2C9Dh			XXh
2C9Eh			XXh
2C9Fh			XXh
2CA0h	DTC Control Data 12	DTCD12	XXh
2CA1h			XXh
2CA2h			XXh
2CA3h			XXh
2CA4h			XXh
2CA5h			XXh
2CA6h			XXh
2CA7h			XXh
2CA8h	DTC Control Data 13	DTCD13	XXh
2CA9h			XXh
2CAAh			XXh
2CABh			XXh
2CACh			XXh
2CADh			XXh
2CAEh			XXh
2CAFh			XXh
2CB0h	DTC Control Data 14	DTCD14	XXh
2CB1h			XXh
2CB2h			XXh
2CB3h			XXh
2CB4h			XXh
2CB5h			XXh
2CB6h			XXh
2CB7h			XXh
2CB8h	DTC Control Data 15	DTCD15	XXh
2CB9h			XXh
2CBAh			XXh
2CBBh			XXh
2CBCh			XXh
2CBDh			XXh
2CBEh			XXh
2CBFh			XXh
2CC0h	DTC Control Data 16	DTCD16	XXh
2CC1h			XXh
2CC2h			XXh
2CC3h			XXh
2CC4h			XXh
2CC5h			XXh
2CC6h			XXh
2CC7h			XXh
2CC8h	DTC Control Data 17	DTCD17	XXh
2CC9h			XXh
2CCAh			XXh
2CCBh			XXh
2CCCh			XXh
2CCDh			XXh
2CCEh			XXh
2CCFh			XXh

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.12 SFR Information (12) (1)

Address	Register	Symbol	After Reset
2CD0h	DTC Control Data 18	DTCD18	XXh
2CD1h			XXh
2CD2h			XXh
2CD3h			XXh
2CD4h			XXh
2CD5h			XXh
2CD6h			XXh
2CD7h			XXh
2CD8h	DTC Control Data 19	DTCD19	XXh
2CD9h			XXh
2CDAh			XXh
2CDBh			XXh
2CDCh			XXh
2CDDh			XXh
2CDEh			XXh
2CDFh			XXh
2CE0h	DTC Control Data 20	DTCD20	XXh
2CE1h			XXh
2CE2h			XXh
2CE3h			XXh
2CE4h			XXh
2CE5h			XXh
2CE6h			XXh
2CE7h			XXh
2CE8h	DTC Control Data 21	DTCD21	XXh
2CE9h			XXh
2CEAh			XXh
2CEBh			XXh
2CECh			XXh
2CEDh			XXh
2CEEh			XXh
2CEFh			XXh
2CF0h	DTC Control Data 22	DTCD22	XXh
2CF1h			XXh
2CF2h			XXh
2CF3h			XXh
2CF4h			XXh
2CF5h			XXh
2CF6h			XXh
2CF7h			XXh
2CF8h	DTC Control Data 23	DTCD23	XXh
2CF9h			XXh
2CFAh			XXh
2CFBh			XXh
2CFCh			XXh
2CFDh			XXh
2CFEh			XXh
2CFFh			XXh
2D00h			
:			
2FFFh			

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.13 ID Code Areas and Option Function Select Area

Address	Area Name	Symbol	After Reset
:			
FFDBh	Option Function Select Register 2	OFS2	(Note 1)
:			
FFDFh	ID1		(Note 2)
:			
FFE3h	ID2		(Note 2)
:			
FFEBh	ID3		(Note 2)
:			
FFEFh	ID4		(Note 2)
:			
FFF3h	ID5		(Note 2)
:			
FFF7h	ID6		(Note 2)
:			
FFFBh	ID7		(Note 2)
:			
FFFFh	Option Function Select Register	OFS	(Note 1)

Notes:
1. The option function select area is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not write additions to the option function select area. If the block including the option function select area is erased, the option function select area is set to FFh.
   When blank products are shipped, the option function select area is set to FFh. It is set to the written value after written by the user.
   When factory-programming products are shipped, the value of the option function select area is the value programmed by the user.
2. The ID code areas are allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not write additions to the ID code areas. If the block including the ID code areas is erased, the ID code areas are set to FFh.
   When blank products are shipped, the ID code areas are set to FFh. They are set to the written value after written by the user.
   When factory-programming products are shipped, the value of the ID code areas is the value programmed by the user.

5. Resets

The following resets are implemented: hardware reset, power-on reset, voltage monitor 0 reset, watchdog timer reset, and software reset.
Table 5.1 lists the Reset Names and Sources and Figure 5.1 shows the Block Diagram of Reset Circuit.

Table 5.1 Reset Names and Sources

Reset Name	Source
Hardware reset	Input voltage of $\overline{\text{RESET}}$ pin is held “L”
Power-on reset	VCC rises
Voltage monitor 0 reset	VCC falls (monitor voltage: Vdet0)
Watchdog timer reset	Underflow of watchdog timer
Software reset	Write 1 to PM03 bit in PM0 register

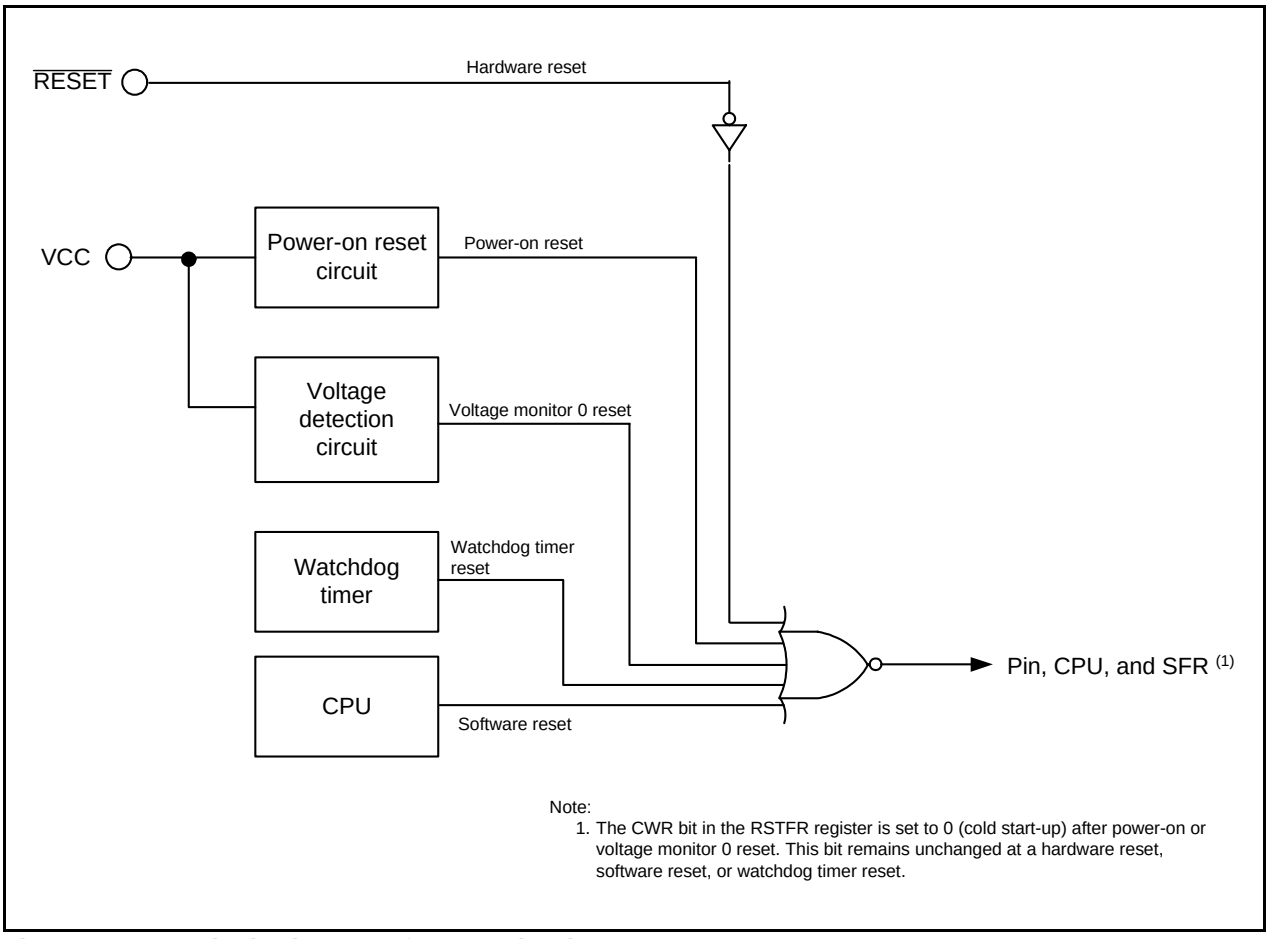


Figure 5.1 Block Diagram of Reset Circuit

Table 5.2 lists the Pin Functions while $\overline{\text{RESET}}$ Pin Level is “L”, Figure 5.2 shows the CPU Register Status after Reset, Figure 5.3 shows the Reset Sequence.

Table 5.2 Pin Functions while $\overline{\text{RESET}}$ Pin Level is “L”

Pin Name	Pin Function
P0_0 to P0_2, P1, P3_0, P3_1, P3_3 to P3_5, P3_7	Input port
P4_5 to P4_7	Input port

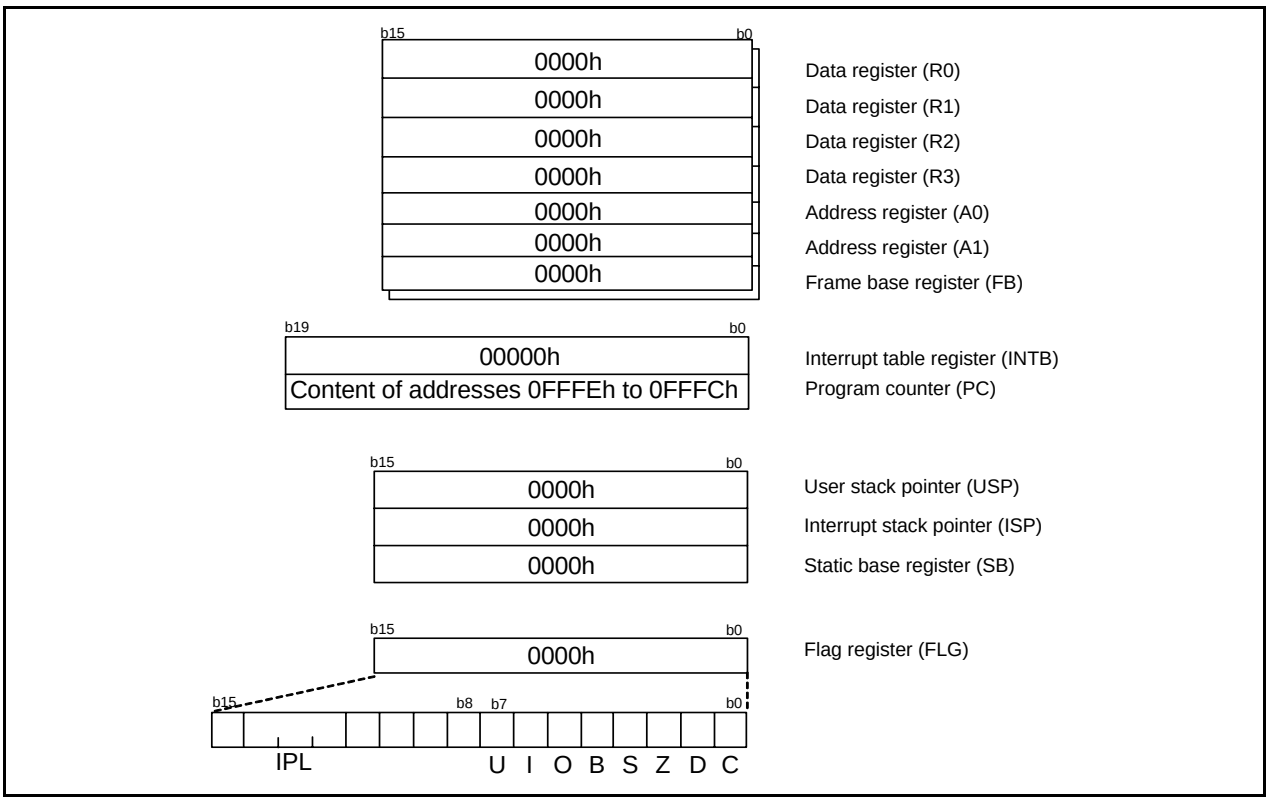
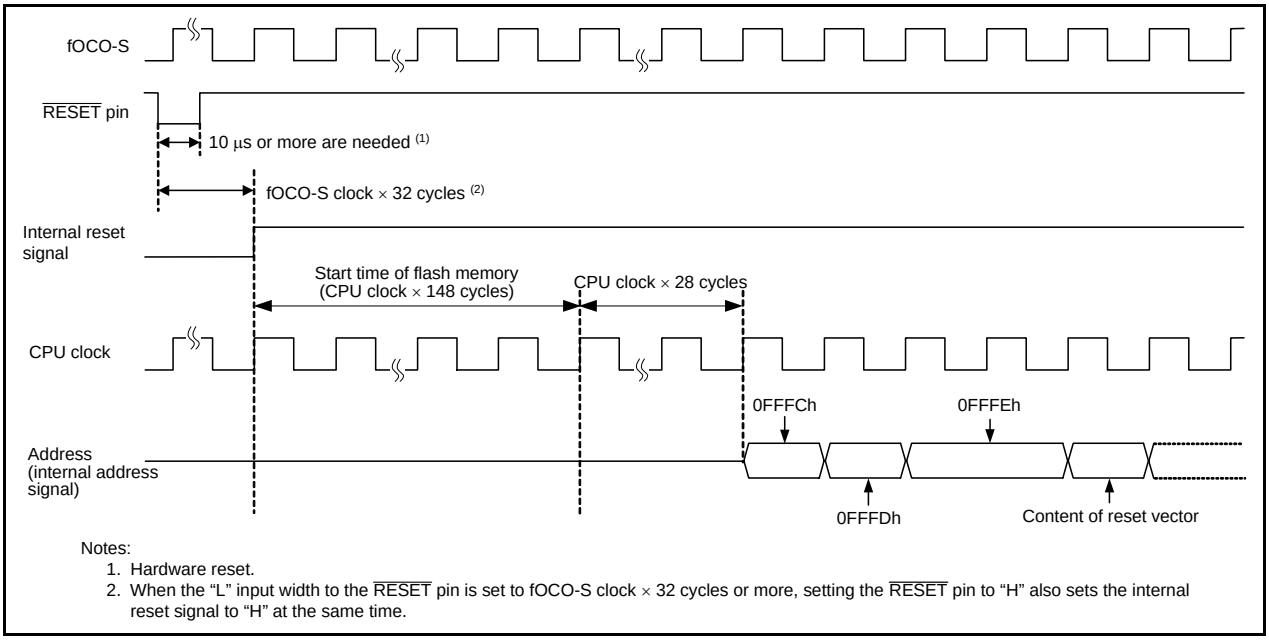


Figure 5.2 CPU Register Status after Reset



Notes:
1. Hardware reset.
2. When the “L” input width to the $\overline{\text{RESET}}$ pin is set to fOCO-S clock × 32 cycles or more, setting the $\overline{\text{RESET}}$ pin to “H” also sets the internal reset signal to “H” at the same time.

Figure 5.3 Reset Sequence

5.1 Registers

5.1.1 Processor Mode Register 0 (PM0)

Address 0004h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	PM03	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved bits	Set to 0.	R/W
b1	—			
b2	—			
b3	PM03	Software reset bit	The MCU is reset when this bit is set to 1. When read, the content is 0.	R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b5	—			
b6	—			
b7	—			

Set the PRC1 bit in the PRCR register to 1 (write enabled) before rewriting the PM0 register.

5.1.2 Reset Source Determination Register (RSTFR)

Address 000Bh

Bit	b7	b6	b5	b4	b3	b2	b1	b0	
Symbol	—	—	—	—	WDR	SWR	HWR	CWR	
After Reset	0	X	X	X	X	X	X	X	(Note 1)

Bit	Symbol	Bit Name	Function	R/W
b0	CWR	Cold start-up/warm start-up determine flag (2, 3)	0: Cold start-up 1: Warm start-up	R/W
b1	HWR	Hardware reset detect flag	0: Not detected 1: Detected	R
b2	SWR	Software reset detect flag	0: Not detected 1: Detected	R
b3	WDR	Watchdog timer reset detect flag	0: Not detected 1: Detected	R
b4	—	Reserved bits	When read, the content is undefined.	R
b5	—			
b6	—			
b7	—	Reserved bit	Set to 0.	R/W

Notes:
1. The CWR bit is set to 0 (cold start-up) after power-on or voltage monitor 0 reset. This bit remains unchanged at a hardware reset, software reset, or watchdog timer reset.
2. If 1 is written to the CWR bit by a program, it is set to 1. (Writing 0 does not affect this bit.)
3. When the VW0C0 bit in the VW0C register is set to 0 (voltage monitor 0 reset disabled), the CWR bit value is undefined.

5.1.3 Option Function Select Register (OFS)

Address 0FFFFh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CSPROINI	LVDAS	VDSEL1	VDSEL0	ROMCP1	ROMCR	—	WDTON
After Reset	User Setting Value (1)							

Bit	Symbol	Bit Name	Function	R/W
b0	WDTON	Watchdog timer start select bit	0: Watchdog timer automatically starts after reset. 1: Watchdog timer is stopped after reset.	R/W
b1	—	Reserved bit	Set to 1.	R/W
b2	ROMCR	ROM code protect disable bit	0: ROM code protect disabled 1: ROMCP1 bit enabled	R/W
b3	ROMCP1	ROM code protect bit	0: ROM code protect enabled 1: ROM code protect disabled	R/W
b4	VDSEL0	Voltage detection 0 level select bit (2)	b5 b4 0 0: 3.80 V selected (Vdet0_3) 0 1: 2.85 V selected (Vdet0_2) 1 0: 2.35 V selected (Vdet0_1) 1 1: 1.90 V selected (Vdet0_0)	R/W
b5	VDSEL1			R/W
b6	LVDAS	Voltage detection 0 circuit start bit (3)	0: Voltage monitor 0 reset enabled after reset 1: Voltage monitor 0 reset disabled after reset	R/W
b7	CSPROINI	Count source protection mode after reset select bit	0: Count source protect mode enabled after reset 1: Count source protect mode disabled after reset	R/W

Notes:
1. The OFS register is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not write additions to the OFS register. If the block including the OFS register is erased, the OFS register is set to FFh.
   When blank products are shipped, the OFS register is set to FFh. It is set to the written value after written by the user.
   When factory-programming products are shipped, the value of the OFS register is the value programmed by the user.
2. The same level of the voltage detection 0 level selected by bits VDSEL0 and VDESL1 is set in both functions of voltage monitor 0 reset and power-on reset.
3. To use power-on reset and voltage monitor 0 reset, set the LVDAS bit to 0 (voltage monitor 0 reset enabled after reset).

For a setting example of the OFS register, refer to **13.3.1 Setting Example of Option Function Select Area**.

LVDAS Bit (Voltage Detection 0 Circuit Start Bit)

The Vdet0 voltage to be monitored by the voltage detection 0 circuit is selected by bits VDSEL0 and VDSEL1.

5.1.4 Option Function Select Register 2 (OFS2)

Address 0FFDBh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	WDTRCS1	WDTRCS0	WDTUFS1	WDTUFS0
After Reset	User Setting Value (1)							

Bit	Symbol	Bit Name	Function	R/W
b0	WDTUFS0	Watchdog timer underflow period set bit	b1 b0 0 0: 03FFh 0 1: 0FFFh 1 0: 1FFFh 1 1: 3FFFh	R/W
b1	WDTUFS1			R/W
b2	WDTRCS0	Watchdog timer refresh acknowledgement period set bit	b3 b2 0 0: 25% 0 1: 50% 1 0: 75% 1 1: 100%	R/W
b3	WDTRCS1			R/W
b4	—	Reserved bits	Set to 1.	R/W
b5	—			
b6	—			
b7	—			

Note:

1. The OFS2 register is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not write additions to the OFS2 register. If the block including the OFS2 register is erased, the OFS2 register is set to FFh.
   When blank products are shipped, the OFS2 register is set to FFh. It is set to the written value after written by the user.
   When factory-programming products are shipped, the value of the OFS2 register is the value programmed by the user.

   For a setting example of the OFS2 register, refer to **13.3.1 Setting Example of Option Function Select Area**.

Bits WDTRCS0 and WDTRCS1 (Watchdog Timer Refresh Acknowledgement Period Set Bit)

Assuming that the period from when the watchdog timer starts counting until it underflows is 100%, the refresh acknowledgement period for the watchdog timer can be selected.
For details, refer to **14.3.1.1 Refresh Acknowledgment Period**.

5.2 Hardware Reset

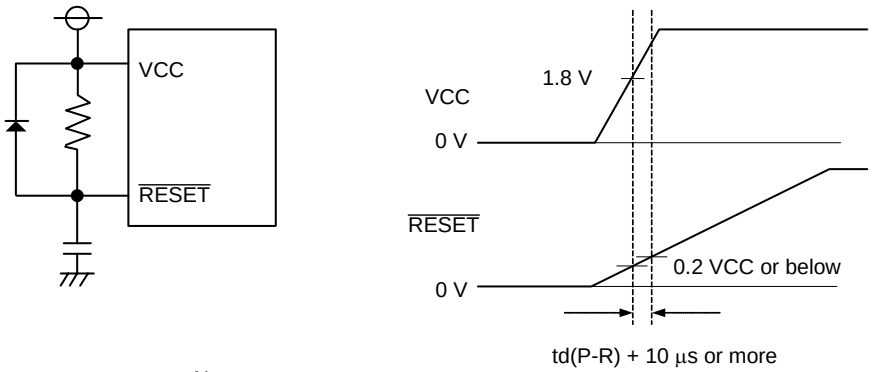
A reset is applied using the $\overline{\text{RESET}}$ pin. When an “L” signal is applied to the $\overline{\text{RESET}}$ pin while the supply voltage meets the recommended operating conditions, pins, CPU, and SFRs are all reset (refer to **Table 5.2 Pin Functions while $\overline{\text{RESET}}$ Pin Level is “L”**, **Figure 5.2 CPU Register Status after Reset**, and **Table 4.1 to 4.12 SFR Information**). When the input level applied to the $\overline{\text{RESET}}$ pin changes from “L” to “H”, a program is executed beginning with the address indicated by the reset vector. After reset, the low-speed on-chip oscillator clock with no division is automatically selected as the CPU clock.
Refer to **4. Special Function Registers (SFRs)** for the states of the SFRs after reset.
The internal RAM is not reset. If the $\overline{\text{RESET}}$ pin is pulled “L” while writing to the internal RAM is in progress, the contents of internal RAM will be undefined.
Figure 5.4 shows an Example of Hardware Reset Circuit and Operation and Figure 5.5 shows an Example of Hardware Reset Circuit (Usage Example of External Supply Voltage Detection Circuit) and Operation.

5.2.1 When Power Supply is Stable

(1) Apply “L” to the $\overline{\text{RESET}}$ pin.
(2) Wait for 10 µs.
(3) Apply “H” to the $\overline{\text{RESET}}$ pin.

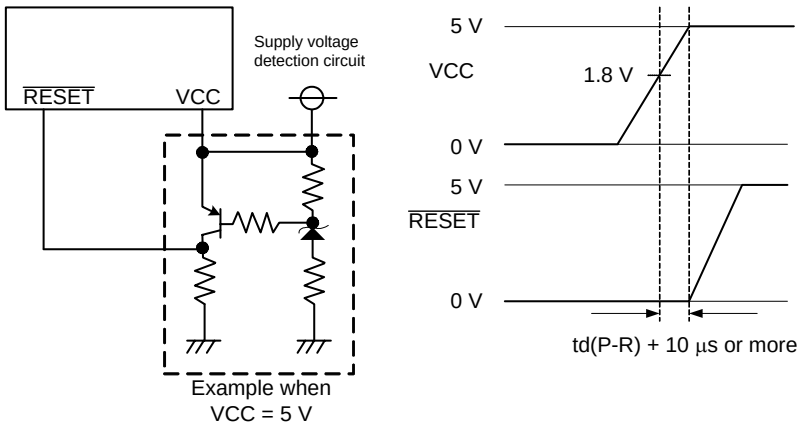
5.2.2 Power On

(1) Apply “L” to the $\overline{\text{RESET}}$ pin.
(2) Let the supply voltage increase until it meets the recommended operating conditions.
(3) Wait for td(P-R) or more to allow the internal power supply to stabilize (refer to **24. Electrical Characteristics**).
(4) Wait for 10 µs.
(5) Apply “H” to the $\overline{\text{RESET}}$ pin.



Note:
1. Refer to **24. Electrical Characteristics**.

Figure 5.4 Example of Hardware Reset Circuit and Operation



Note:
1. Refer to **24. Electrical Characteristics**.

Figure 5.5 Example of Hardware Reset Circuit (Usage Example of External Supply Voltage Detection Circuit) and Operation

5.3 Power-On Reset Function

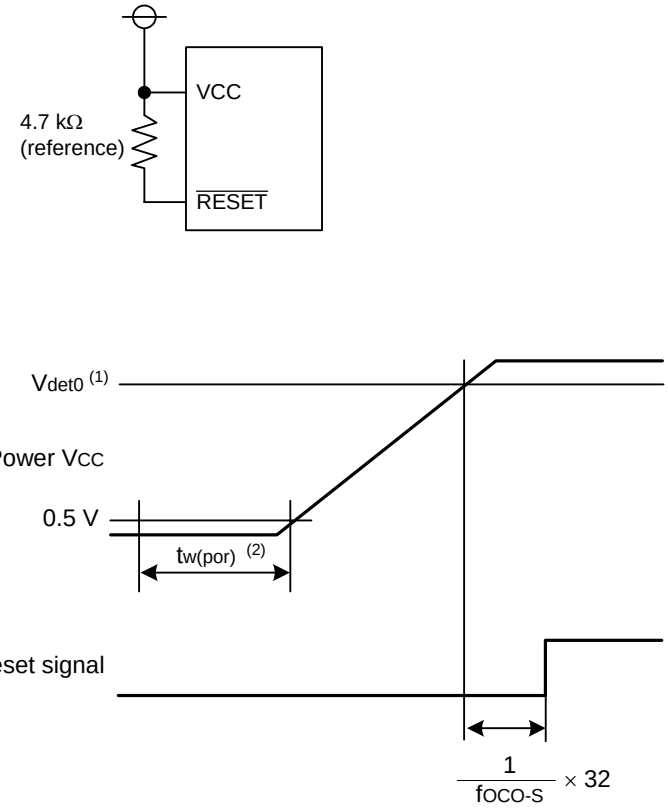
When the $\overline{\text{RESET}}$ pin is connected to the VCC pin via a pull-up resistor, and the VCC pin voltage level rises, the power-on reset function is enabled and the MCU resets its pins, CPU, and SFRs. When a capacitor is connected to the $\overline{\text{RESET}}$ pin, too, always keep the voltage to the $\overline{\text{RESET}}$ pin 0.8VCC or more.

When the input voltage to the VCC pin reaches the Vdet0 level or above, the low-speed on-chip oscillator clock starts counting. When the low-speed on-chip oscillator clock count reaches 32, the internal reset signal is held "H" and the MCU enters the reset sequence (refer to Figure 5.3). The low-speed on-chip oscillator clock with no division is automatically selected as the CPU clock after reset.

Refer to **4. Special Function Registers (SFRs)** for the states of the SFRs after power-on reset.

To use the power-on reset function, enable voltage monitor 0 reset by setting the LVDAS bit in the OFS register to 0.

Figure 5.6 shows an Example of Power-On Reset Circuit and Operation.



Notes:
1. V_{det0} indicates the voltage detection level of the voltage detection 0 circuit. Refer to **6. Voltage Detection Circuit** for details.
2. $t_{w(por)}$ indicates the duration the external power V_{CC} must be held below the valid voltage (0.5 V) to enable a power-on reset. When turning on the power after it falls with voltage monitor 0 reset disabled, maintain $t_{w(por)}$ for 1 ms or more.
3. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVDAS bit in the OFS register to 0.

Figure 5.6 Example of Power-On Reset Circuit and Operation

5.4 Voltage Monitor 0 Reset

A reset is applied using the on-chip voltage detection 0 circuit. The voltage detection 0 circuit monitors the input voltage to the VCC pin. The voltage to monitor is Vdet0. To use voltage monitor 0 reset, set the LVDAS bit in the OFS register to 0 (voltage monitor 0 reset enabled after reset). The Vdet0 voltage detection level can be changed by the settings of bits VDSEL0 to VDSEL1 in the OFS register.

When the input voltage to the VCC pin reaches the Vdet0 level or below, the pins, CPU, and SFRs are reset.

When the input voltage to the VCC pin reaches the Vdet0 level or above, the low-speed on-chip oscillator clock starts counting. When the low-speed on-chip oscillator clock count reaches 32, the internal reset signal is held “H” and the MCU enters the reset sequence (refer to Figure 5.3). The low-speed on-chip oscillator clock with no division is automatically selected as the CPU clock after reset.

To use the power-on reset function, enable voltage monitor 0 reset by setting the LVDAS bit in the OFS register to 0.

Bits VDSEL0 to VDSEL1 and LVDAS cannot be changed by a program. To set these bits, write values to b4 to b6 of address 0FFFFh using a flash programmer.

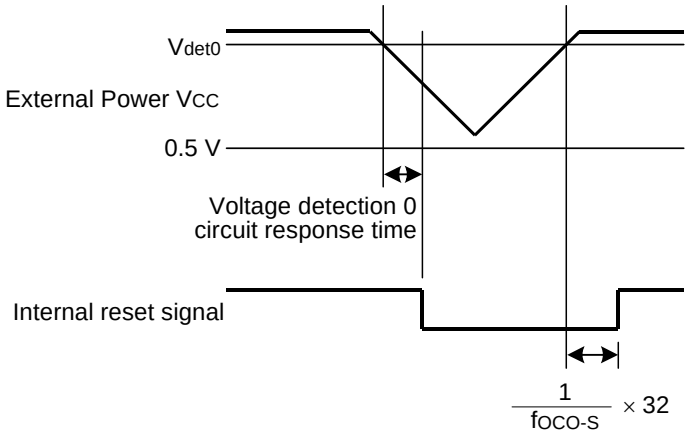
Refer to **5.1.3 Option Function Select Register (OFS)** for details of the OFS register.

Refer to **4. Special Function Registers (SFRs)** for the status of the SFRs after voltage monitor 0 reset.

The internal RAM is not reset. When the input voltage to the VCC pin reaches the Vdet0 level or below while writing to the internal RAM is in progress, the contents of internal RAM are undefined.

Refer to **6. Voltage Detection Circuit** for details of voltage monitor 0 reset.

Figure 5.7 shows an Example of Voltage Monitor 0 Reset Circuit and Operation.



Notes:
1. V_{det0} indicates the voltage detection level of the voltage detection 0 circuit. Refer to **6. Voltage Detection Circuit** for details.
2. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVDAS bit in the OFS register to 0.

Figure 5.7 Example of Voltage Monitor 0 Reset Circuit and Operation

5.5 Watchdog Timer Reset

When the PM12 bit in the PM1 register is set to 1 (reset when watchdog timer underflows), the MCU resets its pins, CPU, and SFRs if the watchdog timer underflows. Then the program beginning with the address indicated by the reset vector is executed. After reset, the low-speed on-chip oscillator clock with no division is automatically selected as the CPU clock.
Refer to **4. Special Function Registers (SFRs)** for the states of the SFRs after watchdog timer reset.
The internal RAM is not reset. When the watchdog timer underflows, while writing to the internal RAM is in progress, the contents of internal RAM are undefined.
The underflow period and refresh acknowledge period for the watchdog timer can be set by bits WDTUFS0 to WDTUFS1 and bits WDTRCS0 to WDTRCS1 in the OFS2 register, respectively.
Refer to **14. Watchdog Timer** for details of the watchdog timer.

5.6 Software Reset

When the PM03 bit in the PM0 register is set to 1 (MCU reset), the MCU resets its pins, CPU, and SFRs. The program beginning with the address indicated by the reset vector is executed. After reset, the low-speed on-chip oscillator clock with no division is automatically selected for the CPU clock.
Refer to **4. Special Function Registers (SFRs)** for the states of the SFRs after software reset.
The internal RAM is not reset.

5.7 Cold Start-Up/Warm Start-Up Determination Function

The cold start-up/warm start-up determination function uses the CWR bit in the RSTFR register to determine cold start-up (reset process) at power-on and warm start-up (reset process) when a reset occurred during operation.
The CWR bit is set to 0 (cold start-up) at power-on and also set to 0 at a voltage monitor 0 reset. If 1 is written to the CWR bit by a program, it is set to 1. This bit remains unchanged at a hardware reset, software reset, or watchdog timer reset.
The cold start-up/warm start-up determination function uses voltage monitor 0 reset.
Figure 5.8 shows an Operating Example of Cold Start-Up/Warm Start-Up Function

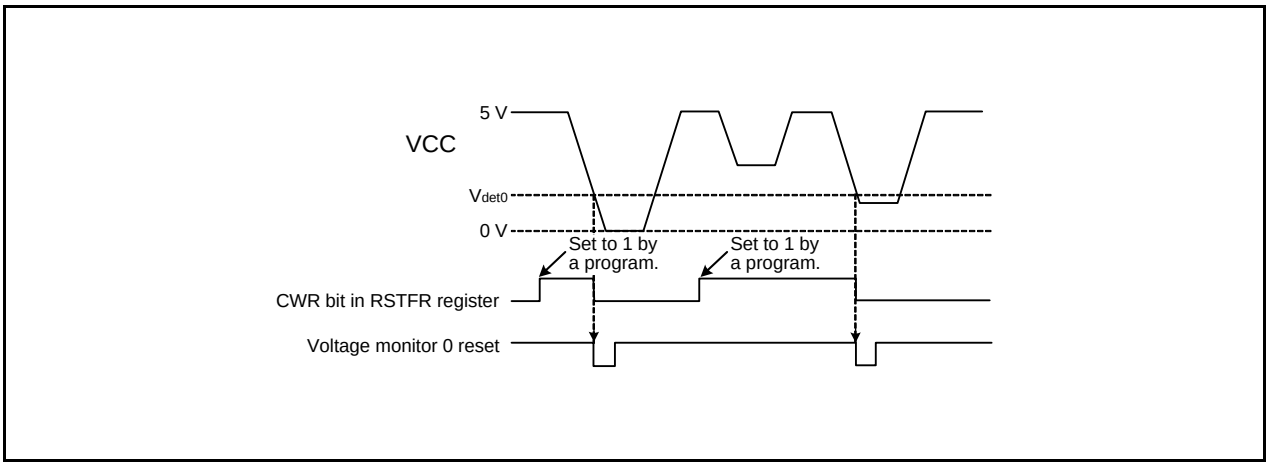


Figure 5.8 Operating Example of Cold Start-Up/Warm Start-Up Function

5.8 Reset Source Determination Function

The RSTFR register can be used to detect whether a hardware reset, software reset, or watchdog timer reset has occurred.
If a hardware reset occurs, the HWR bit is set to 1 (detected). If a software reset occurs, the SWR bit is set to 1 (detected). If a watchdog timer reset occurs, the WDR bit is set to 1 (detected).

6. Voltage Detection Circuit

The voltage detection circuit monitors the voltage input to the VCC pin. This circuit can be used to monitor the VCC input voltage by a program.

6.1 Overview

The detection voltage of voltage detection 0 can be selected among four levels using the OFS register.
The detection voltage of voltage detection 1 can be selected among 16 levels using the VD1LS register.
The voltage monitor 0 reset, and voltage monitor 1 interrupt and voltage monitor 2 interrupt can also be used.

Table 6.1 Voltage Detection Circuit Specifications

Item		Voltage Monitor 0	Voltage Monitor 1	Voltage Monitor 2
VCC monitor	Voltage to monitor	Vdet0	Vdet1	Vdet2
	Detection target	Whether passing through Vdet0 by rising or falling	Whether passing through Vdet1 by rising or falling	Whether passing through Vdet2 by rising or falling
	Detection voltage	Selectable among 4 levels using the OFS register.	Selectable among 16 levels using the VD1LS register.	Fixed level
	Monitor	None	The VW1C3 bit in the VW1C register	The VCA13 bit in the VCA1 register
			Whether VCC is higher or lower than Vdet1	Whether VCC is higher or lower than Vdet2
Process at voltage detection	Reset	Voltage monitor 0 reset	None	None
		Reset at Vdet0 > VCC; CPU operation restarts at VCC > Vdet0		
	Interrupts	None	Voltage monitor 1 interrupt	Voltage monitor 2 interrupt
			Non-maskable or maskable selectable	Non-maskable or maskable selectable
			Interrupt request at: Vdet1 > VCC and/or VCC > Vdet1	Interrupt request at: Vdet2 > VCC and/or VCC > Vdet2
Digital filter	Switching enable/ disable	No digital filter function	Supported	Supported
	Sampling time	—	(fOCO-S divided by n) × 2 n: 1, 2, 4, and 8	(fOCO-S divided by n) × 2 n: 1, 2, 4, and 8

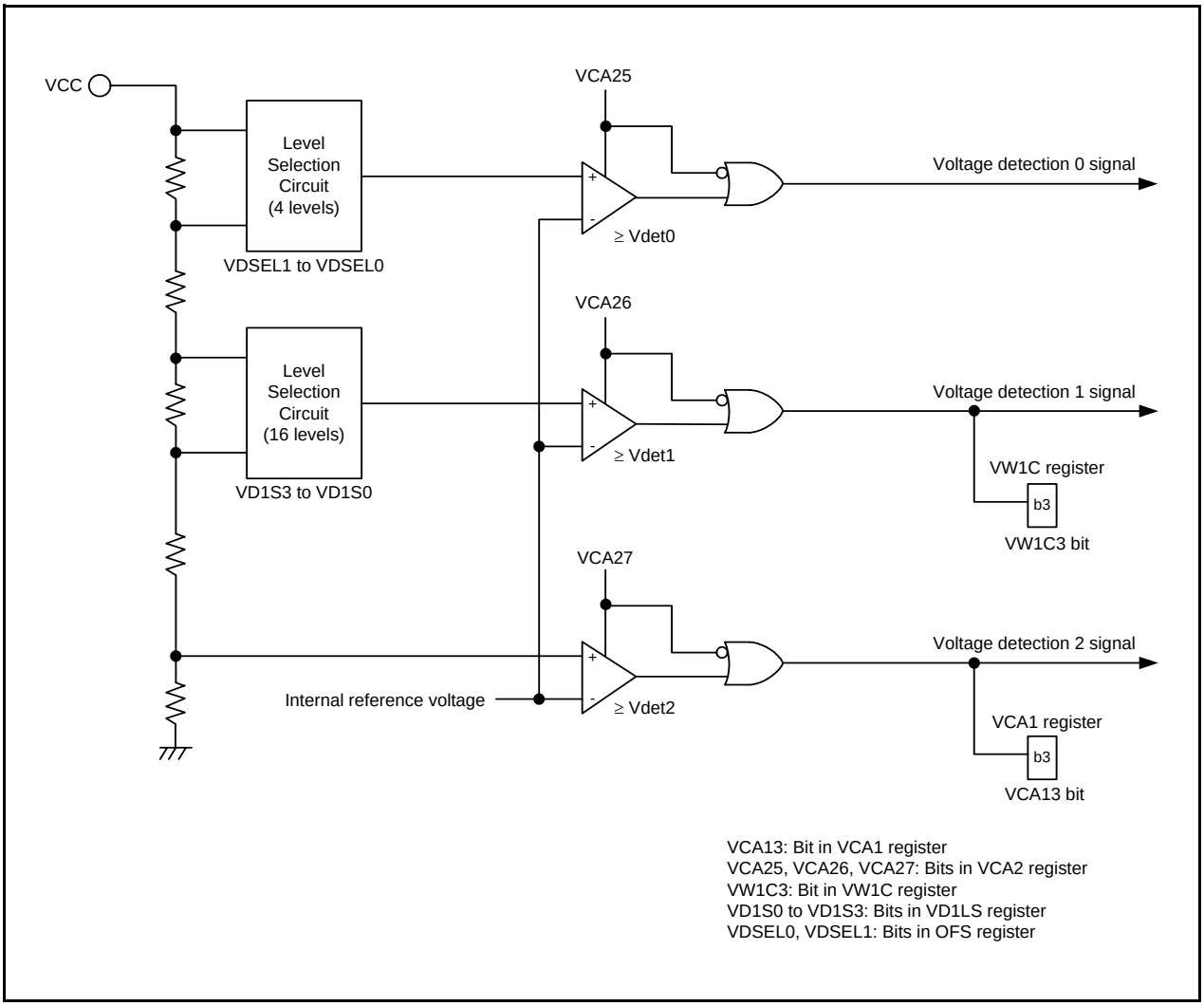


Figure 6.1 Voltage Detection Circuit Block Diagram

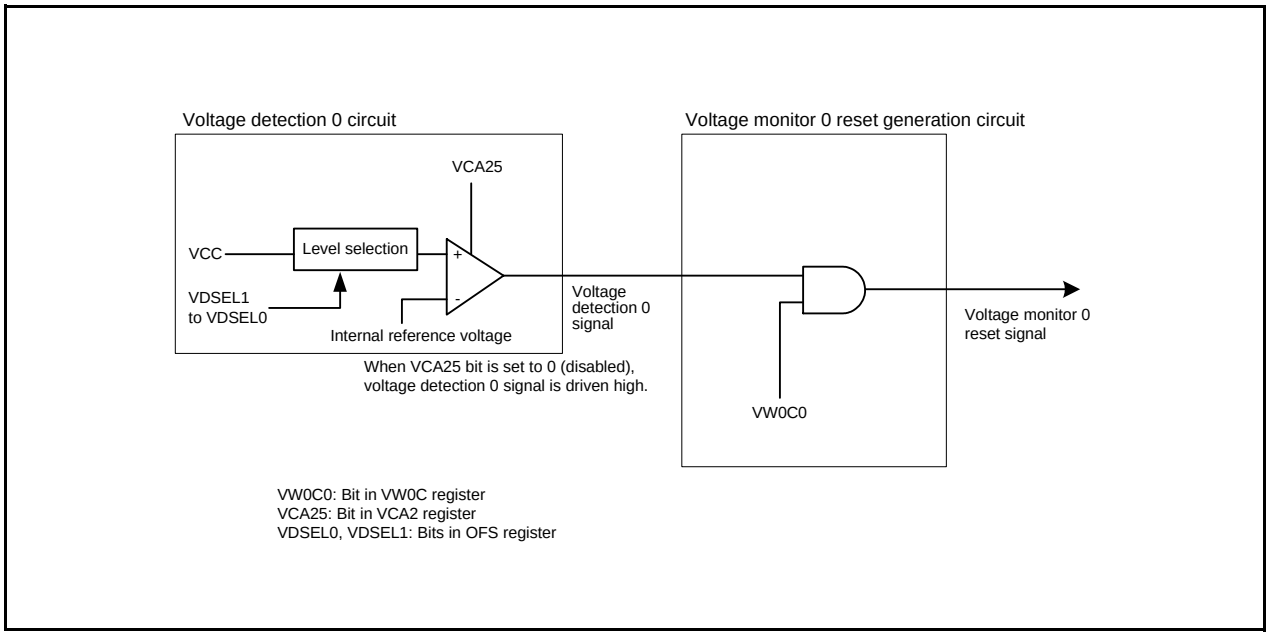


Figure 6.2 Block Diagram of Voltage Monitor 0 Reset Generation Circuit

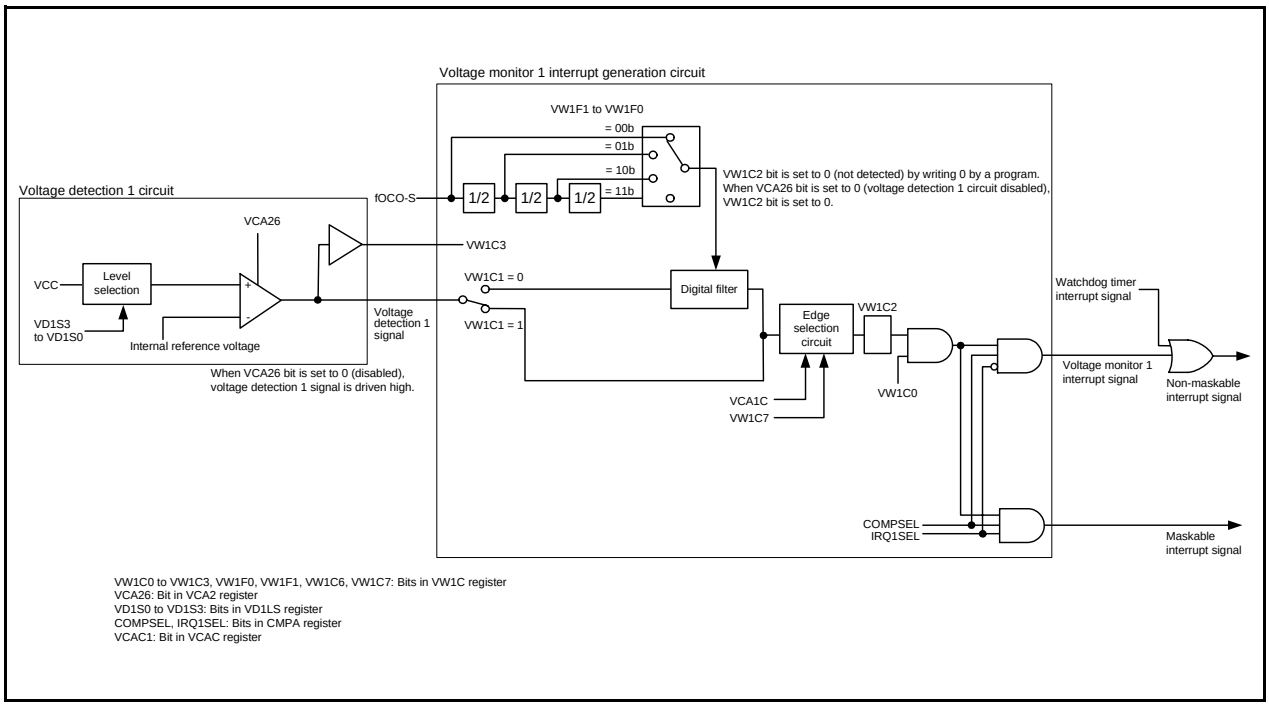


Figure 6.3 Block Diagram of Voltage Monitor 1 Interrupt Generation Circuit

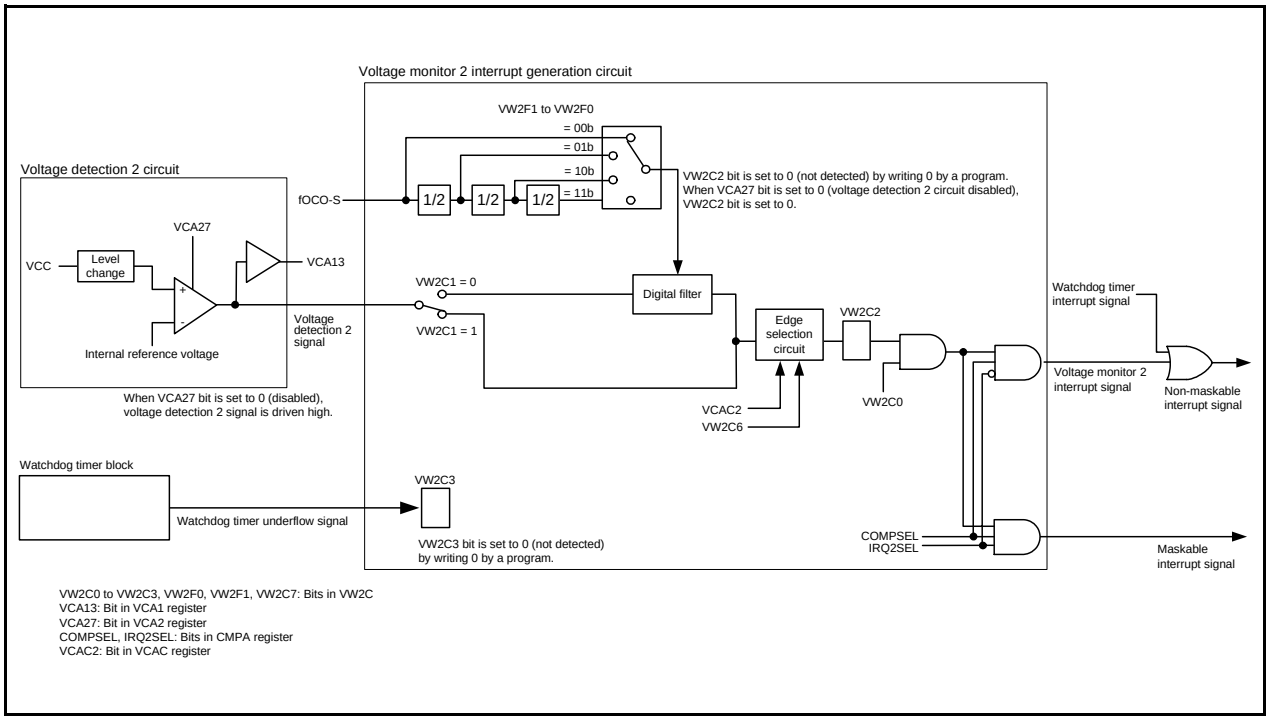


Figure 6.4 Block Diagram of Voltage Monitor 2 Interrupt Generation Circuit

6.2 Registers

6.2.1 Voltage Monitor Circuit Control Register (CMPA)

Address 0030h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	COMPSEL	—	IRQ2SEL	IRQ1SEL	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved bits	Set to 0.	R/W
b1	—			
b2	—			
b3	—			
b4	IRQ1SEL	Voltage monitor 1 interrupt type select bit (1)	0: Non-maskable interrupt 1: Maskable interrupt	R/W
b5	IRQ2SEL	Voltage monitor 2 interrupt type select bit (2)	0: Non-maskable interrupt 1: Maskable interrupt	R/W
b6	—	Reserved bit	Set to 0.	R/W
b7	COMPSEL	Voltage monitor interrupt type selection enable bit (1, 2)	0: Bits IRQ1SEL and IRQ2SEL disabled 1: Bits IRQ1SEL and IRQ2SEL enabled	R/W

Notes:
1. When the VW1C0 bit in the VW1C register is set to 1 (enabled), do not set bits IRQ1SEL and COMPSEL simultaneously (with one instruction).
2. When the VW2C0 bit in the VW2C register is set to 1 (enabled), do not set bits IRQ2SEL and COMPSEL simultaneously (with one instruction).

6.2.2 Voltage Monitor Circuit Edge Select Register (VCAC)

Address 0031h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	VCAC2	VCAC1	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b1	VCAC1	Voltage monitor 1 circuit edge select bit (1)	0: One edge 1: Both edges	R/W
b2	VCAC2	Voltage monitor 2 circuit edge select bit (2)	0: One edge 1: Both edges	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	—			
b5	—			
b6	—			
b7	—			

Notes:
1. When the VCAC1 bit is set tot 0 (one edge), the VW1C7 bit in the VW1C register is enabled. Set the VW1C7 bit after setting the VCAC1 bit to 0.
2. When the VCAC2 bit is set tot 0 (one edge), the VW2C7 bit in the VW2C register is enabled. Set the VW2C7 bit after setting the VCAC2 bit to 0.

6.2.3 Voltage Detect Register 1 (VCA1)

Address 0033h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	VCA13	—	—	—
After Reset	0	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved bits	Set to 0.	R/W
b1	—			
b2	—			
b3	VCA13	Voltage detection 2 signal monitor flag (1)	0: VCC < Vdet2 1: VCC ≥ Vdet2 or voltage detection 2 circuit disabled	R
b4	—	Reserved bits	Set to 0.	R/W
b5	—			
b6	—			
b7	—			

Note:
1. When the VCA27 bit in the VCA2 register is set to 1 (voltage detection 2 circuit enabled), the VCA13 bit is enabled.
   When the VCA27 bit in the VCA2 register is set to 0 (voltage detection 2 circuit disabled), the VCA13 bit is set to 1 (VCC ≥ Vdet2).

6.2.4 Voltage Detect Register 2 (VCA2)

Address 0034h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	VCA27	VCA26	VCA25	—	—	—	—	VCA20
After Reset	0	0	0	0	0	0	0	0

The above applies when the LVDAS bit in the OFS register is set to 1.

After Reset	0	0	1	0	0	0	0	0

The above applies when the LVDAS bit in the OFS register is set to 0.

Bit	Symbol	Bit Name	Function	R/W
b0	VCA20	Internal power low consumption enable bit (1)	0: Low consumption disabled 1: Low consumption enabled (2)	R/W
b1	—	Reserved bits	Set to 0.	R/W
b2	—			
b3	—			
b4	—			
b5	VCA25	Voltage detection 0 enable bit (3)	0: Voltage detection 0 circuit disabled 1: Voltage detection 0 circuit enabled	R/W
b6	VCA26	Voltage detection 1 enable bit (4)	0: Voltage detection 1 circuit disabled 1: Voltage detection 1 circuit enabled	R/W
b7	VCA27	Voltage detection 2 enable bit (5)	0: Voltage detection 2 circuit disabled 1: Voltage detection 2 circuit enabled	R/W

Notes:
1. Use the VCA20 bit only when the MCU enters wait mode. To set the VCA20 bit, follow the procedure shown in **23.2.7 Reducing Internal Power Consumption Using VCA20 Bit**.
2. When the VCA20 bit is set to 1 (low consumption enabled), do not set the CM10 bit in the CM1 register to 1 (stop mode).
3. When writing to the VCA25 bit, set a value after reset.
4. To use the voltage detection 1 interrupt or the VW1C3 bit in the VW1C register, set the VCA26 bit to 1. After the VCA26 bit is set to 1 from 0, allow td(E-A) to elapse before the voltage detection 1 circuit starts operation.
5. To use the voltage detection 2 interrupt or the VCA13 bit in the VCA1 register, set the VCA27 bit to 1. After the VCA27 bit is set to 1 from 0, allow td(E-A) to elapse before the voltage detection 2 circuit starts operation.

Set the PRC3 bit in the PRCR register to 1 (write enabled) before rewriting the VCA2 register.

6.2.5 Voltage Detection 1 Level Select Register (VD1LS)

Address 0036h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	VD1S3	VD1S2	VD1S1	VD1S0
After Reset	0	0	0	0	0	1	1	1

Bit	Symbol	Bit Name	Function	R/W
b0	VD1S0	Voltage detection 1 level select bit (Reference voltage when the voltage falls)	b3 b2 b1 b0 0 0 0 0: 2.20 V (Vdet1_0) 0 0 0 1: 2.35 V (Vdet1_1) 0 0 1 0: 2.50 V (Vdet1_2) 0 0 1 1: 2.65 V (Vdet1_3) 0 1 0 0: 2.80 V (Vdet1_4) 0 1 0 1: 2.95 V (Vdet1_5) 0 1 1 0: 3.10 V (Vdet1_6) 0 1 1 1: 3.25 V (Vdet1_7) 1 0 0 0: 3.40 V (Vdet1_8) 1 0 0 1: 3.55 V (Vdet1_9) 1 0 1 0: 3.70 V (Vdet1_A) 1 0 1 1: 3.85 V (Vdet1_B) 1 1 0 0: 4.00 V (Vdet1_C) 1 1 0 1: 4.15 V (Vdet1_D) 1 1 1 0: 4.30 V (Vdet1_E) 1 1 1 1: 4.45 V (Vdet1_F)	R/W
b1	VD1S1			R/W
b2	VD1S2			R/W
b3	VD1S3			R/W
b4	—	Reserved bits	Set to 0.	R/W
b5	—			
b6	—			
b7	—			

Set the PRC3 bit in the PRCR register to 1 (write enabled) before rewriting the VD1LS register.

6.2.6 Voltage Monitor 0 Circuit Control Register (VW0C)

Address 0038h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	VW0C0
After Reset	1	1	0	0	X	0	1	0

The above applies when the LVDAS bit in the OFS register is set to 1.

After Reset	1	1	0	0	X	0	1	1

The above applies when the LVDAS bit in the OFS register is set to 0.

Bit	Symbol	Bit Name	Function	R/W
b0	VW0C0	Voltage monitor 0 reset enable bit (1)	0: Disabled 1: Enabled	R/W
b1	—	Reserved bit	Set to 1.	R/W
b2	—	Reserved bit	Set to 0.	R/W
b3	—	Reserved bit	When read, the content is undefined.	R
b4	—	Reserved bits	Set to 0.	R/W
b5	—			
b6	—	Reserved bits	Set to 1.	R/W
b7	—			

Note:
1. The VW0C0 bit is enabled when the VCA25 bit in the VCA2 register is set to 1 (voltage detection 0 circuit enabled). When writing to the VW0C0 bit, set a value after reset.

Set the PRC3 bit in the PRCR register to 1 (write enabled) before writing the VW0C register.

6.2.7 Voltage Monitor 1 Circuit Control Register (VW1C)

Address 0039h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	VW1C7	—	VW1F1	VW1F0	VW1C3	VW1C2	VW1C1	VW1C0
After Reset	1	0	0	0	1	0	1	0

Bit	Symbol	Bit Name	Function	R/W
b0	VW1C0	Voltage monitor 1 interrupt enable bit (1)	0: Disabled 1: Enabled	R/W
b1	VW1C1	Voltage monitor 1 digital filter disable mode select bit (2, 6)	0: Digital filter enabled mode (digital filter circuit enabled) 1: Digital filter disable mode (digital filter circuit disabled)	R/W
b2	VW1C2	Voltage change detection flag (3, 4)	0: Not detected 1: Vdet1 passing detected	R/W
b3	VW1C3	Voltage detection 1 signal monitor flag (3)	0: VCC < Vdet1 1: VCC ≥ Vdet1 or voltage detection 1 circuit disabled	R
b4	VW1F0	Sampling clock select bit (6)	b5 b4 0 0: fOCO-S divided by 1 0 1: fOCO-S divided by 2 1 0: fOCO-S divided by 4 1 1: fOCO-S divided by 8	R/W
b5	VW1F1			R/W
b6	—	Reserved bit	Set to 0.	R/W
b7	VW1C7	Voltage monitor 1 interrupt generation condition select bit (5)	0: When VCC reaches Vdet1 or above. 1: When VCC reaches Vdet1 or below.	R/W

Notes:

1. The VW1C0 is enabled when the VCA26 bit in the VCA2 register is set to 1 (voltage detection 1 circuit enabled). Set the VW1C0 bit to 0 (disabled) when the VCA26 bit is set to 0 (voltage detection 1 circuit disabled).
   To set the VW1C0 bit to 1 (enabled), follow the procedure shown in **Table 6.2 Procedure for Setting Bits Associated with Voltage Monitor 1 Interrupt**.
2. When using the digital filter (while the VW1C1 bit is 0), set the CM14 bit in the CM1 register to 0 (low-speed on-chip oscillator on).
   To use the voltage monitor 1 interrupt to exit stop mode, set the VW1C1 bit in the VW1C register to 1 (digital filter disabled).
3. Bits VW1C2 and VW1C3 are enabled when the VCA26 bit in the VCA2 register is set to 1(voltage detection 1 circuit enabled).
4. Set the VW1C2 bit to 0 by a program. When 0 is written by a program, this bit is set to 0 (and remains unchanged even if 1 is written to it).
5. The VW1C7 bit is enabled when the VCAC1 bit in the VCAC register is set to 0 (one edge). After setting the VCAC1 bit to 0, set the VW1C7 bit.
6. When the VW1C0 bit is set to 1 (enabled), do not set the VW1C1 bit and bits VW1F1 and VW1F0 simultaneously (with one instruction).

   Set the PRC3 bit in the PRCR register to 1 (write enabled) before writing the VW1C register.
   Rewriting the VW1C register may set the VW1C2 bit to 1. Set the VW1C2 bit to 0 after rewriting the VW1C register.

6.2.8 Voltage Monitor 2 Circuit Control Register (VW2C)

Address 003Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	VW2C7	—	VW2F1	VW2F0	VW2C3	VW2C2	VW2C1	VW2C0
After Reset	1	0	0	0	0	0	1	0

Bit	Symbol	Bit Name	Function	R/W
b0	VW2C0	Voltage monitor 2 interrupt enable bit (1)	0: Disabled 1: Enabled	R/W
b1	VW2C1	Voltage monitor 2 digital filter disable mode select bit (2, 6)	0: Digital filter enable mode (digital filter circuit enabled) 1: Digital filter disable mode (digital filter circuit disabled)	R/W
b2	VW2C2	Voltage change detection flag (3, 4)	0: Not detected 1: Vdet2 passing detected	R/W
b3	VW2C3	WDT detection monitor flag (4)	0: Not detected 1: Detected	R/W
b4	VW2F0	Sampling clock select bit (6)	b5 b4 0 0: fOCO-S divided by 1 0 1: fOCO-S divided by 2 1 0: fOCO-S divided by 4 1 1: fOCO-S divided by 8	R/W
b5	VW2F1			R/W
b6	—	Reserved bit	Set to 0.	R/W
b7	VW2C7	Voltage monitor 2 interrupt generation condition select bit (5)	0: When VCC reaches Vdet2 or above. 1: When VCC reaches Vdet2 or below.	R/W

Notes:

1. The VW2C0 is enabled when the VCA27 bit in the VCA2 register is set to 1 (voltage detection 2 circuit enabled). Set the VW2C0 bit to 0 (disabled) when the VCA27 bit is set to 0 (voltage detection 2 circuit disabled).
   To set the VW2C0 bit to 1 (enabled), follow the procedure shown in **Table 6.3 Procedure for Setting Bits Associated with Voltage Monitor 2 Interrupt**.
2. When using the digital filter (while the VW2C1 bit is 0), set the CM14 bit in the CM1 register to 0 (low-speed on-chip oscillator on).
   To use the voltage monitor 2 interrupt to exit stop mode, set the VW2C1 bit in the VW2C register to 1 (digital filter disabled).
3. The VW2C2 bit is enabled when the VCA27 bit in the VCA2 register is set to 1 (voltage detection 2 circuit enabled).
4. Set this bit to 0 by a program. When 0 is written by a program, this bit is set to 0 (and remains unchanged even if 1 is written to it).
5. The VW2C7 bit is enabled when the VCAC2 bit in the VCAC register is set to 0 (one edge). After setting the VCAC2 bit to 0, set the VW2C7 bit.
6. When the VW2C0 bit is set to 1 (enabled), do not set the VW2C1 bit and bits VW2F1 and VW2F0 simultaneously (with one instruction).

Set the PRC3 bit in the PRCR register to 1 (write enabled) before rewriting the VW2C register.
Rewriting the VW2C register may set the VW2C2 bit to 1. After rewriting this register, set the VW2C2 bit to 0.

6.2.9 Option Function Select Register (OFS)

Address 0FFFFh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CSPROINI	LVDAS	VDSEL1	VDSEL0	ROMCP1	ROMCR	—	WDTON
After Reset	User Setting Value (1)							

Bit	Symbol	Bit Name	Function	R/W
b0	WDTON	Watchdog timer start select bit	0: Watchdog timer automatically starts after reset. 1: Watchdog timer is stopped after reset.	R/W
b1	—	Reserved bit	Set to 1.	R/W
b2	ROMCR	ROM code protect disable bit	0: ROM code protect disabled 1: ROMCP1 bit enabled	R/W
b3	ROMCP1	ROM code protect bit	0: ROM code protect enabled 1: ROM code protect disabled	R/W
b4	VDSEL0	Voltage detection 0 level select bit (2)	b5 b4 0 0: 3.80 V selected (Vdet0_3) 0 1: 2.85 V selected (Vdet0_2) 1 0: 2.35 V selected (Vdet0_1) 1 1: 1.90 V selected (Vdet0_0)	R/W
b5	VDSEL1			R/W
b6	LVDAS	Voltage detection 0 circuit start bit (3)	0: Voltage monitor 0 reset enabled after reset 1: Voltage monitor 0 reset disabled after reset	R/W
b7	CSPROINI	Count source protection mode after reset select bit	0: Count source protect mode enabled after reset 1: Count source protect mode disabled after reset	R/W

Notes:
1. The OFS register is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not write additions to the OFS register. If the block including the OFS register is erased, the OFS register is set to FFh.
   When blank products are shipped, the OFS register is set to FFh. It is set to the written value after written by the user.
   When factory-programming products are shipped, the value of the OFS register is the value programmed by the user.
2. The same level of the voltage detection 0 level selected by bits VDSEL0 and VDESL1 is set in both functions of voltage monitor 0 reset and power-on reset.
3. To use power-on reset and voltage monitor 0 reset, set the LVDAS bit to 0 (voltage monitor 0 reset enabled after reset).

For a setting example of the OFS register, refer to **13.3.1 Setting Example of Option Function Select Area**.

LVDAS Bit (Voltage Detection 0 Circuit Start Bit)

The Vdet0 voltage to be monitored by the voltage detection 0 circuit is selected by bits VDSEL0 and VDSEL1.

6.3 VCC Input Voltage

6.3.1 Monitoring Vdet0

Vdet0 cannot be monitored.

6.3.2 Monitoring Vdet1

Once the following settings are made, the comparison result of voltage monitor 1 can be monitored by the VW1C3 bit in the VW1C register after td(E-A) has elapsed (refer to **24. Electrical Characteristics**).

(1) Set bits VD1S3 to VD1S0 in the VD1LS register (voltage detection 1 detection voltage).
(2) Set the VCA26 bit in the VCA2 register to 1 (voltage detection 1 circuit enabled).

6.3.3 Monitoring Vdet2

Once the following settings are made, the comparison result of voltage monitor 2 can be monitored by the VCA13 bit in the VCA1 register after td(E-A) has elapsed (refer to **24. Electrical Characteristics**).

- Set the VCA27 bit in the VCA2 register to 1 (voltage detection 2 circuit enabled).

6.4 Voltage Monitor 0 Reset

To use voltage monitor 0 reset, set the LVDAS bit in the OFS register to 0 (voltage monitor 0 reset enabled after reset).

Figure 6.5 shows an Operating Example of Voltage Monitor 0 Reset.

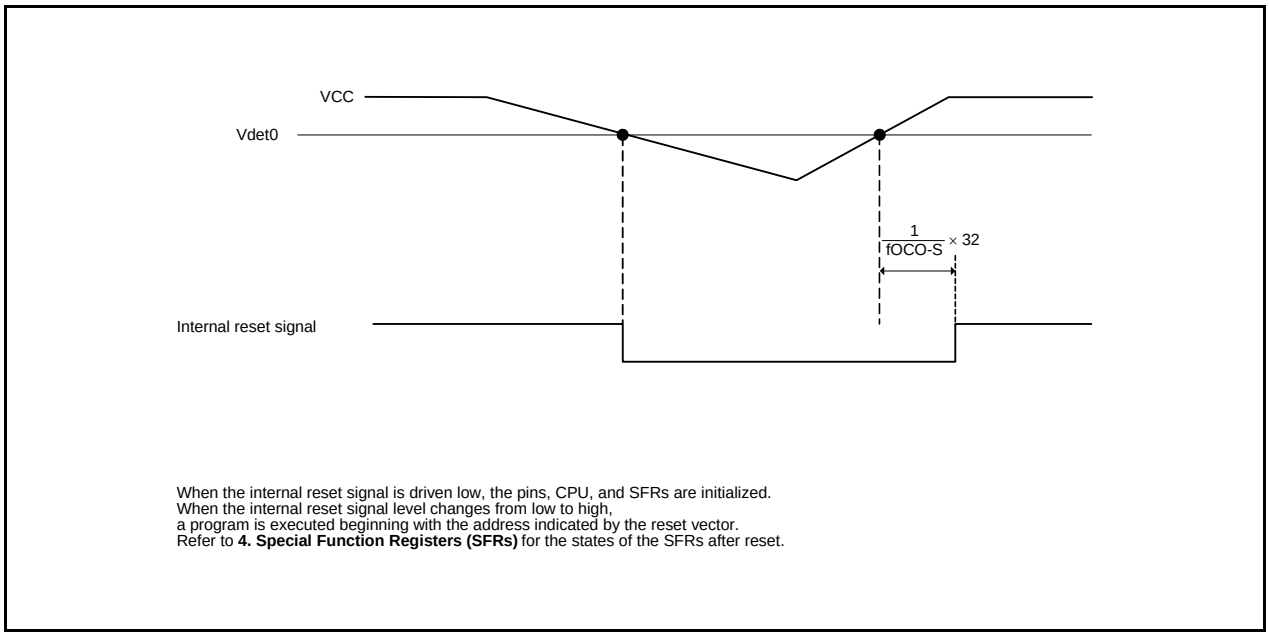


Figure 6.5 Operating Example of Voltage Monitor 0 Reset

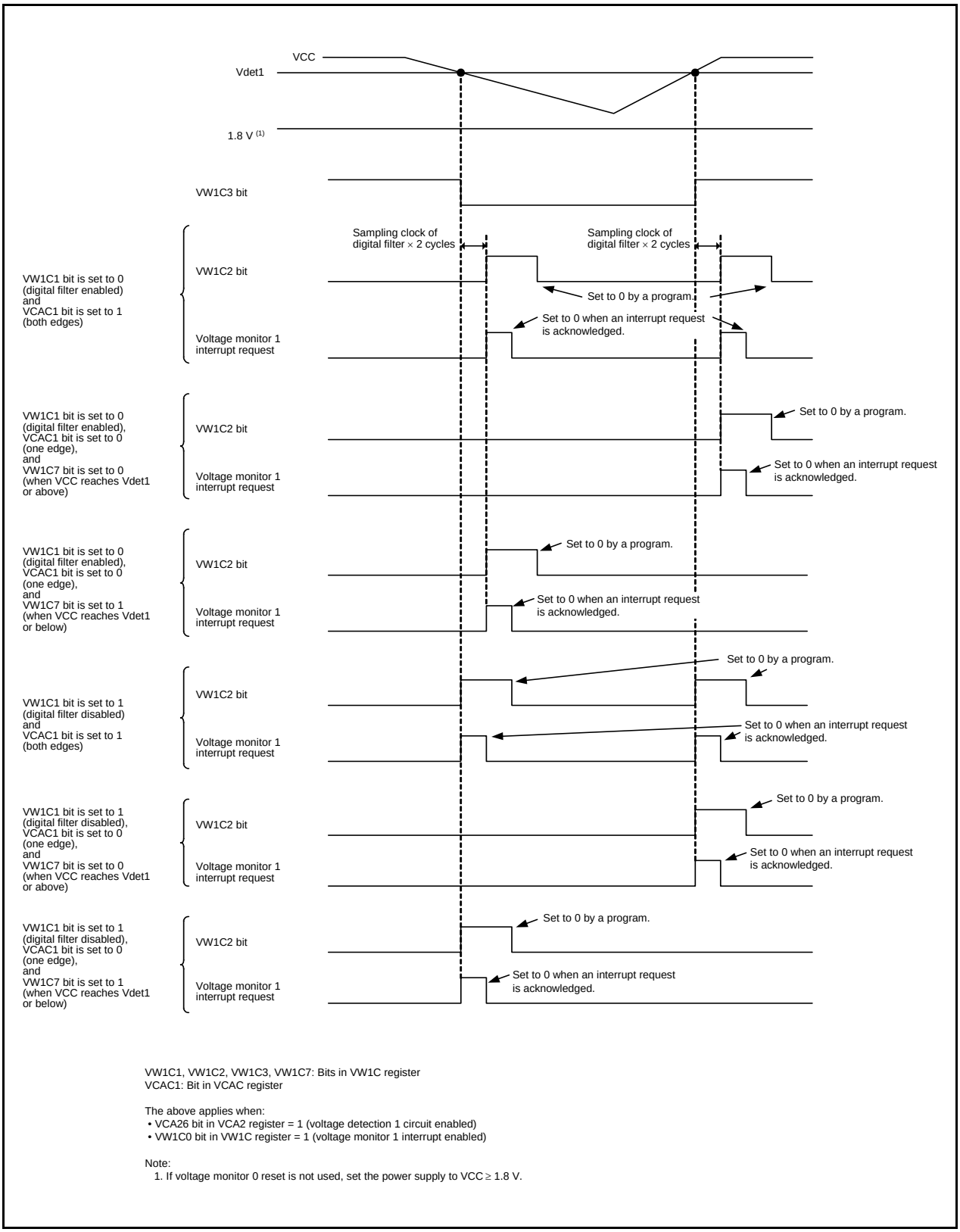
6.5 Voltage Monitor 1 Interrupt

Table 6.2 lists the Procedure for Setting Bits Associated with Voltage Monitor 1 Interrupt. Figure 6.6 shows an Operating Example of Voltage Monitor 1 Interrupt.
To use the voltage monitor 1 interrupt to exit stop mode, set the VW1C1 bit in the VW1C register to 1 (digital filter disabled).

Table 6.2 Procedure for Setting Bits Associated with Voltage Monitor 1 Interrupt

Step	When Using Digital Filter	When Using No Digital Filter
1	Select the voltage detection 1 detection voltage by bits VD1S3 to VD1S0 in the VD1LS register.	
2	Set the VCA26 bit in the VCA2 register to 1 (voltage detection 1 circuit enabled).	
3	Wait for td(E-A).	
4	Set the COMPSEL bit in the CMPA register to 1.	
5 (1)	Select the interrupt type by the IRQ1SEL in the CMPA register.	
6	Select the sampling clock of the digital filter by bits VW1F0 and VW1F1 in the VW1C register.	Set the VW1C1 bit in the VW1C register to 1 (digital filter disabled).
7 (2)	Set the VW1C1 bit in the VW1C register to 0 (digital filter enabled).	—
8	Select the interrupt request timing by the VCAC1 bit in the VCAC register and the VW1C7 bit in the VW1C register.	
9	Set the VW1C2 bit in the VW1C register to 0.	
10	Set the CM14 bit in the CM1 register to 0 (low-speed on-chip oscillator on)	—
11	Wait for 2 cycles of the sampling clock of the digital filter	— (No wait time required)
12 (3)	Set the VW1C0 bit in the VW1C register to 1 (voltage monitor 1 interrupt enabled)	

Notes:
1. When the VW1C0 bit is set to 0, steps 4 and 5 can be executed simultaneously (with one instruction).
2. When the VW1C0 bit is set to 0, steps 6 and 7 can be executed simultaneously (with one instruction).
3. When the voltage detection 1 circuit is enabled while the voltage monitor 1 interrupt is disabled, low voltage is detected and the VW1C2 bit becomes 1.
   When low voltage is detected after the voltage detection 1 circuit is enabled until an interrupt is enabled for the setting procedure of bits associated with voltage monitor 1 interrupt, an interrupt is not generated. After an interrupt is enabled, read the VW1C2 bit. When the bit is read as 1, perform the process that occurs when low voltage is detected.



VW1C1, VW1C2, VW1C3, VW1C7: Bits in VW1C register
VCAC1: Bit in VCAC register

The above applies when:
- VCA26 bit in VCA2 register = 1 (voltage detection 1 circuit enabled)
- VW1C0 bit in VW1C register = 1 (voltage monitor 1 interrupt enabled)

Note:
1. If voltage monitor 0 reset is not used, set the power supply to VCC ≥ 1.8 V.

Figure 6.6 Operating Example of Voltage Monitor 1 Interrupt

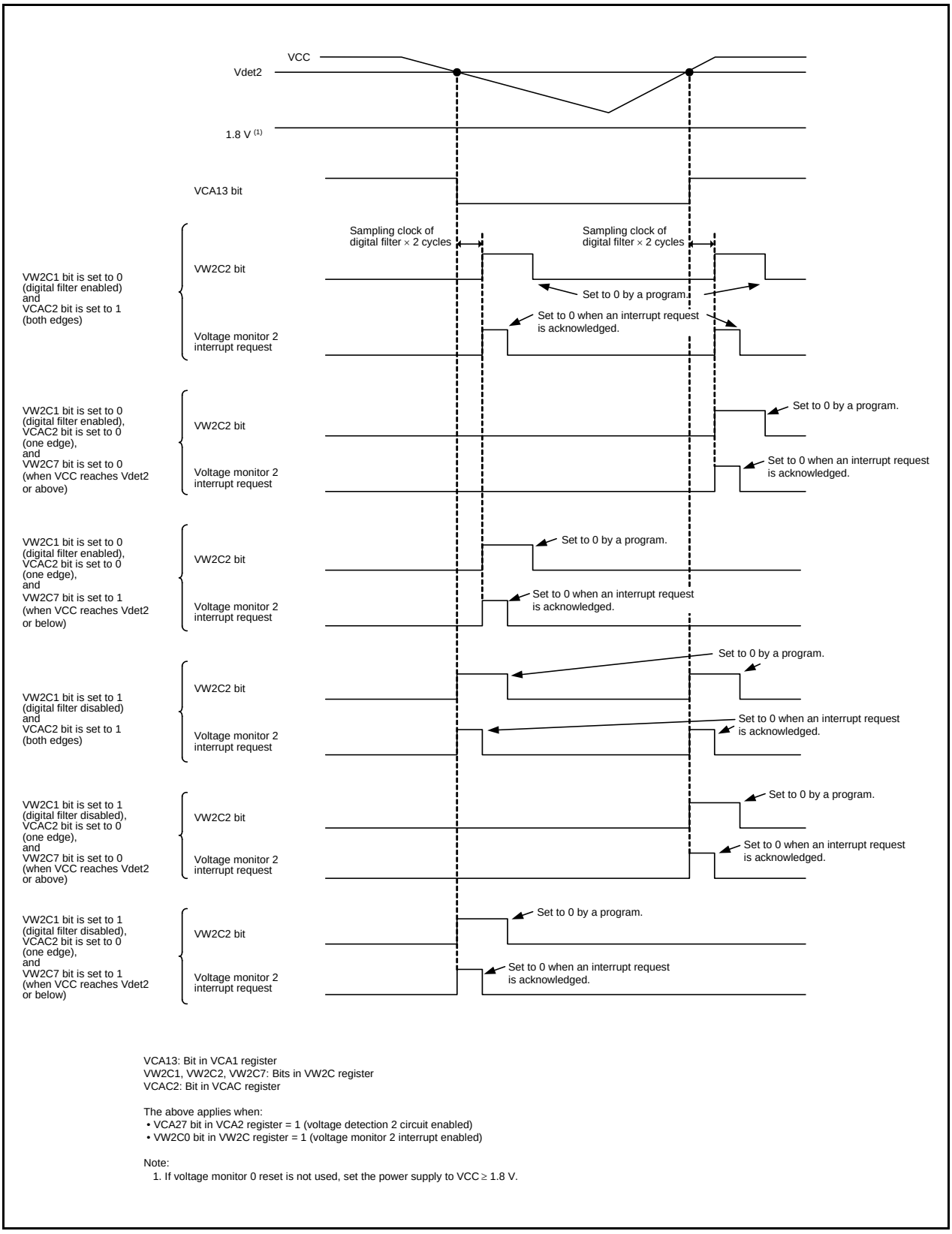
6.6 Voltage Monitor 2 Interrupt

Table 6.3 lists the Procedure for Setting Bits Associated with Voltage Monitor 2 Interrupt. Figure 6.7 shows an Operating Example of Voltage Monitor 2 Interrupt.
To use the voltage monitor 2 interrupt to exit stop mode, set the VW2C1 bit in the VW2C register to 1 (digital filter disabled).

Table 6.3 Procedure for Setting Bits Associated with Voltage Monitor 2 Interrupt

Step	When Using Digital Filter	When Using No Digital Filter
1	Set the VCA27 bit in the VCA2 register to 1 (voltage detection 2 circuit enabled).	
2	Wait for td(E-A).	
3	Set the COMPSEL bit in the CMPA register to 1.	
4 (1)	Select the interrupt type by the IRQ2SEL in the CMPA register.	
5	Select the sampling clock of the digital filter by bits VW2F0 and VW2F1 in the VW2C register.	Set the VW2C1 bit in the VW2C register to 1 (digital filter disabled).
6 (2)	Set the VW2C1 bit in the VW2C register to 0 (digital filter enabled).	—
7	Select the interrupt request timing by the VCAC2 bit in the VCAC register and the VW2C7 bit in the VW2C register.	
8	Set the VW2C2 bit in the VW2C register to 0.	
9	Set the CM14 bit in the CM1 register to 0 (low-speed on-chip oscillator on).	—
10	Wait for 2 cycles of the sampling clock of the digital filter.	— (No wait time required)
11 (3)	Set the VW2C0 bit in the VW2C register to 1 (voltage monitor 2 interrupt enabled).	

Notes:
1. When the VW2C0 bit is set to 0, steps 3 and 4 can be executed simultaneously (with one instruction).
2. When the VW2C0 bit is set to 0, steps 5 and 6 can be executed simultaneously (with one instruction).
3. When the voltage detection 2 circuit is enabled while the voltage monitor 2 interrupt is disabled, low voltage is detected and the VW2C2 bit becomes 1.
   When low voltage is detected after the voltage detection 2 circuit is enabled until an interrupt is enabled for the setting procedure of bits associated with voltage monitor 2 interrupt, an interrupt is not generated. After an interrupt is enabled, read the VW2C2 bit. When the bit is read as 1, perform the process that occurs when low voltage is detected.



VCA13: Bit in VCA1 register
VW2C1, VW2C2, VW2C7: Bits in VW2C register
VCAC2: Bit in VCAC register

The above applies when:
- VCA27 bit in VCA2 register = 1 (voltage detection 2 circuit enabled)
- VW2C0 bit in VW2C register = 1 (voltage monitor 2 interrupt enabled)

Note:
1. If voltage monitor 0 reset is not used, set the power supply to VCC ≥ 1.8 V.

Figure 6.7 Operating Example of Voltage Monitor 2 Interrupt

7. I/O Ports

There are 20 I/O ports P0_0 to P0_2, P1, P3_0, P3_1, P3_3 to P3_5, P3_7, and P4_5 to P4_7 (P4_6 and P4_7 can be used as I/O ports if the XIN clock oscillation circuit is not used).
Table 7.1 lists an Overview of I/O Ports.

Table 7.1 Overview of I/O Ports

Ports	I/O	Type of Output	I/O Setting	Internal Pull-Up Resister	Drive Capacity Switch	Input Level Switch
P0_0 to P0_2	I/O	CMOS3 state	Set in 1-bit units	Set in 3-bit units (1)	Set in 3-bit units (3)	Set in 3-bit units (4)
P1	I/O	CMOS3 state	Set in 1-bit units	Set in 4-bit units (1)	Set in 1-bit units (2)	Set in 8-bit units (4)
P3_0, P3_1, P3_3 to P3_5, P3_7	I/O	CMOS3 state	Set in 1-bit units	Set in 3-bit units (1)	Set in 3-bit units (3)	Set in 6-bit units (4)
P4_5, P4_6 (5), P4_7 (5)	I/O	CMOS3 state	Set in 1-bit units	Set in 3-bit units (1)	Set in 3-bit units (3)	Set in 3-bit units (4)

Notes:
1. In input mode, whether an internal pull-up resistor is connected or not can be selected by registers PUR0 and PUR1.
2. Whether the drive capacity of the output transistor is set to low or high can be selected using registers P1DRR.
3. Whether the drive capacity of the output transistor is set to low or high can be selected using registers DRR0 and DRR1.
4. The input threshold value can be selected among three voltage levels (0.35 VCC, 0.50 VCC, and 0.70 VCC) using registers VLT0 and VLT1.
5. When the XIN clock oscillation circuit is not used, these ports can be used as I/O ports.

7.1 Functions of I/O Ports

The PDi_j (j = 0 to 7) bit in the PDi (i = 0, 1, 3, 4) register controls I/O of the ports P0_0 to P0_2, P1, P3_0, P3_1, P3_3 to P3_5, P3_7, and P4_5 to P4_7. The Pi register consists of a port latch to hold output data and a circuit to read pin states.
Figures 7.1 to 7.6 show the Configurations of I/O Ports. Table 7.2 lists the Functions of I/O Ports.

Table 7.2 Functions of I/O Ports

Operation When Accessing Pi Register	Value of PDi_j Bit in PDi Register (1)	
	When PDi_j Bit is Set to 0 (Input Mode)	When PDi_j Bit is Set to 1 (Output Mode)
Read	Read the pin input level.	Read the port latch.
Write	Write to the port latch.	Write to the port latch. The value written to the port latch is output from the pin.

i = 0, 1, 3, 4, j = 0 to 7
Note:
1. Nothing is assigned to bits PD0_3 to PD0_7, PD3_2, PD3_6, PD4_0 to PD4_4.

7.2 Effect on Peripheral Functions

I/O ports function as I/O ports for peripheral functions (refer to **Table 1.4 Pin Name Information by Pin Number**).

Table 7.3 lists the Setting of PDi_j Bit when Functioning as I/O Ports for Peripheral Functions (i = 0, 1, 3, 4, j = 0 to 7).

Refer to the description of each function for information on how to set peripheral functions.

Table 7.3 Setting of PDi_j Bit when Functioning as I/O Ports for Peripheral Functions (i = 0, 1, 3, 4, j = 0 to 7)

I/O of Peripheral Function	PDi_j Bit Settings for Shared Pin Function
Input	Set this bit to 0 (input mode).
Output	This bit can be set to either 0 or 1 (output regardless of the port setting).

7.3 Pins Other than I/O Ports

Figure 7.7 shows the Configuration of I/O Pins.

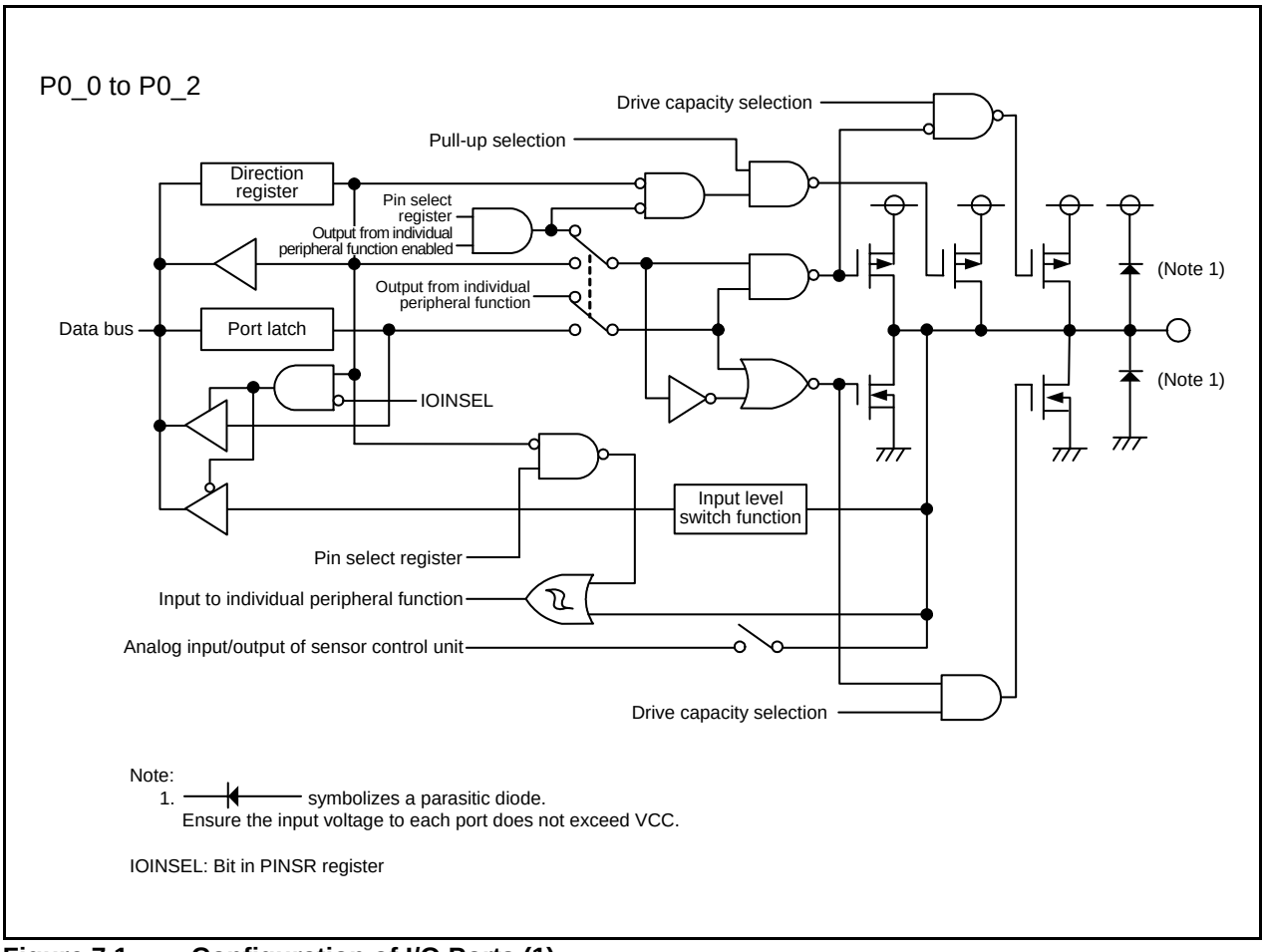
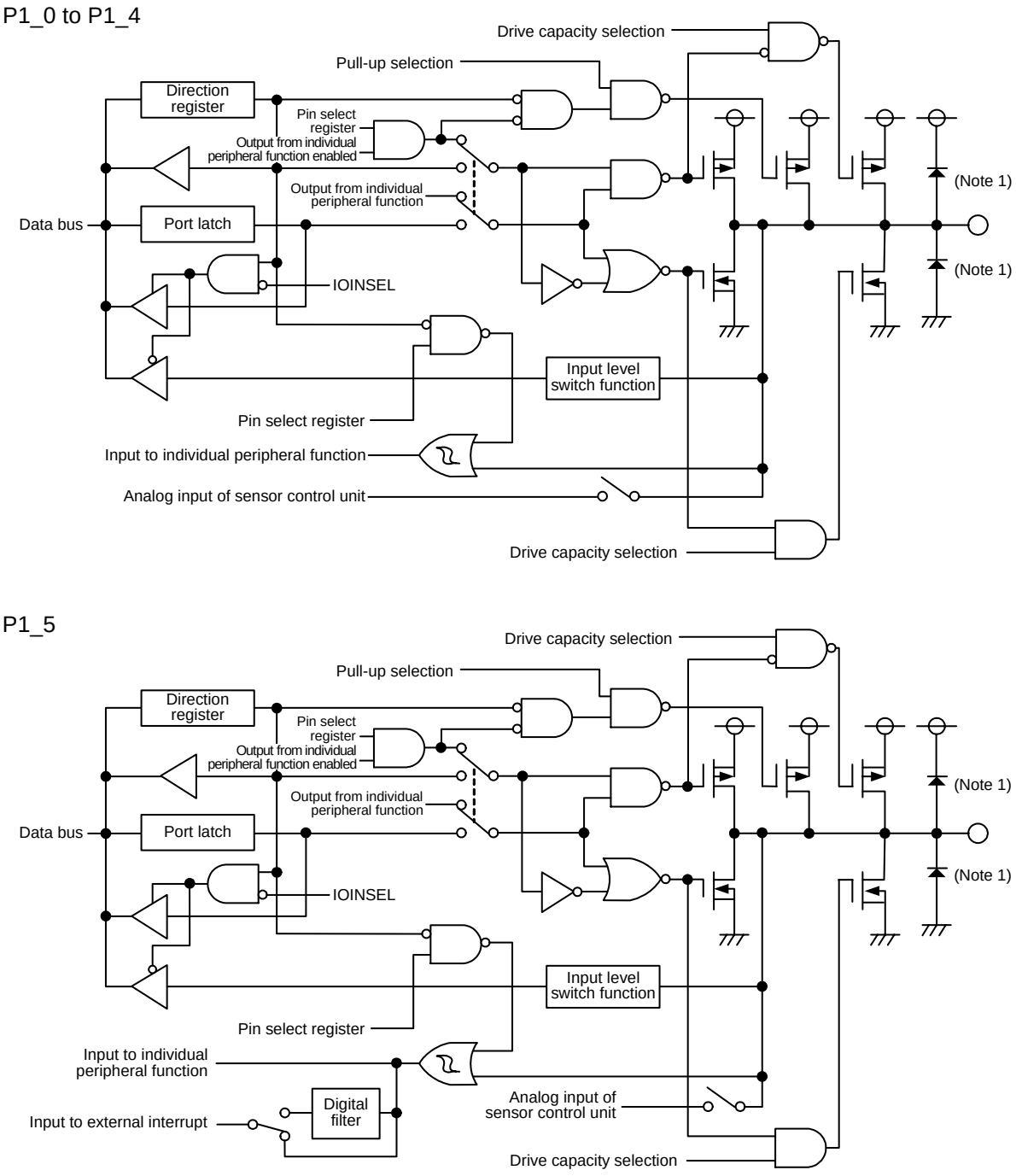


Figure 7.1 Configuration of I/O Ports (1)



Note:
1. ⟵| symbolizes a parasitic diode.
Ensure the input voltage to each port does not exceed VCC.

IOINSEL: Bit in PINSR register

Figure 7.2 Configuration of I/O Ports (2)

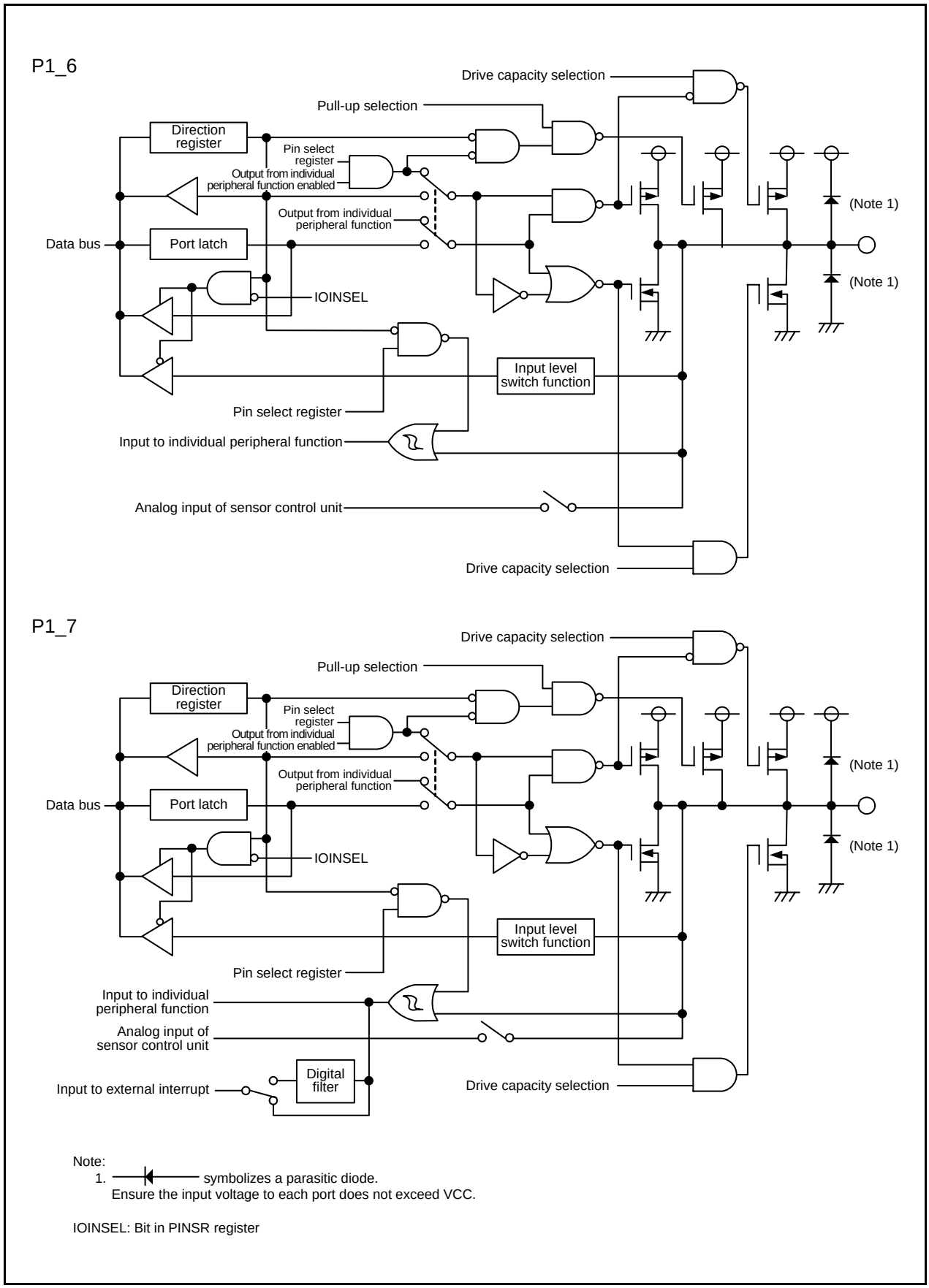


Figure 7.3 Configuration of I/O Ports (3)

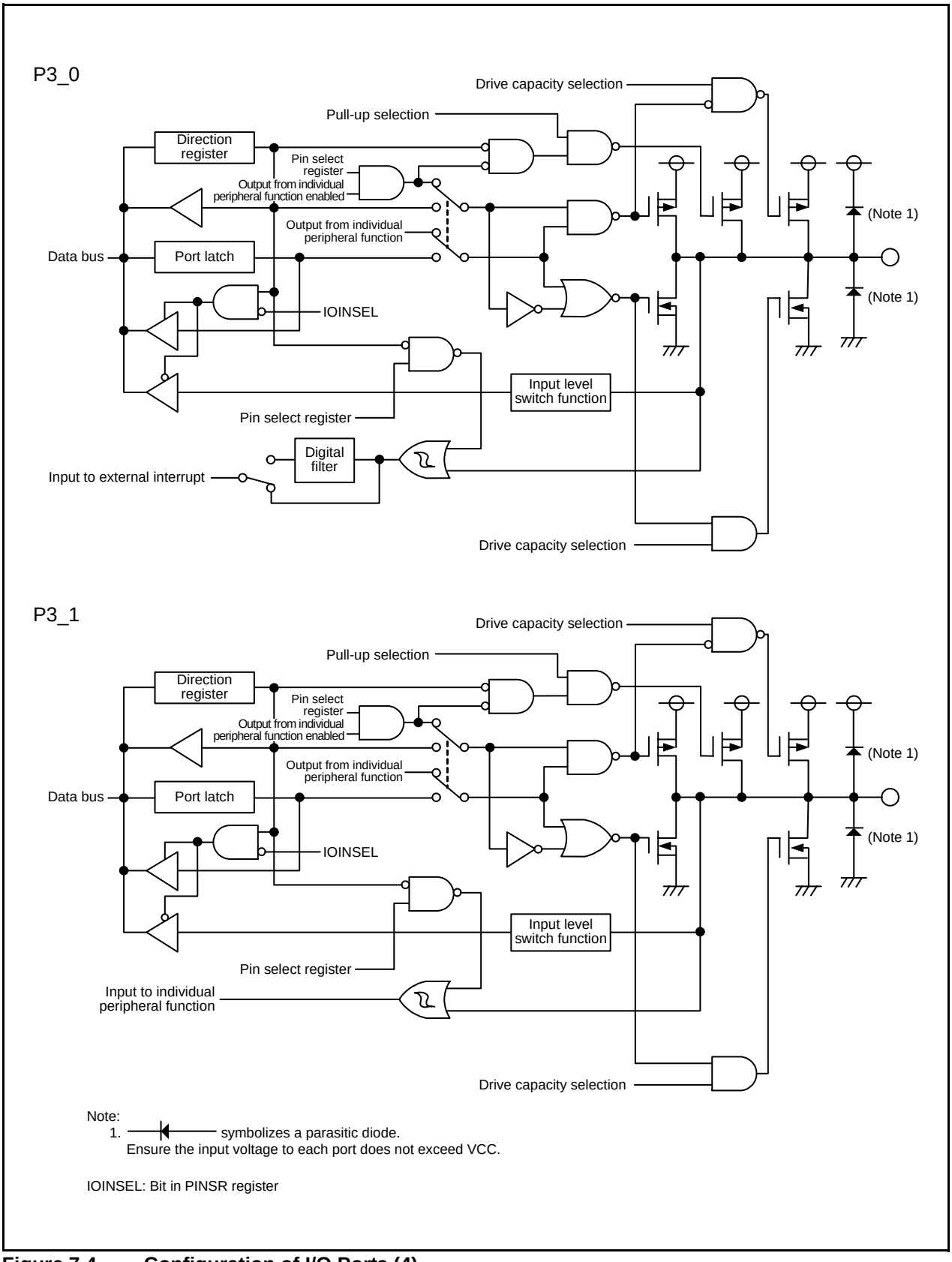
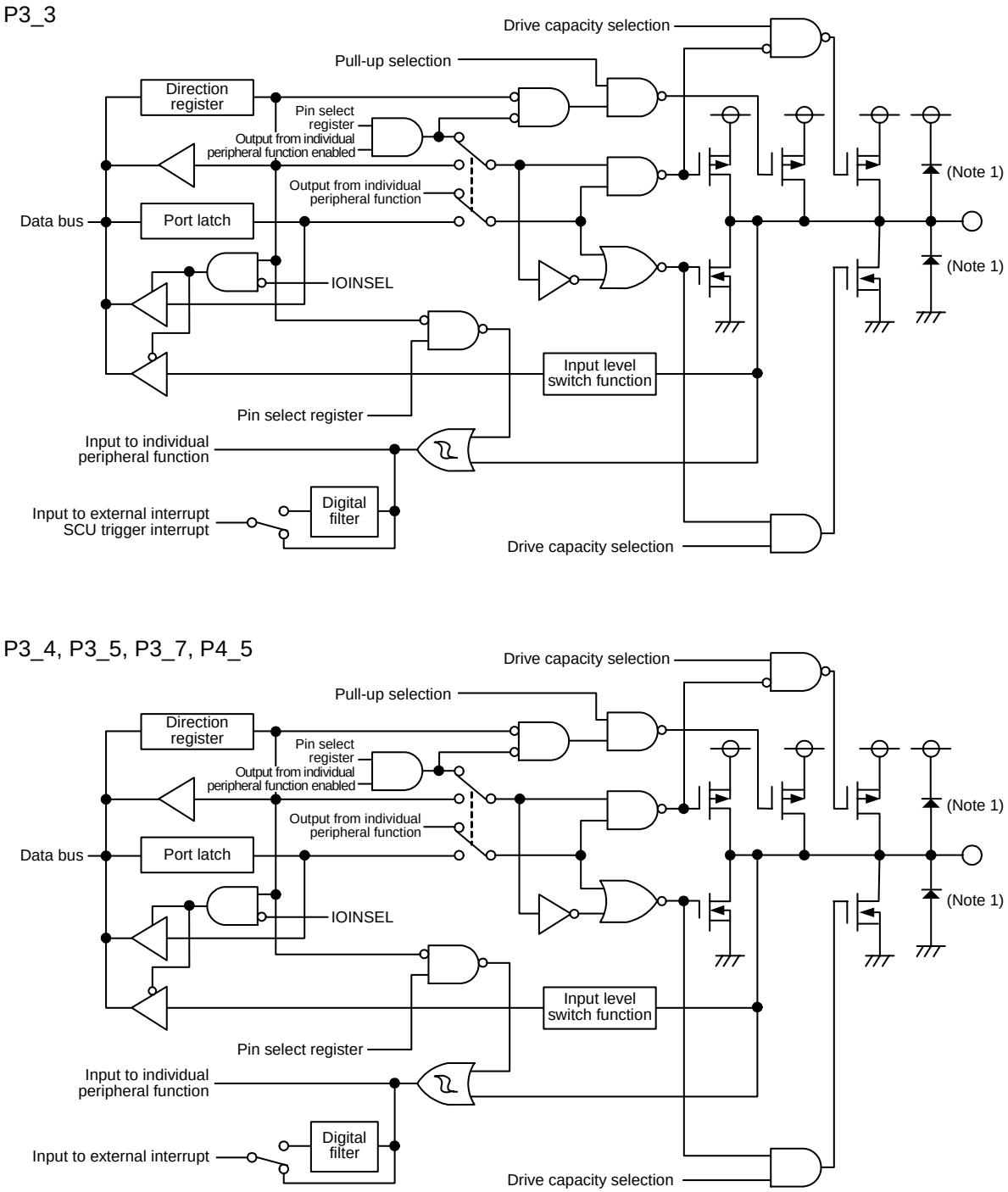


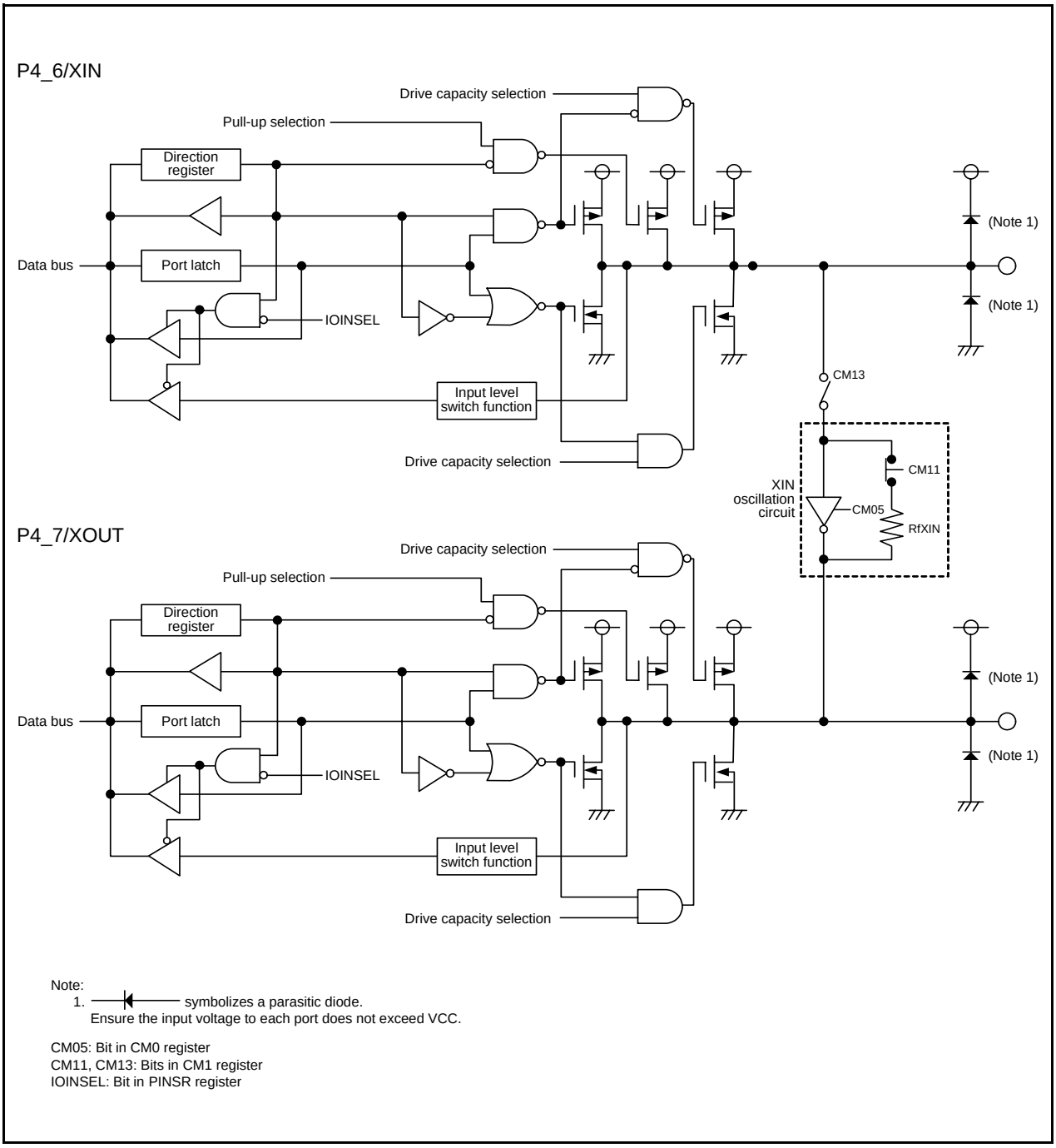
Figure 7.4 Configuration of I/O Ports (4)



Note:
1. ⟵ symbolizes a parasitic diode.
Ensure the input voltage to each port does not exceed VCC.

IOINSEL: Bit in PINSR register

Figure 7.5 Configuration of I/O Ports (5)



Note:
1. ——|◄—— symbolizes a parasitic diode.
Ensure the input voltage to each port does not exceed VCC.

CM05: Bit in CM0 register
CM11, CM13: Bits in CM1 register
IOINSEL: Bit in PINSR register

Figure 7.6 Configuration of I/O Ports (6)

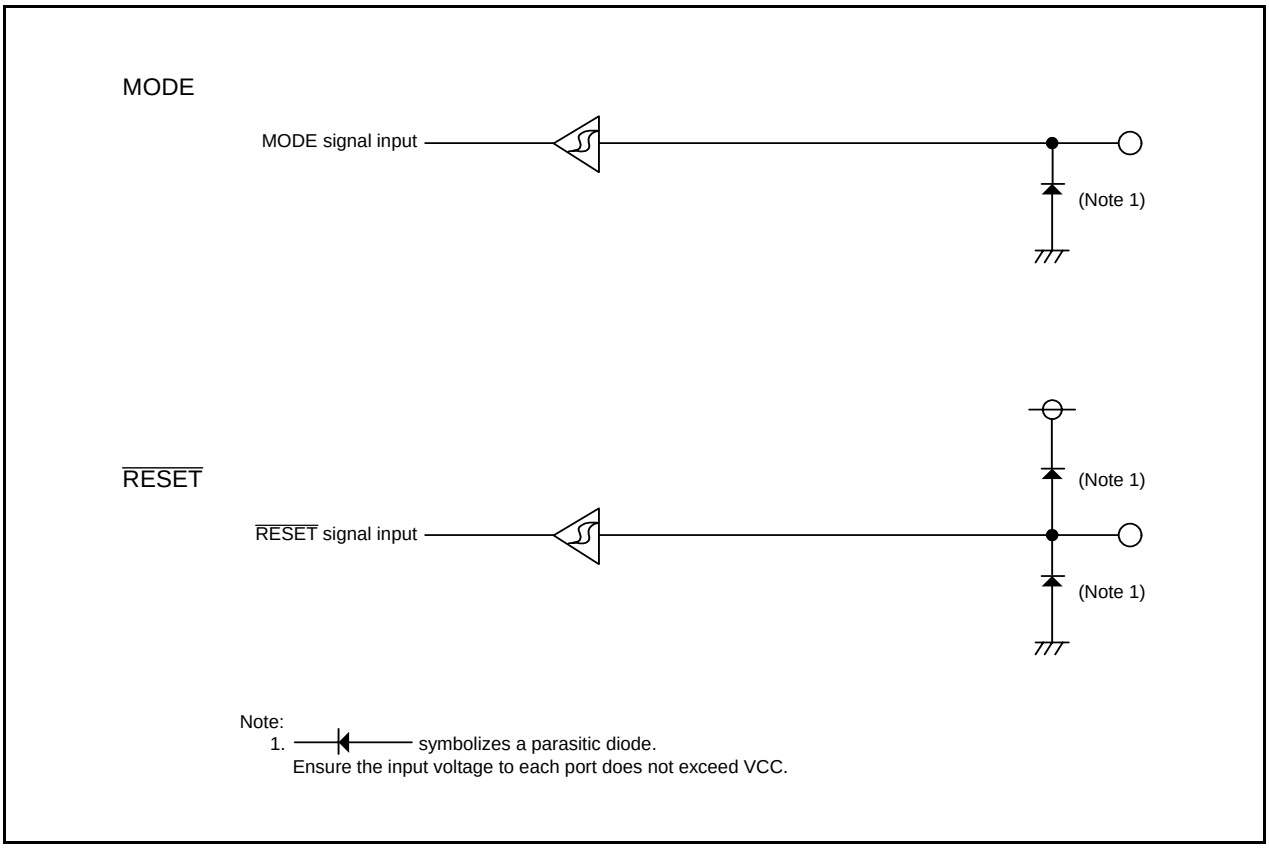


Figure 7.7 Configuration of I/O Pins

7.4 Registers

7.4.1 Port Pi Direction Register (PDi) (i = 0, 1, 3, 4)

Address 00E2h (PD0 (1)), 00E3h (PD1), 00E7h (PD3 (2)), 00EAh (PD4 (3))

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	PDi_7	PDi_6	PDi_5	PDi_4	PDi_3	PDi_2	PDi_1	PDi_0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	PDi_0	Port Pi_0 direction bit	0: Input mode (functions as an input port) 1: Output mode (functions as an output port)	R/W
b1	PDi_1	Port Pi_1 direction bit		R/W
b2	PDi_2	Port Pi_2 direction bit		R/W
b3	PDi_3	Port Pi_3 direction bit		R/W
b4	PDi_4	Port Pi_4 direction bit		R/W
b5	PDi_5	Port Pi_5 direction bit		R/W
b6	PDi_6	Port Pi_6 direction bit		R/W
b7	PDi_7	Port Pi_7 direction bit		R/W

Notes:
1. Write to the PD0 register with the next instruction after that used to set the PRC2 bit in the PRCR register to 1 (write enabled).
2. Bits PD3_2, and PD3_6 in the PD3 register are reserved bits. If it is necessary to set bits PD3_2 and PD3_6, set to 0. When read, the content is 0.
3. Bits PD4_0 to PD4_2 in the PD4 register are unavailable on this MCU. If it is necessary to set bits PD4_0 to PD4_2 set to 0. When read, the content is 0. Bits PD4_3 and PD4_4 are reserved bits. If it is necessary to set bits PD4_3 and PD4_4, set to 0. When read, the content is 0.

The PDi register selects whether I/O ports are used for input or output. Each bit in the PDi register corresponds to one port.

7.4.2 Port Pi Register (Pi) (i = 0, 1, 3, 4)

Address 00E0h (P0), 00E1h (P1), 00E5h (P3 (1)), 00E8h (P4 (2))

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	Pi_7	Pi_6	Pi_5	Pi_4	Pi_3	Pi_2	Pi_1	Pi_0
After Reset	X	X	X	X	X	X	X	X

Bit	Symbol	Bit Name	Function	R/W
b0	Pi_0	Port Pi_0 bit	0: “L” level 1: “H” level	R/W
b1	Pi_1	Port Pi_1 bit		R/W
b2	Pi_2	Port Pi_2 bit		R/W
b3	Pi_3	Port Pi_3 bit		R/W
b4	Pi_4	Port Pi_4 bit		R/W
b5	Pi_5	Port Pi_5 bit		R/W
b6	Pi_6	Port Pi_6 bit		R/W
b7	Pi_7	Port Pi_7 bit		R/W

Notes:
1. Bits P3_2, and P3_6 in the P3 register are reserved bits. If it is necessary to set bits P3_2 and P3_6, set to 0. When read, the content is 0.
2. Bits P4_0 to P4_1 in the P4 register are unavailable on this MCU. If it is necessary to set bits P4_0 to P4_1 set to 0. When read, the content is 0. Bits P4_3 and P4_4 are reserved bits. If it is necessary to set bits P4_3 and P4_4, set to 0. When read, the content is 0.

Data input and output to and from external devices are accomplished by reading and writing to the Pi register. The Pi register consists of a port latch to retain output data and a circuit to read the pin status. The value written in the port latch is output from the pin. Each bit in the Pi register corresponds to one port.

Pi_j Bit (i = 0, 1, 3, 4, j = 0 to 7) (Port Pi_j Bit)

The pin level of any I/O port which is set to input mode can be read by reading the corresponding bit in this register. The pin level of any I/O port which is set to output mode can be controlled by writing to the corresponding bit in this register.

7.4.3 Timer RA Pin Select Register (TRASR)

Address 0180h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	TRAOSEL0	TRAIOSEL2	TRAIOSEL1	TRAIOSEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TRAIOSEL0	TRAIO pin select bit	b2 b1 b0 0 0 0: TRAIO pin not used 0 0 1: P1_7 assigned 0 1 0: P1_5 assigned 1 0 1: P3_5 assigned Other than above: Do not set. (TRAIO pin not used.)	R/W
b1	TRAIOSEL1			R/W
b2	TRAIOSEL2			R/W
b3	TRAOSEL0	TRAO pin select bit	0: P3_7 assigned 1: P3_0 assigned	R/W
b4	—	Reserved bit	Set to 0.	R/W
b5	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b6	—			
b7	—			

The TRASR register selects which pin is assigned to the timer RA I/O. To use the I/O pin for timer RA, set this register.
Set the TRASR register before setting the timer RA associated registers. Also, do not change the setting value in this register during timer RA operation.
Change the TRASR register from the initial value to any value during the initial setting of the user's program. Do not change this register again while the main program is executed.

7.4.4 Timer RB/RC Pin Select Register (TRBRCSR)

Address 0181h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	TRCCLKSEL1	TRCCLKSEL0	—	TRBOSEL2	TRBOSEL1	TRBOSEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TRBOSEL0	TRBO pin select bit	b2 b1 b0 0 0 0: P1_3 assigned 0 0 1: P3_1 assigned 0 1 0: Do not set. (TRBO pin not used) 0 1 1: P3_3 assigned Other than above: Do not set. (TRBO pin not used.)	R/W
b1	TRBOSEL1			R/W
b2	TRBOSEL2			R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	TRCCLKSEL0	TRCCLK pin select bit	b5 b4 0 0: TRCCLK pin not used 0 1: P1_4 assigned 1 0: P3_3 assigned 1 1: P3_7 assigned	R/W
b5	TRCCLKSEL1			R/W
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b7	—			—

The TRBRCSR register selects which pin is assigned to the timer RB and timer RC I/O. To use the I/O pin for timer RB and timer RC, set this register.

Set the TRBOSEL0 bit before setting the timer RB associated registers. Set bits TRCCLKSEL0 and TRCCLKSEL1 before setting the timer RC associated registers. Also, do not change the setting values of the TRBOSEL0 bit during timer RB operation. Do not change the setting values of bits TRCCLKSEL0 and TRCCLKSEL1 during timer RC operation.

Change the TRBRCSR register from the initial value to any value during the initial setting of the user's program. Do not change this register again while the main program is executed.

7.4.5 Timer RC Pin Select Register 0 (TRCPSR0)

Address 0182h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TRCIOBSEL3	TRCIOBSEL2	TRCIOBSEL1	TRCIOBSEL0	—	TRCIOASEL2	TRCIOASEL1	TRCIOASEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TRCIOASEL0	TRCIOA/TRCTRG pin select bit	b2 b1 b0 0 0 0: TRCIOA/TRCTRG pin not used 0 0 1: P1_1 assigned 0 1 0: P0_0 assigned 0 1 1: P0_1 assigned 1 0 0: P0_2 assigned 1 0 1: Do not set. (TRCIOA/TRCTRG pin not used.) 1 1 0: P3_1 assigned Other than above: Do not set. (TRCIOA pin not used.)	R/W
b1	TRCIOASEL1			R/W
b2	TRCIOASEL2			R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	TRCIOBSEL0	TRCIOB pin select bit	b7 b6 b5 b4 0 0 0 0: TRCIOB pin not used 0 0 0 1: P1_2 assigned 1 0 0 1: P4_5 assigned Other than above: Do not set. (TRCIOB pin not used.)	R/W
b5	TRCIOBSEL1			R/W
b6	TRCIOBSEL2			R/W
b7	TRCIOBSEL3			R/W

The TRCPSR0 register selects which pin is assigned to the timer RC I/O. To use the I/O pin for timer RC, set this register.
Set the TRCPSR0 register before setting the timer RC associated registers. Also, do not change the setting value in this register during timer RC operation.
Change the TRCPSR0 register from the initial value to any value during the initial setting of the user's program. Do not change this register again while the main program is executed.

7.4.6 Timer RC Pin Select Register 1 (TRCPSR1)

Address 0183h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	TRCIODSEL2	TRCIODSEL1	TRCIODSEL0	—	TRCIOCSEL2	TRCIOCSEL1	TRCIOCSEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TRCIOCSEL0	TRCIOC pin select bit	b2 b1 b0 0 0 0: TRCIOC pin not used 0 0 1: P1_3 assigned 0 1 0: P3_4 assigned Other than above: Do not set. (TRCIOC pin not used.)	R/W
b1	TRCIOCSEL1			R/W
b2	TRCIOCSEL2			R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	TRCIODSEL0	TRCIOD pin select bit	b6 b5 b4 0 0 0: TRCIOD pin not used 0 0 1: P1_0 assigned 0 1 0: P3_5 assigned Other than above: Do not set. (TRCIOD pin not used.)	R/W
b5	TRCIODSEL1			R/W
b6	TRCIODSEL2			R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

The TRCPSR1 register selects which pin is assigned to the timer RC I/O. To use the I/O pin for timer RC, set this register.
Set the TRCPSR1 register before setting the timer RC associated registers. Also, do not change the setting value in this register during timer RC operation.
Change the TRCPSR1 register from the initial value to any value during the initial setting of the user's program. Do not change this register again while the main program is executed.

7.4.7 UART0 Pin Select Register (U0SR)

Address 0188h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	CLK0SEL1	CLK0SEL0	RXD0SEL1	RXD0SEL0	TXD0SEL1	TXD0SEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TXD0SEL0	TXD0 pin select bit	b1 b0 0 0: TXD0 pin not used 0 1: P1_4 assigned 1 0: P3_4 assigned 1 1: Do not set. (TXD0 pin not used.)	R/W
b1	TXD0SEL1			R/W
b2	RXD0SEL0	RXD0 pin select bit	b3 b2 0 0: RXD0 pin not used 0 1: P1_5 assigned 1 0: P3_5 assigned 1 1: Do not set. (RXD0 pin not used.)	R/W
b3	RXD0SEL1			R/W
b4	CLK0SEL0	CLK0 pin select bit	b5 b4 0 0: CLK0 pin not used 0 1: P1_6 assigned 1 0: P3_7 assigned 1 1: Do not set. (CLK0 pin not used.)	R/W
b5	CLK0SEL1			R/W
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b7	—			—

The U0SR register selects which pin is assigned to the UART0 I/O. To use the I/O pin for UART0, set this register.
Set the U0SR register before setting the UART0 associated registers. Also, do not change the setting value in this register during UART0 operation.
Change the U0SR register from the initial value to any value during the initial setting of the user's program. Do not change this register again while the main program is executed.

7.4.8 INT Interrupt Input Pin Select Register (INTSR)

Address 018Eh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	INT3SEL0	—	INT2SEL0	INT1SEL2	INT1SEL1	INT1SEL0	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b1	INT1SEL0	$\overline{\text{INT1}}$ pin select bit	b3 b2 b1 0 0 0: P1_7 assigned 0 0 1: P1_5 assigned 1 0 1: P3_5 assigned Other than above: Do not set. ($\overline{\text{INT1}}$ pin not used.)	R/W
b2	INT1SEL1			R/W
b3	INT1SEL2			R/W
b4	INT2SEL0	$\overline{\text{INT2}}$ pin select bit	0: P3_4 assigned 1: P3_0 assigned	R/W
b5	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b6	INT3SEL0	$\overline{\text{INT3}}$ pin select bit	0: P3_3 assigned 1: P3_7 assigned	R/W
b7	—	Reserved bit	Set to 0.	R/W

The INTSR register selects which pin is assigned to the $\overline{\text{INTi}}$ (i = 1 to 3) input. To use $\overline{\text{INTi}}$, set this register. Set the INTSR register before setting the $\overline{\text{INTi}}$ associated registers. Also, do not change the setting values in this register during $\overline{\text{INTi}}$ operation.

7.4.9 I/O Function Pin Select Register (PINSR)

Address 018Fh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	IOINSEL	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b1	—	Reserved bit	Set to 0.	R/W
b2	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b3	IOINSEL	I/O port input function select bit	0: The I/O port input function depends on the PDi (i = 0, 1, 3, 4) register. When the PDi_j (j = 0 to 7) bit in the PDi register is set to 0 (input mode), the pin input level is read. When the PDi_j bit in the PDi register is set to 1 (output mode), the port latch is read. 1: The I/O port input function reads the pin input level regardless of the PDi register.	R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b5	—			
b6	—			
b7	—			

IOINSEL Bit (I/O port input function select bit)

The IOINSEL bit is used to select the pin level of an I/O port when the PDi_j (j = 0 to 7) bit in the PDi (i = 0, 1, 3, 4) register is set to 1 (output mode). When this bit is set to 1, the I/O port input function reads the pin input level regardless of the PDi register.

Table 7.4 lists I/O Port Values Read by Using IOINSEL Bit. The input function of all I/O ports can be changed.

Table 7.4 I/O Port Values Read by Using IOINSEL Bit

PDi_j bit in PDi register	0 (input mode)		1 (output mode)	
IOINSEL bit	0	1	0	1
I/O port values read	Pin input level		Port latch value	Pin input level

7.4.10 Low-Voltage Signal Mode Control Register (TSMR)

Address 0190h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	I3LVM	I2LVM	I1LVM	I0LVM	—	—	U0LVM	LVMPR
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	LVMPR	Low-voltage signal mode protect bit	0: Write disabled 1: Write enabled (1)	R/W
b1	U0LVM	UART0 low-voltage signal mode control bit (1)	0: Low-voltage signal mode disabled 1: Low-voltage signal mode enabled (2)	R/W
b2	—	Reserved bits	Set to 0.	R/W
b3	—			R/W
b4	I0LVM	$\overline{\text{INT0}}$ low-voltage signal mode control bit (1)	0: Low-voltage signal mode disabled 1: Low-voltage signal mode enabled	R/W
b5	I1LVM	$\overline{\text{INT1}}$ low-voltage signal mode control bit (1)		R/W
b6	I2LVM	$\overline{\text{INT2}}$ low-voltage signal mode control bit (1)		R/W
b7	I3LVM	$\overline{\text{INT3}}$ low-voltage signal mode control bit (1)		R/W

Notes:
1. When the LVMPR bit is set to 1 (write enabled), writing to bits U0LVM and IjLVM (j = 0 to 3) is enabled. Rewrite bits U0LVM and IjLVM (j = 0 to 3) after setting the LVMPR bit to 1. When writing 1 to the LVMPR bit, write 0 and then 1 continuously.
2. When the U0LVM bit is set to 1, the TxD0 pin is set to N-channel open-drain output regardless of the setting of the NCH bit in the U0C0 register.

7.4.11 Pull-Up Control Register 0 (PUR0)

Address 01E0h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	PU07	PU06	—	—	PU03	PU02	—	PU00
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	PU00	P0_0 to P0_2 pull-up	0: Not pulled up 1: Pulled up (1)	R/W
b1	—	Reserved bit	Set to 0.	R/W
b2	PU02	P1_0 to P1_3 pull-up	0: Not pulled up	R/W
b3	PU03	P1_4 to P1_7 pull-up	1: Pulled up (1)	R/W
b4	—	Reserved bits	Set to 0.	R/W
b5	—			R/W
b6	PU06	P3_1, P3_3 pull-up	0: Not pulled up	R/W
b7	PU07	P3_4, P3_5, P3_7 pull-up	1: Pulled up (1)	R/W

Note:
1. When this bit is set to 1 (pulled up), the pin whose port direction bit is set to 0 (input mode) is pulled up.

   For ports set as output of I/O pins for the peripheral functions, the setting values in the PUR0 register are invalid and no pull-up resistor is connected.

7.4.12 Pull-Up Control Register 1 (PUR1)

Address 01E1h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	PU11	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is undefined.		—
b1	PU11	P4_5 to P4_7 pull-up	0: Not pulled up 1: Pulled up (1)	R/W
b2	—	Nothing is assigned. If necessary, set to 0. When read, the content is undefined.		—
b3	—			
b4	—			
b5	—			
b6	—			
b7	—			

Note:
1. When this bit is set to 1 (pulled up), the pin whose port direction bit is set to 0 (input mode) is pulled up.

   For ports set as output of I/O pins for the peripheral functions, the setting values in the PUR1 register are invalid and no pull-up resistor is connected.

7.4.13 Port P1 Drive Capacity Control Register (P1DRR)

Address 01F0h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	P1DRR7	P1DRR6	P1DRR5	P1DRR4	P1DRR3	P1DRR2	P1DRR1	P1DRR0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	P1DRR0	P1_0 drive capacity	0: Low	R/W
b1	P1DRR1	P1_1 drive capacity	1: High (1)	R/W
b2	P1DRR2	P1_2 drive capacity		R/W
b3	P1DRR3	P1_3 drive capacity		R/W
b4	P1DRR4	P1_4 drive capacity		R/W
b5	P1DRR5	P1_5 drive capacity		R/W
b6	P1DRR6	P1_6 drive capacity		R/W
b7	P1DRR7	P1_7 drive capacity		R/W

Note:
1. Both “H” and “L” output are set to high drive capacity.

The P1DRR register selects whether the drive capacity of the P1 output transistor is set to low or high. The P1DRRi bit (i = 0 to 7) is used to select whether the drive capacity of the output transistor is set to low or high for each pin.

7.4.14 Drive Capacity Control Register 0 (DRR0)

Address 01F2h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	DRR07	DRR06	—	—	—	—	—	DRR00
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	DRR00	P0_0 to P0_2 drive capacity	0: Low 1: High (1)	R/W
b1	—	Reserved bit	Set to 0.	R/W
b2	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b3	—			
b4	—			
b5	—			
b6	DRR06	P3_1, P3_3 drive capacity	0: Low 1: High (1)	R/W
b7	DRR07	P3_4, P3_5, P3_7 drive capacity		R/W

Note:
1. Both “H” and “L” output are set to high drive capacity.

DRR00 Bit (P0_0 to P0_2 drive capacity)

The DRR00 bit selects whether the drive capacity of the P0_0 to P0_2 output transistors is set to low or high. This bit is used to select whether the drive capacity of the output transistors is set to low or high for three pins.

DRR06 Bit (P3_1, P3_3 drive capacity)

The DRR06 bit selects whether the drive capacity of the P3_1, P3_3 output transistors is set to low or high. This bit is used to select whether the drive capacity of the output transistors is set to low or high for two pins.

DRR07 Bit (P3_4, P3_5, P3_7 drive capacity)

The DRR07 bit selects whether the drive capacity of the P3_4, P3_5, P3_7 output transistors is set to low or high. This bit is used to select whether the drive capacity of the output transistors is set to low or high for three pins.

7.4.15 Drive Capacity Control Register 1 (DRR1)

Address 01F3h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	DRR11	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is undefined.		—
b1	DRR11	P4_5 to P4_7 drive capacity	0: Low 1: High (1)	R/W
b2	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b3	—			
b4	—			
b5	—			
b6	—			
b7	—			

Note:
1. Both “H” and “L” output are set to high drive capacity.

DRR11 Bit (P4_5 to P4_7 drive capacity)

The DRR11 bit selects whether the drive capacity of the P4_5 to P4_7 output transistors is set to low or high. This bit is used to select whether the drive capacity of the output transistors is set to low or high for three pins.

7.4.16 Input Threshold Control Register 0 (VLT0)

Address 01F5h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	VLT07	VLT06	—	—	VLT03	VLT02	VLT01	VLT00
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	VLT00	P0 input level select bit	b1 b0 0 0: 0.50 × VCC 0 1: 0.35 × VCC 1 0: 0.70 × VCC 1 1: Do not set.	R/W
b1	VLT01			R/W
b2	VLT02	P1 input level select bit	b3 b2 0 0: 0.50 × VCC 0 1: 0.35 × VCC 1 0: 0.70 × VCC 1 1: Do not set.	R/W
b3	VLT03			R/W
b4	—	Reserved bits	Set to 0.	R/W
b5	—			R/W
b6	VLT06	P3_1, P3_3 to P3_5, P3_7 input level select bit	b7 b6 0 0: 0.50 × VCC 0 1: 0.35 × VCC 1 0: 0.70 × VCC 1 1: Do not set.	R/W
b7	VLT07			R/W

The VLT0 register selects the voltage level of the input threshold values for ports P0, P1, and P3. Bits VLT00 to VLT03, VLT06, and VLT07 are used to select the input threshold values among three voltage levels (0.35 VCC, 0.50 VCC, and 0.70 VCC).

7.4.17 Input Threshold Control Register 1 (VLT1)

Address 01F6h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	VLT11	VLT10
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	VLT10	P4_5 to P4_7 input level select bit	b1 b0 0 0: 0.50 × VCC 0 1: 0.35 × VCC 1 0: 0.70 × VCC 1 1: Do not set.	R/W
b1	VLT11			R/W
b2	—	Nothing is assigned. If necessary, set to 0. When read, the content is undefined.		—
b3	—			—
b4	—			—
b5	—			—
b6	—			—
b7	—			—

The VLT1 register selects the voltage level of the input threshold values for ports P4_5 to P4_7. Bits VLT10 and VLT11 are used to select the input threshold values among three voltage levels (0.35 VCC, 0.50 VCC, and 0.70 VCC).

7.5 Port Settings

Tables 7.5 to 7.24 list the port settings.

Table 7.5 Port P0_0/CHxC/TRCIOA/TRCTRG

Register	PD0	SCUCR0		TRCPSR0			Timer RC Setting	Function
Bit	PD0_0	SCUE	BCSHORT	TRCIOASEL			—	
				2	1	0		
Setting Value	0	0	X	Other than 010b			X	Input port (1)
	1	0	X	Other than 010b			X	Output port (2)
	X	1	1	X	X	X	X	CHxC input, CHxC forced “H” output (2, 3, 4)
	X	1	0	X	X	X	X	CHxC forced “H” output (2, 3)
	0	0	X	0	1	0	Refer to **Table 7.26 TRCIOA Pin Setting**	TRCIOA input (1)
	X	0	X	0	1	0	Refer to **Table 7.26 TRCIOA Pin Setting**	TRCIOA output (2)

X: 0 or 1

Notes:
1. Pulled up by setting the PU00 bit in the PUR0 register to 1.
2. Output drive capacity high by setting the DRR00 bit in the DRR0 register to 1.
3. After the sensor control unit operates, “H” is forcibly output from CHxC in Status 2.
4. After the sensor control unit operates, CHxC is set to input in Status 6 to 10 and 15 to 20.

Table 7.6 Port P0_1/CHxB/TRCIOA/TRCTRG

Register	PD0	SCUCR0		TRCPSR0			Timer RC Setting	Function
Bit	PD0_1	SCUE	BCSHORT	TRCIOASEL			—	
				2	1	0		
Setting Value	0	0	X	Other than 011b			X	Input port (1)
	1	0	X	Other than 011b			X	Output port (2)
	X	1	1	X	X	X	X	CHxB input, CHxB forced “L” output (2, 3, 4)
	X	1	0	X	X	X	X	CHxB forced “L” output (2, 3)
	0	0	X	0	1	1	Refer to **Table 7.26 TRCIOA Pin Setting**	TRCIOA input (1)
	X	0	X	0	1	1	Refer to **Table 7.26 TRCIOA Pin Setting**	TRCIOA output (2)

X: 0 or 1

Notes:
1. Pulled up by setting the PU00 bit in the PUR0 register to 1.
2. Output drive capacity high by setting the DRR00 bit in the DRR0 register to 1.
3. After the sensor control unit operates, “L” is forcibly output from CHxB in Status 5 and 14.
4. After the sensor control unit operates, CHxB is set to input in Status 6 to 10 and 15 to 20.

Table 7.7 Port P0_2/CHxA/TRCIOA/TRCTRG

Register	PD0	SCUCR0	TRCPSR0			Timer RC Setting	Function
Bit	PD0_2	SCUE	TRCIOASEL			—	
			2	1	0		
Setting Value	0	0	Other than 100b			X	Input port (1)
	1	0	Other than 100b			X	Output port (2)
	X	1	X	X	X	X	CHxA input, CHxA forced “L” output (2, 3)
	0	0	1	0	0	Refer to **Table 7.26 TRCIOA Pin Setting**	TRCIOA input (1)
	X	0	1	0	0	Refer to **Table 7.26 TRCIOA Pin Setting**	TRCIOA output (2)

X: 0 or 1

Notes:
1. Pulled up by setting the PU00 bit in the PUR0 register to 1.
2. Output drive capacity high by setting the DRR00 bit in the DRR0 register to 1.
3. After the sensor control unit operates, “L” is forcibly output from CHxA in Status 4, 5, 13, and 14.

Table 7.8 Port P1_0/$\overline{KI0}$/CH0/TRCIOD

Register	PD1	KIEN	SCUCR0	TSIER0	SCHCR					TRCPSR1			Timer RC Setting	Function
Bit	PD1_0	KI0EN	SCUE	CH00E	CHC					TRCIODSEL			—	
					4	3	2	1	0	2	1	0		
Setting Value	0	X	X	0	X	X	X	X	X	Other than 001b			X	Input port (1)
	1	X	X	0	X	X	X	X	X	Other than 001b			X	Output port (2)
	0	1	X	0	X	X	X	X	X	Other than 001b			X	$\overline{KI0}$ input (1)
	X	X	1	1	0	0	0	0	0	X	X	X	X	CH0 analog input
	X	X	1	1	Other than 00000b					X	X	X	X	CH0 forced “H” output (2)
	0	X	X	0	X	X	X	X	X	0	0	1	Refer to **Table 7.29 TRCIOD Pin Setting**	TRCIOD input (1)
	X	X	X	0	X	X	X	X	X	0	0	1	Refer to **Table 7.29 TRCIOD Pin Setting**	TRCIOD output (2)

X: 0 or 1

Notes:

1. Pulled up by setting the PU00 bit in the PUR0 register to 1.
2. Output drive capacity high by setting the P1DRR0 bit in the P1DRR register to 1.

Table 7.9 Port P1_1/$\overline{KI1}$/CH1/TRCIOA/TRCTRG

Register	PD1	KIEN	SCUCR0	TSIER0	SCHCR					TRCPSR0			Timer RC Setting	Function
Bit	PD1_1	KI1EN	SCUE	CH01E	CHC					TRCIOASEL			—	
					4	3	2	1	0	2	1	0		
Setting Value	0	X	X	0	X	X	X	X	X	Other than 001b			X	Input port (1)
	1	X	X	0	X	X	X	X	X	Other than 001b			X	Output port (2)
	0	1	X	0	X	X	X	X	X	Other than 001b			X	$\overline{KI1}$ input (1)
	X	X	1	1	0	0	0	0	1	X	X	X	X	CH1 analog input
	X	X	1	1	Other than 00001b					X	X	X	X	CH1 forced “H” output (2)
	0	X	X	0	X	X	X	X	X	0	0	1	Refer to **Table 7.26 TRCIOA Pin Setting**	TRCIOA input (1)
	X	X	X	0	X	X	X	X	X	0	0	1	Refer to **Table 7.26 TRCIOA Pin Setting**	TRCIOA output (2)

X: 0 or 1

Notes:

1. Pulled up by setting the PU02 bit in the PUR0 register to 1.
2. Output drive capacity high by setting the P1DRR1 bit in the P1DRR register to 1.

Table 7.10 Port P1_2/$\overline{KI2}$/CH2/TRCIOB

Register	PD1	KIEN	SCUCR0	TSIER0	SCHCR					TRCPSR0				Timer RC Setting	Function
Bit	PD1_2	KI2EN	SCUE	CH02E	CHC					TRCIOBSEL				—	
					4	3	2	1	0	3	2	1	0		
Setting Value	0	X	X	0	X	X	X	X	X	Other than 0001b				X	Input port (1)
	1	X	X	0	X	X	X	X	X	Other than 0001b				X	Output port (2)
	0	1	X	0	X	X	X	X	X	Other than 0001b				X	$\overline{KI2}$ input (1)
	X	X	1	1	0	0	0	1	0	X	X	X	X	X	CH2 analog input
	X	X	1	1	Other than 00010b					X	X	X	X	X	CH2 forced “H” output (2)
	0	X	X	0	X	X	X	X	X	0	0	0	1	Refer to **Table 7.27 TRCIOB Pin Setting**	TRCIOB input (1)
	X	X	X	0	X	X	X	X	X	0	0	0	1	Refer to **Table 7.27 TRCIOB Pin Setting**	TRCIOB output (2)

X: 0 or 1

Notes:
1. Pulled up by setting the PU02 bit in the PUR0 register to 1.
2. Output drive capacity high by setting the P1DRR2 bit in the P1DRR register to 1.

Table 7.11 Port P1_3/$\overline{KI3}$/CH3/TRBO/TRCIOC

Register	PD1	KIEN	SCUCR0	TSIER0	SCHCR					TRBRCSR			Timer RB Setting	TRCPSR1			Timer RC Setting	Function
Bit	PD1_3	KI3EN	SCUE	CH03E	CHC					TRBOSEL			—	TRCIOCSEL			—	
					4	3	2	1	0	2	1	0		2	1	0		
Setting Value	0	X	X	0	X	X	X	X	X	Other than 000b			X	Other than 001b			X	Input port (1)
										X	X	X	Other than TRBO usage conditions					
	1	X	X	0	X	X	X	X	X	Other than 000b			X	Other than 001b			X	Output port (2)
										X	X	X	Other than TRBO usage conditions					
	0	1	X	0	X	X	X	X	X	Other than 000b			X	Other than 001b			X	$\overline{KI3}$ input (1)
										X	X	X	Other than TRBO usage conditions					
	X	X	1	1	0	0	0	1	1	X	X	X	X	X	X	X	X	CH3 analog input
	X	X	1	1	Other than 00011b					X	X	X	X	X	X	X	X	CH3 forced “H” output (2)
	X	X	X	0	X	X	X	X	X	0	0	0	Refer to **Table 7.25 TRBO Pin Setting**	X	X	X	X	TRBO output (2)
	0	X	X	0	X	X	X	X	X	Other than 000b			X	0	0	1	Refer to **Table 7.28 TRCIOC Pin Setting**	TRCIOC input (1)
										X	X	X	Other than TRBO usage conditions					
	X	X	X	0	X	X	X	X	X	Other than 000b			X	0	0	1	Refer to **Table 7.28 TRCIOC Pin Setting**	TRCIOC output (2)
										X	X	X	Other than TRBO usage conditions					

X: 0 or 1

Notes:
1. Pulled up by setting the PU02 bit in the PUR0 register to 1.
2. Output drive capacity high by setting the P1DRR3 bit in the P1DRR register to 1.

Table 7.12 Port P1_4/CH4/TXD0/TRCCLK

Register	PD1	SCUCR0	TSIER0	SCHCR					TSMR	U0SR		U0MR			TRBRCSR		TRCCR1			Function
Bit	PD1_4	SCUE	CH04E	CHC					U0LVM	TXD0SEL		SMD			TRCCLKSEL		TCK			
				4	3	2	1	0		1	0	2	1	0	1	0	2	1	0	
Setting Value	0	X	0	X	X	X	X	X	X	Other than 01b		X	X	X	X	X	X	X	X	Input port (1)
	1	X	0	X	X	X	X	X	X	Other than 01b		X	X	X	X	X	X	X	X	Output port (2)
	X	1	1	0	0	1	0	0	X	Other than 01b		X	X	X	X	X	X	X	X	CH4 analog input
	X	1	1	Other than 00100b					X	Other than 01b		X	X	X	X	X	X	X	X	CH4 forced “H” output (2)
	X	X	0	X	X	X	X	X	0	0	1	0	0	1	X	X	X	X	X	TXD0 output (2, 3)
												1	0	0						
												1	0	1						
												1	1	0						
	X	X	0	X	X	X	X	X	1	0	1	0	0	1	X	X	X	X	X	TXD0 forced N-channel open-drain output
												1	0	0						
												1	0	1						
												1	1	0						
	0	X	0	X	X	X	X	X	X	Other than 01b		X	X	X	0	1	1	0	1	TRCCLK input (1)

X: 0 or 1

Notes:

1. Pulled up by setting the PU03 bit in the PUR0 register to 1.
2. Output drive capacity high by setting the P1DRR4 bit in the P1DRR register to 1.
3. N-channel open-drain output by setting the NCH bit in the U0C0 register to 1. However, when the U0LVM bit in the TSMR register is set to 1 (low-voltage signal mode enabled), the setting of the NCH bit is disabled. Refer to **7.6 Low-Voltage Signal Mode** for details.

Table 7.13 Port P1_5/CH5/RXD0/$\overline{\text{INT1}}$/TRAIO

Register	PD1	SCUCR0	TSIER0	SCHCR					TSMR		U0SR		TRASR			TRAIOC	TRAMR			INTSR			INTEN	Function
Bit	PD1_5	SCUE	CH05E	CHC					U0LVM	I1LVM	RXD0SEL		TRAIOSEL			TOPCR	TMOD			INT1SEL			INT1EN	
				4	3	2	1	0			1	0	2	1	0		2	1	0	2	1	0		
Setting Value	0	X	0	X	X	X	X	X	X	0	Other than 01b		Other than 010b			X	X	X	X	X	X	X	X	Input port (1)
	1	X	0	X	X	X	X	X	X	X	X	X	Other than 010b			X	X	X	X	X	X	X	X	Output port (2)
	X	1	1	0	0	1	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	CH5 analog input
	X	1	1	Other than 00101b					X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	CH5 forced “H” output (2)
	0	X	0	X	X	X	X	X	0	0	0	1	Other than 010b			X	X	X	X	X	X	X	X	RXD1 input (1)
	0	X	0	X	X	X	X	X	1	X	0	1	Other than 010b			X	X	X	X	X	X	X	X	RXD1 CMOS input (1, 3)
	0	X	0	X	X	X	X	X	X	0	Other than 01b		Other than 010b			X	X	X	X	0	0	1	1	$\overline{\text{INT1}}$ input (1)
	0	X	0	X	X	X	X	X	X	1	Other than 01b		Other than 010b			X	X	X	X	0	0	1	1	$\overline{\text{INT1}}$ CMOS input (1, 3)
	0	X	0	X	X	X	X	X	X	0	Other than 01b		0	1	0	0	Other than 000b, 001b			0	0	1	1	TRAIO input (1)
	X	X	0	X	X	X	X	X	X	X	X	X	0	1	0	0	0	0	1	X	X	X	X	TRAIO pulse output (2)

X: 0 or 1

Notes:

1. Pulled up by setting the PU03 bit in the PUR0 register to 1.
2. Output drive capacity high by setting the P1DRR5 bit in the P1DRR register to 1.
3. Schmitt input is switched to CMOS input.

Table 7.14 Port P1_6/CH6/CLK0

Register	PD1	SCUCR0	TSIER0	SCHCR					TSMR	U0SR		U0MR				Function
Bit	PD1_6	SCUE	CH06E	CHC					U0LVM	CLK0SEL		SMD			CKDIR	
				4	3	2	1	0		1	0	2	1	0		
Setting Value	0	X	0	X	X	X	X	X	X	Other than 01b		X	X	X	X	Input port (1)
	1	X	0	X	X	X	X	X	X	Other than 01b		X	X	X	X	Output port (2)
	X	1	1	0	0	1	1	0	X	Other than 01b		X	X	X	X	CH6 analog input
	X	1	1	Other than 00110b					X	Other than 01b		X	X	X	X	CH6 forced “H” output (2)
	0	X	0	X	X	X	X	X	0	0	1	X	X	X	1	CLK0 (external clock) input (1)
	0	X	0	X	X	X	X	X	1	0	1	X	X	X	1	CLK0 (external clock) CMOS input (1, 3)
	X	X	0	X	X	X	X	X	0	0	1	0	0	1	0	CLK0 (internal clock) output (2)
	X	X	0	X	X	X	X	X	1	0	1	0	0	1	0	CLK0 (internal clock) N-channel open-drain output

X: 0 or 1

Notes:

1. Pulled up by setting the PU03 bit in the PUR0 register to 1.
2. Output drive capacity high by setting the P1DRR6 bit in the P1DRR register to 1.
3. Schmitt input is switched to CMOS input.

Table 7.15 Port P1_7/CH7/$\overline{\text{INT1}}$/TRAIO

Register	PD1	SCUCR0	TSIER1	SCHCR					TSMR	TRASR			TRAIOC	TRAMR			INTSR			INTEN	Function
Bit	PD1_7	SCUE	CH07E	CHC					I1LVM	TRAIOSEL			TOPCR	TMOD			INT1SEL			INT1EN	
				4	3	2	1	0		2	1	0		2	1	0	2	1	0		
Setting Value	0	X	0	X	X	X	X	X	0	Other than 001b			X	X	X	X	X	X	X	X	Input port (1)
	1	X	0	X	X	X	X	X	X	Other than 001b			X	X	X	X	X	X	X	X	Output port (2)
	X	1	1	0	0	1	1	1	X	X	X	X	X	X	X	X	X	X	X	X	CH7 analog input
	X	1	1	0Other than 00111b					X	X	X	X	X	X	X	X	X	X	X	X	CH7 forced “H” output (2)
	0	X	0	X	X	X	X	X	0	Other than 001b			X	X	X	X	0	0	0	1	$\overline{\text{INT1}}$ input (1)
	0	X	0	X	X	X	X	X	1	Other than 001b			X	X	X	X	0	0	0	1	$\overline{\text{INT1}}$ CMOS input (1, 3)
	0	X	0	X	X	X	X	X	0	0	0	1	0	Other than 000b, 001b			0	0	0	1	TRAIO input (1)
	X	X	0	X	X	X	X	X	X	0	0	1	0	0	0	1	X	X	X	X	TRAIO pulse output (2)

X: 0 or 1

Notes:

1. Pulled up by setting the PU03 bit in the PUR0 register to 1.
2. Output drive capacity high by setting the P1DRR7 bit in the P1DRR register to 1.
3. Schmitt input is switched to CMOS input.

Table 7.16 Port P3_0/$\overline{\text{INT2}}$/TRAO

Register	PD3	TSMR	TRASR	TRAIOC	INTSR	INTEN	Function
Bit	PD3_0	I2LVM	TRAOSEL0	TOENA	INT2SEL0	INT1EN	
Setting Value	0	0	0	X	X	X	Input port (1)
	1	X	0	X	X	X	Output port (2)
	0	0	0	X	1	1	$\overline{\text{INT2}}$ input (1)
	0	1	0	X	1	1	$\overline{\text{INT2}}$ CMOS input (1, 3)
	X	X	1	1	X	X	TRAO pulse output (2)

X: 0 or 1

Notes:
1. Pulled up by setting the PU06 bit in the PUR0 register to 1.
2. Output drive capacity high by setting the DRR06 bit in the DRR0 register to 1.
3. Schmitt input is switched to CMOS input.

Table 7.17 Port P3_1/TRBO/TRCIOA/TRCTRG

Register	PD3	TRBRCSR			Timer RB Setting	TRCPSR0			Timer RC Setting	Function
Bit	PD3_1	TRBOSEL			—	TRCIOASEL			—	
		2	1	0		2	1	0		
Setting Value	0	Other than 001b			X	Other than 110b			X	Input port (1)
	1	Other than 001b			X	Other than 110b			X	Output port (2)
	X	0	0	1	Refer to **Table 7.25 TRBO Pin Setting**	X	X	X	X	TRBO output (2)
	0	Other than 001b			X	1	1	0	Refer to **Table 7.26 TRCIOA Pin Setting**	TRCIOA input (1)
	X	Other than 001b			X	1	1	0	Refer to **Table 7.26 TRCIOA Pin Setting**	TRCIOA output (2)

X: 0 or 1

Notes:
1. Pulled up by setting the PU06 bit in the PUR0 register to 1.
2. Output drive capacity high by setting the DRR06 bit in the DRR0 register to 1.
3. Schmitt input is switched to CMOS input.

Table 7.18 Port P3_3/$\overline{\text{INT3}}$/TRBO/TRCCLK/$\overline{\text{SCUTRG}}$

Register	PD3	TSMR	INTSR	INTEN	TRBRCSR		TRCCR1			TRBRCSR			Timer RB Setting	SCUMR		Function
Bit	PD3_3	I3LVM	INT3SEL0	INT3EN	TRCCLKSEL		TCK			TRBOSEL			—	SCCAP		
					1	0	2	1	0	2	1	0		1	0	
Setting Value	0	0	X	X	X	X	X	X	X	Other than 011b			X	X	X	Input port (1)
	1	X	X	X	X	X	X	X	X	Other than 011b			X	X	X	Output port (2)
	0	0	0	1	X	X	X	X	X	Other than 011b			X	X	X	$\overline{\text{INT3}}$ input (1)
	0	1	0	1	X	X	X	X	X	Other than 011b			X	X	X	$\overline{\text{INT3}}$ CMOS input (1, 3)
	0	0	X	X	1	0	1	0	1	Other than 011b			X	X	X	TRCCLK input (1)
	X	X	X	X	X	X	X	X	X	0	1	1	Refer to **Table 7.25 TRBO Pin Setting**	X	X	TRBO output (2)
	X	0	0	1	X	X	X	X	X	Other than 011b			X	1	1	$\overline{\text{SCUTRG}}$ input (1)

X: 0 or 1

Notes:

1. Pulled up by setting the PU06 bit in the PUR0 register to 1.
2. Output drive capacity high by setting the DRR06 bit in the DRR0 register to 1.
3. Schmitt input is switched to CMOS input.

Table 7.19 Port P3_4/$\overline{\text{INT2}}$/TRCIOC/TXD0

Register	PD3	TSMR		INTSR	INTEN	U0SR		U0MR			TRCPSR0			Timer RC Setting	Function
Bit	PD3_4	U0LVM	I2LVM	INT2SEL0	INT2EN	TXD0SEL		SMD			TRCIOCSEL			—	
						1	0	2	1	0	2	1	0		
Setting Value	0	X	0	X	X	Other than 10b		X	X	X	Other than 010b			X	Input port (1)
	1	X	X	X	X	Other than 10b		X	X	X	Other than 010b			X	Output port (2)
	0	X	0	0	1	Other than 10b		X	X	X	Other than 010b			X	$\overline{\text{INT2}}$ input (1)
	0	X	1	0	1	Other than 10b		X	X	X	Other than 010b			X	$\overline{\text{INT2}}$ CMOS input (1, 3)
	0	0	X	X	X	1	0	0	0	1	Other than 010b			X	TXD0 output (2, 3)
								1	0	0					
								1	0	1					
								1	1	0					
	0	1	X	X	X	1	0	0	0	1	Other than 010b			X	TXD0 N-channel open-drain output
								1	0	0					
								1	0	1					
								1	1	0					
	0	X	0	1	X	Other than 10b		X	X	X	0	1	0	Refer to **Table 7.28 TRCIOC Pin Setting**	TRCIOC input (1)
	X	X	X	1	X	Other than 10b		X	X	X	0	1	0	Refer to **Table 7.28 TRCIOC Pin Setting**	TRCIOC output (2)

X: 0 or 1

Notes:

1. Pulled up by setting the PU07 bit in the PUR0 register to 1.
2. Output drive capacity high by setting the DRR07 bit in the DRR0 register to 1.
3. Schmitt input is switched to CMOS input.

Table 7.20 Port P3_5/RXD0/$\overline{\text{INT1}}$/TRAIO/TRCIOD

Register	PD3	TSMR		U0SR		TRASR			TRAIOC	TRAMR			INTSR			INTEN	TRCPSR1			Timer RC Setting	Function
Bit	PD3_5	U0LVM	I1LVM	RXD0SEL		TRAIOSEL			TOPCR	TMOD			INT1SEL			INT1EN	TRCIODSEL			—	
				1	0	2	1	0		2	1	0	2	1	0		2	1	0		
Setting Value	0	X	0	Other than 10b		Other than 101b			X	X	X	X	X	X	X	X	Other than 010b			X	Input port (1)
	1	X	X	X	X	Other than 101b			X	X	X	X	X	X	X	X	Other than 010b			X	Output port (2)
	0	X	0	Other than 10b		Other than 101b			X	X	X	X	X	X	X	X	0	1	0	Refer to **Table 7.29 TRCIOD Pin Setting**	TRCIOD input (1)
	X	X	X	X	X	Other than 101b			X	X	X	X	X	X	X	X	0	1	0	Refer to **Table 7.29 TRCIOD Pin Setting**	TRCIOD output (2)
	0	0	0	1	0	Other than 101b			X	X	X	X	X	X	X	X	Other than 010b			X	RXD0 input (1)
	0	1	0	1	0	Other than 101b			X	X	X	X	X	X	X	X	Other than 010b			X	RXD0 CMOS input (1, 3)
	0	X	0	Other than 10b		Other than 101b			X	X	X	X	1	0	1	1	Other than 010b			X	$\overline{\text{INT1}}$ input (1)
	0	X	1	Other than 10b		Other than 101b			X	X	X	X	1	0	1	1	Other than 010b			X	$\overline{\text{INT1}}$ CMOS input (1, 3)
	0	X	0	Other than 10b		1	0	1	0	Other than 000b, 001b			X	X	X	X	Other than 010b			X	TRAIO input (1)
	0	X	X	X	X	1	0	1	0	0	0	1	X	X	X	X	X	X	X	X	TRAIO pulse output (2)

X: 0 or 1

Notes:
1. Pulled up by setting the PU07 bit in the PUR0 register to 1.
2. Output drive capacity high by setting the DRR07 bit in the DRR0 register to 1.
3. Schmitt input is switched to CMOS input.

Table 7.21 Port P3_7/$\overline{\text{INT3}}$/TRAO/CLK0/TRCCLK

Register	PD3	TSMR		U0SR		U0MR				TRASR	TRAIOC	INTSR	INTEN	TRBRCSR		TRCCR1			Function
Bit	PD3_7	U0LVM	I3LVM	CLK0SEL		SMD			CKDIR	TRAOSEL0	TOENA	INT3SEL0	INT3EN	TRCCLKSEL		TCK			
				1	0	2	1	0						1	0	2	1	0	
Setting Value	0	X	0	Other than 10b		X	X	X	X	X	0	X	X	Other than 11b		X	X	X	Input port (1)
	1	X	X	Other than 10b		X	X	X	X	X	0	X	X	Other than 11b		X	X	X	Output port (2)
	0	0	0	1	0	X	X	X	1	X	0	X	X	X	X	X	X	X	CLK0 (external clock) input (1)
	0	1	0	1	0	X	X	X	1	X	0	X	X	X	X	X	X	X	CLK0 (external clock) CMOS input (1, 3)
	0	0	X	1	0	0	0	1	0	X	0	X	X	X	X	X	X	X	CLK0 (internal clock) output (2)
	0	1	X	1	0	0	0	1	0	X	0	X	X	X	X	X	X	X	CLK0 (internal clock) N-channel open-drain output
	X	X	X	Other than 10b		X	X	X	X	0	1	X	X	X	X	X	X	X	TRAO output (2)
	0	X	0	Other than 10b		X	X	X	X	X	0	1	1	X	X	X	X	X	$\overline{\text{INT3}}$ input (1)
	0	X	1	Other than 10b		X	X	X	X	X	0	1	1	X	X	X	X	X	$\overline{\text{INT3}}$ CMOS input (1, 3)
	0	X	0	Other than 10b		X	X	X	X	X	0	X	X	1	1	1	0	1	TRCCLK input (1)

X: 0 or 1

Notes:
1. Pulled up by setting the PU07 bit in the PUR0 register to 1.
2. Output drive capacity high by setting the DRR07 bit in the DRR0 register to 1.
3. Schmitt input is switched to CMOS input.

Table 7.22 Port P4_5/$\overline{\text{INT0}}$/TRCIOB

Register	PD4	TSMR	INTEN	TRCPSR0				TIMRC	Function
Bit	PD4_5	I0LVM	INT0EN	TRCIOBSEL				—	
				3	2	1	0		
Setting Value	0	0	X	Other than 1001b				X	Input port (1)
	1	X	X	Other than 1001b				X	Output port (2)
	0	0	1	Other than 1001b				X	$\overline{\text{INT0}}$ input (1)
	0	1	1	Other than 1001b				X	$\overline{\text{INT0}}$ CMOS input (1, 3)
	0	0	X	1	0	0	1	Refer to **Table 7.27 TRCIOB Pin Setting**	TRCIOB input (1)
	X	X	X	1	0	0	1	Refer to **Table 7.27 TRCIOB Pin Setting**	TRCIOB output (2)

X: 0 or 1
Notes:
1. Pulled up by setting the PU11 bit in the PUR1 register to 1.
2. Output drive capacity high by setting the DRR11 bit in the DRR1 register to 1.
3. Schmitt input is switched to CMOS input.

Table 7.23 Port P4_6/XIN

Register	PD4	CM0	CM1			Circuit specifications		Function
Bit	PD4_6	CM05	CM10	CM11	CM13	Oscillation buffer	Feedback resistor	
Setting Value	0	1	0	X	0	OFF	—	Input port (1)
	1	1	0	X	0	OFF	—	Output port (2)
	X	0	0	0	1	ON	ON	XIN-XOUT oscillation (on-chip feedback resistor enabled)
	X	0	0	1	1	ON	OFF	XIN-XOUT oscillation (on-chip feedback resistor disabled)
	X	1	0	0	1	OFF	ON	XIN-XOUT oscillation stop (on-chip feedback resistor enabled)
	X	1	0	1	1	OFF	OFF	XIN-XOUT oscillation stop (on-chip feedback resistor disabled)
	X	1	1	X	1	OFF	OFF	XIN-XOUT oscillation stop (STOP mode)

X: 0 or 1
Notes:
1. Pulled up by setting the PU11 bit in the PUR1 register to 1.
2. Output drive capacity high by setting the DRR11 bit in the DRR1 register to 1.

Table 7.24 Port P4_7/XOUT

Register	PD4	CM0	CM1			Circuit specifications		Function
Bit	PD4_7	CM05	CM10	CM11	CM13	Oscillation buffer	Feedback resistor	
Setting Value	0	1	0	X	0	OFF	—	Input port (1)
	1	1	0	X	0	OFF	—	Output port (2)
	X	0	0	0	1	ON	ON	XIN-XOUT oscillation (on-chip feedback resistor enabled)
	X	0	0	1	1	ON	OFF	XIN-XOUT oscillation (on-chip feedback resistor disabled)
	X	1	0	0	1	OFF	ON	XIN-XOUT oscillation stop (on-chip feedback resistor enabled)
	X	1	0	1	1	OFF	OFF	XIN-XOUT oscillation stop (on-chip feedback resistor disabled)
	X	1	1	X	1	OFF	OFF	XOUT pull-up

X: 0 or 1
Notes:
1. Pulled up by setting the PU11 bit in the PUR1 register to 1.
2. Output drive capacity high by setting the DRR11 bit in the DRR1 register to 1.

Table 7.25 TRBO Pin Setting

Register	TRBIOC	TRBMR		Function
Bit	TOCNT	TMOD1	TMOD0	
Setting Value	0	0	1	Programmable waveform generation mode (pulse output)
	1	0	1	Programmable waveform generation mode (programmable output)
	0	1	0	Programmable one-shot generation mode
	0	1	1	Programmable wait one-shot generation mode

Table 7.26 TRCIOA Pin Setting

Register	TRCOER	TRCMR	TRCIOR0			TRCCR2		Function
Bit	EA	PWM2	IOA2	IOA1	IOA0	TCEG1	TCEG0	
Setting Value	0	1	0	0	1	X	X	Timer waveform output (output compare function)
			0	1	X	X	X	
	0	1	1	X	X	X	X	Timer mode (input capture function)
	1					X	X	
	0	0	X	X	X	0	1	PWM2 mode TRCTRG input
	1					1	X	

X: 0 or 1

Table 7.27 TRCIOB Pin Setting

Register	TRCOER	TRCMR		TRCIOR0			Function
Bit	EB	PWM2	PWMB	IOB2	IOB1	IOB0	
Setting Value	0	0	X	X	X	X	PWM2 mode waveform output
	0	1	1	X	X	X	PWM mode waveform output
	0	1	0	0	0	1	Timer waveform output (output compare function)
				0	1	X	
	0	1	0	1	X	X	Timer mode (input capture function)
	1						

X: 0 or 1

Table 7.28 TRCIOC Pin Setting

Register	TRCOER	TRCMR		TRCIOR1			Function
Bit	EC	PWM2	PWMC	IOC2	IOC1	IOC0	
Setting Value	0	1	1	X	X	X	PWM mode waveform output
	0	1	0	0	0	1	Timer waveform output (output compare function)
				0	1	X	
	0	1	0	1	X	X	Timer mode (input capture function)
	1						

X: 0 or 1

Table 7.29 TRCIOD Pin Setting

Register	TRCOER	TRCMR		TRCIOR1			Function
Bit	ED	PWM2	PWMD	IOD2	IOD1	IOD0	
Setting Value	0	1	1	X	X	X	PWM mode waveform output
	0	1	0	0	0	1	Timer waveform output (output compare function)
				0	1	X	
	0	1	0	1	X	X	Timer mode (input capture function)
	1						

X: 0 or 1

7.6 Low-Voltage Signal Mode

Serial interface (UART0) communication and the $\overline{\text{INT}}$ input for the $\overline{\text{INT}}$ interrupt can be performed using a low-voltage signal. Table 7.30 lists the Pins Usable for Inputting and Outputting Low-Voltage Signal.
Depending on the setting of the TSMR register, the pins enabled for low-voltage signal mode is switched from schmitt input to CMOS input when they are used as input.
Set the input threshold values for CMOS input using registers VLT0 and VLT1.
When low-voltage signal mode is used, all inputs are set to CMOS input. Since schmitt input is disabled, always take countermeasures against noise.

Table 7.30 Pins Usable for Inputting and Outputting Low-Voltage Signal

Peripheral Function Name		Pin
Serial interface	UART0 Clock synchronous serial I/O Clock asynchronous serial I/O	CLK0, RXD0, TXD0
$\overline{\text{INT}}$	$\overline{\text{INT0}}$ to $\overline{\text{INT3}}$	$\overline{\text{INT0}}$ to $\overline{\text{INT3}}$

7.7 Unassigned Pin Handling

Table 7.31 lists Unassigned Pin Handling. Figure 7.8 shows the Unassigned Pin Handling.

Table 7.31 Unassigned Pin Handling

Pin Name	Connection
Ports P0_0 to P0_2, P1, P3_1, P3_3 to P3_5, P3_7, P4_5 to P4_7	• After setting to input mode, connect each pin to VSS via a resistor (pull-down) or connect each pin to VCC via a resistor (pull-up). (2) • After setting to output mode, leave these pins open. (1, 2)
$\overline{\text{RESET}}$ (3)	Connect to VCC via a pull-up resistor (2)

Notes:
1. If these ports are set to output mode and left open, they remain in input mode until they are switched to output mode by a program. The voltage level of these pins may be undefined and the power current may increase while the ports remain in input mode.
   The content of the direction registers may change due to noise or program runaway caused by noise. In order to enhance program reliability, the program should periodically repeat the setting of the direction registers.
2. Connect these unassigned pins to the MCU using the shortest wire length (2 cm or less) possible.
3. When the power-on reset function is in use.

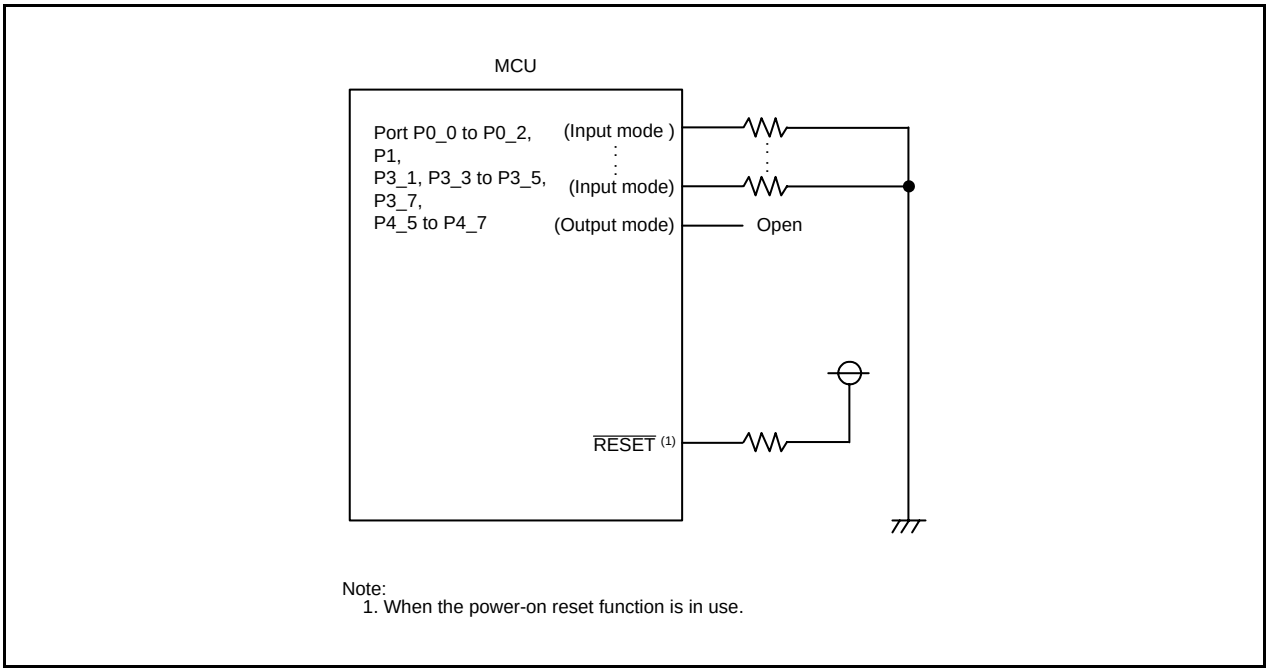


Figure 7.8 Unassigned Pin Handling

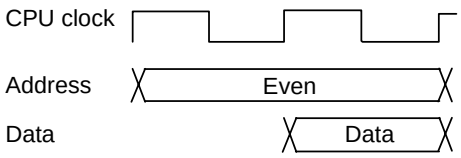
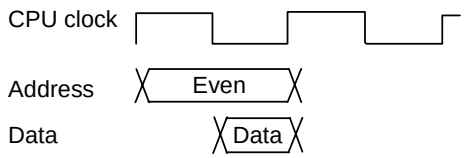
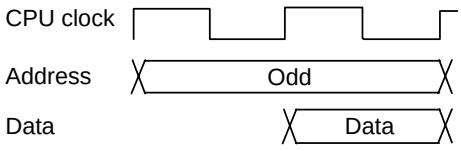
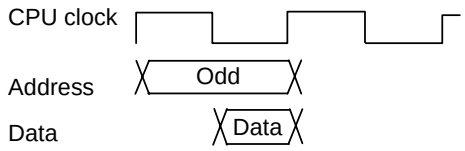
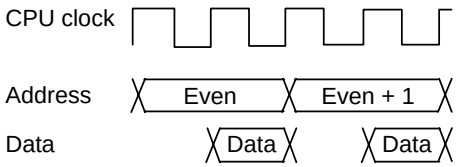
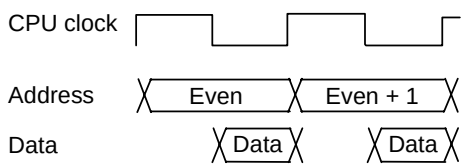
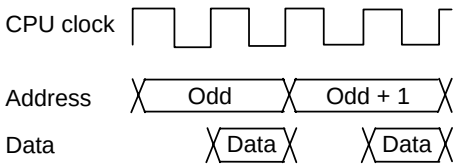
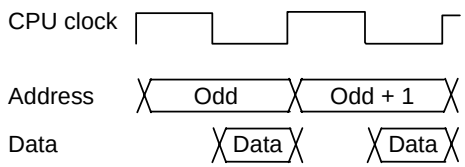
8. Bus

The bus cycles differ when accessing ROM, RAM, DTC vector area, DTC control data and when accessing SFR. Table 8.1 lists Bus Cycles by Access Area of R5R0C0B Group.
ROM, RAM, DTC vector area, DTC control data and SFR are connected to the CPU by an 8-bit bus. When accessing in word (16-bit) units, these areas are accessed twice in 8-bit units.
Table 8.2 lists Access Units and Bus Operations.

Table 8.1 Bus Cycles by Access Area of R5R0C0B Group

Access Area	Bus Cycle
SFR	2 cycles of CPU clock
Program ROM, RAM	1 cycle of CPU clock

Table 8.2 Access Units and Bus Operations

Area	SFR	ROM (program ROM), RAM, DTC vector area, DTC control data
Even address Byte access		
Odd address Byte access		
Even address Word access		
Odd address Word access		

However, only the following SFRs are connected with the 16-bit bus:

Interrupts: Each interrupt control register
Timer RC: Registers TRC, TRCGRA, TRCGRB, TRCGRC, and TRCGRD
Address match interrupt: Registers RMAD0, AIER0, RMAD1, and AIER1
Therefore, they are accessed once in 16-bit units. The bus operation is the same as “Area: SFR, Even address Byte access” in Table 8.2 Access Units and Bus Operations, and 16-bit data is accessed at a time.

9. Clock Generation Circuit

The following four circuits are incorporated in the clock generation circuit:
- XIN clock oscillation circuit
- Low-speed on-chip oscillator
- High-speed on-chip oscillator
- Low-speed on-chip oscillator for watchdog timer

9.1 Overview

Table 9.1 lists the Specification Overview of Clock Generation Circuit. Figure 9.1 shows a Clock Generation Circuit. Figure 9.2 shows a Peripheral Function Clock.

Table 9.1 Specification Overview of Clock Generation Circuit

Item	XIN Clock Oscillation Circuit	On-Chip Oscillator		Low-Speed On-Chip Oscillator for Watchdog Timer
		High-Speed On-Chip Oscillator	Low-Speed On-Chip Oscillator	
Applications	• CPU clock source • Peripheral function clock source	• CPU clock source • Peripheral function clock source • CPU and peripheral function clock source when XIN clock stops oscillating	• CPU clock source • Peripheral function clock source • CPU and peripheral function clock source when XIN clock stops oscillating	• Watchdog timer clock source
Clock frequency	0 to 20 MHz	Approx. 40 MHz (3)	Approx. 125 kHz	Approx. 125 kHz
Connectable oscillator	• Ceramic resonator • Crystal oscillator	—	—	—
Oscillator connect pins	XIN, XOUT (1)	— (1)	— (1)	—
Oscillation stop, restart function	Usable	Usable	Usable	Usable
Oscillator status after reset	Stop	Stop	Oscillate	Stop (4) Oscillate (5)
Others	Externally generated clock can be input (2)	—	—	—

Notes:
1. These pins can be used as P4_6 or P4_7 when using the on-chip oscillator clock as the CPU clock while the XIN clock oscillation circuit is not used.
2. To input an external clock, set the CM05 bit in the CM0 register to 1 (XIN clock stops), the CM11 bit in the CM1 register to 1 (internal feedback resistor disabled), and the CM13 bit to 1 (XIN-XOUT pin).
3. The clock frequency is automatically set to up to approx. 20 MHz by a divider when using the high-speed on-chip oscillator as the CPU clock source.
4. This applies when the CSPROINI bit in the OFS register is set to 1 (count source protection mode disabled after reset).
5. This applies when the CSPROINI bit in the OFS register is set to 0 (count source protection mode enabled after reset).

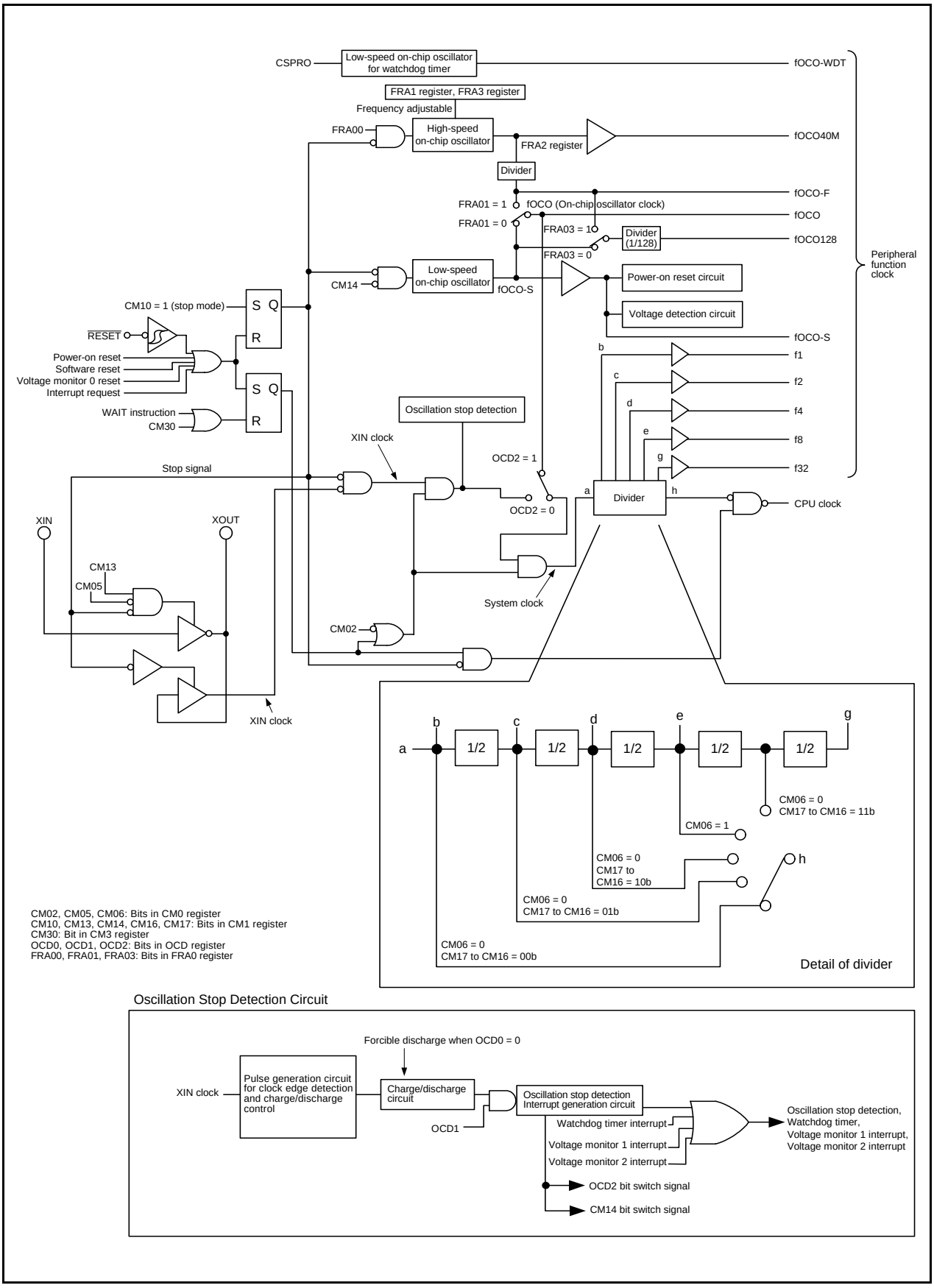


Figure 9.1 Clock Generation Circuit

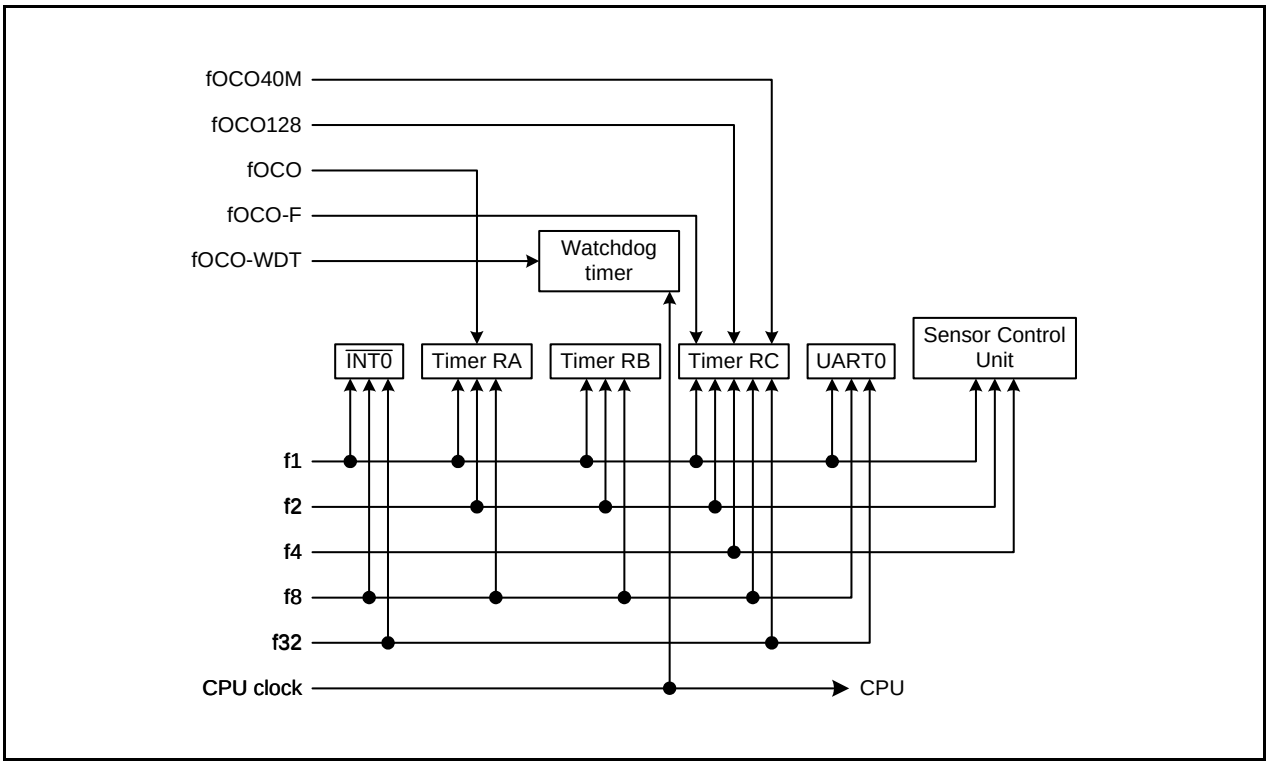


Figure 9.2 Peripheral Function Clock

9.2 Registers

9.2.1 System Clock Control Register 0 (CM0)

Address 0006h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	CM06	CM05	—	—	CM02	—	—
After Reset	0	0	1	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved bits	Set to 0.	R/W
b1	—			
b2	CM02	Wait mode peripheral function clock stop bit	0: Peripheral function clock does not stop in wait mode 1: Peripheral function clock stops in wait mode	R/W
b3	—	Reserved bits	Set to 0.	R/W
b4	—			
b5	CM05	XIN clock (XIN-XOUT) stop bit (1, 3)	0: XIN clock oscillates 1: XIN clock stops (2)	R/W
b6	CM06	CPU clock division select bit 0 (4)	0: Bits CM16 and CM17 in CM1 register enabled 1: Divide-by-8 mode	R/W
b7	—	Reserved bit	Set to 0.	R/W

Notes:
1. The CM05 bit stops the XIN clock when the high-speed on-chip oscillator mode or low-speed on-chip oscillator mode is selected. This bit cannot be used to detect whether the XIN clock has stopped. To stop the XIN clock, set the bits in the following order:
   (1) Set bits OCD1 to OCD0 in the OCD register to 00b.
   (2) Set the OCD2 bit to 1 (on-chip oscillator clock selected).
2. During external clock input, only the clock oscillation buffer stops and clock input is acknowledged.
3. Only when the CM05 bit is set to 1 (XIN clock stops) and the CM13 bit in the CM1 register is set to 0 (P4_6 and P4_7), P4_6 and P4_7 can be used as I/O ports.
4. When the MCU enters stop mode, the CM06 bit is set to 1 (divide-by-8 mode).

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the CM0 register.

9.2.2 System Clock Control Register 1 (CM1)

Address 0007h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CM17	CM16	—	CM14	CM13	—	CM11	CM10
After Reset	0	0	1	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CM10	All clock stop control bit (2, 6)	0: Clock oscillates 1: All clocks stop (stop mode)	R/W
b1	CM11	XIN-XOUT on-chip feedback resistor select bit	0: On-chip feedback resistor enabled 1: On-chip feedback resistor disabled	R/W
b2	—	Reserved bit	Set to 0.	R/W
b3	CM13	Port/XIN-XOUT switch bit (5)	0: I/O ports P4_6 and P4_7 1: XIN-XOUT pin	R/W
b4	CM14	Low-speed on-chip oscillator stop bit (3, 4)	0: Low-speed on-chip oscillator on 1: Low-speed on-chip oscillator off	R/W
b5	—	Reserved bit	Set to 1.	R/W
b6	CM16	CPU clock division select bit 1 (1)	b7 b6 0 0: No division mode 0 1: Divide-by-2 mode 1 0: Divide-by-4 mode 1 1: Divide-by-16 mode	R/W
b7	CM17			R/W

Notes:
1. When the CM06 bit is set to 0 (bits CM16 and CM17 enabled), bits CM16 and CM17 are enabled.
2. If the CM10 bit is set to 1 (stop mode), the on-chip feedback resistor is disabled.
3. When the OCD2 bit is set to 0 (XIN clock selected), the CM14 bit can be set to 1 (low-speed on-chip oscillator off). When the OCD2 bit is set to 1 (on-chip oscillator clock selected), the CM14 bit is set to 0 (low-speed on-chip oscillator on). It remains unchanged even if 1 is written to it.
4. To use the voltage monitor 1 interrupt or voltage monitor 2 interrupt (when the digital filter is used), set the CM14 bit to 0 (low-speed on-chip oscillator on).
5. Once the CM13 bit is set to 1 by a program, it cannot be set to 0.
6. Do not set the CM10 bit to 1 (stop mode) when the VCA20 bit in the VCA2 register to 1 (low consumption enabled).

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the CM1 register.

9.2.3 System Clock Control Register 3 (CM3)

Address 0009h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CM37	CM36	CM35	—	—	—	—	CM30
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CM30	Wait control bit (1)	0: Other than wait mode 1: MCU enters wait mode	R/W
b1	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b2	—			
b3	—	Reserved bits	Set to 0.	R/W
b4	—			
b5	CM35	CPU clock division when exiting wait mode select bit (2)	0: Following settings are enabled: CM06 bit in CM0 register Bits CM16 and CM17 in CM1 register 1: No division	R/W
b6	CM36	System clock when exiting wait mode or stop mode select bit	b7 b6 0 0: MCU exits with the CPU clock immediately before entering wait or stop mode. 0 1: Do not set. 1 0: High-speed on-chip oscillator clock selected (3) 1 1: XIN clock selected (4)	R/W
b7	CM37			R/W

Notes:
1. When the MCU exits wait mode by a peripheral function interrupt, the CM30 bit is set to 0 (other than wait mode).
2. Set the CM35 bit to 0 in stop mode. When the MCU enters wait mode, if the CM35 bit is set to 1 (no division), the CM06 bit in the CM0 register is set to 0 (bits CM16 and CM17 enabled) and bits CM17 and CM16 in the CM1 register is set to 00b (no division mode).
3. When bits CM37 and CM36 are set to 10b (high-speed on-chip oscillator clock selected), the following will be set when the MCU exits wait mode or stop mode.
   • OCD2 bit in OCD register = 1 (on-chip oscillator selected)
   • FRA00 bit in FRA0 register = 1 (high-speed on-chip oscillator on)
   • FRA01 bit in FRA0 register = 1 (high-speed on-chip oscillator selected)
4. When bits CM37 and CM36 are set to 11b (XIN clock selected), the following will be set when the MCU exits wait mode or stop mode.
   • CM15 bit in CM0 register = 0 (XIN clock oscillates)
   • CM13 bit in CM1 register = 1 (XIN-XOUT pin)
   • OCD2 bit in OCD register = 0 (XIN clock selected)
   When the MCU enters wait mode while the CM05 bit in the CM0 register is 1 (XIN clock stops), if the XIN clock is selected as the CPU clock when exiting wait mode, set the CM06 bit to 1 (divide-by-8 mode) and the CM35 bit to 0.
   However, if an externally generated clock is used as the XIN clock, do not set bits CM37 to CM36 to 11b (XIN clock selected).

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the CM3 register.

CM30 bit (Wait Control Bit)

When the CM30 bit is set to 1 (MCU enters wait mode), the CPU clock stops (wait mode). Since the XIN clock and the on-chip oscillator clock do not stop, the peripheral functions using these clocks continue operating. To set the CM30 bit to 1, set the I flag to 0 (maskable interrupt disabled).

The MCU exits wait mode by a reset or peripheral function interrupt. When the MCU exits wait mode by a peripheral function interrupt, it resumes executing the instruction immediately after the instruction to set the CM30 bit to 1.

When the MCU enters wait mode with the WAIT instruction, make sure to set the I flag to 1 (maskable interrupt enabled). With this setting, interrupt handling is performed by the CPU when the MCU exits wait mode.

9.2.4 Oscillation Stop Detection Register (OCD)

Address 000Ch

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	OCD3	OCD2	OCD1	OCD0
After Reset	0	0	0	0	0	1	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	OCD0	Oscillation stop detection enable bit (6)	0: Oscillation stop detection function disabled (1) 1: Oscillation stop detection function enabled	R/W
b1	OCD1	Oscillation stop detection interrupt enable bit	0: Disabled (1) 1: Enabled	R/W
b2	OCD2	System clock select bit (3)	0: XIN clock selected (6) 1: On-chip oscillator clock selected (2)	R/W
b3	OCD3	Clock monitor bit (4, 5)	0: XIN clock oscillates 1: XIN clock stops	R
b4	—	Reserved bits	Set to 0.	R/W
b5	—			
b6	—			
b7	—			

Notes:
1. Set bits OCD1 to OCD0 to 00b before the MCU enters stop mode, high-speed on-chip oscillator mode, or low-speed on-chip oscillator mode (XIN clock stops).
2. If the OCD2 bit is set to 1 (on-chip oscillator clock selected), the CM14 bit is set to 0 (low-speed on-chip oscillator on).
3. The OCD2 bit is automatically set to 1 (on-chip oscillator clock selected) if XIN clock oscillation stop is detected while bits OCD1 to OCD0 are set to 11b. If the OCD3 bit is set to 1 (XIN clock stops), the OCD2 bit remains unchanged even when set to 0 (XIN clock selected).
4. The OCD3 bit is enabled when the OCD0 bit is set to 1 (oscillation stop detection function enabled). In addition, the OCD3 bit cannot be used to confirm whether the XIN clock oscillation is stable.
5. The OCD3 bit remains 0 (XIN clock oscillates) if bits OCD1 to OCD0 are set to 00b.
6. Refer to **Figure 9.8 Procedure for Switching to XIN Clock when XIN Clock Re-Oscillates after Oscillation Stop is Detected** for the switching procedure when the XIN clock re-oscillates after detecting oscillation stop.

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the OCD register.

9.2.5 High-Speed On-Chip Oscillator Control Register 7 (FRA7)

Address 0015h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	When shipping							

Bit	Function	R/W
b7-b0	32 MHz frequency correction data is stored. The frequency can be adjusted by transferring this value to the FRA3 register and by transferring the correction value in the FRA6 register to the FRA1 register.	R

9.2.6 High-Speed On-Chip Oscillator Control Register 0 (FRA0)

Address 0023h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	FRA03	—	FRA01	FRA00
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	FRA00	High-speed on-chip oscillator enable bit	0: High-speed on-chip oscillator off 1: HIgh-speed on-chip oscillator on	R/W
b1	FRA01	High-speed on-chip oscillator select bit (1)	0: Low-speed on-chip oscillator selected (2) 1: High-speed on-chip oscillator selected (3)	R/W
b2	—	Reserved bit	Set to 0.	R/W
b3	FRA03	fOCO128 clock select bit	0: fOCO-S divided by 128 selected 1: fOCO-F divided by 128 selected	R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b5	—			
b6	—			
b7	—			

Notes:
1. Change the FRA01 bit in the following conditions.
   - FRA00 = 1 (high-speed on-chip oscillator on)
   - The CM14 bit in the CM1 register = 0 (low-speed on-chip oscillator on)
   - Bits FRA22 to FRA20 in the FRA2 register:
     All division mode can be set when VCC = 2.7 V to 5.5 V 000b to 111b
2. When setting the FRA01 bit to 0 (low-speed on-chip oscillator selected), do not set the FRA00 bit to 0 (high-speed on-chip oscillator off) at the same time. Set the FRA00 bit to 0 after setting the FRA01 bit to 0.
3. When setting the FRA01 bit to be 1 (high-speed on-chip oscillator selected) and stopping the low-speed on-chip oscillator, wait for one or more cycles of the low-speed on-chip oscillator and then set the CM14 bit in the CM1 register to 1 (low-speed on-chip oscillator off).

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the FRA0 register.

9.2.7 High-Speed On-Chip Oscillator Control Register 1 (FRA1)

Address 0024h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	When shipping							

Bit	Function	R/W
b7-b0	The frequency of the high-speed on-chip oscillator can be adjusted by setting as follows: 40 MHz: FRA1 = value after reset, FRA3 = value after reset 36.864 MHz: Transfer the value in the FRA4 register to the FRA1 register and the value in the FRA5 register to the FRA3 register. 32 MHz: Transfer the value in the FRA6 register to the FRA1 register and the value in the FRA7 register to the FRA3 register.	R/W

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the FRA1 register.
Also, rewrite the FRA1 register when the FRA00 bit in the FRA0 register is set 0 (high-speed on-chip oscillator off).

9.2.8 High-Speed On-Chip Oscillator Control Register 2 (FRA2)

Address 0025h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	FRA22	FRA21	FRA20
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	FRA20	High-speed on-chip oscillator frequency switching bit	Division selection These bits select the division ratio for the high-speed on-chip oscillator clock. b2 b1 b0 0 0 0: Divide-by-2 mode 0 0 1: Divide-by-3 mode 0 1 0: Divide-by-4 mode 0 1 1: Divide-by-5 mode 1 0 0: Divide-by-6 mode 1 0 1: Divide-by-7 mode 1 1 0: Divide-by-8 mode 1 1 1: Divide-by-9 mode	R/W
b1	FRA21			R/W
b2	FRA22			R/W
b3	—	Reserved bits	Set to 0.	R/W
b4	—			
b5	—			
b6	—			
b7	—			

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the FRA2 register.

9.2.9 Clock Prescaler Reset Flag (CPSRF)

Address 0028h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CPSR	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved bits	Set to 0.	R/W
b1	—			
b2	—			
b3	—			
b4	—			
b5	—			
b6	—			
b7	CPSR	Clock prescaler reset flag	Setting this bit to 1 initializes the clock prescaler. (When read, the content is 0)	R/W

9.2.10 High-Speed On-Chip Oscillator Control Register 4 (FRA4)

Address 0029h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	When shipping							

Bit	Function	R/W
b7-b0	36.864 MHz frequency correction data is stored. The frequency can be adjusted by transferring this value to the FRA1 register and by transferring the correction value in the FRA5 register to the FRA3 register.	R

9.2.11 High-Speed On-Chip Oscillator Control Register 5 (FRA5)

Address 002Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	When shipping							

Bit	Function	R/W
b7-b0	36.864 MHz frequency correction data is stored. The frequency can be adjusted by transferring this value to the FRA3 register and by transferring the correction value in the FRA4 register to the FRA1 register.	R

9.2.12 High-Speed On-Chip Oscillator Control Register 6 (FRA6)

Address 002Bh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	When shipping							

Bit	Function	R/W
b7-b0	32 MHz frequency correction data is stored. The frequency can be adjusted by transferring this value to the FRA1 register and by transferring the correction value in the FRA7 register to the FRA3 register.	R

9.2.13 High-Speed On-Chip Oscillator Control Register 3 (FRA3)

Address 002Fh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	When shipping							

Bit	Function	R/W
b7-b0	The frequency of the high-speed on-chip oscillator can be adjusted by setting as follows: 40 MHz: FRA1 = value after reset, FRA3 = value after reset 36.864 MHz: Transfer the value in the FRA4 register to the FRA1 register and the value in the FRA5 register to the FRA3 register. 32 MHz: Transfer the value in the FRA6 register to the FRA1 register and the value in the FRA7 register to the FRA3 register.	R/W

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the FRA3 register.
Also, rewrite the FRA3 register when the FRA00 bit in the FRA0 register is set 0 (high-speed on-chip oscillator off).

9.2.14 Voltage Detect Register 2 (VCA2)

Address 0034h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	VCA27	VCA26	VCA25	—	—	—	—	VCA20
After Reset	0	0	0	0	0	0	0	0

The above applies when the LVDAS bit in the OFS register is set to 1.

After Reset	0	0	1	0	0	0	0	0

The above applies when the LVDAS bit in the OFS register is set to 0.

Bit	Symbol	Bit Name	Function	R/W
b0	VCA20	Internal power low consumption enable bit (1)	0: Low consumption disabled 1: Low consumption enabled (2)	R/W
b1	—	Reserved bits	Set to 0.	R/W
b2	—			
b3	—			
b4	—			
b5	VCA25	Voltage detection 0 enable bit (3)	0: Voltage detection 0 circuit disabled 1: Voltage detection 0 circuit enabled	R/W
b6	VCA26	Voltage detection 1 enable bit (4)	0: Voltage detection 1 circuit disabled 1: Voltage detection 1 circuit enabled	R/W
b7	VCA27	Voltage detection 2 enable bit (5)	0: Voltage detection 2 circuit disabled 1: Voltage detection 2 circuit enabled	R/W

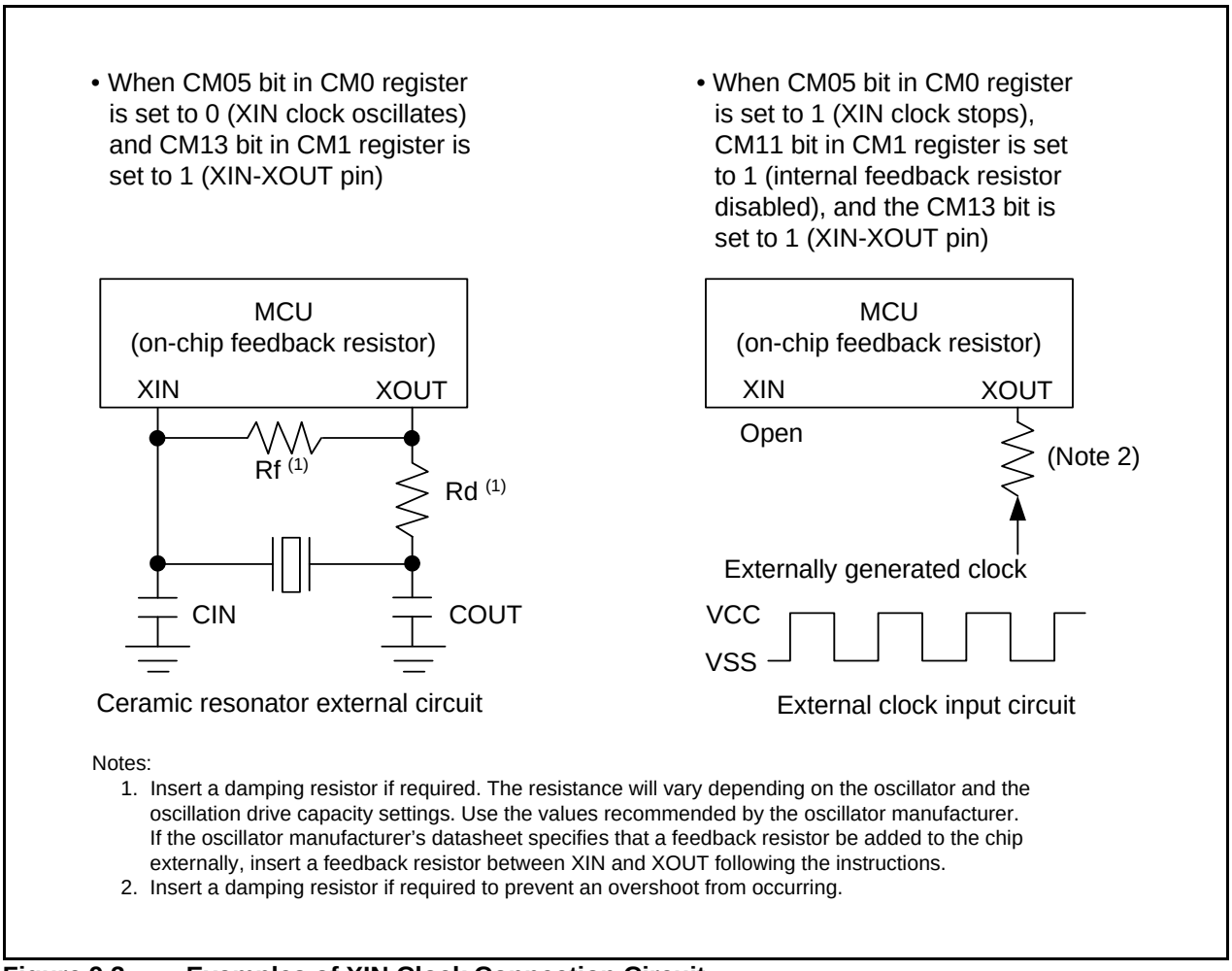
Notes:
1. Use the VCA20 bit only when the MCU enters wait mode. To set the VCA20 bit, follow the procedure shown in **23.2.7 Reducing Internal Power Consumption Using VCA20 Bit**.
2. When the VCA20 bit is set to 1 (low consumption enabled), do not set the CM10 bit in the CM1 register to 1 (stop mode).
3. When writing to the VCA25 bit, set a value after reset.
4. To use the voltage detection 1 interrupt or the VW1C3 bit in the VW1C register, set the VCA26 bit to 1. After the VCA26 bit is set to 1 from 0, allow td(E-A) to elapse before the voltage detection 1 circuit starts operation.
5. To use the voltage detection 2 interrupt or the VCA13 bit in the VCA1 register, set the VCA27 bit to 1. After the VCA27 bit is set to 1 from 0, allow td(E-A) to elapse before the voltage detection 2 circuit starts operation.

Set the PRC3 bit in the PRCR register to 1 (write enabled) before rewriting the VCA2 register.

The clocks generated by the clock generation circuits are described below.

9.3 XIN Clock

The XIN clock is supplied by the XIN clock oscillation circuit. This clock is used as the clock source for the CPU and peripheral function clocks. The XIN clock oscillation circuit is configured by connecting a resonator between pins XIN and XOUT. The XIN clock oscillation circuit includes an on-chip feedback resistor, which is disconnected from the oscillation circuit in stop mode in order to reduce the amount of power consumed by the chip. The XIN clock oscillation circuit may also be configured by feeding an externally generated clock to the XOUT pin.
Figure 9.3 shows Examples of XIN Clock Connection Circuit.
During and after a reset, the XIN clock stops.
After setting the CM13 bit in the CM1 register to 1 (XIN-XOUT pin), the XIN clock starts oscillating when the CM05 bit in the CM0 register is set to 0 (XIN clock oscillates). After the XIN clock oscillation stabilizes, the XIN clock is used as the CPU clock source when the OCD2 bit in the OCD register is set to 0 (XIN clock selected).
The power consumption can be reduced by setting the CM05 bit in the CM0 register to 1 (XIN clock stops) if the OCD2 bit is set to 1 (on-chip oscillator clock selected).
When an externally generated clock is input to the XOUT pin, the XIN clock does not stop even if the CM05 bit is set to 1. If necessary, use an external circuit to stop the clock.
In stop mode, all clocks including the XIN clock stop. Refer to **9.6 Power Control** for details.



Notes:
1. Insert a damping resistor if required. The resistance will vary depending on the oscillator and the oscillation drive capacity settings. Use the values recommended by the oscillator manufacturer. If the oscillator manufacturer's datasheet specifies that a feedback resistor be added to the chip externally, insert a feedback resistor between XIN and XOUT following the instructions.
2. Insert a damping resistor if required to prevent an overshoot from occurring.

Figure 9.3 Examples of XIN Clock Connection Circuit

9.4 On-Chip Oscillator Clock

The on-chip oscillator clock is supplied by the on-chip oscillator (high-speed on-chip oscillator or low-speed on-chip oscillator). This clock is selected by the FRA01 bit in the FRA0 register.

9.4.1 Low-Speed On-Chip Oscillator Clock

The clock generated by the low-speed on-chip oscillator is used as the clock source for the CPU clock, peripheral function clock, fOCO, fOCO-S, and fOCO128.
After a reset, the on-chip oscillator clock generated by the low-speed on-chip oscillator divided by 1 (no division) is selected as the CPU clock.
If the XIN clock stops oscillating when bits OCD1 to OCD0 in the OCD register are set to 11b, the low-speed on-chip oscillator automatically starts operating and supplies the necessary clock for the MCU.
The frequency of the low-speed on-chip oscillator varies depending on the supply voltage and the operating ambient temperature. Application products must be designed with sufficient margin to allow for frequency changes.

9.4.2 High-Speed On-Chip Oscillator Clock

The clock generated by the high-speed on-chip oscillator is used as the clock source for the CPU clock, peripheral function clock, fOCO, fOCO-F, fOCO40M, and fOCO128.
To use the high-speed on-chip oscillator clock as the clock source for the CPU clock, peripheral clock, fOCO, and fOCO-F, set bits FRA20 to FRA22 in the FRA2 register as follows:

- All division mode can be set when VCC = 2.7 V to 5.5 V 000b to 111b

After a reset, the on-chip oscillator clock generated by the high-speed on-chip oscillator stops. Oscillation is started by setting the FRA00 bit in the FRA0 register to 1 (high-speed on-chip oscillator on).

Frequency correction data is stored in registers FRA4 to FRA7.
To adjust the frequency of the high-speed on-chip oscillator clock to 36.864 MHz, first transfer the correction value in the FRA4 register to the FRA1 register and the correction value in the FRA5 register to the FRA3 register before using the values. This enables the setting errors of bit rates such as 9600 bps and 38400 bps to be 0% when the serial interface is used in UART mode (refer to **Table 20.8 Bit Rate Setting Example in UART Mode (Internal Clock Selected)**).
To adjust the frequency of the high-speed on-chip oscillator clock to 32 MHz, first transfer the correction value in the FRA6 register to the FRA1 register and the correction value in the FRA7 register to the FRA3 register before using the values.

9.5 CPU Clock and Peripheral Function Clock

There are a CPU clock to operate the CPU and a peripheral function clock to operate the peripheral functions. Refer to **Figure 9.1 Clock Generation Circuit**.

9.5.1 System Clock

The system clock is the clock source for the CPU and peripheral function clocks. The XIN clock or the on-chip oscillator clock can be selected. The high-speed on-chip oscillator clock is used with supply voltage VCC = 2.7 V to 5.5 V.

9.5.2 CPU Clock

The CPU clock is an operating clock for the CPU and the watchdog timer.
The system clock divided by 1 (no division), 2, 4, 8, or 16 is used as the CPU clock. Use the CM06 bit in the CM0 register and bits CM16 and CM17 in the CM1 register to select the value of the division.
After a reset, the low-speed on-chip oscillator clock divided by 1 (no division) is used as the CPU clock.
When the MCU enters stop mode, the CM06 bit is set to 1 (divide-by-8 mode). To enter stop mode, set the CM35 bit in the CM3 register to 0 (settings of CM06 in CM0 register and bits CM16 and CM17 in CM1 register enabled).

9.5.3 Peripheral Function Clock (f1, f2, f4, f8, and f32)

The peripheral function clock is an operating clock for the peripheral functions.
The fi (i = 1, 2, 4, 8, and 32) clock is generated by the system clock divided by i. It is used for timers RA, RB, RC, and the serial interface.
If the MCU enters wait mode after the CM02 bit in the CM0 register is set to 1 (peripheral function clock stops in wait mode), the fi clock stops.

9.5.4 fOCO

fOCO is an operating clock for the peripheral functions.
The frequency of fOCO is the frequency of the on-chip oscillator clock selected by the FRA01 bit in the FRA0 register. For the high-speed on-chip oscillator, its frequency is the frequency divided by the divide ratio selected by bits FRA20 to FRA22 in the FRA2 register. fOCO can be used for timer RA.
In wait mode, the fOCO clock does not stop.

9.5.5 fOCO40M

fOCO40M is used as the count source for timer RC.
This clock is generated by the high-speed on-chip oscillator and supplied by setting the FRA00 bit to 1.
In wait mode, the fOCO40M clock does not stop.
This clock can be used with supply voltage VCC = 2.7 V to 5.5 V.

9.5.6 fOCO-F

fOCO-F is used as the count source for timer RC.
fOCO-F is a clock generated by the high-speed on-chip oscillator and divided by i (i = 2, 3, 4, 5, 6, 7, 8, and 9; divide ratio selected by the FRA2 register). This clock is supplied by setting the FRA00 bit to 1.
In wait mode, the fOCO-F clock does not stop.

9.5.7 fOCO-S

fOCO-S is an operating clock for the voltage detection circuit.
This clock is generated by the low-speed on-chip oscillator and supplied by setting the CM14 bit to 0 (low-speed on-chip oscillator on).
In wait mode, the fOCO-S clock does not stop.

9.5.8 fOCO128

fOCO128 is a clock generated by dividing fOCO-S or fOCO-F by 128. When the FRA03 bit is set to 0, fOCO-S divided by 128 is selected. When this bit is set to 1, fOCO-F divided by 128 is selected.
fOCO128 is configured as the capture signal used in the TRCGRA register for timer RC.

9.5.9 fOCO-WDT

fOCO-WDT is an operating clock for the watchdog timer.
This clock is generated by the low-speed on-chip oscillator for the watchdog timer and supplied by setting the CSPRO bit in the CSPR register to 1 (count source protect mode enabled).
In count source protection mode for the watchdog timer, the fOCO-WDT clock does not stop.

9.6 Power Control

There are three power control modes. All modes other than wait mode and stop mode are referred to as standard operating mode.

9.6.1 Standard Operating Mode

Standard operating mode is further separated into four modes.
In standard operating mode, the CPU and peripheral function clocks are supplied to operate the CPU and the peripheral functions. Power consumption control is enabled by controlling the CPU clock frequency. The higher the CPU clock frequency, the more processing power increases. The lower the CPU clock frequency, the more power consumption decreases. If unnecessary oscillator circuits stop, power consumption is further reduced.
Before the clock sources for the CPU clock can be switched over, the new clock source needs to be oscillating and stable. Allow sufficient wait time in a program until oscillation stabilizes before switching the clock.

Table 9.2 Settings and Modes of Clock Associated Bits

Modes		OCD Register	CM1 Register			CM0 Register		FRA0 Register	
		OCD2	CM17, CM16	CM14	CM13	CM06	CM05	FRA01	FRA00
High-speed clock mode	No division	0	00b	—	1	0	0	—	—
	Divide-by-2	0	01b	—	1	0	0	—	—
	Divide-by-4	0	10b	—	1	0	0	—	—
	Divide-by-8	0	—	—	1	1	0	—	—
	Divide-by-16	0	11b	—	1	0	0	—	—
High-speed on-chip oscillator mode	No division	1	00b	—	—	0	—	1	1
	Divide-by-2	1	01b	—	—	0	—	1	1
	Divide-by-4	1	10b	—	—	0	—	1	1
	Divide-by-8	1	—	—	—	1	—	1	1
	Divide-by-16	1	11b	—	—	0	—	1	1
Low-speed on-chip oscillator mode	No division	1	00b	0	—	0	—	0	—
	Divide-by-2	1	01b	0	—	0	—	0	—
	Divide-by-4	1	10b	0	—	0	—	0	—
	Divide-by-8	1	—	0	—	1	—	0	—
	Divide-by-16	1	11b	0	—	0	—	0	—

—: Indicates that either 0 or 1 can be set.

9.6.1.1 High-Speed Clock Mode

The XIN clock divided by 1 (no division), 2, 4, 8, or 16 is used as the CPU clock. If the CM14 bit is set to 0 (low-speed on-chip oscillator on) or the FRA00 bit in the FRA0 register is set to 1 (high-speed on-chip oscillator on), fOCO can be used for timer RA.
Also, if the FRA00 bit is set to 1, fOCO40M can be used for timer RC.
If the CM14 bit is set to 0 (low-speed on-chip oscillator on), fOCO-S can be used for the voltage detection circuit.

9.6.1.2 High-Speed On-Chip Oscillator Mode

The high-speed on-chip oscillator is used as the on-chip oscillator clock when the FRA00 bit in the FRA0 register is set to 1 (high-speed on-chip oscillator on) and the FRA01 bit in the FRA0 register is set to 1. The on-chip oscillator divided by 1 (no division), 2, 4, 8, or 16 is used as the CPU clock. If the FRA00 bit is set to 1, fOCO40M can be used for timer RC.
Also, if the CM14 bit is set to 0 (low-speed on-chip oscillator on), fOCO-S can be used for the voltage detection circuit.

9.6.1.3 Low-Speed On-Chip Oscillator Mode

If the CM14 bit in the CM1 register is set to 0 (low-speed on-chip oscillator on) and the FRA01 bit in the FRA0 register is set to 0, the low-speed on-chip oscillator is used as the on-chip oscillator clock. At this time, the on-chip oscillator clock divided by 1 (no division), 2, 4, 8 or 16 is used as the CPU clock. The on-chip oscillator clock is also the clock source for the peripheral function clocks. If the FRA00 bit is set to 1, fOCO40M can be used for timer RC.
Also, if the CM14 bit is set to 0 (low-speed on-chip oscillator on), fOCO-S can be used for the voltage detection circuit.
In this mode, low consumption operation is enabled by stopping the XIN clock and the high-speed on-chip oscillator, and by setting the FMR27 bit in the FMR2 register to 1 (low-consumption-current read mode enabled). When the CPU clock is set to the low-speed on-chip oscillator clock divided by 4, 8, or 16, low-consumption-current read mode can be used. When divided by 1 (no division) or divided by 2 is set, do not use low-consumption-current read mode. After setting the divide ratio of the CPU clock, set the FMR27 bit to 1.
To enter wait mode from low-speed on-chip oscillator mode, lower consumption current in wait mode is enabled by setting the VCA20 bit in the VCA2 register to 1 (internal power low consumption enabled).
To reduce the power consumption, refer to **23. Reducing Power Consumption**.

9.6.2 Wait Mode

Since the CPU clock stops in wait mode, the CPU operating with the CPU clock and the watchdog timer when count source protection mode is disabled stop. Since the XIN clock and on-chip oscillator clock do not stop, the peripheral functions using these clocks continue operating.

9.6.2.1 Peripheral Function Clock Stop Function

If the CM02 bit is set to 1 (peripheral function clock stops in wait mode), the f1, f2, f4, f8, and f32 clocks stop in wait mode. This reduces power consumption.

9.6.2.2 Entering Wait Mode

The MCU enters wait mode by executing the WAIT instruction or setting the CM30 bit in the CM3 register to 1 (MCU enters wait mode).
When the OCD2 bit in the OCD register is set to 1 (on-chip oscillator selected as system clock), set the OCD1 bit in the OCD register to 0 (oscillation stop detection interrupt disabled) before executing the WAIT instruction or setting the CM30 bit in the CM3 register to 1 (MCU enters wait mode).
If the MCU enters wait mode while the OCD1 bit is set to 1 (oscillation stop detection interrupt enabled), current consumption is not reduced because the CPU clock does not stop.
When entering wait mode, set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled) and the FMR27 bit to 0 (low-current-consumption read mode disabled) before entering the mode.
Do not enter wait mode while the FMR01 bit is 1 (CPU rewrite mode enabled) or the FMR27 bit is 1 (low-current-consumption read mode enabled).
To enter wait mode by setting the CM30 bit to 1, set the I flag to 0 (maskable interrupt disabled). To enter wait mode using the WAIT instruction, set the I flag to 1 (maskable interrupt enabled).
When setting bits CM37 and CM36 to values other than 00b to enter wait mode from high-speed clock mode, set the XIN clock frequency to 28 kHz or more.

9.6.2.3 Reducing Internal Power Using VCA20 Bit

When the MCU enters wait mode using low-speed on-chip oscillator mode, internal power consumption can be reduced using the VCA20 bit in the VCA2 register. To enable internal power consumption using the VCA20 bit, follow the procedure shown in 23.2.7 Reducing Internal Power Consumption Using VCA20 Bit.

9.6.2.4 Pin Status in Wait Mode

The I/O ports retain the status immediately before the MCU enters wait mode.

9.6.2.5 Exiting Wait Mode

The MCU exits wait mode by a reset or peripheral function interrupt.
The peripheral function interrupts are affected by the CM02 bit. When the CM02 bit is set to 0 (peripheral function clock does not stop in wait mode), the peripheral function interrupts can be used to exit wait mode. When the CM02 bit is set to 1 (peripheral function clock stops in wait mode), the peripheral functions using the peripheral function clock stop and the peripheral functions operating with external signals or the on-chip oscillator clock can be used to exit wait mode.
Table 9.3 lists Interrupts to Exit Wait Mode and Usage Conditions.

Table 9.3 Interrupts to Exit Wait Mode and Usage Conditions

Interrupt	CM02 = 0	CM02 = 1
Serial interface interrupt	Usable when operating with internal or external clock	Usable when operating with external clock
Key input interrupt	Usable	Usable
Timer RA interrupt	Usable in all modes	Usable if there is no filter in event counter mode. Usable by selecting fOCO as count source.
Timer RB interrupt	Usable in all modes	Usable by selecting fOCO as timer RA count source and timer RA underflow as timer RB count source
Timer RC interrupt	Usable in all modes	(Do not use)
$\overline{\text{INT}}$ interrupt	Usable	Usable ($\overline{\text{INT0}}$ to $\overline{\text{INT3}}$ can be used if there is no filter.)
Voltage monitor 1 interrupt	Usable	Usable
Voltage monitor 2 interrupt	Usable	Usable
Oscillation stop detection interrupt	Usable	(Do not use)
Sensor control unit interrupt	Usable	(Do not use)

9.6.2.6 Exiting Wait Mode after CM30 Bit in CM3 Register is Set to 1 (MCU Enters Wait Mode)

Figure 9.4 shows the Time from Wait Mode to First Instruction Execution following Exit after CM30 Bit in CM3 Register is Set to 1 (MCU Enters Wait Mode).

To use a peripheral function interrupt to exit wait mode, set up the following before setting the CM30 bit to 1.

(1) Set the I flag to 0 (maskable interrupt disabled)
(2) Set the interrupt priority level in bits ILVL2 to ILVL0 in the interrupt control registers of the peripheral function interrupts to be used for exiting wait mode. Set bits ILVL2 to ILVL0 of the peripheral function interrupts that are not to be used for exiting wait mode to 000b (interrupt disabled).
(3) Operate the peripheral function to be used for exiting wait mode.

When the MCU exits by a peripheral function interrupt, the time (number of cycles) between interrupt request generation and interrupt routine execution is determined by the settings of the FMSTP bit in the FMR0 register and the VCA20 bit in the VCA2 register, as shown in Figure 9.4.

The clock set by bits CM35, CM36, and CM37 in the CM3 register is used as the CPU clock when the MCU exits wait mode by a peripheral function interrupt. At this time, the CM06 bit in the CM0 register and bits CM16 and CM17 in the CM1 register automatically change.

FMR0 Register	VCA2 Register	Internal Power Stabilization Time (T0)	Time until Flash Memory Activation (T1)	Time until CPU Clock Supply (T2)	Remarks
FMSTP Bit	VCA20 Bit				
0 (flash memory operates)	0 (internal power low consumption disabled)	0 μs	Period of system clock × 1 cycle + 60 μs (max.)	Period of CPU clock × 2 cycles	The total of T0 to T2 is the time from wait mode to first instruction execution following exit.
	1 (internal power low consumption enabled)	100 μs (max.)			
1 (flash memory stops)	0 (internal power low consumption disabled	0 μs	Period of system clock × 1 cycle	Same as above	
	1 (internal power low consumption enabled)	100 μs (max.)			

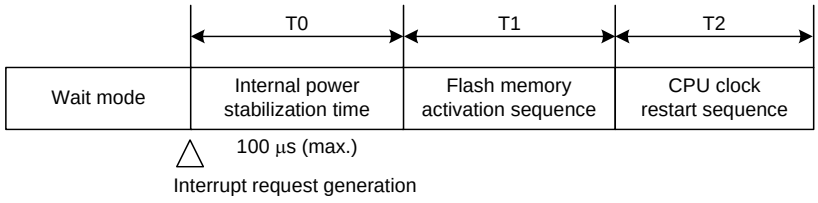


Figure 9.4 Time from Wait Mode to First Instruction Execution following Exit after CM30 Bit in CM3 Register is Set to 1 (MCU Enters Wait Mode)

9.6.2.7 Exiting Wait Mode after WAIT Instruction is Executed

Figure 9.5 shows the Time from Wait Mode to Interrupt Routine Execution after WAIT instruction is Executed. To use a peripheral function interrupt to exit wait mode, set up the following before executing the WAIT instruction.

(1) Set the interrupt priority level in bits ILVL2 to ILVL0 in the interrupt control registers of the peripheral function interrupts to be used for exiting wait mode. Set bits ILVL2 to ILVL0 of the peripheral function interrupts that are not to be used for exiting wait mode to 000b (interrupt disabled).
(2) Set the I flag to 1.
(3) Operate the peripheral function to be used for exiting wait mode.

When the MCU exits by a peripheral function interrupt, the time (number of cycles) between interrupt request generation and interrupt routine execution is determined by the settings of the FMSTP bit in the FMR0 register and the VCA20 bit in the VCA2 register, as shown in Figure 9.5.
The clock set by bits CM35, CM36, and CM37 in the CM3 register is used as the CPU clock when the MCU exits wait mode by a peripheral function interrupt. At this time, the CM06 bit in the CM0 register and bits CM16 and CM17 in the CM1 register automatically change.

FMR0 Register / FMSTP Bit	VCA2 Register / VCA20 Bit	Internal Power Stabilization Time (T0)	Time until Flash Memory Activation (T1)	Time until CPU Clock Supply (T2)	Time for Interrupt Sequence (T3)	Remarks
0 (flash memory operates)	0 (internal power low consumption disabled)	0 μs	Period of system clock × 1 cycle + 60 μs (max.)	Period of CPU clock × 2 cycles	Period of CPU clock × 20 cycles	The total of T0 to T3 is the time from wait mode to interrupt routine execution.
	1 (internal power low consumption enabled)	100 μs (max.)				
1 (flash memory stops)	0 (internal power low consumption disabled	0 μs	Period of system clock × 1 cycle	Same as above	Same as above	
	1 (internal power low consumption enabled)	100 μs (max.)				

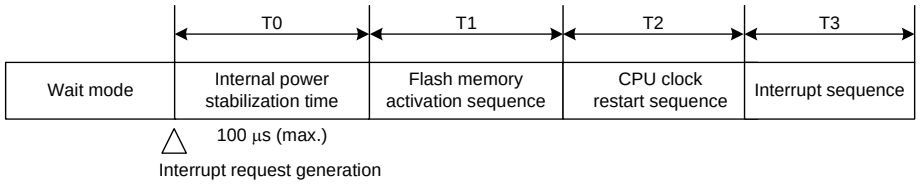


Figure 9.5 Time from Wait Mode to Interrupt Routine Execution after WAIT instruction is Executed

9.6.3 Stop Mode

Since all oscillator circuits except fOCO-WDT stop in stop mode, the CPU and peripheral function clocks stop and the CPU and the peripheral functions operating with these clocks also stop. The least power required to operate the MCU is in stop mode. If the voltage applied to the VCC pin is VRAM or more, the contents of internal RAM is retained.
The peripheral functions clocked by external signals continue operating.
Table 9.4 lists Interrupts to Exit Stop Mode and Usage Conditions.

Table 9.4 Interrupts to Exit Stop Mode and Usage Conditions

Interrupt	Usage Conditions
Key input interrupt	Usable
$\overline{\text{INT0}}$ to $\overline{\text{INT3}}$ interrupt	Usable if there is no filter
Timer RA interrupt	Usable if there is no filter when external pulse is counted in event counter mode
Serial interface interrupt	When external clock selected
Voltage monitor 1 interrupt	Usable in digital filter disabled mode (VW1C1 bit in VW1C register is set to 1)
Voltage monitor 2 interrupt	Usable in digital filter disabled mode (VW2C1 bit in VW2C register is set to 1)

9.6.3.1 Entering Stop Mode

The MCU enters stop mode when the CM10 bit in the CM1 register is set to 1 (all clocks stop). At the same time, the CM06 bit in the CM0 register is set to 1 (divide-by-8 mode).
To use stop mode, set the following before the MCU enters stop mode:

- Bits OCD1 to OCD0 in the OCD register = 00b
- CM35 bit in CM3 register = 0 (settings of CM06 bit in CM0 register and bits CM16 and CM17 in CM1 register enabled)

Enter stop mode after setting the FMR27 bit in the FMR2 register to 0 (low-current-consumption read mode disabled). Do not enter stop mode while the FMR27 bit is 1 (low-current-consumption read mode enabled).

9.6.3.2 Pin Status in Stop Mode

The I/O port retains the status immediately before the MCU enters stop mode.
However, when the CM13 bit in the CM1 register is set to 1 (XIN-XOUT pin), the XOUT(P4_7) pin is held “H”. When the CM13 bit is set to 0 (I/O ports P4_6 and P4_7), P4_6 (XIN) and P4_7 (XOUT) each retain the previous I/O status.

9.6.3.3 Exiting Stop Mode

The MCU exits stop mode by a reset or peripheral function interrupt.
Figure 9.6 shows the Time from Stop Mode to Interrupt Routine Execution.
To use a peripheral function interrupt to exit stop mode, set up the following before setting the CM10 bit to 1.

(1) Set the interrupt priority level in bits ILVL2 to ILVL0 of the peripheral function interrupts to be used for exiting stop mode. Set bits ILVL2 to ILVL0 of the peripheral function interrupts that are not to be used for exiting stop mode to 000b (interrupt disabled).
(2) Set the I flag to 1.
(3) Operate the peripheral function to be used for exiting stop mode.
When the MCU exits stop mode by a peripheral function interrupt, the interrupt sequence is executed when an interrupt request is generated and the CPU clock supply starts.

The clock used immediately before stop mode divided by 8 is used as the CPU clock when the MCU exits stop mode by a peripheral function interrupt. To enter stop mode, set the CM35 bit in the CM3 register to 0 (settings of CM06 bit in CM0 register and bits CM16 and CM17 in CM1 register enabled)

FMR0 Register / FMSTP Bit	Internal Power Stabilization Time (T0)	Time until Flash Memory Activation (T2)	Time until CPU Clock Supply (T3)	Time for Interrupt Sequence (T4)	Remarks
0 (flash memory operates)	100 μs (max.)	Period of system clock × 1 cycle + 60 μs (max.)	Period of CPU clock × 2 cycles	Period of CPU clock × 20 cycles	The total of T0 to T4 is the time from stop mode to interrupt routine execution.
1 (flash memory stops)	100 μs (max.)	Period of system clock × 1 cycle	Same as above	Same as above	

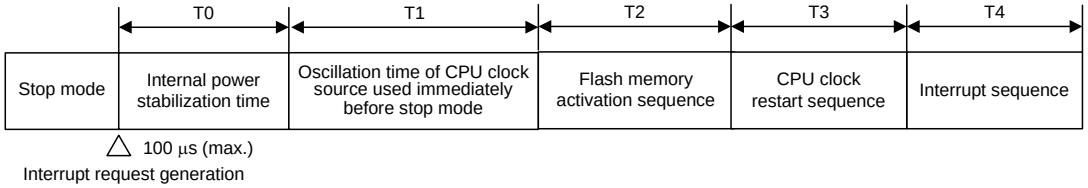


Figure 9.6 Time from Stop Mode to Interrupt Routine Execution

Figure 9.7 shows the State Transitions in Power Control Mode.

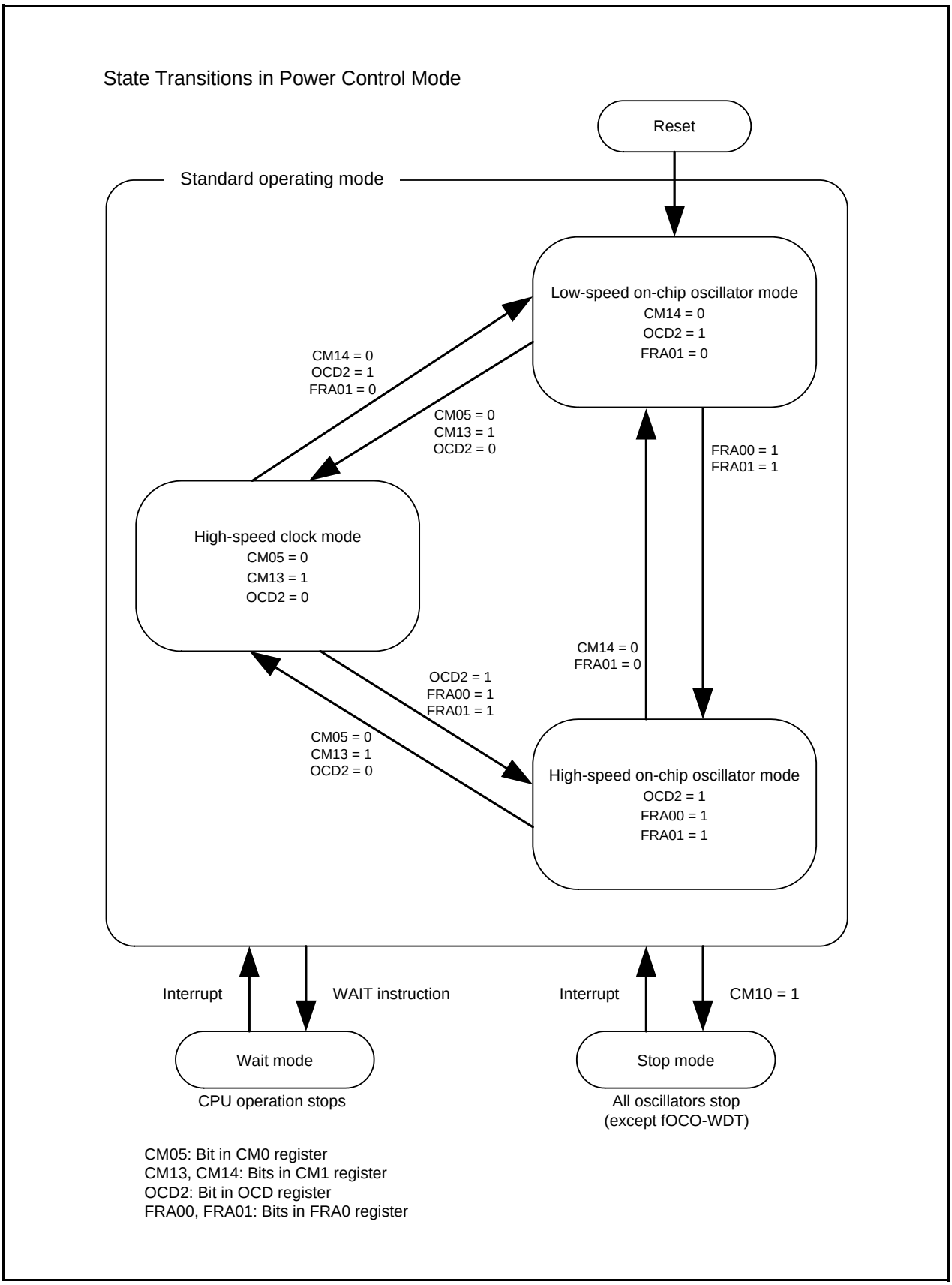


Figure 9.7 State Transitions in Power Control Mode

9.7 Oscillation Stop Detection Function

The oscillation stop detection function detects the stop of the XIN clock oscillating circuit.
The oscillation stop detection function can be enabled and disabled by the OCD0 bit in the OCD register.
Table 9.5 lists the Specifications of Oscillation Stop Detection Function.

When the XIN clock is the CPU clock source and bits OCD1 to OCD0 are set to 11b, the MCU is placed in the following state if the XIN clock stops.

- OCD2 bit in OCD register = 1 (on-chip oscillator clock selected)
- OCD3 bit in OCD register = 1 (XIN clock stops)
- CM14 bit in CM1 register = 0 (low-speed on-chip oscillator oscillates)
- Oscillation stop detection interrupt request is generated

Table 9.5 Specifications of Oscillation Stop Detection Function

Item	Specification
Oscillation stop detection clock and frequency bandwidth	f(XIN) ≥ 2 MHz
Enabled condition for oscillation stop detection function	Bits OCD1 to OCD0 set to 11b
Operation at oscillation stop detection	Oscillation stop detection interrupt generated

9.7.1 How to Use Oscillation Stop Detection Function

- The oscillation stop detection interrupt shares a vector with the watchdog timer interrupt, the voltage monitor 1 interrupt, and the voltage monitor 2 interrupt. To use the oscillation stop detection interrupt and watchdog timer interrupt, the interrupt source needs to be determined.
  Table 9.6 lists the Determination of Interrupt Sources for Oscillation Stop Detection, Watchdog Timer, Voltage Monitor 1, or Voltage Monitor 2 Interrupt. Figure 9.9 shows an Example of Determining Interrupt Sources for Oscillation Stop Detection, Watchdog Timer, Voltage Monitor 1, or Voltage Monitor 2 Interrupt.
- When the XIN clock restarts after oscillation stop, switch the XIN clock to the clock source for the CPU clock and the peripheral functions by a program.
  Figure 9.8 shows the Procedure for Switching to XIN Clock when XIN Clock Re-Oscillates after Oscillation Stop is Detected.
- To enter wait mode while the oscillation stop detection function is used, set the CM02 bit to 0 (peripheral function clock does not stop in wait mode).
- Since the oscillation stop detection function is a function for cases where the XIN clock is stopped by an external cause, set bits OCD1 to OCD0 to 00b to stop or start the XIN clock by a program (select stop mode or change the CM05 bit).
- This function cannot be used when the XIN clock frequency is below 2 MHz. In this case, set bits OCD1 to OCD0 to 00b.
- To use the low-speed on-chip oscillator clock as the clock source for the CPU clock and the peripheral functions after detecting the oscillation stop, set the FRA01 bit in the FRA0 register to 0 (low-speed on-chip oscillator selected) and bits OCD1 to OCD0 to 11b.
  To use the high-speed on-chip oscillator clock as the clock source for the CPU clock and the peripheral functions after detecting the oscillation stop, first set the FRA00 bit to 1 (high-speed on-chip oscillator oscillates) and the FRA01 bit to 1 (high-speed on-chip oscillator selected). Then set bits OCD1 to OCD0 to 11b.

Table 9.6 Determination of Interrupt Sources for Oscillation Stop Detection, Watchdog Timer, Voltage Monitor 1, or Voltage Monitor 2 Interrupt

Generated Interrupt Source	Bit Indicating Interrupt Source
Oscillation stop detection ((a) or (b))	(a) OCD3 bit in OCD register = 1
	(b) OCD1 to OCD0 bits in OCD register = 11b and OCD2 bit = 1
Watchdog timer	VW2C3 bit in VW2C register = 1
Voltage monitor 1	VW1C2 bit in VW1C register = 1
Voltage monitor 2	VW2C2 bit in VW2C register = 1

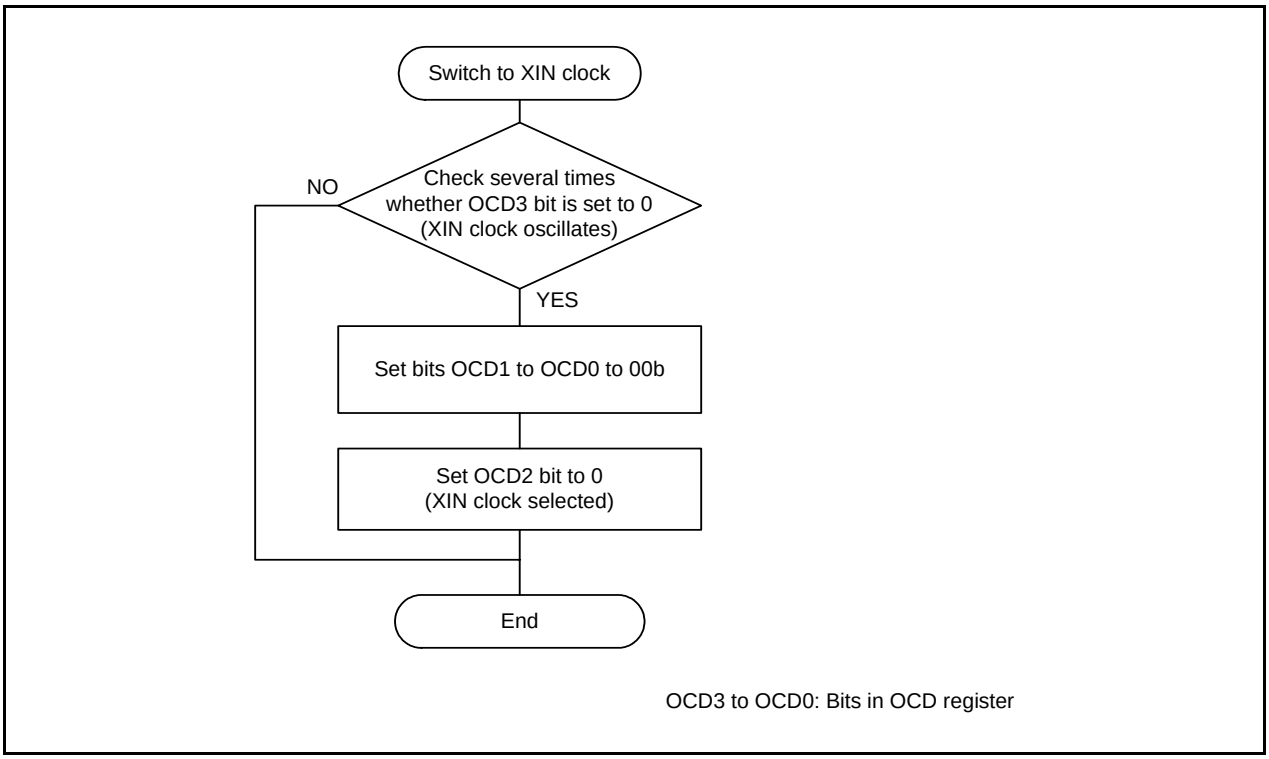
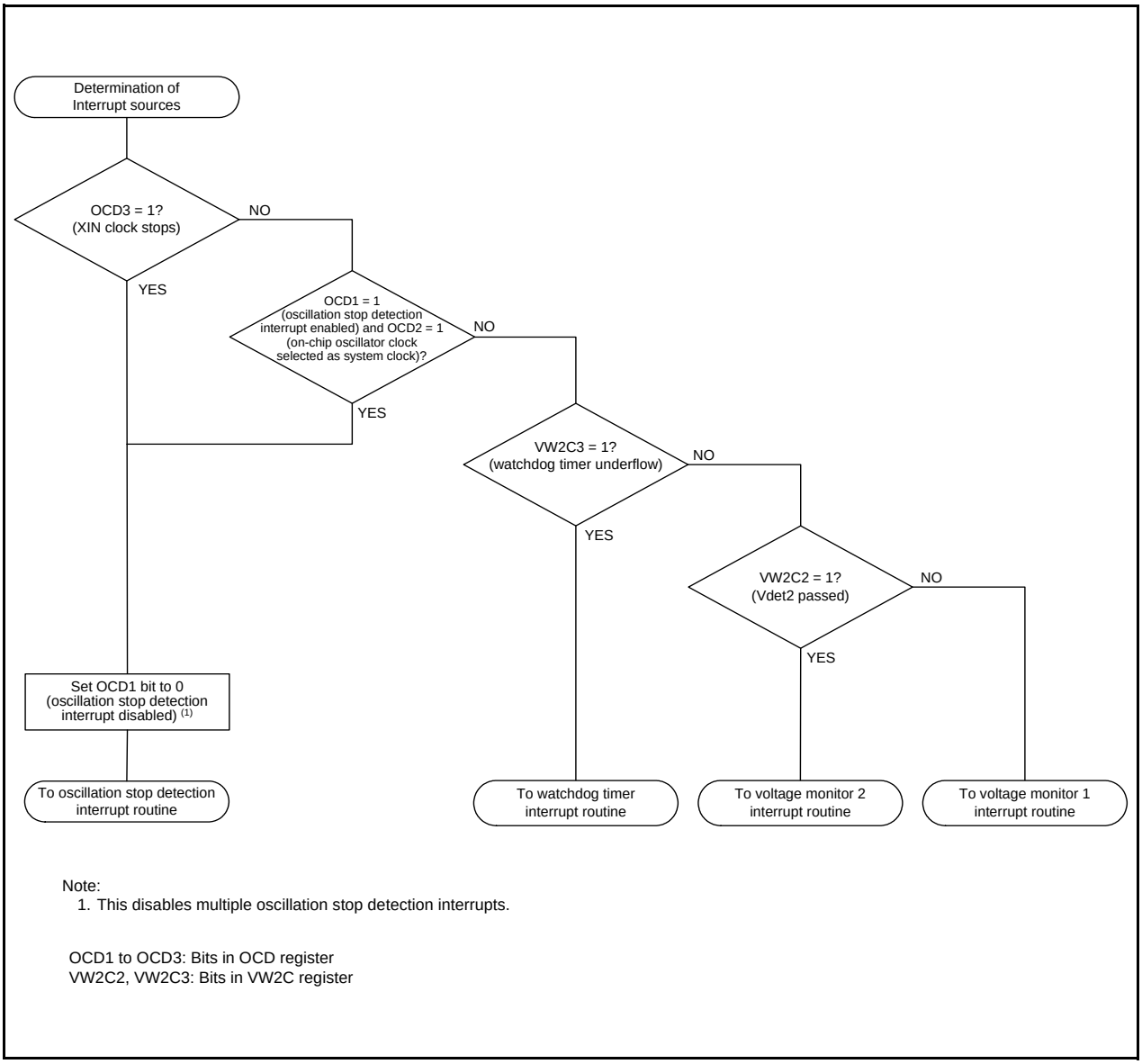


Figure 9.8 Procedure for Switching to XIN Clock when XIN Clock Re-Oscillates after Oscillation Stop is Detected



Note:
1. This disables multiple oscillation stop detection interrupts.

OCD1 to OCD3: Bits in OCD register
VW2C2, VW2C3: Bits in VW2C register

Figure 9.9 Example of Determining Interrupt Sources for Oscillation Stop Detection, Watchdog Timer, Voltage Monitor 1, or Voltage Monitor 2 Interrupt

9.8 Notes on Clock Generation Circuit

9.8.1 Stop Mode

To enter stop mode, set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled) and then the CM10 bit in the CM1 register to 1 (stop mode). An instruction queue pre-reads 4 bytes from the instruction which sets the CM10 bit to 1 (stop mode) and the program stops.
Insert at least four NOP instructions following the JMP.B instruction after the instruction which sets the CM10 bit to 1.

- Program example to enter stop mode

```
        BCLR    1, FMR0         ; CPU rewrite mode disabled
        BCLR    7, FMR2         ; Low-current-consumption read mode disabled
        BSET    0, PRCR         ; Writing to CM1 register enabled
        FSET    I               ; Enable interrupt
        BSET    0, CM1          ; Stop mode
        JMP.B   LABEL_001
LABEL_001:
        NOP
        NOP
        NOP
        NOP
```

9.8.2 Wait Mode

When entering wait mode, set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled) and the FMR27 bit to 0 (low-current-consumption read mode disabled) before entering the mode. Do not enter wait mode while the FMR01 bit is 1 (CPU rewrite mode enabled) or the FMR27 bit is 1 (low-current-consumption read mode enabled).
To enter wait mode by setting the CM30 bit to 1, set the I flag to 0 (maskable interrupt disabled).
To enter wait mode using the WAIT instruction, set the I flag to 1 (maskable interrupt enabled). An instruction queue pre-reads 4 bytes from the instruction to set the CM30 bit to 1 (MCU enters wait mode) or the WAIT instruction, and then the program stops. Insert at least four NOP instructions after the instruction to set the CM30 bit to 1 (MCU enters wait mode) or the WAIT instruction.

- Program example to execute the WAIT instruction

```
        BCLR    1, FMR0         ; CPU rewrite mode disabled
        BCLR    7, FMR2         ; Low-current-consumption read mode disabled
        FSET    I               ; Enable interrupt
        WAIT                    ; Wait mode
        NOP
        NOP
        NOP
        NOP
```

- Program example to execute the instruction to set the CM30 bit to 1

```
        BCLR    1, FMR0         ; CPU rewrite mode disabled
        BCLR    7, FMR2         ; Low-current-consumption read mode disabled
        BSET    0, PRCR         ; Writing to CM3 register enabled
        FCLR    I               ; Interrupt disabled
        BSET    0, CM3          ; Wait mode
        NOP
        NOP
        NOP
        NOP
        BCLR    0, PRCR         ; Writing to CM3 register disabled
        FSET    I               ; Interrupt enabled
```

9.8.3 Reducing Internal Power Using VCA20 Bit

Set the VCA20 bit to 1 in low-speed clock mode or low-speed on-chip oscillator mode before entering wait mode. To enter wait mode by setting the CM30 bit in the CM3 register to 1 (MCU enters wait mode), follow the procedure shown in Figure 23.1 to set the procedure for reducing internal power consumption using the VCA20 bit.
To enter wait mode by executing WAIT instruction, follow the procedure shown in Figure 23.2 to set the procedure for reducing internal power consumption using the VCA20 bit.

9.8.4 Oscillation Stop Detection Function

Since the oscillation stop detection function cannot be used if the XIN clock frequency is below 2 MHz, set bits OCD1 to OCD0 to 00b. In addition, the OCD3 bit cannot be used to confirm whether the XIN clock oscillation is stable.

9.8.5 Oscillation Circuit Constants

Consult the oscillator manufacturer to determine the optimal oscillation circuit constants for the user system.

10. Protection

The protection function protects important registers from being easily overwritten if a program runs out of control. The registers protected by the PRCR register are as follows:

- Registers protected by PRC0 bit: Registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3
- Registers protected by PRC1 bit: Registers PM0 and PM1
- Registers protected by PRC2 bit: PD0 register
- Registers protected by PRC3 bit: Registers VCA2, VD1LS, VW0C, VW1C, and VW2C

10.1 Register

10.1.1 Protect Register (PRCR)

Address 000Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	PRC3	PRC2	PRC1	PRC0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	PRC0	Protect bit 0	Enables writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3. 0: Write disabled 1: Write enabled (2)	R/W
b1	PRC1	Protect bit 1	Enables writing to registers PM0 and PM1. 0: Write disabled 1: Write enabled (2)	R/W
b2	PRC2	Protect bit 2	Enables writing to the PD0 register. 0: Write disabled 1: Write enabled (1)	R/W
b3	PRC3	Protect bit 3	Enables writing to registers VCA2, VD1LS, VW0C, VW1C, and VW2C. 0: Write disabled 1: Write enabled (2)	R/W
b4	—	Reserved bits	Set to 0.	R/W
b5	—			
b6	—			
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

Notes:

1. The PRC2 bit is set to 0 after setting it to 1 (write enabled) and writing to the SFR area. Change the register protected by the PRC2 bit with the next instruction after that used to set the PRC2 bit to 1. Do not allow interrupts or DTC activation between the instruction to set to the PRC2 bit to 1 and the next instruction.
2. Bits PRC0, PRC1, and PRC3 are not set to 0 even after setting them to 1 (write enabled) and writing to the SFR areas. Set these bits to 0 by a program.

11. Interrupts

11.1 Overview

11.1.1 Types of Interrupts

Figure 11.1 shows the Types of Interrupts.

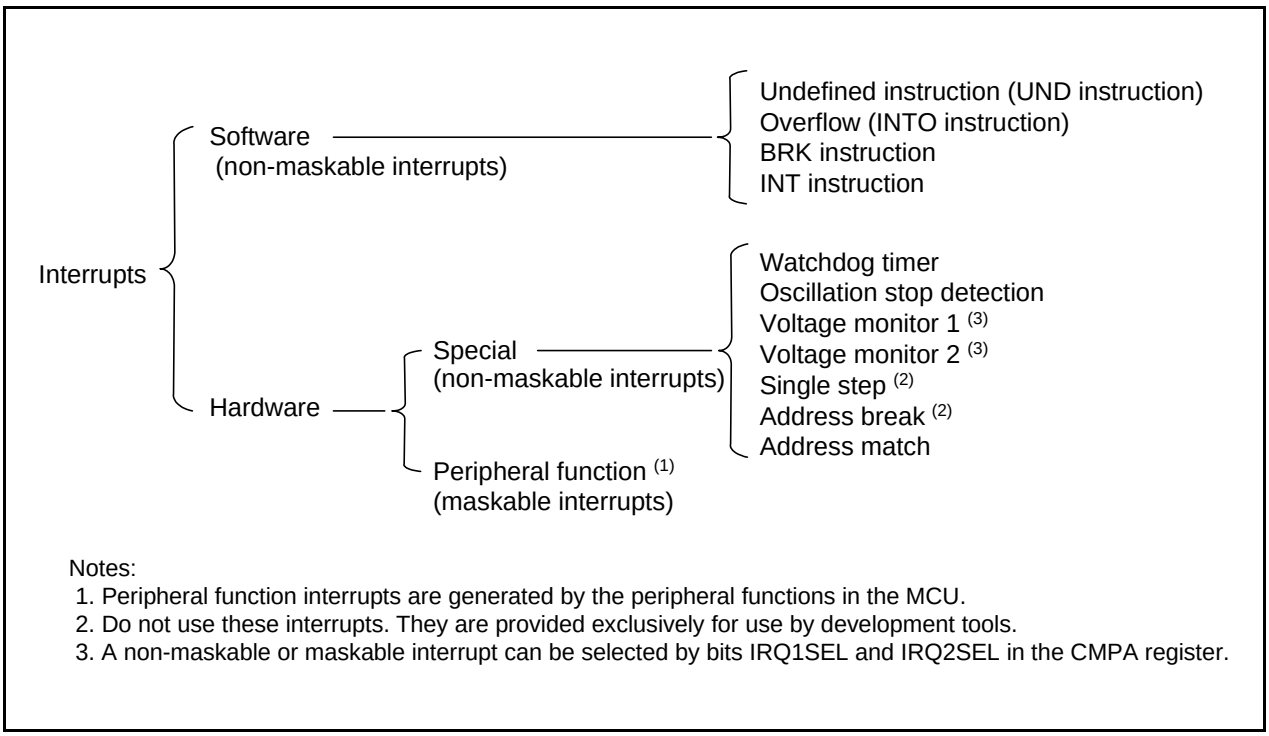


Figure 11.1 Types of Interrupts

- Maskable interrupts: These interrupts are enabled or disabled by the interrupt enable flag (I flag). The interrupt priority **can be changed** based on the interrupt priority level.
- Non-maskable interrupts: These interrupts are not enabled or disabled by the interrupt enable flag (I flag). The interrupt priority **cannot be changed** based on the interrupt priority level.

11.1.2 Software Interrupts

A software interrupt is generated when an instruction is executed. Software interrupts are non-maskable.

11.1.2.1 Undefined Instruction Interrupt

An undefined instruction interrupt is generated when the UND instruction is executed.

11.1.2.2 Overflow Interrupt

An overflow interrupt is generated when the O flag is set to 1 (arithmetic operation overflow) and the INTO instruction is executed. Instructions that set the O flag are as follows:
ABS, ADC, ADCF, ADD, CMP, DIV, DIVU, DIVX, NEG, RMPA, SBB, SHA, and SUB.

11.1.2.3 BRK Interrupt

A BRK interrupt is generated when the BRK instruction is executed.

11.1.2.4 INT Instruction Interrupt

An INT instruction interrupt is generated when the INT instruction is executed. Software interrupt numbers 0 to 63 can be specified with the INT instruction. Because some software interrupt numbers are assigned to peripheral function interrupts, the same interrupt routine as for peripheral function interrupts can be executed by executing the INT instruction.
For software interrupt numbers 0 to 31, the U flag is saved on the stack during instruction execution and the U flag is set to 0 (ISP selected) before the interrupt sequence is executed. The U flag is restored from the stack when returning from the interrupt routine. For software interrupt numbers 32 to 63, the U flag does not change state during instruction execution, and the selected SP is used.

11.1.3 Special Interrupts

Special interrupts are non-maskable.

11.1.3.1 Watchdog Timer Interrupt

A watchdog timer interrupt is generated by the watchdog timer. For details, refer to **14. Watchdog Timer**.

11.1.3.2 Oscillation Stop Detection Interrupt

An oscillation stop detection interrupt is generated by the oscillation stop detection function. For details of the oscillation stop detection function, refer to **9. Clock Generation Circuit**.

11.1.3.3 Voltage Monitor 1 Interrupt

A voltage monitor 1 interrupt is generated by the voltage detection circuit. A non-maskable or maskable interrupt can be selected by IRQ1SEL bit in the CMPA register. For details of the voltage detection circuit, refer to **6. Voltage Detection Circuit** and for details.

11.1.3.4 Voltage Monitor 2 Interrupt

A voltage monitor 2 interrupt is generated by the voltage detection circuit. A non-maskable or maskable interrupt can be selected by IRQ2SEL bit in the CMPA register. For details of the voltage detection circuit, refer to **6. Voltage Detection Circuit** and for details.

11.1.3.5 Single-Step Interrupt, and Address Break Interrupt

Do not use these interrupts. They are provided exclusively for use by development tools.

11.1.3.6 Address Match Interrupt

An address match interrupt is generated immediately before executing an instruction that is stored at an address indicated by registers RMAD0 to RMAD1 if the AIER00 bit in the AIER0 register or the AIER10 bit in the AIER1 register is set to 1 (address match interrupt enabled).
For details of the address match interrupt, refer to **11.7 Address Match Interrupt**.

11.1.4 Peripheral Function Interrupts

A peripheral function interrupt is generated by a peripheral function in the MCU. Peripheral function interrupts are maskable. Refer to **Table 11.2 Relocatable Vector Tables** for sources of the corresponding peripheral function interrupt. For details of peripheral functions, refer to the descriptions of individual peripheral functions.

11.1.5 Interrupts and Interrupt Vectors

There are 4 bytes in each vector. Set the starting address of an interrupt routine in each interrupt vector. When an interrupt request is acknowledged, the CPU branches to the address set in the corresponding interrupt vector. Figure 11.2 shows an Interrupt Vector.

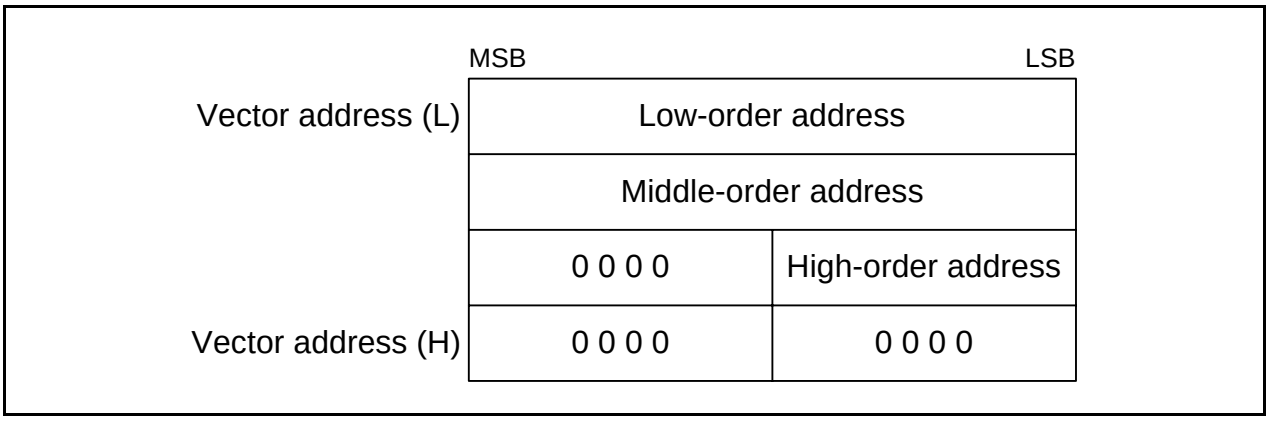


Figure 11.2 Interrupt Vector

11.1.5.1 Fixed Vector Tables

The fixed vector tables are allocated addresses 0FFDCh to 0FFFFh.
Table 11.1 lists the Fixed Vector Tables. The vector addresses (H) of fixed vectors are used by the ID code check function. For details, refer to **22.3 Functions to Prevent Flash Memory from being Rewritten**.

Table 11.1 Fixed Vector Tables

Interrupt Source	Vector Addresses Address (L) to (H)	Remarks	Reference
Undefined instruction	0FFDCh to 0FFDFh	Interrupt with UND instruction	R8C/Tiny Series Software Manual
Overflow	0FFE0h to 0FFE3h	Interrupt with INTO instruction	
BRK instruction	0FFE4h to 0FFE7h	If the content of address 0FFE6h is FFh, program execution starts from the address shown by the vector in the relocatable vector table.	
Address match	0FFE8h to 0FFEBh		11.7 Address Match Interrupt
Single step (1)	0FFECh to 0FFEFh		
Watchdog timer, Oscillation stop detection, Voltage monitor 1 (2), Voltage monitor 2 (3)	0FFF0h to 0FFF3h		14. Watchdog Timer 9. Clock Generation Circuit 6. Voltage Detection Circuit
Address break (1)	0FFF4h to 0FFF7h		
(Reserved)	0FFF8h to 0FFFBh		
Reset	0FFFCh to 0FFFFh		5. Resets

Notes:
1. Do not use these interrupts. They are provided exclusively for use by development tools.
2. Voltage monitor 1 interrupt is selected when the IRQ1SEL bit in the CMPA register is set to 0 (non-maskable interrupt).
3. Voltage monitor 2 interrupt is selected when the IRQ2SEL bit in the CMPA register is set to 0 (non-maskable interrupt).

11.1.5.2 Relocatable Vector Tables

The relocatable vector tables occupy 256 bytes beginning from the starting address set in the INTB register. Table 11.2 lists the Relocatable Vector Tables.

Table 11.2 Relocatable Vector Tables

Interrupt Source	Vector Addresses (1) Address (L) to Address (H)	Software Interrupt Number	Interrupt Control Register	Reference
BRK instruction (2)	+0 to +3 (0000h to 0003h)	0	—	R8C/Tiny Series Software Manual
Flash memory ready	+4 to +7 (0004h to 0007h)	1	FMRDYIC	22. Flash Memory
(Reserved)		2 to 5	—	—
(Reserved)	+24 to +27 (0018h to 001Bh)	6	—	—
Timer RC	+28 to +31 (001Ch to 001Fh)	7	TRCIC	19. Timer RC
(Reserved)	+32 to +35 (0020h to 0023h)	8	—	—
(Reserved)	+36 to +39 (0024h to 0027h)	9	—	—
(Reserved)	+40 to +43 (0028h to 002Bh)	10	—	—
(Reserved)	+44 to +47 (002Ch to 002Fh)	11	—	—
(Reserved)	+48 to +51 (0030h to 0033h)	12	—	—
Key input	+52 to +55 (0034h to 0037h)	13	KUPIC	11.6 Key Input Interrupt
(Reserved)	+56 to +59 (0038h to 003Bh)	14	—	—
(Reserved)	+60 to +63 (003Ch to 003Fh)	15	—	—
(Reserved)		16	—	—
UART0 transmit	+68 to +71 (0044h to 0047h)	17	S0TIC	20. Serial Interface (UART0)
UART0 receive	+72 to +75 (0048h to 004Bh)	18	S0RIC	
(Reserved)		19	—	—
(Reserved)		20	—	—
$\overline{\text{INT2}}$	+84 to +87 (0054h to 0057h)	21	INT2IC	11.4 $\overline{\text{INT}}$ Interrupt
Timer RA	+88 to +91 (0058h to 005Bh)	22	TRAIC	17. Timer RA
(Reserved)		23	—	—
Timer RB	+96 to +99 (0060h to 0063h)	24	TRBIC	18. Timer RB
$\overline{\text{INT1}}$	+100 to +103 (0064h to 0067h)	25	INT1IC	11.4 $\overline{\text{INT}}$ Interrupt
$\overline{\text{INT3}}$	+104 to +107 (0068h to 006Bh)	26	INT3IC	
(Reserved)		27	—	—
(Reserved)		28	—	—
$\overline{\text{INT0}}$	+116 to +119 (0074h to 0077h)	29	INT0IC	11.4 $\overline{\text{INT}}$ Interrupt
(Reserved)	+120 to +123 (0078h to 007Bh)	30	—	—
(Reserved)		31	—	—
Software (2)	+128 to +131 (0080h to 0083h) to +164 to +167 (00A4h to 00A7h)	32 to 41	—	R8C/Tiny Series Software Manual
Sensor control unit	+168 to +171 (00A8h to 00ABh)	42	SCUIC	21. Sensor Control Unit
(Reserved)		43 to 49	—	—
Voltage monitor 1 (3)	+200 to +203 (00C8h to 00CBh)	50	VCMP1IC	6. Voltage Detection Circuit
Voltage monitor 2 (4)	+204 to +207 (00CCh to 00CFh)	51	VCMP2IC	
(Reserved)		52 to 55	—	—
Software (2)	+224 to +227 (00E0h to 00E3h) to +252 to +255 (00FCh to 00FFh)	56 to 63	—	R8C/Tiny Series Software Manual

Notes:
1. These addresses are relative to those in the INTB register.
2. These interrupts are not disabled by the I flag.
3. Voltage monitor 1 interrupt is selected when the IRQ1SEL bit in the CMPA register is set to 1 (maskable interrupt).
4. Voltage monitor 2 interrupt is selected when the IRQ2SEL bit in the CMPA register is set to 1 (maskable interrupt).

11.2 Registers

11.2.1 Interrupt Control Register (KUPIC, S0TIC, S0RIC, TRAIC, TRBIC, SCUIC, VCMP1IC, VCMP2IC)

Address 004Dh (KUPIC), 0051h (S0TIC), 0052h (S0RIC), 0056h (TRAIC), 0058h (TRBIC), 006Ah (SCUIC), 0072h (VCMP1IC), 0073h (VCMP2IC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	IR	ILVL2	ILVL1	ILVL0
After Reset	X	X	X	X	X	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ILVL0	Interrupt priority level select bit	b2 b1 b0 0 0 0: Level 0 (interrupt disabled) 0 0 1: Level 1 0 1 0: Level 2 0 1 1: Level 3 1 0 0: Level 4 1 0 1: Level 5 1 1 0: Level 6 1 1 1: Level 7	R/W
b1	ILVL1			R/W
b2	ILVL2			R/W
b3	IR	Interrupt request bit	0: No interrupt requested 1: Interrupt requested	R/W (1)
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is undefined.		—
b5	—			
b6	—			
b7	—			

Note:
1. Only 0 can be written to the IR bit. Do not write 1 to this bit.

Rewrite the interrupt control register when an interrupt request corresponding to the register is not generated. Refer to **11.9.5 Rewriting Interrupt Control Register**.

11.2.2 Interrupt Control Register (FMRDYIC, TRCIC)

Address 0041h (FMRDYIC), 0047h (TRCIC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	IR	ILVL2	ILVL1	ILVL0
After Reset	X	X	X	X	X	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ILVL0	Interrupt priority level select bit	b2 b1 b0 0 0 0: Level 0 (interrupt disabled) 0 0 1: Level 1 0 1 0: Level 2 0 1 1: Level 3 1 0 0: Level 4 1 0 1: Level 5 1 1 0: Level 6 1 1 1: Level 7	R/W
b1	ILVL1			R/W
b2	ILVL2			R/W
b3	IR	Interrupt request bit	0: No interrupt requested 1: Interrupt requested	R
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is undefined.		—
b5	—			
b6	—			
b7	—			

Rewrite the interrupt control register when an interrupt request corresponding to the register is not generated. Refer to **11.9.5 Rewriting Interrupt Control Register**.

11.2.3 INTi Interrupt Control Register (INTiIC) (i = 0 to 3)

Address 0055h (INT2IC), 0059h (INT1IC), 005Ah (INT3IC), 005Dh (INT0IC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	POL	IR	ILVL2	ILVL1	ILVL0
After Reset	X	X	0	0	X	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ILVL0	Interrupt priority level select bit	b2 b1 b0 0 0 0: Level 0 (interrupt disabled) 0 0 1: Level 1 0 1 0: Level 2 0 1 1: Level 3 1 0 0: Level 4 1 0 1: Level 5 1 1 0: Level 6 1 1 1: Level 7	R/W
b1	ILVL1			R/W
b2	ILVL2			R/W
b3	IR	Interrupt request bit	0: No interrupt requested 1: Interrupt requested	R/W (1)
b4	POL	Polarity switch bit (3)	0: Falling edge selected 1: Rising edge selected (2)	R/W
b5	—	Reserved bit	Set to 0.	R/W
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is undefined.		—
b7	—			

Notes:
1. Only 0 can be written to the IR bit. Do not write 1 to this bit.
2. If the INTiPL bit in the INTEN register is set to 1 (both edges), set the POL bit to 0 (falling edge selected).
3. The IR bit may be set to 1 (interrupt requested) when the POL bit is rewritten. Refer to **11.9.4 Changing Interrupt Sources**.

Rewrite the interrupt control register when an interrupt request corresponding to the register is not generated. Refer to **11.9.5 Rewriting Interrupt Control Register**.

11.3 Interrupt Control

The following describes enabling and disabling maskable interrupts and setting the acknowledgement priority. This description does not apply to non-maskable interrupts.
Use the I flag in the FLG register, IPL, and bits ILVL2 to ILVL0 in the corresponding interrupt control register to enable or disable a maskable interrupt. Whether an interrupt is requested or not is indicated by the IR bit in the corresponding interrupt control register.

11.3.1 I Flag

The I flag enables or disables maskable interrupts. Setting the I flag to 1 (enabled) enables maskable interrupts. Setting the I flag to 0 (disabled) disables all maskable interrupts.

11.3.2 IR Bit

The IR bit is set to 1 (interrupt requested) when an interrupt request is generated. After the interrupt request is acknowledged and the CPU branches to the corresponding interrupt vector, the IR bit is set to 0 (no interrupt requested).
The IR bit can be set to 0 by a program. Do not write 1 to this bit.
However, the IR bit operations of the timer RC interrupt and the flash memory interrupt are different. Refer to **11.8 Timer RC Interrupt, Flash Memory Interrupt (Interrupts with Multiple Interrupt Request Sources), and Sensor Control Unit Interrupt (Interrupt with Single Interrupt Request Sources)**.

11.3.3 Bits ILVL2 to ILVL0, IPL

Interrupt priority levels can be set using bits ILVL2 to ILVL0.
Table 11.3 lists the Settings of Interrupt Priority Levels and Table 11.4 lists the Interrupt Priority Levels Enabled by IPL.

The following are the conditions when an interrupt is acknowledged:
- I flag = 1
- IR bit = 1
- Interrupt priority level > IPL

The I flag, IR bit, bits ILVL2 to ILVL0, and IPL are independent of each other. They do not affect one another.

Table 11.3 Settings of Interrupt Priority Levels

Bits ILVL2 to ILVL0	Interrupt Priority Level	Priority
000b	Level 0 (interrupt disabled)	—
001b	Level 1	Low
010b	Level 2	
011b	Level 3	
100b	Level 4	
101b	Level 5	
110b	Level 6	
111b	Level 7	High

Table 11.4 Interrupt Priority Levels Enabled by IPL

IPL	Enabled Interrupt Priority Level
000b	Interrupt level 1 and above
001b	Interrupt level 2 and above
010b	Interrupt level 3 and above
011b	Interrupt level 4 and above
100b	Interrupt level 5 and above
101b	Interrupt level 6 and above
110b	Interrupt level 7 and above
111b	All maskable interrupts are disabled

11.3.4 Interrupt Sequence

The following describes an interrupt sequence which is performed from when an interrupt request is acknowledged until the interrupt routine is executed.
When an interrupt request is generated while an instruction is being executed, the CPU determines its interrupt priority level after the instruction is completed. The CPU starts the interrupt sequence from the following cycle. However, for the SMOVB, SMOVF, SSTR, or RMPA instruction, if an interrupt request is generated while the instruction is being executed, the MCU suspends the instruction to start the interrupt sequence. The interrupt sequence is performed as indicated below.
Figure 11.3 shows the Time Required for Executing Interrupt Sequence.

(1) The CPU obtains interrupt information (interrupt number and interrupt request level) by reading address 00000h. The IR bit for the corresponding interrupt is set to 0 (no interrupt requested). (2)
(2) The FLG register is saved to a temporary register (1) in the CPU immediately before entering the interrupt sequence.
(3) The I, D and U flags in the FLG register are set as follows:
The I flag is set to 0 (interrupts disabled).
The D flag is set to 0 (single-step interrupt disabled).
The U flag is set to 0 (ISP selected).
However, the U flag does not change state if an INT instruction for software interrupt number 32 to 63 is executed.
(4) The CPU internal temporary register (1) is saved on the stack.
(5) The PC is saved on the stack.
(6) The interrupt priority level of the acknowledged interrupt is set in the IPL.
(7) The starting address of the interrupt routine set in the interrupt vector is stored in the PC.

After the interrupt sequence is completed, instructions are executed from the starting address of the interrupt routine.

Notes:
1. These registers cannot be accessed by the user.
2. Refer to **11.8 Timer RC Interrupt, Flash Memory Interrupt (Interrupts with Multiple Interrupt Request Sources), and Sensor Control Unit Interrupt (Interrupt with Single Interrupt Request Sources)** for the IR bit operations of the timer RC Interrupt.

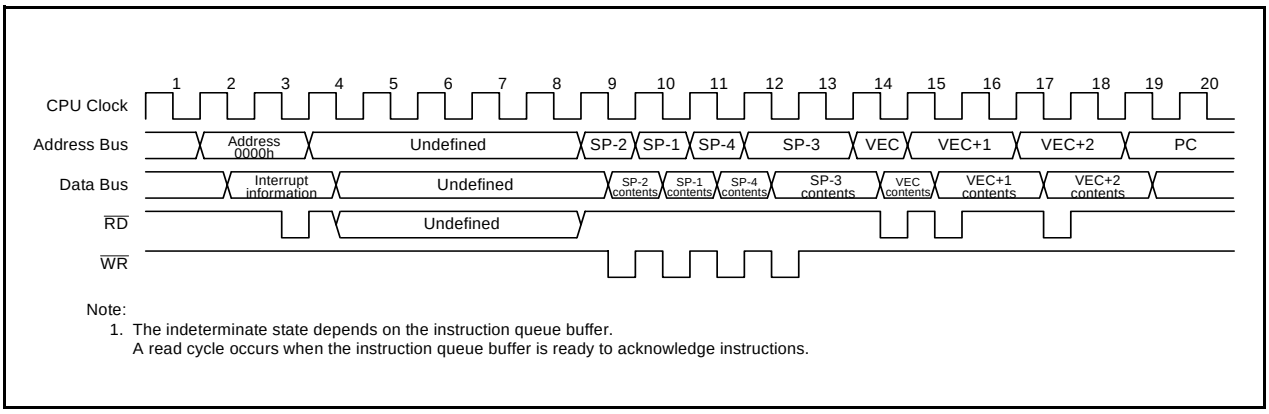
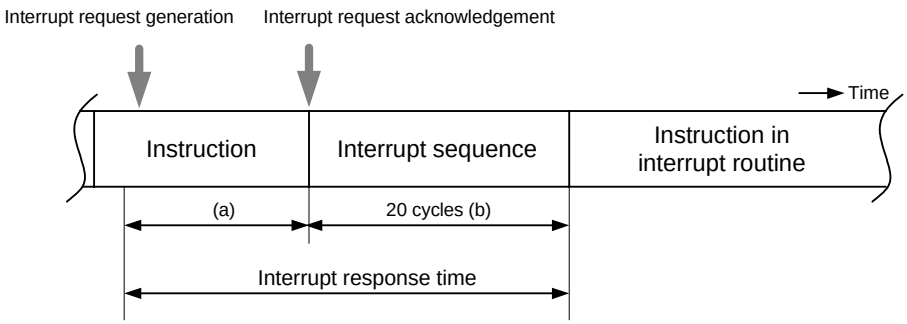


Figure 11.3 Time Required for Executing Interrupt Sequence

11.3.5 Interrupt Response Time

Figure 11.4 shows the Interrupt Response Time. The interrupt response time is the period from when an interrupt request is generated until the first instruction in the interrupt routine is executed. The interrupt response time includes the period from when an interrupt request is generated until the currently executing instruction is completed (refer to (a) in Figure 11.4) and the period required for executing the interrupt sequence (20 cycles, refer to (b) in Figure 11.4).



(a) The period from when an interrupt request is generated until the currently executing instruction is completed. The length of time varies depending on the instruction being executed. The DIVX instruction requires the longest time, 30 cycles (no wait states if the divisor is a register).
(b) 21 cycles for address match and single-step interrupts.

Figure 11.4 Interrupt Response Time

11.3.6 IPL Change when Interrupt Request is Acknowledged

When a maskable interrupt request is acknowledged, the interrupt priority level of the acknowledged interrupt is set in the IPL.
When a software interrupt or special interrupt request is acknowledged, the level listed in Table 11.5 is set in the IPL.
Table 11.5 lists the IPL Value When Software or Special Interrupt is Acknowledged.

Table 11.5 IPL Value When Software or Special Interrupt is Acknowledged

Interrupt Source without Interrupt Priority Level	Value Set in IPL
Watchdog timer, oscillation stop detection, voltage monitor 1, voltage monitor 2, address break	7
Software, address match, single-step	Not changed

11.3.7 Saving Registers

In the interrupt sequence, the FLG register and PC are saved on the stack.
After an extended 16 bits, 4 high-order bits in the PC and 4 high-order (IPL) and 8 low-order bits in the FLG register, are saved on the stack, the 16 low-order bits in the PC are saved.
Figure 11.5 shows the Stack State Before and After Acknowledgement of Interrupt Request.
The other necessary registers should be saved by a program at the beginning of the interrupt routine. The PUSHM instruction can save several registers in the register bank being currently used (1) with a single instruction.

Note:
1. Selectable from registers R0, R1, R2, R3, A0, A1, SB, and FB.

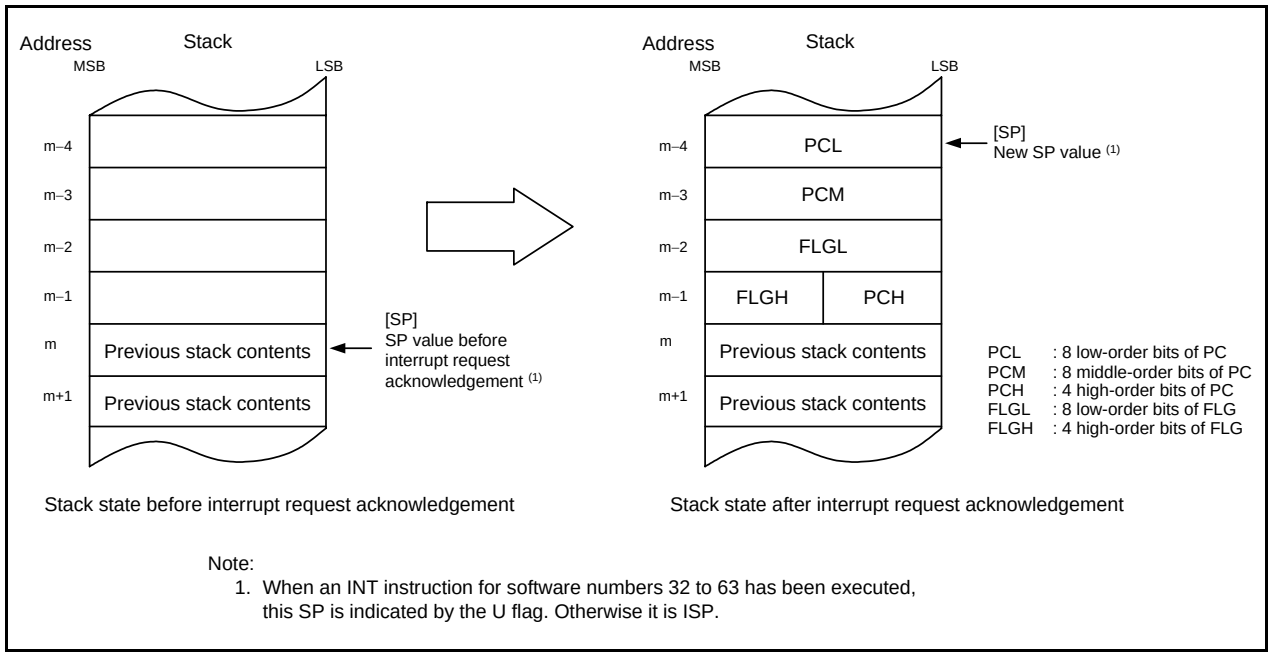
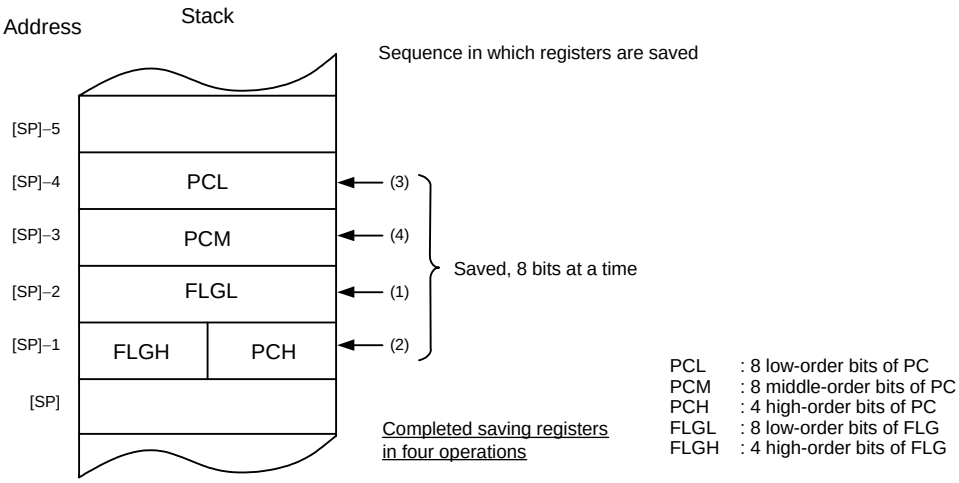


Figure 11.5 Stack State Before and After Acknowledgement of Interrupt Request

The register saving operation, which is performed as part of the interrupt sequence, saved in 8 bits at a time in four steps.
Figure 11.6 shows the Register Saving Operation.



Note:
1. [SP] indicates the SP initial value when an interrupt request is acknowledged.
After registers are saved, the SP content is [SP] minus 4.
When an INT instruction for software numbers 32 to 63 has been executed,
this SP is indicated by the U flag. Otherwise it is ISP.

Figure 11.6 Register Saving Operation

11.3.8 Returning from Interrupt Routine

When the REIT instruction is executed at the end of an interrupt routine, the FLG register and PC, which have been saved on the stack, are automatically restored. The program, that was running before the interrupt request was acknowledged, starts running again.

Registers saved by a program in an interrupt routine should be saved using the POPM instruction or a similar instruction before executing the REIT instruction.

11.3.9 Interrupt Priority

If two or more interrupt requests are generated while a single instruction is being executed, the interrupt with the higher priority is acknowledged.

Set bits ILVL2 to ILVL0 to select any priority level for maskable interrupts (peripheral function). However, if two or more maskable interrupts have the same priority level, their interrupt priority is resolved by hardware, with the higher priority interrupts acknowledged.

The priority of watchdog timer and other special interrupts is set by hardware.

Figure 11.7 shows the Hardware Interrupt Priority.

Software interrupts are not affected by the interrupt priority. If an instruction is executed, the MCU executes the interrupt routine.

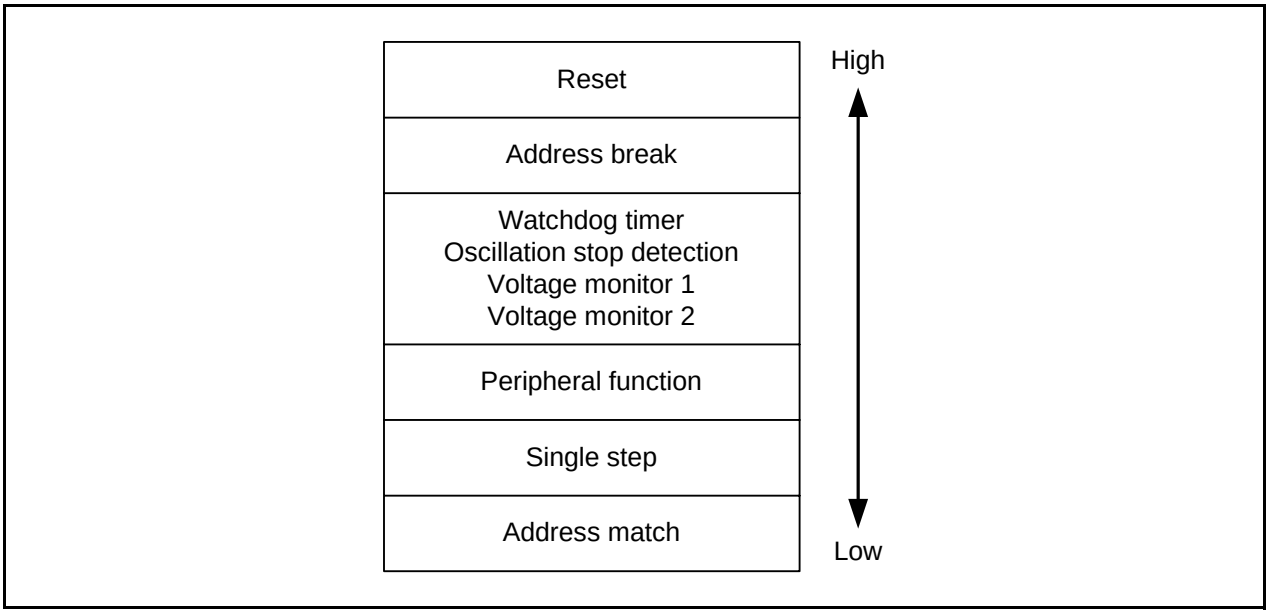


Figure 11.7 Hardware Interrupt Priority

11.3.10 Interrupt Priority Level Selection Circuit

The interrupt priority level selection circuit is used to select the highest priority interrupt. Figure 11.8 shows the Interrupt Priority Level Selection Circuit.

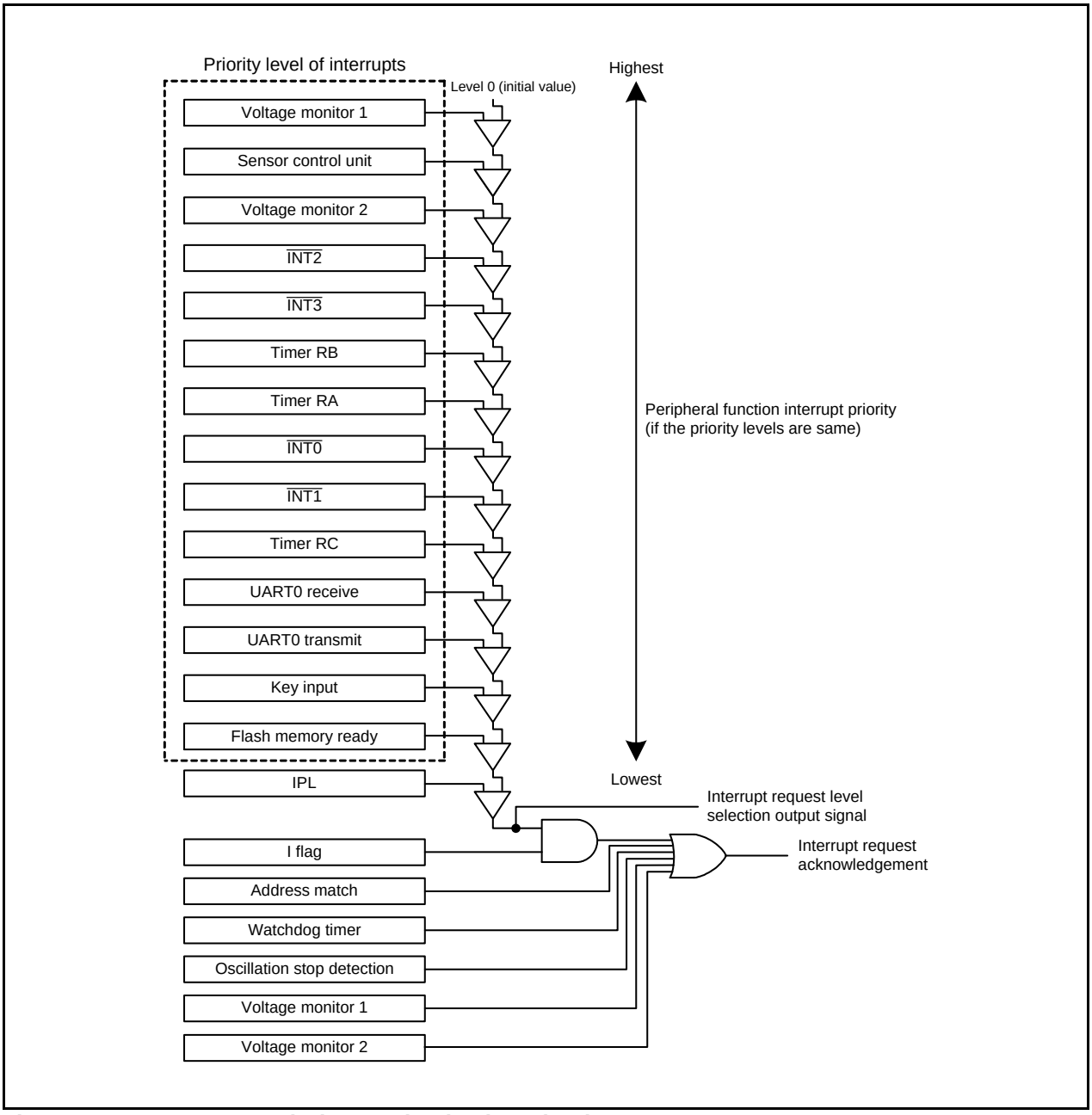


Figure 11.8 Interrupt Priority Level Selection Circuit

11.4 $\overline{\text{INT}}$ Interrupt

11.4.1 $\overline{\text{INTi}}$ Interrupt (i = 0 to 3)

The $\overline{\text{INTi}}$ interrupt is generated by an $\overline{\text{INTi}}$ input. To use the $\overline{\text{INTi}}$ interrupt, set the INTiEN bit in the INTEN register is to 1 (enabled). The edge polarity is selected using the INTiPL bit in the INTEN register and the POL bit in the INTiIC register. The input pins used as the $\overline{\text{INT1}}$ and $\overline{\text{INT3}}$ input can be selected.
Also, inputs can be passed through a digital filter with three different sampling clocks.
The $\overline{\text{INT0}}$ pin is shared with the pulse output forced cutoff input of timer RC, and the external trigger input of timer RB. The $\overline{\text{INT2}}$ pin is shared with the event input enabled of timer RA.
Table 11.6 lists the Pin Configuration of $\overline{\text{INT}}$ Interrupt.

Table 11.6 Pin Configuration of $\overline{\text{INT}}$ Interrupt

Pin Name	Assigned Pin	I/O	Function
$\overline{\text{INT0}}$	P4_5	Input	$\overline{\text{INT0}}$ interrupt input, timer RB external trigger input, timer RC pulse output forced cutoff input
$\overline{\text{INT1}}$	P1_5, P1_7, or P3_5	Input	$\overline{\text{INT1}}$ interrupt input
$\overline{\text{INT2}}$	P3_0 or P3_4	Input	$\overline{\text{INT2}}$ interrupt input, timer RA event input enabled
$\overline{\text{INT3}}$	P3_3 or P3_7	Input	$\overline{\text{INT3}}$ interrupt input

11.4.2 INT Interrupt Input Pin Select Register (INTSR)

Address 018Eh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	INT3SEL0	—	INT2SEL0	INT1SEL2	INT1SEL1	INT1SEL0	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b1	INT1SEL0	$\overline{\text{INT1}}$ pin select bit	b3 b2 b1 0 0 0: P1_7 assigned 0 0 1: P1_5 assigned 1 0 1: P3_5 assigned Other than above: Do not set. ($\overline{\text{INT1}}$ pin not used.)	R/W
b2	INT1SEL1			R/W
b3	INT1SEL2			R/W
b4	INT2SEL0	$\overline{\text{INT2}}$ pin select bit	0: P3_4 assigned 1: P3_0 assigned	R/W
b5	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b6	INT3SEL0	$\overline{\text{INT3}}$ pin select bit	0: P3_3 assigned 1: P3_7 assigned	R/W
b7	—	Reserved bit	Set to 0.	R/W

The INTSR register selects which pin is assigned to the $\overline{\text{INTi}}$ (i = 1 to 3) input. To use $\overline{\text{INTi}}$, set this register.
Set the INTSR register before setting the $\overline{\text{INTi}}$ associated registers. Also, do not change the setting values in this register during $\overline{\text{INTi}}$ operation.

11.4.3 Low-Voltage Signal Mode Control Register (TSMR)

Address 0190h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	I3LVM	I2LVM	I1LVM	I0LVM	—	—	U0LVM	LVMPR
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	LVMPR	Low-voltage signal mode protect bit	0: Write disabled 1: Write enabled (1)	R/W
b1	U0LVM	UART0 low-voltage signal mode control bit (1)	0: Low-voltage signal mode disabled 1: Low-voltage signal mode enabled (2)	R/W
b2	—	Reserved bits	Set to 0.	R/W
b3	—			R/W
b4	I0LVM	$\overline{\text{INT0}}$ low-voltage signal mode control bit (1)	0: Low-voltage signal mode disabled 1: Low-voltage signal mode enabled	R/W
b5	I1LVM	$\overline{\text{INT1}}$ low-voltage signal mode control bit (1)		R/W
b6	I2LVM	$\overline{\text{INT2}}$ low-voltage signal mode control bit (1)		R/W
b7	I3LVM	$\overline{\text{INT3}}$ low-voltage signal mode control bit (1)		R/W

Notes:
1. When the LVMPR bit is set to 1 (write enabled), writing to bits U0LVM and IjLVM (j = 0 to 3) is enabled. Rewrite bits U0LVM and IjLVM (j = 0 to 3) after setting the LVMPR bit to 1. When writing 1 to the LVMPR bit, write 0 and then 1 continuously.
2. When the U0LVM bit is set to 1, the TxD0 pin is set to N-channel open-drain output regardless of the setting of the NCH bit in the U0C0 register.

11.4.4 External Input Enable Register 0 (INTEN)

Address 01FAh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	INT3PL	INT3EN	INT2PL	INT2EN	INT1PL	INT1EN	INT0PL	INT0EN
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	INT0EN	$\overline{INT0}$ input enable bit	0: Disabled 1: Enabled	R/W
b1	INT0PL	$\overline{INT0}$ input polarity select bit (1, 2)	0: One edge 1: Both edges	R/W
b2	INT1EN	$\overline{INT1}$ input enable bit	0: Disabled 1: Enabled	R/W
b3	INT1PL	$\overline{INT1}$ input polarity select bit (1, 2)	0: One edge 1: Both edges	R/W
b4	INT2EN	$\overline{INT2}$ input enable bit	0: Disabled 1: Enabled	R/W
b5	INT2PL	$\overline{INT2}$ input polarity select bit (1, 2)	0: One edge 1: Both edges	R/W
b6	INT3EN	$\overline{INT3}$ input enable bit	0: Disabled 1: Enabled	R/W
b7	INT3PL	$\overline{INT3}$ input polarity select bit (1, 2)	0: One edge 1: Both edges	R/W

Notes:
1. To set the INTiPL bit (i = 0 to 3) to 1 (both edges), set the POL bit in the INTiIC register to 0 (falling edge selected).
2. The IR bit in the INTiIC register may be set to 1 (interrupt requested) if the INTEN register is rewritten. Refer to **11.9.4 Changing Interrupt Sources**.

11.4.5 INT Input Filter Select Register 0 (INTF)

Address 01FCh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	INT3F1	INT3F0	INT2F1	INT2F0	INT1F1	INT1F0	INT0F1	INT0F0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	INT0F0	$\overline{INT0}$ input filter select bit	b1 b0 0 0: No filter 0 1: Filter with f1 sampling 1 0: Filter with f8 sampling 1 1: Filter with f32 sampling	R/W
b1	INT0F1			R/W
b2	INT1F0	$\overline{INT1}$ input filter select bit	b3 b2 0 0: No filter 0 1: Filter with f1 sampling 1 0: Filter with f8 sampling 1 1: Filter with f32 sampling	R/W
b3	INT1F1			R/W
b4	INT2F0	$\overline{INT2}$ input filter select bit	b5 b4 0 0: No filter 0 1: Filter with f1 sampling 1 0: Filter with f8 sampling 1 1: Filter with f32 sampling	R/W
b5	INT2F1			R/W
b6	INT3F0	$\overline{INT3}$ input filter select bit	b7 b6 0 0: No filter 0 1: Filter with f1 sampling 1 0: Filter with f8 sampling 1 1: Filter with f32 sampling	R/W
b7	INT3F1			R/W

11.4.6 $\overline{\text{INTi}}$ Input Filter (i = 0 to 3)

The $\overline{\text{INTi}}$ input contains a digital filter. The sampling clock is selected using bits INTiF1 and INTiF0 in the INTF register. The $\overline{\text{INTi}}$ level is sampled every sampling clock cycle and if the sampled input level matches three times, the IR bit in the INTiIC register is set to 1 (interrupt requested).
Figure 11.9 shows the $\overline{\text{INTi}}$ Input Filter Configuration. Figure 11.10 shows an Operating Example of $\overline{\text{INTi}}$ Input Filter.

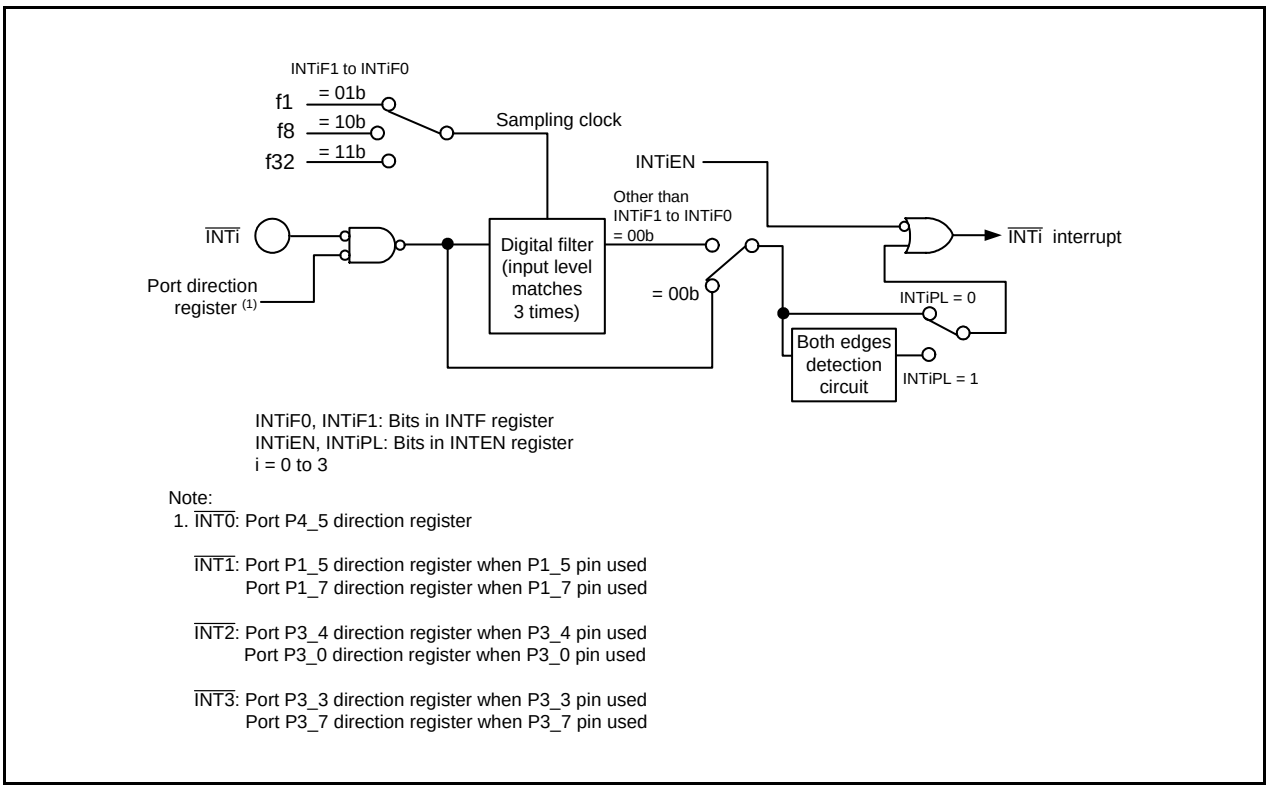


Figure 11.9 $\overline{\text{INTi}}$ Input Filter Configuration

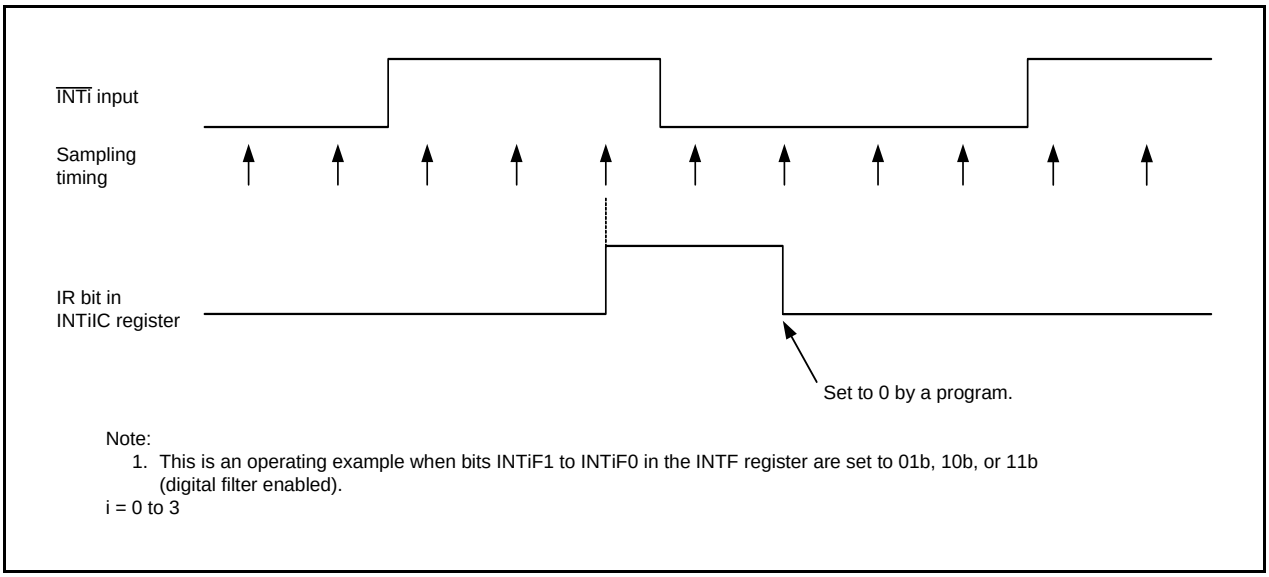


Figure 11.10 Operating Example of $\overline{\text{INTi}}$ Input Filter

11.5 Low-Voltage Signal Mode

Serial interface (UART0) communication and the $\overline{INT}$ input for the $\overline{INT}$ interrupt can be performed using a low-voltage signal. Table 11.7 lists the Pins Usable for Inputting and Outputting Low-Voltage Signal.
Depending on the setting of the TSMR register, the pins enabled for low-voltage signal mode is switched from schmitt input to CMOS input when they are used as input.
Set the input threshold values for CMOS input using registers VLT0 and VLT1.
When low-voltage signal mode is used, all inputs are set to CMOS input. Since schmitt input is disabled, always take countermeasures against noise.

Table 11.7 Pins Usable for Inputting and Outputting Low-Voltage Signal

Peripheral Function Name		Pin
Serial interface	UART0 Clock synchronous serial I/O Clock asynchronous serial I/O	CLK0, RXD0, TXD0
$\overline{INT}$	$\overline{INT0}$ to $\overline{INT3}$	$\overline{INT0}$ to $\overline{INT3}$

11.6 Key Input Interrupt

A key input interrupt request is generated by one of the input edges of pins $\overline{K10}$ to $\overline{K13}$. The key input interrupt can be used as a key-on wake-up function to exit wait or stop mode.

The KIiEN (i = 0 to 3) bit in the KIEN register is be used to select whether or not the pins are used as the $\overline{KIi}$ input. The KIiPL bit in the KIEN register is also be used to select the input polarity.

When inputting "L" to the $\overline{KIi}$ pin, which sets the KIiPL bit to 0 (falling edge), the input to the other pins $\overline{K10}$ to $\overline{K13}$ is not detected as interrupts. When inputting "H" to the $\overline{KIi}$ pin, which sets the KIiPL bit to 1 (rising edge), the input to the other pins $\overline{K10}$ to $\overline{K13}$ is not also detected as interrupts.

Figure 11.11 shows a Block Diagram of Key Input Interrupt. Table 11.8 lists the Pin Configuration of Key Input Interrupt.

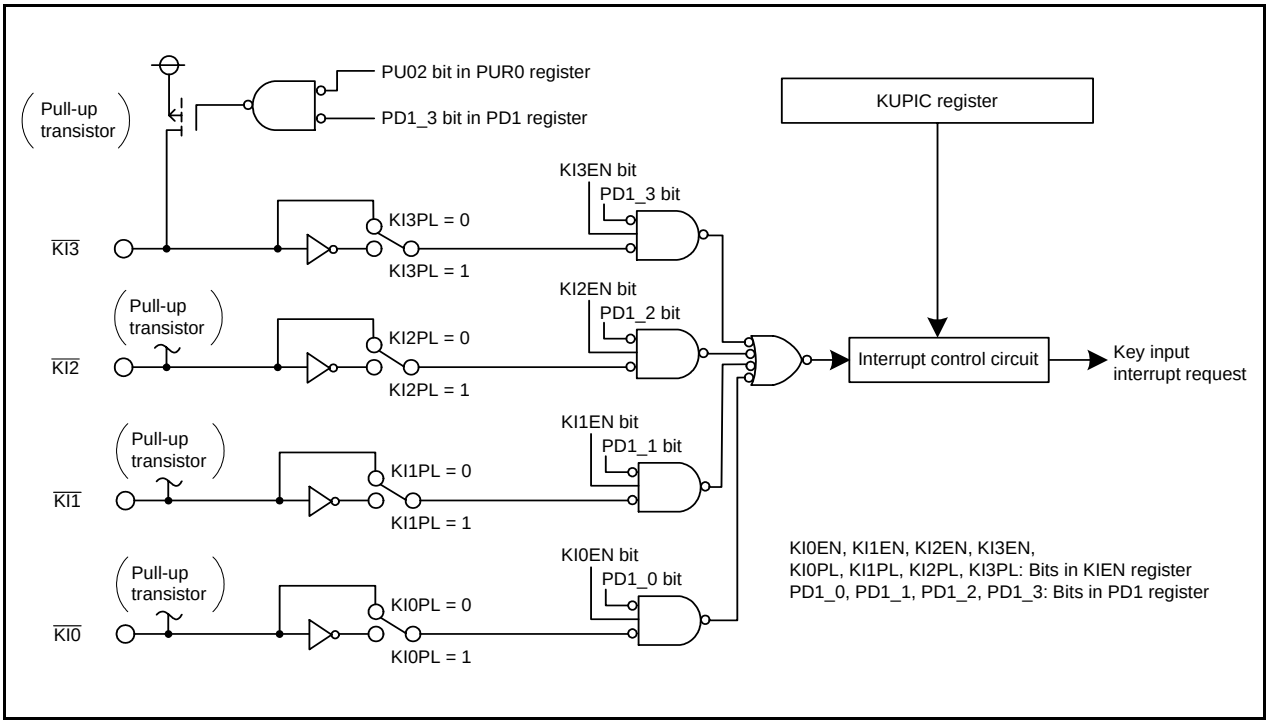


Figure 11.11 Block Diagram of Key Input Interrupt

Table 11.8 Pin Configuration of Key Input Interrupt

Pin Name	I/O	Function
$\overline{KI0}$	Input	$\overline{KI0}$ interrupt input
$\overline{KI1}$	Input	$\overline{KI1}$ interrupt input
$\overline{KI2}$	Input	$\overline{KI2}$ interrupt input
$\overline{KI3}$	Input	$\overline{KI3}$ interrupt input

11.6.1 Key Input Enable Register 0 (KIEN)

Address 01FEh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	KI3PL	KI3EN	KI2PL	KI2EN	KI1PL	KI1EN	KI0PL	KI0EN
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	KI0EN	KI0 input enable bit	0: Disabled 1: Enabled	R/W
b1	KI0PL	KI0 input polarity select bit	0: Falling edge 1: Rising edge	R/W
b2	KI1EN	KI1 input enable bit	0: Disabled 1: Enabled	R/W
b3	KI1PL	KI1 input polarity select bit	0: Falling edge 1: Rising edge	R/W
b4	KI2EN	KI2 input enable bit	0: Disabled 1: Enabled	R/W
b5	KI2PL	KI2 input polarity select bit	0: Falling edge 1: Rising edge	R/W
b6	KI3EN	KI3 input enable bit	0: Disabled 1: Enabled	R/W
b7	KI3PL	KI3 input polarity select bit	0: Falling edge 1: Rising edge	R/W

The IR bit in the KUPIC register may be set to 1 (interrupt requested) when the KIEN register is rewritten. Refer to **11.9.4 Changing Interrupt Sources**.

11.7 Address Match Interrupt

An address match interrupt request is generated immediately before execution of the instruction at the address indicated by the RMADi register (i = 0 or 1). This interrupt is used as a break function by the debugger. When the on-chip debugger is used, do not set an address match interrupt (registers AIER0, AIER1, RMAD0, and RMAD1, and fixed vector tables) in the user system.

Set the starting address of any instruction in the RMADi register (i = 0 or 1). The AIERi0 bit in the AIERi register can be used to select enable or disable the interrupt. The address match interrupt is not affected by the I flag and IPL.

The PC value (refer to **11.3.7 Saving Registers**) which is saved on the stack when an address match interrupt request is acknowledged varies depending on the instruction at the address indicated by the RMADi register. (The appropriate return address is not saved on the stack.) When returning from the address match interrupt, follow one of the following means:

- Rewrite the contents of the stack and use the REIT instruction to return.
- Use an instruction such as POP to restore the stack to its previous state before the interrupt request was acknowledged. Then use a jump instruction to return.

Table 11.9 lists the PC Value Saved on Stack When Address Match Interrupt Request is Acknowledged and Table 11.10 lists the Correspondence Between Address Match Interrupt Sources and Associated Registers.

Table 11.9 PC Value Saved on Stack When Address Match Interrupt Request is Acknowledged

Address Indicated by RMADi Register (i = 0 or 1)	PC Value Saved (1)
• Instruction with 2-byte operation code (2) • Instruction with 1-byte operation code (2) ADD.B:S #IMM8,dest SUB.B:S #IMM8,dest AND.B:S #IMM8,dest OR.B:S #IMM8,dest MOV.B:S #IMM8,dest STZ #IMM8,dest STNZ #IMM8,dest STZX #IMM81,#IMM82,dest CMP.B:S #IMM8,dest PUSHM src POPM dest JMPS #IMM8 JSRS #IMM8 MOV.B:S #IMM,dest (however, dest = A0 or A1)	Address indicated by RMADi register + 2
• Instructions other than above	Address indicated by RMADi register + 1

Notes:
1. Refer to the **11.3.7 Saving Registers**.
2. Operation code: Refer to the **R8C/Tiny Series Software Manual** (REJ09B0001). **Chapter 4. Instruction Code/Number of Cycles** contains diagrams showing operation code below each syntax. Operation code is shown in the bold frame in the diagrams.

Table 11.10 Correspondence Between Address Match Interrupt Sources and Associated Registers

Address Match Interrupt Source	Address Match Interrupt Enable Bit	Address Match Interrupt Register
Address match interrupt 0	AIER00	RMAD0
Address match interrupt 1	AIER10	RMAD1

11.7.1 Address Match Interrupt Enable Register i (AIERi) (i = 0 or 1)

Address 01C3h (AIER0), 01C7h (AIER1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0	
Symbol	—	—	—	—	—	—	—	AIER00	AIER0 register
After Reset	0	0	0	0	0	0	0	0	

Symbol	—	—	—	—	—	—	—	AIER10	AIER1 register
After Reset	0	0	0	0	0	0	0	0	

Bit	Symbol	Bit Name	Function	R/W
b0	AIERi0	Address match interrupt i enable bit	0: Disabled 1: Enabled	R/W
b1	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b2	—			
b3	—			
b4	—			
b5	—			
b6	—			
b7	—			

11.7.2 Address Match Interrupt Register i (RMADi) (i = 0 or 1)

Address 01C2h to 01C0h (RMAD0), 01C6h to 01C4h (RMAD1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	b23	b22	b21	b20	b19	b18	b17	b16
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	X	X	X	X

Bit	Symbol	Function	Setting Range	R/W
b19 to b0	—	Address setting register for address match interrupt	00000h to FFFFFh	R/W
b20	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b21	—			
b22	—			
b23	—			

11.8 Timer RC Interrupt, Flash Memory Interrupt (Interrupts with Multiple Interrupt Request Sources), and Sensor Control Unit Interrupt (Interrupt with Single Interrupt Request Sources)

The timer RC interrupt and flash memory interrupt each have multiple interrupt request sources. An interrupt request is generated by the logical OR of several interrupt request sources and is reflected in the IR bit in the corresponding interrupt control register. Therefore, each of these peripheral functions has its own interrupt request source status register (status register) and interrupt request source enable register (enable register) to control the generation of interrupt requests (change of the IR bit in the interrupt control register).
The Sensor Control Unit interrupt has single interrupt request sources. An interrupt request is generated by the logical OR of several interrupt request sources and is reflected in the IR bit in the corresponding interrupt control register.
Therefore, Sensor Control Unit has its own interrupt request source status register (status register) and interrupt request source enable register (enable register) to control the generation of interrupt requests (change of the IR bit in the interrupt control register).
Table 11.11 lists the Registers Associated with Timer RC Interrupt, Sensor Control Unit Interrupt, and Flash Memory Interrupt.

Table 11.11 Registers Associated with Timer RC Interrupt, Sensor Control Unit Interrupt, and Flash Memory Interrupt

Peripheral Function Name	Status Register of Interrupt Request Source	Enable Register of Interrupt Request Source	Interrupt Control Register
Timer RC	TRCSR	TRCIER	TRCIC
Sensor Control Unit	SIF	SCUIE	SCUIC
Flash memory	RDYSTI	RDYSTIE	FMRDYIC
	BSYAEI	BSYAEIE	
		CMDERIE	

As with other maskable interrupts, the timer RC interrupt and flash memory interrupt are controlled by the combination of the I flag, IR bit, bits ILVL0 to ILVL2, and IPL. However, since each interrupt source is generated by a combination of multiple interrupt request sources, the following differences from other maskable interrupts apply:

- When bits in the enable register are set to 1 and the corresponding bits in the status register are set to 1 (interrupt enabled), the IR bit in the interrupt control register is set to 1 (interrupt requested).
- When either bits in the status register or the corresponding bits in the enable register, or both are set to 0, the IR bit is set to 0 (no interrupt requested).
  That is, even if the interrupt is not acknowledged after the IR bit is set to 1, the interrupt request will not be retained.
  Also, the IR bit is not set to 0 even if 0 is written to this bit.
- Individual bits in the status register are not automatically set to 0 even if the interrupt is acknowledged.
  The IR bit is also not automatically set to 0 when the interrupt is acknowledged.
  Set individual bits in the status register to 0 in the interrupt routine. Refer to the status register figure for how to set individual bits in the status register to 0.
- When multiple bits in the enable register are set to 1 and other request sources are generated after the IR bit is set to 1, the IR bit remains 1.
- When multiple bits in the enable register are set to 1, use the status register to determine which request source causes an interrupt.

Refer to chapters of the individual peripheral functions (**19. Timer RC** and **22. Flash Memory**) for the status register and enable register.
For the interrupt control register, refer to **11.3 Interrupt Control**.

11.9 Notes on Interrupts

11.9.1 Reading Address 00000h

Do not read address 00000h by a program. When a maskable interrupt request is acknowledged, the CPU reads interrupt information (interrupt number and interrupt request level) from 00000h in the interrupt sequence. At this time, the IR bit for the acknowledged interrupt is set to 0.
If address 00000h is read by a program, the IR bit for the interrupt which has the highest priority among the enabled interrupts is set to 0. This may cause the interrupt to be canceled, or an unexpected interrupt to be generated.

11.9.2 SP Setting

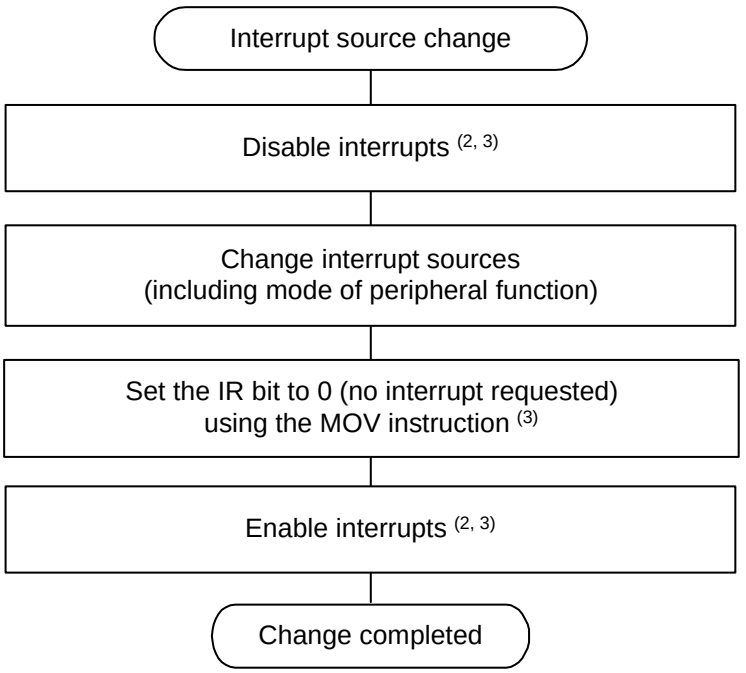
Set a value in the SP before an interrupt is acknowledged. The SP is set to 0000h after a reset. If an interrupt is acknowledged before setting a value in the SP, the program may run out of control.

11.9.3 External Interrupt and Key Input Interrupt

Either the “L” level width or “H” level width shown in the Electrical Characteristics is required for the signal input to pins $\overline{\text{INT0}}$ to $\overline{\text{INT3}}$ and pins $\overline{\text{KI0}}$ to $\overline{\text{KI3}}$, regardless of the CPU clock.
For details, refer to **Table 24.16** (VCC = 5 V), **Table 24.22** (VCC = 3 V), **Table 24.28** (VCC = 2.2 V) **External Interrupt $\overline{\text{INT}}$i (i = 0 to 3) Input, Key Input Interrupt $\overline{\text{KI}}$i (i = 0 to 3)**.

11.9.4 Changing Interrupt Sources

The IR bit in the interrupt control register may be set to 1 (interrupt requested) when the interrupt source changes. To use an interrupt, set the IR bit to 0 (no interrupt requested) after changing interrupt sources.
Changing interrupt sources as referred to here includes all factors that change the source, polarity, or timing of the interrupt assigned to a software interrupt number. Therefore, if a mode change of a peripheral function involves the source, polarity, or timing of an interrupt, set the IR bit to 0 (no interrupt requested) after making these changes. Refer to the descriptions of the individual peripheral functions for related interrupts.
Figure 11.12 shows a Procedure Example for Changing Interrupt Sources.



IR bit: The interrupt control register bit for the interrupt whose source is to be changed

Notes:
1. The above settings must be executed individually. Do not execute two or more settings simultaneously (using one instruction).
2. To prevent interrupt requests from being generated disable the peripheral function before changing the interrupt source. In this case, use the I flag if all maskable interrupts can be disabled.
   If all maskable interrupts cannot be disabled, use bits ILVL0 to ILVL2 for the interrupt whose source is to be changed.
3. To change the interrupt source to the input with the digital filter used, wait for three or more cycles of the sampling clock of the digital filter before setting the IR bit to 0 (no interrupt requested). Refer to **11.9.5 Rewriting Interrupt Control Register** for the instructions to use and related notes.

Figure 11.12 Procedure Example for Changing Interrupt Sources

11.9.5 Rewriting Interrupt Control Register

(a) The contents of the interrupt control register can be rewritten only while no interrupt requests corresponding to that register are generated. If an interrupt request may be generated, disable the interrupt before rewriting the contents of the interrupt control register.

(b) When rewriting the contents of the interrupt control register after disabling the interrupt, be careful to choose appropriate instructions.
Changing any bit other than the IR bit
If an interrupt request corresponding to the register is generated while executing the instruction, the IR bit may not be set to 1 (interrupt requested), and the interrupt may be ignored. If this causes a problem, use one of the following instructions to rewrite the contents of the register: AND, OR, BCLR, and BSET.

Changing the IR bit
Depending on the instruction used, the IR bit may not be set to 0 (no interrupt requested).
Use the MOV instruction to set the IR bit to 0.

(c) When using the I flag to disable an interrupt, set the I flag as shown in the sample programs below. Refer to (b) regarding rewriting the contents of interrupt control registers using the sample programs.

Examples 1 to 3 show how to prevent the I flag from being set to 1 (interrupts enabled) before the contents of the interrupt control register are rewritten for the effects of the internal bus and the instruction queue buffer.

Example 1: Use the NOP instructions to pause program until the interrupt control register is rewritten

```
INT_SWITCH1:
    FCLR    I               ; Disable interrupts
    AND.B   #00H, 0056H     ; Set the TRAIC register to 00h
    NOP
    NOP
    FSET    I               ; Enable interrupts
```

Example 2: Use a dummy read to delay the FSET instruction

```
INT_SWITCH2:
    FCLR    I               ; Disable interrupts
    AND.B   #00H, 0056H     ; Set the TRAIC register to 00h
    MOV.W   MEM,R0          ; Dummy read
    FSET    I               ; Enable interrupts
```

Example 3: Use the POPC instruction to change the I flag

```
INT_SWITCH3:
    PUSHC   FLG
    FCLR    I               ; Disable interrupts
    AND.B   #00H, 0056H     ; Set the TRAIC register to 00h
    POPC    FLG             ; Enable interrupts
```

12. ID Code Areas

The ID code areas are used to implement a function that prevents the flash memory from being rewritten in standard serial I/O mode. This function prevents the flash memory from being read, rewritten, or erased.

12.1 Overview

The ID code areas are assigned to 0FFDFh, 0FFE3h, 0FFEBh, 0FFEFh, 0FFF3h, 0FFF7h, and 0FFFBh of the respective vector highest-order addresses of the fixed vector table. Figure 12.1 shows the ID Code Areas.

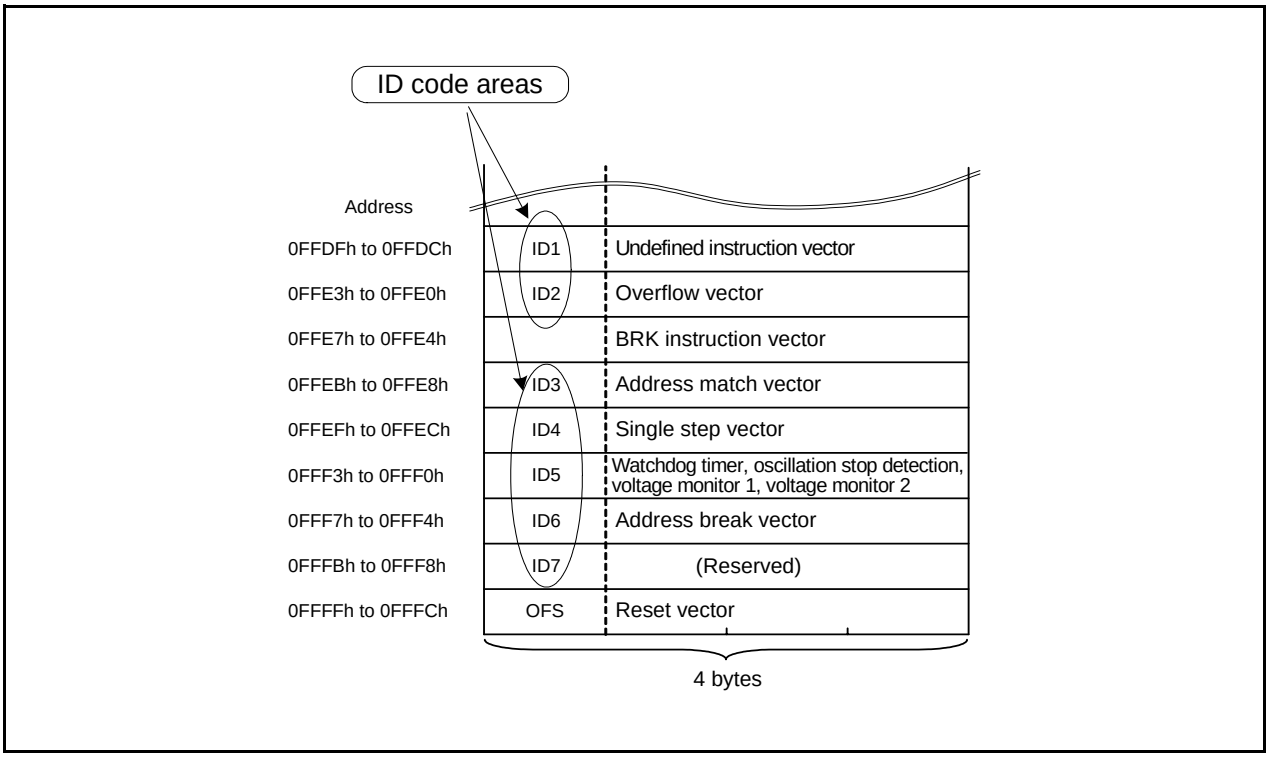


Figure 12.1 ID Code Areas

12.2 Functions

The ID code areas are used in standard serial I/O mode. Unless 3 bytes (addresses 0FFFCh to 0FFFEh) of the reset vector are set to FFFFFFh, the ID codes stored in the ID code areas and the ID codes sent from the serial programmer or the on-chip debugging emulator are checked to see if they match. If the ID codes match, the commands sent from the serial programmer or the on-chip debugging emulator are acknowledged. If the ID codes do not match, the commands are not acknowledged. To use the serial programmer or the on-chip debugging emulator, first write predetermined ID codes to the ID code areas.
If 3 bytes (addresses 0FFFCh to 0FFFEh) of the reset vector are set to FFFFFFh, the ID codes are not checked and all commands are accepted.

The ID code areas are allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.

The character sequence of the ASCII codes “ALeRASE” is the reserved word used for the forced erase function. The character sequence of the ASCII codes “Protect” is the reserved word used for the standard serial I/O mode disabled function. Table 12.1 lists the ID Code Reserved Word. The reserved word is a set of reserved characters when all the addresses and data in the ID code storage addresses sequentially match Table 12.1. When the forced erase function or standard serial I/O mode disabled function is not used, use another character sequence of the ASCII codes.

Table 12.1 ID Code Reserved Word

ID Code Storage Address		ID Code Reserved Word (ASCII) (1)	
		ALeRASE	Protect
0FFDFh	ID1	41h (upper-case “A”)	50h (upper-case “P”)
0FFE3h	ID2	4Ch (upper-case “L”)	72h (lower-case “r”)
0FFEBh	ID3	65h (lower-case “e”)	6Fh (lower-case “o”)
0FFEFh	ID4	52h (upper-case “R”)	74h (lower-case “t”)
0FFF3h	ID5	41h (upper-case “A”)	65h (lower-case “e”)
0FFF7h	ID6	53h (upper-case “S”)	63h (lower-case “c”)
0FFFBh	ID7	45h (upper-case “E”)	74h (lower-case “t”)

Note:
1. Reserve word: A set of characters when all the addresses and data in the ID code storage addresses sequentially match Table 12.1.

12.3 Forced Erase Function

This function is used in standard serial I/O mode. When the ID codes sent from the serial programmer or the on-chip debugging emulator are “ALeRASE” in ASCII code, the content of the user ROM area will be erased at once. However, if the contents of the ID code addresses are set to other than “ALeRASE” (other than **Table 12.1 ID Code Reserved Word**) when the ROMCR bit in the OFS register is set to 1 and the ROMCP1 bit is set to 0 (ROM code protect enabled), forced erasure is not executed and the ID codes are checked with the ID code check function. Table 12.2 lists the Conditions and Operations of Forced Erase Function.
Also, when the contents of the ID code addresses are set to “ALeRASE” in ASCII code, if the ID codes sent from the serial programmer or the on-chip debugging emulator are “ALeRASE”, the content of the user ROM area will be erased. If the ID codes sent from the serial programmer are other than “ALeRASE”, the ID codes do not match and no command is acknowledged, thus the user ROM area remains protected.

Table 12.2 Conditions and Operations of Forced Erase Function

Condition			Operation
ID code from serial programmer or the on-chip debugging emulator	ID code in ID code storage address	Bits ROMCP1 and ROMCR in OFS register	
ALeRASE	ALeRASE	—	All erasure of user ROM area (forced erase function)
	Other than ALeRASE (1)	Other than 01b (ROM code protect disabled)	
		01b (ROM code protect enabled)	ID code check (ID code check function)
Other than ALeRASE	ALeRASE	—	ID code check (ID code check function. No ID code match.)
	Other than ALeRASE (1)	—	ID code check (ID code check function)

Note:
1. For “Protect”, refer to **12.4 Standard Serial I/O Mode Disabled Function**.

12.4 Standard Serial I/O Mode Disabled Function

This function is used in standard serial I/O mode. When the I/D codes in the ID code storage addresses are set to the reserved character sequence of the ASCII codes “Protect” (refer to **Table 12.1 ID Code Reserved Word**), communication with the serial programmer or the on-chip debugging emulator is not performed. This does not allow the flash memory to be read, rewritten, or erased using the serial programmer or the on-chip debugging emulator.
Also, if the ID codes are also set to the reserved character sequence of the ASCII codes “Protect” when the ROMCR bit in the OFS register is set to 1 and the ROMCP1 bit is set to 0 (ROM code protect enabled), ROM code protection cannot be disabled using the serial programmer or the on-chip debugging emulator. This prevents the flash memory from being read, rewritten, or erased using the serial programmer, the on-chip debugging emulator, or parallel programmer.

12.5 Notes on ID Code Areas

12.5.1 Setting Example of ID Code Areas

The ID code areas are allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program. The following shows a setting example.

- To set 55h in all of the ID code areas

```
.org 00FFDCH
.lword dummy | (55000000h)   ; UND
.lword dummy | (55000000h)   ; INTO
.lword dummy; BREAK
.lword dummy | (55000000h)   ; ADDRESS MATCH
.lword dummy | (55000000h)   ; SET SINGLE STEP
.lword dummy | (55000000h)   ; WDT
.lword dummy | (55000000h)   ; ADDRESS BREAK
.lword dummy | (55000000h)   ; RESERVE
```

(Programming formats vary depending on the compiler. Check the compiler manual.)

13. Option Function Select Area

13.1 Overview

The option function select area is used to select the MCU state after a reset, the function to prevent rewriting in parallel I/O mode, or the watchdog timer operation. The reset vector highest-order-address, 0FFFFh and 0FFDBh, are assigned as the option function select area. Figure 13.1 shows the Option Function Select Area.

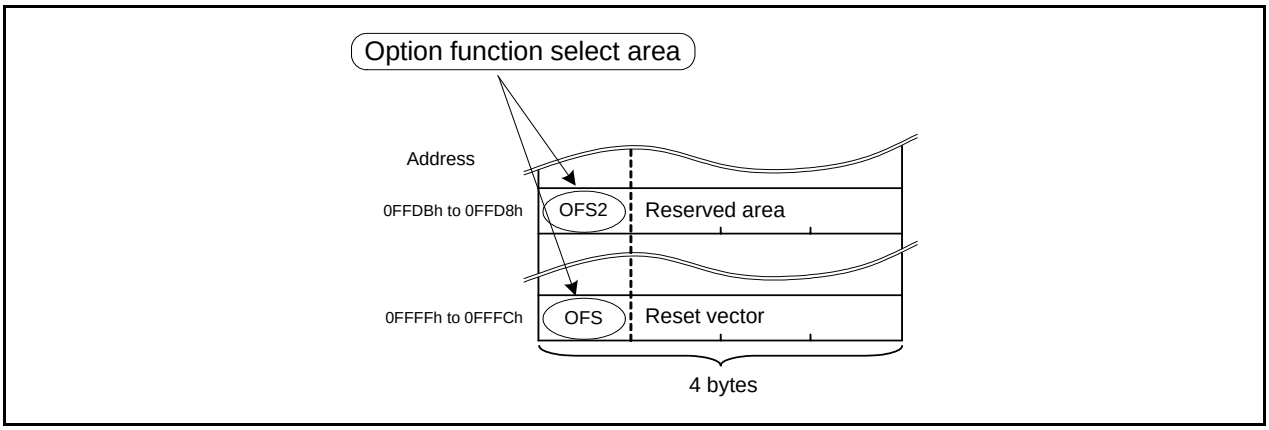


Figure 13.1 Option Function Select Area

13.2 Registers

Registers OFS and OFS2 are used to select the MCU state after a reset, the function to prevent rewriting in parallel I/O mode, or the watchdog timer operation.

13.2.1 Option Function Select Register (OFS)

Address 0FFFFh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CSPROINI	LVDAS	VDSEL1	VDSEL0	ROMCP1	ROMCR	—	WDTON
After Reset	User Setting Value (1)							

Bit	Symbol	Bit Name	Function	R/W
b0	WDTON	Watchdog timer start select bit	0: Watchdog timer automatically starts after reset. 1: Watchdog timer is stopped after reset.	R/W
b1	—	Reserved bit	Set to 1.	R/W
b2	ROMCR	ROM code protect disable bit	0: ROM code protect disabled 1: ROMCP1 bit enabled	R/W
b3	ROMCP1	ROM code protect bit	0: ROM code protect enabled 1: ROM code protect disabled	R/W
b4	VDSEL0	Voltage detection 0 level select bit (2)	b5 b4 0 0: 3.80 V selected (Vdet0_3) 0 1: 2.85 V selected (Vdet0_2) 1 0: 2.35 V selected (Vdet0_1) 1 1: 1.90 V selected (Vdet0_0)	R/W
b5	VDSEL1			R/W
b6	LVDAS	Voltage detection 0 circuit start bit (3)	0: Voltage monitor 0 reset enabled after reset 1: Voltage monitor 0 reset disabled after reset	R/W
b7	CSPROINI	Count source protection mode after reset select bit	0: Count source protect mode enabled after reset 1: Count source protect mode disabled after reset	R/W

Notes:

1. The OFS register is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not write additions to the OFS register. If the block including the OFS register is erased, the OFS register is set to FFh.
   When blank products are shipped, the OFS register is set to FFh. It is set to the written value after written by the user.
   When factory-programming products are shipped, the value of the OFS register is the value programmed by the user.
2. The same level of the voltage detection 0 level selected by bits VDSEL0 and VDESL1 is set in both functions of voltage monitor 0 reset and power-on reset.
3. To use power-on reset and voltage monitor 0 reset, set the LVDAS bit to 0 (voltage monitor 0 reset enabled after reset).

For a setting example of the OFS register, refer to **13.3.1 Setting Example of Option Function Select Area**.

LVDAS Bit (Voltage Detection 0 Circuit Start Bit)

The Vdet0 voltage to be monitored by the voltage detection 0 circuit is selected by bits VDSEL0 and VDSEL1.

13.2.2 Option Function Select Register 2 (OFS2)

Address 0FFDBh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	WDTRCS1	WDTRCS0	WDTUFS1	WDTUFS0
After Reset	User Setting Value (1)							

Bit	Symbol	Bit Name	Function	R/W
b0	WDTUFS0	Watchdog timer underflow period set bit	b1 b0 0 0: 03FFh 0 1: 0FFFh 1 0: 1FFFh 1 1: 3FFFh	R/W
b1	WDTUFS1			R/W
b2	WDTRCS0	Watchdog timer refresh acknowledgement period set bit	b3 b2 0 0: 25% 0 1: 50% 1 0: 75% 1 1: 100%	R/W
b3	WDTRCS1			R/W
b4	—	Reserved bits	Set to 1.	R/W
b5	—			
b6	—			
b7	—			

Note:

1. The OFS2 register is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not write additions to the OFS2 register. If the block including the OFS2 register is erased, the OFS2 register is set to FFh.
   When blank products are shipped, the OFS2 register is set to FFh. It is set to the written value after written by the user.
   When factory-programming products are shipped, the value of the OFS2 register is the value programmed by the user.

   For a setting example of the OFS2 register, refer to **13.3.1 Setting Example of Option Function Select Area**.

Bits WDTRCS0 and WDTRCS1 (Watchdog Timer Refresh Acknowledgement Period Set Bit)

Assuming that the period from when the watchdog timer starts counting until it underflows is 100%, the refresh acknowledgement period for the watchdog timer can be selected.
For details, refer to **14.3.1.1 Refresh Acknowledgment Period**.

13.3 Notes on Option Function Select Area

13.3.1 Setting Example of Option Function Select Area

The option function select area is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program. The following shows a setting example.

- To set FFh in the OFS register

```
.org 00FFFCH
.lword reset | (0FF000000h)     ; RESET
```

(Programming formats vary depending on the compiler. Check the compiler manual.)

- To set FFh in the OFS2 register

```
.org 00FFDBH
.byte 0FFh
```

(Programming formats vary depending on the compiler. Check the compiler manual.)

14. Watchdog Timer

The watchdog timer is a function that detects when a program is out of control. Use of the watchdog timer is recommended to improve the reliability of the system.

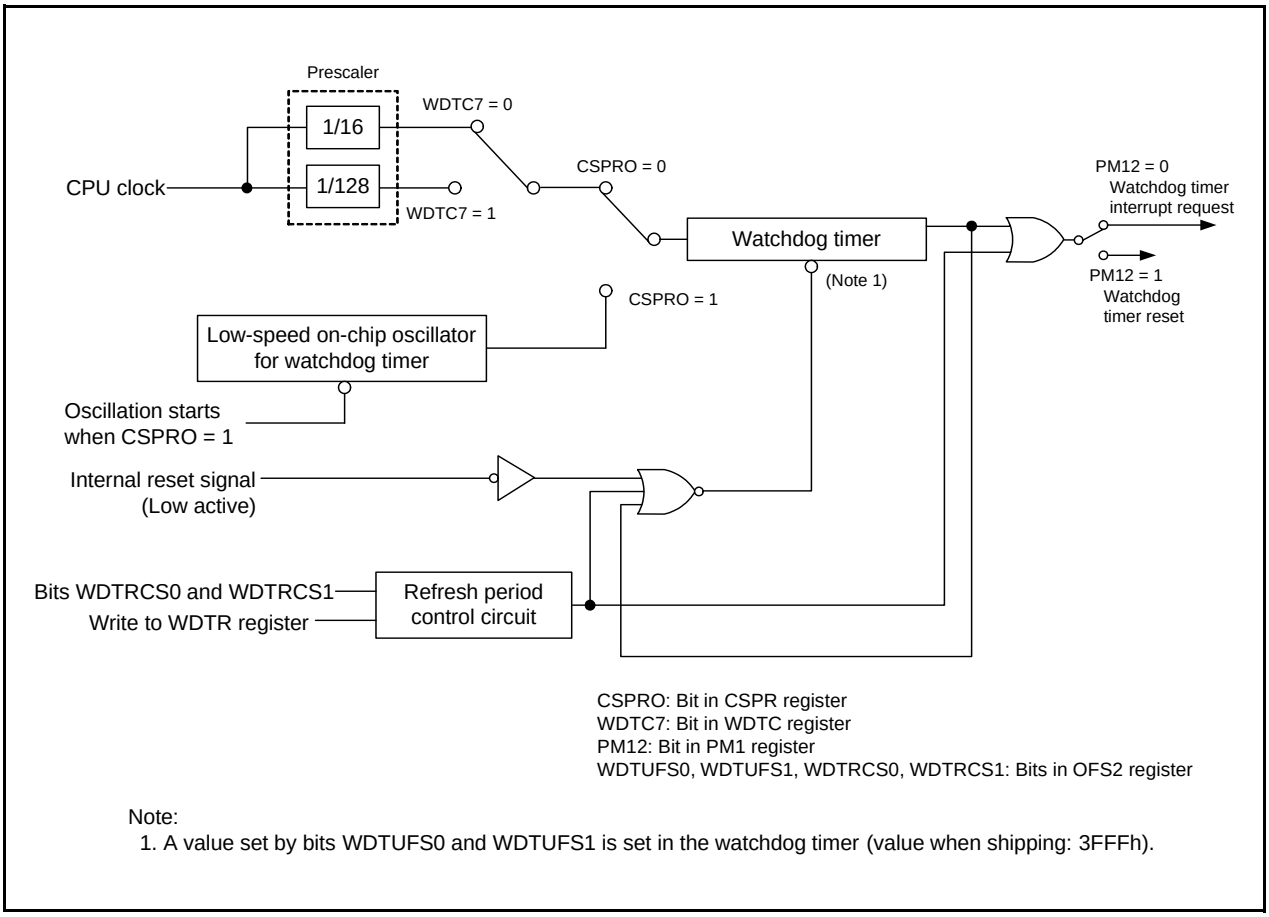
14.1 Overview

The watchdog timer contains a 14-bit counter and allows selection of count source protection mode enable or disable.
Table 14.1 lists the Watchdog Timer Specifications.
Refer to **5.5 Watchdog Timer Reset** for details of the watchdog timer reset.
Figure 14.1 shows a Watchdog Timer Block Diagram.

Table 14.1 Watchdog Timer Specifications

Item	Count Source Protection Mode Disabled	Count Source Protection Mode Enabled
Count source	CPU clock	Low-speed on-chip oscillator clock for the watchdog timer
Count operation	Decrement	
Count start condition	Either of the following can be selected: • After a reset, count starts automatically. • Count starts by writing to the WDTS register.	
Count stop condition	Stop mode, wait mode	None
Watchdog timer initialization conditions	• Reset • Write 00h and then FFh to the WDTR register (with acknowledgement period setting). (1) • Underflow	
Operations at underflow	Watchdog timer interrupt or watchdog timer reset	Watchdog timer reset
Selectable functions	• Division ratio of the prescaler Selected by the WDTC7 bit in the WDTC register. • Count source protection mode Whether count source protection mode is enabled or disabled after a reset can be selected by the CSPROINI bit in the OFS register (flash memory). If count source protection mode is disabled after a reset, it can be enabled or disabled by the CSPRO bit in the CSPR register (program). • Start or stop of the watchdog timer after a reset Selected by the WDTON bit in the OFS register (flash memory). • Initial value of the watchdog timer Selectable by bits WDTUFS0 and WDTUFS1 in the OFS2 register. • Refresh acknowledgement period for the watchdog timer Selectable by bits WDTRCS0 and WDTRCS1 in the OFS2 register.	

Note:
1. Write the WDTR register during the count operation of the watchdog timer.



Note:
1. A value set by bits WDTUFS0 and WDTUFS1 is set in the watchdog timer (value when shipping: 3FFFh).

Figure 14.1 Watchdog Timer Block Diagram

14.2 Registers

14.2.1 Processor Mode Register 1 (PM1)

Address 0005h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	PM12	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved bits	Set to 0.	R/W
b1	—			
b2	PM12	WDT interrupt/reset switch bit	0: Watchdog timer interrupt 1: Watchdog timer reset (1)	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	—			
b5	—			
b6	—			
b7	—	Reserved bit	Set to 0.	R/W

Note:
1. The PM12 bit is set to 1 when 1 is written by a program (and remains unchanged even if 0 is written to it). This bit is automatically set to 1 when the CSPRO bit in the CSPR register is set to 1 (count source protection mode enabled).

Set the PRC1 bit in the PRCR register to 1 (write enabled) before rewriting the PM1 register.

14.2.2 Watchdog Timer Reset Register (WDTR)

Address 000Dh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	Function	R/W
b7 to b0	Writing 00h and then FFh to this register initializes the watchdog timer. The initial value of the watchdog timer is specified by bits WDTUFS0 and WDTUF1 in the OFS2 register. (1)	W

Note:
1. Write the WDTR register during the count operation of the watchdog timer.

14.2.3 Watchdog Timer Start Register (WDTS)

Address 000Eh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	Function	R/W
b7 to b0	A write instruction to this register starts the watchdog timer.	W

14.2.4 Watchdog Timer Control Register (WDTC)

Address 000Fh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	WDTC7	—	—	—	—	—	—	—
When Shipping	0	0	1	1	1	1	1	1

Bit	Symbol	Bit Name	Function	R/W
b0	—	The following bits of the watchdog timer can be read. When bits WDTUFS1 to WDTUFS0 in the OFS2 register are 00b (03FFh): b5 to b0 01b (0FFFh): b7 to b2 10b (1FFFh): b8 to b3 11b (3FFFh): b9 to b4		R
b1	—			R
b2	—			R
b3	—			R
b4	—			R
b5	—			R
b6	—	Reserved bit	When read, the content is 0.	R
b7	WDTC7	Prescaler select bit	0: Divided-by-16 1: Divided-by-128	R/W

14.2.5 Count Source Protection Mode Register (CSPR)

Address 001Ch

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CSPRO	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

The above applies when the CSPROINI bit in the OFS register is set to 1.

After Reset	1	0	0	0	0	0	0	0

The above applies when the CSPROINI bit in the OFS register is set to 0.

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved bits	Set to 0.	R/W
b1	—			
b2	—			
b3	—			
b4	—			
b5	—			
b6	—			
b7	CSPRO	Count source protection mode select bit (1)	0: Count source protection mode disabled 1: Count source protection mode enabled	R/W

Note:
1. To set the CSPRO bit to 1, write 0 and then 1 to it. This bit cannot be set to 0 by a program. Disable interrupts and DTC activation between writing 0 and writing 1.

14.2.6 Option Function Select Register (OFS)

Address 0FFFFh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CSPROINI	LVDAS	VDSEL1	VDSEL0	ROMCP1	ROMCR	—	WDTON
After Reset	User Setting Value (1)							

Bit	Symbol	Bit Name	Function	R/W
b0	WDTON	Watchdog timer start select bit	0: Watchdog timer automatically starts after reset. 1: Watchdog timer is stopped after reset.	R/W
b1	—	Reserved bit	Set to 1.	R/W
b2	ROMCR	ROM code protect disable bit	0: ROM code protect disabled 1: ROMCP1 bit enabled	R/W
b3	ROMCP1	ROM code protect bit	0: ROM code protect enabled 1: ROM code protect disabled	R/W
b4	VDSEL0	Voltage detection 0 level select bit (2)	b5 b4 0 0: 3.80 V selected (Vdet0_3) 0 1: 2.85 V selected (Vdet0_2) 1 0: 2.35 V selected (Vdet0_1) 1 1: 1.90 V selected (Vdet0_0)	R/W
b5	VDSEL1			R/W
b6	LVDAS	Voltage detection 0 circuit start bit (3)	0: Voltage monitor 0 reset enabled after reset 1: Voltage monitor 0 reset disabled after reset	R/W
b7	CSPROINI	Count source protection mode after reset select bit	0: Count source protect mode enabled after reset 1: Count source protect mode disabled after reset	R/W

Notes:
1. The OFS register is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not write additions to the OFS register. If the block including the OFS register is erased, the OFS register is set to FFh.
   When blank products are shipped, the OFS register is set to FFh. It is set to the written value after written by the user.
   When factory-programming products are shipped, the value of the OFS register is the value programmed by the user.
2. The same level of the voltage detection 0 level selected by bits VDSEL0 and VDESL1 is set in both functions of voltage monitor 0 reset and power-on reset.
3. To use power-on reset and voltage monitor 0 reset, set the LVDAS bit to 0 (voltage monitor 0 reset enabled after reset).

For a setting example of the OFS register, refer to **13.3.1 Setting Example of Option Function Select Area**.

LVDAS Bit (Voltage Detection 0 Circuit Start Bit)

The Vdet0 voltage to be monitored by the voltage detection 0 circuit is selected by bits VDSEL0 and VDSEL1.

14.2.7 Option Function Select Register 2 (OFS2)

Address 0FFDBh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	WDTRCS1	WDTRCS0	WDTUFS1	WDTUFS0
After Reset	User Setting Value (1)							

Bit	Symbol	Bit Name	Function	R/W
b0	WDTUFS0	Watchdog timer underflow period set bit	b1 b0 0 0: 03FFh 0 1: 0FFFh 1 0: 1FFFh 1 1: 3FFFh	R/W
b1	WDTUFS1			R/W
b2	WDTRCS0	Watchdog timer refresh acknowledgement period set bit	b3 b2 0 0: 25% 0 1: 50% 1 0: 75% 1 1: 100%	R/W
b3	WDTRCS1			R/W
b4	—	Reserved bits	Set to 1.	R/W
b5	—			
b6	—			
b7	—			

Note:

1. The OFS2 register is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not write additions to the OFS2 register. If the block including the OFS2 register is erased, the OFS2 register is set to FFh.
   When blank products are shipped, the OFS2 register is set to FFh. It is set to the written value after written by the user.
   When factory-programming products are shipped, the value of the OFS2 register is the value programmed by the user.

   For a setting example of the OFS2 register, refer to **13.3.1 Setting Example of Option Function Select Area**.

Bits WDTRCS0 and WDTRCS1 (Watchdog Timer Refresh Acknowledgement Period Set Bit)

Assuming that the period from when the watchdog timer starts counting until it underflows is 100%, the refresh acknowledgement period for the watchdog timer can be selected.
For details, refer to **14.3.1.1 Refresh Acknowledgment Period**.

14.3 Functional Description

14.3.1 Common Items for Multiple Modes

14.3.1.1 Refresh Acknowledgment Period

The period for acknowledging refreshment operation to the watchdog timer (write to the WDTR register) can be selected by bits WDTRCS0 and WDTRCS1 in the OFS2 register. Figure 14.2 shows the Refresh Acknowledgement Period for Watchdog Timer.

Assuming that the period from when the watchdog timer starts counting until it underflows is 100%, a refresh operation executed during the refresh acknowledgement period is acknowledged. Any refresh operation executed during the period other than the above is processed as an incorrect write, and a watchdog timer interrupt or watchdog timer reset (selectable by the PM12 bit in the PM1 register) is generated.

Do not execute any refresh operation while the count operation of the watchdog timer is stopped.

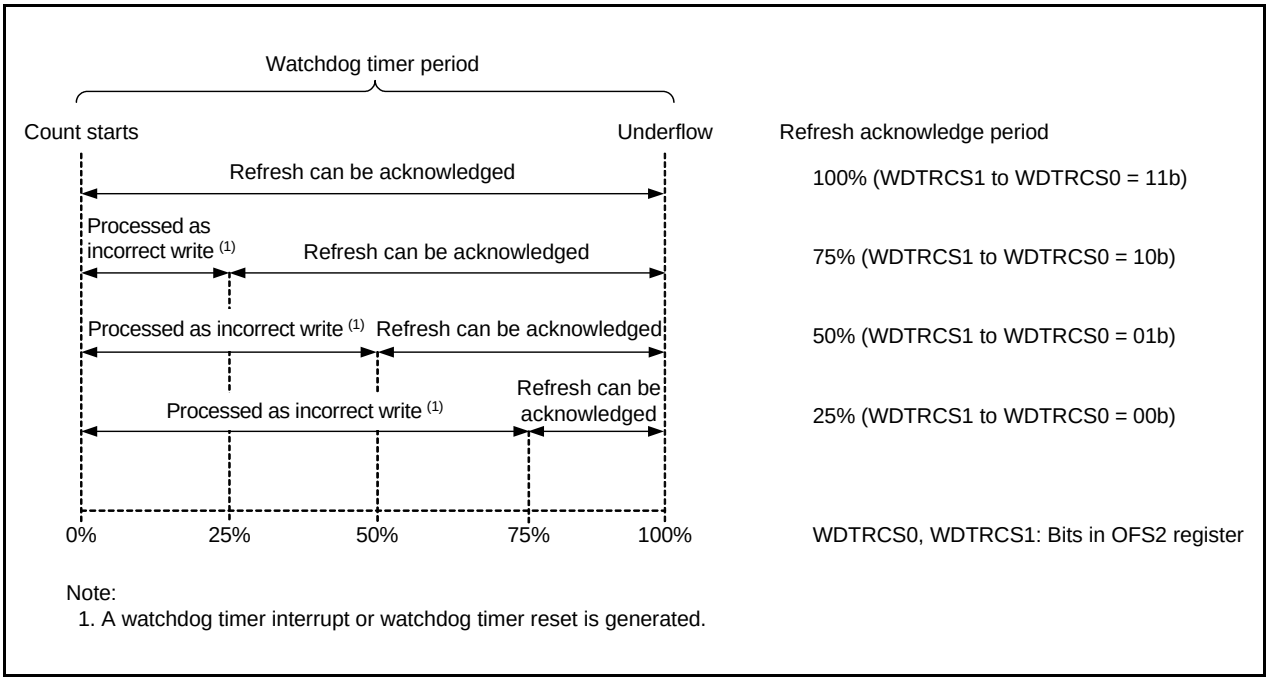


Figure 14.2 Refresh Acknowledgement Period for Watchdog Timer

14.3.2 Count Source Protection Mode Disabled

The count source for the watchdog timer is the CPU clock when count source protection mode is disabled. Table 14.2 lists the Watchdog Timer Specifications (Count Source Protection Mode Disabled).

Table 14.2 Watchdog Timer Specifications (Count Source Protection Mode Disabled)

Item	Specification
Count source	CPU clock
Count operation	Decrement
Period	$\frac{\text{Division ratio of prescaler (n)} \times \text{count value of watchdog timer (m)}}{\text{CPU clock}}$ (1) n: 16 or 128 (selected by the WDTC7 bit in the WDTC register) m: Value set by bits WDTUFS0 and WDTUFS1 in the OFS2 register Example: The period is approximately 13.1 ms when: - The CPU clock frequency is set to 20 MHz. - The prescaler is divided by 16. - Bits WDTUFS1 to WDTUFS0 are set to 11b (3FFFh).
Watchdog timer initialization conditions	• Reset • Write 00h and then FFh to the WDTR register. (3) • Underflow
Count start conditions	The operation of the watchdog timer after a reset is selected by the WDTON bit (2) in the OFS register (address 0FFFFh). • When the WDTON bit is set to 1 (watchdog timer is stopped after reset). The watchdog timer and prescaler are stopped after a reset and start counting when the WDTS register is written to. • When the WDTON bit is set to 0 (watchdog timer starts automatically after reset). The watchdog timer and prescaler start counting automatically after a reset.
Count stop condition	Stop mode, wait mode (Count resumes from the retained value after exiting.)
Operations at underflow	• When the PM12 bit in the PM1 register is set to 0. Watchdog timer interrupt • When the PM12 bit in the PM1 register is set to 1. Watchdog timer reset (Refer to **5.5 Watchdog Timer Reset**.)

Notes:
1. The watchdog timer is initialized when 00h and then FFh is written to the WDTR register. The prescaler is initialized after a reset. This may cause some errors due to the prescaler during the watchdog timer period.
2. The WDTON bit cannot be changed by a program. To set this bit, write 0 to bit 0 of address 0FFFFh with a flash programmer.
3. Write the WDTR register during the count operation of the watchdog timer.

14.3.3 Count Source Protection Mode Enabled

The count source for the watchdog timer is the low-speed on-chip oscillator clock for the watchdog timer when count source protection mode is enabled. If the CPU clock stops when a program is out of control, the clock can still be supplied to the watchdog timer.
Table 14.3 lists the Watchdog Timer Specifications (Count Source Protection Mode Enabled).

Table 14.3 Watchdog Timer Specifications (Count Source Protection Mode Enabled)

Item	Specification
Count source	Low-speed on-chip oscillator clock
Count operation	Decrement
Period	$\frac{\text{Count value of watchdog timer (m)}}{\text{Low-speed on-chip oscillator clock for the watchdog timer}}$ m: Value set by bits WDTUFS0 and WDTUFS1 in the OFS2 register Example: The period is approximately 8.2 ms when: - The on-chip oscillator clock for the watchdog timer is set to 125 kHz. - Bits WDTUFS1 to WDTUFS0 are set to 00b (03FFh).
Watchdog timer initialization conditions	• Reset • Write 00h and then FFh to the WDTR register. (3) • Underflow
Count start conditions	The operation of the watchdog timer after a reset is selected by the WDTON bit (1) in the OFS register (address 0FFFFh). • When the WDTON bit is set to 1 (watchdog timer is stopped after reset). The watchdog timer and prescaler are stopped after a reset and start counting when the WDTS register is written to. • When the WDTON bit is set to 0 (watchdog timer starts automatically after reset). The watchdog timer and prescaler start counting automatically after a reset.
Count stop condition	None (Count does not stop even in wait mode and stop mode once it starts.)
Operation at underflow	Watchdog timer reset (Refer to **5.5 Watchdog Timer Reset**.)
Registers, bits	• When the CSPPRO bit in the CSPR register is set to 1 (count source protection mode enabled) (2), the following are set automatically: - The low-speed on-chip oscillator for the watchdog timer is on. - The PM12 bit in the PM1 register is set to 1 (watchdog timer reset when the watchdog timer underflows).

Notes:
1. The WDTON bit cannot be changed by a program. To set this bit, write 0 to bit 0 of address 0FFFFh with a flash programmer.
2. Even if 0 is written to the CSPROINI bit in the OFS register, the CSPRO bit is set to 1. The CSPROINI bit cannot be changed by a program. To set this bit, write 0 to bit 7 of address 0FFFFh with a flash programmer.
3. Write the WDTR register during the count operation of the watchdog timer.

15. DTC

The DTC (data transfer controller) is a function that transfers data between the SFR and on-chip memory without using the CPU. This chip incorporates one DTC channel. The DTC is activated by a peripheral function interrupt to perform data transfers. The DTC and CPU use the same bus, and the DTC takes priority over the CPU in using the bus.
To control DTC data transfers, control data comprised of a transfer source address, a transfer destination address, and operating modes are allocated in the DTC control data area. Each time the DTC is activated, the DTC reads control data to perform data transfers.

15.1 Overview

Table 15.1 lists the DTC Specifications.

Table 15.1 DTC Specifications

Item		Specification
Activation sources		17 sources
Allocatable control data		24 sets
Address space which can be transferred		64 Kbytes (00000h to 0FFFFh)
Maximum number of transfer times	Normal mode	256 times
	Repeat mode	255 times
Maximum size of block to be transferred	Normal mode	256 bytes
	Repeat mode	255 bytes
Unit of transfers		Byte
Transfer mode	Normal mode	Transfers end on completion of the transfer causing the DTCCTj register value to change from 1 to 0.
	Repeat mode	On completion of the transfer causing the DTCCTj register value to change from 1 to 0, the repeat area address is initialized and the DTRLDj register value is reloaded to the DTCCTj register to continue transfers.
Address control	Normal mode	Fixed or incremented
	Repeat mode	Addresses of the area not selected as the repeat area are fixed or incremented.
Priority of activation sources		Refer to **Table 15.5 DTC Activation Sources and DTC Vector Addresses**.
Interrupt request	Normal mode	When the data transfer causing the DTCCTj register value to change from 1 to 0 is performed, the activation source interrupt request is generated for the CPU, and interrupt handling is performed on completion of the data transfer.
	Repeat mode	When the data transfer causing the DTCCTj register value to change from 1 to 0 is performed while the RPTINT bit in the DTCCRj register is 1 (interrupt generation enabled), the activation source interrupt request is generated for the CPU, and interrupt handling is performed on completion of the transfer.
Transfer start		When bits DTCENi0 to DTCENi7 in the DTCENi registers are 1 (activation enabled), data transfer is started each time the corresponding DTC activation sources are generated.
Transfer stop	Normal mode	• When bits DTCENi0 to DTCENi7 are set to 0 (activation disabled). • When the data transfer causing the DTCCTj register value to change from 1 to 0 is completed.
	Repeat mode	• When bits DTCENi0 to DTCENi7 are set to 0 (activation disabled). • When the data transfer causing the DTCCTj register value to change from 1 to 0 is completed while the RPTINT bit is 1 (interrupt generation enabled).

i = 0 to 3, 5, 6, j = 0 to 23

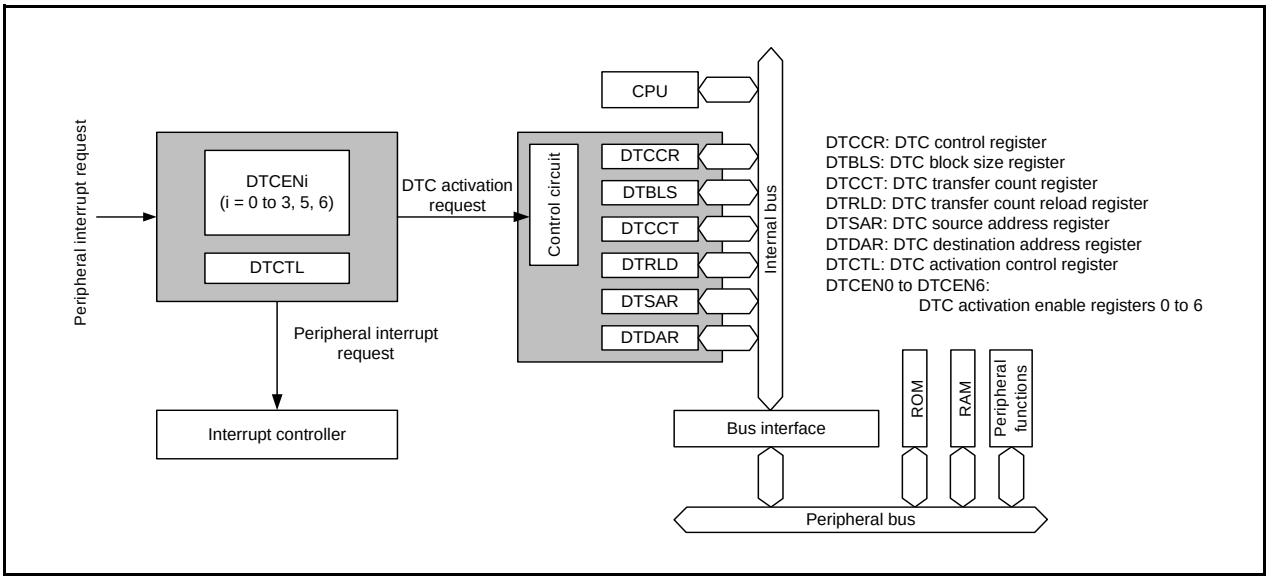


Figure 15.1 DTC Block Diagram

15.2 Registers

When the DTC is activated, control data (DTCCRj, DTBLSj, DTCCTj, DTRLDj, DTSARj, and DTDARj, j = 0 to 23) allocated in the control data area is read, and then transferred to the control registers (DTCCR, DTBLS, DTCCT, DTRLD, DTSAR, and DTDAR) in the DTC. On completion of the DTC data transfer, the contents of the DTC control registers are written back to the control data area.

Each DTCCR, DTBLS, DTCCT, DTRLD, DTSAR, and DTDAR register cannot be directly read or written to. DTCCRj, DTBLSj, DTCCTj, DTRLDj, DTSARj, and DTDARj are allocated as control data at addresses from 2C40h to 2CFFh in the DTC control data area, and can be directly accessed.
Also, registers DTCTL and DTCENi (i = 0 to 3, 5, 6) can be directly accessed.

15.2.1 DTC Control Register j (DTCCRj) (j = 0 to 23)

Address Refer to **Table 15.4 Control Data Allocation Addresses**.

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	RPTINT	CHNE	DAMOD	SAMOD	RPTSEL	MODE
After Reset	X	X	X	X	X	X	X	X

Bit	Symbol	Bit Name	Function	R/W
b0	MODE	Transfer mode select bit	0: Normal mode 1: Repeat mode	R/W
b1	RPTSEL	Repeat area select bit (1)	0: Transfer destination is the repeat area. 1: Transfer source is the repeat area.	R/W
b2	SAMOD	Source address control bit (2)	0: Fixed 1: Incremented	R/W
b3	DAMOD	Destination address control bit (2)	0: Fixed 1: Incremented	R/W
b4	CHNE	Chain transfer enable bit (3)	0: Chain transfers disabled 1: Chain transfers enabled	R/W
b5	RPTINT	Repeat mode interrupt enable bit (1)	0: Interrupt generation disabled 1: Interrupt generation enabled	R/W
b6	—	Reserved bits	Set to 0.	R/W
b7	—			

Notes:
1. This bit is valid when the MODE bit is 1 (repeat mode).
2. Settings of bits SAMOD and DAMOD are invalid for the repeat area.
3. Set the CHNE bit in the DTCCR23 register to 0 (chain transfers disabled).

15.2.2 DTC Block Size Register j (DTBLSj) (j = 0 to 23)

Address Refer to **Table 15.4 Control Data Allocation Addresses**.

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	Function	Setting Range	R/W
b7 to b0	These bits specify the size of the data block to be transferred by one activation.	00h to FFh (1)	R/W

Note:
1. When the DTBLS register is set to 00h, the block size is 256 bytes.

15.2.3 DTC Transfer Count Register j (DTCCTj) (j = 0 to 23)

Address Refer to **Table 15.4 Control Data Allocation Addresses**.

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	Function	Setting Range	R/W
b7 to b0	These bits specify the number of times of DTC data transfers.	00h to FFh (1)	R/W

Note:
1. When the DTCCT register is set to 00h, the number of transfer times is 256. Each time the DTC is activated, the DTCCT register is decremented by 1.

15.2.4 DTC Transfer Count Reload Register j (DTRLDj) (j = 0 to 23)

Address Refer to **Table 15.4 Control Data Allocation Addresses**.

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	Function	Setting Range	R/W
b7 to b0	This register value is reloaded to the DTCCT register in repeat mode.	00h to FFh (1)	R/W

Note:
1. Set the initial value for the DTCCT register.

15.2.5 DTC Source Address Register j (DTSARj) (j = 0 to 23)

Address Refer to **Table 15.4 Control Data Allocation Addresses**.

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	Function	Setting Range	R/W
b15 to b0	These bits specify a transfer source address for data transfer.	0000h to FFFFh	R/W

15.2.6 DTC Destination Address Register j (DTDARj) (j = 0 to 23)

Address Refer to **Table 15.4 Control Data Allocation Addresses**.

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	Function	Setting Range	R/W
b15 to b0	These bits specify a transfer destination address for data transfer.	0000h to FFFFh	R/W

15.2.7 DTC Activation Enable Register i (DTCENi) (i = 0 to 3, 5, 6)

Address 0088h (DTCEN0), 0089h (DTCEN1), 008Ah (DTCEN2), 008Bh (DTCEN3), 008Dh (DTCEN5), 008Eh (DTCEN6)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	DTCENi7	DTCENi6	DTCENi5	DTCENi4	DTCENi3	DTCENi2	DTCENi1	DTCENi0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	DTCENi0	DTC activation enable bit (1)	0: Activation disabled 1: Activation enabled	R/W
b1	DTCENi1			R/W
b2	DTCENi2			R/W
b3	DTCENi3			R/W
b4	DTCENi4			R/W
b5	DTCENi5			R/W
b6	DTCENi6			R/W
b7	DTCENi7			R/W

Note:
1. For the operation of this bit, refer to **15.3.7 Interrupt Sources**.

The DTCENi registers enable/disable DTC activation by interrupt sources. Table 15.2 lists Correspondences between Bits DTCENi0 to DTCENi7 (i = 0 to 3, 5, 6) and Interrupt Sources.

Table 15.2 Correspondences between Bits DTCENi0 to DTCENi7 (i = 0 to 3, 5, 6) and Interrupt Sources

Register	DTCENi7 Bit	DTCENi6 Bit	DTCENi5 Bit	DTCENi4 Bit	DTCENi3 Bit	DTCENi2 Bit	DTCENi1 Bit	DTCENi0 Bit
DTCEN0	$\overline{\text{INT0}}$	$\overline{\text{INT1}}$	$\overline{\text{INT2}}$	$\overline{\text{INT3}}$	—	—	—	—
DTCEN1	Key input	—	UART0 reception	UART0 transmission	—	—	—	—
DTCEN2	—	—	Voltage Monitor 2	Voltage Monitor 1	Sensor control unit data transfer request	—	Timer RC input-capture/ compare-match A	Timer RC input-capture/ compare-match B
DTCEN3	Timer RC input-capture/ compare-match C	Timer RC input-capture/ compare-match D	—	—	—	—	—	—
DTCEN5	—	—	—	—	—	—	—	—
DTCEN6	—	Timer RA	—	Timer RB	Flash ready status	—	—	—

15.2.8 DTC Activation Control Register (DTCTL)

Address 0080h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	NMIF	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved bit	Set to 0.	R/W
b1	NMIF	Non-maskable interrupt generation bit (1)	0: Non-maskable interrupts not generated 1: Non-maskable interrupts generated	R/W
b2	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b3	—			
b4	—			
b5	—			
b6	—			
b7	—			

Note:
1. This bit is set to 0 when the read result is 1 and 0 is written to the same bit. This bit remains unchanged even if the read result is 0 and 0 is written to the same bit. This bit remains unchanged if 1 is written to it.

The DTCTL register controls DTC activation when a non-maskable interrupt (an interrupt by the watchdog timer, oscillation stop detection, voltage monitor 1, or voltage monitor 2) is generated.

NMIF Bit (Non-Maskable Interrupt Generation Bit)

The NMIF bit is set to 1 when a watchdog timer interrupt, an oscillation stop detection interrupt, a voltage monitor 1 interrupt, or a voltage monitor 2 interrupt is generated.
When the NMIF bit is 1, the DTC is not activated even if the interrupt which enables DTC activation is generated. If the NMIF bit is changed to 1 during DTC transfer, the transfer is continued until it is completed.

When an interrupt source is the watchdog timer, wait for the following cycles before writing 0 to the NMIF bit:
If the WDTC7 bit in the WDTC register is set to 0 (divide-by-16 using the prescaler), wait for 16 cycles of the CPU clock after the interrupt source is generated.
If the WDTC7 bit is set to 1 (divide-by-128 using the prescaler), wait for 128 cycles of the CPU clock after the interrupt source is generated.
When an interrupt source is oscillation stop detection, set to the OCD1 bit in the OCD register to 0 (oscillation stop detection interrupt disabled) before writing 0 to the NMIF bit.

15.3 Function Description

15.3.1 Overview

When the DTC is activated, control data is read from the DTC control data area to perform data transfers and control data after data transfer is written back to the DTC control data area. Twenty-four sets of control data can be stored in the DTC control data area, which allows 24 types of data transfers to be performed.
There are two transfer modes: normal mode and repeat mode. When the CHNE bit in the DTCCRj (j = 0 to 23) register is set to 1 (chain transfers enabled), multiple control data is read and data transfers are continuously performed by one activation source (chain transfers).
A transfer source address is specified by the 16-bit register DTSARj, and a transfer destination address is specified by the 16-bit register DTDARj. The values in the registers DTSARj and DTDARj are separately fixed or incremented according to the control data on completion of the data transfer.

15.3.2 Activation Sources

The DTC is activated by an interrupt source. Figure 15.2 is a Block Diagram Showing Control of DTC Activation Sources.
The interrupt sources to activate the DTC are selected with the DTCENi (i = 0 to 3, 5, 6) registers.
The DTC sets 0 (activation disabled) to the corresponding bit among bits DTCENi0 to DTCENi7 in the DTCENi register during operation when the setting of data transfer (the first transfer in chain transfers) is either of the following:

- Transfer causing the DTCCTj (j = 0 to 23) register value to change to 0 in normal mode
- Transfer causing the DTCCTj register value to change to 0 while the RPTINT bit in the DTCCRj register is 1 (interrupt generation enabled) in repeat mode

If the data transfer setting is not either of the above and the activation source is an interrupt source for timer RC or the flash memory, the DTC sets 0 to the interrupt source flag corresponding to the activation source during operation.
Table 15.3 lists the DTC Activation Sources and Interrupt Source Flags for Setting to 0 during DTC Operation.
If multiple activation sources are simultaneously generated, the DTC activation will be performed according to the DTC activation source priority.
If multiple activation sources are simultaneously generated on completion of DTC operation, the next transfer will be performed according to the priority.
DTC activation is not affected by the I flag or interrupt control register, unlike with interrupt request operation. Therefore, even if interrupt requests cannot be acknowledged because interrupts are disabled, DTC activation requests can be acknowledged. The IR bit in the interrupt control register does not change even when an interrupt source to enable DTC activation is generated.

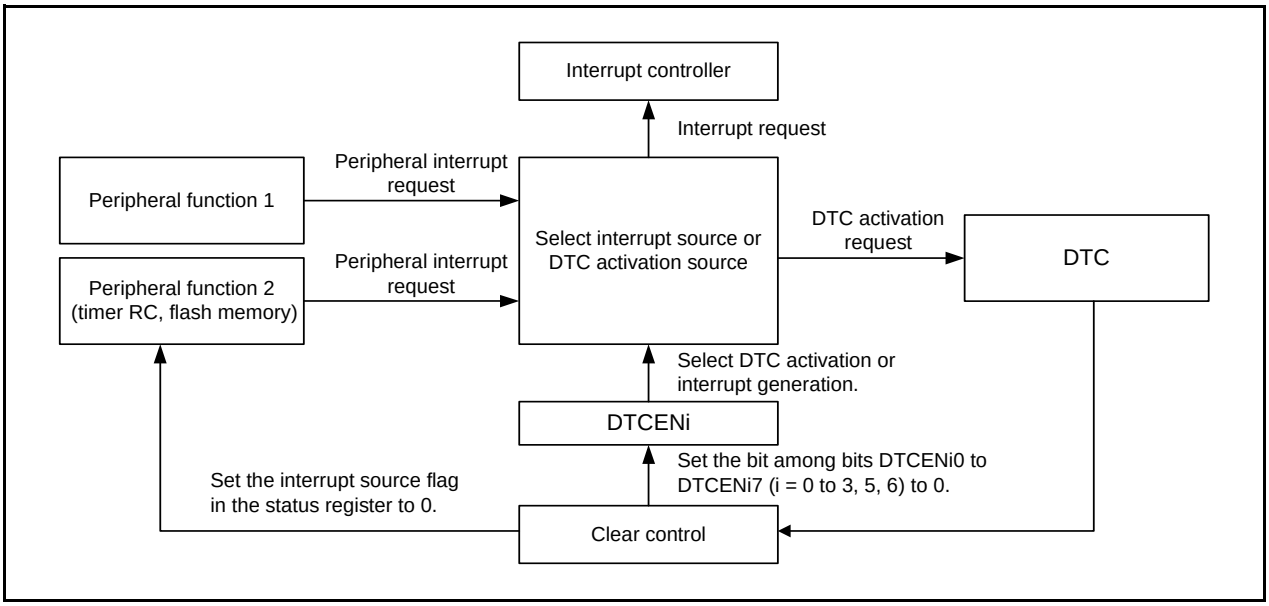


Figure 15.2 Block Diagram Showing Control of DTC Activation Sources

Table 15.3 DTC Activation Sources and Interrupt Source Flags for Setting to 0 during DTC Operation

DTC activation source generation	Interrupt Source Flag for Setting to 0
Timer RC input-capture/compare-match A	IMFA bit in TRCSR register
Timer RC input-capture/compare-match B	IMFB bit in TRCSR register
Timer RC input-capture/compare-match C	IMFC bit in TRCSR register
Timer RC input-capture/compare-match D	IMFD bit in TRCSR register
Flash ready status	RDYSTI bit in FST register

15.3.3 Control Data Allocation and DTC Vector Table

Control data is allocated in the order: Registers DTCCRj, DTBLSj, DTCCTj, DTRLDj, DTSARj, and DTDARj (j = 0 to 23). Table 15.4 lists the Control Data Allocation Addresses.

Table 15.4 Control Data Allocation Addresses

Register Symbol	Control Data No.	Address	DTCCRj Register	DTBLSj Register	DTCCTj Register	DTRLDj Register	DTSARj Register (Lower 8 Bits)	DTSARj Register (Higher 8 Bits)	DTDARj Register (Lower 8 Bits)	DTDARj Register (Higher 8 Bits)
DTCD0	Control Data 0	2C40h to 2C47h	2C40h	2C41h	2C42h	2C43h	2C44h	2C45h	2C46h	2C47h
DTCD1	Control Data 1	2C48h to 2C4Fh	2C48h	2C49h	2C4Ah	2C4Bh	2C4Ch	2C4Dh	2C4Eh	2C4Fh
DTCD2	Control Data 2	2C50h to 2C57h	2C50h	2C51h	2C52h	2C53h	2C54h	2C55h	2C56h	2C57h
DTCD3	Control Data 3	2C58h to 2C5Fh	2C58h	2C59h	2C5Ah	2C5Bh	2C5Ch	2C5Dh	2C5Eh	2C5Fh
DTCD4	Control Data 4	2C60h to 2C67h	2C60h	2C61h	2C62h	2C63h	2C64h	2C65h	2C66h	2C67h
DTCD5	Control Data 5	2C68h to 2C6Fh	2C68h	2C69h	2C6Ah	2C6Bh	2C6Ch	2C6Dh	2C6Eh	2C6Fh
DTCD6	Control Data 6	2C70h to 2C77h	2C70h	2C71h	2C72h	2C73h	2C74h	2C75h	2C76h	2C77h
DTCD7	Control Data 7	2C78h to 2C7Fh	2C78h	2C79h	2C7Ah	2C7Bh	2C7Ch	2C7Dh	2C7Eh	2C7Fh
DTCD8	Control Data 8	2C80h to 2C87h	2C80h	2C81h	2C82h	2C83h	2C84h	2C85h	2C86h	2C87h
DTCD9	Control Data 9	2C88h to 2C8Fh	2C88h	2C89h	2C8Ah	2C8Bh	2C8Ch	2C8Dh	2C8Eh	2C8Fh
DTCD10	Control Data 10	2C90h to 2C97h	2C90h	2C91h	2C92h	2C93h	2C94h	2C95h	2C96h	2C97h
DTCD11	Control Data 11	2C98h to 2C9Fh	2C98h	2C99h	2C9Ah	2C9Bh	2C9Ch	2C9Dh	2C9Eh	2C9Fh
DTCD12	Control Data 12	2CA0h to 2CA7h	2CA0h	2CA1h	2CA2h	2CA3h	2CA4h	2CA5h	2CA6h	2CA7h
DTCD13	Control Data 13	2CA8h to 2CAFh	2CA8h	2CA9h	2CAAh	2CABh	2CACh	2CADh	2CAEh	2CAFh
DTCD14	Control Data 14	2CB0h to 2CB7h	2CB0h	2CB1h	2CB2h	2CB3h	2CB4h	2CB5h	2CB6h	2CB7h
DTCD15	Control Data 15	2CB8h to 2CBFh	2CB8h	2CB9h	2CBAh	2CBBh	2CBCh	2CBDh	2CBEh	2CBFh
DTCD16	Control Data 16	2CC0h to 2CC7h	2CC0h	2CC1h	2CC2h	2CC3h	2CC4h	2CC5h	2CC6h	2CC7h
DTCD17	Control Data 17	2CC8h to 2CCFh	2CC8h	2CC9h	2CCAh	2CCBh	2CCCh	2CCDh	2CCEh	2CCFh
DTCD18	Control Data 18	2CD0h to 2CD7h	2CD0h	2CD1h	2CD2h	2CD3h	2CD4h	2CD5h	2CD6h	2CD7h
DTCD19	Control Data 19	2CD8h to 2CDFh	2CD8h	2CD9h	2CDAh	2CDBh	2CDCh	2CDDh	2CDEh	2CDFh
DTCD20	Control Data 20	2CE0h to 2CE7h	2CE0h	2CE1h	2CE2h	2CE3h	2CE4h	2CE5h	2CE6h	2CE7h
DTCD21	Control Data 21	2CE8h to 2CEFh	2CE8h	2CE9h	2CEAh	2CEBh	2CECh	2CEDh	2CEEh	2CEFh
DTCD22	Control Data 22	2CF0h to 2CF7h	2CF0h	2CF1h	2CF2h	2CF3h	2CF4h	2CF5h	2CF6h	2CF7h
DTCD23	Control Data 23	2CF8h to 2CFFh	2CF8h	2CF9h	2CFAh	2CFBh	2CFCh	2CFDh	2CFEh	2CFFh

j = 0 to 23

When the DTC is activated, one control data is selected according to the data read from the vector table which has been assigned to each activation source, and the selected control data is read from the DTC control data area.
Table 15.5 lists the DTC Activation Sources and DTC Vector Addresses. A one-byte vector table area is assigned to each activation source and one value from 00000000b to 00010111b (control data numbers in Table 15.4) is stored in each area to select one of the 24 control data sets.
Figures 15.3 to 15.5 show the DTC Internal Operation Flowchart.

Table 15.5 DTC Activation Sources and DTC Vector Addresses

Interrupt Request Source	Interrupt Name	Source No.	DTC Vector Address	Priority
External input	$\overline{\text{INT0}}$	0	2C00h	High
	$\overline{\text{INT1}}$	1	2C01h	
	$\overline{\text{INT2}}$	2	2C02h	
	$\overline{\text{INT3}}$	3	2C03h	
	(Reserved)	4	2C04h	
Key input	Key input	8	2C08h	
(Reserved)	—	9	2C09h	
UART0	UART0 reception	10	2C0Ah	
	UART0 transmission	11	2C0Bh	
(Reserved)	—	12	2C0Ch	
	—	13	2C0Dh	
(Reserved)	—	14	2C0Eh	
	—	15	2C0Fh	
Voltage detection circuit	Voltage monitor 2	18	2C12h	
	Voltage monitor 1	19	2C13h	
Sensor control unit	Data transfer request	20	2C14h	
Timer RC	Input-capture/compare-match A	22	2C16h	
	Input-capture/compare-match B	23	2C17h	
	Input-capture/compare-match C	24	2C18h	
	Input-capture/compare-match D	25	2C19h	
(Reserved)	—	26	2C1Ah	
	—	27	2C1Bh	
	—	28	2C1Ch	
	—	29	2C1Dh	
	—	30	2C1Eh	
	—	31	2C1Fh	
	—	32	2C20h	
	—	33	2C21h	
Timer RA	Timer RA	49	2C31h	
Timer RB	Timer RB	51	2C33h	
Flash memory	Flash ready status	52	2C34h	Low

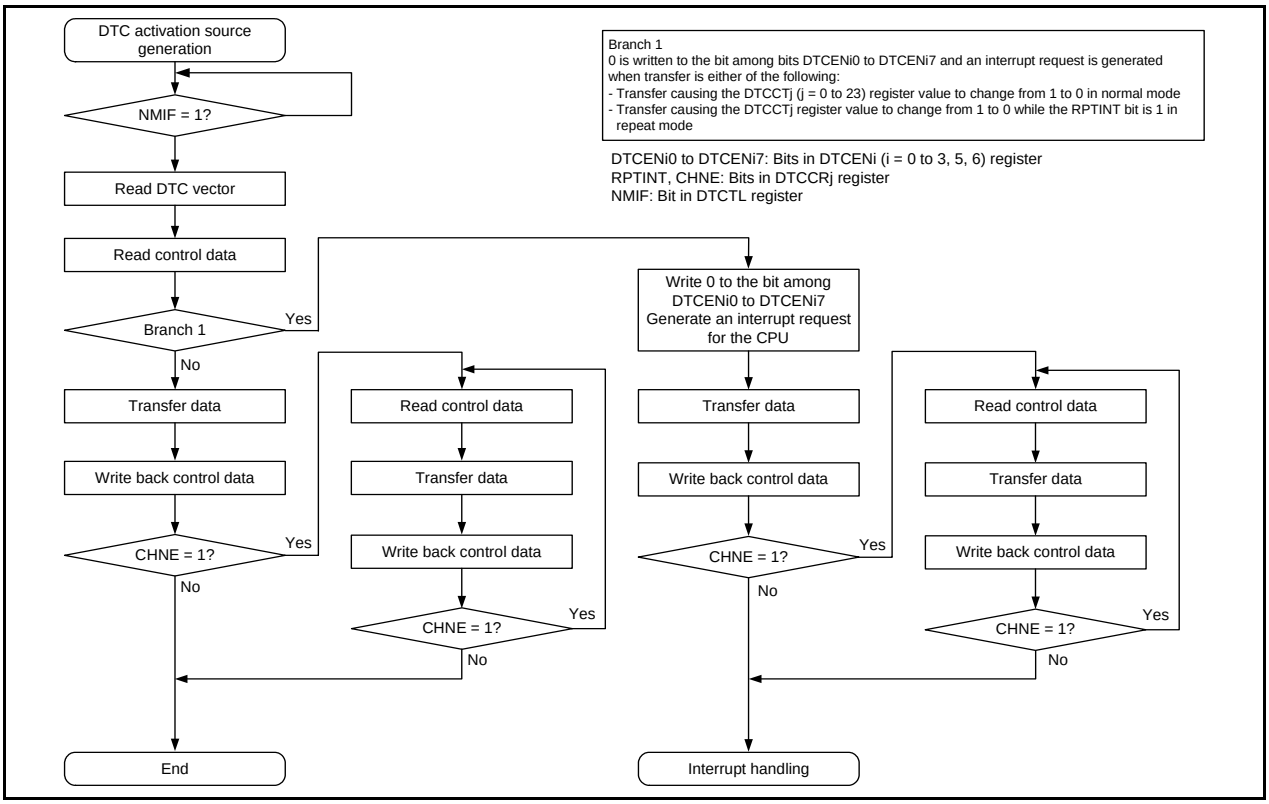


Figure 15.3 DTC Internal Operation Flowchart When DTC Activation Source is not Timer RC or Flash Memory Interrupt Source

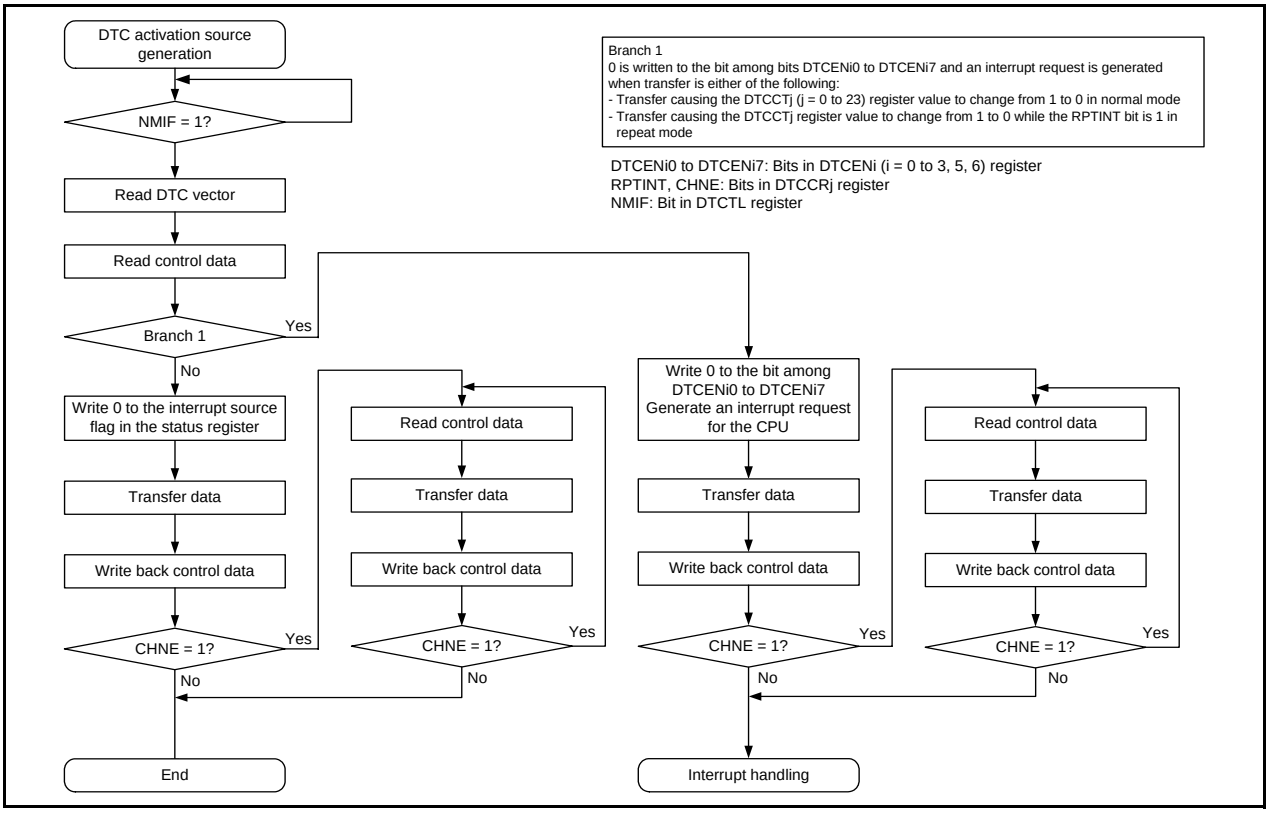


Figure 15.4 DTC Internal Operation Flowchart When DTC Activation Source is Timer RC Interrupt Source

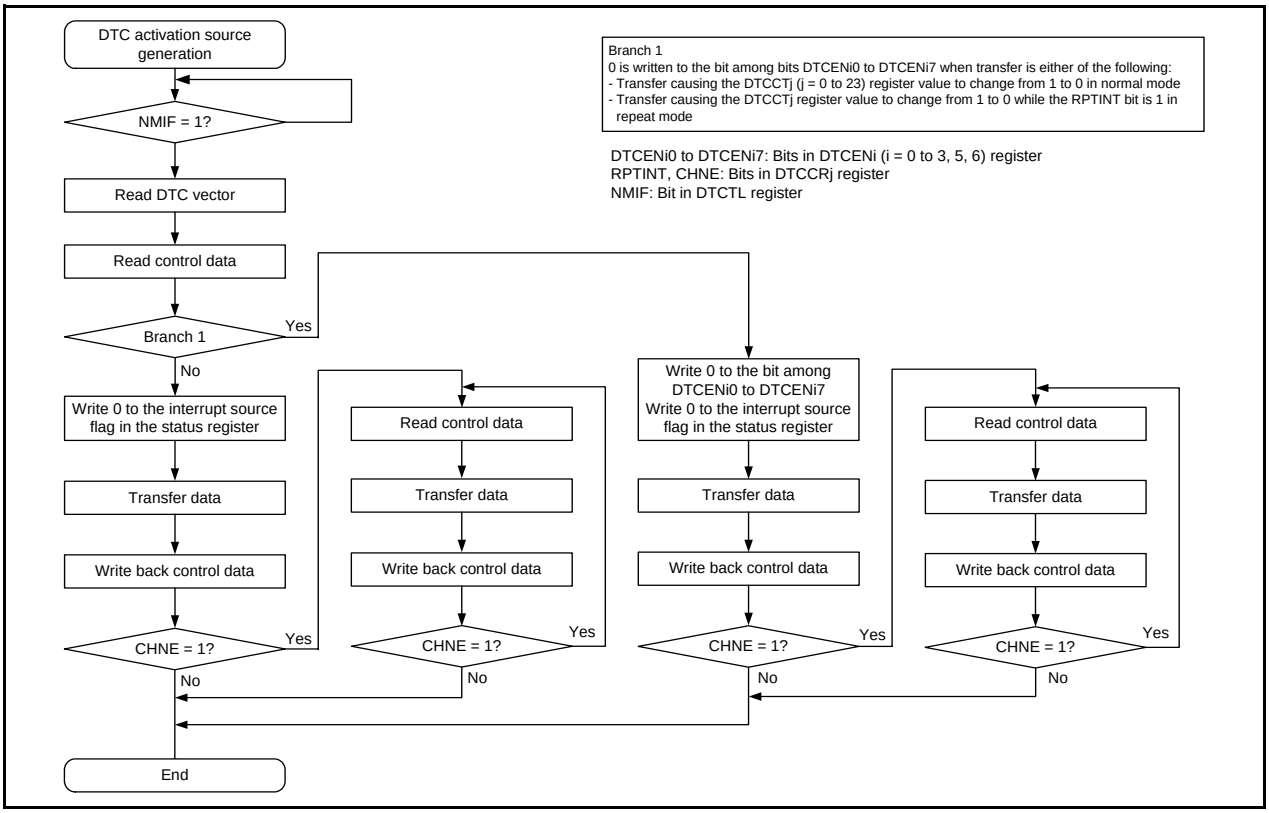


Figure 15.5 DTC Internal Operation Flowchart When DTC Activation Source is Flash ready status

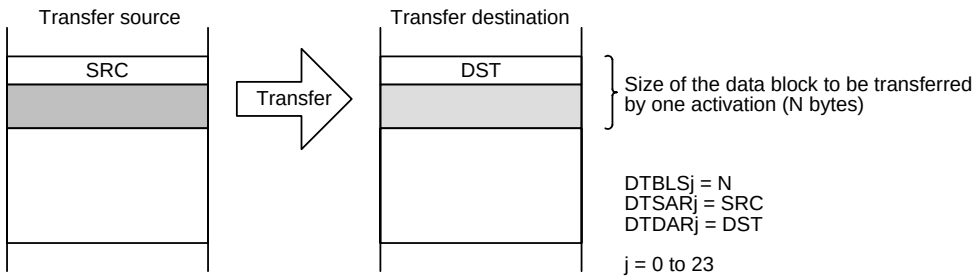
15.3.4 Normal Mode

One to 256 bytes of data are transferred by one activation. The number of transfer times can be 1 to 256. When the data transfer causing the DTCCTj (j = 0 to 23) register value to change to 0 is performed, an interrupt request for the CPU is generated during DTC operation.
Table 15.6 lists Register Functions in Normal Mode. Figure 15.6 shows Data Transfers in Normal Mode.

Table 15.6 Register Functions in Normal Mode

Register	Symbol	Function
DTC block size register j	DTBLSj	Size of the data block to be transferred by one activation
DTC transfer count register j	DTCCTj	Number of times of data transfers
DTC transfer count reload register j	DTRLDj	Not used
DTC source address register j	DTSARj	Data transfer source address
DTC destination address register j	DTDARj	Data transfer destination address

j = 0 to 23



Bits b3 to b0 in DTCCR register	Source address control	Destination address control	Source address after transfer	Destination address after transfer
00X0b	Fixed	Fixed	SRC	DST
01X0b	Incremented	Fixed	SRC+N	DST
10X0b	Fixed	Incremented	SRC	DST+N
11X0b	Incremented	Incremented	SRC+N	DST+N

X: 0 or 1

Figure 15.6 Data Transfers in Normal Mode

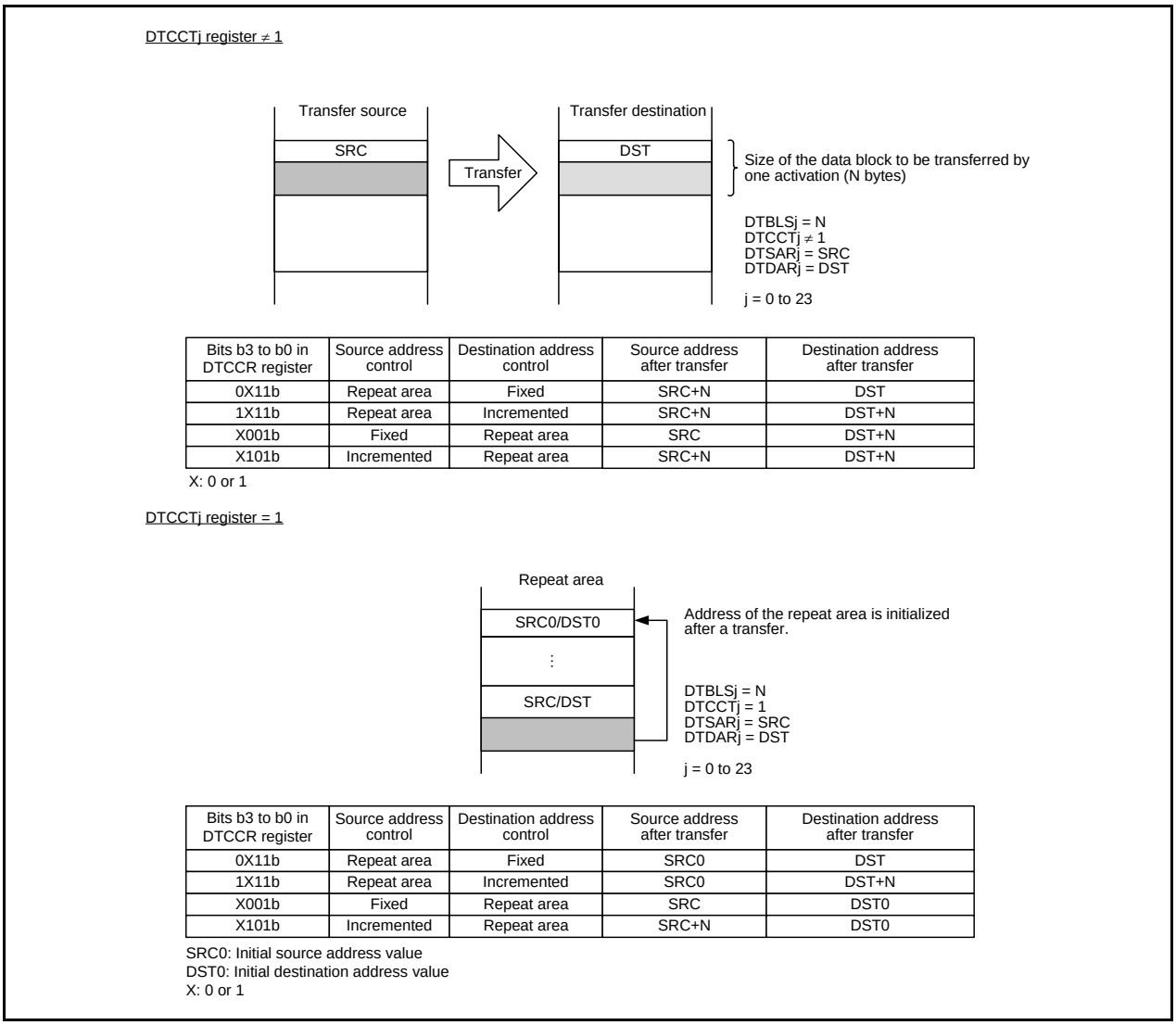
15.3.5 Repeat Mode

One to 255 bytes of data are transferred by one activation. Either of the transfer source or destination should be specified as the repeat area. The number of transfer times can be 1 to 255. On completion of the specified number of transfer times, the DTCCTj (i = 0 to 23) register and the address specified for the repeat area are initialized to continue transfers. When the data transfer causing the DTCCTj register value to change to 0 is performed while the RPTINT bit in the DTCCRj register is 1 (interrupt generation enabled), an interrupt request for the CPU is generated during DTC operation.
The lower 8 bits of the initial value for the repeat area address must be 00h. The size of data to be transferred must be set to 255 bytes or less before the specified number of transfer times is completed.
Table 15.7 lists Register Functions in Repeat Mode. Figure 15.7 shows Data Transfers in Repeat Mode.

Table 15.7 Register Functions in Repeat Mode

Register	Symbol	Function
DTC block size register j	DTBLSj	Size of the data block to be transferred by one activation
DTC transfer count register j	DTCCTj	Number of times of data transfers
DTC transfer count reload register j	DTRLDj	This register value is reloaded to the DTCCT register. (Data transfer count is initialized.)
DTC source address register j	DTSARj	Data transfer source address
DTC destination address register j	DTDARj	Data transfer destination address

j = 0 to 23



Bits b3 to b0 in DTCCR register	Source address control	Destination address control	Source address after transfer	Destination address after transfer
0X11b	Repeat area	Fixed	SRC+N	DST
1X11b	Repeat area	Incremented	SRC+N	DST+N
X001b	Fixed	Repeat area	SRC	DST+N
X101b	Incremented	Repeat area	SRC+N	DST+N

X: 0 or 1

Bits b3 to b0 in DTCCR register	Source address control	Destination address control	Source address after transfer	Destination address after transfer
0X11b	Repeat area	Fixed	SRC0	DST
1X11b	Repeat area	Incremented	SRC0	DST+N
X001b	Fixed	Repeat area	SRC	DST0
X101b	Incremented	Repeat area	SRC+N	DST0

SRC0: Initial source address value
DST0: Initial destination address value
X: 0 or 1

Figure 15.7 Data Transfers in Repeat Mode

15.3.6 Chain Transfers

When the CHNE bit in the DTCCRj (j = 0 to 22) register is 1 (chain transfers enabled), multiple data transfers can be continuously performed by one activation source. Figure 15.8 shows a Flow of Chain Transfers.
When the DTC is activated, one control data is selected according to the data read from the DTC vector address corresponding to the activation source, and the selected control data is read from the DTC control data area. When the CHNE bit for the control data is 1 (chain transfers enabled), the next control data immediately following the current control data is read and transferred after the current transfer is completed. This operation is repeated until the data transfer with the control data for which the CHNE bit is 0 (chain transfers disabled) is completed.
When performing chain transfers using several control data, the number of transfers set to the first control data is enabled and the number of transfers proceeded after the first control data is disabled.
Set the CHNE bit in the DTCCR23 register to 0 (chain transfers disabled).

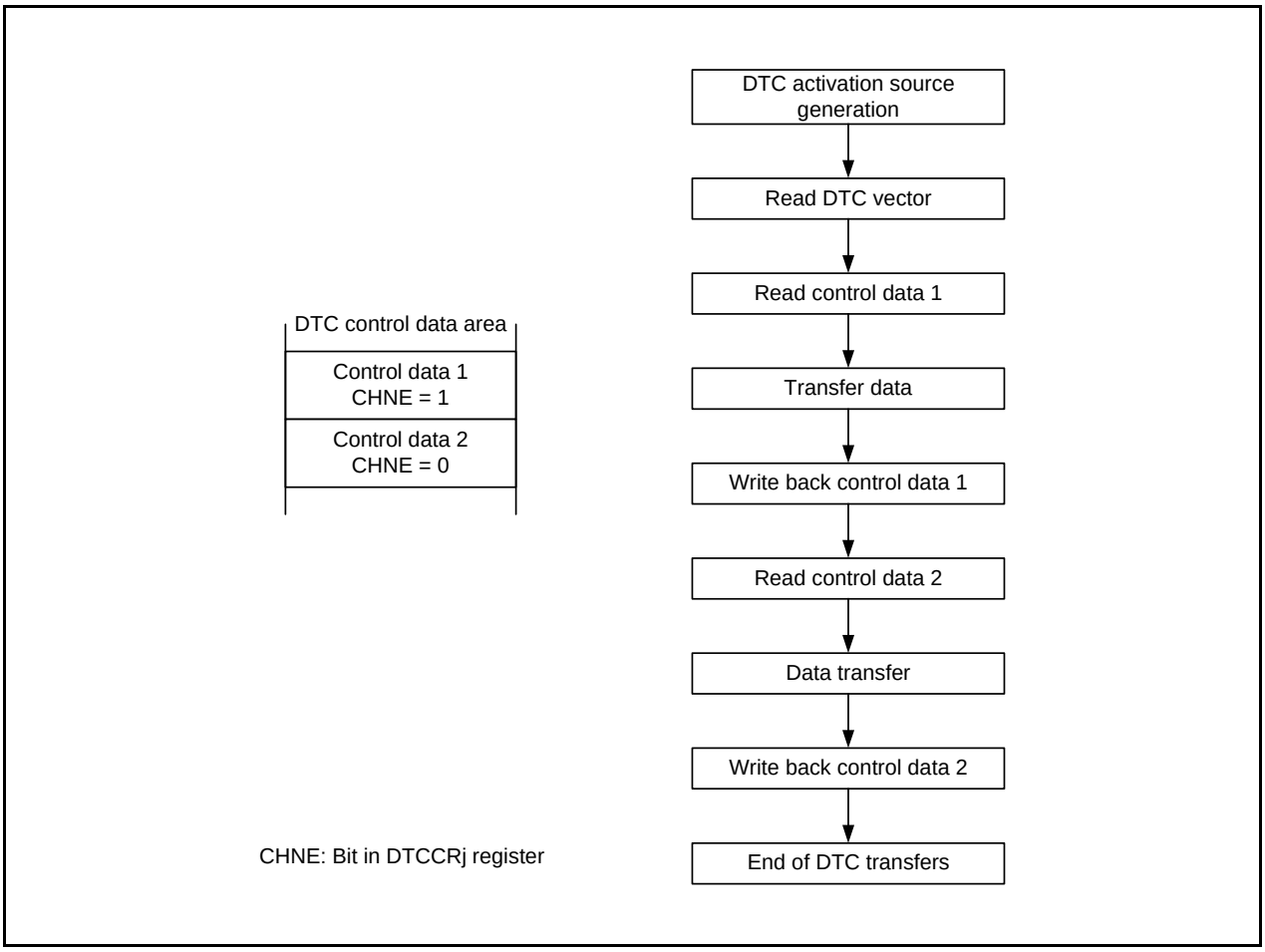


Figure 15.8 Flow of Chain Transfers

15.3.7 Interrupt Sources

When the data transfer causing the DTCCTj (j = 0 to 23) register value to change to 0 is performed in normal mode, and when the data transfer causing the DTCCTj register value to change to 0 is performed while the RPTINT bit in the DTCCRj register is 1 (interrupt generation enabled) in repeat mode, the interrupt request corresponding to the activation source is generated for the CPU during DTC operation. However, no interrupt request is generated for the CPU when the activation source is flash ready status.
Interrupt requests for the CPU are affected by the I flag or interrupt control register. In chain transfers, whether the interrupt request is generated or not is determined either by the number of transfer times specified for the first type of the transfer or the RPTINT bit. When an interrupt request is generated for the CPU, the bit among bits DTCENi0 to DTCENi7 in the DTCENi (i = 0 to 3, 5, 6) registers corresponding to the activation source are set to 0 (activation disabled).

15.3.8 Operation Timings

The DTC requires nine clock cycles to read control data allocated in the DTC control data area. The number of clock cycles required to write back control data differs depending on the control data settings.
Figure 15.9 shows an Example of DTC Operation Timings and Figure 15.10 shows an Example of DTC Operation Timings in Chain Transfers. Table 15.8 lists the Specifications of Control Data Write-Back Operation.

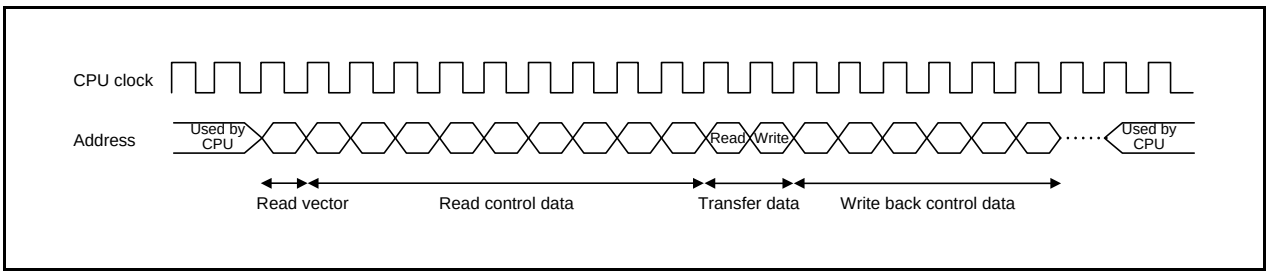


Figure 15.9 Example of DTC Operation Timings

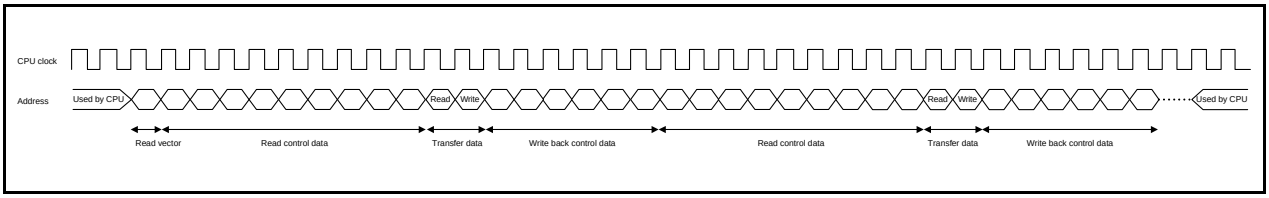


Figure 15.10 Example of DTC Operation Timings in Chain Transfers

Table 15.8 Specifications of Control Data Write-Back Operation

Bits b3 to b0 in DTCCR Register	Operating Mode	Address Control		Control Data to be Written Back				Number of Clock Cycles
		Source	Destination	DTCCTj Register	DTRLDj Register	DTSARj Register	DTDARj Register	
00X0b	Normal mode	Fixed	Fixed	Written back	Written back	Not written back	Not written back	2
01X0b		Incremented	Fixed	Written back	Written back	Written back	Not written back	4
10X0b		Fixed	Incremented	Written back	Written back	Not written back	Written back	4
11X0b		Incremented	Incremented	Written back	Written back	Written back	Written back	6
0X11b	Repeat mode	Repeat area	Fixed	Written back	Written back	Written back	Not written back	4
1X11b			Incremented	Written back	Written back	Written back	Written back	6
X001b		Fixed	Repeat area	Written back	Written back	Not written back	Written back	4
X101b		Incremented		Written back	Written back	Written back	Written back	6

j = 0 to 23
X: 0 or 1

15.3.9 Number of DTC Execution Cycles

Table 15.9 lists the Operations Following DTC Activation and Required Number of Cycles for each operation. Table 15.10 lists the Number of Clock Cycles Required for Data Transfers.

Table 15.9 Operations Following DTC Activation and Required Number of Cycles

Vector Read	Control Data		Data Read	Data Write	Internal Operation
	Read	Write-back			
1	9	(Note 2)	(Note 1)	(Note 1)	1

Notes:
1. For the number of clock cycles required for data read/write, refer to **Table 15.10 Number of Clock Cycles Required for Data Transfers**.
2. For the number of clock cycles required for control data write-back, refer to **Table 15.8 Specifications of Control Data Write-Back Operation**.

Data is transferred as described below, when the DTBLSj (j = 0 to 23) register = N,
(1) When N = 2n (even), two-byte transfers are performed n times.
(2) When N = 2n + 1 (odd), two-byte transfers are performed n times followed by one time of one-byte transfer.

Table 15.10 Number of Clock Cycles Required for Data Transfers

Operation	Unit of Transfers	Internal RAM (During DTC Transfers)	Internal ROM (Program ROM)	SFR (Word Access)		SFR (Byte Access)	SFR (DTC control data area)
				Even Address	Odd Address		
Data read	1-byte SK1	1	1	2		2	1
	2-byte SK2	2	2	2	4	4	2
Data write	1-byte SL1	1	—	2		2	1
	2-byte SL2	2	—	2	4	4	2

From Tables 15.9 and 15.10, the total number of required execution cycles can be obtained by the following formula:

Number of required execution cycles = 1 + Σ[formula A] + 1
Σ: Sum of the cycles for the number of transfer times performed by one activation source ([the number of transfer times for which CHNE is set to 1] + 1)
(1) For N = 2n (even)
Formula A = J + n • SK2 + n • SL2
(2) For N = 2n + 1 (odd)
Formula A = J + n • SK2 + 1 • SK1 + n • SL2 + 1 • SL1
J: Number of cycles required to read control data (9 cycles) + number of cycles required to write back control data

To read data from or write data to the register that to be accessed in 16-bit units, set an even value of 2 or greater to the DTBLSj (j = 0 to 23) register.
The DTC performs accesses in 16-bit units.

15.3.10 DTC Activation Source Acknowledgement and Interrupt Source Flags

15.3.10.1 Interrupt Sources Except for Flash Memory and Timer RC

When the DTC activation source is an interrupt source except for the flash memory or timer RC, the same DTC activation source cannot be acknowledged for 8 to 12 cycles of the CPU clock after the interrupt source is generated. If an interrupt source is generated when a software command is executed, the same DTC activation source cannot be acknowledged for 9 to 16 cycles of the CPU clock. If a DTC activation source is generated during DTC operation and acknowledged, the same DTC activation source cannot be acknowledged for 8 to 12 cycles of the CPU clock on completion of the DTC transfer immediately before the DTC is activated by the source. When a software command is executed on completion of the DTC transfer immediately before the DTC is activated, the same DTC activation source cannot be acknowledged for 16 cycles of the CPU clock.

15.3.10.2 Flash Memory

When the DTC activation source is flash ready status, even if a flash ready status interrupt request is generated, it is not acknowledged as the DTC activation source after the RDYSTI bit in the FST register is set to 1 (flash ready status interrupt request) and before the DTC sets the RDYSTI bit to 0 (no flash ready status interrupt request). If a flash ready status interrupt request is generated after the DTC sets the RDYSTI bit to 0, the DTC acknowledges it as the activation source. 8 to 12 cycles of the CPU clock are required after the RDYSTI bit is set to 1 and before the DTC sets the interrupt request flag to 0. If a flash ready status interrupt is generated when a software command is executed, 9 to 16 cycles of the CPU clock are required before the DTC sets the interrupt source flag to 0. If a flash ready status interrupt request is generated during DTC operation and acknowledged as the DTC activation source, the RDYSTI bit is set to 0 after 8 to 12 cycles of the CPU clock on completion of the DTC transfer immediately before the DTC is activated by the source. When a software command is executed on completion of the DTC transfer immediately before the DTC is activated, the RDYSTI bit is set to 0 after 16 cycles of the CPU clock.

15.3.10.3 Timer RC

When the DTC activation source is an interrupt source for timer RC, even if an input capture/compare match occurs, it is not acknowledged as the DTC activation source after the interrupt source flag is set to 1 and before the DTC sets the flag to 0. If an input capture/compare match occurs after the DTC sets the interrupt source flag to 0, the DTC acknowledges it as the activation source. 8 to 12 cycles of the CPU clock plus 0.5 to 1.5 cycles of the timer operating clock are required after the interrupt source flag is set to 1 and before the DTC sets the flag to 0. If the interrupt request flag is set to 1 when a software command is executed, 9 to 16 cycles of the CPU clock plus 0.5 to 1.5 cycles of the timer operating clock are required before the DTC sets the interrupt source flag to 0. If individual DTC activation sources are generated for timer RC during DTC operation and acknowledged, the interrupt source flag is set to 0 after 8 to 12 cycles of the CPU clock plus 0.5 to 1.5 cycles of the timer operating clock on completion of the DTC transfer immediately before the DTC is activated by the source. When a software command is executed on completion of the DTC transfer immediately before the DTC is activated, the interrupt source flag is set to 0 after 16 cycles of the CPU clock plus 0.5 to 1.5 cycles of the timer operating clock.

15.4 Notes on DTC

15.4.1 DTC activation source

- Do not generate any DTC activation sources before entering wait mode or during wait mode.
- Do not generate any DTC activation sources before entering stop mode or during stop mode.

15.4.2 DTCENi (i = 0 to 3, 5, 6) Registers

- Modify bits DTCENi0 to DTCENi7 only while an interrupt request corresponding to the bit is not generated.
- When the interrupt source flag in the status register for the peripheral function is 1, do not modify the corresponding activation source bit among bits DTCENi0 to DTCENi7.
- Do not access the DTCENi registers using DTC transfers.

15.4.3 Peripheral Modules

Do not set the status register bit for the peripheral function to 0 using a DTC transfer.

15.4.4 Interrupt Request

No interrupt is generated for the CPU during DTC operation in any of the following cases:
- When the DTC activation source is flash ready status
- When performing the data transfer causing the DTCCTj (j = 0 to 23) register value to change to 0 in normal mode
- When performing the data transfer causing the DTCCRj register value to change to 0 while the RPTINT bit in the DTCCRj register is 1 (interrupt generation enabled) in repeat mode

15.4.5 DTC Chain Transfers

When performing chain transfers using several control data, the number of transfers set to the first control data is enabled and the number of transfers proceeded after the first control data is disabled.
Examples:
- When DTCCT0 = 5 and DTCCT1 = 10, chain transfers are performed as DTCCT0 = DTCCT1 = 5.
- When DTCCT0 = 10 and DTCCT1 = 5, chain transfers are performed as DTCCT0 = DTCCT1 = 10.
- When DTCCT0 = 10, DTCCT1 = 5, and DTCCT2 = 2, chain transfers are performed as DTCCT0 = DTCCT1 = DTCCT2 = 10.

16. General Overview of Timers

The MCU has two 8-bit timers with 8-bit prescalers and a 16-bit timer. The two 8-bit timers with 8-bit prescalers are timer RA and timer RB. These timers contain a reload register to store the default value of the counter. The 16-bit timers are timer RC, and have input capture and output compare functions. All the timers operate independently.
Table 16.1 lists Functional Comparison of Timers.

Table 16.1 Functional Comparison of Timers

Item		Timer RA	Timer RB	Timer RC
Configuration		8-bit timer with 8-bit prescaler (with reload register)	8-bit timer with 8-bit prescaler (with reload register)	16-bit timer (with input capture and output compare)
Count		Decrement	Decrement	Increment
Count sources		• f1 • f2 • f8 • fOCO	• f1 • f2 • f8 • Timer RA underflow	• f1 • f2 • f4 • f8 • f32 • fOCO40M • fOCO-F • TRCCLK
Function	Count of the internal count source	Timer mode	Timer mode	Timer mode (output compare function)
	Count of the external count source	Event counter mode	—	Timer mode (output compare function)
	External pulse width/period measurement	Pulse width measurement mode, pulse period measurement mode	—	Timer mode (input capture function; 4 pins)
	PWM output	Pulse output mode (1), Event counter mode (1)	Programmable waveform generation mode	Timer mode (output compare function; 4 pins) (1), PWM mode (3 pins), PWM2 mode (1 pin)
	One-shot waveform output	—	Programmable one-shot generation mode, Programmable wait one-shot generation mode	PWM mode (3 pins)
	Three-phase waveforms output	—	—	—
	Timer	—	—	—
Input pin		TRAIO	$\overline{\text{INT0}}$	$\overline{\text{INT0}}$, TRCCLK, TRCTRG, TRCIOA, TRCIOB, TRCIOC, TRCIOD
Output pin		TRAO TRAIO	TRBO	TRCIOA, TRCIOB, TRCIOC, TRCIOD
Related interrupt		Timer RA interrupt	$\overline{\text{Timer}}$ RB interrupt, $\overline{\text{INT0}}$ interrupt	Compare match/input capture A to D interrupt, $\overline{\text{Overflow}}$ interrupt, $\overline{\text{INT0}}$ interrupt
Timer stop		Provided	Provided	Provided

Note:
1. Rectangular waves are output in these modes. Since the waves are inverted at each overflow, the “H” and “L” level widths of the pulses are the same.

17. Timer RA

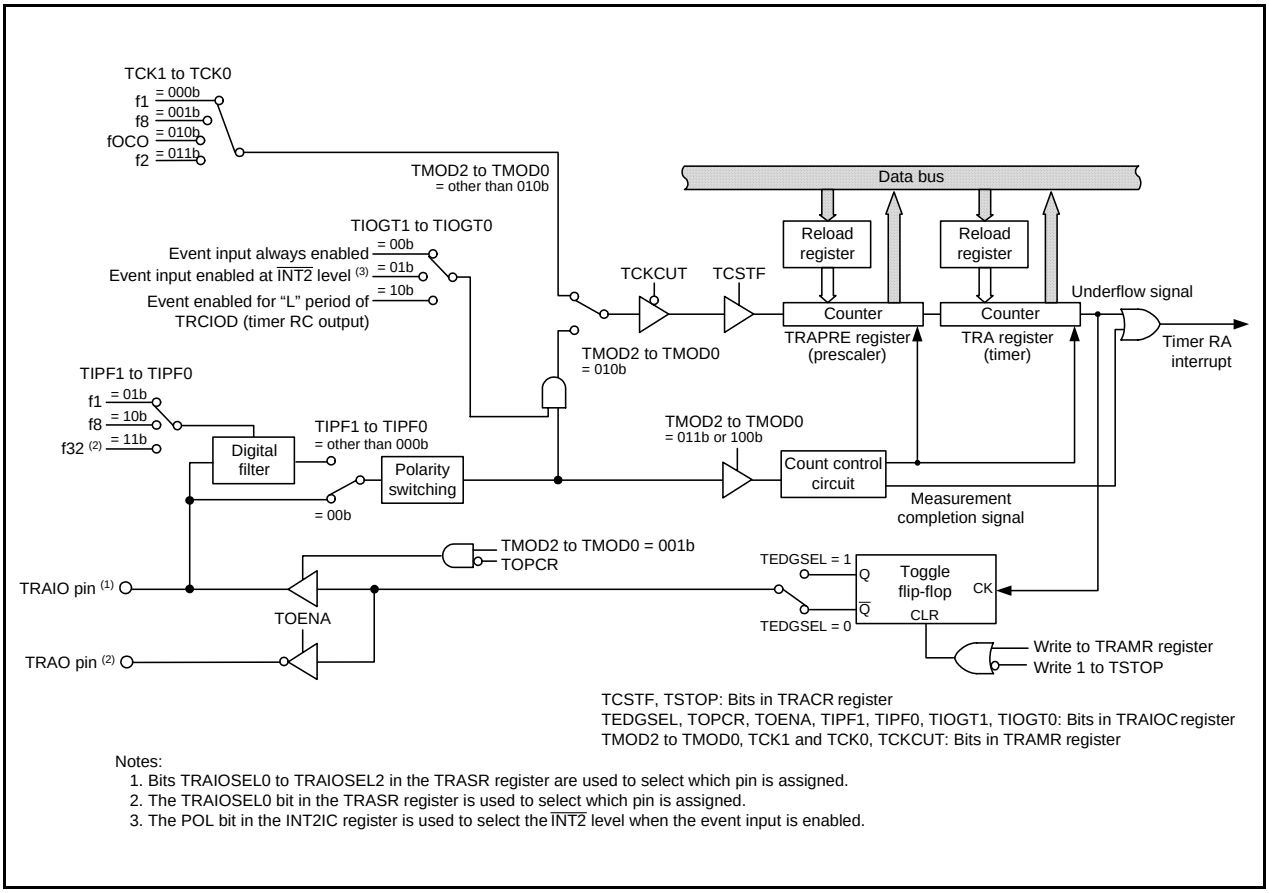
Timer RA is an 8-bit timer with an 8-bit prescaler.

17.1 Overview

The prescaler and timer each consist of a reload register and counter. The reload register and counter are allocated at the same address, and can be accessed when accessing registers TRAPRE and TRA (refer to **Tables 17.2 to 17.6 the Specification of Each Modes**).
The count source for timer RA is the operating clock that regulates the timing of timer operations such as counting and reloading.
Figure 17.1 shows a Timer RA Block Diagram. Table 17.1 lists the Pin Configuration of Timer RA.

Timer RA contains the following five operating modes:

- Timer mode: The timer counts the internal count source.
- Pulse output mode: The timer counts the internal count source and outputs pulses which invert the polarity by underflow of the timer.
- Event counter mode: The timer counts external pulses.
- Pulse width measurement mode: The timer measures the pulse width of an external pulse.
- Pulse period measurement mode: The timer measures the pulse period of an external pulse.



Notes:
1. Bits TRAIOSEL0 to TRAIOSEL2 in the TRASR register are used to select which pin is assigned.
2. The TRAIOSEL0 bit in the TRASR register is used to select which pin is assigned.
3. The POL bit in the INT2IC register is used to select the INT2 level when the event input is enabled.

Figure 17.1 Timer RA Block Diagram

Table 17.1 Pin Configuration of Timer RA

Pin Name	Assigned Pin	I/O	Function
TRAIO	P1_5, P1_7 or P3_5	I/O	Function differs according to the mode. Refer to descriptions of individual modes for details.
TRAO	P3_0 or P3_7	Output	

17.2 Registers

17.2.1 Timer RA Control Register (TRACR)

Address 0100h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	TUNDF	TEDGF	—	TSTOP	TCSTF	TSTART
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TSTART	Timer RA count start bit (1)	0: Count stops 1: Count starts	R/W
b1	TCSTF	Timer RA count status flag (1)	0: Count stops 1: During count	R
b2	TSTOP	Timer RA count forcible stop bit (2)	When this bit is set to 1, the count is forcibly stopped. When read, its content is 0.	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	TEDGF	Active edge judgment flag (3, 4)	0: Active edge not received 1: Active edge received (end of measurement period)	R/W
b5	TUNDF	Timer RA underflow flag (3)	0: No underflow 1: Underflow	R/W
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b7	—			

Notes:
1. Refer to **17.8 Notes on Timer RA** for precautions regarding bits TSTART and TCSTF.
2. When the TSTOP bit is set to 1, bits TSTART and TCSTF and registers TRAPRE and TRA are set to the values after a reset.
3. Bits TEDGF and TUNDF can be set to 0 by writing 0 to these bits by a program. However, their value remains unchanged when 1 is written.
4. The TEDGF bit is not used in timer mode, pulse output mode, or event count mode.

In pulse width measurement mode and pulse period measurement mode, use the MOV instruction to set the TRACR register. If it is necessary to avoid changing the values of bits TEDGF and TUNDF, write 1 to them.

17.2.2 Timer RA I/O Control Register (TRAIOC)

Address 0101h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TIOGT1	TIOGT0	TIPF1	TIPF0	—	TOENA	TOPCR	TEDGSEL
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TEDGSEL	TRAIO polarity switch bit	Function varies according to the operating mode.	R/W
b1	TOPCR	TRAIO output control bit		R/W
b2	TOENA	TRAO output enable bit		R/W
b3	—	Reserved bit	Set to 0.	R/W
b4	TIPF0	TRAIO input filter select bit	Function varies according to the operating mode.	R/W
b5	TIPF1			R/W
b6	TIOGT0	TRAIO event input control bit		R/W
b7	TIOGT1			R/W

17.2.3 Timer RA Mode Register (TRAMR)

Address 0102h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TCKCUT	—	TCK1	TCK0	—	TMOD2	TMOD1	TMOD0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TMOD0	Timer RA operating mode select bit	b2 b1 b0 0 0 0: Timer mode 0 0 1: Pulse output mode 0 1 0: Event counter mode 0 1 1: Pulse width measurement mode 1 0 0: Pulse period measurement mode 1 0 1: Do not set. 1 1 0: Do not set. 1 1 1: Do not set.	R/W
b1	TMOD1			R/W
b2	TMOD2			R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	TCK0	Timer RA count source select bit	b5 b4 0 0: f1 0 1: f8 1 0: fOCO 1 1: f2	R/W
b5	TCK1			R/W
b6	—	Reserved bit	Set to 0.	R/W
b7	TCKCUT	Timer RA count source cutoff bit	0: Provides count source 1: Cuts off count source	R/W

When both the TSTART and TCSTF bits in the TRACR register are set to 0 (count stops), rewrite this register.

17.2.4 Timer RA Prescaler Register (TRAPRE)

Address 0103h

Bit	b7	b6	b5	b4	b3	b2	b1	b0	
Symbol	—	—	—	—	—	—	—	—	
After Reset	1	1	1	1	1	1	1	1	(Note 1)

Bit	Mode	Function	Setting Range	R/W
b7 to b0	Timer mode	Counts an internal count source	00h to FFh	R/W
	Pulse output mode		00h to FFh	R/W
	Event counter mode	Counts an external count source	00h to FFh	R/W
	Pulse width measurement mode	Measure pulse width of input pulses from external (counts internal count source)	00h to FFh	R/W
	Pulse period measurement mode	Measure pulse period of input pulses from external (counts internal count source)	00h to FFh	R/W

Note:
1. When the TSTOP bit in the TRACR register is set to 1, the TRAPRE register is set to FFh.

17.2.5 Timer RA Register (TRA)

Address 0104h

Bit	b7	b6	b5	b4	b3	b2	b1	b0	
Symbol	—	—	—	—	—	—	—	—	
After Reset	1	1	1	1	1	1	1	1	(Note 1)

Bit	Mode	Function	Setting Range	R/W
b7 to b0	All modes	Counts on underflow of TRAPRE register	00h to FFh(2)	R/W

Notes:
1. When the TSTOP bit in the TRACR register is set to 1, the TRA register is set to FFh.
2. Do not set 00h to the TRA register in pulse width measurement mode and pulse period measurement mode.

17.2.6 Timer RA Pin Select Register (TRASR)

Address 0180h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	TRAOSEL0	TRAIOSEL2	TRAIOSEL1	TRAIOSEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TRAIOSEL0	TRAIO pin select bit	b2 b1 b0 0 0 0: TRAIO pin not used 0 0 1: P1_7 assigned 0 1 0: P1_5 assigned 1 0 1: P3_5 assigned Other than above: Do not set. (TRAIO pin not used.)	R/W
b1	TRAIOSEL1			R/W
b2	TRAIOSEL2			R/W
b3	TRAOSEL0	TRAO pin select bit	0: P3_7 assigned 1: P3_0 assigned	R/W
b4	—	Reserved bit	Set to 0.	R/W
b5	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b6	—			
b7	—			

The TRASR register selects which pin is assigned to the timer RA I/O. To use the I/O pin for timer RA, set this register.
Set the TRASR register before setting the timer RA associated registers. Also, do not change the setting value in this register during timer RA operation.
Change the TRASR register from the initial value to any value during the initial setting of the user's program. Do not change this register again while the main program is executed.

17.3 Timer Mode

In this mode, the timer counts an internally generated count source (refer to **Table 17.2 Timer Mode Specifications**).

Table 17.2 Timer Mode Specifications

Item	Specification
Count sources	f1, f2, f8, fOCO
Count operations	• Decrement • When the timer underflows, the contents of the reload register are reloaded and the count is continued.
Divide ratio	1/(n+1)(m+1) n: Value set in TRAPRE register, m: Value set in TRA register
Count start condition	1 (count starts) is written to the TSTART bit in the TRACR register.
Count stop conditions	• 0 (count stops) is written to the TSTART bit in the TRACR register. • 1 (count forcibly stops) is written to the TSTOP bit in the TRACR register.
Interrupt request generation timing	When timer RA underflows [timer RA interrupt].
TRAIO pin function	Programmable I/O port
TRAO pin function	Programmable I/O port
Read from timer	The count value can be read by reading registers TRA and TRAPRE.
Write to timer	• When registers TRAPRE and TRA are written while the count is stopped, values are written to both the reload register and counter. • When registers TRAPRE and TRA are written during the count, values are written to the reload register and counter (refer to **17.3.2 Timer Write Control during Count Operation**).

17.3.1 Timer RA I/O Control Register (TRAIOC) in Timer Mode

Address 0101h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TIOGT1	TIOGT0	TIPF1	TIPF0	—	TOENA	TOPCR	TEDGSEL
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TEDGSEL	TRAIO polarity switch bit	Set to 0 in timer mode.	R/W
b1	TOPCR	TRAIO output control bit		R/W
b2	TOENA	TRAO output enable bit		R/W
b3	—	Reserved bit	Set to 0.	R/W
b4	TIPF0	TRAIO input filter select bit	Set to 0 in timer mode.	R/W
b5	TIPF1			R/W
b6	TIOGT0	TRAIO event input control bit		R/W
b7	TIOGT1			R/W

17.3.2 Timer Write Control during Count Operation

Timer RA has a prescaler and a timer (which counts the prescaler underflows). The prescaler and timer each consist of a reload register and a counter. When writing to the prescaler or timer, values are written to both the reload register and counter.

However, values are transferred from the reload register to the counter of the prescaler in synchronization with the count source. In addition, values are transferred from the reload register to the counter of the timer in synchronization with prescaler underflows. Therefore, if the prescaler or timer is written to when count operation is in progress, the counter value is not updated immediately after the WRITE instruction is executed.

Figure 17.2 shows an Operating Example of Timer RA when Counter Value is Rewritten during Count Operation.

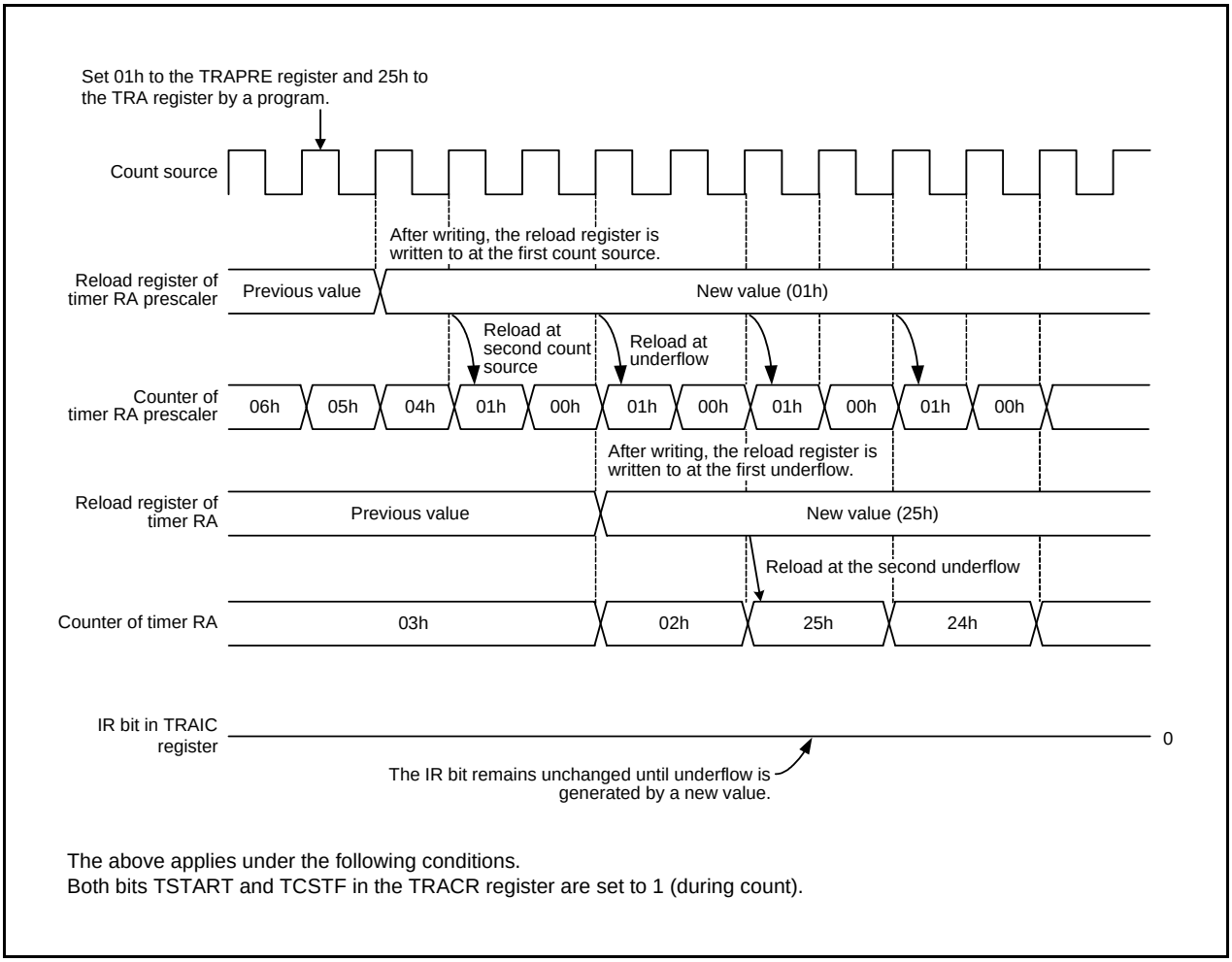


Figure 17.2 Operating Example of Timer RA when Counter Value is Rewritten during Count Operation

17.4 Pulse Output Mode

In pulse output mode, the internally generated count source is counted, and a pulse with inverted polarity is output from the TRAIO pin each time the timer underflows (refer to **Table 17.3 Pulse Output Mode Specifications**).

Table 17.3 Pulse Output Mode Specifications

Item	Specification
Count sources	f1, f2, f8, fOCO
Count operations	• Decrement • When the timer underflows, the contents in the reload register is reloaded and the count is continued.
Divide ratio	1/(n+1)(m+1) n: Value set in TRAPRE register, m: Value set in TRA register
Count start condition	1 (count starts) is written to the TSTART bit in the TRACR register.
Count stop conditions	• 0 (count stops) is written to the TSTART bit in the TRACR register. • 1 (count forcibly stops) is written to the TSTOP bit in the TRACR register.
Interrupt request generation timing	When timer RA underflows [timer RA interrupt].
TRAIO pin function	Pulse output, programmable output port
TRAO pin function	Programmable I/O port or inverted output of TRAIO
Read from timer	The count value can be read by reading registers TRA and TRAPRE.
Write to timer	• When registers TRAPRE and TRA are written while the count is stopped, values are written to both the reload register and counter. • When registers TRAPRE and TRA are written during the count, values are written to the reload register and counter (refer to **17.3.2 Timer Write Control during Count Operation**).
Selectable functions	• TRAIO signal polarity switch function The level when the pulse output starts is selected by the TEDGSEL bit in the TRAIOC register. (1) • TRAO output function Pulses inverted from the TRAIO output polarity can be output from the TRAO pin (selectable by the TOENA bit in the TRAIOC register). • Pulse output stop function Output from the TRAIO pin is stopped by the TOPCR bit in the TRAIOC register. • TRAIO pin select function P1_5, P1_7, or P3_5 is selected by bits TRAIOSEL0 to TRAIOSEL2 in the TRASR register.

Note:
1. The level of the output pulse becomes the level when the pulse output starts when the TRAMR register is written to.

17.4.1 Timer RA I/O Control Register (TRAIOC) in Pulse Output Mode

Address 0101h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TIOGT1	TIOGT0	TIPF1	TIPF0	—	TOENA	TOPCR	TEDGSEL
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TEDGSEL	TRAIO polarity switch bit	0: TRAIO output starts at “H” 1: TRAIO output starts at “L”	R/W
b1	TOPCR	TRAIO output control bit	0: TRAIO output 1: TRAIO output disabled	R/W
b2	TOENA	TRAO output enable bit	0: TRAO output disabled 1: TRAO output (inverted TRAIO output from the port)	R/W
b3	—	Reserved bit	Set to 0.	R/W
b4	TIPF0	TRAIO input filter select bit	Set to 0 in pulse output mode.	R/W
b5	TIPF1			R/W
b6	TIOGT0	TRAIO event input control bit		R/W
b7	TIOGT1			R/W

17.5 Event Counter Mode

In event counter mode, external signal inputs to the TRAIO pin are counted (refer to **Table 17.4 Event Counter Mode Specifications**).

Table 17.4 Event Counter Mode Specifications

Item	Specification
Count source	External signal which is input to TRAIO pin (active edge selectable by a program)
Count operations	• Decrement • When the timer underflows, the contents of the reload register are reloaded and the count is continued.
Divide ratio	1/(n+1)(m+1) n: setting value of TRAPRE register, m: setting value of TRA register
Count start condition	1 (count starts) is written to the TSTART bit in the TRACR register.
Count stop conditions	• 0 (count stops) is written to the TSTART bit in the TRACR register. • 1 (count forcibly stops) is written to the TSTOP bit in the TRACR register.
Interrupt request generation timing	When timer RA underflows [timer RA interrupt].
TRAIO pin function	Count source input
TRAO pin function	Programmable I/O port or pulse output (1)
Read from timer	The count value can be read by reading registers TRA and TRAPRE.
Write to timer	• When registers TRAPRE and TRA are written while the count is stopped, values are written to both the reload register and counter. • When registers TRAPRE and TRA are written during the count, values are written to the reload register and counter (refer to **17.3.2 Timer Write Control during Count Operation**).
Selectable functions	• TRAIO input polarity switch function The active edge of the count source is selected by the TEDGSEL bit in the TRAIOC register. • Count source input pin select function P1_5, P1_7, or P3_5 is selected by bits TRAIOSEL0 to TRAIOSEL2 in the TRASR register. • Pulse output function Pulses of inverted polarity can be output from the TRAO pin each time the timer underflows (selectable by the TOENA bit in the TRAIOC register). (1) • Digital filter function Whether enabling or disabling the digital filter and the sampling frequency is selected by bits TIPF0 and TIPF1 in the TRAIOC register. • Event input control function The enabled period for the event input to the TRAIO pin is selected by bits TIOGT0 and TIOGT1 in the TRAIOC register.

Note:
1. The level of the output pulse becomes the level when the pulse output starts when the TRAMR register is written to.

17.5.1 Timer RA I/O Control Register (TRAIOC) in Event Counter Mode

Address 0101h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TIOGT1	TIOGT0	TIPF1	TIPF0	—	TOENA	TOPCR	TEDGSEL
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TEDGSEL	TRAIO polarity switch bit	0: Starts counting at rising edge of the TRAIO input and TRAO starts output at “L” 1: Starts counting at falling edge of the TRAIO input and TRAO starts output at “H”	R/W
b1	TOPCR	TRAIO output control bit	Set to 0 in event counter mode.	R/W
b2	TOENA	TRAO output enable bit	0: TRAO output disabled 1: TRAO output	R/W
b3	—	Reserved bit	Set to 0.	R/W
b4	TIPF0	TRAIO input filter select bit (1)	b5 b4 0 0: No filter 0 1: Filter with f1 sampling 1 0: Filter with f8 sampling 1 1: Filter with f32 sampling	R/W
b5	TIPF1			R/W
b6	TIOGT0	TRAIO event input control bit	b7 b6 0 0: Event input always enabled 0 1: Event input enabled at $\overline{\text{INT2}}$ level (2) 1 0: Event input enabled for “L” period of TRCIOD (timer RC output) 1 1: Do not set.	R/W
b7	TIOGT1			R/W

Notes:
1. When the same value from the TRAIO pin is sampled three times continuously, the input is determined.
2. Make the following settings to use event input enabled at $\overline{\text{INT2}}$ level:
   - Set the $\overline{\text{INT2}}$EN bit in the INTEN register to 1 ($\overline{\text{INT2}}$ input enabled) and the INT2PL bit to 0 (one edge).
   - Set the $\overline{\text{INT2}}$ polarity by the POL bit in the INT2IC register.
     When the POL bit is set 0 (falling edge selected), the event input for the $\overline{\text{INT2}}$ high-level period is enabled.
     When the POL bit is set 1 (rising edge selected), the event input for the $\overline{\text{INT2}}$ low-level period is enabled.
   - Set the PD3_2 bit in the PD3 register for the port assigned as the $\overline{\text{INT2}}$ pin to 0 (input mode).
   - Select the $\overline{\text{INT2}}$ digital filter by bits INT2F1 to INT2F0 in the INTF register.

   The IR bit in the INT2IC register is set to 1 (interrupt request) in accordance with the setting of the POL bit in the INT2IC register and the INT2PL bit in the INTEN register and a change in the $\overline{\text{INT2}}$ pin input (refer to **11.9 Notes on Interrupts**).
   For details on interrupts, refer to **11. Interrupts**.

17.6 Pulse Width Measurement Mode

In pulse width measurement mode, the pulse width of an external signal input to the TRAIO pin is measured (refer to **Table 17.5 Pulse Width Measurement Mode Specifications**).
Figure 17.3 shows an Operating Example of Pulse Width Measurement Mode.

Table 17.5 Pulse Width Measurement Mode Specifications

Item	Specification
Count sources	f1, f2, f8, fOCO
Count operations	• Decrement • Continuously counts the selected signal only when measurement pulse is “H” level, or conversely only “L” level. • When the timer underflows, the contents of the reload register are reloaded and the count is continued.
Count start condition	1 (count starts) is written to the TSTART bit in the TRACR register.
Count stop conditions	• 0 (count stops) is written to the TSTART bit in the TRACR register. • 1 (count forcibly stops) is written to the TSTOP bit in the TRACR register.
Interrupt request generation timing	• When timer RA underflows [timer RA interrupt]. • Rising or falling of the TRAIO input (end of measurement period) [timer RA interrupt].
TRAIO pin function	Measured pulse input
TRAO pin function	Programmable I/O port
Read from timer	The count value can be read by reading registers TRA and TRAPRE.
Write to timer	• When registers TRAPRE and TRA are written while the count is stopped, values are written to both the reload register and counter. • When registers TRAPRE and TRA are written during the count, values are written to the reload register and counter (refer to **17.3.2 Timer Write Control during Count Operation**).
Selectable functions	• Measurement level setting The “H” level or “L” level period is selected by the TEDGSEL bit in the TRAIOC register. • Measured pulse input pin select function P1_5, P1_7, or P3_5 is selected by bits TRAIOSEL0 to TRAIOSEL2 in the TRASR register. • Digital filter function Whether enabling or disabling the digital filter and the sampling frequency is selected by bits TIPF0 and TIPF1 in the TRAIOC register.

17.6.1 Timer RA I/O Control Register (TRAIOC) in Pulse Width Measurement Mode

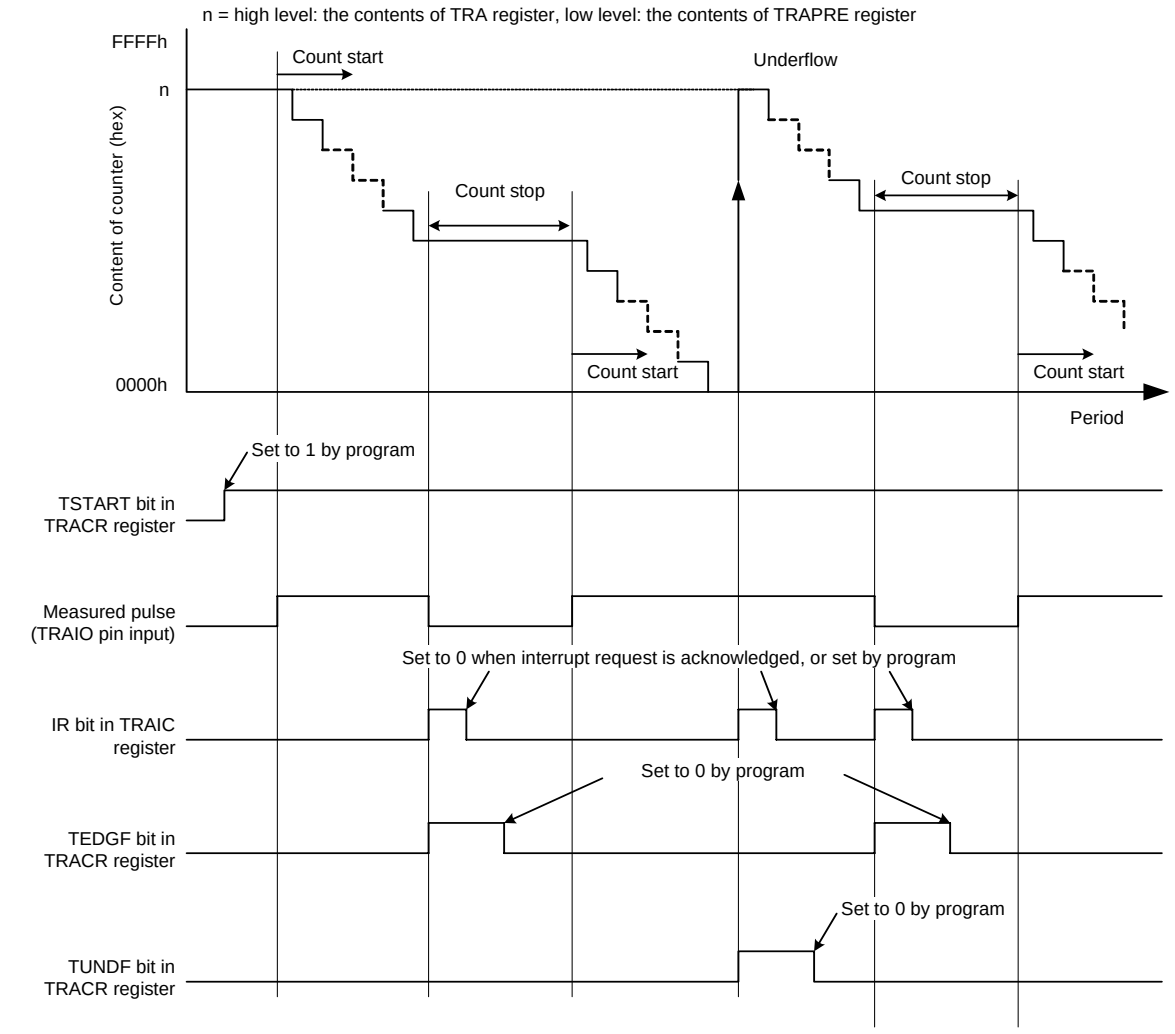
Address 0101h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TIOGT1	TIOGT0	TIPF1	TIPF0	—	TOENA	TOPCR	TEDGSEL
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TEDGSEL	TRAIO polarity switch bit	0: TRAIO input starts at “L” 1: TRAIO input starts at “H”	R/W
b1	TOPCR	TRAIO output control bit	Set to 0 in pulse width measurement mode.	R/W
b2	TOENA	TRAO output enable bit		R/W
b3	—	Reserved bit	Set to 0.	R/W
b4	TIPF0	TRAIO input filter select bit (1)	b5 b4 0 0: No filter 0 1: Filter with f1 sampling 1 0: Filter with f8 sampling 1 1: Filter with f32 sampling	R/W
b5	TIPF1			R/W
b6	TIOGT0	TRAIO event input control bit	Set to 0 in pulse width measurement mode.	R/W
b7	TIOGT1			R/W

Note:
1. When the same value from the TRAIO pin is sampled three times continuously, the input is determined.

17.6.2 Operating Example



The above applies under the following conditions.
- "H" level width of measured pulse is measured. (TEDGSEL = 1)
- TRAPRE = FFh

Figure 17.3 Operating Example of Pulse Width Measurement Mode

17.7 Pulse Period Measurement Mode

In pulse period measurement mode, the pulse period of an external signal input to the TRAIO pin is measured (refer to **Table 17.6 Pulse Period Measurement Mode Specifications**).
Figure 17.4 shows an Operating Example of Pulse Period Measurement Mode.

Table 17.6 Pulse Period Measurement Mode Specifications

Item	Specification
Count sources	f1, f2, f8, fOCO
Count operations	• Decrement • After the active edge of the measured pulse is input, the contents of the read-out buffer are retained at the first underflow of timer RA prescaler. Then timer RA reloads the contents in the reload register at the second underflow of timer RA prescaler and continues counting.
Count start condition	1 (count starts) is written to the TSTART bit in the TRACR register.
Count stop conditions	• 0 (count stops) is written to TSTART bit in the TRACR register. • 1 (count forcibly stops) is written to the TSTOP bit in the TRACR register.
Interrupt request generation timing	• When timer RA underflows or reloads [timer RA interrupt]. • Rising or falling of the TRAIO input (end of measurement period) [timer RA interrupt].
TRAIO pin function	Measured pulse input (1)
TRAO pin function	Programmable I/O port
Read from timer	The count value can be read by reading registers TRA and TRAPRE.
Write to timer	• When registers TRAPRE and TRA are written while the count is stopped, values are written to both the reload register and counter. • When registers TRAPRE and TRA are written during the count, values are written to the reload register and counter (refer to **17.3.2 Timer Write Control during Count Operation**).
Selectable functions	• Measurement period selection The measurement period of the input pulse is selected by the TEDGSEL in the TRAIOC register. • Measured pulse input pin select function P1_5, P1_7, or P3_5 is selected by bits TRAIOSEL0 to TRAIOSEL2 in the TRASR register. • Digital filter function Whether enabling or disabling the digital filter and the sampling frequency is selected by bits TIPF0 and TIPF1 in the TRAIOC register.

Note:
1. Input a pulse with a period longer than twice the timer RA prescaler period. Input a pulse with a longer “H” and “L” width than the timer RA prescaler period. If a pulse with a shorter period is input to the TRAIO pin, the input may be ignored.

17.7.1 Timer RA I/O Control Register (TRAIOC) in Pulse Period Measurement Mode

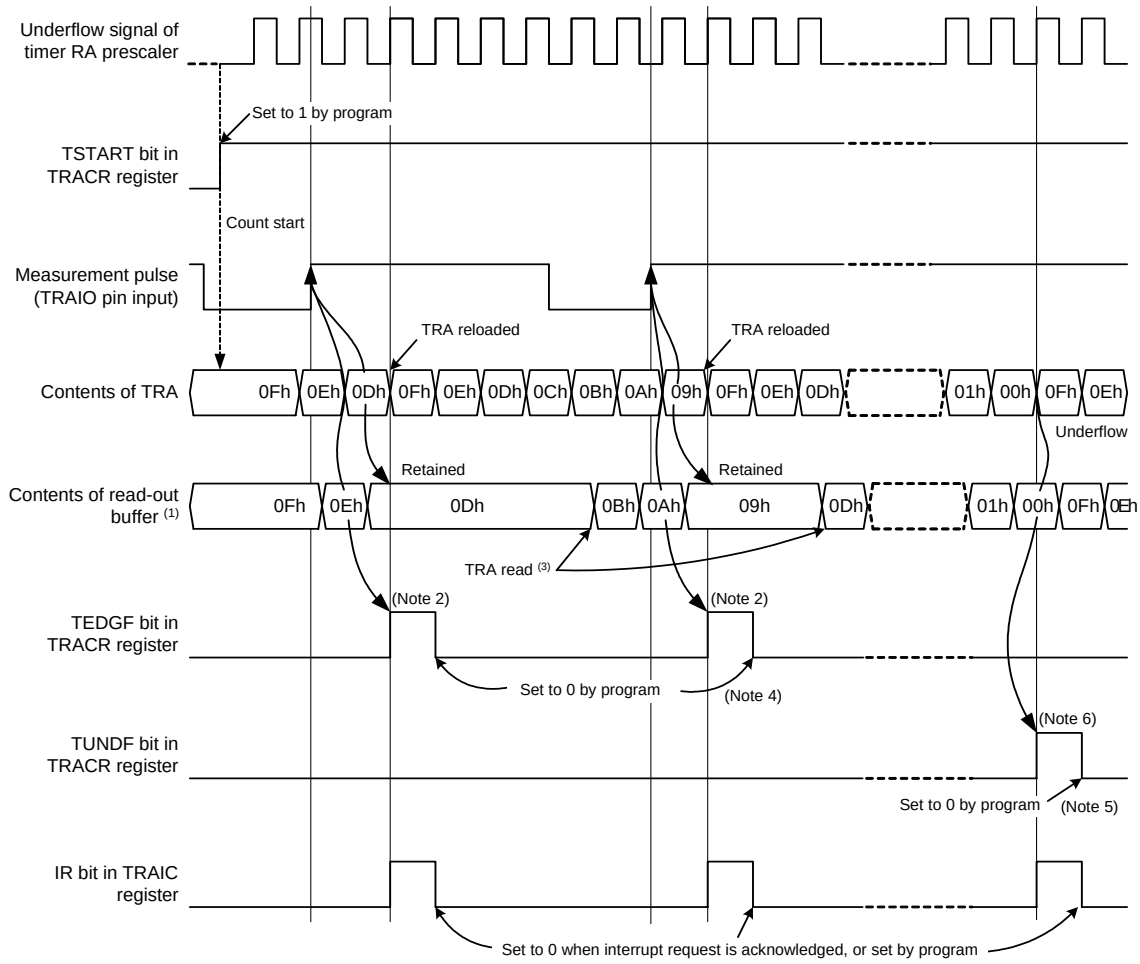
Address 0101h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TIOGT1	TIOGT0	TIPF1	TIPF0	—	TOENA	TOPCR	TEDGSEL
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TEDGSEL	TRAIO polarity switch bit	0: Measures measurement pulse from one rising edge to next rising edge 1: Measures measurement pulse from one falling edge to next falling edge	R/W
b1	TOPCR	TRAIO output control bit	Set to 0 in pulse period measurement mode.	R/W
b2	TOENA	TRAO output enable bit		R/W
b3	—	Reserved bit	Set to 0.	R/W
b4	TIPF0	TRAIO input filter select bit (1)	b5 b4 0 0: No filter 0 1: Filter with f1 sampling 1 0: Filter with f8 sampling 1 1: Filter with f32 sampling	R/W
b5	TIPF1			R/W
b6	TIOGT0	TRAIO event input control bit	Set to 0 in pulse period measurement mode.	R/W
b7	TIOGT1			R/W

Note:
1. When the same value from the TRAIO pin is sampled three times continuously, the input is determined.

17.7.2 Operating Example



Conditions: The period from one rising edge to the next rising edge of the measured pulse is measured (TEDGSEL = 0) with the default value of the TRA register as 0Fh.

Notes:
1. The contents of the read-out buffer can be read by reading the TRA register in pulse period measurement mode.
2. After an active edge of the measured pulse is input, the TEDGF bit in the TRACR register is set to 1 (active edge received) when the timer RA prescaler underflows for the second time.
3. The TRA register should be read before the next active edge is input after the TEDGF bit is set to 1 (active edge received). The contents in the read-out buffer are retained until the TRA register is read. If the TRA register is not read before the next active edge is input, the measured result of the previous period is retained.
4. To set to 0 by a program, use a MOV instruction to write 0 to the TEDGF bit in the TRACR register. At the same time, write 1 to the TUNDF bit in the TRACR register.
5. To set to 0 by a program, use a MOV instruction to write 0 to the TUNDF bit. At the same time, write 1 to the TEDGF bit.
6. Bits TUNDF and TEDGF are both set to 1 if timer RA underflows and reloads on an active edge simultaneously.

Figure 17.4 Operating Example of Pulse Period Measurement Mode

17.8 Notes on Timer RA

- Timer RA stops counting after a reset. Set the values in the timer RA and timer RA prescalers before the count starts.
- Even if the prescaler and timer RA are read out in 16-bit units, these registers are read 1 byte at a time by the MCU. Consequently, the timer value may be updated during the period when these two registers are being read.
- In pulse width measurement mode and pulse period measurement mode, bits TEDGF and TUNDF in the TRACR register can be set to 0 by writing 0 to these bits by a program. However, these bits remain unchanged if 1 is written. When using the READ-MODIFY-WRITE instruction for the TRACR register, the TEDGF or TUNDF bit may be set to 0 although these bits are set to 1 while the instruction is being executed. In this case, write 1 to the TEDGF or TUNDF bit which is not supposed to be set to 0 with the MOV instruction.
- When changing to pulse period measurement mode from another mode, the contents of bits TEDGF and TUNDF are undefined. Write 0 to bits TEDGF and TUNDF before the count starts.
- The TEDGF bit may be set to 1 by the first timer RA prescaler underflow generated after the count starts.
- When using the pulse period measurement mode, leave two or more periods of the timer RA prescaler immediately after the count starts, then set the TEDGF bit to 0.
- The TCSTF bit retains 0 (count stops) for 0 to 1 cycle of the count source after setting the TSTART bit to 1 (count starts) while the count is stopped.

  During this time, do not access registers associated with timer RA (1) other than the TCSTF bit. Timer RA starts counting at the first valid edge of the count source after the TCSTF bit is set to 1 (during count).

  The TCSTF bit remains 1 for 0 to 1 cycle of the count source after setting the TSTART bit to 0 (count stops) while the count is in progress. Timer RA counting is stopped when the TCSTF bit is set to 0.

  During this time, do not access registers associated with timer RA (1) other than the TCSTF bit.

  Note:
  1. Registers associated with timer RA: TRACR, TRAIOC, TRAMR, TRAPRE, and TRA.

- When the TRAPRE register is continuously written during count operation (TCSTF bit is set to 1), allow three or more cycles of the count source clock for each write interval.
- When the TRA register is continuously written during count operation (TCSTF bit is set to 1), allow three or more cycles of the prescaler underflow for each write interval.
- Do not set 00h to the TRA register in pulse width measurement mode and pulse period measurement mode.

18. Timer RB

Timer RB is an 8-bit timer with an 8-bit prescaler.

18.1 Overview

The prescaler and timer each consist of a reload register and counter (refer to **Tables 18.2 to 18.5 the Specifications of Each Mode**). Timer RB has timer RB primary and timer RB secondary as reload registers.
The count source for timer RB is the operating clock that regulates the timing of timer operations such as counting and reloading.
Figure 18.1 shows a Timer RB Block Diagram. Table 18.1 lists Pin Configuration of Timer RB.

Timer RB has four operation modes listed as follows:

- Timer mode: The timer counts an internal count source (peripheral function clock or timer RA underflows).
- Programmable waveform generation mode: The timer outputs pulses of a given width successively.
- Programmable one-shot generation mode: The timer outputs a one-shot pulse.
- Programmable wait one-shot generation mode: The timer outputs a delayed one-shot pulse.

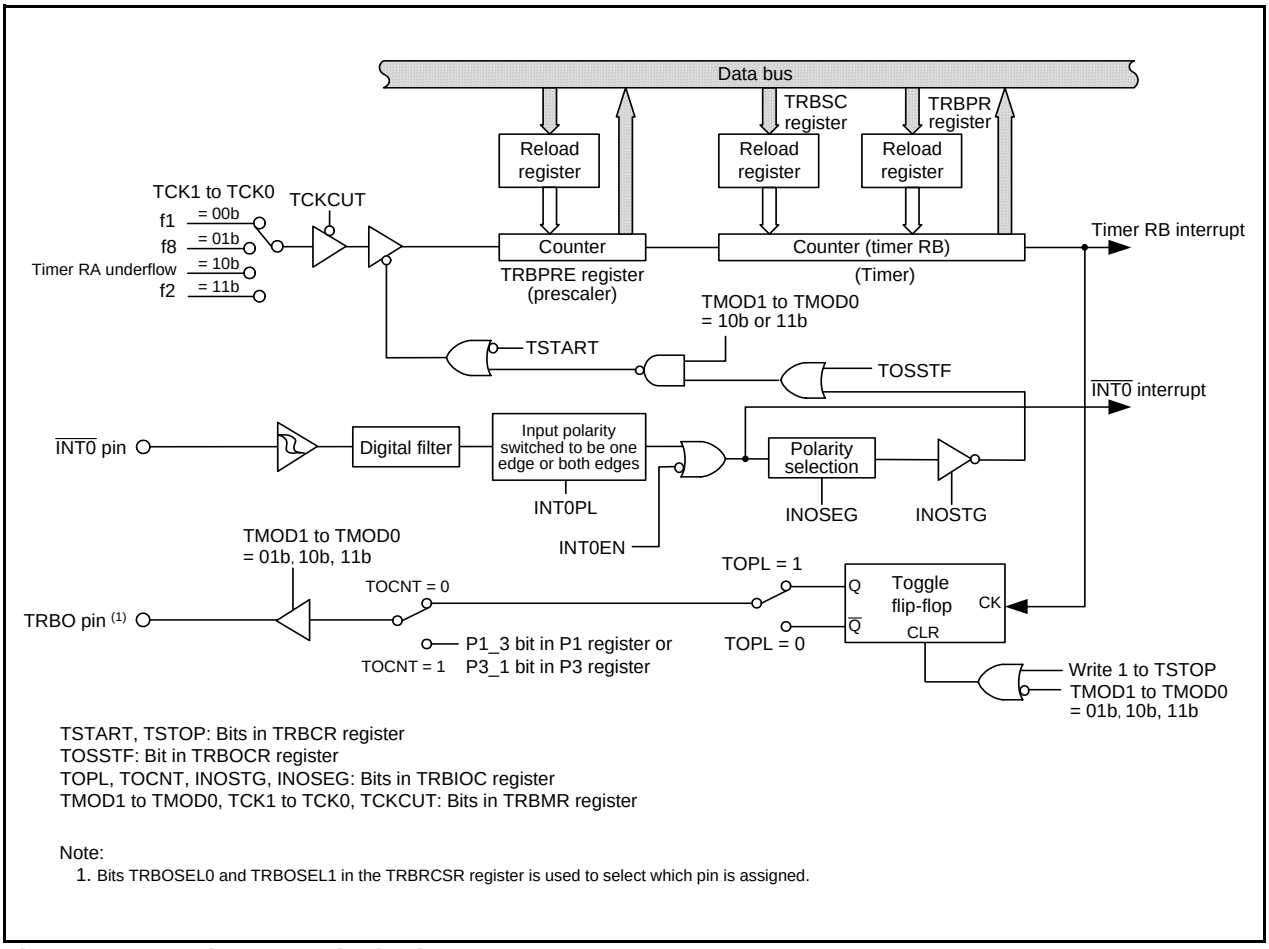


Figure 18.1 Timer RB Block Diagram

Table 18.1 Pin Configuration of Timer RB

Pin Name	Assigned Pin	I/O	Function
TRBO	P1_3, P3_1, or P3_3	Output	Pulse output (programmable waveform generation mode, programmable one-shot generation mode, programmable wait one-shot generation mode)

18.2 Registers

18.2.1 Timer RB Control Register (TRBCR)

Address 0108h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	TSTOP	TCSTF	TSTART
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TSTART	Timer RB count start bit (1)	0: Count stops 1: Count starts	R/W
b1	TCSTF	Timer RB count status flag (1)	0: Count stops 1: During count (3)	R
b2	TSTOP	Timer RB count forcible stop bit (1, 2)	When this bit is set to 1, the count is forcibly stopped. When read, the content is 0.	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	—			
b5	—			
b6	—			
b7	—			

Notes:
1. Refer to **18.7 Notes on Timer RB** for precautions regarding bits TSTART, TCSTF and TSTOP.
2. When the TSTOP bit is set to 1, registers TRBPRE, TRBSC, TRBPR, and bits TSTART and TCSTF, and the TOSSTF bit in the TRBOCR register are set to values after a reset.
3. Indicates that count operation is in progress in timer mode or programmable waveform mode. In programmable one-shot generation mode or programmable wait one-shot generation mode, indicates that a one-shot pulse trigger has been acknowledged.

18.2.2 Timer RB One-Shot Control Register (TRBOCR)

Address 0109h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	TOSSTF	TOSSP	TOSST
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TOSST	Timer RB one-shot start bit	When this bit is set to 1, one-shot trigger generated. When read, its content is 0.	R/W
b1	TOSSP	Timer RB one-shot stop bit	When this bit is set to 1, counting of one-shot pulses (including programmable wait one-shot pulses) stops. When read, the content is 0.	R/W
b2	TOSSTF	Timer RB one-shot status flag (1)	0: One-shot stopped 1: One-shot operating (Including wait period)	R
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	—			
b5	—			
b6	—			
b7	—			

Note:
1. When 1 is set to the TSTOP bit in the TRBCR register, the TOSSTF bit is set to 0.

This register is enabled when bits TMOD1 to TMOD0 in the TRBMR register is set to 10b (programmable one-shot generation mode) or 11b (programmable wait one-shot generation mode).

18.2.3 Timer RB I/O Control Register (TRBIOC)

Address 010Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	INOSEG	INOSTG	TOCNT	TOPL
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TOPL	Timer RB output level select bit	Function varies according to the operating mode.	R/W
b1	TOCNT	Timer RB output switch bit		R/W
b2	INOSTG	One-shot trigger control bit		R/W
b3	INOSEG	One-shot trigger polarity select bit		R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b5	—			
b6	—			
b7	—			

18.2.4 Timer RB Mode Register (TRBMR)

Address 010Bh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TCKCUT	—	TCK1	TCK0	TWRC	—	TMOD1	TMOD0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TMOD0	Timer RB operating mode select bit (1)	b1 b0 0 0: Timer mode 0 1: Programmable waveform generation mode 1 0: Programmable one-shot generation mode 1 1: Programmable wait one-shot generation mode	R/W
b1	TMOD1			R/W
b2	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b3	TWRC	Timer RB write control bit (2)	0: Write to reload register and counter 1: Write to reload register only	R/W
b4	TCK0	Timer RB count source select bit (1)	b5 b4 0 0: f1 0 1: f8 1 0: Timer RA underflow (3) 1 1: f2	R/W
b5	TCK1			R/W
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b7	TCKCUT	Timer RB count source cutoff bit (1)	0: Provides count source 1: Cuts off count source	R/W

Notes:
1. Change bits TMOD1 and TMOD0; TCK1 and TCK0; and TCKCUT when both the TSTART and TCSTF bits in the TRBCR register are set to 0 (count stops).
2. The TWRC bit can be set to either 0 or 1 in timer mode. In programmable waveform generation mode, programmable one-shot generation mode, or programmable wait one-shot generation mode, the TWRC bit must be set to 1 (write to reload register only).
3. To use the underflow signal of timer RA as the count source for timer RB, set timer RA in timer mode, pulse output mode, or event count mode.

18.2.5 Timer RB Prescaler Register (TRBPRE)

Address 010Ch

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	Mode	Function	Setting Range	R/W
b7 to b0	Timer mode	Counts an internal count source or timer RA underflows	00h to FFh	R/W
	Programmable waveform generation mode		00h to FFh	R/W
	Programmable one-shot generation mode		00h to FFh	R/W
	Programmable wait one-shot generation mode		00h to FFh	R/W

When the TSTOP bit in the TRBCR register is set to 1, the TRBPRE register is set to FFh.

18.2.6 Timer RB Secondary Register (TRBSC)

Address 010Dh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	Mode	Function	Setting Range	R/W
b7 to b0	Timer mode	Disabled	00h to FFh	—
	Programmable waveform generation mode	Counts timer RB prescaler underflows (1)	00h to FFh	W (2)
	Programmable one-shot generation mode	Disabled	00h to FFh	—
	Programmable wait one-shot generation mode	Counts timer RB prescaler underflows (one-shot width is counted)	00h to FFh	W (2)

Notes:
1. The values of registers TRBPR and TRBSC are reloaded to the counter alternately and counted.
2. The count value can be read out by reading the TRBPR register even when the secondary period is being counted.

When the TSTOP bit in the TRBCR register is set to 1, the TRBSC register is set to FFh.
To write to the TRBSC register, perform the following steps.
(1) Write the value to the TRBSC register.
(2) Write the value to the TRBPR register. (If the value does not change, write the same value second time.)

18.2.7 Timer RB Primary Register (TRBPR)

Address 010Eh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	Mode	Function	Setting Range	R/W
b7 to b0	Timer mode	Counts timer RB prescaler underflows	00h to FFh	R/W
	Programmable waveform generation mode	Counts timer RB prescaler underflows (1)	00h to FFh	R/W
	Programmable one-shot generation mode	Counts timer RB prescaler underflows (one-shot width is counted)	00h to FFh	R/W
	Programmable wait one-shot generation mode	Counts timer RB prescaler underflows (wait period width is counted)	00h to FFh	R/W

Note:
1. The values of registers TRBPR and TRBSC are reloaded to the counter alternately and counted.

When the TSTOP bit in the TRBCR register is set to 1, the TRBPR register is set to FFh.

18.2.8 Timer RB/RC Pin Select Register (TRBRCSR)

Address 0181h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	TRCCLKSEL1	TRCCLKSEL0	—	TRBOSEL2	TRBOSEL1	TRBOSEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TRBOSEL0	TRBO pin select bit	b2 b1 b0 0 0 0: P1_3 assigned 0 0 1: P3_1 assigned 0 1 0: Do not set. (TRBO pin not used) 0 1 1: P3_3 assigned Other than above: Do not set. (TRBO pin not used.)	R/W
b1	TRBOSEL1			R/W
b2	TRBOSEL2			R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	TRCCLKSEL0	TRCCLK pin select bit	b5 b4 0 0: TRCCLK pin not used 0 1: P1_4 assigned 1 0: P3_3 assigned 1 1: P3_7 assigned	R/W
b5	TRCCLKSEL1			R/W
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b7	—			—

The TRBRCSR register selects which pin is assigned to the timer RB and timer RC I/O. To use the I/O pin for timer RB and timer RC, set this register.
Set the TRBOSEL0 bit before setting the timer RB associated registers. Set bits TRCCLKSEL0 and TRCCLKSEL1 before setting the timer RC associated registers. Also, do not change the setting values of the TRBOSEL0 bit during timer RB operation. Do not change the setting values of bits TRCCLKSEL0 and TRCCLKSEL1 during timer RC operation.
Change the TRBRCSR register from the initial value to any value during the initial setting of the user's program. Do not change this register again while the main program is executed.

18.3 Timer Mode

In timer mode, a count source which is internally generated or timer RA underflows are counted (refer to **Table 18.2 Timer Mode Specifications**). Registers TRBOCR and TRBSC are not used in timer mode.

Table 18.2 Timer Mode Specifications

Item	Specification
Count sources	f1, f2, f8, timer RA underflow
Count operations	• Decrement • When the timer underflows, it reloads the reload register contents before the count continues (when timer RB underflows, the contents of timer RB primary reload register is reloaded).
Divide ratio	1/(n+1)(m+1) n: setting value in TRBPRE register, m: setting value in TRBPR register
Count start condition	1 (count starts) is written to the TSTART bit in the TRBCR register.
Count stop conditions	• 0 (count stops) is written to the TSTART bit in the TRBCR register. • 1 (count forcibly stop) is written to the TSTOP bit in the TRBCR register.
Interrupt request generation timing	When timer RB underflows [timer RB interrupt].
TRBO pin function	Programmable I/O port
$\overline{\text{INT0}}$ pin function	Programmable I/O port or $\overline{\text{INT0}}$ interrupt input
Read from timer	The count value can be read out by reading registers TRBPR and TRBPRE.
Write to timer	• When registers TRBPRE and TRBPR are written while the count is stopped, values are written to both the reload register and counter. • When registers TRBPRE and TRBPR are written to while count operation is in progress: If the TWRC bit in the TRBMR register is set to 0, the value is written to both the reload register and the counter. If the TWRC bit is set to 1, the value is written to the reload register only. (Refer to **18.3.2 Timer Write Control during Count Operation**.)

18.3.1 Timer RB I/O Control Register (TRBIOC) in Timer Mode

Address 010Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	INOSEG	INOSTG	TOCNT	TOPL
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TOPL	Timer RB output level select bit	Set to 0 in timer mode.	R/W
b1	TOCNT	Timer RB output switch bit		R/W
b2	INOSTG	One-shot trigger control bit		R/W
b3	INOSEG	One-shot trigger polarity select bit		R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b5	—			
b6	—			
b7	—			

18.3.2 Timer Write Control during Count Operation

Timer RB has a prescaler and a timer (which counts the prescaler underflows). The prescaler and timer each consist of a reload register and a counter. In timer mode, the TWRC bit in the TRBMR register can be used to select whether writing to the prescaler or timer during count operation is performed to both the reload register and counter or only to the reload register.

However, values are transferred from the reload register to the counter of the prescaler in synchronization with the count source. In addition, values are transferred from the reload register to the counter of the timer in synchronization with prescaler underflows. Therefore, even if the TWRC bit is set for writing to both the reload register and counter, the counter value is not updated immediately after the WRITE instruction is executed. In addition, if the TWRC bit is set for writing to the reload register only, the synchronization of the writing will be shifted if the prescaler value changes. Figure 18.2 shows an Operating Example of Timer RB when Counter Value is Rewritten during Count Operation.

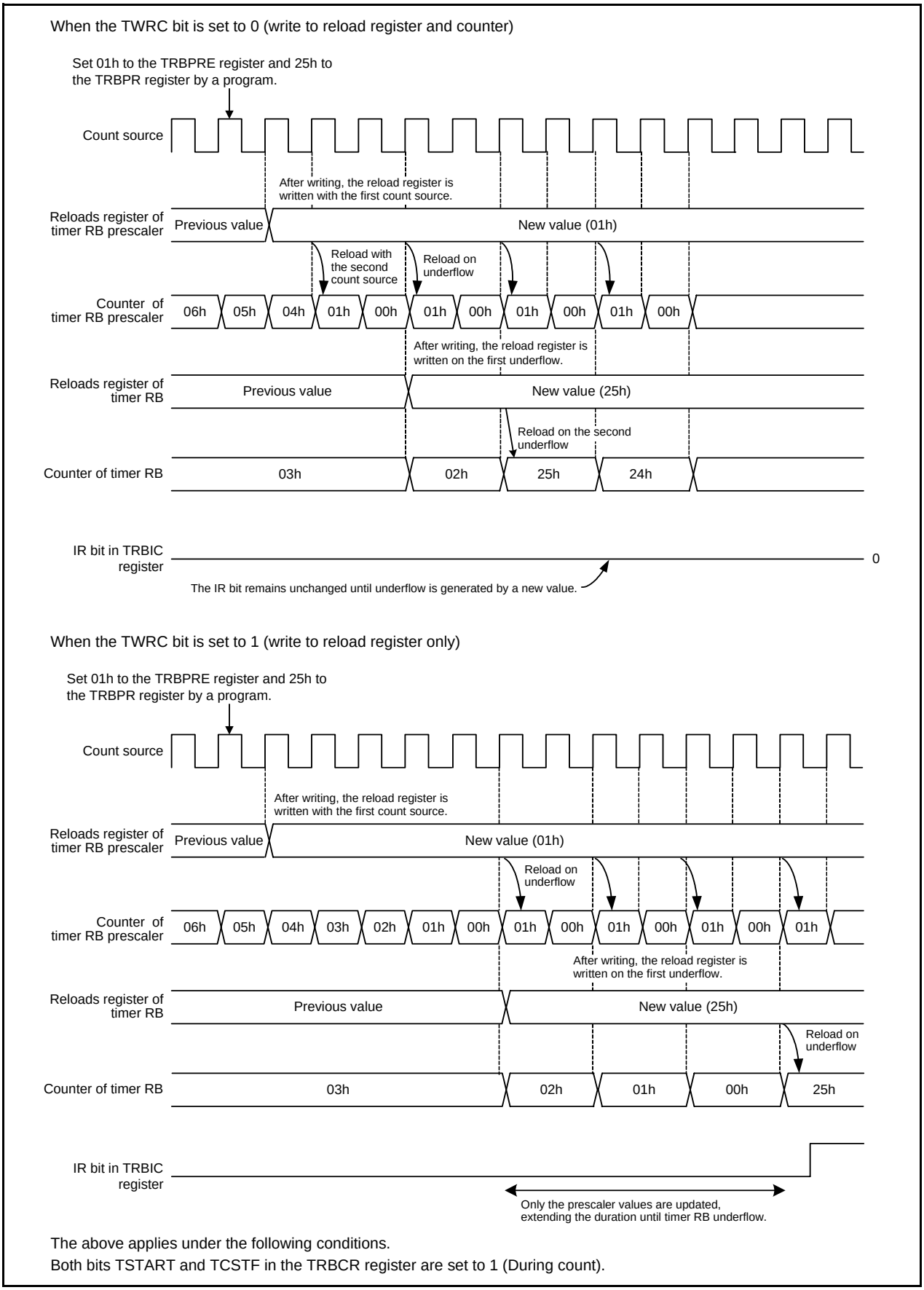


Figure 18.2 Operating Example of Timer RB when Counter Value is Rewritten during Count Operation

18.4 Programmable Waveform Generation Mode

In programmable waveform generation mode, the signal output from the TRBO pin is inverted each time the counter underflows, while the values in registers TRBPR and TRBSC are counted alternately (refer to **Table 18.3 Programmable Waveform Generation Mode Specifications**). Counting starts by counting the setting value in the TRBPR register. The TRBOCR register is unused in this mode.
Figure 18.3 shows an Operating Example of Timer RB in Programmable Waveform Generation Mode.

Table 18.3 Programmable Waveform Generation Mode Specifications

Item	Specification
Count sources	f1, f2, f8, timer RA underflow
Count operations	• Decrement • When the timer underflows, it reloads the contents of the primary reload and secondary reload registers alternately before the count continues.
Width and period of output waveform	Primary period: (n+1)(m+1)/fi Secondary period: (n+1)(p+1)/fi Period: (n+1){(m+1)+(p+1)}/fi fi: Count source frequency n: Value set in TRBPRE register, m: Value set in TRBPR register p: Value set in TRBSC register
Count start condition	1 (count start) is written to the TSTART bit in the TRBCR register.
Count stop conditions	• 0 (count stop) is written to the TSTART bit in the TRBCR register. • 1 (count forcibly stop) is written to the TSTOP bit in the TRBCR register.
Interrupt request generation timing	In half a cycle of the count source, after timer RB underflows during the secondary period (at the same time as the TRBO output change) [timer RB interrupt]
TRBO pin function	Programmable output port or pulse output
$\overline{\text{INT0}}$ pin function	Programmable I/O port or $\overline{\text{INT0}}$ interrupt input
Read from timer	The count value can be read out by reading registers TRBPR and TRBPRE. (1)
Write to timer	• When registers TRBPRE, TRBSC, and TRBPR are written while the count is stopped, values are written to both the reload register and counter. • When registers TRBPRE, TRBSC, and TRBPR are written to during count operation, values are written to the reload registers only. (2)
Selectable functions	• Output level select function The output level during primary and secondary periods is selected by the TOPL bit in the TRBIOC register. • TRBO pin output switch function Timer RB pulse output or P3_1 (P1_3) latch output is selected by the TOCNT bit in the TRBIOC register. (3)

Notes:
1. Even when counting the secondary period, the TRBPR register may be read.
2. The set values are reflected in the waveform output beginning with the following primary period after writing to the TRBPR register.
3. The value written to the TOCNT bit is enabled by the following.
   • When counting starts.
   • When a timer RB interrupt request is generated.
   The contents after the TOCNT bit is changed are reflected from the output of the following primary period.

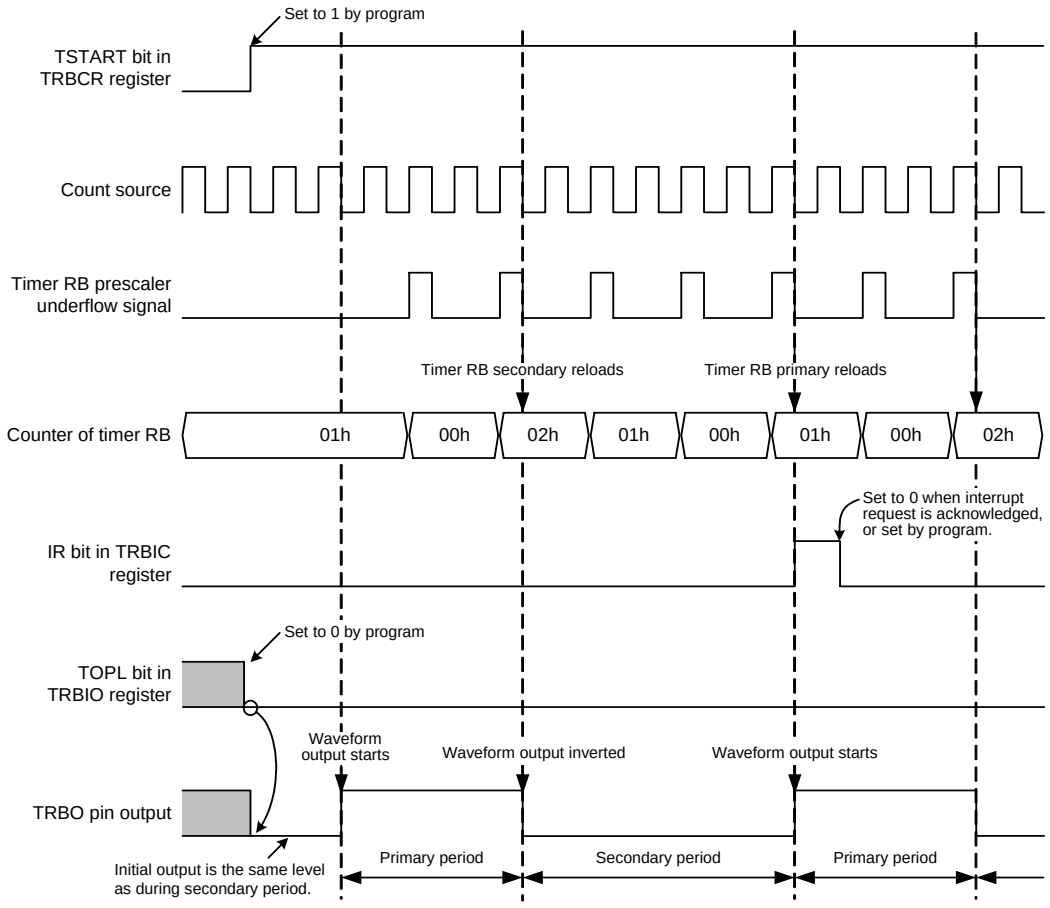
18.4.1 Timer RB I/O Control Register (TRBIOC) in Programmable Waveform Generation Mode

Address 010Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	INOSEG	INOSTG	TOCNT	TOPL
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TOPL	Timer RB output level select bit	0: Outputs “H” for primary period Outputs “L” for secondary period Outputs “L” when the timer is stopped 1: Outputs “L” for primary period Outputs “H” for secondary period Outputs “H” when the timer is stopped	R/W
b1	TOCNT	Timer RB output switch bit	0: Outputs timer RB waveform 1: Outputs value in P3_1 (P1_3) port register	R/W
b2	INOSTG	One-shot trigger control bit	Set to 0 in programmable waveform generation mode.	R/W
b3	INOSEG	One-shot trigger polarity select bit		R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b5	—			
b6	—			
b7	—			

18.4.2 Operating Example



The above applies under the following conditions.
TRBPRE = 01h, TRBPR = 01h, TRBSC = 02h
TRBIOC register TOCNT = 0 (timer RB waveform is output from the TRBO pin)

Figure 18.3 Operating Example of Timer RB in Programmable Waveform Generation Mode

18.5 Programmable One-shot Generation Mode

In programmable one-shot generation mode, a one-shot pulse is output from the TRBO pin by a program or an external trigger input (input to the $\overline{\text{INT0}}$ pin) (refer to **Table 18.4 Programmable One-Shot Generation Mode Specifications**). When a trigger is generated, the timer starts operating from the point only once for a given period equal to the set value in the TRBPR register. The TRBSC register is not used in this mode.
Figure 18.4 shows an Operating Example of Programmable One-Shot Generation Mode.

Table 18.4 Programmable One-Shot Generation Mode Specifications

Item	Specification
Count sources	f1, f2, f8, timer RA underflow
Count operations	• Decrement the setting value in the TRBPR register • When the timer underflows, it reloads the contents of the reload register before the count completes and the TOSSTF bit is set to 0 (one-shot stops). • When the count stops, the timer reloads the contents of the reload register before it stops.
One-shot pulse output time	(n+1)(m+1)/fi fi: Count source frequency n: Setting value in TRBPRE register, m: Setting value in TRBPR register
Count start conditions	• The TSTART bit in the TRBCR register is set to 1 (count starts) and the next trigger is generated • Set the TOSST bit in the TRBOCR register to 1 (one-shot starts) • Input trigger to the $\overline{\text{INT0}}$ pin
Count stop conditions	• When reloading completes after timer RB underflows during primary period • When the TOSSP bit in the TRBOCR register is set to 1 (one-shot stops) • When the TSTART bit in the TRBCR register is set to 0 (stops counting) • When the TSTOP bit in the TRBCR register is set to 1 (forcibly stops counting)
Interrupt request generation timing	In half a cycle of the count source, after the timer underflows (at the same time as the TRBO output ends) [timer RB interrupt].
TRBO pin function	Pulse output
$\overline{\text{INT0}}$ pin functions	• When the INOSTG bit in the TRBIOC register is set to 0 ($\overline{\text{INT0}}$ pin one-shot trigger disabled): programmable I/O port or $\overline{\text{INT0}}$ interrupt input • When the INOSTG bit in the TRBIOC register is set to 1 ($\overline{\text{INT0}}$ pin one-shot trigger enabled): external trigger ($\overline{\text{INT0}}$ interrupt input)
Read from timer	The count value can be read out by reading registers TRBPR and TRBPRE.
Write to timer	• When registers TRBPRE and TRBPR are written while the count is stopped, values are written to both the reload register and counter. • When registers TRBPRE and TRBPR are written during the count, values are written to the reload register only (the data is transferred to the counter at the following reload). (1)
Selectable functions	• Output level select function The output level of the one-shot pulse waveform is selected by the TOPL bit in the TRBIOC register. • One-shot trigger select function Refer to **18.5.3 One-Shot Trigger Selection**.

Note:
1. The set value is reflected at the following one-shot pulse after writing to the TRBPR register.

18.5.1 Timer RB I/O Control Register (TRBIOC) in Programmable One-Shot Generation Mode

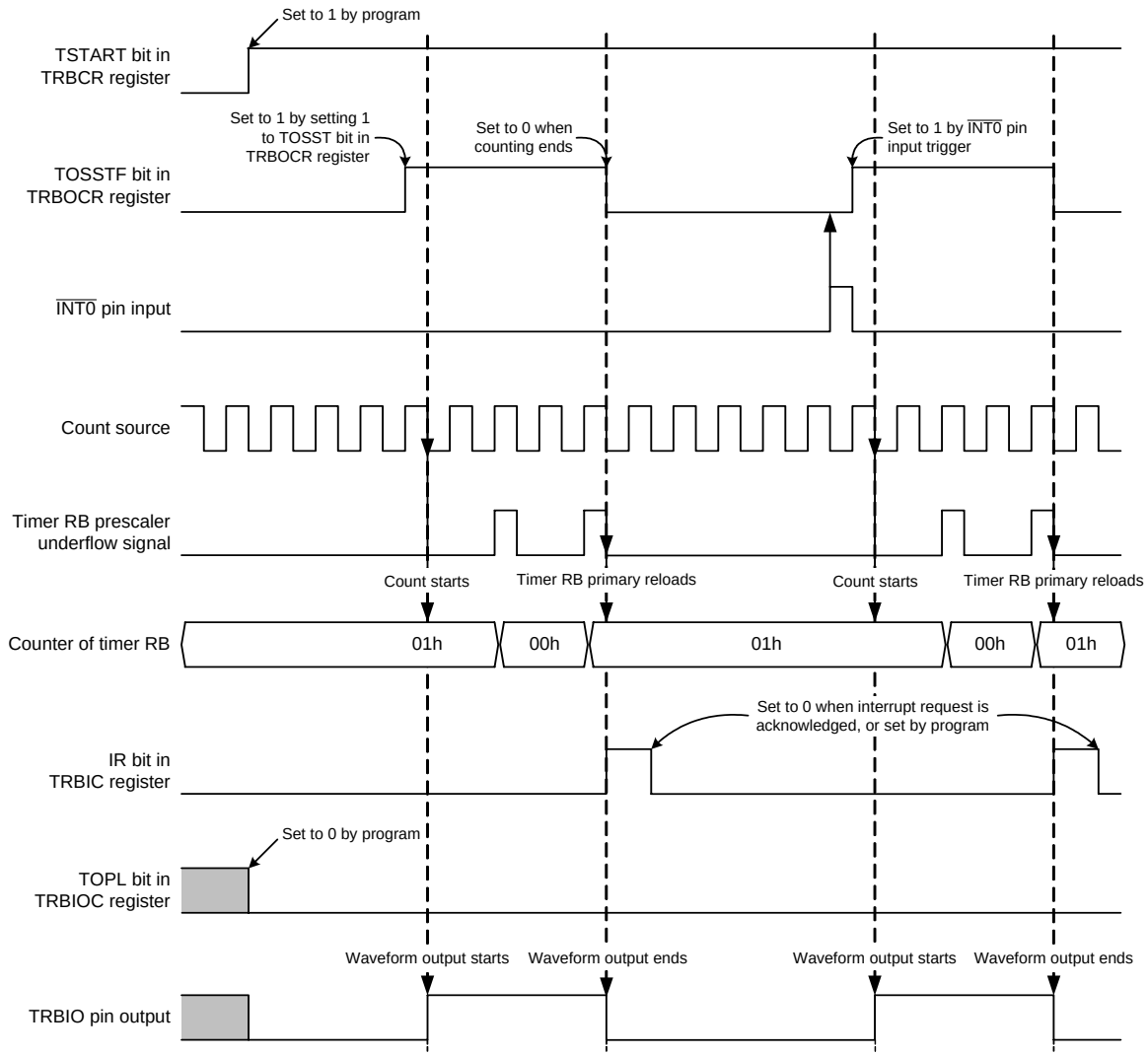
Address 010Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	INOSEG	INOSTG	TOCNT	TOPL
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TOPL	Timer RB output level select bit	0: Outputs one-shot pulse “H” Outputs “L” when the timer is stopped 1: Outputs one-shot pulse “L” Outputs “H” when the timer is stopped	R/W
b1	TOCNT	Timer RB output switch bit	Set to 0 in programmable one-shot generation mode.	R/W
b2	INOSTG	One-shot trigger control bit (1)	0: $\overline{\text{INT0}}$ pin one-shot trigger disabled 1: $\overline{\text{INT0}}$ pin one-shot trigger enabled	R/W
b3	INOSEG	One-shot trigger polarity select bit (1)	0: Falling edge trigger 1: Rising edge trigger	R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b5	—			
b6	—			
b7	—			

Note:
1. Refer to **18.5.3 One-Shot Trigger Selection**.

18.5.2 Operating Example



The above applies under the following conditions.
TRBPRE = 01h, TRBPR = 01h
TRBIOC register TOPL = 0, TOCNT = 0
INOSTG = 1 (INT0 pin one-shot trigger enabled), INOSEG = 1 (edge trigger at rising edge)

Figure 18.4 Operating Example of Programmable One-Shot Generation Mode

18.5.3 One-Shot Trigger Selection

In programmable one-shot generation mode and programmable wait one-shot generation mode, operation starts when a one-shot trigger is generated while the TCSTF bit in the TRBCR register is set to 1 (count starts).
A one-shot trigger can be generated by either of the following causes:

- 1 is written to the TOSST bit in the TRBOCR register by a program.
- Trigger input from the $\overline{\text{INT0}}$ pin.

When a one-shot trigger occurs, the TOSSTF bit in the TRBOCR register is set to 1 (one-shot operation in progress) after one or two cycles of the count source have elapsed. Then, in programmable one-shot generation mode, count operation begins and one-shot waveform output starts. (In programmable wait one-shot generation mode, count operation starts for the wait period.) If a one-shot trigger occurs while the TOSSTF bit is set to 1, no retriggering occurs.

To use trigger input from the $\overline{\text{INT0}}$ pin, input the trigger after making the following settings:

- Set the PD4_5 bit in the PD4 register to 0 (input port).
- Select the $\overline{\text{INT0}}$ digital filter with bits INT0F1 and INT0F0 in the INTF register.
- Select both edges or one edge with the INT0PL bit in INTEN register. If one edge is selected, further select falling or rising edge with the INOSEG bit in TRBIOC register.
- Set the INT0EN bit in the INTEN register to 1 (enabled).
- After completing the above, set the INOSTG bit in the TRBIOC register to 1 ($\overline{\text{INT0}}$ pin one-shot trigger enabled).

Note the following points with regard to generating interrupt requests by trigger input from the $\overline{\text{INT0}}$ pin.

- Processing to handle the interrupts is required. Refer to **11. Interrupts**, for details.
- If one edge is selected, use the POL bit in the INT0IC register to select falling or rising edge. (The INOSEG bit in the TRBIOC register does not affect $\overline{\text{INT0}}$ interrupts).
- If a one-shot trigger occurs while the TOSSTF bit is set to 1, timer RB operation is not affected, but the value of the IR bit in the INT0IC register changes.

18.6 Programmable Wait One-Shot Generation Mode

In programmable wait one-shot generation mode, a one-shot pulse is output from the TRBO pin by a program or an external trigger input (input to the $\overline{\text{INT0}}$ pin) (refer to **Table 18.5 Programmable Wait One-Shot Generation Mode Specifications**). When a trigger is generated from that point, the timer outputs a pulse only once for a given length of time equal to the setting value in the TRBSC register after waiting for a given length of time equal to the setting value in the TRBPR register.
Figure 18.5 shows an Operating Example of Programmable Wait One-Shot Generation Mode.

Table 18.5 Programmable Wait One-Shot Generation Mode Specifications

Item	Specification
Count sources	f1, f2, f8, timer RA underflow
Count operations	• Decrement the timer RB primary setting value. • When a count of the timer RB primary underflows, the timer reloads the contents of timer RB secondary before the count continues. • When a count of the timer RB secondary underflows, the timer reloads the contents of timer RB primary before the count completes and the TOSSTF bit is set to 0 (one-shot stops). • When the count stops, the timer reloads the contents of the reload register before it stops.
Wait time	(n+1)(m+1)/fi fi: Count source frequency n: Value set in the TRBPRE register, m: Value set in the TRBPR register
One-shot pulse output time	(n+1)(p+1)/fi fi: Count source frequency n: Value set in the TRBPRE register, p: Value set in the TRBSC register
Count start conditions	• The TSTART bit in the TRBCR register is set to 1 (count starts) and the next trigger is generated. • Set the TOSST bit in the TRBOCR register to 1 (one-shot starts). • Input trigger to the $\overline{\text{INT0}}$ pin
Count stop conditions	• When reloading completes after timer RB underflows during secondary period. • When the TOSSP bit in the TRBOCR register is set to 1 (one-shot stops). • When the TSTART bit in the TRBCR register is set to 0 (starts counting). • When the TSTOP bit in the TRBCR register is set to 1 (forcibly stops counting).
Interrupt request generation timing	In half a cycle of the count source after timer RB underflows during secondary period (complete at the same time as waveform output from the TRBO pin) [timer RB interrupt].
TRBO pin function	Pulse output
$\overline{\text{INT0}}$ pin functions	• When the INOSTG bit in the TRBIOC register is set to 0 ($\overline{\text{INT0}}$ pin one-shot trigger disabled): programmable I/O port or $\overline{\text{INT0}}$ interrupt input • When the INOSTG bit in the TRBIOC register is set to 1 ($\overline{\text{INT0}}$ pin one-shot trigger enabled): external trigger ($\overline{\text{INT0}}$ interrupt input)
Read from timer	The count value can be read out by reading registers TRBPR and TRBPRE.
Write to timer	• When registers TRBPRE, TRBSC, and TRBPR are written while the count stops, values are written to both the reload register and counter. • When registers TRBPRE, TRBSC, and TRBPR are written to during count operation, values are written to the reload registers only. (1)
Selectable functions	• Output level select function The output level of the one-shot pulse waveform is selected by the TOPL bit in the TRBIOC register. • One-shot trigger select function Refer to **18.5.3 One-Shot Trigger Selection**.

Note:
1. The set value is reflected at the following one-shot pulse after writing to registers TRBSC and TRBPR.

18.6.1 Timer RB I/O Control Register (TRBIOC) in Programmable Wait One-Shot Generation Mode

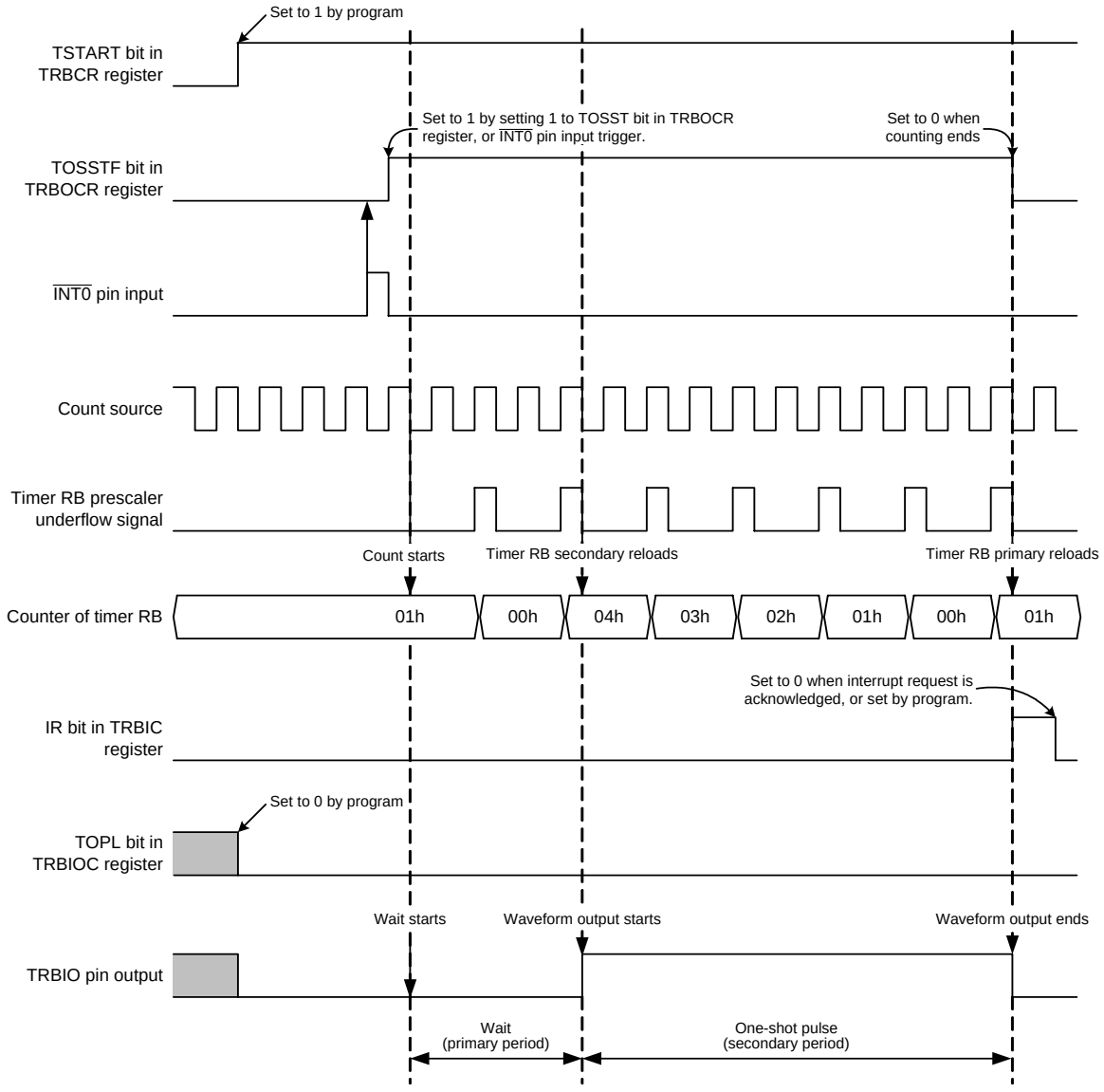
Address 010Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	INOSEG	INOSTG	TOCNT	TOPL
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TOPL	Timer RB output level select bit	0: Outputs one-shot pulse “H” Outputs “L” when the timer stops or during wait 1: Outputs one-shot pulse “L” Outputs “H” when the timer stops or during wait	R/W
b1	TOCNT	Timer RB output switch bit	Set to 0 in programmable wait one-shot generation mode.	R/W
b2	INOSTG	One-shot trigger control bit (1)	0: $\overline{\text{INT0}}$ pin one-shot trigger disabled 1: $\overline{\text{INT0}}$ pin one-shot trigger enabled	R/W
b3	INOSEG	One-shot trigger polarity select bit (1)	0: Falling edge trigger 1: Rising edge trigger	R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b5	—			
b6	—			
b7	—			

Note:
1. Refer to **18.5.3 One-Shot Trigger Selection**.

18.6.2 Operating Example



The above applies under the following conditions.
TRBPRE = 01h, TRBPR = 01h, TRBSC = 04h
INOSTG = 1 (INT0 pin one-shot trigger enabled), INOSEG = 1 (edge trigger at rising edge)

Figure 18.5 Operating Example of Programmable Wait One-Shot Generation Mode

18.7 Notes on Timer RB

- Timer RB stops counting after a reset. Set the values in the timer RB and timer RB prescalers before the count starts.
- Even if the prescaler and timer RB is read out in 16-bit units, these registers are read 1 byte at a time by the MCU. Consequently, the timer value may be updated during the period when these two registers are being read.
- In programmable one-shot generation mode and programmable wait one-shot generation mode, when setting the TSTART bit in the TRBCR register to 0 (stops counting) or setting the TOSSP bit in the TRBOCR register to 1 (stops one-shot), the timer reloads the value of reload register and stops. Therefore, in programmable one-shot generation mode and programmable wait one-shot generation mode, read the timer count value before the timer stops.
- The TCSTF bit remains 0 (count stops) for 1 to 2 cycles of the count source after setting the TSTART bit to 1 (count starts) while the count is stopped.
  During this time, do not access registers associated with timer RB (1) other than the TCSTF bit. Timer RB starts counting at the first valid edge of the count source after the TCSTF bit is set to 1 (during count).
  The TCSTF bit remains 1 for 1 to 2 cycles of the count source after setting the TSTART bit to 0 (count stops) while the count is in progress. Timer RB counting is stopped when the TCSTF bit is set to 0.
  During this time, do not access registers associated with timer RB (1) other than the TCSTF bit.

  Note:
  1. Registers associated with timer RB: TRBCR, TRBOCR, TRBIOC, TRBMR, TRBPRE, TRBSC, and TRBPR.

- If the TSTOP bit in the TRBCR register is set to 1 during timer operation, timer RB stops immediately.
- If 1 is written to the TOSST or TOSSP bit in the TRBOCR register, the value of the TOSSTF bit changes after one or two cycles of the count source have elapsed. If the TOSSP bit is written to 1 during the period between when the TOSST bit is written to 1 and when the TOSSTF bit is set to 1, the TOSSTF bit may be set to either 0 or 1 depending on the content state. Likewise, if the TOSST bit is written to 1 during the period between when the TOSSP bit is written to 1 and when the TOSSTF bit is set to 0, the TOSSTF bit may be set to either 0 or 1.
- To use the underflow signal of timer RA as the count source for timer RB, set timer RA in timer mode, pulse output mode, or event count mode.

18.7.1 Timer Mode

To write to registers TRBPRE and TRBPR during count operation (TCSTF bit in the TRBCR register is set to 1), note the following points:

- When the TRBPRE register is written continuously, allow three or more cycles of the count source for each write interval.
- When the TRBPR register is written continuously, allow three or more cycles of the prescaler underflow for each write interval.

18.7.2 Programmable Waveform Generation Mode

To write to registers TRBPRE and TRBPR during count operation (TCSTF bit in the TRBCR register is set to 1), note the following points:

- When the TRBPRE register is written continuously, allow three or more cycles of the count source for each write interval.
- When the TRBPR register is written continuously, allow three or more cycles of the prescaler underflow for each write interval.

18.7.3 Programmable One-shot Generation Mode

To write to registers TRBPRE and TRBPR during count operation (TCSTF bit in the TRBCR register is set to 1), note the following points:

- When the TRBPRE register is written continuously, allow three or more cycles of the count source for each write interval.
- When the TRBPR register is written continuously, allow three or more cycles of the prescaler underflow for each write interval.

18.7.4 Programmable Wait One-shot Generation Mode

To write to registers TRBPRE and TRBPR during count operation (TCSTF bit in the TRBCR register is set to 1), note the following points:

- When the TRBPRE register is written continuously, allow three or more cycles of the count source for each write interval.
- When the TRBPR register is written continuously, allow three or more cycles of the prescaler underflow for each write interval.

19. Timer RC

Timer RC is a 16-bit timer with four I/O pins.

19.1 Overview

Timer RC uses either f1, fOCO40M or fOCO-F as its operation clock. Table 19.1 lists the Timer RC Operation Clock.

Table 19.1 Timer RC Operation Clock

Condition	Timer RC Operation Clock
Count source is f1, f2, f4, f8, f32, or TRCCLK input (bits TCK2 to TCK0 in TRCCR1 register are set to a value from 000b to 101b)	f1
Count source is fOCO40M (bits TCK2 to TCK0 in TRCCR1 register are set to 110b)	fOCO40M
Count source is fOCO-F (bits TCK2 to TCK0 in TRCCR1 register are set to 111b)	fOCO-F

Table 19.2 lists the Pin Configuration of Timer RC, and Figure 19.1 shows a Timer RC Block Diagram.
Timer RC has three modes.

- Timer mode
  - Input capture function — The counter value is captured to a register, using an external signal as the trigger.
  - Output compare function — Matches between the counter and register values are detected. (Pin output state changes when a match is detected.)

The following two modes use the output compare function.

- PWM mode — Pulses of a given width are output continuously.
- PWM2 mode — A one-shot waveform or PWM waveform is output following the trigger after the wait time has elapsed.

Input capture function, output compare function, and PWM mode settings may be specified independently for each pin.
In PWM2 mode waveforms are output based on a combination of the counter or the register.

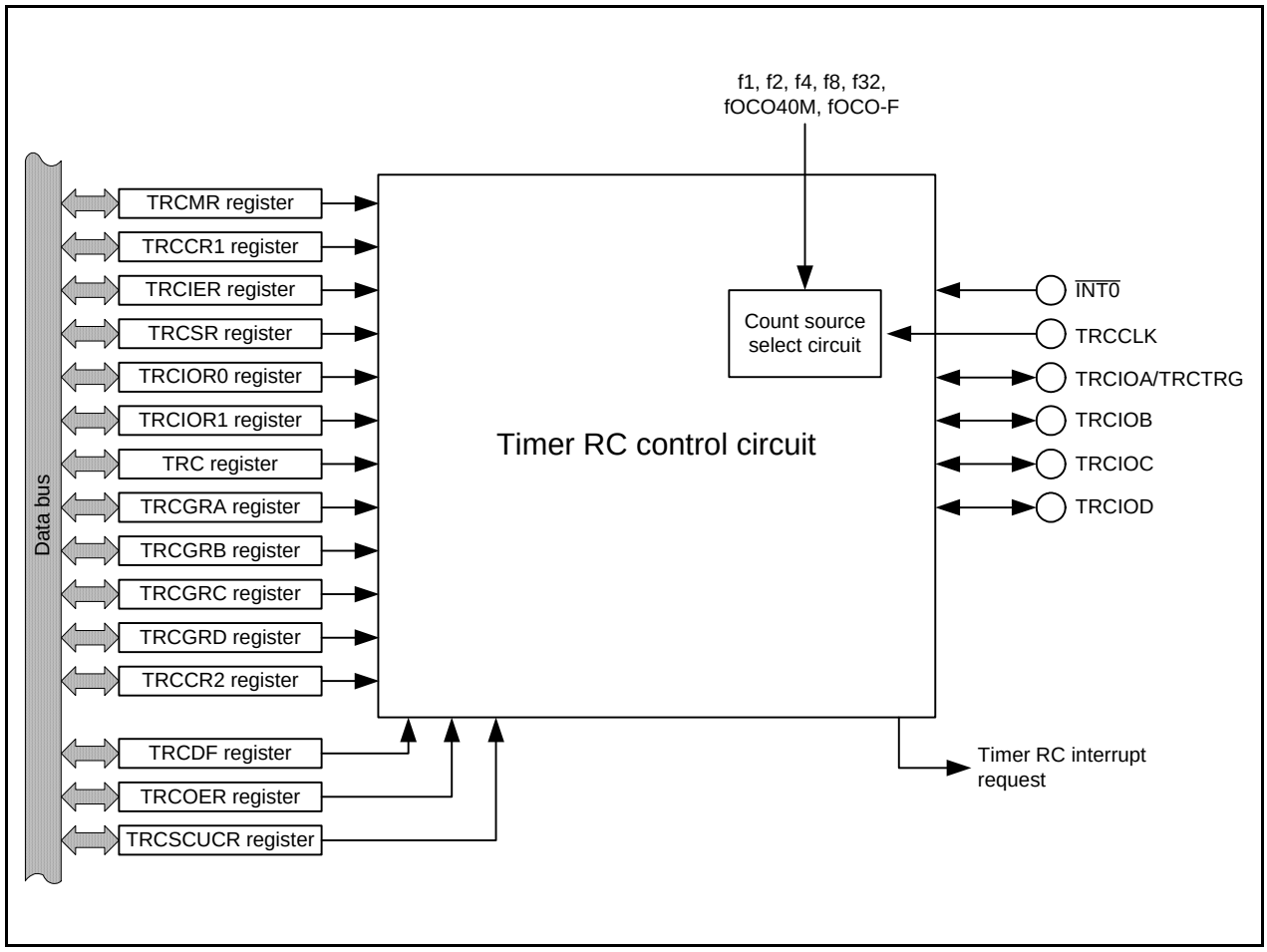


Figure 19.1 Timer RC Block Diagram

Table 19.2 Pin Configuration of Timer RC

Pin Name	Assigned Pin	I/O	Function
TRCIOA	P0_0, P0_1, P0_2, P1_1, or P3_1	I/O	Function differs according to the mode. Refer to descriptions of individual modes for details.
TRCIOB	P1_2, or P4_5		
TRCIOC	P1_3, or P3_4		
TRCIOD	P1_0, or P3_5		
TRCCLK	P1_4, P3_3, or P3_7	Input	External clock input
TRCTRG	P0_0, P0_1, P0_2, P1_1, or P3_1	Input	PWM2 mode external trigger input

19.2 Registers

Table 19.3 lists the Registers Associated with Timer RC.

Table 19.3 Registers Associated with Timer RC

Address	Symbol	Mode				Related Information
		Timer		PWM	PWM2	
		Input Capture Function	Output Compare Function			
0008h	MSTCR	Valid	Valid	Valid	Valid	19.2.1 Module Standby Control Register (MSTCR)
0120h	TRCMR	Valid	Valid	Valid	Valid	19.2.2 Timer RC Mode Register (TRCMR)
0121h	TRCCR1	Valid	Valid	Valid	Valid	Timer RC control register 1 19.2.3 Timer RC Control Register 1 (TRCCR1) 19.5.1 Timer RC Control Register 1 (TRCCR1) for Output Compare Function 19.6.1 Timer RC Control Register 1 (TRCCR1) in PWM Mode 19.7.1 Timer RC Control Register 1 (TRCCR1) in PWM2 Mode
0122h	TRCIER	Valid	Valid	Valid	Valid	19.2.4 Timer RC Interrupt Enable Register (TRCIER)
0123h	TRCSR	Valid	Valid	Valid	Valid	19.2.5 Timer RC Status Register (TRCSR)
0124h	TRCIOR0	Valid	Valid	—	—	Timer RC I/O control register 0, timer RC I/O control register 1 19.2.6 Timer RC I/O Control Register 0 (TRCIOR0) 19.2.7 Timer RC I/O Control Register 1 (TRCIOR1) 19.4.1 Timer RC I/O Control Register 0 (TRCIOR0) for Input Capture Function 19.4.2 Timer RC I/O Control Register 1 (TRCIOR1) for Input Capture Function 19.5.2 Timer RC I/O Control Register 0 (TRCIOR0) for Output Compare Function 19.5.3 Timer RC I/O Control Register 1 (TRCIOR1) for Output Compare Function
0125h	TRCIOR1					
0126h 0127h	TRC	Valid	Valid	Valid	Valid	19.2.8 Timer RC Counter (TRC)
0128h 0129h	TRCGRA	Valid	Valid	Valid	Valid	19.2.9 Timer RC General Registers A, B, C, and D (TRCGRA, TRCGRB, TRCGRC, TRCGRD)
012Ah 012Bh	TRCGRB					
012Ch 012Dh	TRCGRC					
012Eh 012Fh	TRCGRD					
0130h	TRCCR2	—	Valid	Valid	Valid	19.2.10 Timer RC Control Register 2 (TRCCR2)
0131h	TRCDF	Valid	—	—	Valid	19.2.11 Timer RC Digital Filter Function Select Register (TRCDF)
0132h	TRCOER	—	Valid	Valid	Valid	19.2.12 Timer RC Output Master Enable Register (TRCOER)
0133h	TRCSCUCR	—	Valid	Valid	Valid	19.2.13 Timer RC Trigger Control Register (TRCSCUCR)
0181h	TRBRCSR	Valid	Valid	Valid	Valid	19.2.14 Timer RB/RC Pin Select Register (TRBRCSR)
0182h	TRCPSR0	Valid	Valid	Valid	Valid	19.2.15 Timer RC Pin Select Register 0 (TRCPSR0)
0183h	TRCPSR1	Valid	Valid	Valid	Valid	19.2.16 Timer RC Pin Select Register 1 (TRCPSR1)

—: Invalid

19.2.1 Module Standby Control Register (MSTCR)

Address 0008h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	MSTTRC	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b1	—			
b2	—			
b3	—	Reserved bit	Set to 0.	R/W
b4	—			R/W
b5	MSTTRC	Timer RC standby bit	0: Active 1: Standby (1)	R/W
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b7	—			

Note:
1. Stop the timer RC function before setting to standby. When the MSTTRC bit is set to 1 (standby), any access to the timer RC associated registers (addresses 0120h to 0133h) is disabled.

19.2.2 Timer RC Mode Register (TRCMR)

Address 0120h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TSTART	—	BFD	BFC	PWM2	PWMD	PWMC	PWMB
After Reset	0	1	0	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	PWMB	PWM mode of TRCIOB select bit (1)	0: Timer mode 1: PWM mode	R/W
b1	PWMC	PWM mode of TRCIOC select bit (1)	0: Timer mode 1: PWM mode	R/W
b2	PWMD	PWM mode of TRCIOD select bit (1)	0: Timer mode 1: PWM mode	R/W
b3	PWM2	PWM2 mode select bit	0: PWM 2 mode 1: Timer mode or PWM mode	R/W
b4	BFC	TRCGRC register function select bit (2)	0: General register 1: Buffer register of TRCGRA register	R/W
b5	BFD	TRCGRD register function select bit	0: General register 1: Buffer register of TRCGRB register	R/W
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b7	TSTART	TRC count start bit	0: Count stops 1: Count starts	R/W

Notes:
1. These bits are enabled when the PWM2 bit is set to 1 (timer mode or PWM mode).
2. Set the BFC bit to 0 (general register) in PWM2 mode.

For notes on PWM2 mode, refer to **19.9.6 TRCMR Register in PWM2 Mode**.

19.2.3 Timer RC Control Register 1 (TRCCR1)

Address 0121h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CCLR	TCK2	TCK1	TCK0	TOD	TOC	TOB	TOA
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TOA	TRCIOA output level select bit (1)	Function varies according to the operating mode (function).	R/W
b1	TOB	TRCIOB output level select bit (1)		R/W
b2	TOC	TRCIOC output level select bit (1)		R/W
b3	TOD	TRCIOD output level select bit (1)		R/W
b4	TCK0	Count source select bit (1)	b6 b5 b4 0 0 0: f1 0 0 1: f2 0 1 0: f4 0 1 1: f8 1 0 0: f32 1 0 1: TRCCLK input rising edge 1 1 0: fOCO40M 1 1 1: fOCO-F (2)	R/W
b5	TCK1			R/W
b6	TCK2			R/W
b7	CCLR	TRC counter clear select bit	0: Disable clear (free-running operation) 1: Clear TRC counter by input capture or by compare match in TRCGRA	R/W

Notes:
1. Set to these bits when the TSTART bit in the TRCMR register is set to 0 (count stops).
2. To select fOCO-F, set it to the clock frequency higher than the CPU clock frequency.

19.2.4 Timer RC Interrupt Enable Register (TRCIER)

Address 0122h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	OVIE	—	—	—	IMIED	IMIEC	IMIEB	IMIEA
After Reset	0	1	1	1	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IMIEA	Input capture / compare match interrupt enable bit A	0: Disable interrupt (IMIA) by the IMFA bit 1: Enable interrupt (IMIA) by the IMFA bit	R/W
b1	IMIEB	Input capture / compare match interrupt enable bit B	0: Disable interrupt (IMIB) by the IMFB bit 1: Enable interrupt (IMIB) by the IMFB bit	R/W
b2	IMIEC	Input capture / compare match interrupt enable bit C	0: Disable interrupt (IMIC) by the IMFC bit 1: Enable interrupt (IMIC) by the IMFC bit	R/W
b3	IMIED	Input capture / compare match interrupt enable bit D	0: Disable interrupt (IMID) by the IMFD bit 1: Enable interrupt (IMID) by the IMFD bit	R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b5	—			
b6	—			
b7	OVIE	Overflow interrupt enable bit	0: Disable interrupt (OVI) by the OVF bit 1: Enable interrupt (OVI) by the OVF bit	R/W

19.2.5 Timer RC Status Register (TRCSR)

Address 0123h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	OVF	—	—	—	IMFD	IMFC	IMFB	IMFA
After Reset	0	1	1	1	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IMFA	Input capture / compare match flag A	[Source for setting this bit to 0] Write 0 after read. (1) [Source for setting this bit to 1] Refer to **Table 19.4 Source for Setting Bit of Each Flag to 1**.	R/W
b1	IMFB	Input capture / compare match flag B		R/W
b2	IMFC	Input capture / compare match flag C		R/W
b3	IMFD	Input capture / compare match flag D		R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b5	—			
b6	—			
b7	OVF	Overflow flag	[Source for setting this bit to 0] Write 0 after read. (1) [Source for setting this bit to 1] Refer to **Table 19.4 Source for Setting Bit of Each Flag to 1**.	R/W

Note:
1. The writing results are as follows:
   - This bit is set to 0 when the read result is 1 and 0 is written to the same bit.
   - This bit remains unchanged even if the read result is 0 and 0 is written to the same bit. (This bit remains 1 even if it is set to 1 from 0 after reading, and writing 0.)
   - This bit remains unchanged if 1 is written to it.

Table 19.4 Source for Setting Bit of Each Flag to 1

Bit Symbol	Timer Mode		PWM Mode	PWM2 Mode
	Input Capture Function	Output Compare Function		
IMFA	TRCIOA pin input edge (1)	When the values of the registers TRC and TRCGRA match.		
IMFB	TRCIOB pin input edge (1)	When the values of the registers TRC and TRCGRB match.		
IMFC	TRCIOC pin input edge (1)	When the values of the registers TRC and TRCGRC match. (2)		
IMFD	TRCIOD pin input edge (1)	When the values of the registers TRC and TRCGRD match. (2)		
OVF	When the TRC register overflows.			

Notes:
1. Edge selected by bits IOj1 to IOj0 (j = A, B, C, or D).
2. Includes the condition that bits BFC and BFD in the TRCMR register are set to 1 (buffer registers of registers TRCGRA and TRCGRB).

19.2.6 Timer RC I/O Control Register 0 (TRCIOR0)

Address 0124h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	IOB2	IOB1	IOB0	IOA3	IOA2	IOA1	IOA0
After Reset	1	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IOA0	TRCGRA control bit	Function varies according to the operating mode (function).	R/W
b1	IOA1			R/W
b2	IOA2	TRCGRA mode select bit (1)	0: Output compare function 1: Input capture function	R/W
b3	IOA3	TRCGRA input capture input switch bit (3)	0: fOCO128 signal 1: TRCIOA pin input	R/W
b4	IOB0	TRCGRB control bit	Function varies according to the operating mode (function).	R/W
b5	IOB1			R/W
b6	IOB2	TRCGRB mode select bit (2)	0: Output compare function 1: Input capture function	R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—

Notes:
1. When the BFC bit in the TRCMR register is set to 1 (buffer register of TRCGRA register), set the IOC2 bit in the TRCIOR1 register to the same value as the IOA2 bit in the TRCIOR0 register.
2. When the BFD bit in the TRCMR register is set to 1 (buffer register of TRCGRB register), set the IOD2 bit in the TRCIOR1 register to the same value as the IOB2 bit in the TRCIOR0 register.
3. The IOA3 bit is enabled when the IOA2 bit is set to 1 (input capture function).

The TRCIOR0 register is enabled in timer mode. It is disabled in modes PWM and PWM2.

19.2.7 Timer RC I/O Control Register 1 (TRCIOR1)

Address 0125h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	IOD3	IOD2	IOD1	IOD0	IOC3	IOC2	IOC1	IOC0
After Reset	1	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IOC0	TRCGRC control bit	Function varies according to the operating mode (function).	R/W
b1	IOC1			R/W
b2	IOC2	TRCGRC mode select bit (1)	0: Output compare function 1: Input capture function	R/W
b3	IOC3	TRCGRC register function select bit	0: TRCIOA output register 1: General register or buffer register	R/W
b4	IOD0	TRCGRD control bit	Function varies according to the operating mode (function).	R/W
b5	IOD1			R/W
b6	IOD2	TRCGRD mode select bit (2)	0: Output compare function 1: Input capture function	R/W
b7	IOD3	TRCGRD register function select bit	0: TRCIOB output register 1: General register or buffer register	R/W

Notes:
1. When the BFC bit in the TRCMR register is set to 1 (buffer register of TRCGRA register), set the IOC2 bit in the TRCIOR1 register to the same value as the IOA2 bit in the TRCIOR0 register.
2. When the BFD bit in the TRCMR register is set to 1 (buffer register of TRCGRB register), set the IOD2 bit in the TRCIOR1 register to the same value as the IOB2 bit in the TRCIOR0 register.

The TRCIOR1 register is enabled in timer mode. It is disabled in modes PWM and PWM2.

19.2.8 Timer RC Counter (TRC)

Address 0127h to 0126h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Function	Setting Range	R/W
b15 to b0	Count a count source. Count operation is incremented. When an overflow occurs, the OVF bit in the TRCSR register is set to 1.	0000h to FFFFh	R/W

Access the TRC register in 16-bit units. Do not access it in 8-bit units.

19.2.9 Timer RC General Registers A, B, C, and D (TRCGRA, TRCGRB, TRCGRC, TRCGRD)

Address 0129h to 0128h (TRCGRA), 012Bh to 012Ah (TRCGRB), 012Dh to 012Ch (TRCGRC), 012Fh to 012Eh (TRCGRD)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	Function	R/W
b15 to b0	Function varies according to the operating mode.	R/W

Access registers TRCGRA to TRCGRD in 16-bit units. Do not access them in 8-bit units.

19.2.10 Timer RC Control Register 2 (TRCCR2)

Address 0130h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TCEG1	TCEG0	CSEL	—	—	POLD	POLC	POLB
After Reset	0	0	0	1	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	POLB	PWM mode output level control bit B (1)	0: TRCIOB output level selected as “L” active 1: TRCIOB output level selected as “H” active	R/W
b1	POLC	PWM mode output level control bit C (1)	0: TRCIOC output level selected as “L” active 1: TRCIOC output level selected as “H” active	R/W
b2	POLD	PWM mode output level control bit D (1)	0: TRCIOD output level selected as “L” active 1: TRCIOD output level selected as “H” active	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b4	—			
b5	CSEL	TRC count operation select bit (2)	0: Count continues at compare match with the TRCGRA register 1: Count stops at compare match with the TRCGRA register	R/W
b6	TCEG0	TRCTRG input edge select bit (3)	b7 b6 0 0: Disable the trigger input from the TRCTRG pin 0 1: Rising edge selected 1 0: Falling edge selected 1 1: Both edges selected	R/W
b7	TCEG1			R/W

Notes:
1. Enabled when in PWM mode.
2. Enabled when in output compare function, PWM mode, or PWM2 mode. For notes on PWM2 mode, refer to **19.9.6 TRCMR Register in PWM2 Mode**.
3. Enabled when in PWM2 mode.

19.2.11 Timer RC Digital Filter Function Select Register (TRCDF)

Address 0131h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	DFCK1	DFCK0	—	DFTRG	DFD	DFC	DFB	DFA
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	DFA	TRCIOA pin digital filter function select bit (1)	0: Function is not used 1: Function is used	R/W
b1	DFB	TRCIOB pin digital filter function select bit (1)		R/W
b2	DFC	TRCIOC pin digital filter function select bit (1)		R/W
b3	DFD	TRCIOD pin digital filter function select bit (1)		R/W
b4	DFTRG	TRCTRG pin digital filter function select bit (2)		R/W
b5	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b6	DFCK0	Clock select bits for digital filter function (1, 2)	b7 b6 0 0: f32 0 1: f8 1 0: f1 1 1: Count source (clock selected by bits TCK2 to TCK0 in the TRCCR1 register)	R/W
b7	DFCK1			R/W

Notes:
1. These bits are enabled for the input capture function.
2. These bits are enabled when in PWM2 mode and bits TCEG1 to TCEG0 in the TRCCR2 register are set to 01b, 10b, or 11b (TRCTRG trigger input enabled).

19.2.12 Timer RC Output Master Enable Register (TRCOER)

Address 0132h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	PTO	—	—	—	ED	EC	EB	EA
After Reset	0	1	1	1	1	1	1	1

Bit	Symbol	Bit Name	Function	R/W
b0	EA	TRCIOA output disable bit (1)	0: Enable output 1: Disable output (The TRCIOA pin is used as a programmable I/O port.)	R/W
b1	EB	TRCIOB output disable bit (1)	0: Enable output 1: Disable output (The TRCIOB pin is used as a programmable I/O port.)	R/W
b2	EC	TRCIOC output disable bit (1)	0: Enable output 1: Disable output (The TRCIOC pin is used as a programmable I/O port.)	R/W
b3	ED	TRCIOD output disable bit (1)	0: Enable output 1: Disable output (The TRCIOD pin is used as a programmable I/O port.)	R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b5	—			
b6	—			
b7	PTO	$\overline{\text{INT0}}$ of pulse output forced cutoff signal input enabled bit	0: Pulse output forced cutoff input disabled 1: Pulse output forced cutoff input enabled (Bits EA, EB, EC, and ED are set to 1 (disable output) when “L” is applied to the $\overline{\text{INT0}}$ pin)	R/W

Note:
1. These bits are disabled for input pins set to the input capture function.

19.2.13 Timer RC Trigger Control Register (TRCSCUCR)

Address 0133h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	SCUTRGDE	SCUTRGCE	SCUTRGBE	SCUTRGAE
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	SCUTRGAE	SCU trigger A enable bit	0: SCU trigger disabled 1: SCU trigger generated at compare match with registers TRC and TRCGRA	R/W
b1	SCUTRGBE	SCU trigger B enable bit	0: SCU trigger disabled 1: SCU trigger generated at compare match with registers TRC and TRCGRB	R/W
b2	SCUTRGCE	SCU trigger C enable bit	0: SCU trigger disabled 1: SCU trigger generated at compare match with registers TRC and TRCGRC	R/W
b3	SCUTRGDE	SCU trigger D enable bit	0: SCU trigger disabled 1: SCU trigger generated at compare match with registers TRC and TRCGRD	R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b5	—			
b6	—			
b7	—			

19.2.14 Timer RB/RC Pin Select Register (TRBRCSR)

Address 0181h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	TRCCLKSEL1	TRCCLKSEL0	—	TRBOSEL2	TRBOSEL1	TRBOSEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TRBOSEL0	TRBO pin select bit	b2 b1 b0 0 0 0: P1_3 assigned 0 0 1: P3_1 assigned 0 1 0: Do not set. (TRBO pin not used) 0 1 1: P3_3 assigned Other than above: Do not set. (TRBO pin not used.)	R/W
b1	TRBOSEL1			R/W
b2	TRBOSEL2			R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	TRCCLKSEL0	TRCCLK pin select bit	b5 b4 0 0: TRCCLK pin not used 0 1: P1_4 assigned 1 0: P3_3 assigned 1 1: P3_7 assigned	R/W
b5	TRCCLKSEL1			R/W
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b7	—			—

The TRBRCSR register selects which pin is assigned to the timer RB and timer RC I/O. To use the I/O pin for timer RB and timer RC, set this register.

Set the TRBOSEL0 bit before setting the timer RB associated registers. Set bits TRCCLKSEL0 and TRCCLKSEL1 before setting the timer RC associated registers. Also, do not change the setting values of the TRBOSEL0 bit during timer RB operation. Do not change the setting values of bits TRCCLKSEL0 and TRCCLKSEL1 during timer RC operation.

Change the TRBRCSR register from the initial value to any value during the initial setting of the user's program. Do not change this register again while the main program is executed.

19.2.15 Timer RC Pin Select Register 0 (TRCPSR0)

Address 0182h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TRCIOBSEL3	TRCIOBSEL2	TRCIOBSEL1	TRCIOBSEL0	—	TRCIOASEL2	TRCIOASEL1	TRCIOASEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TRCIOASEL0	TRCIOA/TRCTRG pin select bit	b2 b1 b0 0 0 0: TRCIOA/TRCTRG pin not used 0 0 1: P1_1 assigned 0 1 0: P0_0 assigned 0 1 1: P0_1 assigned 1 0 0: P0_2 assigned 1 0 1: Do not set. (TRCIOA/TRCTRG pin not used.) 1 1 0: P3_1 assigned Other than above: Do not set. (TRCIOA pin not used.)	R/W
b1	TRCIOASEL1			R/W
b2	TRCIOASEL2			R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	TRCIOBSEL0	TRCIOB pin select bit	b7 b6 b5 b4 0 0 0 0: TRCIOB pin not used 0 0 0 1: P1_2 assigned 1 0 0 1: P4_5 assigned Other than above: Do not set. (TRCIOB pin not used.)	R/W
b5	TRCIOBSEL1			R/W
b6	TRCIOBSEL2			R/W
b7	TRCIOBSEL3			R/W

The TRCPSR0 register selects which pin is assigned to the timer RC I/O. To use the I/O pin for timer RC, set this register.

Set the TRCPSR0 register before setting the timer RC associated registers. Also, do not change the setting value in this register during timer RC operation.

Change the TRCPSR0 register from the initial value to any value during the initial setting of the user's program. Do not change this register again while the main program is executed.

19.2.16 Timer RC Pin Select Register 1 (TRCPSR1)

Address 0183h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	TRCIODSEL2	TRCIODSEL1	TRCIODSEL0	—	TRCIOCSEL2	TRCIOCSEL1	TRCIOCSEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TRCIOCSEL0	TRCIOC pin select bit	b2 b1 b0 0 0 0: TRCIOC pin not used 0 0 1: P1_3 assigned 0 1 0: P3_4 assigned Other than above: Do not set. (TRCIOC pin not used.)	R/W
b1	TRCIOCSEL1			R/W
b2	TRCIOCSEL2			R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	TRCIODSEL0	TRCIOD pin select bit	b6 b5 b4 0 0 0: TRCIOD pin not used 0 0 1: P1_0 assigned 0 1 0: P3_5 assigned Other than above: Do not set. (TRCIOD pin not used.)	R/W
b5	TRCIODSEL1			R/W
b6	TRCIODSEL2			R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

The TRCPSR1 register selects which pin is assigned to the timer RC I/O. To use the I/O pin for timer RC, set this register.

Set the TRCPSR1 register before setting the timer RC associated registers. Also, do not change the setting value in this register during timer RC operation.

Change the TRCPSR1 register from the initial value to any value during the initial setting of the user's program. Do not change this register again while the main program is executed.

19.3 Common Items for Multiple Modes

19.3.1 Count Source

The method of selecting the count source is common to all modes.
Table 19.5 lists the Count Source Selection, and Figure 19.2 shows a Count Source Block Diagram.

Table 19.5 Count Source Selection

Count Source	Selection Method
f1, f2, f4, f8, f32	Count source selected using bits TCK2 to TCK0 in TRCCR1 register
fOCO40M fOCO-F	FRA00 bit in FRA0 register set to 1 (high-speed on-chip oscillator on) Bits TCK2 to TCK0 in TRCCR1 register are set to 110b (fOCO40M) Bits TCK2 to TCK0 in TRCCR1 register are set to 111b (fOCO-F)
External signal input to TRCCLK pin	Bits TCK2 to TCK0 in TRCCR1 register are set to 101b (count source is rising edge of external clock) and the corresponding direction bit in the corresponding direction register is set to 0 (input mode)

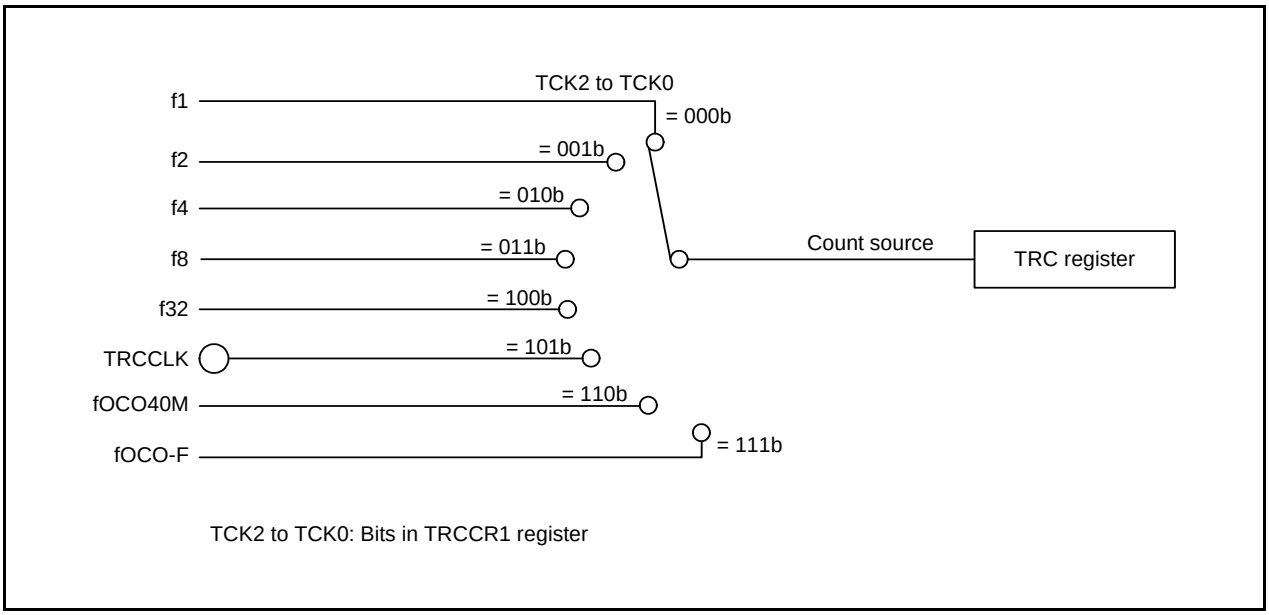


Figure 19.2 Count Source Block Diagram

The pulse width of the external clock input to the TRCCLK pin should be three cycles or more of the timer RC operation clock (refer to **Table 19.1 Timer RC Operation Clock**).
To select fOCO40M or fOCO-F as the count source, set the FRA00 bit in the FRA0 register set to 1 (high-speed on-chip oscillator on), and then set bits TCK2 to TCK0 in the TRCCR1 register to 110b (fOCO40M) or 111b (fOCO-F).

19.3.2 Buffer Operation

Bits BFC and BFD in the TRCMR register are used to select the TRCGRC or TRCGRD register as the buffer register for the TRCGRA or TRCGRB register.

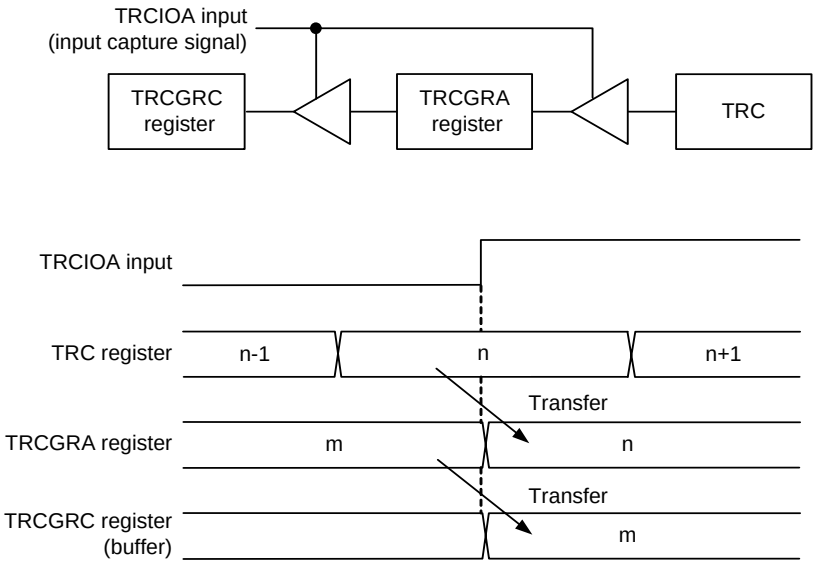
- Buffer register for TRCGRA register: TRCGRC register
- Buffer register for TRCGRB register: TRCGRD register

Buffer operation differs depending on the mode.

Table 19.6 lists the Buffer Operation in Each Mode, Figure 19.3 shows the Buffer Operation for Input Capture Function, and Figure 19.4 shows the Buffer Operation for Output Compare Function.

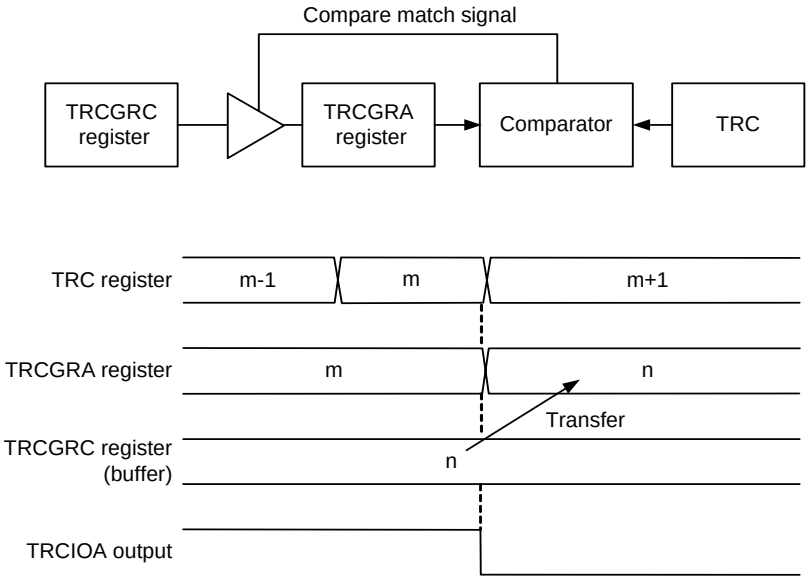
Table 19.6 Buffer Operation in Each Mode

Function, Mode	Transfer Timing	Transfer Destination Register
Input capture function	Input capture signal input	Contents of TRCGRA (TRCGRB) register are transferred to buffer register
Output compare function	Compare match between TRC register and TRCGRA (TRCGRB) register	Contents of buffer register are transferred to TRCGRA (TRCGRB) register
PWM mode		
PWM2 mode	• Compare match between TRC register and TRCGRA register • TRCTRG pin trigger input	Contents of buffer register (TRCGRD) are transferred to TRCGRB register



The above applies under the following conditions:
- The BFC bit in the TRCMR register is set to 1 (the TRCGRC register functions as the buffer register for the TRCGRA register).
- Bits IOA2 to IOA0 in the TRCIOR0 register are set to 100b (input capture at the rising edge).

Figure 19.3 Buffer Operation for Input Capture Function



The above applies under the following conditions:
- The BFC bit in the TRCMR register is set to 1 (the TRCGRC register functions as the buffer register for the TRCGRA register).
- Bits IOA2 to IOA0 in the TRCIOR0 register are set to 001b (“L” output at compare match).

Figure 19.4 Buffer Operation for Output Compare Function

Make the following settings in timer mode.
- To use the TRCGRC register as the buffer register for the TRCGRA register:
  Set the IOC2 bit in the TRCIOR1 register to the same value as the IOA2 bit in the TRCIOR0 register.
- To use the TRCGRD register as the buffer register for the TRCGRB register:
  Set the IOD2 bit in the TRCIOR1 register to the same value as the IOB2 bit in the TRCIOR0 register.

If the TRCGRC or TRCGRD register is functioning as a buffer register for the output compare function, PWM mode or PWM2 mode, the IMFC bit or IMFD bit in the TRCSR register is set to 1 when a compare match with the TRC register occurs.
If the TRCGRC or TRCGRD register is functioning as a buffer register for the input capture function, the IMFC bit or IMFD bit in the TRCSR register is set to 1 at the input edge of a signal input to the TRCIOC pin or TRCIOD pin.

19.3.3 Digital Filter

The input to TRCTRG or TRCIOj (j = A, B, C, or D) is sampled, and the level is considered to be determined when three matches occur. The digital filter function and sampling clock are selected using the TRCDF register. Figure 19.5 shows a Digital Filter Block Diagram.

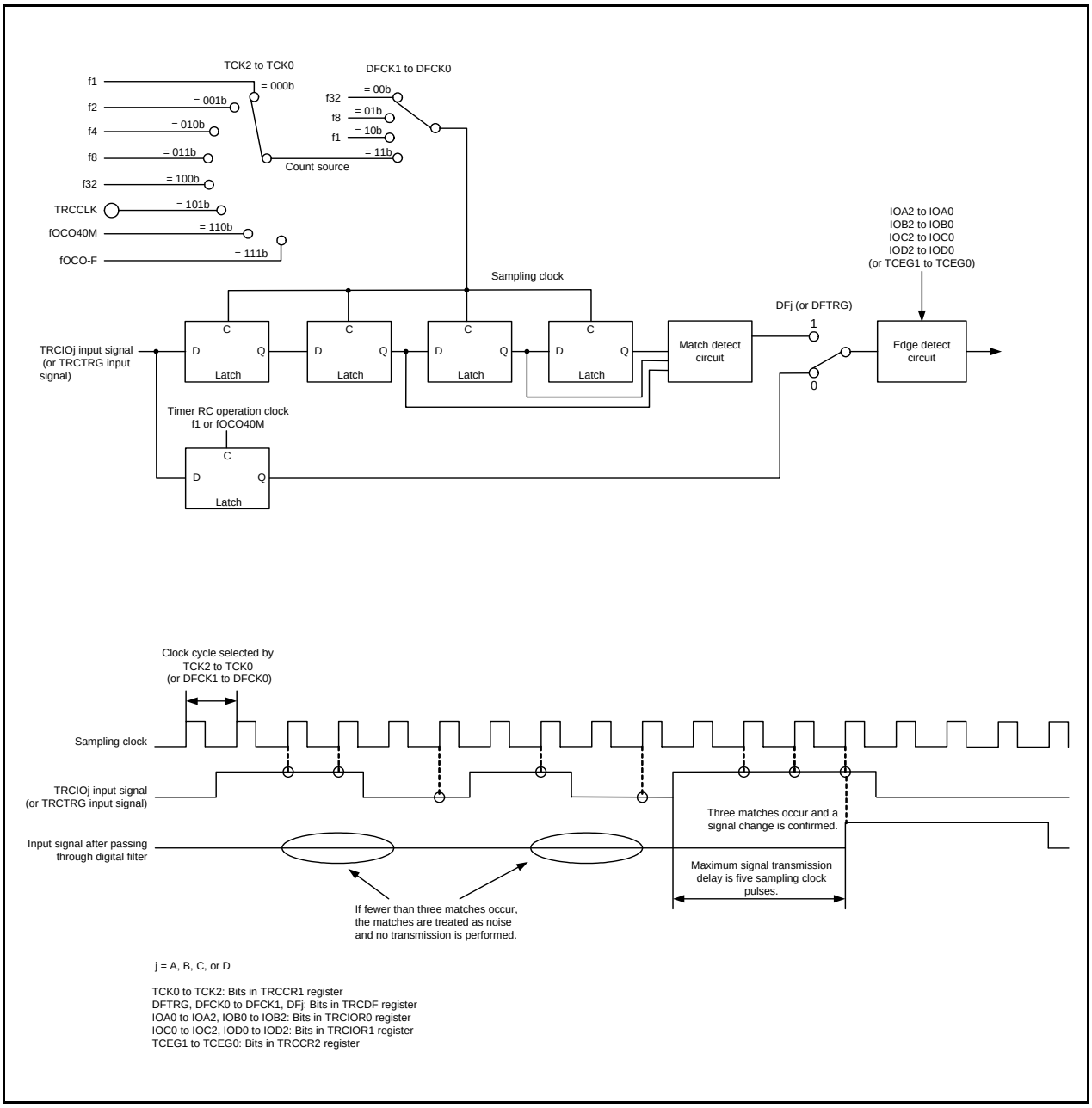


Figure 19.5 Digital Filter Block Diagram

19.3.4 Forced Cutoff of Pulse Output

When using the timer mode's output compare function, the PWM mode, or the PWM2 mode, pulse output from the TRCIOj (j = A, B, C, or D) output pin can be forcibly cut off and the TRCIOj pin set to function as a programmable I/O port by means of input to the $\overline{\text{INT0}}$ pin.
A pin used for output by the timer mode's output compare function, the PWM mode, or the PWM2 mode can be set to function as the timer RC output pin by setting the Ej bit in the TRCOER register to 0 (timer RC output enabled). If "L" is input to the $\overline{\text{INT0}}$ pin while the PTO bit in the TRCOER register is set to 1 (pulse output forced cutoff signal input $\overline{\text{INT0}}$ enabled), bits EA, EB, EC, and ED in the TRCOER register are all set to 1 (timer RC output disabled, TRCIOj output pin functions as the programmable I/O port). When one or two cycles of the timer RC operation clock after "L" input to the $\overline{\text{INT0}}$ pin (refer to **Table 19.1 Timer RC Operation Clock**) have elapsed, the TRCIOj output pin becomes a programmable I/O port.

Make the following settings to use this function:
- Set the pin state following forced cutoff of pulse output (high impedance (input), "L" output, or "H" output). (refer to **7. I/O Ports**).
- Set the INT0EN bit in the INTEN register to 1 ($\overline{\text{INT0}}$ input enabled) and the INT0PL bit to 0 (one edge), and set the POL bit in the INT0IC register to 0 (falling edge selected).
- Set the PD4_5 bit in the PD4 register to 0 (input mode).
- Select the $\overline{\text{INT0}}$ digital filter by bits INT0F1 to INT0F0 in the INTF register.
- Set the PTO bit in the TRCOER register to 1 (pulse output forced cutoff signal input $\overline{\text{INT0}}$ enabled).

The IR bit in the INT0IC register is set to 1 (interrupt request) in accordance with the setting of the POL bit in the INT0IC register and the INT0PL bit in the INTEN register, and a change in the $\overline{\text{INT0}}$ pin input (refer to **11.9 Notes on Interrupts**).
For details on interrupts, refer to **11. Interrupts**.

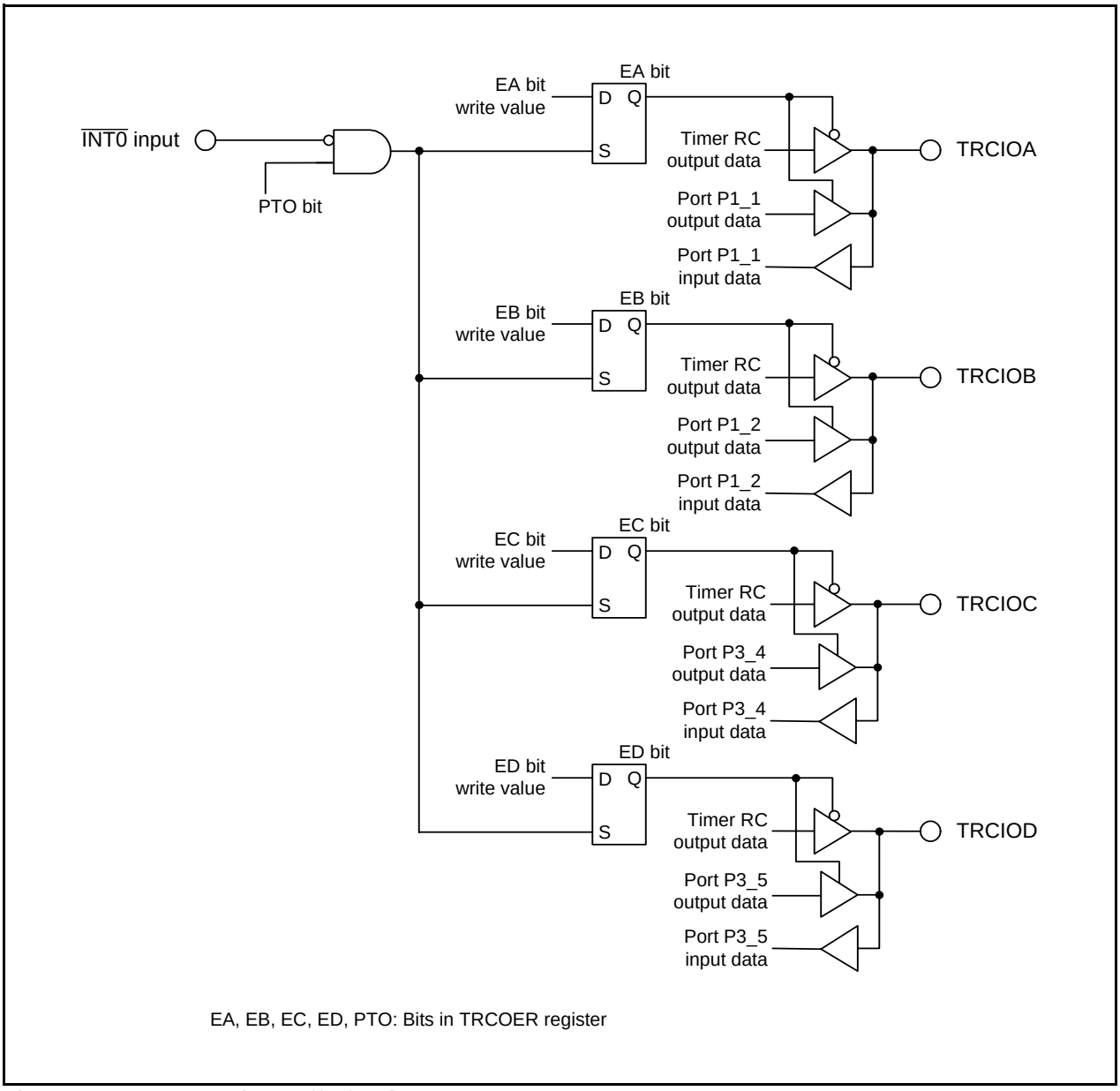


Figure 19.6 Forced Cutoff of Pulse Output

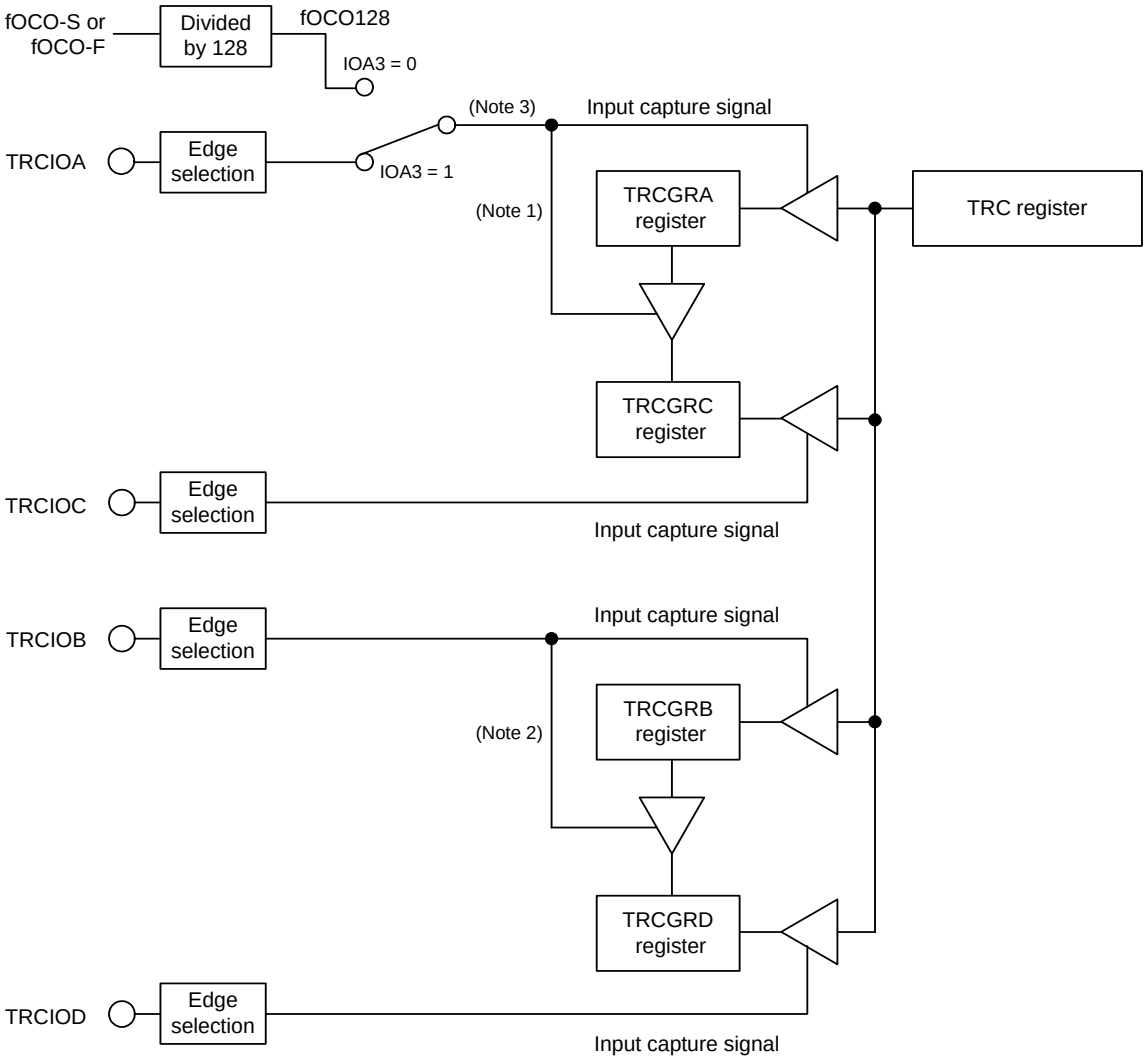
19.4 Timer Mode (Input Capture Function)

This function measures the width or period of an external signal. An external signal input to the TRCIOj (j = A, B, C, or D) pin acts as a trigger for transferring the contents of the TRC register (counter) to the TRCGRj register (input capture). The input capture function, or any other mode or function, can be selected for each individual pin. The TRCGRA register can also select fOCO128 signal as input-capture trigger input.
Table 19.7 lists the Specifications of Input Capture Function, Figure 19.7 shows a Block Diagram of Input Capture Function, Table 19.8 lists the Functions of TRCGRj Register when Using Input Capture Function, and Figure 19.8 shows an Operating Example of Input Capture Function.

Table 19.7 Specifications of Input Capture Function

Item	Specification
Count source	f1, f2, f4, f8, f32, fOCO40M, fOCO-F, or external signal (rising edge) input to TRCCLK pin
Count operation	Increment
Count period	• The CCLR bit in the TRCCR1 register is set to 0 (free running operation): 1/fk × 65,536 fk: Count source frequency • The CCLR bit in the TRCCR1 register is set to 1 (TRC register set to 0000h at TRCGRA input capture): 1/fk × (n+1) n: TRCGRA register setting value
Count start condition	1 (count starts) is written to the TSTART bit in the TRCMR register.
Count stop condition	0 (count stops) is written to the TSTART bit in the TRCMR register. The TRC register retains a value before count stops.
Interrupt request generation timing	• Input capture (valid edge of TRCIOj input or fOCO128 signal edge) • The TRC register overflows.
TRCIOA, TRCIOB, TRCIOC, and TRCIOD pin functions	Programmable I/O port or input capture input (selectable individually for each pin)
$\overline{\text{INT0}}$ pin function	Programmable I/O port or $\overline{\text{INT0}}$ interrupt input
Read from timer	The count value can be read by reading TRC register.
Write to timer	The TRC register can be written to.
Select functions	• Input capture input pin selection One or more of pins TRCIOA, TRCIOB, TRCIOC, and TRCIOD • Input capture input valid edge selection Rising edge, falling edge, or both rising and falling edges • Buffer operation (Refer to **19.3.2 Buffer Operation**.) • Digital filter (Refer to **19.3.3 Digital Filter**.) • Timing for setting the TRC register to 0000h Overflow or input capture • Input-capture trigger selected fOCO128 can be selected for input-capture trigger input of the TRCGRA register.

j = A, B, C, or D



IOA3: Bit in TRCIOR0 register

Notes:
1. The BFC bit in the TRCMR register is set to 1 (TRCGRC register functions as the buffer register for the TRCGRA register).
2. The BFD bit in the TRCMR register is set to 1 (TRCGRD register functions as the buffer register for the TRCGRB register).
3. The trigger input of the TRCGRA register can select the TRCIOA pin input or fOCO128 signal.

Figure 19.7 Block Diagram of Input Capture Function

19.4.1 Timer RC I/O Control Register 0 (TRCIOR0) for Input Capture Function

Address 0124h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	IOB2	IOB1	IOB0	IOA3	IOA2	IOA1	IOA0
After Reset	1	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IOA0	TRCGRA control bit	b1 b0 0 0: Input capture to the TRCGRA register at the rising edge 0 1: Input capture to the TRCGRA register at the falling edge 1 0: Input capture to the TRCGRA register at both edges 1 1: Do not set.	R/W
b1	IOA1			R/W
b2	IOA2	TRCGRA mode select bit (1)	Set to 1 (input capture) in the input capture function.	R/W
b3	IOA3	TRCGRA input capture input switch bit (3)	0: fOCO128 signal 1: TRCIOA pin input	R/W
b4	IOB0	TRCGRB control bit	b5 b4 0 0: Input capture to the TRCGRB register at the rising edge 0 1: Input capture to the TRCGRB register at the falling edge 1 0: Input capture to the TRCGRB register at both edges 1 1: Do not set.	R/W
b5	IOB1			R/W
b6	IOB2	TRCGRB mode select bit (2)	Set to 1 (input capture) in the input capture function.	R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—

Notes:
1. When the BFC bit in the TRCMR register is set to 1 (buffer register of TRCGRA register), set the IOC2 bit in the TRCIOR1 register to the same value as the IOA2 bit in the TRCIOR0 register.
2. When the BFD bit in the TRCMR register is set to 1 (buffer register of TRCGRB register), set the IOD2 bit in the TRCIOR1 register to the same value as the IOB2 bit in the TRCIOR0 register.
3. The IOA3 bit is enabled when the IOA2 bit is set to 1 (input capture function).

19.4.2 Timer RC I/O Control Register 1 (TRCIOR1) for Input Capture Function

Address 0125h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	IOD3	IOD2	IOD1	IOD0	IOC3	IOC2	IOC1	IOC0
After Reset	1	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IOC0	TRCGRC control bit	b1 b0 0 0: Input capture to the TRCGRC register at the rising edge 0 1: Input capture to the TRCGRC register at the falling edge 1 0: Input capture to the TRCGRC register at both edges 1 1: Do not set.	R/W
b1	IOC1			R/W
b2	IOC2	TRCGRC mode select bit (1)	Set to 1 (input capture) in the input capture function.	R/W
b3	IOC3	TRCGRC register function select bit	Set to 1.	R/W
b4	IOD0	TRCGRD control bit	b5 b4 0 0: Input capture to the TRCGRD register at the rising edge 0 1: Input capture to the TRCGRD register at the falling edge 1 0: Input capture to the TRCGRD register at both edges 1 1: Do not set.	R/W
b5	IOD1			R/W
b6	IOD2	TRCGRD mode select bit (2)	Set to 1 (input capture) in the input capture function.	R/W
b7	IOD3	TRCGRD register function select bit	Set to 1.	R/W

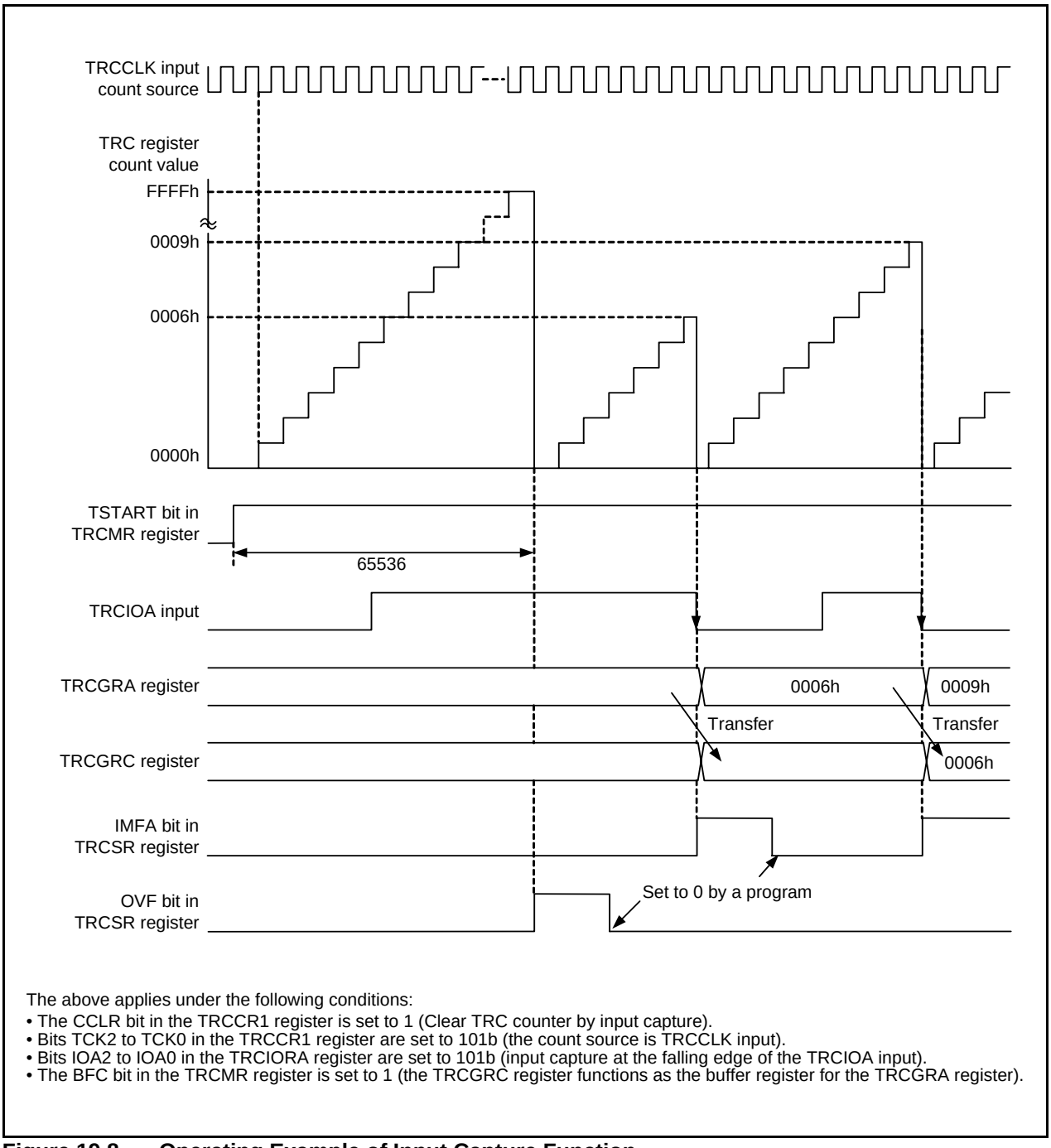
Notes:
1. When the BFC bit in the TRCMR register is set to 1 (buffer register of TRCGRA register), set the IOC2 bit in the TRCIOR1 register to the same value as the IOA2 bit in the TRCIOR0 register.
2. When the BFD bit in the TRCMR register is set to 1 (buffer register of TRCGRB register), set the IOD2 bit in the TRCIOR1 register to the same value as the IOB2 bit in the TRCIOR0 register.

Table 19.8 Functions of TRCGRj Register when Using Input Capture Function

Register	Setting	Register Function	Input Capture Input Pin
TRCGRA	—	General register. Can be used to read the TRC register value at input capture.	TRCIOA
TRCGRB			TRCIOB
TRCGRC	BFC = 0	General register. Can be used to read the TRC register value at input capture.	TRCIOC
TRCGRD	BFD = 0		TRCIOD
TRCGRC	BFC = 1	Buffer registers. Can be used to hold transferred value from the general register. (Refer to **19.3.2 Buffer Operation**.)	TRCIOA
TRCGRD	BFD = 1		TRCIOB

j = A, B, C, or D
BFC, BFD: Bits in TRCMR register

19.4.3 Operating Example



The above applies under the following conditions:
- The CCLR bit in the TRCCR1 register is set to 1 (Clear TRC counter by input capture).
- Bits TCK2 to TCK0 in the TRCCR1 register are set to 101b (the count source is TRCCLK input).
- Bits IOA2 to IOA0 in the TRCIORA register are set to 101b (input capture at the falling edge of the TRCIOA input).
- The BFC bit in the TRCMR register is set to 1 (the TRCGRC register functions as the buffer register for the TRCGRA register).

Figure 19.8 Operating Example of Input Capture Function

19.5 Timer Mode (Output Compare Function)

This function detects when the contents of the TRC register (counter) and the TRCGRj register (j = A, B, C, or D) match (compare match). When a match occurs a signal is output from the TRCIOj pin at a given level. The output compare function, or other mode or function, can be selected for each individual pin.
Table 19.9 lists the Specifications of Output Compare Function, Figure 19.9 shows a Block Diagram of Output Compare Function, Table 19.10 lists the Functions of TRCGRj Register when Using Output Compare Function, and Figure 19.10 shows an Operating Example of Output Compare Function.

Table 19.9 Specifications of Output Compare Function

Item	Specification
Count source	f1, f2, f4, f8, f32, fOCO40M, fOCO-F, or external signal (rising edge) input to TRCCLK pin
Count operation	Increment
Count period	• The CCLR bit in the TRCCR1 register is set to 0 (free running operation): 1/fk × 65,536 fk: Count source frequency • The CCLR bit in the TRCCR1 register is set to 1 (TRC register set to 0000h at TRCGRA compare match): 1/fk × (n+1) n: TRCGRA register setting value
Waveform output timing	Compare match
Count start condition	1 (count starts) is written to the TSTART bit in the TRCMR register.
Count stop condition	• When the CSEL bit in the TRCCR2 register is set to 0 (count continues after compare match with TRCGRA). 0 (count stops) is written to the TSTART bit in the TRCMR register. The output compare output pin retains output level before count stops, the TRC register retains a value before count stops. • When the CSEL bit in the TRCCR2 register is set to 1 (count stops at compare match with TRCGRA register). The count stops at the compare match with the TRCGRA register. The output compare output pin retains the level after the output is changed by the compare match.
Interrupt request generation timing	• Compare match (contents of registers TRC and TRCGRj match) • The TRC register overflows.
TRCIOA, TRCIOB, TRCIOC, and TRCIOD pin functions	Programmable I/O port or output compare output (Selectable individually for each pin)
$\overline{\text{INT0}}$ pin function	Programmable I/O port, pulse output forced cutoff signal input, or $\overline{\text{INT0}}$ interrupt input
Read from timer	The count value can be read by reading the TRC register.
Write to timer	The TRC register can be written to.
Select functions	• Output compare output pin selection One or more of pins TRCIOA, TRCIOB, TRCIOC, and TRCIOD • Compare match output level selection “L” output, “H” output, or toggle output • Initial output level selection Sets output level for period from count start to compare match • Timing for setting the TRC register to 0000h Overflow or compare match with the TRCGRA register • Buffer operation (Refer to **19.3.2 Buffer Operation**.) • Pulse output forced cutoff signal input (Refer to **19.3.4 Forced Cutoff of Pulse Output**.) • Can be used as an internal timer by disabling timer RC output • Changing output pins for registers TRCGRC and TRCGRD TRCGRC can be used for output control of the TRCIOA pin and TRCGRD can be used for output control of the TRCIOB pin. • SCU trigger generation

j = A, B, C, or D

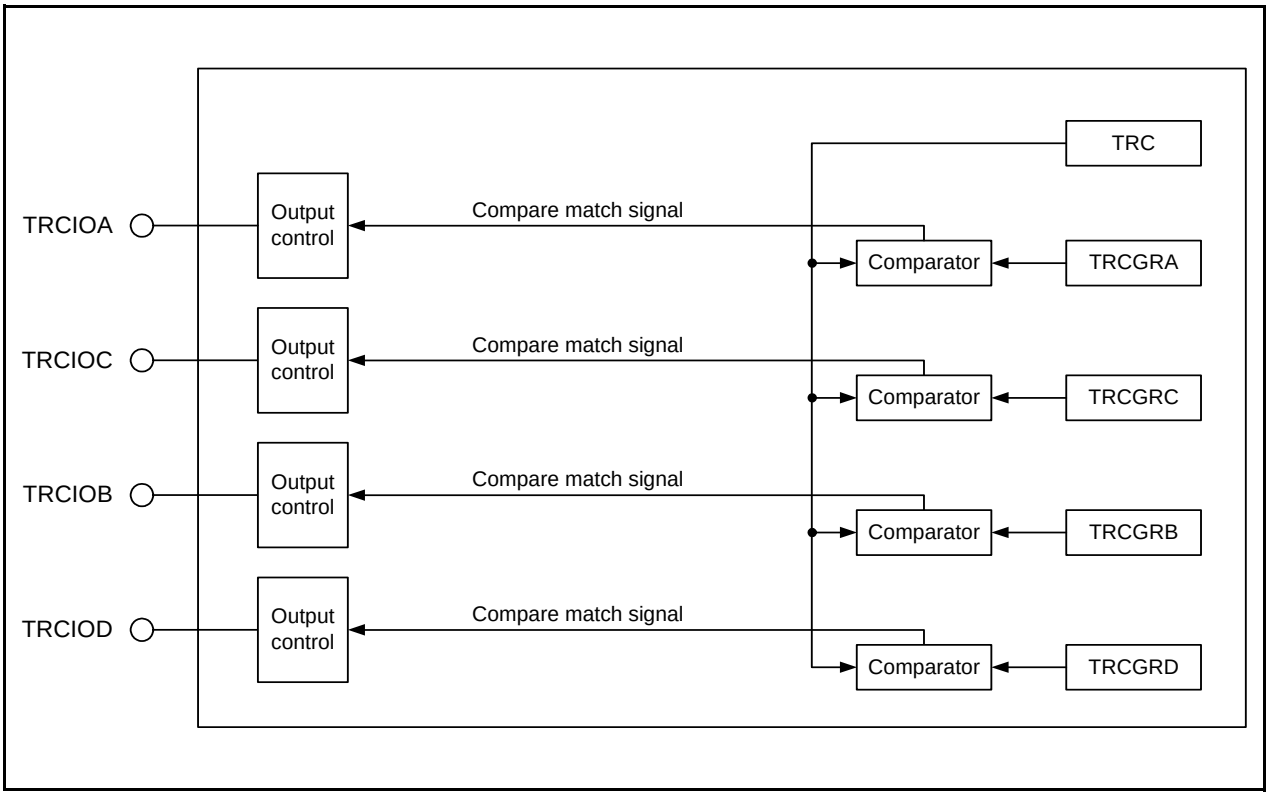


Figure 19.9 Block Diagram of Output Compare Function

19.5.1 Timer RC Control Register 1 (TRCCR1) for Output Compare Function

Address 0121h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CCLR	TCK2	TCK1	TCK0	TOD	TOC	TOB	TOA
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TOA	TRCIOA output level select bit (1, 2)	0: Initial output “L” 1: Initial output “H”	R/W
b1	TOB	TRCIOB output level select bit (1, 2)		R/W
b2	TOC	TRCIOC output level select bit (1, 2)		R/W
b3	TOD	TRCIOD output level select bit (1, 2)		R/W
b4	TCK0	Count source select bit (1)	b6 b5 b4 0 0 0: f1 0 0 1: f2 0 1 0: f4 0 1 1: f8 1 0 0: f32 1 0 1: TRCCLK input rising edge 1 1 0: fOCO40M 1 1 1: fOCO-F (3)	R/W
b5	TCK1			R/W
b6	TCK2			R/W
b7	CCLR	TRC counter clear select bit	0: Disable clear (free-running operation) 1: Clear by compare match in the TRCGRA register	R/W

Notes:
1. Set to these bits when the TSTART bit in the TRCMR register is set to 0 (count stops).
2. If the pin function is set for waveform output (refer to **7.5 Port Settings**), the initial output level is output when the TRCCR1 register is set.
3. To select fOCO-F, set it to the clock frequency higher than the CPU clock frequency.

Table 19.10 Functions of TRCGRj Register when Using Output Compare Function

Register	Setting	Register Function	Output Compare Output Pin
TRCGRA	—	General register. Write a compare value to one of these registers.	TRCIOA
TRCGRB			TRCIOB
TRCGRC	BFC = 0	General register. Write a compare value to one of these registers.	TRCIOC
TRCGRD	BFD = 0		TRCIOD
TRCGRC	BFC = 1	Buffer register. Write the next compare value to one of these registers. (Refer to **19.3.2 Buffer Operation**.)	TRCIOA
TRCGRD	BFD = 1		TRCIOB

j = A, B, C, or D
BFC, BFD: Bits in TRCMR register

19.5.2 Timer RC I/O Control Register 0 (TRCIOR0) for Output Compare Function

Address 0124h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	IOB2	IOB1	IOB0	IOA3	IOA2	IOA1	IOA0
After Reset	1	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IOA0	TRCGRA control bit	b1 b0 0 0: Disable pin output by compare match (TRCIOA pin functions as the programmable I/O port) 0 1: “L” output by compare match in the TRCGRA register 1 0: “H” output by compare match in the TRCGRA register 1 1: Toggle output by compare match in the TRCGRA register	R/W
b1	IOA1			R/W
b2	IOA2	TRCGRA mode select bit (1)	Set to 0 (output compare) in the output compare function.	R/W
b3	IOA3	TRCGRA input capture input switch bit	Set to 1.	R/W
b4	IOB0	TRCGRB control bit	b5 b4 0 0: Disable pin output by compare match (TRCIOB pin functions as the programmable I/O port) 0 1: “L” output by compare match in the TRCGRB register 1 0: “H” output by compare match in the TRCGRB register 1 1: Toggle output by compare match in the TRCGRB register	R/W
b5	IOB1			R/W
b6	IOB2	TRCGRB mode select bit (2)	Set to 0 (output compare) in the output compare function.	R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—

Notes:
1. When the BFC bit in the TRCMR register is set to 1 (buffer register of TRCGRA register), set the IOC2 bit in theTRCIOR1 register to the same value as the IOA2 bit in the TRCIOR0 register.
2. When the BFD bit in the TRCMR register is set to 1 (buffer register of TRCGRB register), set the IOD2 bit in the TRCIOR1 register to the same value as the IOB2 bit in the TRCIOR0 register.

19.5.3 Timer RC I/O Control Register 1 (TRCIOR1) for Output Compare Function

Address 0125h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	IOD3	IOD2	IOD1	IOD0	IOC3	IOC2	IOC1	IOC0
After Reset	1	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IOC0	TRCGRC control bit	b1 b0 0 0: Disable pin output by compare match 0 1: “L” output by compare match in the TRCGRC register 1 0: “H” output by compare match in the TRCGRC register 1 1: Toggle output by compare match in the TRCGRC register	R/W
b1	IOC1			R/W
b2	IOC2	TRCGRC mode select bit (1)	Set to 0 (output compare) in the output compare function.	R/W
b3	IOC3	TRCGRC register function select bit	0: TRCIOA output register 1: General register or buffer register	R/W
b4	IOD0	TRCGRD control bit	b5 b4 0 0: Disable pin output by compare match 0 1: “L” output by compare match in the TRCGRD register 1 0: “H” output by compare match in the TRCGRD register 1 1: Toggle output by compare match in the TRCGRD register	R/W
b5	IOD1			R/W
b6	IOD2	TRCGRD mode select bit (2)	Set to 0 (output compare) in the output compare function.	R/W
b7	IOD3	TRCGRD register function select bit	0: TRCIOB output register 1: General register or buffer register	R/W

Notes:
1. When the BFC bit in the TRCMR register is set to 1 (buffer register of TRCGRA register), set the IOC2 bit in theTRCIOR1 register to the same value as the IOA2 bit in the TRCIOR0 register.
2. When the BFD bit in the TRCMR register is set to 1 (buffer register of TRCGRB register), set the IOD2 bit in theTRCIOR1 register to the same value as the IOB2 bit in the TRCIOR0 register.

19.5.4 Timer RC Control Register 2 (TRCCR2) for Output Compare Function

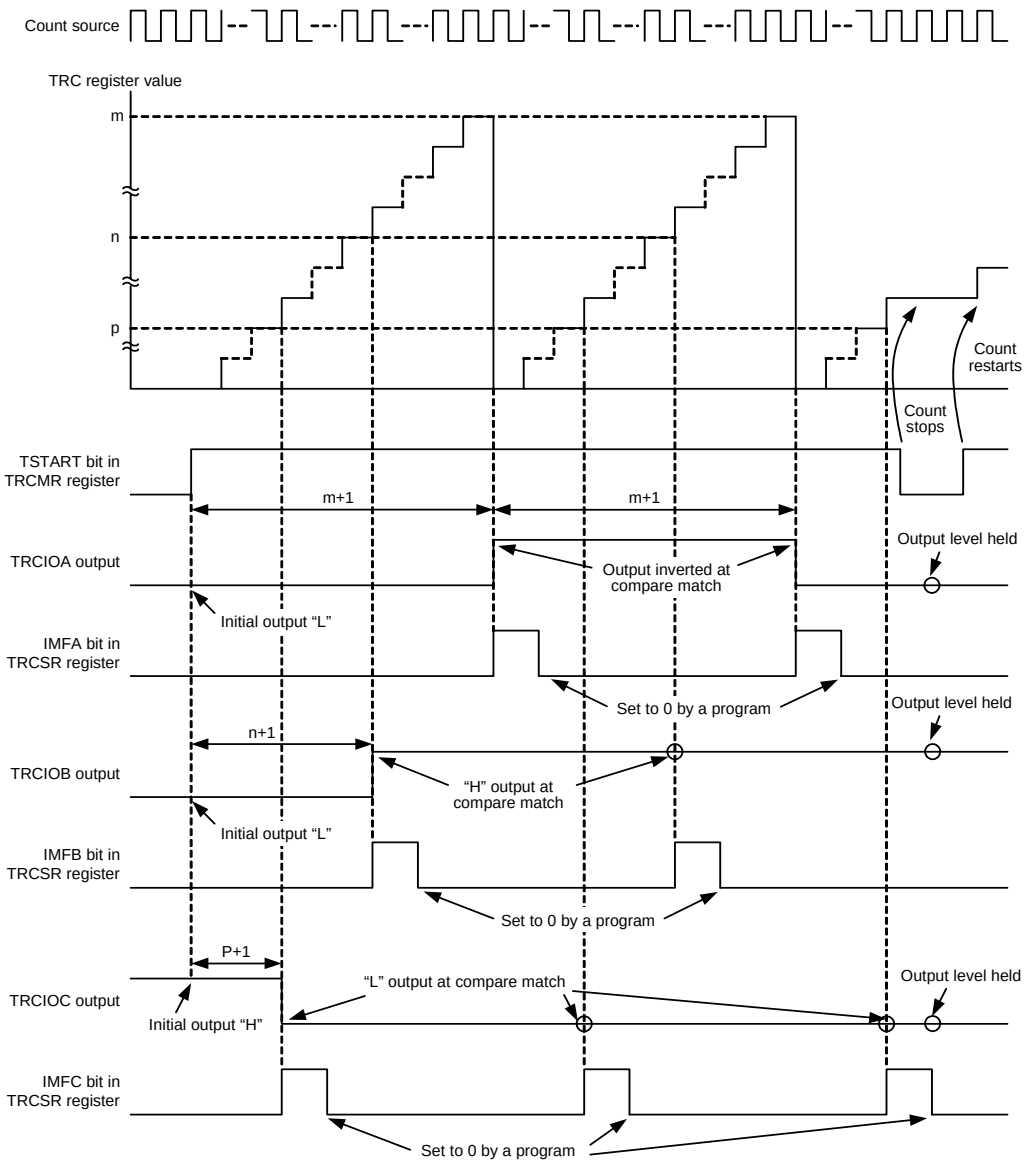
Address 0130h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TCEG1	TCEG0	CSEL	—	—	POLD	POLC	POLB
After Reset	0	0	0	1	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	POLB	PWM mode output level control bit B (1)	0: TRCIOB output level selected as “L” active 1: TRCIOB output level selected as “H” active	R/W
b1	POLC	PWM mode output level control bit C (1)	0: TRCIOC output level selected as “L” active 1: TRCIOC output level selected as “H” active	R/W
b2	POLD	PWM mode output level control bit D (1)	0: TRCIOD output level selected as “L” active 1: TRCIOD output level selected as “H” active	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b4	—			
b5	CSEL	TRC count operation select bit (2)	0: Count continues at compare match with the TRCGRA register 1: Count stops at compare match with the TRCGRA register	R/W
b6	TCEG0	TRCTRG input edge select bit (3)	b7 b6 0 0: Disable the trigger input from the TRCTRG pin 0 1: Rising edge selected 1 0: Falling edge selected 1 1: Both edges selected	R/W
b7	TCEG1			R/W

Notes:
1. Enabled when in PWM mode.
2. Enabled when in output compare function, PWM mode, or PWM2 mode. For notes on PWM2 mode, refer to **19.9.6 TRCMR Register in PWM2 Mode**.
3. Enabled when in PWM2 mode.

19.5.5 Operating Example



m: TRCGRA register setting value
n: TRCGRB register setting value
p: TRCGRC register setting value

The above applies under the following conditions:
- Bits BFC and BFD in the TRCMR register are set to 0 (TRCGRC and TRCGRD do not operate as buffers).
- Bits EA, EB, and EC in the TRCOER register are set to 0 (output from TRCIOA, TRCIOB, and TRCIOC enabled).
- The CCLR bit in the TRCCR1 register is set to 1 (set the TRC register to 0000h by TRCGRA compare match).
- In the TRCCR1 register, bits TOA and TOB are set to 0 ("L" initial output until compare match) and the TOC bit is set to 1 ("H" initial output until compare match).
- Bits IOA2 to IOA0 in the TRCIOR0 register are set to 011b (TRCIOA output inverted at TRCGRA compare match).
- Bits IOB2 to IOB0 in the TRCIOR0 register are set to 010b ("H" TRCIOB output at TRCGRB compare match).
- Bits IOC2 to IOC2 in the TRCIOR1 register are set to 001b ("L" TRCIOC output at TRCGRC compare match).
- The CSEL bit in the TRCCR2 register is set to 0 (TRC count continues after TRCGRA compare match).

Figure 19.10 Operating Example of Output Compare Function

19.5.6 Changing Output Pins in Registers TRCGRC and TRCGRD

The TRCGRC register can be used for output control of the TRCIOA pin, and the TRCGRD register can be used for output control of the TRCIOB pin. Therefore, each pin output can be controlled as follows:

- TRCIOA output is controlled by the values in registers TRCGRA and TRCGRC.
- TRCIOB output is controlled by the values in registers TRCGRB and TRCGRD.

Change output pins in registers TRCGRC and TRCGRD as follows:

- Set the IOC3 bit in the TRCIOR1 register to 0 (TRCIOA output register) and set the IOD3 bit to 0 (TRCIOB output register).
- Set bits BFC and BFD in the TRCMR register to 0 (general register).
- Set different values in registers TRCGRC and TRCGRA. Also, set different values in registers TRCGRD and TRCGRB.

Figure 19.12 shows an Operating Example When TRCGRC Register is Used for Output Control of TRCIOA Pin and TRCGRD Register is Used for Output Control of TRCIOB Pin.

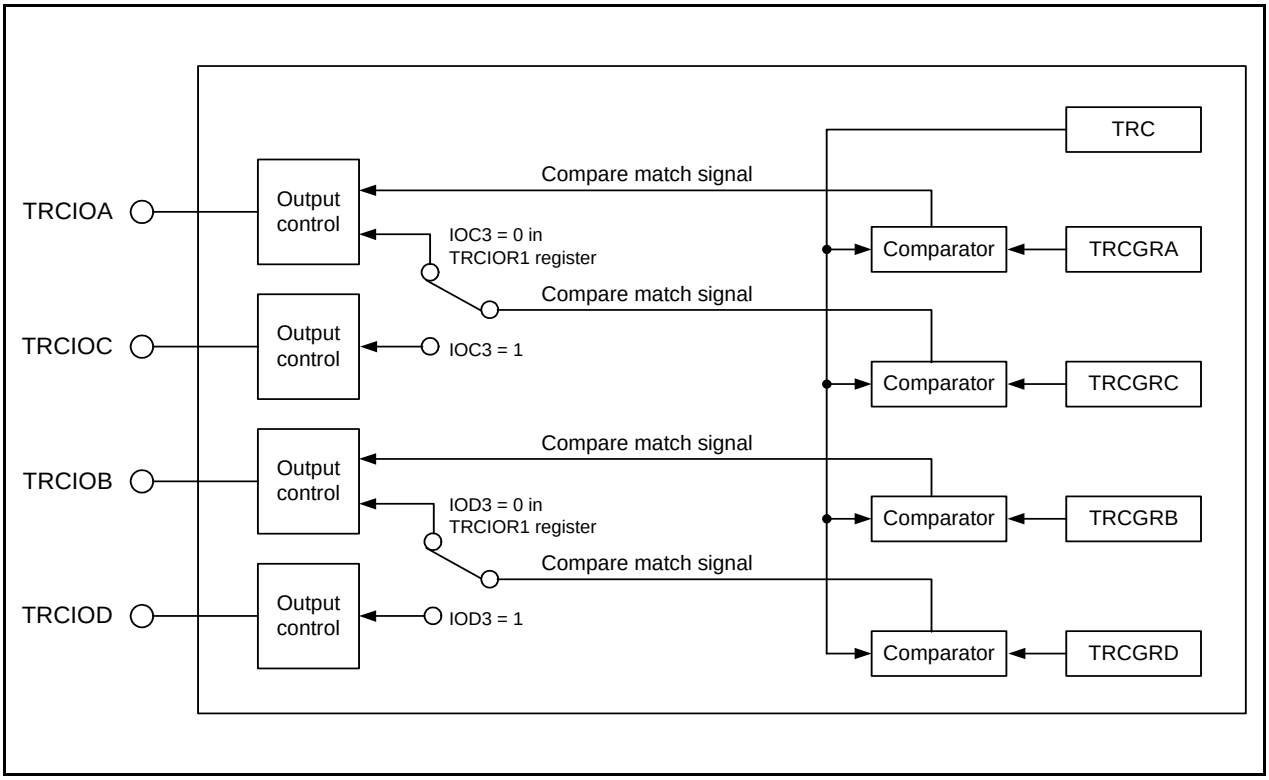
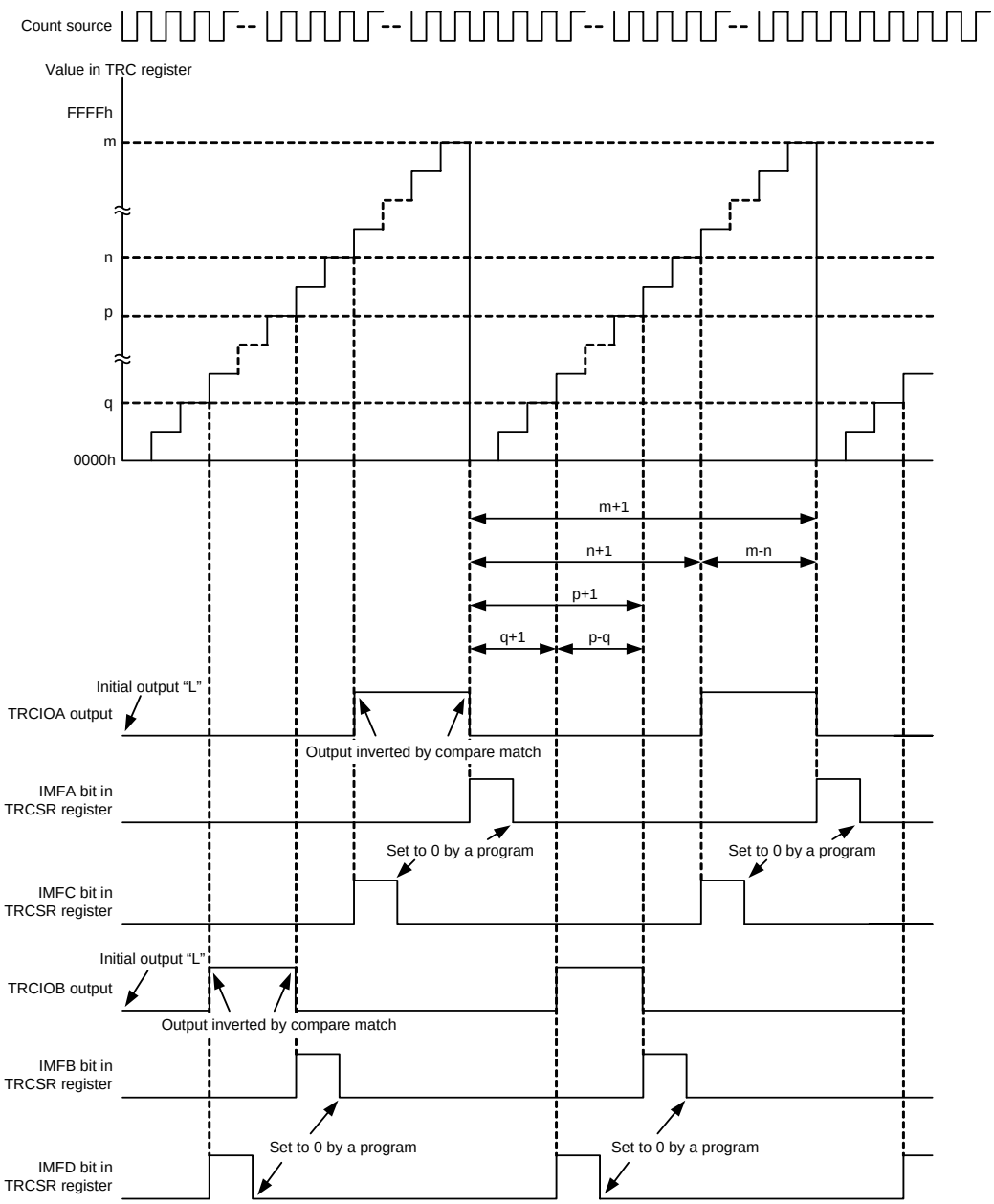


Figure 19.11 Changing Output Pins in Registers TRCGRC and TRCGRD



m: Value set in TRCGRA register
n: Value set in TRCGRC register
p: Value set in TRCGRB register
q: Value set in TRCGRD register

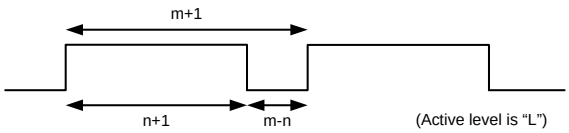
The above applies under the following conditions:
- Bits BFC and BFD in the TRCMR register are set to 0 (registers TRCGRC and TRCGRD are not used as buffer register).
- Bits EA and EB in the TRCOER register are set to 0 (enable TRCIOA and TRCIOB pin outputs).
- The CCLR bit in the TRCCR1 register are set to 1 (set the TRC register to 0000h by compare match in the TRCGRA register).
- Bits TOA and TOB in the TRCCR1 register are set to 0 (initial output "L" to compare match).
- Bits IOA2 to IOA0 in the TRCIOR0 register are set to 011b (TRCIOA output inverted at TRCGRA register compare match).
- Bits IOB2 to IOB0 in the TRCIOR0 register are set to 011b (TRCIOB output inverted at TRCGRB register compare match).
- Bits IOC2 to IOC0 in the TRCIOR1 register are set to 011b (TRCIOA output inverted at TRCGRC register compare match).
- The IOC3 bit in the TRCIOR1 register are set to 0 (TRCIOA output register).
- Bits IOD2 to IOD0 in the TRCIOR1 register are set to 011b (TRCIOB output inverted at TRCGRD register compare match).
- The IOD3 bit in the TRCIOR1 register are set to 0 (TRCIOB output register).
- The CSEL bit in the TRCCR2 register are set to 0 (TRC continues counting after compare match).

Figure 19.12 Operating Example When TRCGRC Register is Used for Output Control of TRCIOA Pin and TRCGRD Register is Used for Output Control of TRCIOB Pin

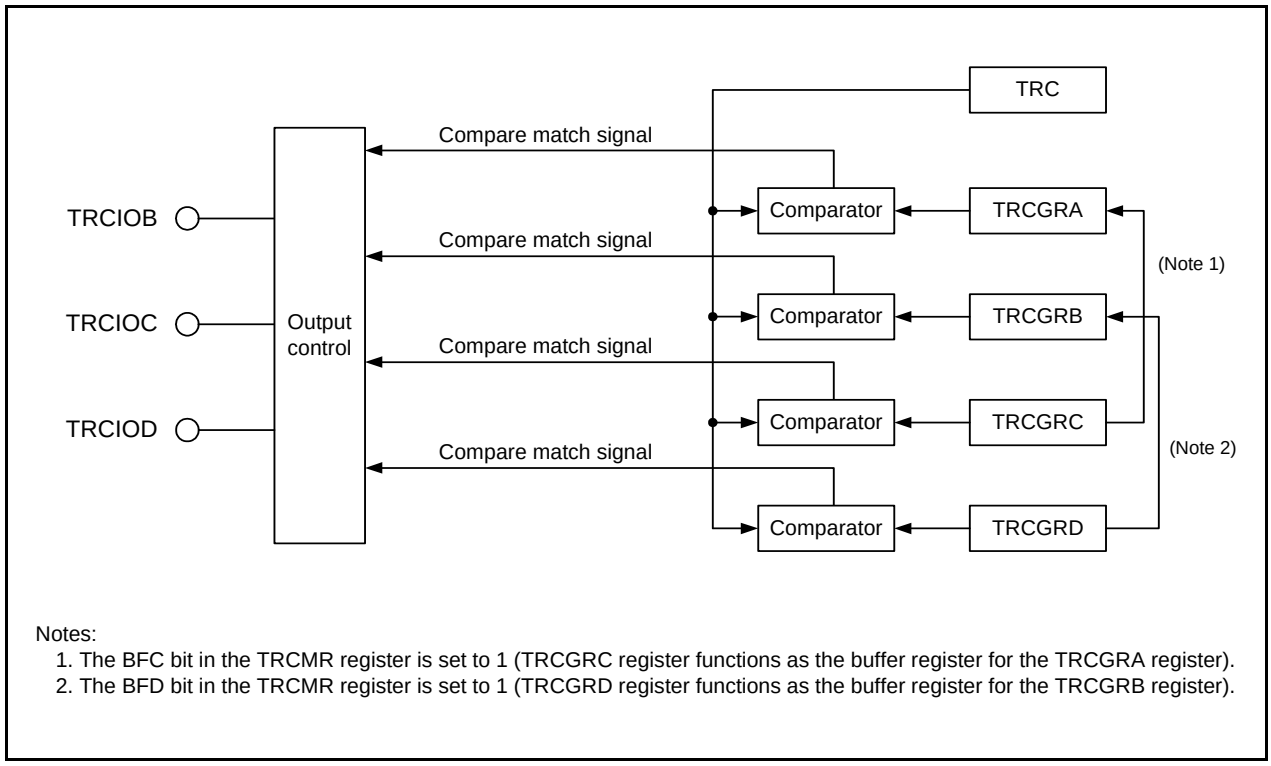
19.6 PWM Mode

This mode outputs PWM waveforms. A maximum of three PWM waveforms with the same period are output. The PWM mode, or the timer mode, can be selected for each individual pin. (However, since the TRCGRA register is used when using any pin for the PWM mode, the TRCGRA register cannot be used for the timer mode.)
Table 19.11 lists the Specifications of PWM Mode, Figure 19.13 shows a PWM Mode Block Diagram, Table 19.12 lists the Functions of TRCGRh Register in PWM Mode, and Figures 19.14 and 19.15 show Operating Examples of PWM Mode.

Table 19.11 Specifications of PWM Mode

Item	Specification
Count source	f1, f2, f4, f8, f32, fOCO40M, fOCO-F, or external signal (rising edge) input to TRCCLK pin
Count operation	Increment
PWM waveform	PWM period: 1/fk × (m+1) Active level width: 1/fk × (m-n) Inactive level width: 1/fk × (n+1) fk: Count source frequency m: TRCGRA register setting value n: TRCGRj register setting value 
Count start condition	1 (count starts) is written to the TSTART bit in the TRCMR register.
Count stop condition	• When the CSEL bit in the TRCCR2 register is set to 0 (count continues after compare match with TRCGRA). 0 (count stops) is written to the TSTART bit in the TRCMR register. PWM output pin retains output level before count stops, TRC register retains value before count stops. • When the CSEL bit in the TRCCR2 register is set to 1 (count stops at compare match with TRCGRA register). The count stops at the compare match with the TRCGRA register. The PWM output pin retains the level after the output is changed by the compare match.
Interrupt request generation timing	• Compare match (contents of registers TRC and TRCGRh match) • The TRC register overflows.
TRCIOA pin function	Programmable I/O port
TRCIOB, TRCIOC, and TRCIOD pin functions	Programmable I/O port or PWM output (selectable individually for each pin)
$\overline{\text{INT0}}$ pin function	Programmable I/O port, pulse output forced cutoff signal input, or $\overline{\text{INT0}}$ interrupt input
Read from timer	The count value can be read by reading the TRC register.
Write to timer	The TRC register can be written to.
Select functions	• One to three pins selectable as PWM output pins One or more of pins TRCIOB, TRCIOC, and TRCIOD • Active level selectable for each pin • Initial level selectable for each pin • Buffer operation (Refer to **19.3.2 Buffer Operation**.) • Pulse output forced cutoff signal input (Refer to **19.3.4 Forced Cutoff of Pulse Output**.) • SCU trigger generation

j = B, C, or D
h = A, B, C, or D



Notes:
1. The BFC bit in the TRCMR register is set to 1 (TRCGRC register functions as the buffer register for the TRCGRA register).
2. The BFD bit in the TRCMR register is set to 1 (TRCGRD register functions as the buffer register for the TRCGRB register).

Figure 19.13 PWM Mode Block Diagram

19.6.1 Timer RC Control Register 1 (TRCCR1) in PWM Mode

Address 0121h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CCLR	TCK2	TCK1	TCK0	TOD	TOC	TOB	TOA
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TOA	TRCIOA output level select bit (1)	Disabled in PWM mode	R/W
b1	TOB	TRCIOB output level select bit (1, 2)	0: Initial output selected as non-active level 1: Initial output selected as active level	R/W
b2	TOC	TRCIOC output level select bit (1, 2)		R/W
b3	TOD	TRCIOD output level select bit (1, 2)		R/W
b4	TCK0	Count source select bit (1)	b6 b5 b4 0 0 0: f1 0 0 1: f2 0 1 0: f4 0 1 1: f8 1 0 0: f32 1 0 1: TRCCLK input rising edge 1 1 0: fOCO40M 1 1 1: fOCO-F (3)	R/W
b5	TCK1			R/W
b6	TCK2			R/W
b7	CCLR	TRC counter clear select bit	0: Disable clear (free-running operation) 1: Clear by compare match in the TRCGRA register	R/W

Notes:
1. Set to these bits when the TSTART bit in the TRCMR register is set to 0 (count stops).
2. If the pin function is set for waveform output (refer to **7.5 Port Settings**), the initial output level is output when the TRCCR1 register is set.
3. To select fOCO-F, set it to the clock frequency higher than the CPU clock frequency.

19.6.2 Timer RC Control Register 2 (TRCCR2) in PWM Mode

Address 0130h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TCEG1	TCEG0	CSEL	—	—	POLD	POLC	POLB
After Reset	0	0	0	1	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	POLB	PWM mode output level control bit B (1)	0: TRCIOB output level selected as “L” active 1: TRCIOB output level selected as “H” active	R/W
b1	POLC	PWM mode output level control bit C (1)	0: TRCIOC output level selected as “L” active 1: TRCIOC output level selected as “H” active	R/W
b2	POLD	PWM mode output level control bit D (1)	0: TRCIOD output level selected as “L” active 1: TRCIOD output level selected as “H” active	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b4	—			
b5	CSEL	TRC count operation select bit (2)	0: Count continues at compare match with the TRCGRA register 1: Count stops at compare match with the TRCGRA register	R/W
b6	TCEG0	TRCTRG input edge select bit (3)	b7 b6 0 0: Disable the trigger input from the TRCTRG pin 0 1: Rising edge selected 1 0: Falling edge selected 1 1: Both edges selected	R/W
b7	TCEG1			R/W

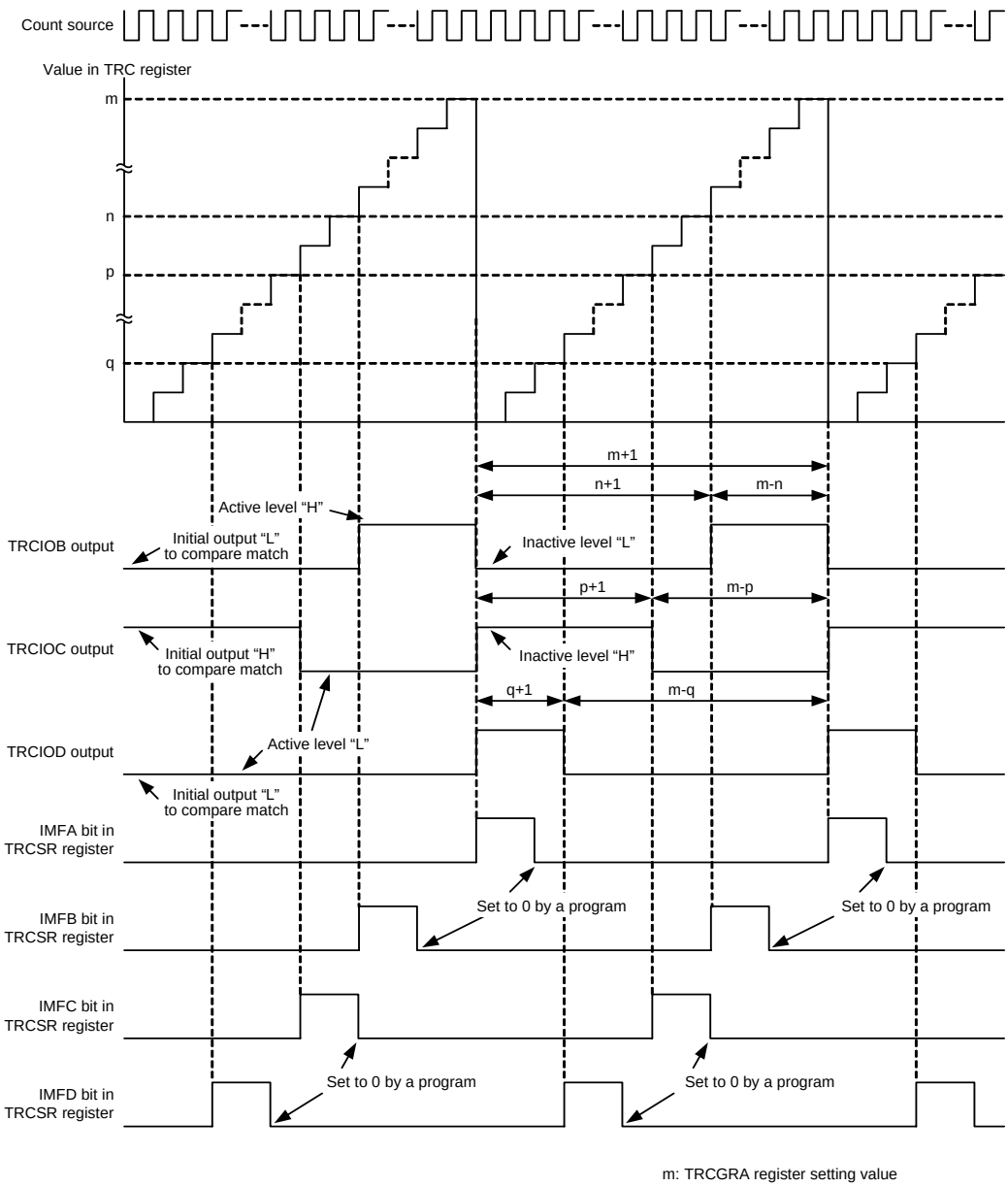
Notes:
1. Enabled when in PWM mode.
2. Enabled when in output compare function, PWM mode, or PWM2 mode. For notes on PWM2 mode, refer to **19.9.6 TRCMR Register in PWM2 Mode**.
3. In timer mode and PWM mode these bits are disabled.

Table 19.12 Functions of TRCGRh Register in PWM Mode

Register	Setting	Register Function	PWM Output Pin
TRCGRA	—	General register. Set the PWM period.	—
TRCGRB	—	General register. Set the PWM output change point.	TRCIOB
TRCGRC	BFC = 0	General register. Set the PWM output change point.	TRCIOC
TRCGRD	BFD = 0		TRCIOD
TRCGRC	BFC = 1	Buffer register. Set the next PWM period. (Refer to **19.3.2 Buffer Operation**.)	—
TRCGRD	BFD = 1	Buffer register. Set the next PWM output change point. (Refer to **19.3.2 Buffer Operation**.)	TRCIOB

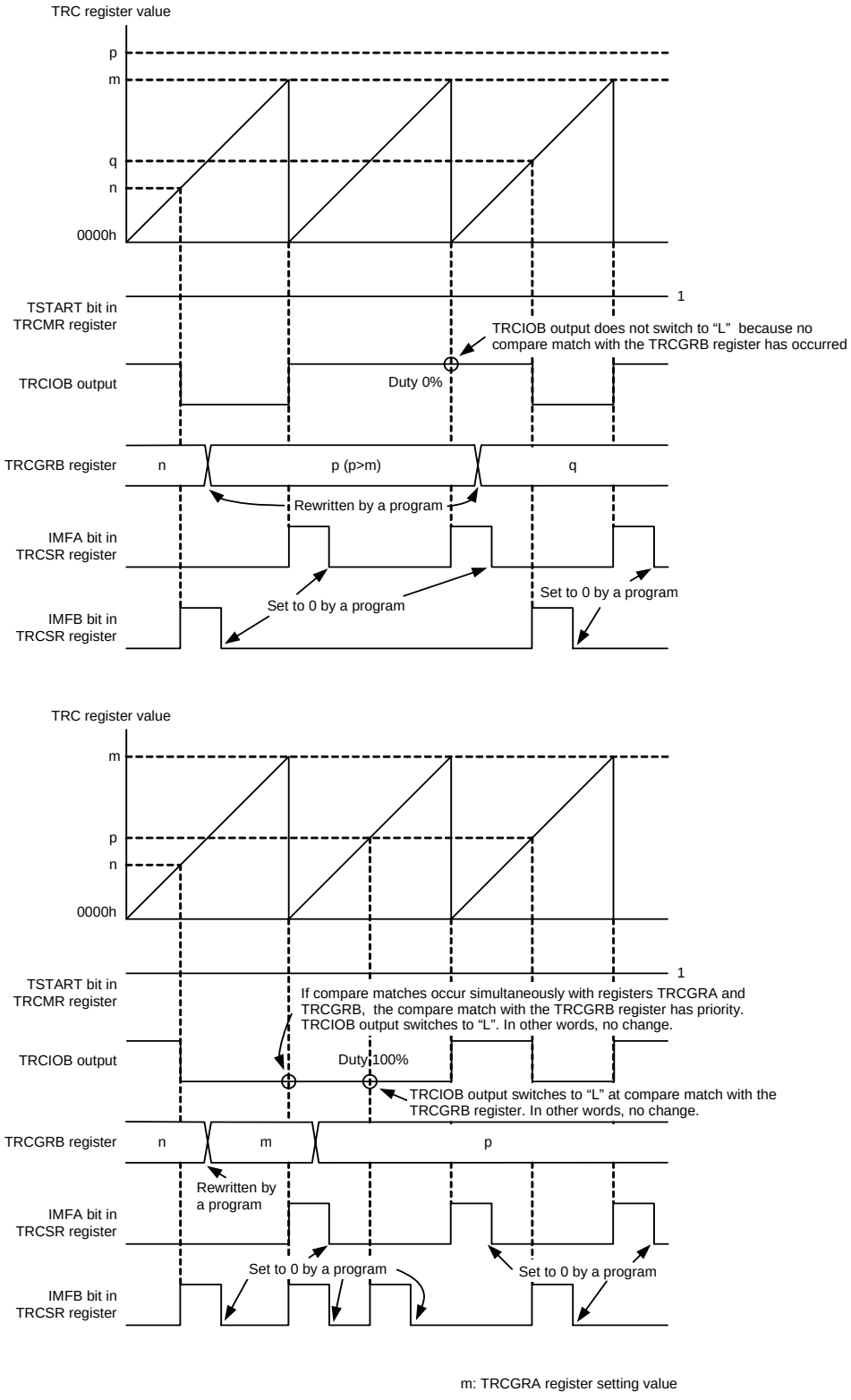
h = A, B, C, or D
BFC, BFD: Bits in TRCMR register
Note:
1. The output level does not change even when a compare match occurs if the TRCGRA register value (PWM period) is the same as the TRCGRB, TRCGRC, or TRCGRD register value.

19.6.3 Operating Example



The above applies under the following conditions:
- Bits BFC and BFD in the TRCMR register are set to 0 (registers TRCGRC and TRCGRD do not operate as buffers).
- Bits EB, EC, and ED in the TRCOER register are set to 0 (output from TRCIOB, TRCIOC, and TRCIOD enabled).
- Bits TOB and TOC in the TRCCR1 register are set to 0 (inactive level), the TOD bit is set to 1 (active level).
- The POLB bit in the TRCCR2 register is set to 1 ("H" active), bits POLC and POLD are set to 0 ("L" active).

Figure 19.14 Operating Example of PWM Mode

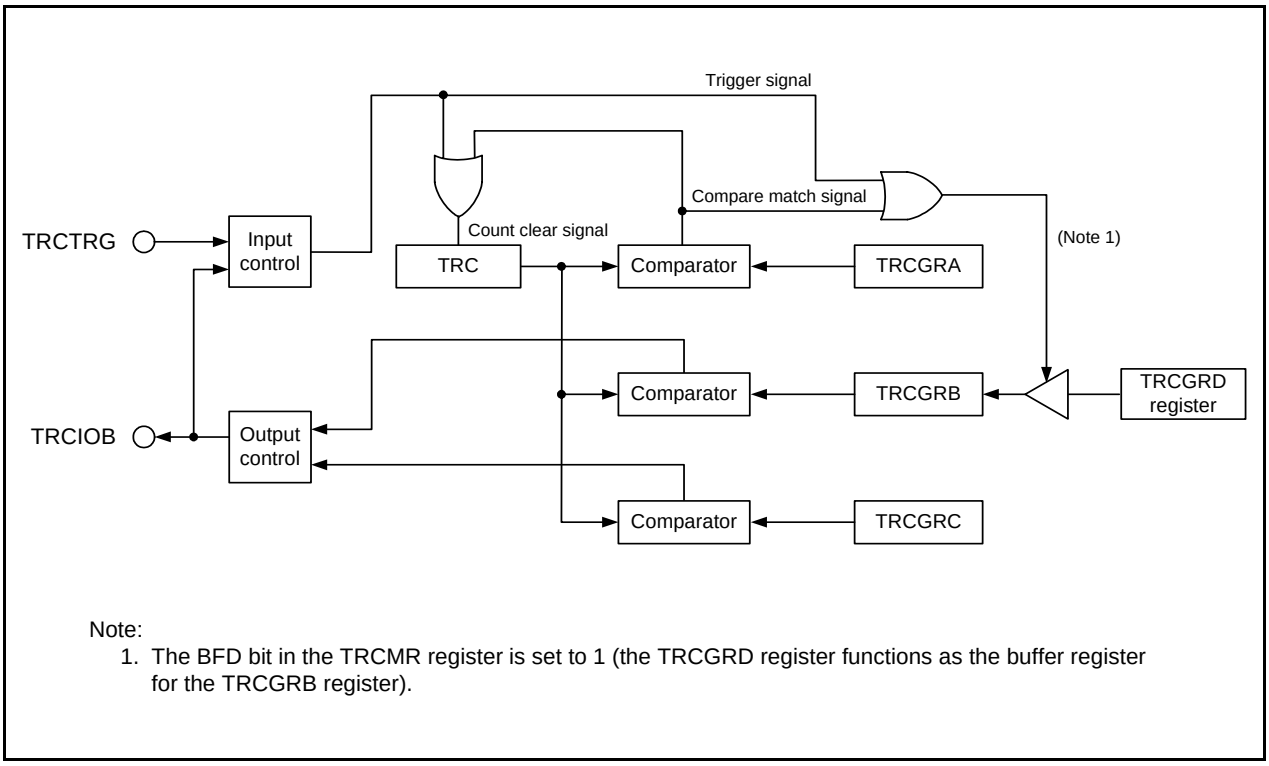


The above applies under the following conditions:
- The EB bit in the TRCOER register is set to 0 (output from TRCIOB enabled).
- The POLB bit in the TRCCR2 register is set to 0 ("L" active).

Figure 19.15 Operating Example of PWM Mode (Duty 0% and Duty 100%)

19.7 PWM2 Mode

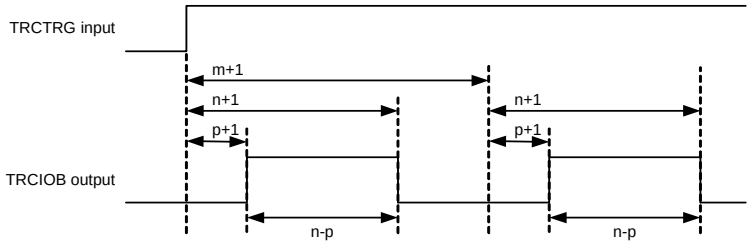
This mode outputs a single PWM waveform. After a given wait duration has elapsed following the trigger, the pin output switches to active level. Then, after a given duration, the output switches back to inactive level. Furthermore, the counter stops at the same time the output returns to inactive level, making it possible to use PWM2 mode to output a programmable wait one-shot waveform.
Since timer RC uses multiple general registers in PWM2 mode, other modes cannot be used in conjunction with it. Figure 19.16 shows a PWM2 Mode Block Diagram, Table 19.13 lists the Specifications of PWM2 Mode, Table 19.14 lists the Functions of TRCGRj Register in PWM2 Mode, and Figures 19.17 to 19.19 show Operating Examples of PWM2 Mode.



Note:
1. The BFD bit in the TRCMR register is set to 1 (the TRCGRD register functions as the buffer register for the TRCGRB register).

Figure 19.16 PWM2 Mode Block Diagram

Table 19.13 Specifications of PWM2 Mode

Item	Specification
Count source	f1, f2, f4, f8, f32, fOCO40M, fOCO-F, or external signal (rising edge) input to TRCCLK pin
Count operation	Increment TRC register
PWM waveform	PWM period: 1/fk × (m+1) (no TRCTRG input) Active level width: 1/fk × (n-p) Wait time from count start or trigger: 1/fk × (p+1) fk: Count source frequency m: TRCGRA register setting value, n: TRCGRB register setting value p: TRCGRC register setting value  (TRCTRG: Rising edge, active level is “H”)
Count start conditions	• Bits TCEG1 to TCEG0 in the TRCCR2 register are set to 00b (TRCTRG trigger disabled) or the CSEL bit in the TRCCR2 register is set to 0 (count continues). 1 (count starts) is written to the TSTART bit in the TRCMR register. • Bits TCEG1 to TCEG0 in the TRCCR2 register are set to 01b, 10b, or 11b (TRCTRG trigger enabled) and the TSTART bit in the TRCMR register is set to 1 (count starts). A trigger is input to the TRCTRG pin
Count stop conditions	• 0 (count stops) is written to the TSTART bit in the TRCMR register while the CSEL bit in the TRCCR2 register is set to 0 or 1. The TRCIOB pin outputs the initial level in accordance with the value of the TOB bit in the TRCCR1 register. The TRC register retains the value before count stops. • The count stops due to a compare match with TRCGRA while the CSEL bit in the TRCCR2 register is set to 1. The TRCIOB pin outputs the initial level. The TRC register retains the value before count stops if the CCLR bit in the TRCCR1 register is set to 0. The TRC register is set to 0000h if the CCLR bit in the TRCCR1 register is set to 1.
Interrupt request generation timing	• Compare match (contents of TRC and TRCGRj registers match) • The TRC register overflows
TRCIOA/TRCTRG pin function	Programmable I/O port or TRCTRG input
TRCIOB pin function	PWM output
TRCIOC and TRCIOD pin functions	Programmable I/O port
$\overline{\text{INT0}}$ pin function	Programmable I/O port, pulse output forced cutoff signal input, or $\overline{\text{INT0}}$ interrupt input
Read from timer	The count value can be read by reading the TRC register.
Write to timer	The TRC register can be written to.
Select functions	• External trigger and valid edge selection The edge or edges of the signal input to the TRCTRG pin can be used as the PWM output trigger: rising edge, falling edge, or both rising and falling edges • Buffer operation (Refer to **19.3.2 Buffer Operation**.) • Pulse output forced cutoff signal input (Refer to **19.3.4 Forced Cutoff of Pulse Output**.) • Digital filter (Refer to **19.3.3 Digital Filter**.) • SCU trigger generation

j = A, B, or C

19.7.1 Timer RC Control Register 1 (TRCCR1) in PWM2 Mode

Address 0121h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CCLR	TCK2	TCK1	TCK0	TOD	TOC	TOB	TOA
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TOA	TRCIOA output level select bit (1)	Disabled in PWM2 mode	R/W
b1	TOB	TRCIOB output level select bit (1, 2)	0: Active level “H” (Initial output “L” “H” output by compare match in the TRCGRC register “L” output by compare match in the TRCGRB register) 1: Active level “L” (Initial output “H” “L” output by compare match in the TRCGRC register “H” output by compare match in the TRCGRB register)	R/W
b2	TOC	TRCIOC output level select bit (1)	Disabled in PWM2 mode	R/W
b3	TOD	TRCIOD output level select bit (1)		R/W
b4	TCK0	Count source select bit (1)	b6 b5 b4 0 0 0: f1 0 0 1: f2 0 1 0: f4 0 1 1: f8 1 0 0: f32 1 0 1: TRCCLK input rising edge 1 1 0: fOCO40M 1 1 1: fOCO-F (3)	R/W
b5	TCK1			R/W
b6	TCK2			R/W
b7	CCLR	TRC counter clear select bit	0: Disable clear (free-running operation) 1: Clear by compare match in the TRCGRA register	R/W

Notes:
1. Set to these bits when the TSTART bit in the TRCMR register is set to 0 (count stops).
2. If the pin function is set for waveform output (refer to **7.5 Port Settings**), the initial output level is output when the TRCCR1 register is set.
3. To select fOCO-F, set it to the clock frequency higher than the CPU clock frequency.

19.7.2 Timer RC Control Register 2 (TRCCR2) in PWM2 Mode

Address 0130h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TCEG1	TCEG0	CSEL	—	—	POLD	POLC	POLB
After Reset	0	0	0	1	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	POLB	PWM mode output level control bit B (1)	0: TRCIOB output level selected as “L” active 1: TRCIOB output level selected as “H” active	R/W
b1	POLC	PWM mode output level control bit C (1)	0: TRCIOC output level selected as “L” active 1: TRCIOC output level selected as “H” active	R/W
b2	POLD	PWM mode output level control bit D (1)	0: TRCIOD output level selected as “L” active 1: TRCIOD output level selected as “H” active	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b4	—			
b5	CSEL	TRC count operation select bit (2)	0: Count continues at compare match with the TRCGRA register 1: Count stops at compare match with the TRCGRA register	R/W
b6	TCEG0	TRCTRG input edge select bit (3)	b7 b6 0 0: Disable the trigger input from the TRCTRG pin 0 1: Rising edge selected 1 0: Falling edge selected 1 1: Both edges selected	R/W
b7	TCEG1			R/W

Notes:
1. Enabled when in PWM mode.
2. Enabled when in output compare function, PWM mode, or PWM2 mode. For notes on PWM2 mode, refer to **19.9.6 TRCMR Register in PWM2 Mode**.
3. Enabled when in PWM2 mode.

19.7.3 Timer RC Digital Filter Function Select Register (TRCDF) in PWM2 Mode

Address 0131h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	DFCK1	DFCK0	—	DFTRG	DFD	DFC	DFB	DFA
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	DFA	TRCIOA pin digital filter function select bit (1)	0: Function is not used 1: Function is used	R/W
b1	DFB	TRCIOB pin digital filter function select bit (1)		R/W
b2	DFC	TRCIOC pin digital filter function select bit (1)		R/W
b3	DFD	TRCIOD pin digital filter function select bit (1)		R/W
b4	DFTRG	TRCTRG pin digital filter function select bit (2)		R/W
b5	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b6	DFCK0	Clock select bits for digital filter function (1, 2)	b7 b6 0 0: f32 0 1: f8 1 0: f1 1 1: Count source (clock selected by bits TCK2 to TCK0 in the TRCCR1 register)	R/W
b7	DFCK1			R/W

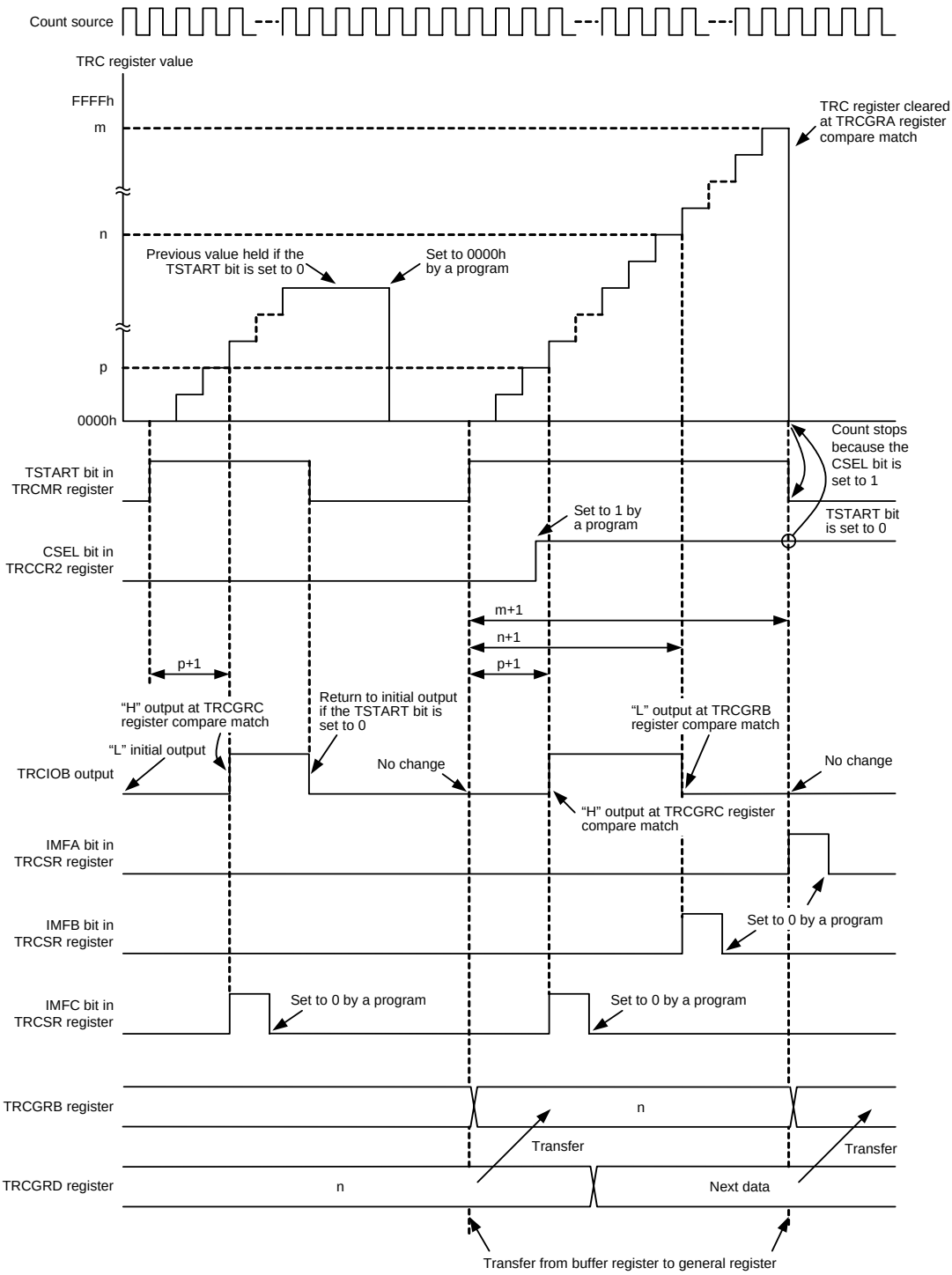
Notes:
1. These bits are enabled for the input capture function.
2. These bits are enabled when in PWM2 mode and bits TCEG1 to TCEG0 in the TRCCR2 register are set to 01b, 10b, or 11b (TRCTRG trigger input enabled).

Table 19.14 Functions of TRCGRj Register in PWM2 Mode

Register	Setting	Register Function	PWM2 Output Pin
TRCGRA	—	General register. Set the PWM period.	TRCIOB pin
TRCGRB (1)	—	General register. Set the PWM output change point.	
TRCGRC (1)	BFC = 0	General register. Set the PWM output change point (wait time after trigger).	
TRCGRD	BFD = 0	(Not used in PWM2 mode)	—
TRCGRD	BFD = 1	Buffer register. Set the next PWM output change point. (Refer to **19.3.2 Buffer Operation**.)	TRCIOB pin

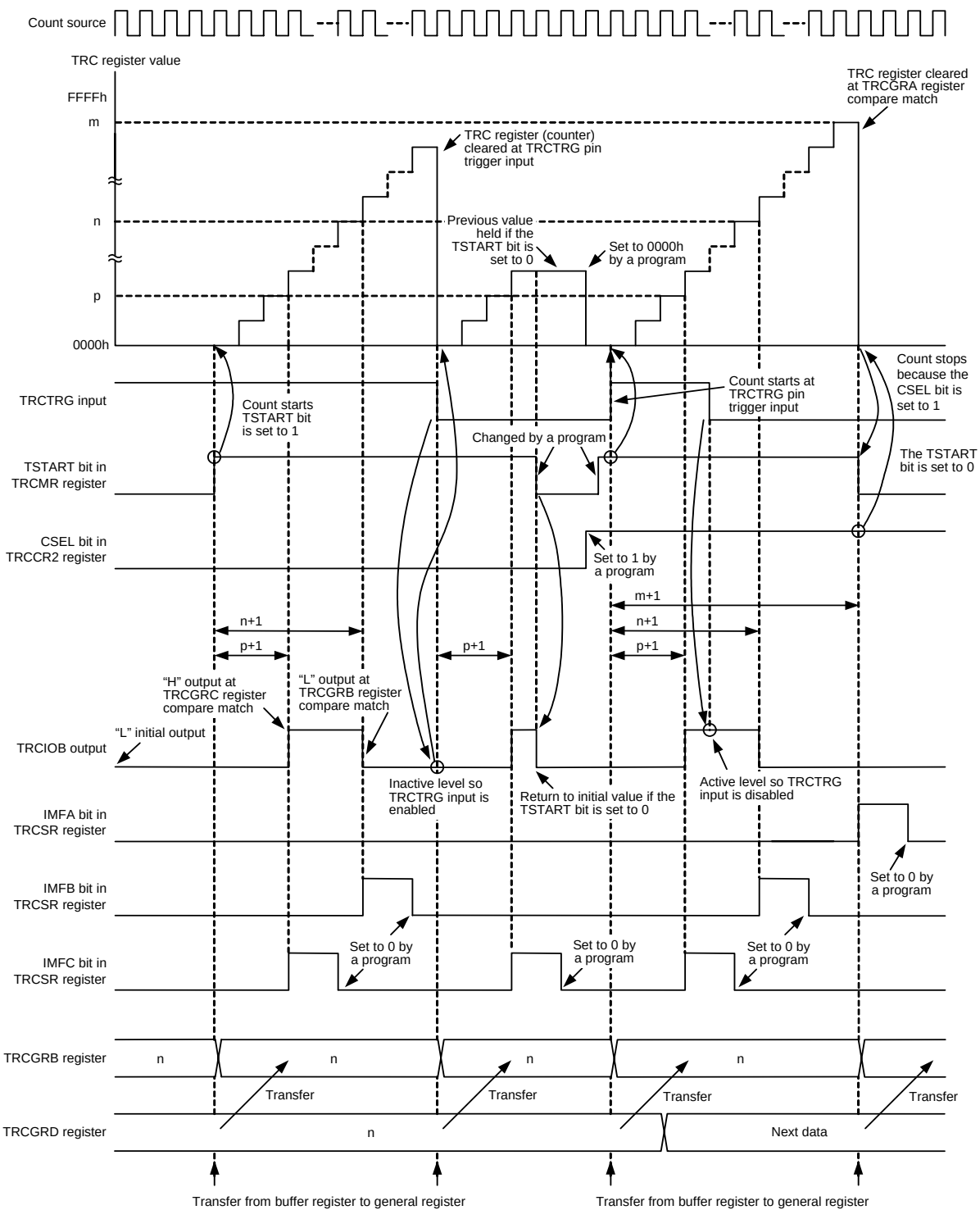
j = A, B, C, or D
BFC, BFD: Bits in TRCMR register
Note:
1. Do not set the TRCGRB and TRCGRC registers to the same value.

19.7.4 Operating Example



The above applies under the following conditions:
- The TOB bit in the TRCCR1 register is set to 0 (initial level is "L", "H" output at compare match with the TRCGRC register, "L" output at compare match with the TRCGRB register).
- Bits TCEG1 and TCEG0 in the TRCCR2 register are set to 00b (TRCTRG trigger input disabled).

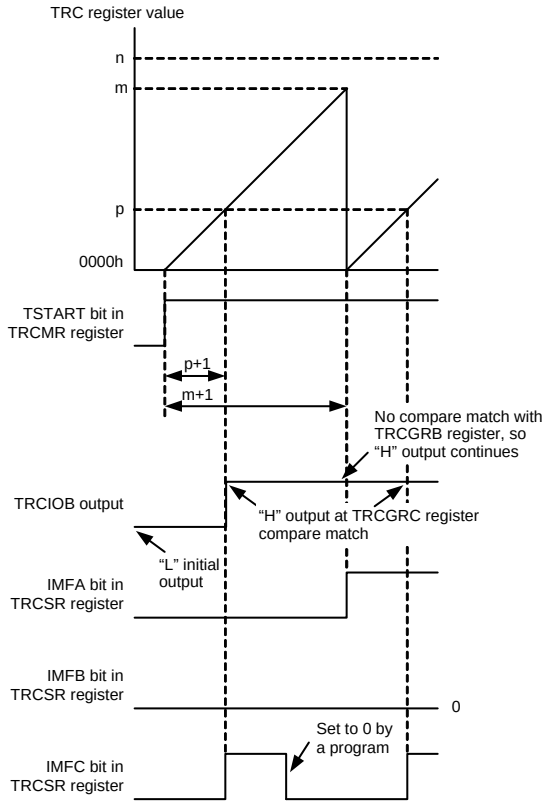
Figure 19.17 Operating Example of PWM2 Mode (TRCTRG Trigger Input Disabled)



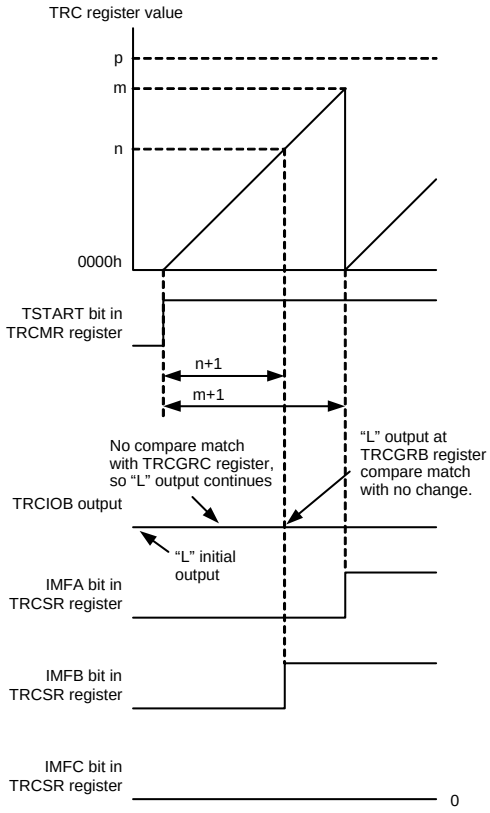
The above applies under the following conditions:
- The TOB bit in the TRCCR1 register is set to 0 (initial level is "L", "H" output at compare match with the TRCGRC register, "L" output at compare match with the TRCGRB register).
- Bits TCEG1 and TCEG0 in the TRCCR2 register are set to 11b (trigger at both rising and falling edges of TRCTRG input).

Figure 19.18 Operating Example of PWM2 Mode (TRCTRG Trigger Input Enabled)

• TRCGRB register setting value greater than TRCGRA register setting value



• TRCGRC register setting value greater than TRCGRA register setting value



m: TRCGRA register setting value
n: TRCGRB register setting value
p: TRCGRC register setting value

The above applies under the following conditions:
- The TOB bit in the TRCCR1 register is set to 0 (initial level is "L", "H" output at compare match with the TRCGRC register, "L" output at compare match with the TRCGRB register).
- Bits TCEG1 and TCEG0 in the TRCCR2 register are set to 00b (TRCTRG trigger input disabled).

Figure 19.19 Operating Example of PWM2 Mode (Duty 0% and Duty 100%)

19.8 Timer RC Interrupt

Timer RC generates a timer RC interrupt request from five sources. The timer RC interrupt uses the single TRCIC register (bits IR and ILVL0 to ILVL2) and a single vector.
Table 19.15 lists the Registers Associated with Timer RC Interrupt, and Figure 19.20 shows a Timer RC Interrupt Block Diagram.

Table 19.15 Registers Associated with Timer RC Interrupt

Timer RC Status Register	Timer RC Interrupt Enable Register	Timer RC Interrupt Control Register
TRCSR	TRCIER	TRCIC

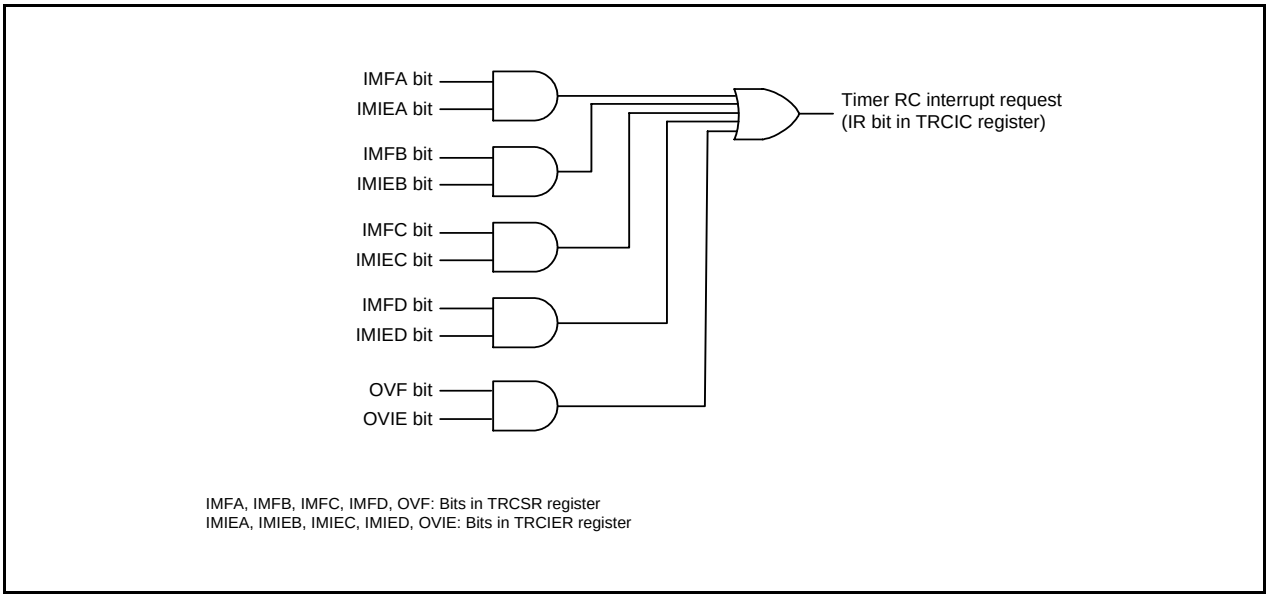


Figure 19.20 Timer RC Interrupt Block Diagram

Like other maskable interrupts, the timer RC interrupt is controlled by the combination of the I flag, IR bit, bits ILVL0 to ILVL2, and IPL. However, it differs from other maskable interrupts in the following respects because a single interrupt source (timer RC interrupt) is generated from multiple interrupt request sources.

- The IR bit in the TRCIC register is set to 1 (interrupt requested) when a bit in the TRCSR register is set to 1 and the corresponding bit in the TRCIER register is also set to 1 (interrupt enabled).
- The IR bit is set to 0 (no interrupt requested) when the bit in the TRCSR register or the corresponding bit in the TRCIER register is set to 0, or both are set to 0. In other words, the interrupt request is not maintained if the IR bit is once set to 1 but the interrupt is not acknowledged.
- If another interrupt source is triggered after the IR bit is set to 1, the IR bit remains set to 1 and does not change.
- If multiple bits in the TRCIER register are set to 1, use the TRCSR register to determine the source of the interrupt request.
- The bits in the TRCSR register are not automatically set to 0 when an interrupt is acknowledged. Set them to 0 within the interrupt routine. Refer to **19.2.5 Timer RC Status Register (TRCSR)**, for the procedure for setting these bits to 0.

Refer to **19.2.4 Timer RC Interrupt Enable Register (TRCIER)**, for details of the TRCIER register.
Refer to **11.3 Interrupt Control**, for details of the TRCIC register and **11.1.5.2 Relocatable Vector Tables**, for information on interrupt vectors.

19.9 Notes on Timer RC

19.9.1 TRC Register

- The following note applies when the CCLR bit in the TRCCR1 register is set to 1 (clear TRC register at compare match with TRCGRA register).
  When using a program to write a value to the TRC register while the TSTART bit in the TRCMR register is set to 1 (count starts), ensure that the write does not overlap with the timing with which the TRC register is set to 0000h.
  If the timing of the write to the TRC register and the setting of the TRC register to 0000h coincide, the write value will not be written to the TRC register and the TRC register will be set to 0000h.

- Reading from the TRC register immediately after writing to it can result in the value previous to the write being read out. To prevent this, execute the JMP.B instruction between the read and the write instructions.

```
Program Example     MOV.W   #XXXXh, TRC    ; Write
                    JMP.B   L1             ; JMP.B instruction
                L1: MOV.W   TRC, DATA      ; Read
```

19.9.2 TRCSR Register

Reading from the TRCSR register immediately after writing to it can result in the value previous to the write being read out. To prevent this, execute the JMP.B instruction between the read and the write instructions.

```
Program Example     MOV.B   #XXh, TRCSR    ; Write
                    JMP.B   L1             ; JMP.B instruction
                L1: MOV.B   TRCSR, DATA    ; Read
```

19.9.3 TRCCR1 Register

To set bits TCK2 to TCK0 in the TRCCR1 register to 111b (fOCO-F), set fOCO-F to the clock frequency higher than the CPU clock frequency.

19.9.4 Count Source Switching

- Stop the count before switching the count source.

Switching procedure
(1) Set the TSTART bit in the TRCMR register to 0 (count stops).
(2) Change the settings of bits TCK2 to TCK0 in the TRCCR1 register.

- After switching the count source from fOCO40M to another clock, allow a minimum of two cycles of f1 to elapse after changing the clock setting before stopping fOCO40M.

Switching procedure
(1) Set the TSTART bit in the TRCMR register to 0 (count stops).
(2) Change the settings of bits TCK2 to TCK0 in the TRCCR1 register.
(3) Wait for a minimum of two cycles of f1.
(4) Set the FRA00 bit in the FRA0 register to 0 (high-speed on-chip oscillator off).

• After switching the count source from fOCO-F to fOCO40M, allow a minimum of two cycles of fOCO-F to elapse after changing the clock setting before stopping fOCO-F.

Switching procedure

(1) Set the TSTART bit in the TRCMR register to 0 (count stops).
(2) Change the settings of bits TCK2 to TCK0 in the TRCCR1 register.
(3) Wait for a minimum of two cycles of fOCO-F.
(4) Set the FRA00 bit in the FRA0 register to 0 (high-speed on-chip oscillator off).

• After switching the count source from fOCO-F to a clock other than fOCO40M, allow a minimum of one cycle of fOCO-F + fOCO40M to elapse after changing the clock setting before stopping fOCO-F.

Switching procedure

(1) Set the TSTART bit in the TRCMR register to 0 (count stops).
(2) Change the settings of bits TCK2 to TCK0 in the TRCCR1 register.
(3) Wait for a minimum of one cycle of fOCO-F + fOCO40M.
(4) Set the FRA00 bit in the FRA0 register to 0 (high-speed on-chip oscillator off).

19.9.5 Input Capture Function

• Set the pulse width of the input capture signal as follows:
[When the digital filter is not used]
Three or more cycles of the timer RC operation clock (refer to **Table 19.1 Timer RC Operation Clock**)
[When the digital filter is used]
Five cycles of the digital filter sampling clock + three cycles of the timer RC operating clock, minimum (refer to **Figure 19.5 Digital Filter Block Diagram**)
• The value of the TRC register is transferred to the TRCGRj register one or two cycles of the timer RC operation clock after the input capture signal is input to the TRCIOj (j = A, B, C, or D) pin (when the digital filter function is not used).
• When the input capture function is used, if an edge selected by bits IOj0 and IOj1 (j = A, B, C, or D) in the TRCIOR0 or TRCIOR1 register is input to the TRCIOj pin, the IMFj bit in the TRCSR register is set to 1 even when the TSTART bit in the TRCMR register is 0 (count stops).

19.9.6 TRCMR Register in PWM2 Mode

When the CSEL bit in the TRCCR2 register is set to 1 (count stops at compare match with the TRCGRA register), do not set the TRCMR register at compare match timing of registers TRC and TRCGRA.

19.9.7 Count Source fOCO40M

The count source fOCO40M can be used with supply voltage VCC = 2.7 V to 5.5 V. For supply voltage other than that, do not set bits TCK2 to TCK0 in the TRCCR1 register to 110b (select fOCO40M as the count source).

20. Serial Interface (UART0)

The serial interface consists of one channel UART0. This chapter describes the UART0.

20.1 Overview

UART0 has a dedicated timer to generate a transfer clock. UART0 supports clock synchronous serial I/O mode and clock asynchronous serial I/O mode (UART mode).
Figure 20.1 shows a UART0 Block Diagram. Figure 20.2 shows a Block Diagram of UART0 Transmit/Receive Unit. Table 20.1 lists the Pin Configuration of UART0.

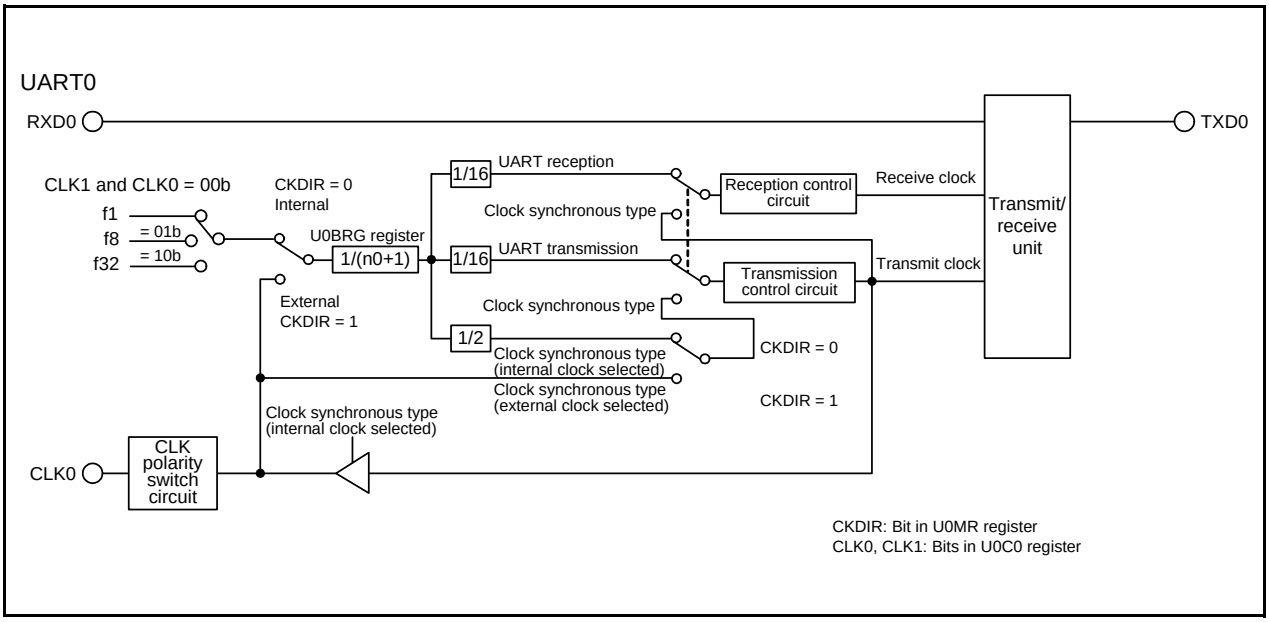


Figure 20.1 UART0 Block Diagram

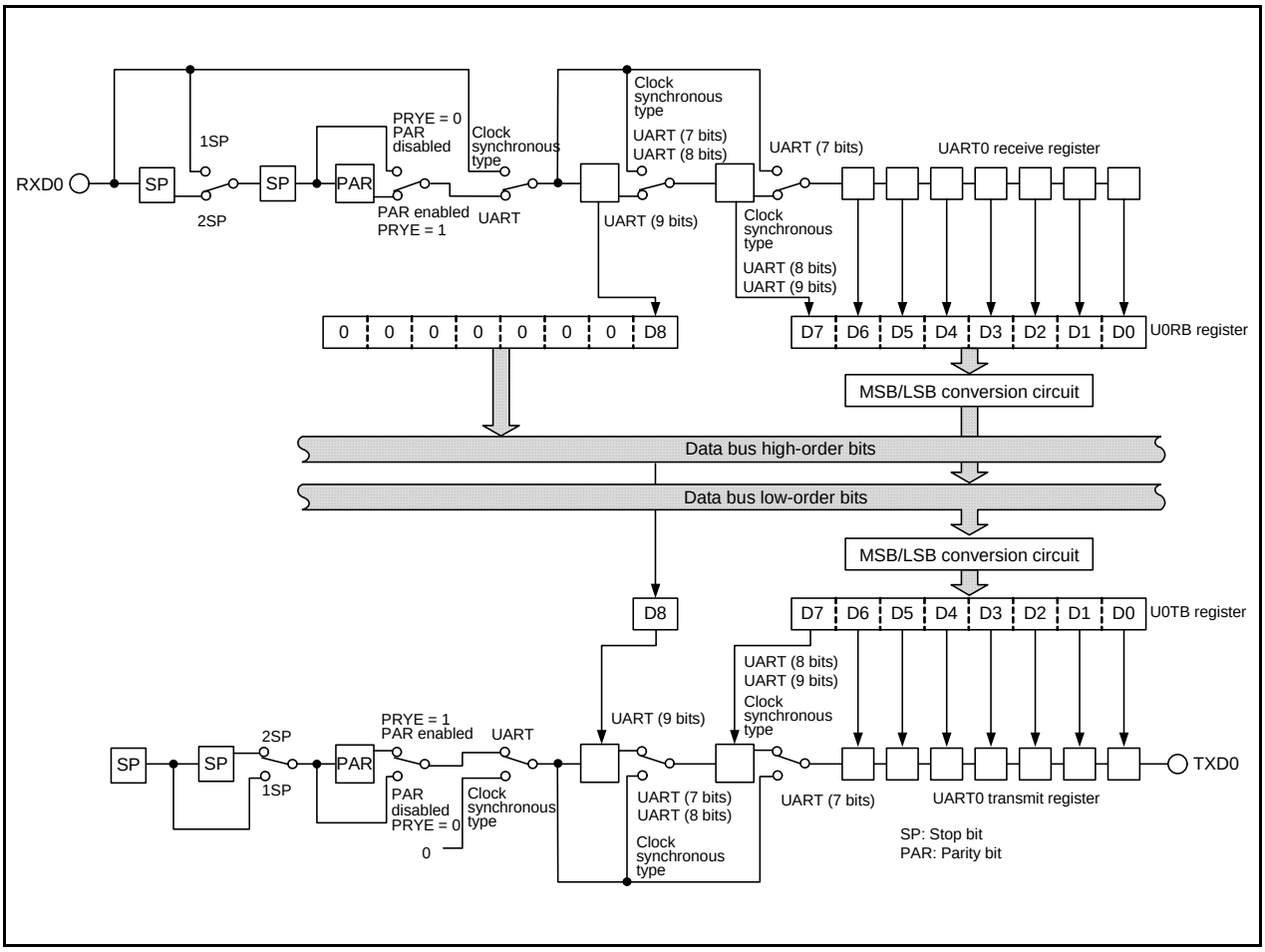


Figure 20.2 Block Diagram of UART0 Transmit/Receive Unit

Table 20.1 Pin Configuration of UART0

Pin Name	Assigned Pin	I/O	Function
TXD0	P1_4 or P3_4	Output	Serial data output
RXD0	P1_5 or P3_5	Input	Serial data input
CLK0	P1_6 or P3_7	I/O	Transfer clock I/O

20.2 Registers

20.2.1 UART0 Transmit/Receive Mode Register (U0MR)

Address 00A0h (U0MR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	PRYE	PRY	STPS	CKDIR	SMD2	SMD1	SMD0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	SMD0	Serial I/O mode select bit	b2 b1 b0 0 0 0: Serial interface disabled 0 0 1: Clock synchronous serial I/O mode 1 0 0: UART mode, transfer data 7 bits long 1 0 1: UART mode, transfer data 8 bits long 1 1 0: UART mode, transfer data 9 bits long Other than above: Do not set.	R/W
b1	SMD1			R/W
b2	SMD2			R/W
b3	CKDIR	Internal/external clock select bit	0: Internal clock 1: External clock	R/W
b4	STPS	Stop bit length select bit	0: One stop bit 1: Two stop bits	R/W
b5	PRY	Odd/even parity select bit	Enabled when PRYE = 1 0: Odd parity 1: Even parity	R/W
b6	PRYE	Parity enable bit	0: Parity disabled 1: Parity enabled	R/W
b7	—	Reserved bit	Set to 0.	R/W

20.2.2 UART0 Bit Rate Register (U0BRG)

Address 00A1h (U0BRG)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	Function	Setting Range	R/W
b7 to b0	If the setting value is n, U0BRG divides the count source by n+1.	00h to FFh	W

Write to the U0BRG register while transmission and reception stop.
Use the MOV instruction to write to this register.
Set bits CLK0 and CLK1 in the U0C0 register before writing to the U0BRG register.

20.2.3 UART0 Transmit Buffer Register (U0TB)

Address 00A3h to 00A2h (U0TB)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	Symbol	Function	R/W
b0	—	Transmit data	W
b1	—		
b2	—		
b3	—		
b4	—		
b5	—		
b6	—		
b7	—		
b8	—		
b9	—	Nothing is assigned. If necessary, set to 0. When read, the content is undefined.	—
b10	—		
b11	—		
b12	—		
b13	—		
b14	—		
b15	—		

If the transfer data is 9 bits long, write data to the high-order byte first, then low-order byte of the U0TB register.
Use the MOV instruction to write to this register.

20.2.4 UART0 Transmit/Receive Control Register 0 (U0C0)

Address 00A4h (U0C0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	UFORM	CKPOL	NCH	—	TXEPT	—	CLK1	CLK0
After Reset	0	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CLK0	BRG count source select bit (1)	b1 b0 0 0: f1 selected 0 1: f8 selected 1 0: f32 selected 1 1: Do not set.	R/W
b1	CLK1			R/W
b2	—	Reserved bit	Set to 0.	R/W
b3	TXEPT	Transmit register empty flag	0: Data present in the transmit register (transmission in progress) 1: No data in the transmit register (transmission completed)	R
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b5	NCH	Data output select bit	0: TXD0 pin set to CMOS output 1: TXD0 pin set to N-channel open-drain output	R/W
b6	CKPOL	CLK polarity select bit	0: Transmit data output at the falling edge and receive data input at the rising edge of the transfer clock 1: Transmit data output at the rising edge and receive data input at the falling edge of the transfer clock	R/W
b7	UFORM	Transfer format select bit	0: LSB first 1: MSB first	R/W

Note:
1. If the BRG count source is switched, set the U0BRG register again.

20.2.5 UART0 Transmit/Receive Control Register 1 (U0C1)

Address 00A5h (U0C1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	U0RRM	U0IRS	RI	RE	TI	TE
After Reset	0	0	0	0	0	0	1	0

Bit	Symbol	Bit Name	Function	R/W
b0	TE	Transmit enable bit	0: Transmission disabled 1: Transmission enabled	R/W
b1	TI	Transmit buffer empty flag	0: Data present in the U0TB register 1: No data in the U0TB register	R
b2	RE	Receive enable bit	0: Reception disabled 1: Reception enabled	R/W
b3	RI	Receive complete flag (1)	0: No data in the U0RB register 1: Data present in the U0RB register	R
b4	U0IRS	UART0 transmit interrupt source select bit	0: Transmission buffer empty (TI = 1) 1: Transmission completed (TXEPT = 1)	R/W
b5	U0RRM	UART0 continuous receive mode enable bit (2)	0: Continuous receive mode disabled 1: Continuous receive mode enabled	R/W
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b7	—			

Notes:
1. The RI bit is set to 0 when the higher byte of the U0RB register is read.
2. In UART mode, set the U0RRM bit to 0 (continuous receive mode disabled).

20.2.6 UART0 Receive Buffer Register (U0RB)

Address 00A7h to 00A6h (U0RB)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	SUM	PER	FER	OER	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	Symbol	Bit Name	Function	R/W
b0	—	—	Receive data (D7 to D0)	R
b1	—			
b2	—			
b3	—			
b4	—			
b5	—			
b6	—			
b7	—			
b8	—	—	Receive data (D8)	R
b9	—	Nothing is assigned. If necessary, set to 0. When read, the content is undefined.		—
b10	—			
b11	—			
b12	OER	Overrun error flag (1)	0: No overrun error 1: Overrun error	R
b13	FER	Framing error flag (1, 2)	0: No framing error 1: Framing error	R
b14	PER	Parity error flag (1, 2)	0: No parity error 1: Parity error	R
b15	SUM	Error sum flag (1, 2)	0: No error 1: Error	R

Notes:

1. Bits SUM, PER, FER, and OER are set to 0 (no error) when either of the following is set:
   • Bits SMD2 to SMD0 in the U0MR register are set to 000b (serial interface disabled), or
   • The RE bit in the U0C1 register is set to 0 (reception disabled)
   The SUM bit is set to 0 (no error) when all of bits PER, FER, and OER are set to 0 (no error).
   Bits PER and FER are also set to 0 when the high-order byte of the U0RB register is read.
   When setting bits SMD2 to SMD0 in the U0MR register to 000b, set the TE bit in the U0C1 register to 0 (transmission disabled) and the RE bit to 0 (reception disabled).
2. These error flags are invalid when bits SMD2 to SMD0 in the U0MR register are set to 001b (clock synchronous serial I/O mode). When read, the content is undefined.

Always read the U0RB register in 16-bit units.

20.2.7 UART0 Pin Select Register (U0SR)

Address 0188h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	CLK0SEL1	CLK0SEL0	RXD0SEL1	RXD0SEL0	TXD0SEL1	TXD0SEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TXD0SEL0	TXD0 pin select bit	b1 b0 0 0: TXD0 pin not used 0 1: P1_4 assigned 1 0: P3_4 assigned 1 1: Do not set. (TXD0 pin not used.)	R/W
b1	TXD0SEL1			R/W
b2	RXD0SEL0	RXD0 pin select bit	b3 b2 0 0: RXD0 pin not used 0 1: P1_5 assigned 1 0: P3_5 assigned 1 1: Do not set. (RXD0 pin not used.)	R/W
b3	RXD0SEL1			R/W
b4	CLK0SEL0	CLK0 pin select bit	b5 b4 0 0: CLK0 pin not used 0 1: P1_6 assigned 1 0: P3_7 assigned 1 1: Do not set. (CLK0 pin not used.)	R/W
b5	CLK0SEL1			R/W
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b7	—			—

The U0SR register selects which pin is assigned to the UART0 I/O. To use the I/O pin for UART0, set this register.
Set the U0SR register before setting the UART0 associated registers. Also, do not change the setting value in this register during UART0 operation.
Change the U0SR register from the initial value to any value during the initial setting of the user's program. Do not change this register again while the main program is executed.

20.2.8 Low-Voltage Signal Mode Control Register (TSMR)

Address 0190h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	I3LVM	I2LVM	I1LVM	I0LVM	—	—	U0LVM	LVMPR
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	LVMPR	Low-voltage signal mode protect bit	0: Write disabled 1: Write enabled (1)	R/W
b1	U0LVM	UART0 low-voltage signal mode control bit (1)	0: Low-voltage signal mode disabled 1: Low-voltage signal mode enabled (2)	R/W
b2	—	Reserved bits	Set to 0.	R/W
b3	—			R/W
b4	I0LVM	$\overline{\text{INT0}}$ low-voltage signal mode control bit (1)	0: Low-voltage signal mode disabled 1: Low-voltage signal mode enabled	R/W
b5	I1LVM	$\overline{\text{INT1}}$ low-voltage signal mode control bit (1)		R/W
b6	I2LVM	$\overline{\text{INT2}}$ low-voltage signal mode control bit (1)		R/W
b7	I3LVM	$\overline{\text{INT3}}$ low-voltage signal mode control bit (1)		R/W

Notes:
1. When the LVMPR bit is set to 1 (write enabled), writing to bits U0LVM and IjLVM (j = 0 to 3) is enabled. Rewrite bits U0LVM and IjLVM (j = 0 to 3) after setting the LVMPR bit to 1. When writing 1 to the LVMPR bit, write 0 and then 1 continuously.
2. When the U0LVM bit is set to 1, the TxD0 pin is set to N-channel open-drain output regardless of the setting of the NCH bit in the U0C0 register.

20.3 Clock Synchronous Serial I/O Mode

In clock synchronous serial I/O mode, data is transmitted and received using a transfer clock.
Table 20.2 lists the Clock Synchronous Serial I/O Mode Specifications. Table 20.3 lists the Registers Used and Settings in Clock Synchronous Serial I/O Mode.

Table 20.2 Clock Synchronous Serial I/O Mode Specifications

Item	Specification
Transfer data format	• Transfer data length: 8 bits
Transfer clocks	• The CKDIR bit in the U0MR register is set to 0 (internal clock): fj/(2(n+1)) fj = f1, f8, f32 n = setting value in the U0BRG register: 00h to FFh • The CKDIR bit is set to 1 (external clock): Input from the CLK0 pin
Transmit start conditions	To start transmission, the following requirements must be met: (1) • The TE bit in the U0C1 register is set to 1 (transmission enabled). • The TI bit in the U0C1 register is set to 0 (data present in the U0TB register).
Receive start conditions	To start reception, the following requirements must be met: (1) • The RE bit in the U0C1 register is set to 1 (reception enabled). • The TE bit in the U0C1 register is set to 1 (transmission enabled). • The TI bit in the U0C1 register is set to 0 (data present in the U0TB register).
Interrupt request generation timing	For transmission: One of the following can be selected. • The U0IRS bit is set to 0 (transmit buffer empty): When data is transferred from the U0TB register to the UART0 transmit register (at start of transmission). • The U0IRS bit is set to 1 (transmission completed): When data transmission from the UART0 transmit register is completed. For reception: • When data is transferred from the UART0 receive register to the U0RB register (at completion of reception).
Error detection	Overrun error (2) This error occurs if the serial interface starts receiving the next unit of data before reading the U0RB register and receives the 7th bit of the next unit of data.
Selectable functions	• CLK polarity selection Transfer data input/output can be selected to occur synchronously with the rising or the falling edge of the transfer clock. • LSB first, MSB first selection Whether transmitting or receiving data begins with bit 0 or begins with bit 7 can be selected. • Continuous receive mode selection Reception is enabled immediately by reading the U0RB register.

Notes:
1. When an external clock is selected, the requirements must be met in either of the following states:
   • The external clock is held high when the CKPOL bit in the U0C0 register is set to 0 (transmit data output at the falling edge and receive data input at the rising edge of the transfer clock)
   • The external clock is held low when the CKPOL bit in the U0C0 register is set to 1 (transmit data output at the rising edge and receive data input at the falling edge of the transfer clock)
2. If an overrun error occurs, the receive data (b0 to b8) in the U0RB register will be undefined.
   The IR bit in the S0RIC register remains unchanged.

Table 20.3 Registers Used and Settings in Clock Synchronous Serial I/O Mode (1)

Register	Bit	Function
U0TB	b0 to b7	Set data transmission.
U0RB	b0 to b7	Receive data can be read.
	OER	Overrun error flag
U0BRG	b0 to b7	Set a bit rate.
U0MR	SMD2 to SMD0	Set to 001b.
	CKDIR	Select the internal clock or external clock.
U0C0	CLK1, CLK0	Select the count source for the U0BRG register.
	TXEPT	Transmit register empty flag
	NCH	Select TXD0 pin output mode.
	CKPOL	Select the transfer clock polarity.
	UFORM	Select LSB first or MSB first.
U0C1	TE	Set to 1 to enable transmission/reception
	TI	Transmit buffer empty flag
	RE	Set to 1 to enable reception.
	RI	Receive complete flag
	U0IRS	Select the UART0 transmit interrupt source.
	U0RRM	Set to 1 to use continuous receive mode.

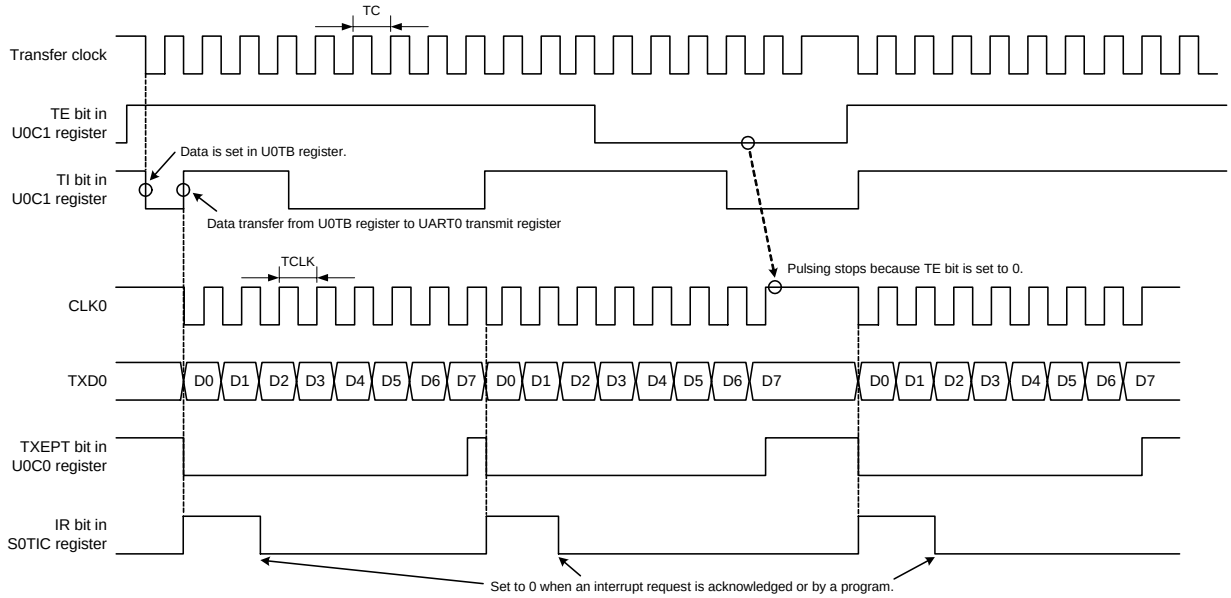
Note:
1. Set the bits not listed in this table to 0 when writing to the above registers in clock synchronous serial I/O mode.

Table 20.4 lists the I/O Pin Functions in Clock Synchronous Serial I/O Mode.
After UART0 operating mode is selected, the TXD0 pin outputs a “H” level until transfer starts. (If the NCH bit is set to 1 (N-channel open-drain output), this pin is in the high-impedance state.)

Table 20.4 I/O Pin Functions in Clock Synchronous Serial I/O Mode

Pin Name	Function	Selection Method
TXD0 (P1_4 or P3_4)	Serial data output	• TXD0 (P1_4) Bits TXD0SEL1 and TXD0SEL0 in U0SR register = 01b (P1_4) • TXD0 (P3_4) Bits TXD0SEL1 and TXD0SEL0 in U0SR register = 10b (P3_4) • P1_4 and P3_4 can be used as a port by setting bits TXD0SEL1 and TXD0SEL0 = 00b.
RXD0 (P1_5 or P3_5)	Serial data input	• RXD0 (P1_5) Bits RXD0SEL1 and RXD0SEL0 in U0SR register = 01b (P1_5) • RXD0 (P3_5) Bits RXD0SEL1 and RXD0SEL0 in U0SR register = 10b (P3_5) • P1_5 and P3_5 can be used as a port by setting bits RXD0SEL1 and RXD0SEL0 = 00b.
CLK0 (P1_6 or P3_7)	Transfer clock output	• CLK0 (P1_6) Bits CLK0SEL1 and CLK0SEL0 in U0SR register = 01b (P1_6) CKDIR bit in U0MR register = 0 • CLK0 (P3_7) Bits CLK0SEL1 and CLK0SEL0 in U0SR register = 10b (P3_7) CKDIR bit in U0MR register = 0
	Transfer clock input	• CLK0 (P1_6) Bits CLK0SEL1 and CLK0SEL0 in U0SR register = 01b (P1_6) PD1_6 bit in PD1 register = 0 • CLK0 (P3_7) Bits CLK0SEL1 and CLK0SEL0 in U0SR register = 10b (P3_7) PD3_7 bit in PD3 register = 0 CKDIR bit in U0MR register = 1

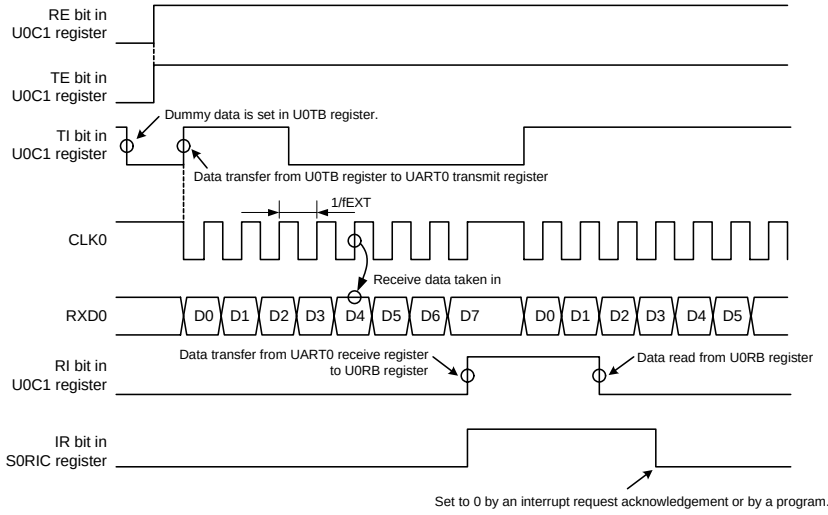
• Transmit Timing Example (Internal Clock Selected)



The above applies when:
- CKDIR bit in U0MR register = 0 (internal clock)
- CKPOL bit in U0C0 register = 0 (transmit data output at the falling edge and receive data input at the rising edge of the transfer clock)
- U0IRS bit in U0C1 register = 0 (interrupt request generation when the transmit buffer is empty)

TC = TCLK = 2(n+1)/fj
fj: Frequency of U0BRG count source (f1, f8, f32)
n: Setting value in U0BRG register

• Receive Timing Example (External Clock Selected)



The above applies when:
- CKDIR bit in U0MR register = 1 (external clock)
- CKPOL bit in U0C0 register = 0 (transmit data output at the falling edge and receive data input at the rising edge of the transfer clock)

The following should be met when “H” is applied to the CLK0 pin before receiving data:
- TE bit in U0C1 register = 1 (transmission enabled)
- RE bit in U0C1 register = 1 (reception enabled)
- Dummy data is written to U0TB register

fEXT: Frequency of external clock

Figure 20.3 Transmit and Receive Timing in Clock Synchronous Serial I/O Mode

20.3.1 Measure for Dealing with Communication Errors

If communication is aborted or a communication error occurs while transmitting or receiving in clock synchronous serial I/O mode, follow the procedures below:

(1) Set the TE bit in the U0C1 register to 0 (transmission disabled) and the RE bit to 0 (reception disabled).
(2) Set bits SMD2 to SMD0 in the U0MR register to 000b (serial interface disabled).
(3) Set bits SMD2 to SMD0 in the U0MR register to 001b (clock synchronous serial I/O mode).
(4) Set the TE bit in the U0C1 register to 1 (transmission enabled) and the RE bit to 1 (reception enabled).

20.3.2 Polarity Select Function

Figure 20.4 shows the Transfer Clock Polarity. Use the CKPOL bit in the U0C0 register to select the transfer clock polarity.

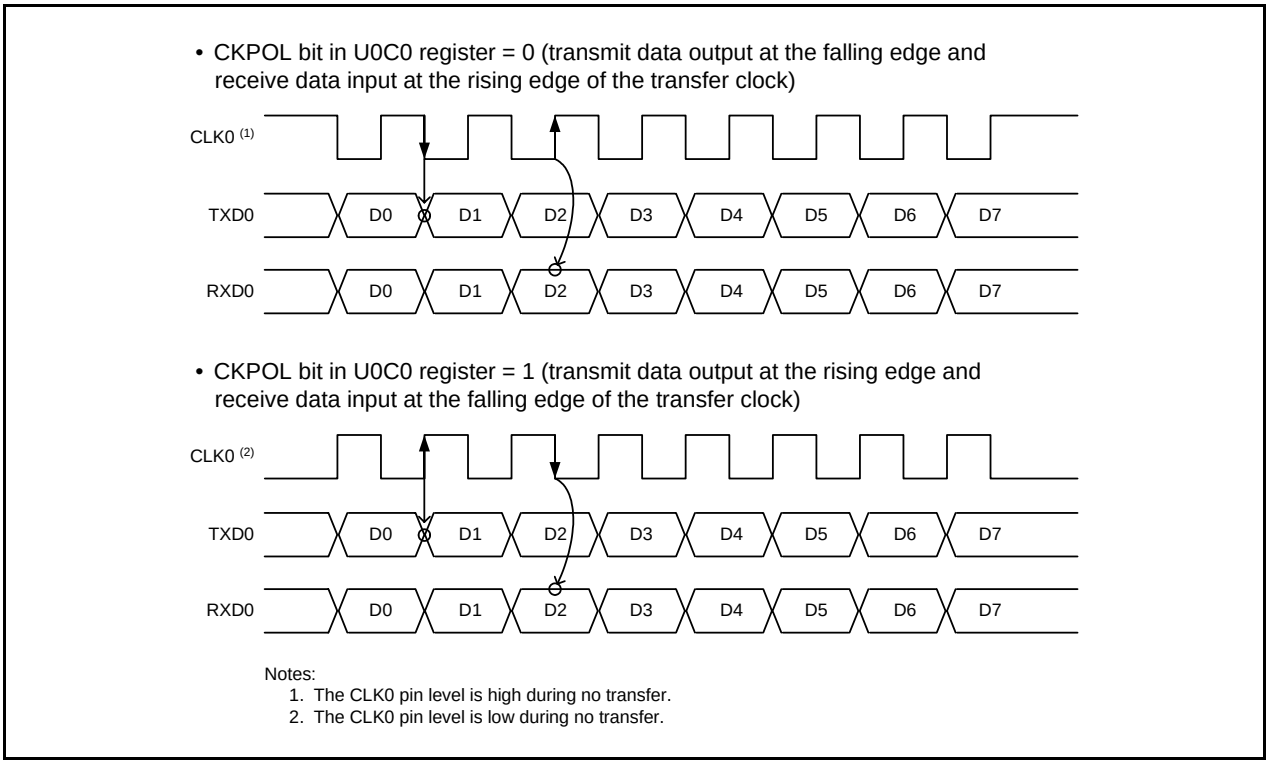


Figure 20.4 Transfer Clock Polarity

20.3.3 LSB First/MSB First Select Function

Figure 20.5 shows the Transfer Format. Use the UFORM bit in the U0C0 register to select the transfer format.

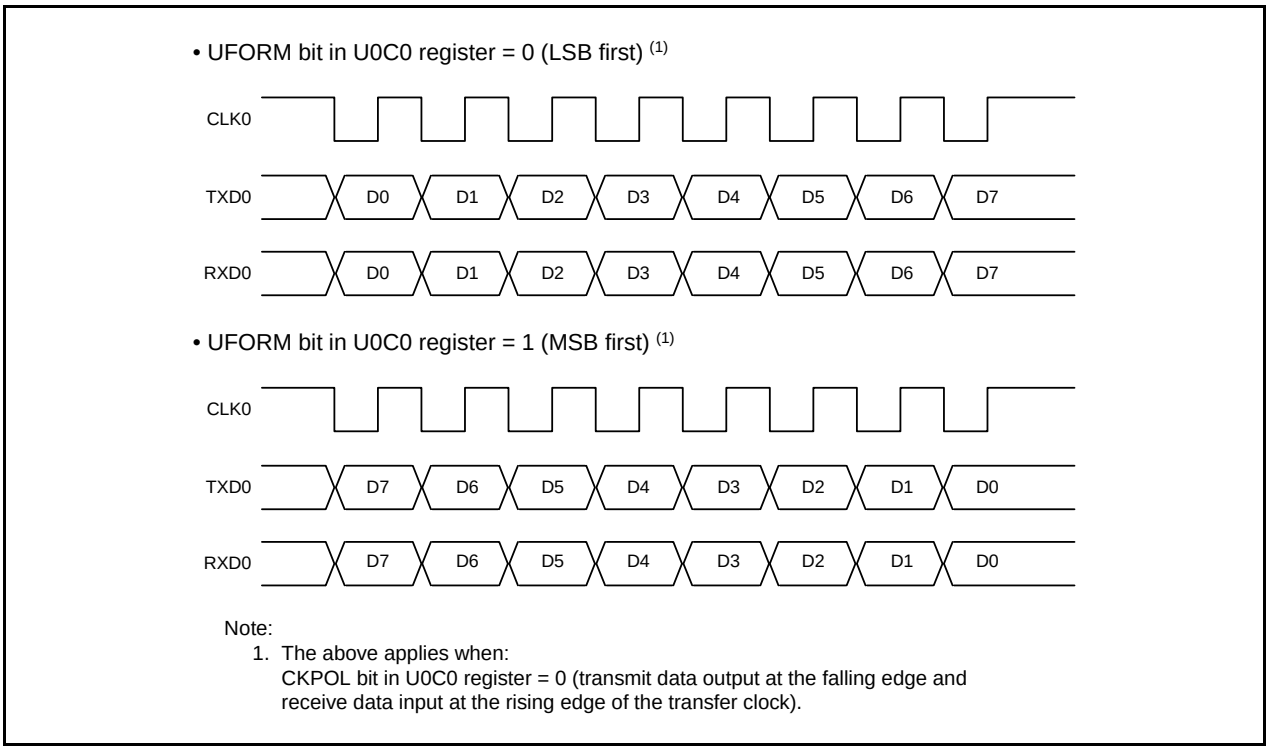


Figure 20.5 Transfer Format

20.3.4 Continuous Receive Mode

Continuous receive mode is selected by setting the U0RRM bit in the U0C1 register to 1 (continuous receive mode enabled). In this mode, reading the U0RB register sets the TI bit in the U0C1 register to 0 (data present in the U0TB register). If the U0RRM bit is set to 1, do not write dummy data to the U0TB register by a program.

20.4 Clock Asynchronous Serial I/O (UART) Mode

The UART mode allows data transmission and reception after setting the desired bit rate and transfer data format. Table 20.5 lists the UART Mode Specifications. Table 20.6 lists the Registers Used and Settings in UART Mode.

Table 20.5 UART Mode Specifications

Item	Specification
Transfer data formats	• Character bits (transfer data): Selectable among 7, 8 or 9 bits • Start bit: 1 bit • Parity bit: Selectable among odd, even, or none • Stop bits: Selectable among 1 or 2 bits
Transfer clocks	• The CKDIR bit in the U0MR register is set to 0 (internal clock): fj/(16(n+1)) fj = f1, f8, f32 n = setting value in the U0BRG register: 00h to FFh • The CKDIR bit is set to 1 (external clock): fEXT/(16(n+1)) fEXT: Input from the CLK0 pin n = setting value in the U0BRG register: 00h to FFh
Transmit start conditions	To start transmission, the following requirements must be met: • The TE bit in the U0C1 register is set to 1 (transmission enabled). • The TI bit in the U0C1 register is set to 0 (data present in the U0TB register).
Receive start conditions	To start reception, the following requirements must be met: • The RE bit in the U0C1 register is set to 1 (reception enabled). • Start bit detection
Interrupt request generation timing	For transmission: One of the following can be selected. • The U0IRS bit is set to 0 (transmit buffer empty): When data is transferred from the U0TB register to the UART0 transmit register (at start of transmission). • The U0IRS bit is set to 1 (transfer completed): When data transmission from the UART0 transmit register is completed. For reception: • When data is transferred from the UART0 receive register to the U0RB register (at completion of reception).
Error detection	• Overrun error (1) This error occurs if the serial interface starts receiving the next unit of data before reading the U0RB register and receive the bit one before the last stop bit of the next unit of data. • Framing error This error occurs when the set number of stop bits is not detected. (2) • Parity error This error occurs when parity is enabled, and the number of 1's in the parity and character bits do not match the set number of 1's. (2) • Error sum flag This flag is set to 1 if an overrun, framing, or parity error occurs.

Notes:
1. If an overrun error occurs, the receive data (b0 to b8) in the U0RB register will be undefined.
2. The framing error flag and the parity error flag are set to 1 when data is transferred from the UART0 receive register to the U0RB register.

Table 20.6 Registers Used and Settings in UART Mode

Register	Bit	Function
U0TB	b0 to b8	Set transmit data. (1)
U0RB	b0 to b8	Receive data can be read. (2)
	OER, FER, PER, SUM	Error flag
U0BRG	b0 to b7	Set a bit rate.
U0MR	SMD2 to SMD0	Set to 100b when transfer data is 7 bits long. Set to 101b when transfer data is 8 bits long. Set to 110b when transfer data is 9 bits long.
	CKDIR	Select the internal clock or external clock.
	STPS	Select the stop bit.
	PRY, PRYE	Select whether parity is included and whether odd or even.
U0C0	CLK0, CLK1	Select the count source for the U0BRG register.
	TXEPT	Transmit register empty flag
	NCH	Select TXD0 pin output mode.
	CKPOL	Set to 0.
	UFORM	Select LSB first or MSB first when transfer data is 8 bits long. Set to 0 when transfer data is 7 bits or 9 bits long.
U0C1	TE	Set to 1 to enable transmission.
	TI	Transmit buffer empty flag
	RE	Set to 1 to enable reception.
	RI	Receive complete flag
	U0IRS	Select the UART0 transmit interrupt source.
	U0RRM	Set to 0.

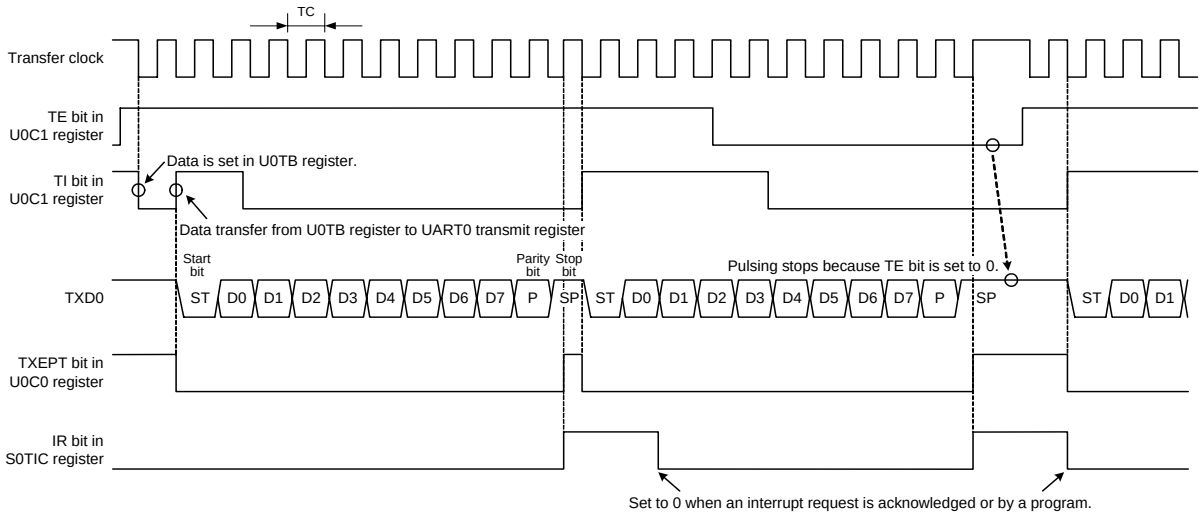
Notes:
1. The bits used for transmission/receive data are as follows:
   • Bits b0 to b6 when transfer data is 7 bits long
   • Bits b0 to b7 when transfer data is 8 bits long
   • Bits b0 to b8 when transfer data is 9 bits long
2. The contents of the following are undefined:
   • Bits 7 and 8 when the transfer data is 7 bits long
   • Bit 8 when the transfer data is 8 bits long

Table 20.7 lists the I/O Pin Functions in UART Mode.
After the UART0 operating mode is selected, the TXD0 pin outputs a “H” level until transfer starts. (If the NCH bit is set to 1 (N-channel open-drain output), this pin is in the high-impedance state.)

Table 20.7 I/O Pin Functions in UART Mode

Pin name	Function	Selection Method
TXD0 (P1_4 or P3_4)	Serial data output	• TXD0 (P1_4) Bits TXD0SEL1 and TXD0SEL0 in U0SR register = 01b (P1_4) • TXD0 (P3_4) Bits TXD0SEL1 and TXD0SEL0 in U0SR register = 10b (P3_4) • P1_4 and P3_4 can be used as a port by setting bits TXD0SEL1 and TXD0SEL0 = 00b.
RXD0 (P1_5 or P3_5)	Serial data input	• RXD0 (P1_5) Bits RXD0SEL1 and RXD0SEL0 in U0SR register = 01b (P1_5) • RXD0 (P3_5) Bits RXD0SEL1 and RXD0SEL0 in U0SR register = 10b (P3_5) • P1_5 and P3_5 can be used as a port by setting bits RXD0SEL1 and RXD0SEL0 = 00b.
CLK0 (P1_6 or P3_7)	Programmable I/O port	• CLK0 (P1_6) Bits CLK0SEL1 and CLK0SEL0 in U0SR register = 01b (P1_6) CKDIR bit in U0MR register = 0 • CLK0 (P3_7) Bits CLK0SEL1 and CLK0SEL0 in U0SR register = 10b (P3_7) CKDIR bit in U0MR register = 0
	Transfer clock input	• CLK0 (P1_6) Bits CLK0SEL1 and CLK0SEL0 in U0SR register = 01b (P1_6) PD1_6 bit in PD1 register = 0 • CLK0 (P3_7) Bits CLK0SEL1 and CLK0SEL0 in U0SR register = 10b (P3_7) PD3_7 bit in PD3 register = 0 CKDIR bit in U0MR register = 1

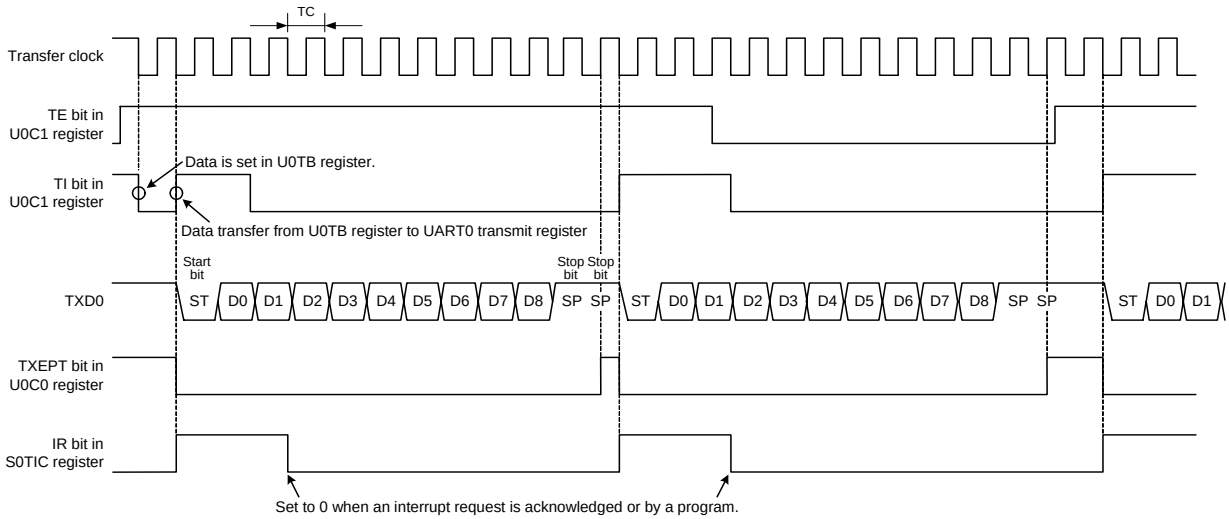
• Transmit Timing Example When Transfer Data is 8 Bits Long (Parity Enabled, One Stop Bit)



The above applies when:
- PRYE bit in U0MR register = 1 (parity enabled)
- STPS bit in U0MR register = 0 (one stop bit)
- U0IRS bit in U0C1 register = 1
  (interrupt request generation when transmission is completed)

TC = 16(n+1)/fj or 16(n+1)/fEXT
fj: Frequency of U0BRG count source (f1, f8, f32)
fEXT: Frequency of U0BRG count source (external clock)
n: Setting value in U0BRG register

• Transmit Timing Example When Transfer Data is 9 Bits Long (Parity Disabled, Two Stop Bits)



The above applies when:
- PRYE bit in U0MR register = 0 (parity disabled)
- STPS bit in U0MR register = 1 (two stop bits)
- U0IRS bit in U0C1 register = 0
  (interrupt request generation when the transmit buffer is empty)

TC = 16(n+1)/fj or 16(n+1)/fEXT
fj: Frequency of U0BRG count source (f1, f8, f32)
fEXT: Frequency of U0BRG count source (external clock)
n: Setting value in U0BRG register

Figure 20.6 Transmit Timing in UART Mode

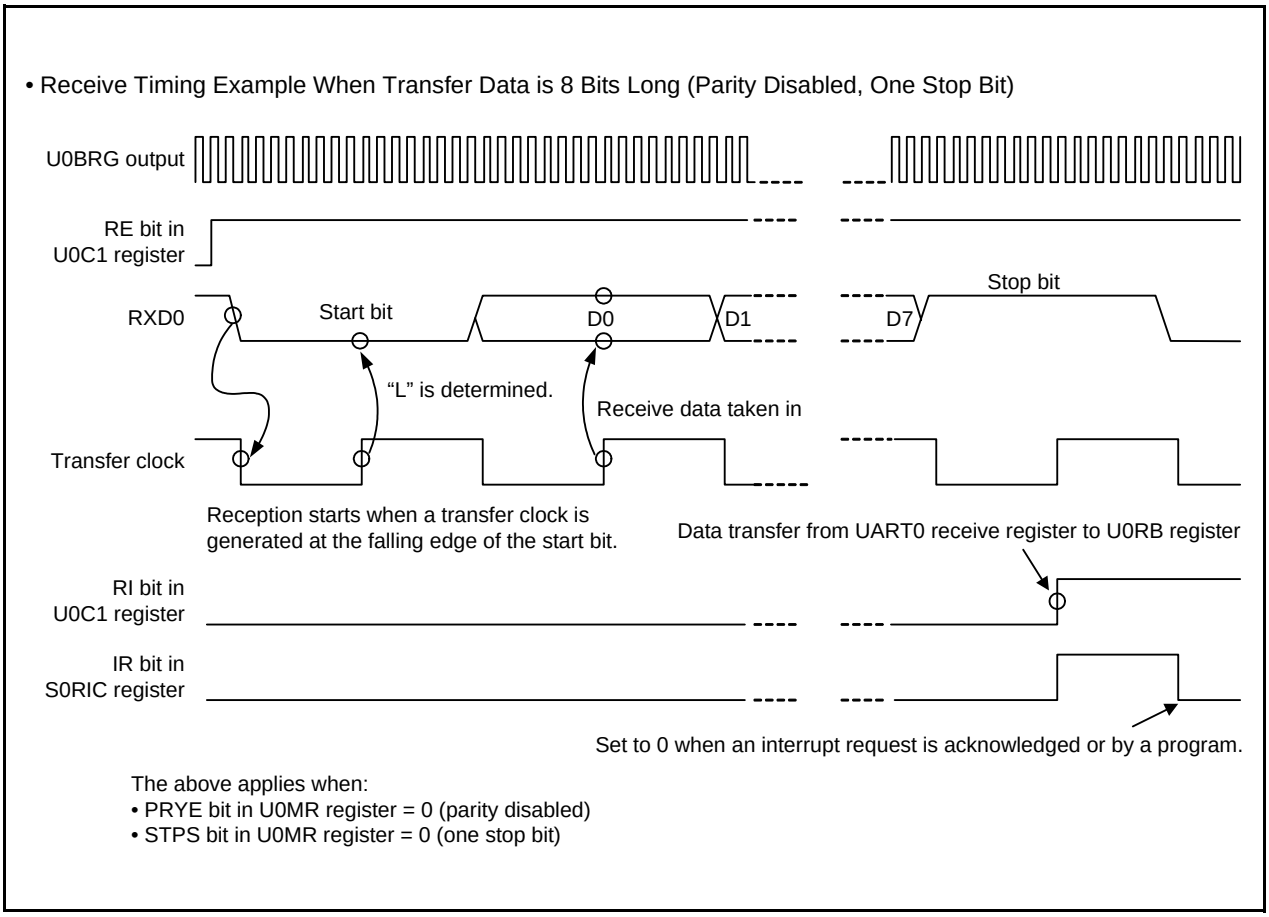


Figure 20.7 Receive Timing in UART Mode

20.4.1 Bit Rate

In UART mode, the bit rate is the frequency divided by the U0BRG register and divided by 16.

UART mode

• Internal clock selected

$$\text{Setting value in U0BRG register} = \frac{fj}{\text{Bit Rate} \times 16} - 1$$

fj: Count source frequency of U0BRG register (f1, f8, or f32)

• External clock selected

$$\text{Setting value in U0BRG register} = \frac{fEXT}{\text{Bit Rate} \times 16} - 1$$

fEXT: Count source frequency of U0BRG register (external clock)

Figure 20.8 Formula for Calculating Setting Value in U0BRG Register

Table 20.8 Bit Rate Setting Example in UART Mode (Internal Clock Selected)

Bit Rate (bps)	U0BRG Count Source	System Clock = 20 MHz			System Clock = 18.432 MHz (1)			System Clock = 8 MHz		
		U0BRG Setting Value	Actual Time (bps)	Setting Error (%)	U0BRG Setting Value	Actual Time (bps)	Setting Error (%)	U0BRG Setting Value	Actual Time (bps)	Setting Error (%)
1200	f8	129 (81h)	1201.92	0.16	119 (77h)	1200.00	0.00	51 (33h)	1201.92	0.16
2400	f8	64 (40h)	2403.85	0.16	59 (3Bh)	2400.00	0.00	25 (19h)	2403.85	0.16
4800	f8	32 (20h)	4734.85	–1.36	29 (1Dh)	4800.00	0.00	12 (0Ch)	4807.69	0.16
9600	f1	129 (81h)	9615.38	0.16	119 (77h)	9600.00	0.00	51 (33h)	9615.38	0.16
14400	f1	86 (56h)	14367.82	–0.22	79 (4Fh)	14400.00	0.00	34 (22h)	14285.71	–0.79
19200	f1	64 (40h)	19230.77	0.16	59 (3Bh)	19200.00	0.00	25 (19h)	19230.77	0.16
28800	f1	42 (2Ah)	29069.77	0.94	39 (27h)	28800.00	0.00	16 (10h)	29411.76	2.12
38400	f1	32 (20h)	37878.79	–1.36	29 (1Dh)	38400.00	0.00	12 (0Ch)	38461.54	0.16
57600	f1	21 (15h)	56818.18	–1.36	19 (13h)	57600.00	0.00	8 (08h)	55555.56	–3.55
115200	f1	10 (0Ah)	113636.36	–1.36	9 (09h)	115200.00	0.00	—	—	—

Note:

1. For the high-speed on-chip oscillator, the correction value in the FRA4 register should be written into the FRA1 register and the correction value in the FRA5 register should be written into the FRA3 register.
   This applies when the high-speed on-chip oscillator is selected as the system clock and bits FRA22 to FRA20 in the FRA2 register are set to 000b (divide-by-2 mode). For the precision of the high-speed on-chip oscillator, refer to **24. Electrical Characteristics**.

20.4.2 Measure for Dealing with Communication Errors

If communication is aborted or a communication error occurs while transmitting or receiving in UART mode, follow the procedures below:

(1) Set the TE bit in the U0C1 register to 0 (transmission disabled) and the RE bit to 0 (reception disabled).
(2) Set bits SMD2 to SMD0 in the U0MR register to 000b (serial interface disabled).
(3) Set bits SMD2 to SMD0 in the U0MR register to 100b (UART mode, transfer data 7 bits long), 101b (UART mode, transfer data 8 bits long), or 110b (UART mode, transfer data 9 bits long).
(4) Set the TE bit in the U0C1 register to 1 (transmission enabled) and the RE bit to 1 (reception enabled).

20.5 Low-Voltage Signal Mode

Serial interface (UART0) communication and the $\overline{\text{INT}}$ input for the $\overline{\text{INT}}$ interrupt can be performed using a low-voltage signal. Table 20.9 lists the Pins Usable for Inputting and Outputting Low-Voltage Signal.
Depending on the setting of the TSMR register, the pins enabled for low-voltage signal mode is switched from schmitt input to CMOS input when they are used as input.
Set the input threshold values for CMOS input using registers VLT0 and VLT1.
When low-voltage signal mode is used, all inputs are set to CMOS input. Since schmitt input is disabled, always take countermeasures against noise.

Table 20.9 Pins Usable for Inputting and Outputting Low-Voltage Signal

Peripheral Function Name		Pin
Serial interface	UART0 Clock synchronous serial I/O Clock asynchronous serial I/O	CLK0, RXD0, TXD0
$\overline{\text{INT}}$	$\overline{\text{INT0}}$ to $\overline{\text{INT3}}$	$\overline{\text{INT0}}$ to $\overline{\text{INT3}}$

20.6 Notes on Serial Interface (UART0)

- When reading data from the U0RB register either in clock synchronous serial I/O mode or in clock asynchronous serial I/O mode, always read data in 16-bit units.
  When the high-order byte of the U0RB register is read, bits PER and FER in the U0RB register and the RI bit in the U0C1 register are set to 0.
  To check receive errors, read the U0RB register and then use the read data.

  Program example to read the receive buffer register:

```
MOV.W    00A6H, R0    ; Read the U0RB register
```

- When writing data to the U0TB register in clock asynchronous serial I/O mode with 9-bit transfer data length, write data to the high-order byte first and then the low-order byte, in 8-bit units.

  Program example to write to the transmit buffer register:

```
MOV.B    #XXH, 00A3H  ; Write to the high-order byte of the U0TB register
MOV.B    #XXH, 00A2H  ; Write to the low-order byte of the U0TB register
```

21. Sensor Control Unit

The sensor control unit (SCU) provides the functions required to control a capacitive touch electrode sensor.
The unit measures the floating capacitance of the touch electrode connected to the measurement pin.
As shown in Figure 21.1, there exist electrostatic capacitances between the electrode and the surrounding conductors. Because the human body is an electrical conductor, when a finger is placed close to the electrode, the value of the floating capacitance increases.
The sensor control unit detects the increase in floating capacitance to determine whether the electrode is being touched or not.
For details on the measurement operation principles on the unit's capacitive touch electrode, refer to **21.4 Principles of Measurement Operation**.

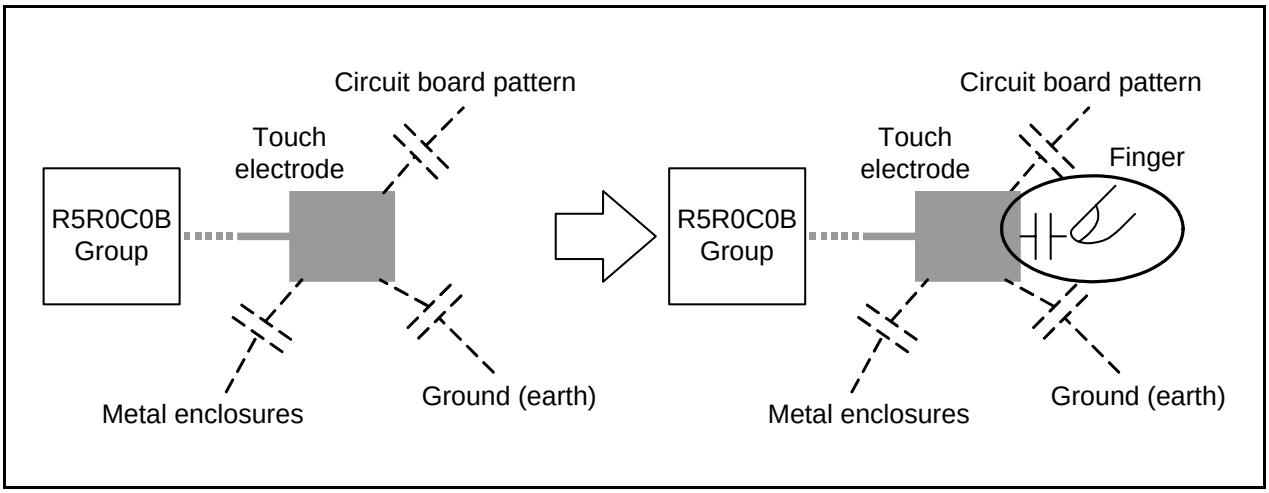


Figure 21.1 Increased Floating Capacitance due to Presence of Finger

21.1 Overview

Figure 21.2 shows the Sensor Control Unit Block Diagram.
As shown in Figure 21.2, the sensor control unit consists of the status control, the secondary counter, and the primary counter.
The unit controls the ports and the counters to detect the floating capacitance of the capacitive touch electrode.
The operating clock for the sensor control unit is f1, f2 or f4, which ever is selected as the count source. The count source is supplied to each counter.
The sensor control unit supports the following two types of measurement mode:

- Single mode: Touches on a channel are detected.
- Scan mode: Touches on multiple channels are detected.

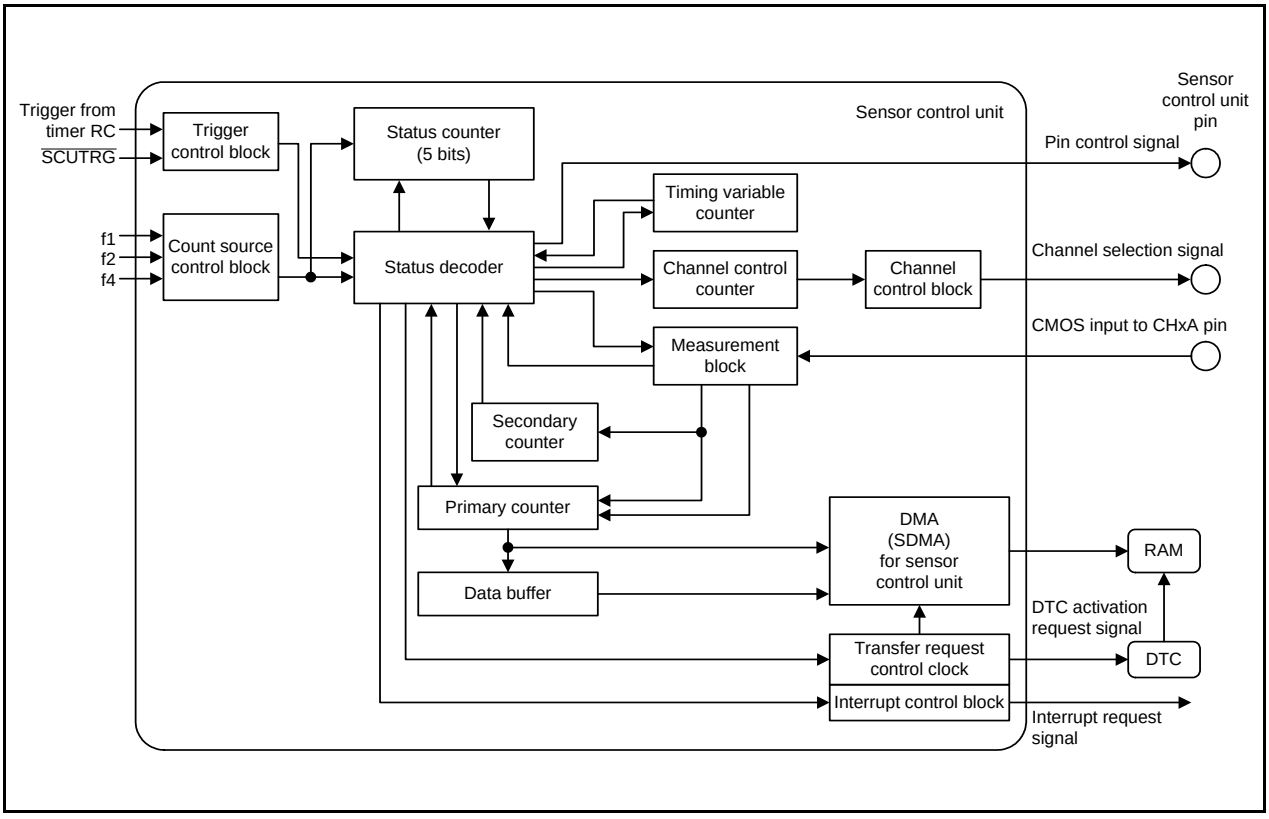


Figure 21.2 Sensor Control Unit Block Diagram

Table 21.1 Sensor Control Unit Pin Configuration

Pin Name	Assigned Pin	I/O	Description
CHxA	P0_2	I/O	Touch detection
CHxB	P0_1		Electrostatic capacitive touch detection control signal input
CHxC	P0_0		
CH0	P1_0	Input	Electrostatic capacitive touch detection pins
CH1	P1_1		
CH2	P1_2		
CH3	P1_3		
CH4	P1_4		
CH5	P1_5		
CH6	P1_6		
CH7	P1_7		
$\overline{\text{SCUTRG}}$	P3_3		External trigger input

21.2 Registers

Table 21.2 lists the Registers used for the SCU.

Table 21.2 Registers

Register Name	Symbol	After Reset	Address	Access Size
SCU Control Register 0	SCUCR0	00h	02C0h	8
SCU Mode Register	SCUMR	00h	02C1h	8
SCU Timing Control Register 0	SCTCR0	03h	02C2h	8
SCU Timing Control Register 1	SCTCR1	01h	02C3h	8
SCU Timing Control Register 2	SCTCR2	10h	02C4h	8
SCU Timing Control Register 3	SCTCR3	00h	02C5h	8
SCU Channel Control Register	SCHCR	00h	02C6h	8
SCU Channel Control Counter	SCUCHC	00h	02C7h	8
SCU Flag Register	SCUFR	00h	02C8h	8
SCU Status Counter Register	SCUSTC	00h	02C9h	8
SCU Secondary Counter Set Register	SCUSCS	07h	02CAh	8
SCU Secondary Counter Register	SCUSCC	07h	02CBh	8
SCU Destination Address Register	SCUDAR	0600h	02CEh	16
			02CFh	
SCU Data Buffer Register	SCUDBR	0000h	02D0h	16
			02D1h	
SCU Primary Counter Register	SCUPRC	0000h	02D2h	16
			02D3h	
SCU Random Value Store Register 0	SCRVR0	00h	02D4h	8
SCU Random Value Store Register 1	SCRVR1	00h	02D5h	8
SCU Random Value Store Register 2	SCRVR2	00h	02D6h	8
SCU Random Value Store Register 3	SCRVR3	00h	02D7h	8
SCU Random Value Store Register 4	SCRVR4	00h	02D8h	8
SCU Random Value Store Register 5	SCRVR5	00h	02D9h	8
SCU Random Value Store Register 6	SCRVR6	00h	02DAh	8
SCU Random Value Store Register 7	SCRVR7	00h	02DBh	8
SCU Input Enable Register 0	TSIER0	00h	02DCh	8

21.2.1 SCU Control Register 0 (SCUCR0)

Address 02C0h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	SCUIE	BCSHORT	SCCLK1	SCCLK0	—	SCINIT	SCUE	SCSTRT
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	SCSTRT	Measurement start bit	0: Measurement stops 1: Measurement starts	R/W
b1	SCUE	SCU operation enable bit	0: Operation disabled (1) 1: Operation enabled	R/W
b2	SCINIT	SCU control block initialize bit	Writing 1 to this bit initializes the SCU control block and the registers. (2)	R/W
b3	—	Reserved bit	Set to 0.	R/W
b4	SCCLK0	Count source select bit	b5 b4 0 0: f1 0 1: f2 1 0: f4 1 1: Do not set.	R/W
b5	SCCLK1			R/W
b6	BCSHORT	CHxB-CHxC short select bit	0: No shorted (The shorting switch is always turned OFF.) 1: Shortened (The shorting switch is turned ON in Status 7 and 14, and turned OFF in Status 4, 11, and 18. The switch is turned ON in Status 6 and 15, and turned OFF in Status 11.)	R/W
b7	SCUIE	SCU interrupt enable bit	0: SCU interrupt disabled 1: SCU interrupt enabled	R/W

Notes:
1. The SCUE bit is not set to 0 (operation disabled) even if the SCSTRT bit is set to 0 (measurement stops), or even if the SCINIT bit is set to 1 (initialized). The SCUE bit is not also set to 0 even if an interrupt request is generated after a measurement finishes. Set this bit to 0 by a program.
2. The following are initialized:
   • Registers SCUSTC, SCUPRC, SCUSCC, SCUDBR, and SCUFR
   • The SCSTRT bit in the SCUCR0 register
   • Bits SCUCHC0 to SCUCHC2 in the SCUCHC register
   • The SCU control block (SCU timing control counter)

SCSTRT Bit (Measurement Start Bit)

[Conditions for setting to 0]
- Set this bit to 0 by a program (forced stop).
- When measurement finishes while bits SCCAP1 to SCCAP0 in the SCUMR register is 0 (software trigger) and an interrupt request is generated.
- When 1 is written to the SCINIT bit.

[Condition for setting to 1]
Set to 1 by a program.

When the SCSTRT bit is set to 0 (measurement stops) while bits SCCAP1 to SCCAP0 in the SCUMR register are 0 (software trigger), the value of each counter is retained. When the SCSTRT bit is set to 1 (measurement starts), measurement starts from the status where the measurement is stopped.

While the SCUCAP1 bit is 1 (trigger from timer RC or external trigger selected), if an external trigger occurs when the SCSTRT bit is set to 0 (measurement stops) and then set to 1, measurement starts from Status 1. Make sure that initialization is performed using the SCINIT bit before setting the SCSTRT bit to 1.

SCUE Bit (SCU Operation Enable Bit)

When the SCUE bit is set to 1 (operation enabled), the states will change to as follows:

- The analog path between the CHxB-CHxC path is disconnected (the disconnecting switch is turned OFF).
- The analog channel control decoder is switched for the sensor control unit.
- The analog switch for CHxA is forcibly turned ON.

21.2.2 SCU Mode Register (SCUMR)

Address 02C1h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	SCCAP1	SCCAP0	CONST	MJNUM2	MJNUM1	MJNUM0	RANDOM	PREMSR
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	PREMSR	PRE measurement select bit	0: No PRE measurement 1: PRE measurement	R/W
b1	RANDOM	Random measurement select bit	0: No random measurement 1: Random measurement	R/W
b2	MJNUM0	Majority measurement sampling count select bits	b4 b3 b2 0 0 0: No majority measurement 0 0 1: 3 times 0 1 0: 5 times 0 1 1: 7 times 1 0 0: 9 times 1 0 1: 11 times 1 1 0: 13 times 1 1 1: 15 times	R/W
b3	MJNUM1			R/W
b4	MJNUM2			R/W
b5	CONST	Measurement period length select bit	0: Not fixed (dependent on the random value and the number of measurements) 1: Fixed	R/W
b6	SCCAP0	SCU measurement start trigger select bit	b7 b6 0 0: Software trigger (the SCSTRT bit in the SCUCR0 register) 0 1: Do not set. 1 0: Measurement start trigger from timer RC 1 1: External trigger ($\overline{\text{SCUTRG}}$)	R/W
b7	SCCAP1			R/W

21.2.3 SCU Timing Control Register 0 (SCTCR0)

Address 02C2h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TCS2C	TCS16	TCS15	TCS14	TCS13	TCS12	TCS11	TCS10
After Reset	0	0	0	0	0	0	1	1

Bit	Symbol	Bit Name	Function	R/W
b0	TCS10	Period 1 cycle count select bit	b6 b5 b4 b3 b2 b1 b0 0 0 0 0 0 0 0: 1 cycle 0 0 0 0 0 0 1: 2 cycles ⋮ ⋮ 1 1 1 1 1 1 1: 128 cycles	R/W
b1	TCS11			R/W
b2	TCS12			R/W
b3	TCS13			R/W
b4	TCS14			R/W
b5	TCS15			R/W
b6	TCS16			R/W
b7	TCS2C	Period 2 control bit	0: The number of cycles for period 2 is selected by bits TCS20 to TCS23 in the SCTCR1 register 1: The number of cycles for period 2 is 0 (skip)	R/W

Bits TCS10 to TCS16 (Period 1 Cycle Count Select Bits)

These bits are used to set the number of cycles for period 1 (period when CHxA = “Hi-Z”, CHxB = “Hi-Z”, and CHxC = “H”). One to 128 cycles can be selected. After reset, these bits are set to 00000011b (4 cycles).

- Period 1 cycle example
  Count source frequency 4 MHz: 250 ns to 32 µs
  Count source frequency 5 MHz: 200 ns to 25.6 µs

21.2.4 SCU Timing Control Register 1 (SCTCR1)

Address 02C3h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	TCS31	TCS30	TCS23	TCS22	TCS21	TCS20
After Reset	0	0	0	0	0	0	0	1

Bit	Symbol	Bit Name	Function	R/W
b0	TCS20	Period 2 cycle count select bit (1)	b3 b2 b1 b0 0 0 0 0: 1 cycle 0 0 0 1: 2 cycles (after reset) 0 0 1 0: 3 cycles 0 0 1 1: 4 cycles 0 1 0 0: 5 cycles 0 1 0 1: 6 cycles 0 1 1 0: 7 cycles 0 1 1 1: 8 cycles 1 0 0 0: 9 cycles 1 0 0 1: 10 cycles 1 0 1 0: 11 cycles 1 0 1 1: 12 cycles 1 1 0 0: 13 cycles 1 1 0 1: 14 cycles 1 1 1 0: 15 cycles 1 1 1 1: 16 cycles	R/W
b1	TCS21			R/W
b2	TCS22			R/W
b3	TCS23			R/W
b4	TCS30	Period 3 cycle count select bit	b5 b4 0 0: 1 cycle (after reset) 0 1: 2 cycles 1 0: 3 cycles 1 1: 4 cycles	R/W
b5	TCS31			R/W
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b7	—			

Note:
1. When the TCS2C bit in the SCTCR0 register is set to 0 (the number of cycles for period 2 is selected by bits TCS20 to TCS23 in the SCTCR1 register), bits TCS20 to TCS23 are enabled.

Bits TCS20 to TCS23 (Period 2 Cycle Count Select Bits)

These bits are used to set the number of cycles for period 2 (period when CHxA = “L”, CHxB = “Hi-Z”, and CHxC = “Hi-Z”).

Table 21.3 Period 2 Cycle example (1)

Count Source Frequency	1 Cycle	2 Cycles (1)	3 Cycles	4 Cycles	5 Cycles	6 Cycles	7 Cycles	8 Cycles
4 MHz	250 ns	500 ns	750 ns	1.0 µs	1.25 µs	1.5 µs	1.75 µs	2.0 µs
5 MHz	200 ns	400 ns	600 ns	800 ns	1.0 µs	1.2 µs	1.4 µs	1.6 µs

Note:
1. Value after reset.

Table 21.4 Period 2 Cycle Example (2)

Count Source Frequency	9 Cycles	10 Cycles	11 Cycles	12 Cycles	13 Cycles	14 Cycles	15 Cycles	16 Cycles
4 MHz	2.25 µs	2.5 µs	2.75 µs	3.0 µs	3.25 µs	3.5 µs	3.75 µs	4.0 µs
5 MHz	1.8 µs	2.0 µs	2.2 µs	2.4 µs	2.6 µs	2.8 µs	3.0 µs	3.2 µs

Bits TCS30 and TCS31(Period 3 Cycle Count Select Bits)

These bits are used to set the number of cycles for period 3 (period when CHxA = “L”, CHxB = “L”, and CHxC = “Hi-Z”).

Table 21.5 Period 3 Cycle Example

Count Source Frequency	1 Cycle (1)	2 Cycles	3 Cycles	4 Cycles
4 MHz	250 ns	500 ns	750 ns	1.0 µs
5 MHz	200 ns	400 ns	600 ns	800 ns

Note:
1. Value after reset.

21.2.5 SCU Timing Control Register 2 (SCTCR2)

Address 02C4h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TCS53	TCS52	TCS51	TCS50	TCS5C	TCS42	TCS41	TCS40
After Reset	0	0	0	1	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TCS40	Period 4 cycle count select bit	b2 b1 b0 0 0 0: 1 cycle (after reset) 0 0 1: 2 cycles 0 1 0: 3 cycles 0 1 1: 4 cycles 1 0 0: 5 cycles 1 0 1: 6 cycles 1 1 0: 7 cycles 1 1 1: 8 cycles	R/W
b1	TCS41			R/W
b2	TCS42			R/W
b3	TCS5C	Period 5 control bit	0: The number of cycles for period 5 is selected by bits SCTCR20 to SCTCR23 1: The number of cycles for period 5 is 0 (skip)	R/W
b4	TCS50	Period 5 cycle count select bit (1)	b7 b6 b5 b4 0 0 0 0: 1 cycle 0 0 0 1: 2 cycles (after reset) 0 0 1 0: 3 cycles 0 0 1 1: 4 cycles 0 1 0 0: 5 cycles 0 1 0 1: 6 cycles 0 1 1 0: 7 cycles 0 1 1 1: 8 cycles 1 0 0 0: 9 cycles 1 0 0 1: 10 cycles 1 0 1 0: 11 cycles 1 0 1 1: 12 cycles 1 1 0 0: 13 cycles 1 1 0 1: 14 cycles 1 1 1 0: 15 cycles 1 1 1 1: 16 cycles	R/W
b5	TCS51			R/W
b6	TCS52			R/W
b7	TCS53			

Note:
1. When the TCS5C bit is set to 0 (the number of cycles for period 5 is selected by bits TCS50 to TCS53), bits TCS50 to TCS53 are enabled.

Bits TCS40 to TCS42 (Period 4 Cycle Count Select Bits)

These bits are used to set the number of cycles for period 4.

Table 21.6 Period 4 Cycle Example

Count Source Frequency	1 Cycle (1)	2 Cycles	3 Cycles	4 Cycles	5 Cycles	6 Cycles	7 Cycles	8 Cycles
4 MHz	250 ns	500 ns	750 ns	1.0 µs	1.25 µs	1.5 µs	1.75 µs	2.0 µs
5 MHz	200 ns	400 ns	600 ns	800 ns	1.0 µs	1.2 µs	1.4 µs	1.6 µs

Note:
1. Value after reset.

Bits TCS50 to TCS53 (Period 5 Cycle Count Select Bits)

These bits are used to set the number of cycles for period 5.

Table 21.7 Period 5 Cycle Example (1)

Count Source Frequency	1 Cycle	2 Cycles (1)	3 Cycles	4 Cycles	5 Cycles	6 Cycles	7 Cycles	8 Cycles
4 MHz	250 ns	500 ns	750 ns	1.0 µs	1.25 µs	1.5 µs	1.75 µs	2.0 µs
5 MHz	200 ns	400 ns	600 ns	800 ns	1.0 µs	1.2 µs	1.4 µs	1.6 µs

Note:
1. Value after reset.

Table 21.8 Period 5 Cycle Example (2)

Count Source Frequency	9 Cycles	10 Cycles	11 Cycles	12 Cycles	13 Cycles	14 Cycles	15 Cycles	16 Cycles
4 MHz	2.25 µs	2.5 µs	2.75 µs	3.0 µs	3.25 µs	3.5 µs	3.75 µs	4.0 µs
5 MHz	1.8 µs	2.0 µs	2.2 µs	2.4 µs	2.6 µs	2.8 µs	3.0 µs	3.2 µs

21.2.6 SCU Timing Control Register 3 (SCTCR3)

Address 02C5h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	TCS63	TCS62	TCS61	TCS60
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TCS60	Period 6 cycle count select bit	b3 b2 b1 b0 0 0 0 0: 1cycle (after reset) 0 0 0 1: 2 cycles 0 0 1 0: 3 cycles 0 0 1 1: 4 cycles 0 1 0 0: 5 cycles 0 1 0 1: 6 cycles 0 1 1 0: 7 cycles 0 1 1 1: 8 cycles 1 0 0 0: 9 cycles 1 0 0 1: 10 cycles 1 0 1 0: 11 cycles 1 0 1 1: 12 cycles 1 1 0 0: 13 cycles 1 1 0 1: 14 cycles 1 1 1 0: 15 cycles 1 1 1 1: 16 cycles	R/W
b1	TCS61			R/W
b2	TCS62			R/W
b3	TCS63			R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b5	—			
b6	—			
b7	—			

Bits TCS60 to TCS63 (Period 6 Cycle Count Select Bits)

These bits are used to set the number of cycles for period 6 (after MAIN measurement).

Table 21.9 Period 6 Cycle Example (1)

Count Source Frequency	1 Cycle(1)	2 Cycles	3 Cycles	4 Cycles	5 Cycles	6 Cycles	7 Cycles	8 Cycles
4 MHz	250 ns	500 ns	750 ns	1.0 µs	1.25 µs	1.5 µs	1.75 µs	2.0 µs
5 MHz	200 ns	400 ns	600 ns	800 ns	1.0 µs	1.2 µs	1.4 µs	1.6 µs

Note:
1. Value after reset.

Table 21.10 Period 6 Cycle Example (2)

Count Source Frequency	9 Cycles	10 Cycles	11 Cycles	12 Cycles	13 Cycles	14 Cycles	15 Cycles	16 Cycles
4 MHz	2.25 µs	2.5 µs	2.75 µs	3.0 µs	3.25 µs	3.5 µs	3.75 µs	4.0 µs
5 MHz	1.8 µs	2.0 µs	2.2 µs	2.4 µs	2.6 µs	2.8 µs	3.0 µs	3.2 µs

21.2.7 SCU Channel Control Register (SCHCR)

Address 02C6h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	SCUMD	UPDOWN	—	—	—	CHC2	CHC1	CHC0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function		R/W
b0	CHC0	Channel select bit	[In single mode] b2 b1 b0 0 0 0: CH0 0 0 1: CH1 0 1 0: CH2 0 1 1: CH3 1 0 0: CH4 1 0 1: CH5 1 1 0: CH6 1 1 1: CH7	[In scan mode] b2 b1 b0 0 0 0: Do not set. 0 0 1: CH0 to CH1 0 1 0: CH0 to CH2 0 1 1: CH0 to CH3 1 0 0: CH0 to CH4 1 0 1: CH0 to CH5 1 1 0: CH0 to CH6 1 1 1: CH0 to CH7	R/W
b1	CHC1				R/W
b2	CHC2				R/W
b3	—	Reserved bit	Set to 0.		R/W
b4	—				
b5	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.			—
b6	UPDOWN	Scan ascending/ descending select bit	0: Ascending order 1: Descending order		R/W
b7	SCUMD	Measurement mode select bit	0: Single mode 1: Scan mode		R/W

21.2.8 SCU Channel Control Counter (SCUCHC)

Address 02C7h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	SCUCHC2	SCUCHC1	SCUCHC0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
b0	SCUCHC0	Counter used for channel control. The values of bits CHC0 to CHC2 in the SCHCR register are transferred in Status 2.	R
b1	SCUCHC1		R
b2	SCUCHC2		R
b3	—	Reserved bits. When read, the content is 0.	R
b4	—		
b5	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.	—
b6	—		
b7	—		

21.2.9 SCU Flag Register (SCUFR)

Address 02C8h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	SIF	—	—	—	MVF	EWMER	OVFER	DTSR
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	DTSR	Data transfer status flag	[Conditions for setting to 0] • When data transfer to RAM is completed. • Write 1 is written to the SCUINIT bit in the SCUCR0 register. (1) [Condition for setting to 1] • When data 1 is captured to the buffer. • When the primary counter overflows.	R
b1	OVFER	Overflow error flag	[Conditions for setting to 0] • Write 1 is written to the SCUINIT bit in the SCUCR0 register. (1) • Write is written 0 by a program. (1) [Condition for setting to 1] When the primary counter overflows.	R/W
b2	EWMER	Exit from wait mode error flag	[Conditions for setting to 0] • Write 1 is written to the SCUINIT bit in the SCUCR0 register. • Write 0 is written by a program. (1) [Condition for setting to 1] When the MCU exits wait mode during the measurement of the touch sensor in wait mode.	R/W
b3	MVF	SCU operation flag	0: Sensor control unit is stopped 1: Sensor control unit is in operation	R
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b5	—			
b6	—			
b7	SIF	SCU interrupt request flag	[Condition for setting to 0] Write is written 0 after read.(2) [Condition for setting to 1] When a measurement of the touch sensor is completed.	R/W

Notes:
1. When the SCSTRT bit in the SCUCR0 register is set to 0 (measurement stops), the DTSR bit is not set to 0.
2. The results of writing this bit are as follows.
   • If 1 is read, writing 0 to the same bit sets it to 0.
   • If 0 is read, writing 0 to the same bit does not change it. (If the bit changes from 0 to 1 after a 0 is read, it remains 1 even if 0 is written.)
   • The bit remains unchanged if 1 is written to it.

EWMER Bit (Exit from Wait Mode Error Flag)

This error flag indicates when the MCU exits wait mode during the measurement of the touch sensor in wait mode.

21.2.10 SCU Status Counter Register (SCUSTC)

Address 02C9h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	SSQ4	SSQ3	SSQ2	SSQ1	SSQ0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
b0	SSQ0	Status counter for the sensor control unit. The value changes to 00000b in the following cases: • When an interrupt request is acknowledged after a measurement of the touch sensor finishes. • Write 1 is written to the SCUINIT bit in the SCUCR0 register. When the SCSTRT bit in the SCUCR0 register is set to 0 (measurement stops), the value remains unchanged (the value does not change to 00000b).	R
b1	SSQ1		R
b2	SSQ2		R
b3	SSQ3		R
b4	SSQ4		R
b5	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.	—
b6	—		
b7	—		

21.2.11 SCU Secondary Counter Set Register (SCSCSR)

Address 02CAh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	SCSCS4	SCSCS3	SCSCS2	SCSCS1	SCSCS0
After Reset	0	0	0	0	0	1	1	1

Bit	Symbol	Function	R/W
b0	SCSCS0	Register for storing the setting value of the secondary counter.	R/W
b1	SCSCS1		R/W
b2	SCSCS2		R/W
b3	SCSCS3		R/W
b4	SCSCS4		R/W
b5	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.	—
b6	—		
b7	—		

21.2.12 SCU Secondary Counter Register (SCUSCC)

Address 02CBh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	SCUSCC4	SCUSCC3	SCUSCC2	SCUSCC1	SCUSCC0
After Reset	0	0	0	0	0	1	1	1

Bit	Symbol	Function	R/W
b0	SCUSCC0	5-bit increment counter. The value of the SCSCSR register is transferred in Status 3.	R
b1	SCUSCC1		R
b2	SCUSCC2		R
b3	SCUSCC3		R
b4	SCUSCC4		R
b5	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.	—
b6	—		
b7	—		

21.2.13 SCU Destination Address Register (SCUDAR)

Address 02CFh to 02CEh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	SCUDAR7	SCUDAR6	SCUDAR5	SCUDAR4	SCUDAR3	SCUDAR2	SCUDAR1	SCUDAR0
After Reset	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	SCUDAR11	SCUDAR10	SCUDAR9	SCUDAR8
After Reset	0	0	0	0	0	1	1	0

Bit	Symbol	Function	R/W
b0	SCUDAR0	Set the start address of the transfer destination.	R/W
b1	SCUDAR1		R/W
b2	SCUDAR2		R/W
b3	SCUDAR3		R/W
b4	SCUDAR4		R/W
b5	SCUDAR5		R/W
b6	SCUDAR6		R/W
b7	SCUDAR7		R/W
b8	SCUDAR8		R/W
b9	SCUDAR9		R/W
b10	SCUDAR10		R/W
b11	SCUDAR11		R/W
b12	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.	—
b13	—		
b14	—		
b15	—		

21.2.14 SCU Data Buffer Register (SCUDBR)

Address 02D1h to 02D0h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	SCUDBR7	SCUDBR6	SCUDBR5	SCUDBR4	SCUDBR3	SCUDBR2	SCUDBR1	SCUDBR0
After Reset	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	SCUDBR8
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
b0	SCUDBR0	Buffer register for storing data 1.	R
b1	SCUDBR1	After data 1 is fixed, the value of the primary counter is stored.	R
b2	SCUDBR2		R
b3	SCUDBR3		R
b4	SCUDBR4		R
b5	SCUDBR5		R
b6	SCUDBR6		R
b7	SCUDBR7		R
b8	SCUDBR8		R
b9	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.	—
b10	—		
b11	—		
b12	—		
b13	—		
b14	—		
b15	—		

21.2.15 SCU Primary Counter Register (SCUPRC)

Address 02D3h to 02D2h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	SCUPRC7	SCUPRC6	SCUPRC5	SCUPRC4	SCUPRC3	SCUPRC2	SCUPRC1	SCUPRC0
After Reset	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	SCUPRC8
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
b0	SCUPRC0	9-bit counter. The upper limit is 1FFh. If the counter overflows, the OVFER bit in the SCUFR register is set to 1, and the status proceeds to No.21.	R
b1	SCUPRC1		R
b2	SCUPRC2		R
b3	SCUPRC3		R
b4	SCUPRC4		R
b5	SCUPRC5		R
b6	SCUPRC6		R
b7	SCUPRC7		R
b8	SCUPRC8		R
b9	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.	—
b10	—		
b11	—		
b12	—		
b13	—		
b14	—		
b15	—		

21.2.16 SCU Random Value Store Register 0 (SCRVR0)

Address 02D4h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	RV013	RV012	RV011	RV010	RV003	RV002	RV001	RV000
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
b0	RV000	Bits used for storing random value 0.	R/W
b1	RV001		R/W
b2	RV002		R/W
b3	RV003		R/W
b4	RV010	Bits used for storing random value 1.	R/W
b5	RV011		R/W
b6	RV012		R/W
b7	RV013		R/W

21.2.17 SCU Random Value Store Register 1 (SCRVR1)

Address 02D5h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	RV033	RV032	RV031	RV030	RV023	RV022	RV021	RV020
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
b0	RV020	Bits used for storing random value 2.	R/W
b1	RV021		R/W
b2	RV022		R/W
b3	RV023		R/W
b4	RV030	Bits used for storing random value 3.	R/W
b5	RV031		R/W
b6	RV032		R/W
b7	RV033		R/W

21.2.18 SCU Random Value Store Register 2 (SCRVR2)

Address 02D6h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	RV053	RV052	RV051	RV050	RV043	RV042	RV041	RV040
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
b0	RV040	Bits used for storing random value 4.	R/W
b1	RV041		R/W
b2	RV042		R/W
b3	RV043		R/W
b4	RV050	Bits used for storing random value 5.	R/W
b5	RV051		R/W
b6	RV052		R/W
b7	RV053		R/W

21.2.19 SCU Random Value Store Register 3 (SCRVR3)

Address 02D7h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	RV073	RV072	RV071	RV070	RV063	RV062	RV061	RV060
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
b0	RV060	Bits used for storing random value 6.	R/W
b1	RV061		R/W
b2	RV062		R/W
b3	RV063		R/W
b4	RV070	Bits used for storing random value 7.	R/W
b5	RV071		R/W
b6	RV072		R/W
b7	RV073		R/W

21.2.20 SCU Random Value Store Register 4 (SCRVR4)

Address 02D8h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	RV093	RV092	RV091	RV090	RV083	RV082	RV081	RV080
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
b0	RV080	Bits used for storing random value 8.	R/W
b1	RV081		R/W
b2	RV082		R/W
b3	RV083		R/W
b4	RV090	Bits used for storing random value 9.	R/W
b5	RV091		R/W
b6	RV092		R/W
b7	RV093		R/W

21.2.21 SCU Random Value Store Register 5 (SCRVR5)

Address 02D9h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	RV113	RV112	RV111	RV110	RV103	RV102	RV101	RV100
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
b0	RV100	Bits used for storing random value 10.	R/W
b1	RV101		R/W
b2	RV102		R/W
b3	RV103		R/W
b4	RV110	Bits used for storing random value 11.	R/W
b5	RV111		R/W
b6	RV112		R/W
b7	RV113		R/W

21.2.22 SCU Random Value Store Register 6 (SCRVR6)

Address 02DAh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	RV133	RV132	RV131	RV130	RV123	RV122	RV121	RV120
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
b0	RV120	Bits used for storing random value 12.	R/W
b1	RV121		R/W
b2	RV122		R/W
b3	RV123		R/W
b4	RV130	Bits used for storing random value 13.	R/W
b5	RV131		R/W
b6	RV132		R/W
b7	RV133		R/W

21.2.23 SCU Random Value Store Register 7 (SCRVR7)

Address 02DBh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	RV153	RV152	RV151	RV150	RV143	RV142	RV141	RV140
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
b0	RV140	Bits used for storing random value 14.	R/W
b1	RV141		R/W
b2	RV142		R/W
b3	RV143		R/W
b4	RV150	Bits used for storing random value 15.	R/W
b5	RV151		R/W
b6	RV152		R/W
b7	RV153		R/W

21.2.24 SCU Input Enable Register 0 (TSIER0)

Address 02DCh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CH07E	CH06E	CH05E	CH04E	CH03E	CH02E	CH01E	CH00E
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CH00E	CH0 enable bit	0: Disabled (used as an I/O port) 1: Enabled (used as a touch sensor pin)	R/W
b1	CH01E	CH1 enable bit		R/W
b2	CH02E	CH2 enable bit		R/W
b3	CH03E	CH3 enable bit		R/W
b4	CH04E	CH4 enable bit		R/W
b5	CH05E	CH5 enable bit		R/W
b6	CH06E	CH6 enable bit		R/W
b7	CH07E	CH7 enable bit		R/W

The TSIER0 register is enabled when the SCUE bit in the SCUCR0 register is set to 1 (operation enabled).
In scan mode, for the CH range set by the CHCi bit (i = 0 to 2) in the SCHCR register, even when a corresponding enable bit is disabled, the bit is measured and its data is stored. However, the data is invalid.

21.3 Functional Description

21.3.1 Common Items for Multiple Modes

21.3.1.1 Status Counter

The status counter operation is divided into the measurement STEP1 and STEP2. When “L” at CHxA is detected in measurement STEP1, the counter proceeds to the measurement STEP2. There are variable periods to improve the accuracy of measurement. This status counter operates (repeating status 0 to status 23) for each measurement in each channel.
Figure 21.3 shows the Status Operation Transitions and Table 21.11 lists the Status Operations.

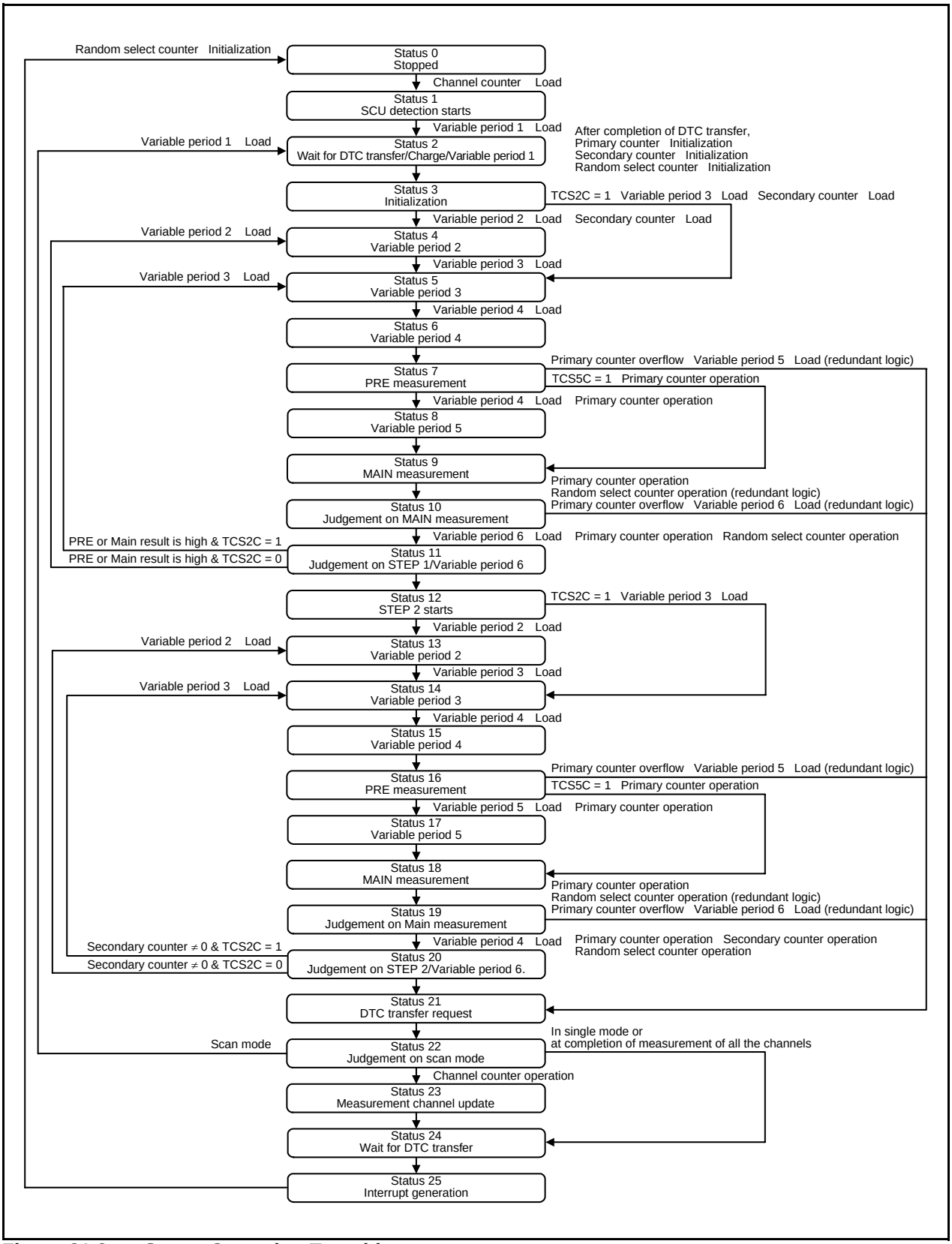


Figure 21.3 Status Operation Transitions

Table 21.11 Status Operations

	Status Counter					Status	Pin State			Re-peat	Operation
	SSQ4	SSQ3	SSQ2	SSQ1	SSQ0		CHxC	CHxB	CHxA		
	0	0	0	0	0	0	Hi-Z	Hi-Z	Hi-Z		Stopped, initial setting
	0	0	0	0	1	1	Hi-Z	Hi-Z	Hi-Z		Transfer of setting values
	0	0	0	1	0	2	“H”	Hi-Z	Hi-Z		Variable period 1 (1 to 128 cycles) selected by bits TCS10 to TCS16, charging period
	0	0	0	1	1	3	Hi-Z	Hi-Z	Hi-Z		Initialization
Measurement STEP 1	0	0	1	0	0	4	Hi-Z	Hi-Z	“L”		Variable period 2 (1 to 16 cycles) selected by bits TCS20 toTCS23 Can be skipped by the TCS2C bit
	0	0	1	0	1	5	Hi-Z	“L”	“L”		Variable period 3 (1 to 4 cycles) selected by bits TCS30 and TCS31
	0	0	1	1	0	6	Hi-Z	Hi-Z	Hi-Z		Variable period 4 (1 to 8 cycles) selected by bits TCS40 to TCS42 CHxB-CHxC short can be turned ON by the BCSHORT bit
	0	0	1	1	1	7	Hi-Z	Hi-Z	Hi-Z		Dummy cycle
	0	1	0	0	0	8	Hi-Z	Hi-Z	Hi-Z		Variable period 5 (1 to 16 cycles) selected by bits TCS50 to TCS53 Can be skipped by the TCS5C bit
	0	1	0	0	1	9	Hi-Z	Hi-Z	Hi-Z		MAIN measurement period
	0	1	0	1	0	10	Hi-Z	Hi-Z	Hi-Z		Judging period for MAIN measurement
	0	1	0	1	1	11	Hi-Z	Hi-Z	Hi-Z		Variable period 6 (1 to16 cycles) selected by bits TCS60 to TCS63 CHxB-CHxC short can be turned OFF by the BCSHORT bit
	0	1	1	0	0	12	Hi-Z	Hi-Z	Hi-Z		Dummy cycle
Measurement STEP 2	0	1	1	0	1	13	Hi-Z	Hi-Z	“L”		Variable period 2 (1 to 16 cycles) selected by bits TCS20 to TCS23 Can be skipped by the TCS2C bit
	0	1	1	1	0	14	Hi-Z	“L”	“L”		Variable period 3 (1 to 4 cycles) selected by bits TCS30 and TCS31
	0	1	1	1	1	15	Hi-Z	Hi-Z	Hi-Z		Variable period 4 (1 to 8 cycles) selected by bits TCS40 to TCS42 CHxB-CHxC short can be turned ON by the BCSHORT bit
	1	0	0	0	0	16	Hi-Z	Hi-Z	Hi-Z		Dummy cycle
	1	0	0	0	1	17	Hi-Z	Hi-Z	Hi-Z		Variable period 5 (1 to 16 cycles) selected by bits TCS50 to TCS53 Can be skipped by the TCS5C bit
	1	0	0	1	0	18	Hi-Z	Hi-Z	Hi-Z		MAIN measurement period
	1	0	0	1	1	19	Hi-Z	Hi-Z	Hi-Z		Judging period for MAIN measurement
	1	0	1	0	0	20	Hi-Z	Hi-Z	Hi-Z		Judging of the secondary counter value (n = 0?) Variable period 6 (1 to16 cycles) selected by bits TCS60 to TCS63 CHxB-CHxC short can be turned OFF by the BCSHORT bit
	1	0	1	0	1	21	Hi-Z	Hi-Z	Hi-Z		DTC activation request or SDMA transfer request
	1	0	1	1	0	22	Hi-Z	Hi-Z	Hi-Z		
	1	0	1	1	1	23	Hi-Z	Hi-Z	Hi-Z		Branch to check whether all the channels selected by bits CHC0 to CHC4 are measured
	1	1	0	0	0	24	Hi-Z	Hi-Z	Hi-Z		Wait until data transfer to RAM is completed
	1	1	0	0	1	25	Hi-Z	Hi-Z	Hi-Z		Sensor control unit interrupt generated
	0	0	0	0	0	0	Hi-Z	Hi-Z	Hi-Z		End

BCSHORT: Bit in SCUCR0 register
TCS10 to TCS16, TCS2C: Bits in SCTCR0 register
TCS20 to TCS23, TCS30, TCS31: Bits in SCTCR1 register
TCS40 to TCS42, TCS5C, TCS50 to TCS53: Bits in SCTCR2 register
TCS60 to TCS63: Bits in SCTCR3 register
CHC0 to CHC2: Bits in SCHCR register

21.3.1.2 Adjustment of Status Periods

The timing of the status periods can be adjusted as shown in Figure 21.4.

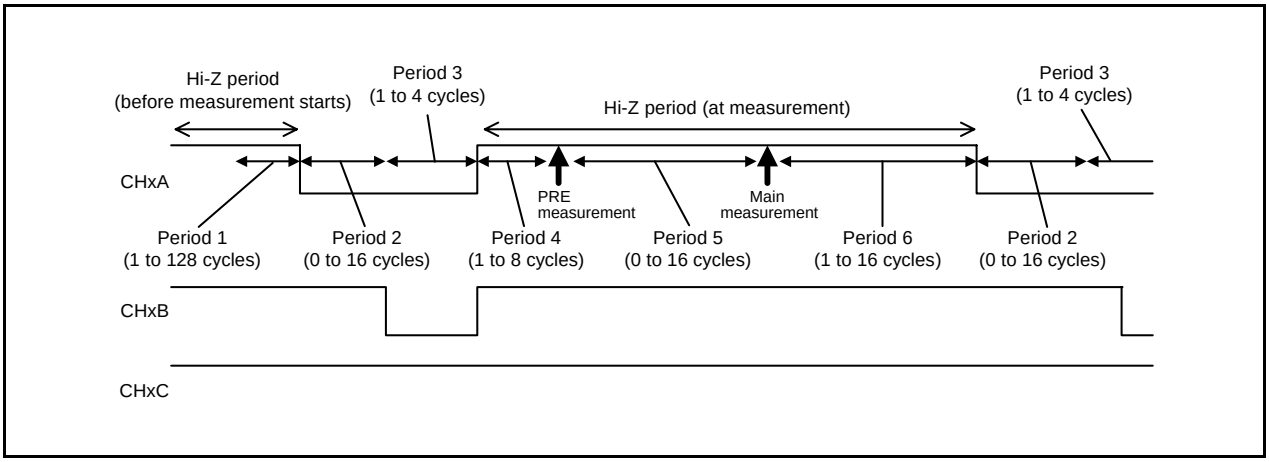


Figure 21.4 Adjustment of Status Periods

21.3.1.3 PRE Measurement Specifications

Turning PRE measurement ON/OFF is controlled by the PREMSR bit in the SCUMR register.

When the PREMSR bit is set to 1 (PRE measurement), the measurement result of PRE measurement is reflected in the primary counter. When the PREMSR bit is set to 0 (no PRE measurement), the measurement result is not reflected in the primary counter.

The random measurement function and the majority measurement function are not used in PRE measurement.

21.3.1.4 MAIN Measurement Specifications

Random measurement and majority measurement are controlled by the SCUMR register.

- Random measurement
  Turning random measurement ON/OFF is controlled by the RANDOM bit in the SCUMR register.
  When the RANDOM bit is set to 1 (RANDOM measurement), measurement timing is sequentially switched by the random value store registers (SCRVR0 to SCRVR7) to perform measurement.

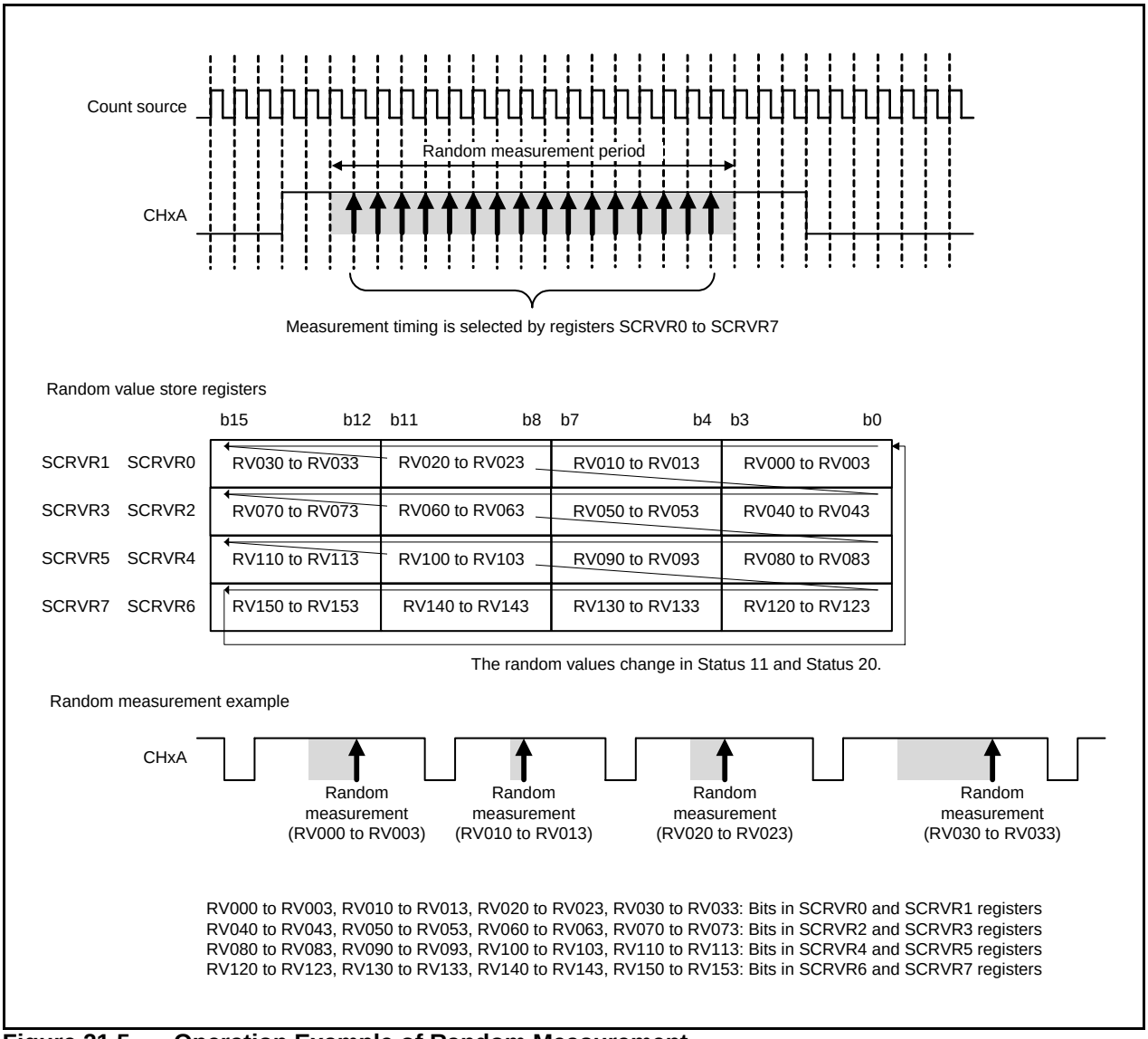


Figure 21.5 Operation Example of Random Measurement

- Majority measurement
  The number of majority measurements is controlled by bits MJNUM0 to MJNUM2 in the SCUMR register. When bits MJNUM0 to MJNUM2 are set to all 0, majority measurement is not performed.

Table 21.12 Number of Measurements during Majority Measurement

MJNUM2	MJNUM1	MJNUM0	Number of Measurements
0	0	0	No majority measurement (measured once)
0	0	1	Measured 3 times
0	1	0	Measured 5 times
0	1	1	Measured 7 times
1	0	0	Measured 9 times
1	0	1	Measured 11 times
1	1	0	Measured 13 times
1	1	1	Measured 15 times

MJNUM0 to MJNUM2: Bits in SCUMR register

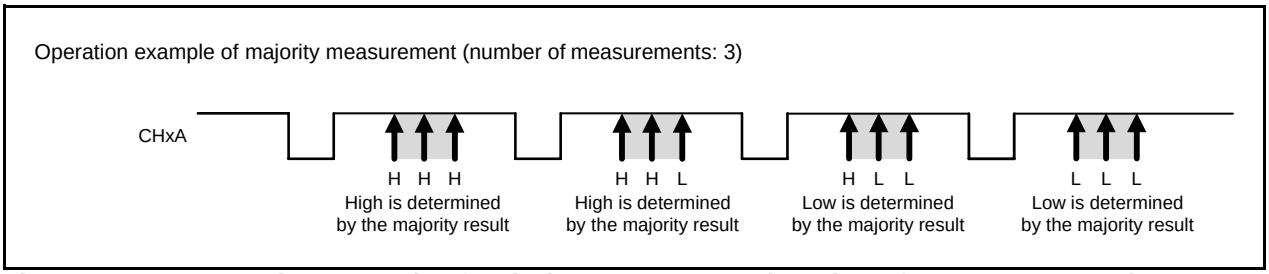


Figure 21.6 Operation Example of Majority Measurement (Number of Measurements: 3)

- Combinations of random measurement and majority measurement
  Random measurement and majority measurement can be combined to perform measurement.
  During random measurement, the measurement period depends on the random value, but it can be fixed by the CONST bit in the SCUMR register.

Table 21.13 Measurement Combinations during MAIN Measurement

RANDOM	MJNUM2 to MJNUM0	CONST	MAIN Measurement Specifications
0	000b	—	No random measurement, no majority measurement
	Other than 000b	—	Majority measurement
1	000b	0	Random measurement (the measurement period depends on the random value)
		1	Random measurement (the measurement period is fixed to 16 cycles)
	Other than 000b	0	Random measurement (the measurement period depends on the random value), majority measurement
		1	Random measurement (the measurement period is set to 16 cycles + the number of measurements), majority measurement

RANDOM: Bit in SCUMR register
MJNUM0 to MJNUM2: Bits in SCUMR register
CONST: Bit in SCUMR register

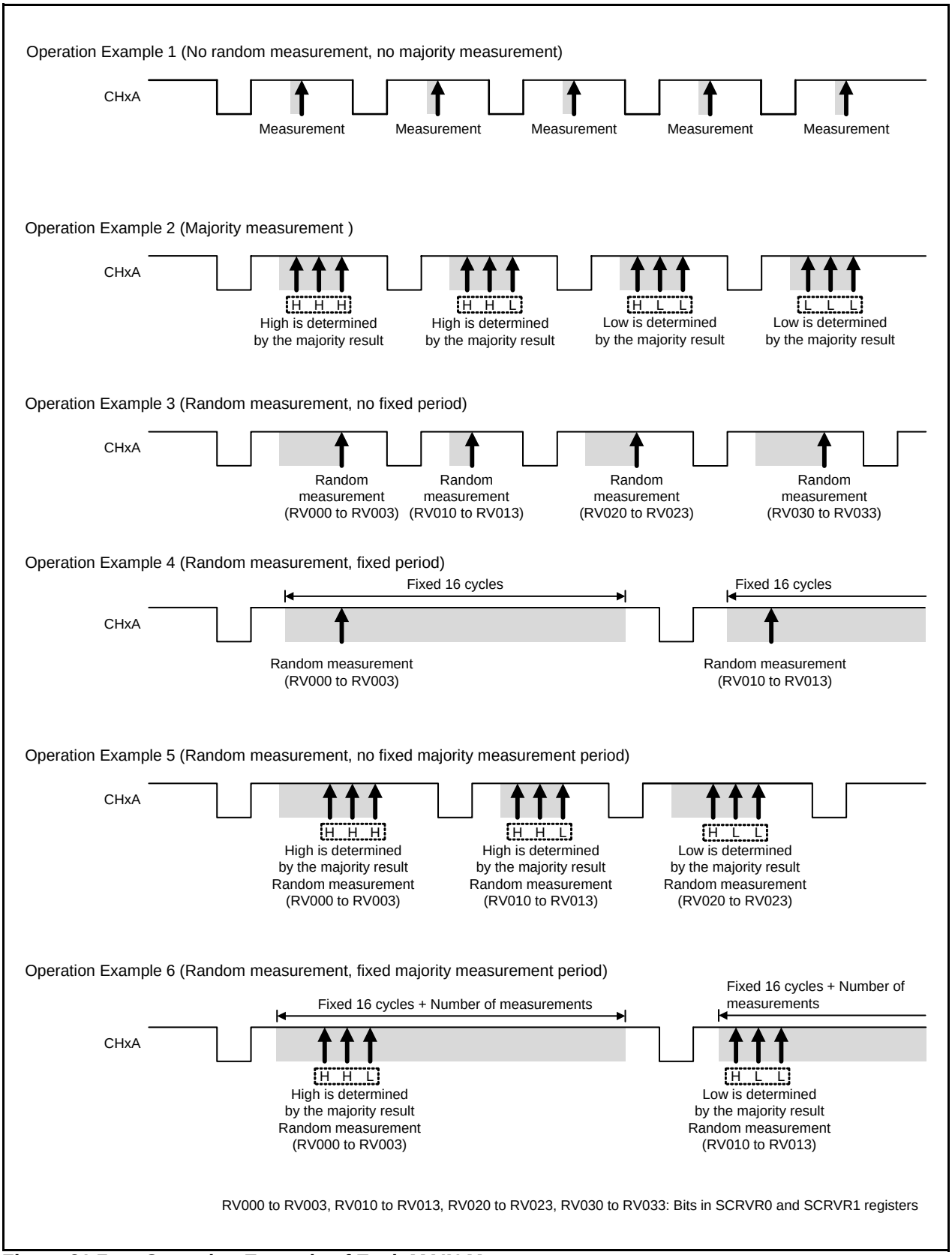


Figure 21.7 Operation Example of Each MAIN Measurement

21.3.1.5 Counter Operation

The primary counter is a 9-bit up counter and the secondary counter is a 5-bit up/down counter.
The primary counter increments when a high level is detected at the CMOS input to CHxA while each channel is measured.
Two types of measurement data, the primary counter value when a low level is detected at CHxA for the first time (data 1 hereafter) and the primary counter value when the secondary counter value reaches 0 (data 2 hereafter), are stored in the register.
This secondary counter is activated in measurement STEP 2, and decrements from the value set by bits SCSCS0 to SCSCS4 in the SCUSCS register when a low level is detected and increments when a high level is detected. However, the counter does not increment any value exceeding the value set by bits SCSCS0 to SCSCS4.
The PRE and MAIN measurement results are reflected in the primary counter.
Only the MAIN measurement result is reflected in the secondary counter.
The conditions for transition from measurement STEP 1 to measurement STEP 2 are as follows:

- The MAIN measurement result is determined to be low when PRE measurement is turned OFF.
- The PRE measurement result is determined to be low and the MAIN measurement result is determined to be low when PRE measurement is turned ON.

Table 21.14 Image of Counter Operation and Measurement Data when PRE Measurement is Turned OFF

	MAIN Judging Value	Primary Counter Value	Secondary Counter Value	
Measurement STEP 1	H	95	7	
	H	96	7	
	H	97	7	
	H	98	7	
	H	99	7	
	L	99	7	← Data 1
Measurement STEP 2	L	99	6	
	H	100	7	
	H	101	7	
	H	102	7	
	H	103	7	
	H	104	7	
	H	105	7	
	H	106	7	
	L	106	6	
	L	106	5	
	L	106	4	
	L	106	3	
	L	106	2	
	L	106	1	
	L	106	0	← Data 2

: Transition to measurement STEP 2 when the first MAIN judging value is low
: Measurement data

Table 21.15 Image of Counter Operation and Measurement Data when PRE Measurement is Turned ON

	PRE Measurement Judging Value	MAIN Measurement Judging Value	Primary Counter Value	Secondary Counter Value	
Measurement STEP 1	H	H	95	7	
	H	L	96	7	
	L	H	97	7	
	H	H	99	7	
	H	H	101	7	
	L	L	101	7	← Data 1
Measurement STEP 2	L	L	101	6	
	L	H	102	7	
	H	L	103	6	
	H	H	105	7	
	H	H	107	7	
	H	H	109	7	
	H	H	111	7	
	H	H	113	7	
	L	L	113	6	
	L	L	113	5	
	L	L	113	4	
	L	L	113	3	
	L	L	113	2	
	L	L	113	1	
	L	L	113	0	← Data 2

: Transition to measurement STEP 2 when the first PRE judging value is low and the MAIN judging value is low

: Measurement data

The PRE and MAIN measurement values are reflected in the primary counter.
Only the MAIN measurement value is reflected in the secondary counter.

21.3.1.6 Measurement Data

Table 21.14 shows the Image of Counter Operation and Measurement Data when PRE Measurement is Turned OFF. Table 21.15 shows the Image of Counter Operation and Measurement Data when PRE Measurement is Turned ON.

In measurement STEP 1, the primary counter values when a low level is detected for the first time are stored in bits SCUDBR0 to SCUDBR8 in the SCUDBR register (data 1).

In measurement STEP 2, the primary counter values when the secondary counter value reaches 0 are stored in bits SCUPRC0 to SCUPRC8 in the SCUPRC register (data 2). Stored data 1 and data 2 are transferred as the measurement data to RAM using the DTC or SDMA in Status 22.

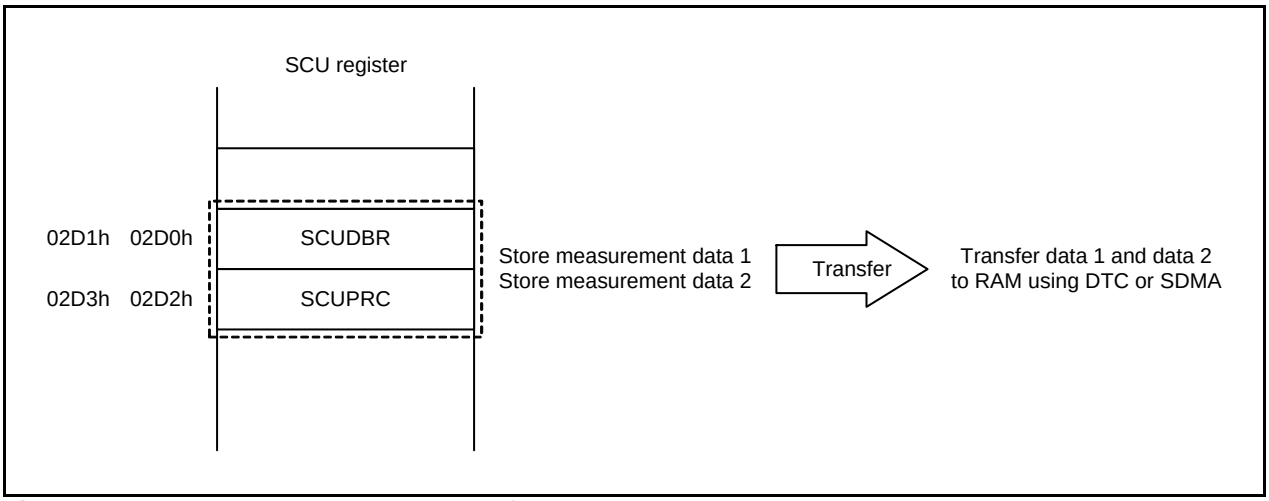


Figure 21.8 Measurement Data Transfer

21.3.1.7 Measurement Channels

For CHxA, CHxB, and CHxC, and target channels from CH0 to CH7, set the corresponding direction bits in the PD1 register to 0 (input mode). However, note that the content of the corresponding port bit in the Pi register is undefined.
Touches are detected at the CHxA (P0_2) pin. Set the threshold value for touch detection using bits VLT00 and VLT01 in the VLT0 register. For details of the I/O port settings, refer to **7. I/O Ports**.

21.3.1.8 Interrupt Generation

An interrupt request signal is output to the control block in Status 26 after measurement of all the channels finishes.
Interrupt requests are acknowledged or disabled in the interrupt control block.
Clearing of an interrupt request signal is controlled by the SIF bit in the SCUFR register.
Refer to **21.2.9 SCU Flag Register (SCUFR)** for details of the SCUFR register.

21.3.1.9 Touch Detection Start Conditions

- Software Trigger
  When bits SCCAP1 to SCCAP0 in the SCUMR register are set to 00b, a software trigger is selected. Detection starts when the SCSTRT bit in the SCUCR0 register is set to 1 (measurement starts).

- Trigger from Timer RC
  When bits SCCAP1 to SCCAP0 in the SCUMR register are set to 10b, a measurement start trigger from timer RC is selected.
  To use the measurement start trigger from timer RC, make the following settings:
  - Set bits SCCAP1 to SCCAP0 in the SCUMR register to 10b (measurement start trigger from timer RC).
  - Use timer RC in the output compare function (timer mode, PWM mode, or PWM2 mode).
  - Set the ADTRGjE bit (j = A, B, C, or D) in the TRCSCUCR register to 1 (SCU trigger occurs at compare match between TRC and TRCGRj register).
  - Set the SCSTRT bit in the SCUCR0 register to 1 (measurement starts).

  After making the above settings, touch detection starts when the IMFj bit in the TRCSR register changes from 0 to 1.
  For details of the timer RC output compare function (timer mode, PWM mode, or PWM2 mode), refer to **19. Timer RC**, **19.5 Timer Mode (Output Compare Function)**, **19.6 PWM Mode**, and **19.7 PWM2 Mode**.

- External Trigger
  When bits SCCAP1 to SCCAP0 in the SCUMR register are set to 11b, an external trigger ($\overline{\text{SCUTRG}}$) is selected.
  To use the external trigger ($\overline{\text{SCUTRG}}$), make the following settings:
  - Set bits SCCAP1 to SCCAP0 in the SCUMR register to 11b (external trigger ($\overline{\text{SCUTRG}}$)).
  - Set the INT3EN bit in the INTEN register to 1 (enabled).
  - Set the PD3_3 bit in the PD3 register to 0 (input mode).
  - Set the SCSTRT bit in the SCUCR0 register to 1 (measurement starts).

  After making the above settings, touch detection starts when the input to the $\overline{\text{SCUTRG}}$ pin is changed from “H” to “L”.

21.3.2 Sensor Control Unit Specifications and Operation Example

Table 21.16 lists the Sensor Control Unit Specifications.

Table 21.16 Sensor Control Unit Specifications

Item		Specification
Operating clock (count source)		f1, f2, or f4 (Set the operating clock for the sensor control unit to 4 MHz or 5 MHz.)
Pins	Touch detection	8 channels (CH0 to CH7)
	System pins	3 channels (CHxA, CHxB, and CHxC)
Measurement modes	Single mode	Touches are detected on any single channel. • Set the SCUMD bit in the SCHCR register to 0. • Select any channel with bits CHC0 to CHC2 in the SCHCR register. • Enable the channels to be measured by setting the corresponding enable bits in the TSIER0 register to 1 (enabled).
	Scan mode	Touches are detected on multiple channels. Ascending or descending can be selected as the channel scan order. • Set the SCUMD bit in the SCHCR register to 1. • Select 0 (ascending order) or 1 (descending order) with the UPDOWN bit in the SCHCR register. • Determine the maximum number of channels arbitrarily selected bits CHC0 to CHC2 in the SCHCR register. • Enable the channels to be measured by setting the corresponding enable bits in the TSIER0 register to 1 (enabled).
Number of detections		One time
Detection threshold value		Touches are detected at the CHxA pin. • Set the detection threshold value using bits VLT00 and VLT01 in the VLT0 register.
Detection data transfer method	During CPU operation	Transfer via the DTC Refer to **15. DTC** for the settings.
	In wait mode	Transfer via the SDMA in the sensor control unit
Detection start conditions		• Software trigger • Measurement start trigger from timer RC • External trigger ($\overline{\text{SCUTRG}}$)
Detection stop conditions		• When an interrupt request is generated after touch detection and data transfer are completed. • Set the SCSTRT bit in the SCUCR0 register to 0 by a program. (If detection is stopped by a program, the value of each counter is retained and not changed to the value after reset.)

21.3.2.1 Operation Example

A detection operation example of the sensor control unit is shown in Figure 21.9.
Detecting “L” at CHxA for the first time leads to transition from the measurement STEP1 to STEP2. The secondary counter operates after the transition to the measurement STEP2.

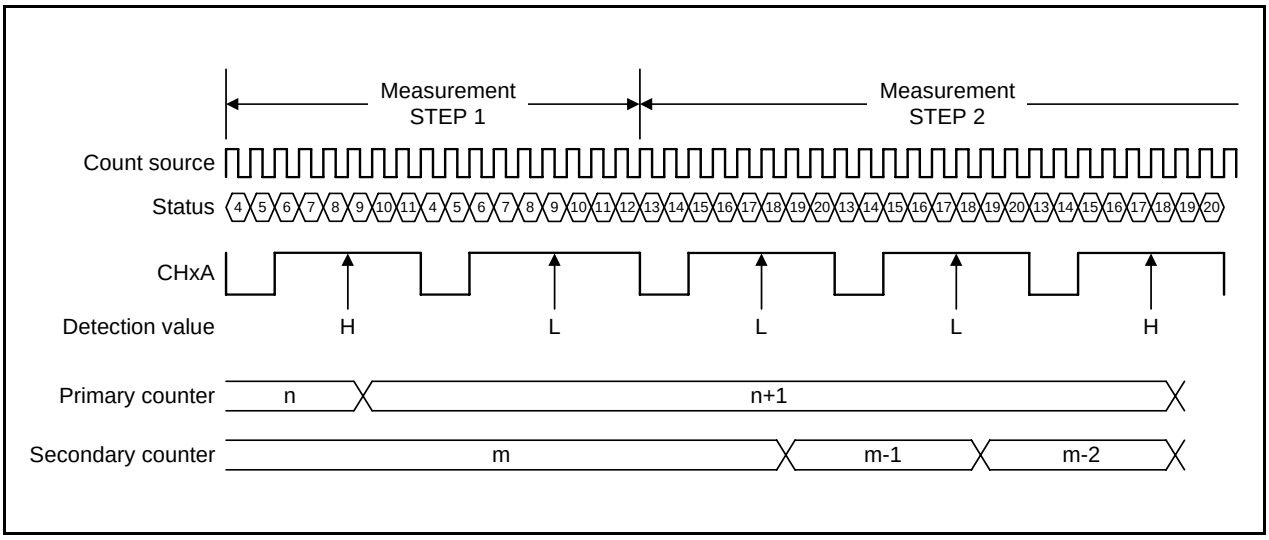


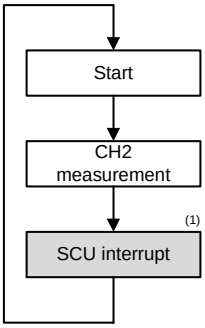
Figure 21.9 Sensor Control Unit Detection Operation Example

21.3.2.2 Measurement Mode Operation Examples

The touch sensor control unit supports two types of measurement mode: single mode and scan mode. Figure 21.10 shows a Measurement Mode Operation Examples.

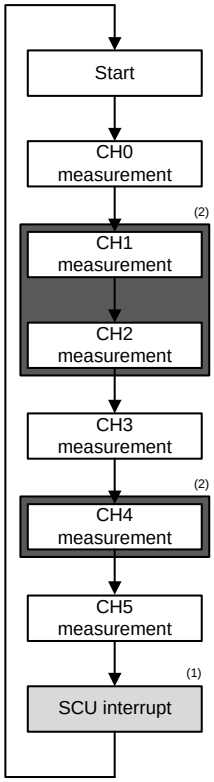
When detecting CH2 only

[Setting]
- Select single mode (SCUMD = 0)
- Set the enable bit (CH02E) for CH2 to 1 (enabled)
- Set bits CHC2 to CHC0 to 010b (2) to select CH2



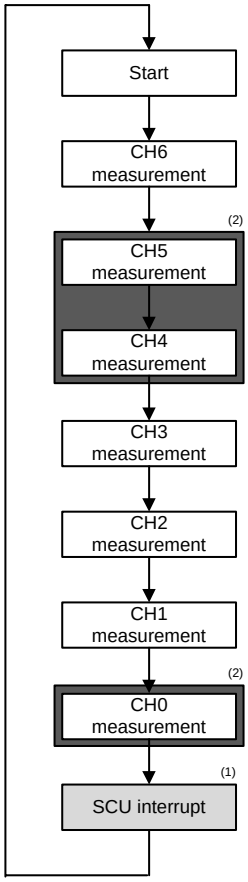
When detecting CH0, CH3, and CH5 in ascending order

[Setting]
- Select scan mode (SCUMD = 1)
- Set the enable bits (CHxxE) for CH0, CH3, and CH5 to 1 (enabled)
- Set CHC2 to CHC0 to 101b (5) to set the maximum CH value to CH5
- Set ascending order (UPDOWN = 0)



When detecting CH1 to CH3, and CH6 in descending order

[Setting]
- Select scan mode (SCUMD = 1)
- Set the enable bits (CHxxE) for CH1 to CH3, and CH6 to 1 (enabled)
- Set CHC2 to CHC0 to 110b (6) to set the maximum CH value to CH6
- Set descending order (UPDOWN = 1)



Notes:
1. An interrupt request to the interrupt control block is sent after the final data transfer is completed (in Status 26).
2. Sections shown in dark shade:

   Process the measurement value as invalid data.

Figure 21.10 Measurement Mode Operation Examples

21.4 Principles of Measurement Operation

Figure 21.11 shows the Measurement Circuit. The measurement operation principles of the sensor touch control unit are explained below.
As shown in Figure 21.11, the operation is described with resistors and capacitors inserted.

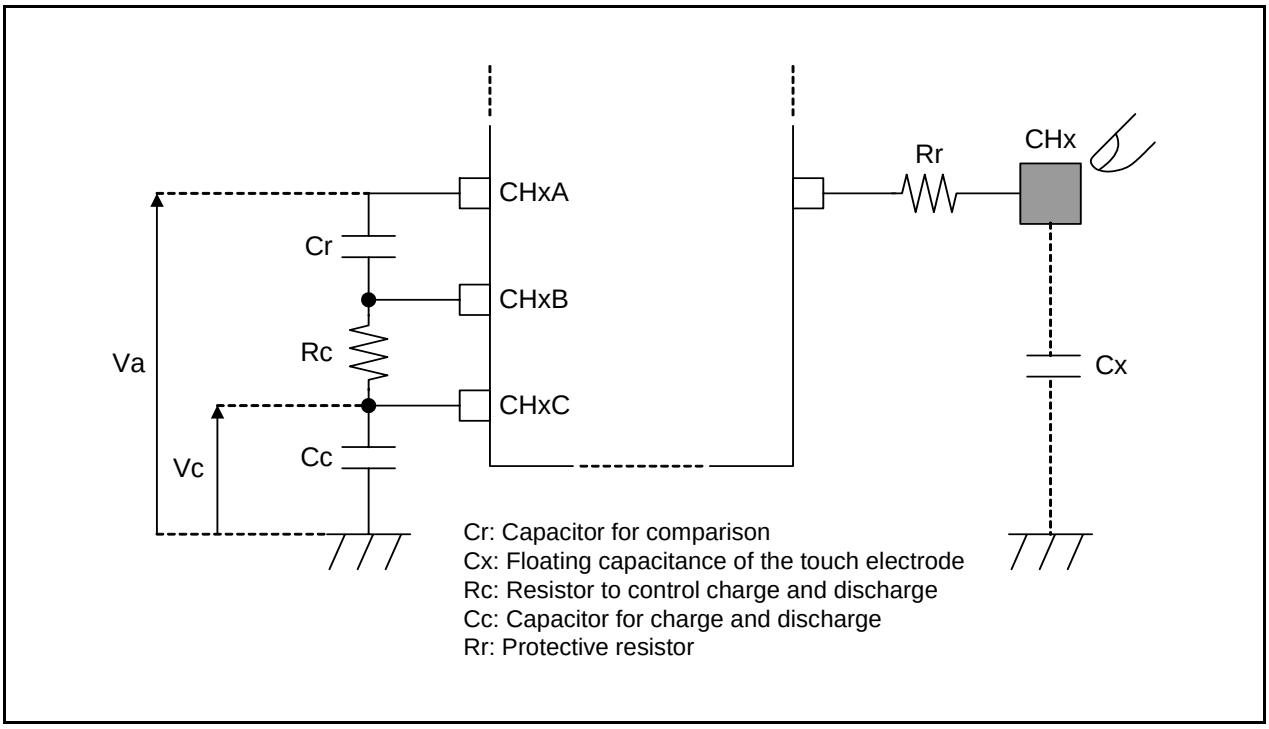


Figure 21.11 Measurement Circuit

The capacitance of the touch electrode is measured by measuring the voltage at CHxA while gradually discharging the electric charge stored in Cc. Measurement is performed using the following procedure.

(1) Charge Cc by connecting the CHxC pin to the voltage supply (VCC).
(2) After charging Cc fully, discharge Cc by connecting pins CHxA and CHxB to the ground level (VSS).
(3) After discharging Cc for a short period of time, keep pins CHxA and CHxB at high-impedance (Hi-Z), and measure the voltage at the CHxA pin. At this point, as shown in Figure 21.11, when the voltage measured at the CHxA pin is Va, and the voltage measured at the CHxC pin is Vc, Va at the time of voltage measurement is expressed by the following formula (A).
The Time-dependent Variation of Va and Vc is shown in Figure 21.12.

$$Va = \frac{Cr}{Cr + Cx} Vc \quad \ldots\ldots \text{formula (A)}$$

(4) Repeat steps (2) and (3).
(5) Set an input level for the CHxA pin using the VLT0 register (input threshold value control register 0).
Count the number of discharges before Va falls below the input threshold value. Continue counting until the secondary counter reaches 0.
(6) The count value is comprised of the primary counter value of data 1 and data 2.

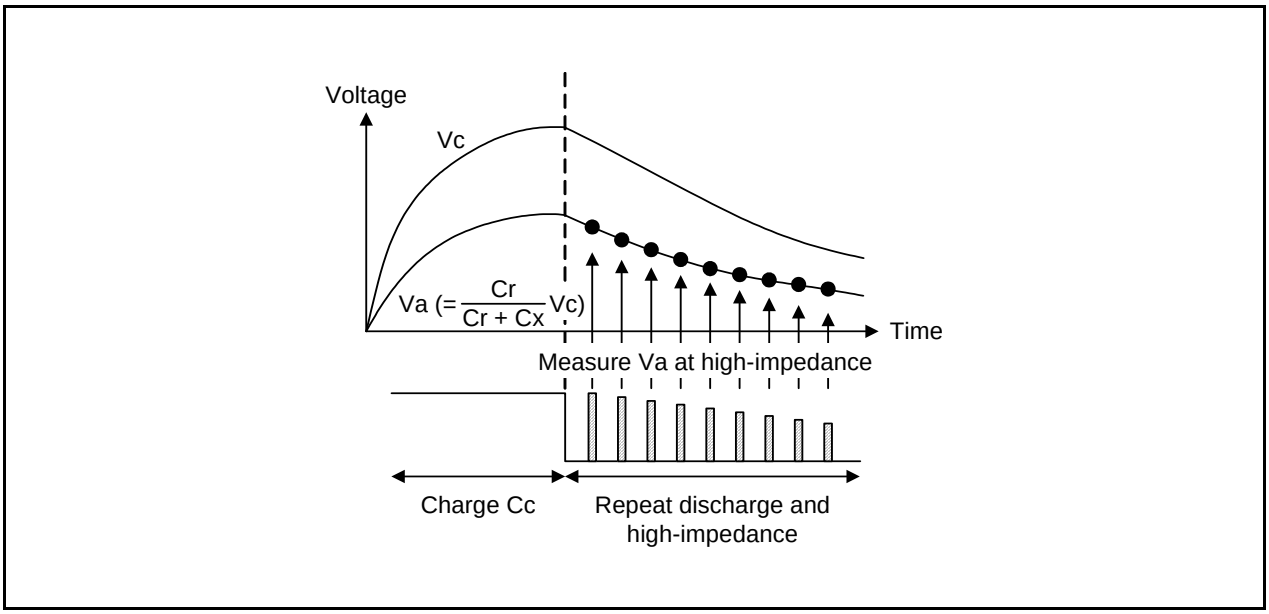


Figure 21.12 Time-dependent Variation of Va and Vc

As the finger comes closer to the touch electrode, a change of ⊿Cx is generated and Va is expressed by the following formula (B).

$$Va = \frac{Cr}{Cr + Cx + \Delta Cx} Vc \quad \ldots\ldots \text{formula (B)}$$

As a result, as shown in Figure 21.13, the voltage level at the CHxA pin changes and the count value gets smaller. The sensor control unit detects this difference to implement touch detection.

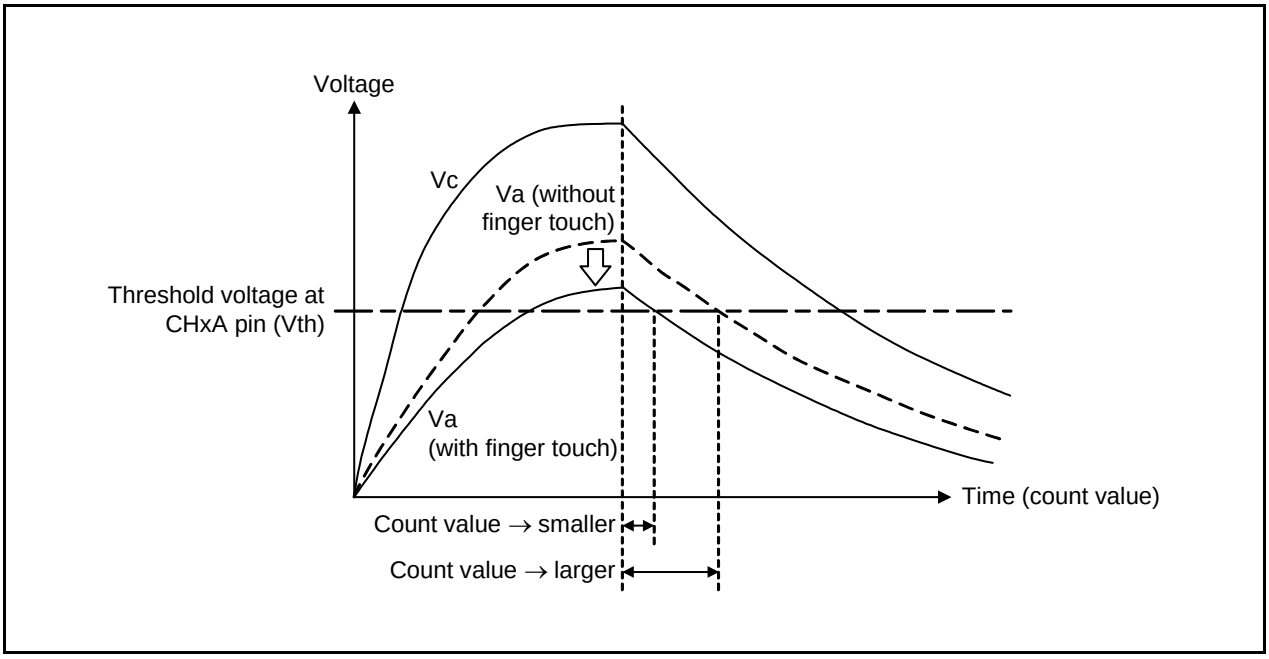


Figure 21.13 Variation of Measured Value with and without Finger Touch

21.5 Notes on Sensor Control Unit

21.5.1 Address to Store Detection Data

Set the start address in the SCUDAR register.
Also set the same start address in the DTDARj (j = 0 to 23) register of the DTC.
After measurement of each channel finishes, the values of data 1 and data 2 stored in the SFRs are transferred to RAM using the DTC or SDMA.
Use the DTC so that a total of 32 bits from registers SCUDBR and SCUPRC are transferred as measurement data by a single DTC transfer request in Status 22.
During DTC transfer from the sensor control unit, set the transfer mode to repeat mode (set the MODE bit in the DTCCRj register (j = 0 to 23) to 1) and disable interrupt generation (set the RPTINT bit in the DTCCRj register (j = 0 to 23) to 0).

21.5.2 Measurement Trigger

- If a measurement start trigger is generated during forced stop, all counter values change to 0.
- The measurement start trigger is recognized when bits SCCAP1 to SCCAP0 in the SCUMR register are set from 10b (measurement start trigger from timer RC) to 11b (external trigger ($\overline{\text{SCUTRG}}$) while the $\overline{\text{SCUTRG}}$ pin is held “L” during measurement operation.

21.5.3 Charging Time

To prevent measurement data from being overwritten to the next measurement data, the sensor control unit should be kept charged until DTC transfer or internal SDMA transfer is completed.

21.5.4 SCU Module Standby

The clock supply to the sensor control unit module can be stopped by setting the sensor control unit to module standby mode.
Since the clock supply to the registers in the sensor control unit is also stopped, cancel standby mode and allow at least two cycles to elapse before changing the settings of these registers.
Perform the same processing when stopping all clocks (when setting the CM1_0 bit in the CM register to 1).

21.5.5 SCU Initialization (SCINIT)

To initialize the sensor control unit by setting the SCINIT bit in the SCUCR0 register to 1, perform the following processing:
- Stop measurement (set the SCSTRT bit in the SCUCR0 register to 0)
- Do not output a SCU interrupt request (read the SIF bit in the SCUFR register as 0) or clear the SCU interrupt request (read the SIF bit as 1 and then write 0 to the same bit).

The DTC is not initialized by initialization using the SCINIT bit.
When initializing the touch sensor control unit, also make the required DTC settings.

21.5.6 Restrictions on Clock Settings

Do not change clock settings while measurement is performed using the touch sensor control unit.
Set the CM36 bit to 0 and the CM37 bit to 0 in the CM3 register and do not switch the clock used when exiting wait mode by an interrupt request signal.

21.5.7 Restrictions on Wait Mode

When the touch sensor control unit is used in wait mode, the following restrictions apply.

- Execute a WAIT instruction or set the CM30 bit in the CM3 register to 1 immediately after the SCSTRT bit is set to 1.
- Set the FMR11 bit in the FMR1 register to 1 and the FMSTP bit in the FMR0 register to 0 to not stop the flash memory even during wait mode.
- Do not use the sensor control unit in low-power-consumption wait mode. Set the SVC0 bit in the SVDC register to 0.

21.5.8 Restrictions on Stop Mode

The touch sensor control unit must be stopped (set the SCSTRT bit to 0) and set for initialization (set the SCINIT bit to 1) before setting stop mode (set the CM1_0 bit in the CM1 register to 1) to stop all clocks.

Any setting changes or initialization of the sensor control unit, including the setting change to stop mode, should be performed after measurement completes or before measurement starts, as much as possible.

22. Flash Memory

The flash memory can perform in the following three rewrite modes: CPU rewrite mode, standard serial I/O mode, and parallel I/O mode.

22.1 Overview

Table 22.1 lists the Flash Memory Performance. (Refer to **Tables 1.1 and 1.2 R5R0C0B Group Specifications** for items not listed in Table 22.1.) Table 22.2 lists the Flash Memory Rewrite Mode.

Table 22.1 Flash Memory Performance

Item		Specification
Flash memory operating mode		3 modes (CPU rewrite, standard serial I/O, and parallel I/O)
Division of erase blocks		Refer to **Figure 22.1**.
Programming method		Byte units
Erasure method		Block erase
Programming and erasure control method (1)		Program and erase control by software commands
Rewrite control method	Blocks 0 to 3 (Program ROM) (3)	Rewrite protect control in block units by the lock bit
Number of commands		7 commands
Programming and erasure endurance (2)	Blocks 0 to 3 (Program ROM) (3)	1,000 times
ID code check function		Standard serial I/O mode supported
ROM code protection		Parallel I/O mode supported

Notes:
1. To perform programming and erasure, use VCC = 2.7 V to 5.5 V as the supply voltage. Do not perform programming and erasure at less than 2.7 V.
2. Definition of programming and erasure endurance
   The programming and erasure endurance is defined on a per-block basis.
   If the programming and erasure endurance is n (n = 1,000 or 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1-Kbyte block, and then the block is erased, the programming/ erasure endurance still stands at one. When performing 100 or more rewrites, the actual erase count can be reduced by executing program operations in such a way that all blank areas are used before performing an erase operation. Avoid rewriting only particular blocks and try to average out the programming and erasure endurance of the blocks. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
3. The number of blocks and block division vary with the MCU. Refer to **Figure 22.1 R5R0C0B Group Flash Memory Block Diagram** for details.

Table 22.2 Flash Memory Rewrite Mode

Flash Memory Rewrite Mode	CPU Rewrite Mode	Standard Serial I/O Mode	Parallel I/O Mode
Function	User ROM area is rewritten by executing software commands from the CPU.	User ROM area is rewritten using a dedicated serial programmer.	User ROM area is rewritten using a dedicated parallel programmer.
Rewritable area	User ROM	User ROM	User ROM
Rewrite programs	User program	Standard boot program	—

22.2 Memory Map

The flash memory contains a user ROM area and a boot ROM area (reserved area).
Figure 22.1 shows the R5R0C0B Group Flash Memory Block Diagram.
The user ROM area contains program ROM.
Program ROM: Flash memory mainly used for storing programs
The user ROM area is divided into several blocks. The user ROM area can be rewritten in CPU rewrite mode, standard serial I/O mode, or parallel I/O mode.
The rewrite control program (standard boot program) for standard serial I/O mode is stored in the boot ROM area before shipment. The boot ROM area is allocated separately from the user ROM area.

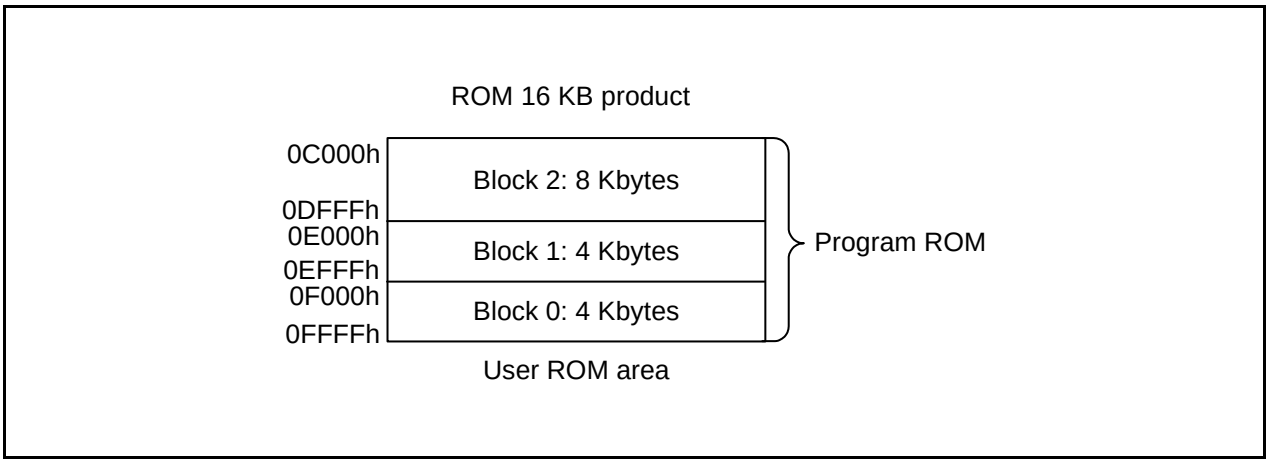


Figure 22.1 R5R0C0B Group Flash Memory Block Diagram

22.3 Functions to Prevent Flash Memory from being Rewritten

Standard serial I/O mode has an ID code check function, and parallel I/O mode has a ROM code protect function to prevent the flash memory from being read or rewritten easily.

22.3.1 ID Code Check Function

The ID code check function is used in standard serial I/O mode. Unless 3 bytes (addresses 0FFFCh to 0FFFEh) of the reset vector are set to FFFFFFh, the ID codes sent from the serial programmer or the on-chip debugging emulator and the 7-byte ID codes written in the flash memory are checked to see if they match. If the ID codes do not match, the commands sent from the serial programmer or the on-chip debugging emulator are not accepted. For details of the ID code check function, refer to **12. ID Code Areas**.

22.3.2 ROM Code Protect Function

The ROM protect function prevents the contents of the flash memory from being read, rewritten, or erased using the OFS register in parallel I/O mode.
Refer to **13. Option Function Select Area** for details of the option function select area.

The ROM code protect function is enabled by writing 1 to the ROMCR bit and writing 0 to the ROMCP1 bit. This prevents the contents of the on-chip flash memory from being read or rewritten.
Once ROM code protection is enabled, the content of the internal flash memory cannot be rewritten in parallel I/O mode. To disable ROM code protection, erase the block including the OFS register using CPU rewrite mode or standard serial I/O mode.

22.3.3 Option Function Select Register (OFS)

Address 0FFFFh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CSPROINI	LVDAS	VDSEL1	VDSEL0	ROMCP1	ROMCR	—	WDTON
After Reset	User Setting Value (1)							

Bit	Symbol	Bit Name	Function	R/W
b0	WDTON	Watchdog timer start select bit	0: Watchdog timer automatically starts after reset. 1: Watchdog timer is stopped after reset.	R/W
b1	—	Reserved bit	Set to 1.	R/W
b2	ROMCR	ROM code protect disable bit	0: ROM code protect disabled 1: ROMCP1 bit enabled	R/W
b3	ROMCP1	ROM code protect bit	0: ROM code protect enabled 1: ROM code protect disabled	R/W
b4	VDSEL0	Voltage detection 0 level select bit (2)	b5 b4 0 0: 3.80 V selected (Vdet0_3) 0 1: 2.85 V selected (Vdet0_2) 1 0: 2.35 V selected (Vdet0_1) 1 1: 1.90 V selected (Vdet0_0)	R/W
b5	VDSEL1			R/W
b6	LVDAS	Voltage detection 0 circuit start bit (3)	0: Voltage monitor 0 reset enabled after reset 1: Voltage monitor 0 reset disabled after reset	R/W
b7	CSPROINI	Count source protection mode after reset select bit	0: Count source protect mode enabled after reset 1: Count source protect mode disabled after reset	R/W

Notes:
1. The OFS register is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not write additions to the OFS register. If the block including the OFS register is erased, the OFS register is set to FFh.
   When blank products are shipped, the OFS register is set to FFh. It is set to the written value after written by the user.
   When factory-programming products are shipped, the value of the OFS register is the value programmed by the user.
2. The same level of the voltage detection 0 level selected by bits VDSEL0 and VDESL1 is set in both functions of voltage monitor 0 reset and power-on reset.
3. To use power-on reset and voltage monitor 0 reset, set the LVDAS bit to 0 (voltage monitor 0 reset enabled after reset).

For a setting example of the OFS register, refer to **13.3.1 Setting Example of Option Function Select Area**.

LVDAS Bit (Voltage Detection 0 Circuit Start Bit)

The Vdet0 voltage to be monitored by the voltage detection 0 circuit is selected by bits VDSEL0 and VDSEL1.

22.4 CPU Rewrite Mode

In CPU rewrite mode, the user ROM area can be rewritten by executing software commands from the CPU. Therefore, the user ROM area can be rewritten directly while the MCU is mounted on a board without using a ROM programmer. Execute the software command only to blocks in the user ROM area.
The flash module has an erase-suspend function which halts the erase operation temporarily during an erase operation in CPU rewrite mode. During erase-suspend, the flash memory can be read or programmed.
Erase-write 0 mode (EW0 mode) and erase-write 1 mode (EW1 mode) are available in CPU rewrite mode.
Table 22.3 lists the Differences between EW0 Mode and EW1 Mode.

Table 22.3 Differences between EW0 Mode and EW1 Mode

Item	EW0 Mode	EW1 Mode
Operating mode	Single-chip mode	Single-chip mode
Rewrite control program allocatable area	User ROM	User ROM
Rewrite control program executable areas	RAM (The rewrite control program must be transferred before being executed.)	User ROM or RAM
Rewritable area	User ROM	User ROM However, blocks which contain the rewrite control program are excluded.
Software command restrictions	—	Program and block erase commands cannot be executed to any block which contains the rewrite control program.
Mode after programming or block erasure or after entering erase-suspend	Read array mode	Read array mode
CPU state during programming and block erasure	The CPU operates.	The CPU is put in a hold state while the program ROM area is being programmed or block erased. (I/O ports retain the state before the command execution).
Flash memory status detection	Read bits FST7, FST5, and FST4 in the FST register by a program.	Read bits FST7, FST5, and FST4 in the FST register by a program.
Conditions for entering erase-suspend	• Set bits FMR20 and FMR21 in the FMR2 register to 1 by a program. • Set bits FMR20 and FMR22 in the FMR2 register to 1 and the enabled maskable interrupt is generated.	Set bits FMR20 and FMR22 in the FMR2 register to 1 and the enabled maskable interrupt is generated.
CPU clock	Max. 20 MHz	Max. 20 MHz

22.4.1 Flash Memory Status Register (FST)

Address 01B2h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	FST7	FST6	FST5	FST4	—	LBDATA	BSYAEI	RDYSTI
After Reset	1	0	0	0	0	X	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	RDYSTI	Flash ready status interrupt request flag (1, 4)	0: No flash ready status interrupt request 1: Flash ready status interrupt request	R/W
b1	BSYAEI	Flash access error interrupt request flag (2, 4)	0: No flash access error interrupt request 1: Flash access error interrupt request	R/W
b2	LBDATA	LBDATA monitor flag	0: Locked 1: Not locked	R
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	FST4	Program error flag (3)	0: No program error 1: Program error	R
b5	FST5	Erase error/blank check error flag (3)	0: No erase error/blank check error 1: Erase error/blank check error	R
b6	FST6	Erase-suspend status flag	0: Other than erase-suspend 1: During erase-suspend	R
b7	FST7	Ready/busy status flag	0: Busy 1: Ready	R

Notes:
1. The RDYSTI bit cannot be set to 1 (flash ready status interrupt request) by a program.
   When writing 0 (no flash ready status interrupt request) to the RDYSTI bit, read this bit (dummy read) before writing to it.
   Make sure the DTC is not activated by the flash ready status source between reading and writing.
   To confirm this bit, set the RDYSTIE bit in the FMR0 register to 1 (flash ready status interrupt enabled).
2. The BSYAEI bit cannot be set to 1 (flash access error interrupt request) by a program.
   When writing 0 (no flash access error interrupt request) to the BSYAEI bit, read this bit (dummy read) before writing to it.
   To confirm this bit, set the BSYAEIE bit in the FMR0 register to 1 (flash access error interrupt enabled) or set the CMDERIE bit in the FMR0 register to 1 (erase/write error interrupt enabled).
3. This bit is also set to 1 (error) when a command error occurs.
4. When this bit is set to 1, do not set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled).

RDYSTI Bit (Flash Ready Status Interrupt Request Flag)

When the RDYSTIE bit in the FMR0 register is set to 1 (flash ready status interrupt enabled) and auto-programming or auto-erasure completes, or erase-suspend mode is entered, the RDYSTI bit is set to 1 (flash ready status interrupt request).
During interrupt handling, set the RDYSTI bit to 0 (no flash ready status interrupt request).

[Condition for setting to 0]
Set to 0 by an interrupt handling program.
[Condition for setting to 1]
When the flash memory status changes from busy to ready while the RDYSTIE bit in the FRMR0 register is set to 1, the RDYSTI bit is set to 1.
The status is changed from busy to ready in the following states:
- Completion of erasing/programming the flash memory
- Suspend acknowledgement
- Completion of forcible termination
- Completion of the lock bit program
- Completion of the read lock bit status
- Completion of the block blank check
- When the flash memory can be read after it is released from stop state.

BSYAEI Bit (Flash Access Error Interrupt Request Flag)

The BSYAEI bit is set to 1 (flash access error interrupt request) when the BSYAEIE bit in the FMR0 register is set to 1 (flash access error interrupt enabled) and the block during auto-programming/auto-erasure is accessed. This bit is also set to 1 if an erase or program error occurs when the CMDERIE bit in the FMR0 register is set to 1 (erase/write error interrupt enabled).
During interrupt handling, set the BSYAEI bit to 0 (no flash access error interrupt request).

[Conditions for setting to 0]
(1) Set to 0 by an interrupt handling program.
(2) Execute the clear status register command.
[Conditions for setting to 1]
(1) Read or write the area that is being erased/written when the BSYAEIE bit in the FMR0 register is set to 1 and while the flash memory is busy.
(Note that the read value is undefined. Writing has no effect.)
(2) If a command sequence error, erase error, blank check error, or program error occurs when the CMDERIE bit in the FMR0 register is set to 1 (erase/write error interrupt enabled).

LBDATA Bit (LBDATA Monitor Flag)

This is a read-only bit indicating the lock bit status. To confirm the lock bit status, execute the read lock bit status command and read the LBDATA bit after the FST7 bit is set to 1 (ready).
The condition for updating this bit is when the program, erase, read lock bit status commands are generated.
When the read lock bit status command is input, the FST7 bit is set to 0 (busy). At the time when the FST7 bit is set to 1 (ready), the lock bit status is stored in the LBDATA bit. The data in the LBDATA bit is retained until the next command is input.

FST4 Bit (Program Error Flag)

This is a read-only bit indicating the auto-programming status. The bit is set to 1 if a program error occurs; otherwise, it is set to 0. Refer to **22.4.11 Full Status Check** for details.

FST5 Bit (Erase Error/Blank Check Error Flag)

This is a read-only bit indicating the status of auto-erasure or the block blank check command. The bit is set to 1 if an erase error or blank check error occurs; otherwise, it is set to 0. Refer to **22.4.11 Full Status Check** for details.

FST6 Bit (Erase Suspend Status Flag)

This is a read-only bit indicating the suspend status. The bit is set to 1 when an erase-suspend request is acknowledged and a suspend status is entered; otherwise, it is set to 0.

FST7 Bit (Ready/Busy Status Flag)

When the FST7 bit is set to 0 (busy), the flash memory is in one of the following states:
- During programming
- During erasure
- During the lock bit program
- During the read lock bit status
- During the block blank check
- During forced stop operation
- The flash memory is being stopped
- The flash memory is being activated

Otherwise, the FST7 bit is set to 1 (ready).

22.4.2 Flash Memory Control Register 0 (FMR0)

Address 01B4h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	RDYSTIE	BSYAEIE	CMDERIE	CMDRST	FMSTP	FMR02	FMR01	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved bit	Set to 0.	R/W
b1	FMR01	CPU rewrite mode select bit (1, 4)	0: CPU rewrite mode disabled 1: CPU rewrite mode enabled	R/W
b2	FMR02	EW1 mode select bit (1)	0: EW0 mode 1: EW1 mode	R/W
b3	FMSTP	Flash memory stop bit (2)	0: Flash memory operates 1: Flash memory stops (Low-power consumption state, flash memory initialization)	R/W
b4	CMDRST	Erase/write sequence reset bit (3)	When the CMDRST bit is set to 1, the erase/write sequence is reset and erasure/writing can be forcibly stopped. When read, the content is 0.	R/W
b5	CMDERIE	Erase/write error interrupt enable bit	0: Erase/write error interrupt disabled 1: Erase/write error interrupt enabled	R/W
b6	BSYAEIE	Flash access error interrupt enable bit	0: Flash access error interrupt disabled 1: Flash access error interrupt enabled	R/W
b7	RDYSTIE	Flash ready status interrupt enable bit	0: Flash ready status interrupt disabled 1: Flash ready status interrupt enabled	R/W

Notes:
1. To set this bit to 1, first write 0 and then 1 immediately. Do not generate an interrupt between writing 0 and writing 1.
2. Write to the FMSTP bit by a program transferred to the RAM. The FMSTP bit is enabled when the FMR01 bit is set to 1 (CPU rewrite mode enabled). To set the FMSTP bit to 1 (flash memory stops), set it when the FST7 bit in the FST register is set to 1 (ready).
3. The CMDRST bit is enabled when the FMR01 bit is set to 1 (CPU rewrite mode enabled) and the FST7 bit in the FST register is set to 0 (busy).
4. To set the FMR01 bit to 0 (CPU rewrite mode disabled), set it when the RDYSTI bit in the FST register is set to 0 (no flash ready status interrupt request) and the BSYAEI bit is set to 0 (no flash access error interrupt request).

FMR01 Bit (CPU Rewrite Mode Select Bit)

When the FMR01 bit is set to 1 (CPU rewrite mode enabled), the MCU is made ready to accept software commands.

FMR02 Bit (EW1 Mode Select Bit)

When the FMR02 bit is set to 1 (EW1 mode), EW1 mode is selected.

FMSTP Bit (Flash Memory Stop Bit)

This bit is used to initialize the flash memory control circuits, and also to reduce the amount of current consumed by the flash memory. Access to the flash memory is disabled by setting the FMSTP bit to 1.
Write to the FMSTP bit by a program transferred to the RAM.
To reduce the power consumption further in high-speed on-chip oscillator mode and low-speed on-chip oscillator mode (XIN clock stopped), set the FMSTP bit to 1. Refer to **23.2.8 Stopping Flash Memory** for details.
When entering stop mode or wait mode while CPU rewrite mode is disabled, the FMR0 register does not need to be set because the power for the flash memory is automatically turned off and is turned back on when exiting stop or wait mode.
When the FMSTP bit is set to 1 (including during the busy status (the period while the FST7 bit is 0) immediately after the FMSTP bit is changed from 1 to 0), do not set to low-current-consumption read mode at the same time.

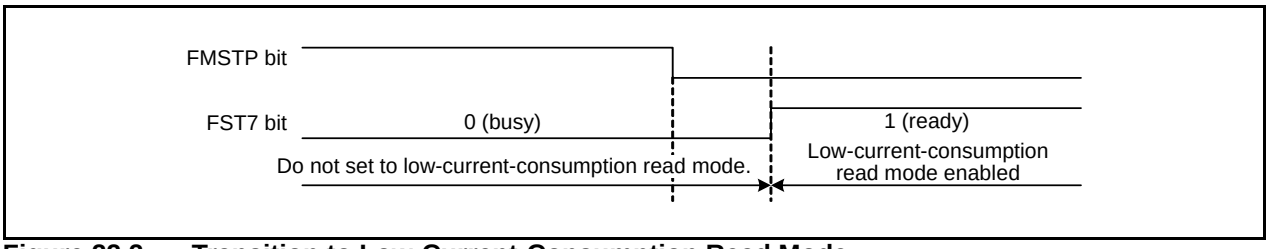


Figure 22.2 Transition to Low-Current-Consumption Read Mode

CMDRST Bit (Erase/Write Sequence Reset Bit)

This bit is used to initialize the flash memory sequence and forcibly stop a program or block erase command. The user ROM area can be read while the flash memory sequence is being initialized.
If the program or block erase command is forcibly stopped using the CMDRST bit in the FMR0 register, execute the clear status register command after the FST7 bit in the FST register is changed to 1 (ready). To program to the same address again, execute the block erase command again and ensure it has been completed normally before programming. If the addresses and blocks which the program or block erase command is forcibly stopped are allocated in the program area, set the FMR13 bit in the FMR1 register to 1 (lock bit disabled) before executing the block erase command again.
When the CMDRST bit is set to 1 (erasure/writing stopped) during erase-suspend, the suspend status is also initialized. Thus execute block erasure again to the block which the block erasure is being suspended.
When td(CMDRST-READY) has elapsed after the CMDRST bit is set to 1 (erasure/writing stopped), the executing command is forcibly terminated and reading from the flash memory is enabled.

CMDERIE Bit (Erase/Write Error Interrupt Enable Bit)

This bit enables a flash command error interrupt to be generated if the following errors occur:
- Program error
- Block erase error
- Command sequence error
- Block blank check error

If the CMDERIE bit is set to 1 (erase/write error interrupt enabled) and erasure/writing is performed, an interrupt is generated if the above errors occur.
If a flash command error interrupt is generated, execute the clear status register command during interrupt handling.

To change the CMDERIE bit from 0 (erase/write error interrupt disabled) to 1 (erase/write error interrupt enabled), make the setting as follows:
(1) Execute the clear status register command.
(2) Set the CMDERIE bit to 1.

BSYAEIE Bit (Flash Access Error Interrupt Enable Bit)

This bit enables a flash access error interrupt to be generated if the flash memory during rewriting is accessed.

To change the BSYAEIE bit from 0 (flash access error interrupt disabled) to 1 (flash access error interrupt enabled), make the setting as follows:
(1) Read the BSYAEI bit in the FST register (dummy read).
(2) Write 0 (no flash access error interrupt request) to the BSYAEI bit.
(3) Set the BSYAEIE bit to 1 (flash access error interrupt enabled).

RDYSTIE Bit (Flash Ready Status Interrupt Enable Bit)

This bit enables a flash ready status error interrupt to be generated when the status of the flash memory sequence changes from the busy to ready status.

To change the RDYSTIE bit from 0 (flash ready status interrupt disabled) to 1 (flash ready status interrupt enabled), make the setting as follows:
(1) Read the RDYSTI bit in the FST register (dummy read).
(2) Write 0 (no flash ready status interrupt request) to the RDYSTI bit.
(3) Set the RDYSTIE bit to 1 (flash ready status interrupt enabled).

22.4.3 Flash Memory Control Register 1 (FMR1)

Address 01B5h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	FMR13	—	WTFMACT	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b1	WTFMACT	Flash memory stop bit in wait mode	0: Flash memory stops in wait mode 1: Flash memory operates in wait mode	R/W
b2	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b3	FMR13	Lock bit disable select bit (1)	0: Lock bit enabled 1: Lock bit disabled	R/W
b4	—	Reserved bits	Set to 0.	R/W
b5	—			R/W
b6	—			R/W
b7	—			R/W

Note:
1. To set the FMR13 bit to 1, first write 0 and then 1 immediately. Disable interrupts and DTC activation between writing 0 and writing 1.

FMR13 Bit (Lock Bit Disable Select Bit)

When the FMR13 bit is set to 1 (lock bit disabled), the lock bit is disabled. When the FMR13 bit is set to 0, the lock bit is enabled. Refer to **22.4.9 Data Protect Function** for the details of the lock bit.
The FMR13 bit enables the lock bit function only and the lock bit data does not change. However, when a block erase command is executed while the FMR13 bit is set to 1, the lock bit data set to 0 (locked) changes to 1 (not locked) after erasure completes.

[Conditions for setting to 0]
The FMR13 bit is set to 0 when one of the following conditions is met.
- Completion of the program command
- Completion of the erase command
- Generation of a command sequence error
- Transition to erase-suspend
- If the FMR01 bit in the FMR0 register is set to 0 (CPU rewrite mode disabled).
- If the FMSTP bit in the FMR0 register is set to 1 (flash memory stops).
- If the CMDRST bit in the FMR0 register is set to 1 (erasure/writing stopped).

[Condition for setting to 1]
Set to 1 by a program.

22.4.4 Flash Memory Control Register 2 (FMR2)

Address 01B6h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	FMR27	—	—	—	—	FMR22	FMR21	FMR20
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	FMR20	Erase-suspend enable bit (1)	0: Erase-suspend disabled 1: Erase-suspend enabled	R/W
b1	FMR21	Erase-suspend request bit (2)	0: Erase restart 1: Erase-suspend request	R/W
b2	FMR22	Interrupt request suspend request enable bit (1)	0: Erase-suspend request disabled by interrupt request 1: Erase-suspend request enabled by interrupt request	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	—	Reserved bits	Set to 0.	R/W
b5	—			
b6	—			
b7	FMR27	Low-consumption-current read mode enable bit (1, 3)	0: Low-consumption-current read mode disabled 1: Low-consumption-current read mode enabled	R/W

Notes:
1. To set this bit to 1, first write 0 and then 1 immediately. Disable interrupts and DTC activation between writing 0 and writing 1.
2. To set the FMR21 bit to 0 (erase restart), set it when the FMR01 bit in the FMR0 register is set to 1 (CPU rewrite mode enabled).
3. After setting the CPU clock to the low-speed on-chip oscillator clock divided by 4, 8, or 16, set the FMR27 bit to 1. When divided by 1 (no division) or divided by 2 is set, do not use low-consumption-current read mode.
   Enter wait mode or stop mode after setting the FMR27 bit to 0 (low-current-consumption read mode disabled).
   Do not enter wait mode or stop mode while the FMR27 bit is 1 (low-current-consumption read mode enabled).

FMR20 Bit (Erase-Suspend Enable Bit)

When the FMR20 bit is set to 1 (enabled), the erase-suspend function is enabled.

FMR21 Bit (Erase-Suspend Request Bit)

When the FMR21 bit is set to 1, erase-suspend mode is entered. If the FMR22 bit is set to 1 (erase-suspend request enabled by interrupt request), the FMR21 bit is automatically set to 1 (erase-suspend request) when an interrupt request for the enabled interrupt is generated, and erase-suspend mode is entered. To restart auto-erasure, set the FMR21 bit to 0 (erase restart).

[Condition for setting to 0]
Set to 0 by a program.
[Conditions for setting to 1]
- When the FMR22 bit is set to 1 (erase-suspend request enabled by interrupt request) at the time an interrupt is generated.
- Set to 1 by a program.

FMR22 Bit (Interrupt Request Suspend-Request Enable Bit)

When the FMR 22 bit is set to 1 (erase-suspend request enabled by interrupt request), the FMR21 bit is automatically set to 1 (erase-suspend request) at the time an interrupt request is generated during auto-erasure. Set the FMR22 bit to 1 when using erase-suspend while rewriting the user ROM area in EW1 mode.

FMR27 Bit (Low-Power-Current Read Mode Enable Bit)

When the FMR 27 bit is set to 1 (low-consumption-current read mode enabled) in low-speed on-chip oscillator mode (XIN clock stopped), power consumption when reading the flash memory can be reduced. Refer to **23.2.9 Low-Current-Consumption Read Mode** for details.

When the CPU clock is set to the low-speed on-chip oscillator clock divided by 4, 8, or 16, low-consumption-current read mode can be used. When divided by 1 (no division) or divided by 2 is set, do not use low-consumption-current read mode. After setting the divide ratio of the CPU clock, set the FMR27 bit to 1.

Enter wait mode or stop mode after setting the FMR27 bit to 0 (low-current-consumption read mode disabled). Do not enter wait mode or stop mode while the FMR27 bit is 1 (low-current-consumption read mode enabled).

When the FMR27 bit is set to 1 (low-consumption-current read mode enabled), do not execute the program, block erase, or lock bit program command. To change the FMSTP bit from 1 (flash memory stops) to 0 (flash memory operates), make the setting when the FMR27 bit is set to 0 (low-consumption-current read mode disabled).

22.4.5 EW0 Mode

When the FMR01 bit in the FMR0 register is set to 1 (CPU rewrite mode enabled), the MCU enters CPU rewrite mode and software commands can be accepted. At this time, the FMR02 bit in the FMR0 register is set to 0 so that EW0 mode is selected.

Software commands are used to control program and erase operations. The FST register can be used to confirm whether programming or erasure has completed.

To enter erase-suspend during auto-erasure, set the FMR20 bit to 1 (erase-suspend enabled) and the FMR21 bit to 1 (erase-suspend request). Next, verify the FST7 bit in the FST register is set to 1 (ready), then verify the FST6 bit is set to 1 (during erase-suspend) before accessing the flash memory. When the FST6 bit is set to 0, erasure completes.

When the FMR21 bit in the FMR2 register is set to 0 (erase restart), auto-erasure restarts. To confirm whether auto-erasure has restarted, verify the FST7 bit in the FST register is set to 0, then verify the FST6 bit is set to 0 (other than erase-suspend).

22.4.6 EW1 Mode

After the FMR01 bit in the FMR0 register is set to 1 (CPU rewrite mode enabled), EW1 mode is selected by setting the FMR02 bit is set to 1.

The FST register can be used to confirm whether programming and erasure has completed.

To enable the erase-suspend function during auto-erasure, execute the block erase command after setting the FMR20 bit in the FMR2 register to 1 (suspend enabled). To enter erase-suspend while auto-erasing the user ROM area, set the FMR22 bit in the FMR2 register to 1 (erase-suspend request enabled by interrupt request). Also, the interrupt to enter erase-suspend must be enabled beforehand.

When an interrupt request is generated, the FMR21 bit in the FMR2 register is automatically set to 1 (erase-suspend request) and auto-erasure suspends after td(SR-SUS). After interrupt handling completes, set the FMR21 bit to 0 (erase restart) to restart auto-erasure.

22.4.7 Suspend Operation

The suspend function halts the auto-erase operation temporarily during auto-erasure.
When auto-erasure is suspended, the next operation can be executed. (Refer to **Table 22.4 Executable Operation during Suspend**.)

- When suspending the auto-erasure of any block in program ROM, auto-programming and reading another block can be executed.
- To check the suspend, verify the FST7 bit is set to 1 (ready), then verify the FST6 bit is set to 1 (during erase-suspend) to confirm whether erasure has been suspended. When the FST6 bit is set to 0 (other than erase suspend), erasure completes.

Figure 22.3 shows the Suspend Operation Timing.

Table 22.4 Executable Operation during Suspend

		Operation during Suspend					
		Program ROM (Block during erasure execution before entering suspend)			Program ROM (Block during no erasure execution before entering suspend)		
		Erase	Program	Read	Erase	Program	Read
Areas during erasure execution before entering suspend	Program ROM	D	D	D	D	E	E

Notes:
1. E indicates operation is enabled by using the suspend function, D indicates operation is disabled, and N/A indicates no combination is available.
2. Operation cannot be suspended during programming.
3. The block erase command can be executed for erasure. The program, lock bit program, and read lock bit status commands can be executed for programming.
   The clear status register command can be executed when the FST7 bit in the FST register is set to 1 (ready).
   The operation of block blank check is disabled during suspend.
4. The MCU enters read array mode immediately after entering erase-suspend.

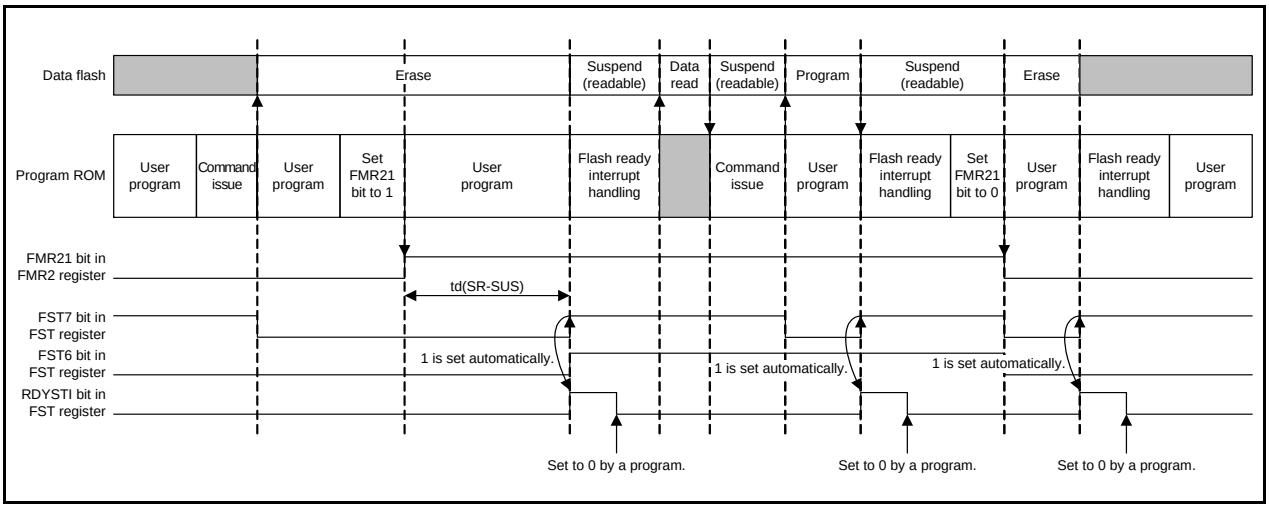


Figure 22.3 Suspend Operation Timing

22.4.8 How to Set and Exit Each Mode

Figure 22.4 shows How to Set and Exit EW0 Mode and Figure 22.5 shows How to Set and Exit EW1 Mode.

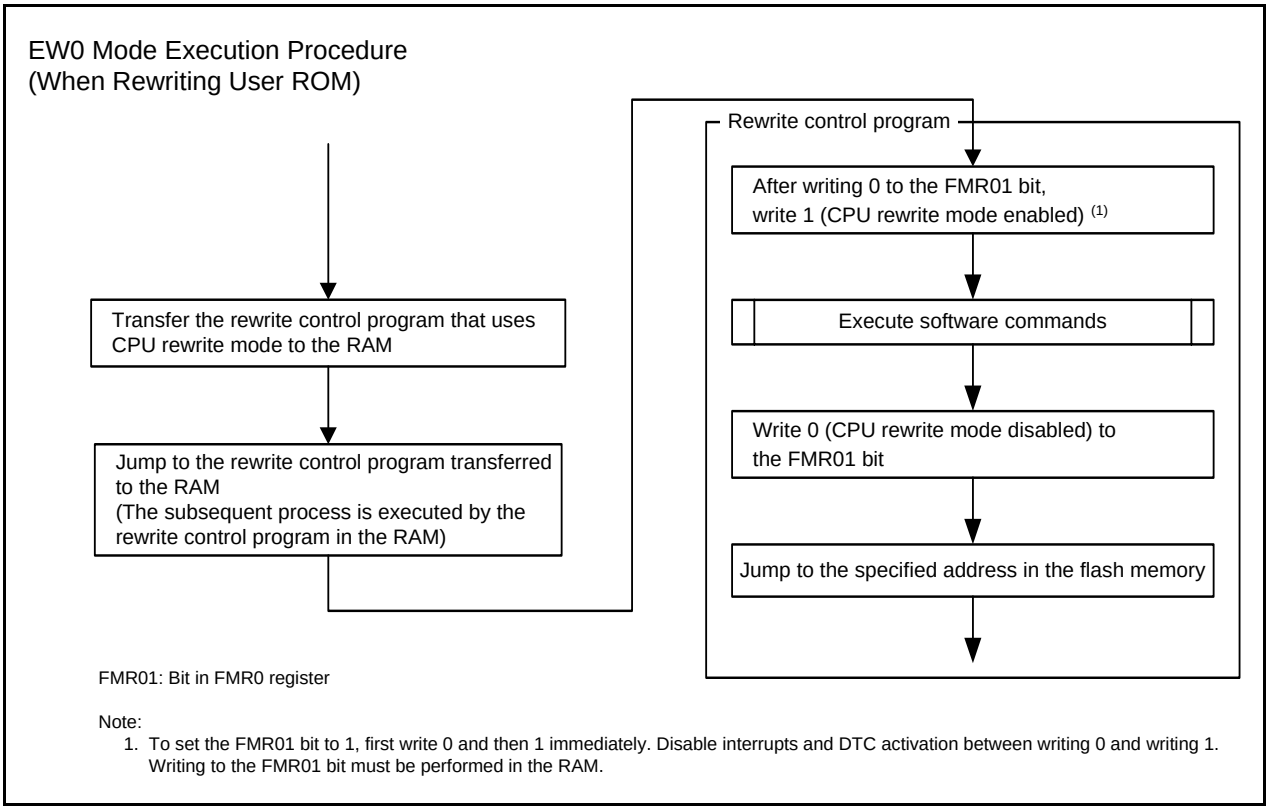


Figure 22.4 How to Set and Exit EW0 Mode

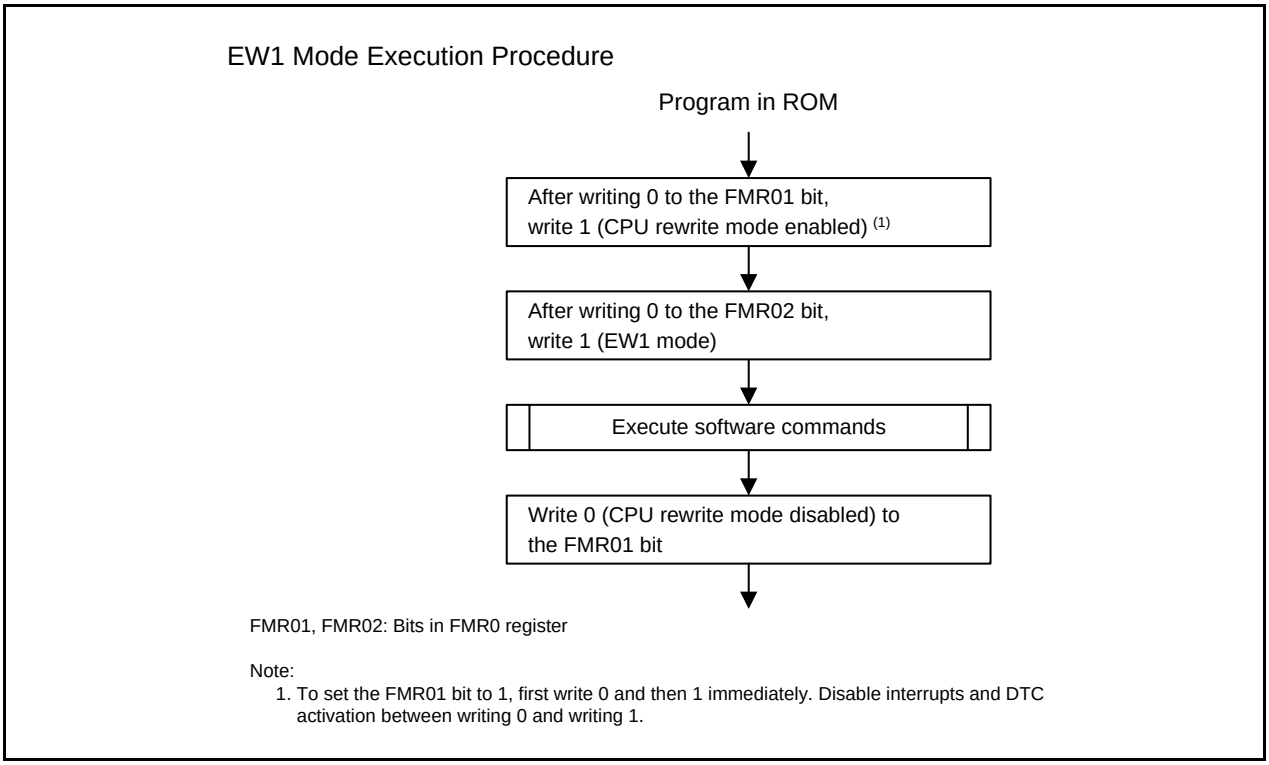


Figure 22.5 How to Set and Exit EW1 Mode

22.4.9 Data Protect Function

Each block in the program ROM has a nonvolatile lock bit. The lock bit is enabled by setting the FMR13 bit in the FMR1 register is set to 0 (lock bit enabled). The lock bit can be used to disable (lock) programming or erasing each block. This prevents data from being written or erased inadvertently. A block status changes according to the lock bit as follows:

- When the lock bit data is set to 0: locked (the block cannot be programmed or erased)
- When the lock bit data is set to 1: not locked (the block can be programmed and erased)

The lock bit data is set to 0 (locked) by executing the lock bit program command and to 1 (not locked) by erasing the block. No commands can be used to set only the lock bit data to 1.
The lock bit data can be read using the read lock bit status command.

When the FMR13 bit is set to 1 (lock bit disabled), the lock bit function is disabled and all blocks are not locked (each lock bit data remains unchanged). The lock bit function is enabled by setting the FMR13 bit to 0 (the lock bit data is retained).
When the block erase command is executed while the FMR13 bit is set to 1, the target block is erased regardless of the lock bit status. The lock bit of the erase target block is set to 1 after auto-erasure completes.
Refer to **22.4.10 Software Commands** for the details of individual commands.
The FMR13 bit is set to 0 after auto-erasure completes. This bit is also set to 0 if one of the following conditions is met. To erase or program a different locked block, set the FMR13 bit to 1 again and execute the block erase or program command.

- If the FST7 bit in the FST register is changed from 0 (busy) to 1 (ready).
- If a command sequence error occurs.
- If the FMR01 bit in the FMR0 register is set to 0 (CPU mode disabled).
- If the FMSTP bit in the FMR0 register is set to 1 (flash memory stops).
- If the CMDRST bit in the FMR0 register is set to 1 (erasure/writing stopped).

Figure 22.6 shows the FMR13 Bit Operation Timing.

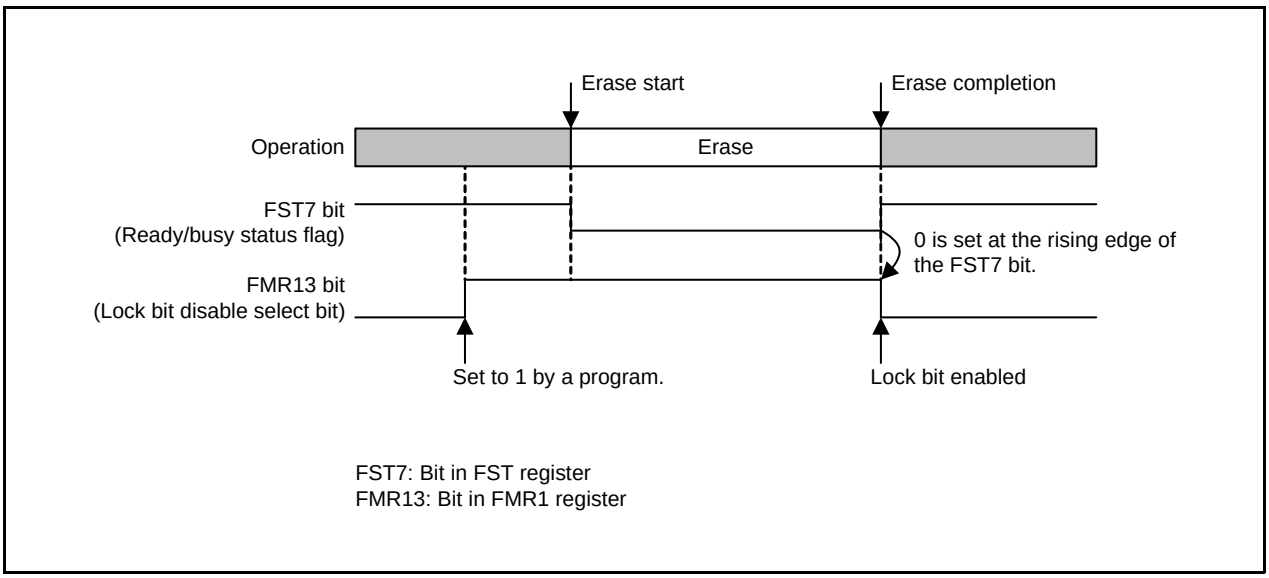


Figure 22.6 FMR13 Bit Operation Timing

22.4.10 Software Commands

The software commands are described below. Read or write commands and data in 8-bit units.
Do not input any command other than those listed in the table below.

Table 22.5 Software Commands

Command	First Bus Cycle			Second Bus Cycle		
	Mode	Address	Data	Mode	Address	Data
Read array	Write	×	FFh			
Clear status register	Write	×	50h			
Program	Write	WA	40h	Write	WA	WD
Block erase	Write	×	20h	Write	BA	D0h
Lock bit program	Write	BT	77h	Write	BT	D0h
Read lock bit status	Write	×	71h	Write	BT	D0h
Block blank check	Write	×	25h	Write	BA	D0h

WA: Write address
WD: Write data
BA: Any block address
BT: Starting block address
×: Any address in the user ROM area

22.4.10.1 Read Array Command

The read array command is used to read the flash memory.
When FFh is written in the first bus cycle, the MCU enters read array mode. When the read address is input in the following bus cycles, the content of the specified address can be read in 8-bit units.
Since read array mode remains until another command is written, the contents of multiple addresses can be read continuously.
In addition, after a reset, the MCU enters read array mode after a program, block erase, block blank check, read lock bit status, or clear status register command, or after entering erase-suspend.

22.4.10.2 Clear Status Register Command

The clear status register command is used to set bits FST4 and FST5 in the FST register to 0.
When 50h is written in the first bus cycle, bits FST4 and FST5 in the FST register are set to 0.

22.4.10.3 Program Command

The program command is used to write data to the flash memory in 1-byte units.
When 40h is written in the first bus cycle and data is written in the second bus cycle to the write address, auto-programming (data program and verify operation) starts. Make sure the address value specified in the first bus cycle is the same address as the write address specified in the second bus cycle.
The FST7 bit in the FST register can be used to confirm whether auto-programming has completed. The FST7 bit is set to 0 during auto-programming and is set to 1 when auto-programming completes.
After auto-programming has completed, the auto-program result can be confirmed by the FST4 bit in the FST register. (Refer to **22.4.11 Full Status Check**.)
Do not write additions to the already programmed addresses.

The program command targeting each block in the program ROM can be disabled using the lock bit.
Figure 22.7 shows a Program Flowchart (Flash Ready Status Interrupt Disabled) and Figure 22.8 shows a Program Flowchart (Flash Ready Status Interrupt Enabled).

In EW1 mode, do not execute this command to any address where a rewrite control program is allocated.

When the RDYSTIE bit in the FMR0 register is set to 1 (flash ready status interrupt enabled), a flash ready status interrupt can be generated upon completion of auto-programming. The auto-program result can be confirmed by reading the FST register during the interrupt routine.

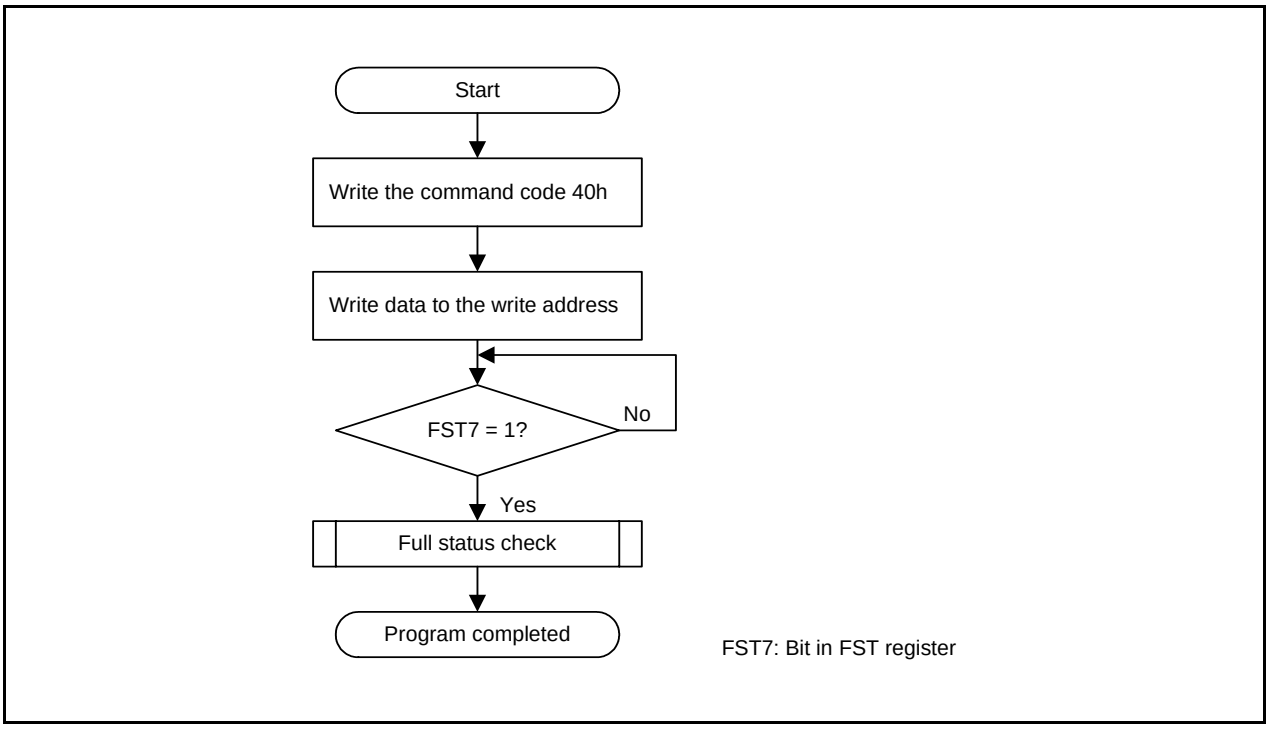


Figure 22.7 Program Flowchart (Flash Ready Status Interrupt Disabled)

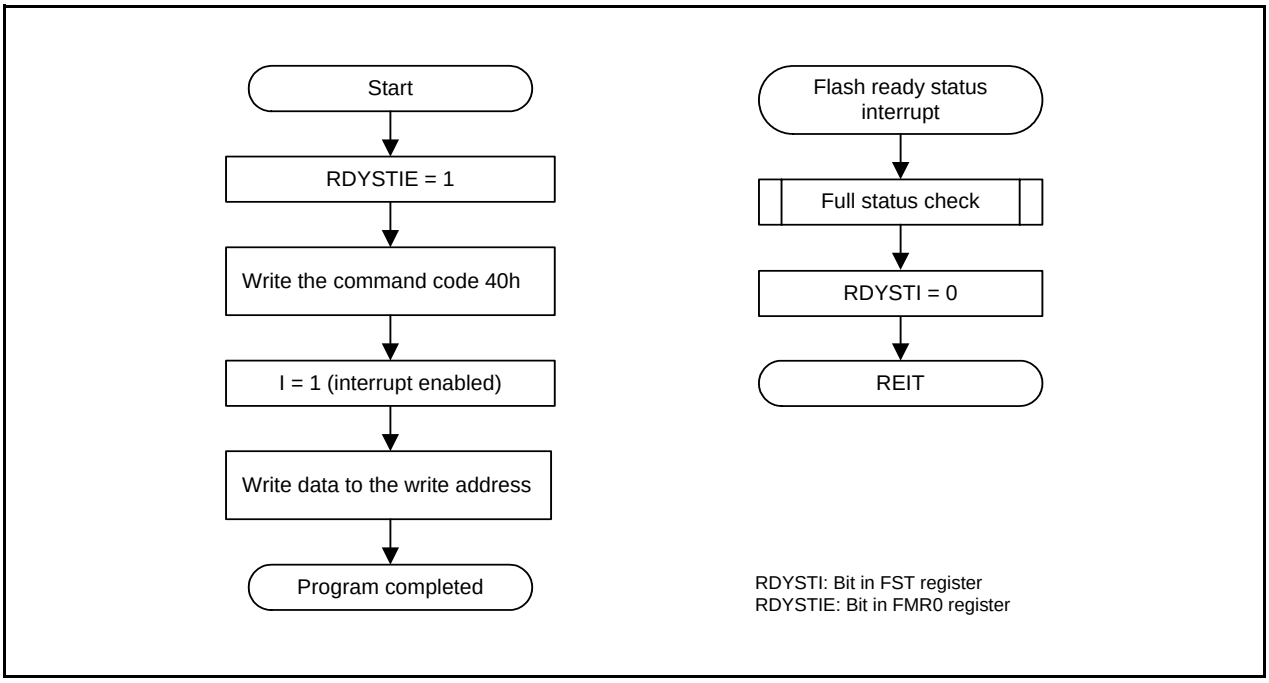


Figure 22.8 Program Flowchart (Flash Ready Status Interrupt Enabled)

22.4.10.4 Block Erase Command

When 20h is written in the first bus cycle and then D0h is written in the second bus cycle to any block address, auto-erasure (erase and erase verify operation) starts in the specified block.
The FST7 bit in the FST register can be used to confirm whether auto-erasure has completed. The FST7 bit is set to 0 during auto-erasure and is set to 1 when auto-erasure completes. After auto-erasure completes, all data in the block is set to FFh.
After auto-erasure has completed, the auto-erase result can be confirmed by the FST5 bit in the FST register. (Refer to **22.4.11 Full Status Check**.)

The block erase command targeting each block in the program ROM can be disabled using the lock bit.

Figure 22.9 shows a Block Erase Flowchart (Flash Ready Status Interrupt Disabled), Figure 22.10 shows a Block Erase Flowchart (Flash Ready Status Interrupt Disabled and Suspend Enabled), and Figure 22.11 shows a Block Erase Flowchart (Flash Ready Status Interrupt Enabled and Suspend Enabled).

In EW1 mode, do not execute this command to any block where a rewrite control program is allocated.

While the RDYSTIE bit in the FMR0 register is set to 1 (flash ready status interrupt enabled), a flash ready status interrupt can be generated upon completion of auto-erasure. While the RDYSTIE bit is set to 1 and the FMR20 bit in the FMR2 register is set to 1 (erase-suspend enabled), a flash ready status interrupt is generated when the FMR21 bit is set to 1 (erase-suspend request) and auto-erasure suspends. The auto-erase result can be confirmed by reading the FST register during the interrupt routine.

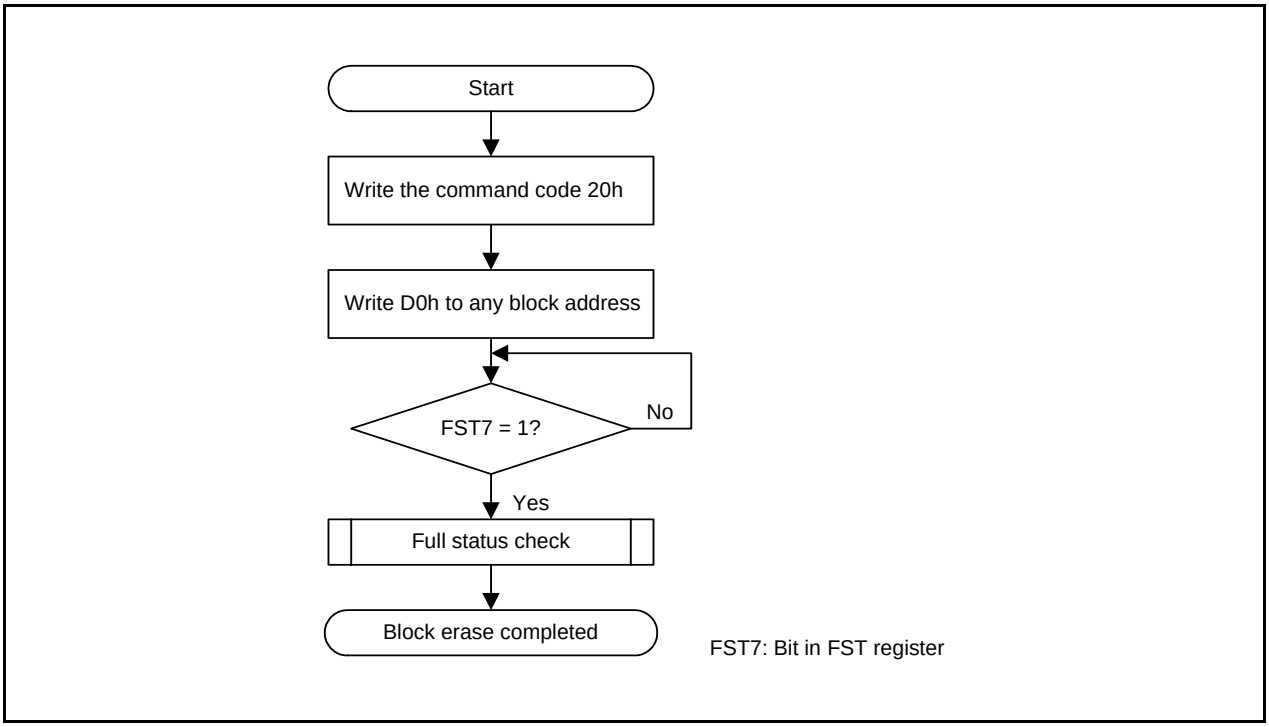
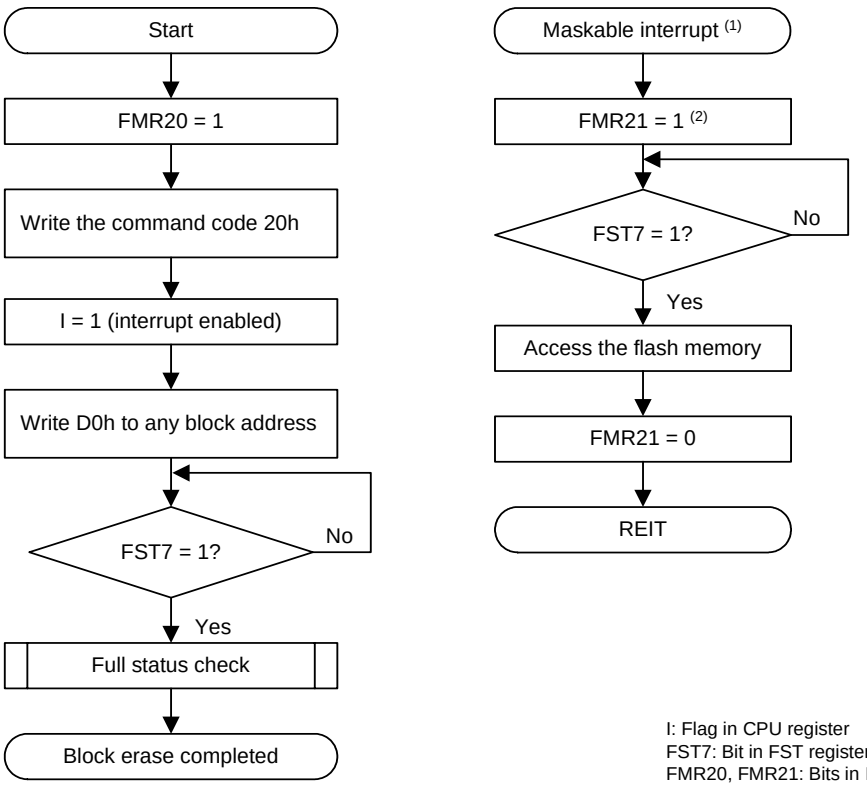
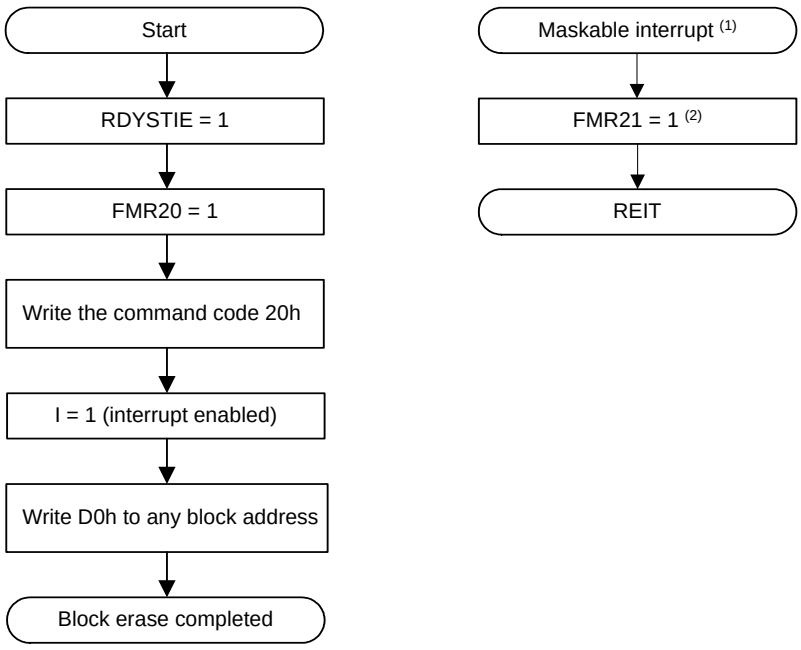


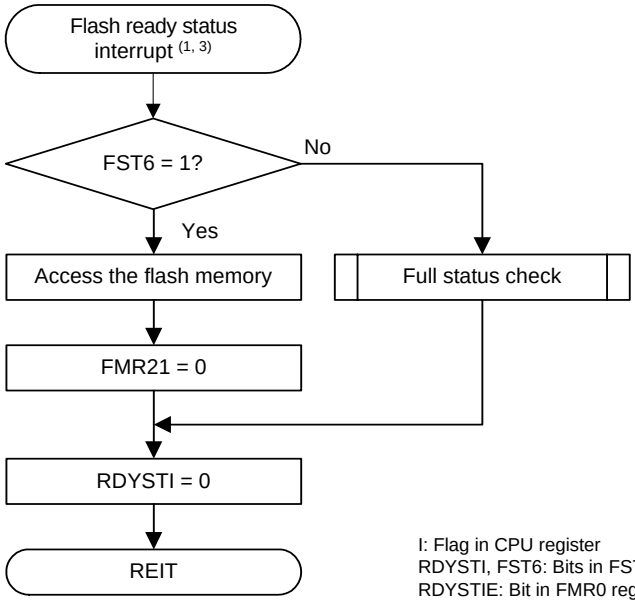
Figure 22.9 Block Erase Flowchart (Flash Ready Status Interrupt Disabled)



Notes:
1. The interrupt vector table and interrupt routine for interrupts to be used must be allocated to an area other than the erase target area.
2. td(SR-SUS) is required until suspend is acknowledged after the FMR21 bit is set to 1.
The interrupt to enter suspend must be enabled beforehand.

Figure 22.10 Block Erase Flowchart (Flash Ready Status Interrupt Disabled and Suspend Enabled)





Notes:
1. The interrupt vector table and interrupt routine for interrupts to be used must be allocated to an area other than the erase target area.
2. td(SR-SUS) is required until suspend is acknowledged after the FMR21 bit is set to 1.
   The interrupt to enter suspend must be enabled beforehand.
3. When auto-erasure suspends, a flash ready status interrupt is generated.

Figure 22.11 Block Erase Flowchart (Flash Ready Status Interrupt Enabled and Suspend Enabled)

22.4.10.5 Lock Bit Program Command

This command is used to set the lock bit of any block in the program ROM area to 0 (locked).
When 77h is written in the first bus cycle and D0h is written in the second bus cycle to the starting block address, 0 is written to the lock bit of the specified block. Make sure the address value in the first bus cycle is the same address as the starting block address specified in the second bus cycle.
Figure 22.12 shows a Lock Bit Program Flowchart. The lock bit status (lock bit data) can be read using the read lock bit status command.
The FST7 bit in the FST register can be used to confirm whether writing to the lock bit has completed.
Refer to **22.4.9 Data Protect Function** for the lock bit function and how to set the lock bit to 1 (not locked).

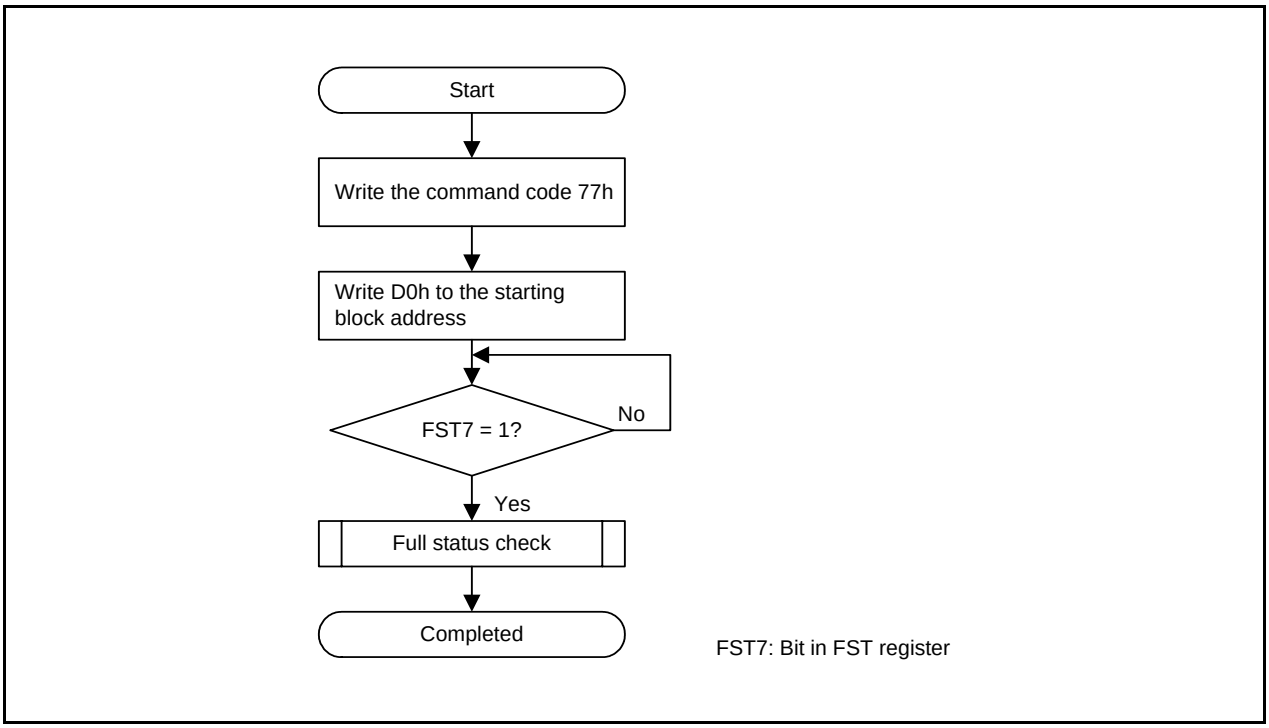


Figure 22.12 Lock Bit Program Flowchart

22.4.10.6 Read Lock Bit Status Command

This command is used to read the lock bit status of any block in the program ROM area.
When 71h is written in the first bus cycle and D0h is written in the second cycle to the starting block address, the lock bit status of the specified block is stored in the LBDATA bit in the FST register. After the FST7 bit in the FST register has been set to 1 (ready), read the LBDATA bit.
Figure 22.13 shows a Read Lock Bit Status Flowchart.

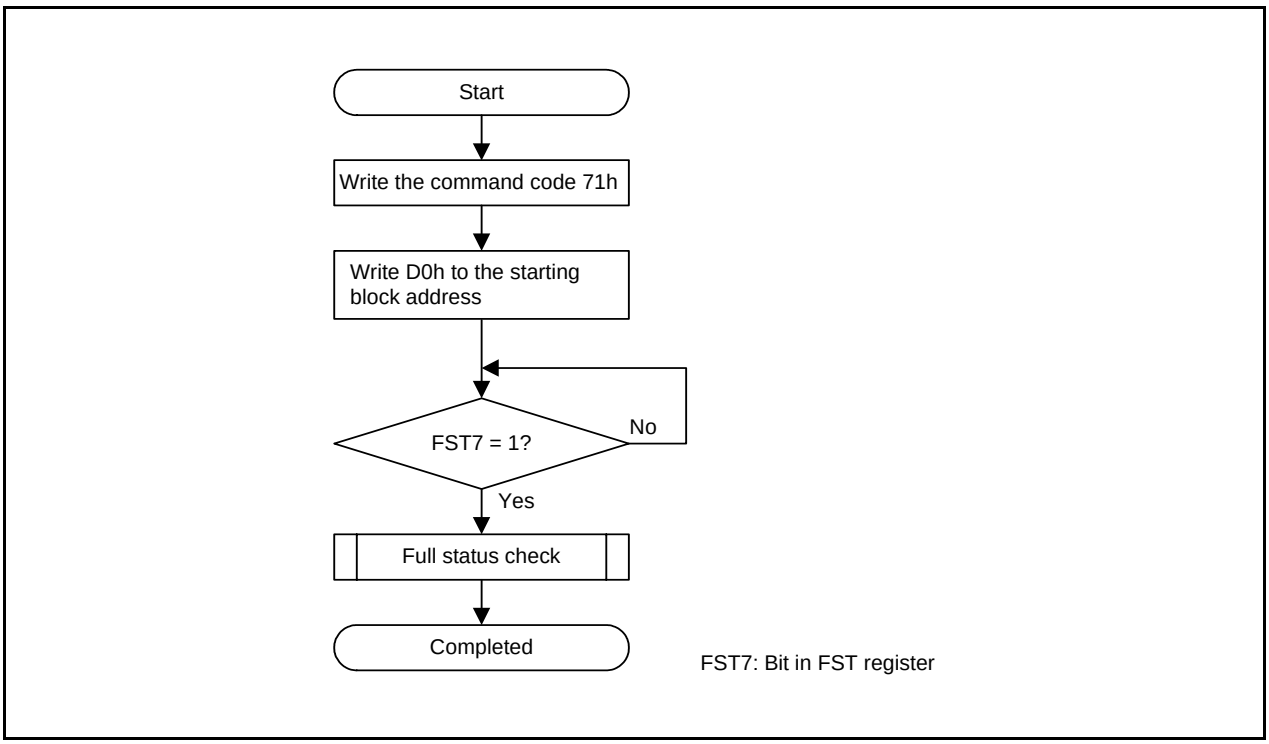


Figure 22.13 Read Lock Bit Status Flowchart

22.4.10.7 Block Blank Check Command

This command is used to confirm that all addresses in any block are blank data FFh.
When 25h is written in the first bus cycle and D0h is written in the second bus cycle to any block address, blank checking starts in the specified block. The FST7 bit in the FST register can be used to confirm whether blank checking has completed. The FST7 bit is set to 0 during the blank-check period and set to 1 when blank checking completes.
After blank checking has completed, the blank-check result can be confirmed by the FST5 bit in the FST register. (Refer to **22.4.11 Full Status Check**.) This command is used to verify the target block has not been written to. To confirm whether erasure has completed normally, execute the full status check.

Do not execute the block blank check command when the FST6 bit is set to 1 (during erase-suspend).
Figure 22.14 shows a Block Blank Check Flowchart.

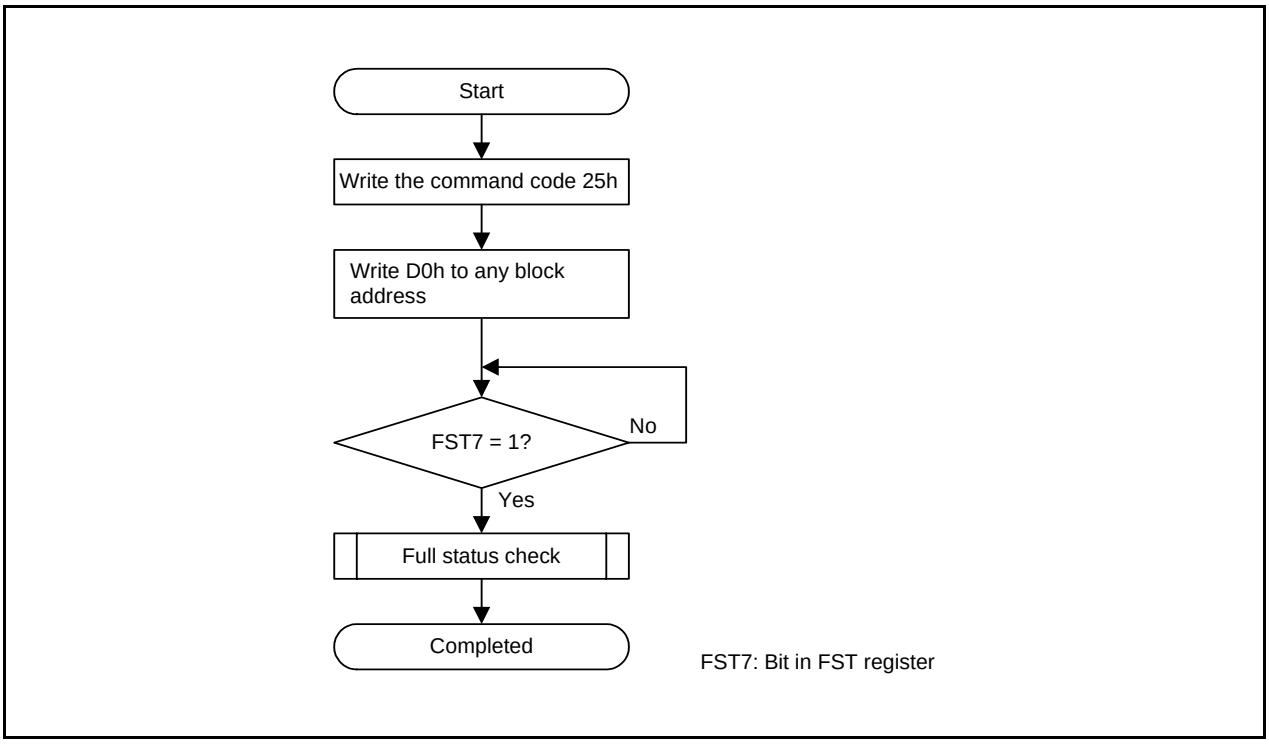


Figure 22.14 Block Blank Check Flowchart

This command is intended for programmer manufactures, not for general users.

22.4.11 Full Status Check

If an error occurs, bits FST4 and FST5 in the FST register are set to 1, indicating the occurrence of an error. The execution result can be confirmed by checking these status bits (full status check).
Table 22.6 lists the Errors and FST Register Status. Figure 22.15 shows the Full Status Check and Handling Procedure for Individual Errors.

Table 22.6 Errors and FST Register Status

FST Register Status		Error	Error Occurrence Condition
FST5	FST4		
1	1	Command sequence error	• When a command is not written correctly. • When data other than valid data (i.e., D0h or FFh) is written in the second bus cycle of the block erase command. (1) • The erase command is executed during suspend. • The command is executed to the block during suspend.
1	0	Erase error	When the block erase command is executed, but auto-erasure does not complete correctly.
		Blank check error	When the block blank check command is executed and data other than blank data FFh is read.
0	1	Program error	When the program command is executed, but auto-programming does not complete correctly.
		Lock bit program error	When the lock bit command is executed, but the lock bit is not set to 0 (locked).

Note:
1. When FFh is written in the second bus cycle of these commands, the MCU enters read array mode. At the same time, the command code written in the first bus cycle is invalid.

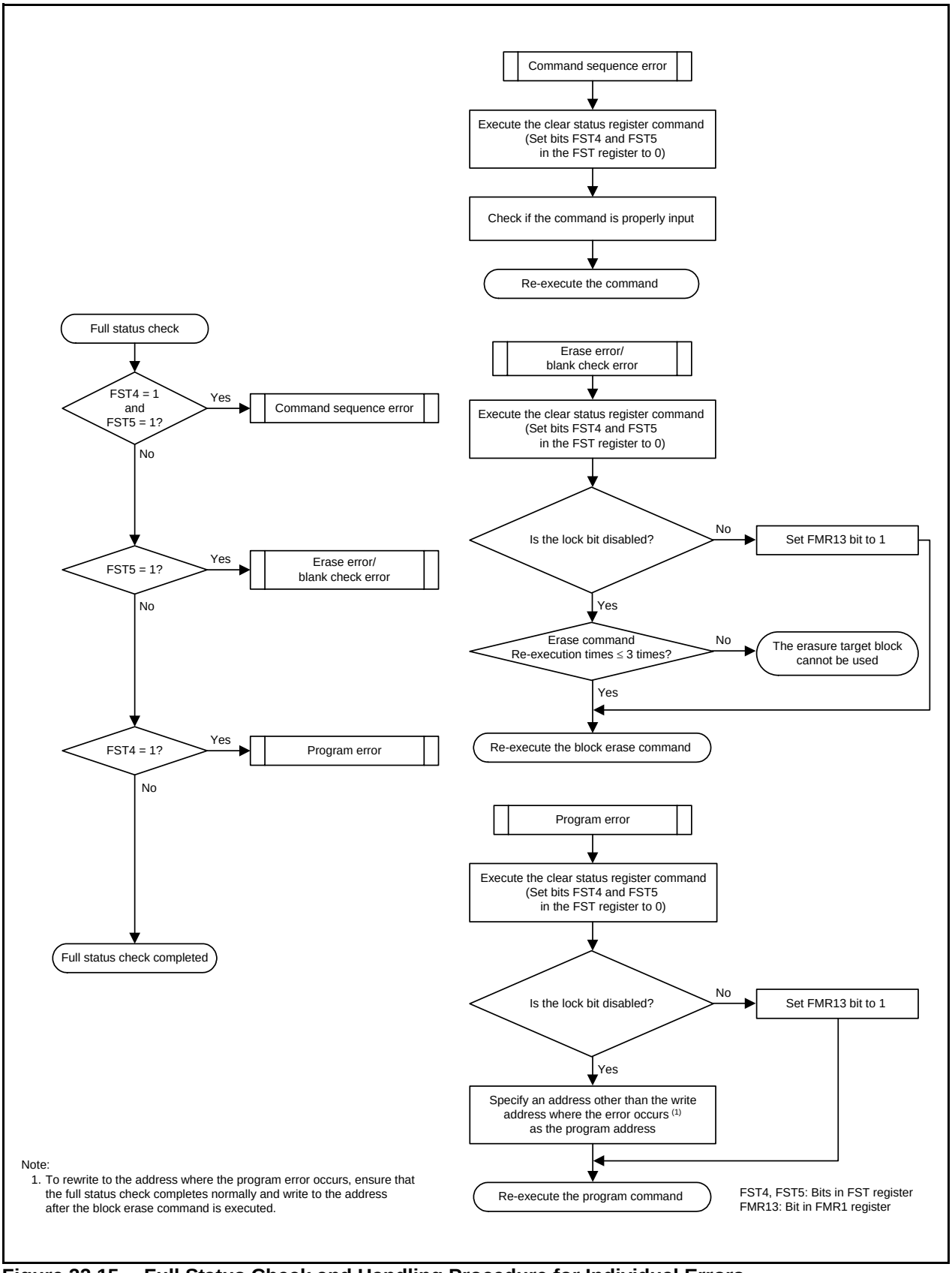


Figure 22.15 Full Status Check and Handling Procedure for Individual Errors

22.5 Standard Serial I/O Mode

In standard serial I/O mode, a serial programmer which supports the MCU can be used to rewrite the user ROM area while the MCU is mounted on-board.
There are three types of standard serial I/O modes:
- Standard serial I/O mode 1 ..... Clock synchronous serial I/O used to connect to a serial programmer
- Standard serial I/O mode 2 ..... Clock asynchronous serial I/O used to connect to a serial programmer
- Standard serial I/O mode 3 ..... Special clock asynchronous serial I/O used to connect to a serial programmer

Standard serial I/O mode 2 and standard serial I/O mode 3 can be used for the MCU.

Refer to **Appendix 2. Connection Examples between Serial Programmer and On-Chip Debugging Emulator** for examples of connecting to a serial programmer. Contact the serial programmer manufacturer for more information. Refer to the user's manual included with your serial programmer for instructions.

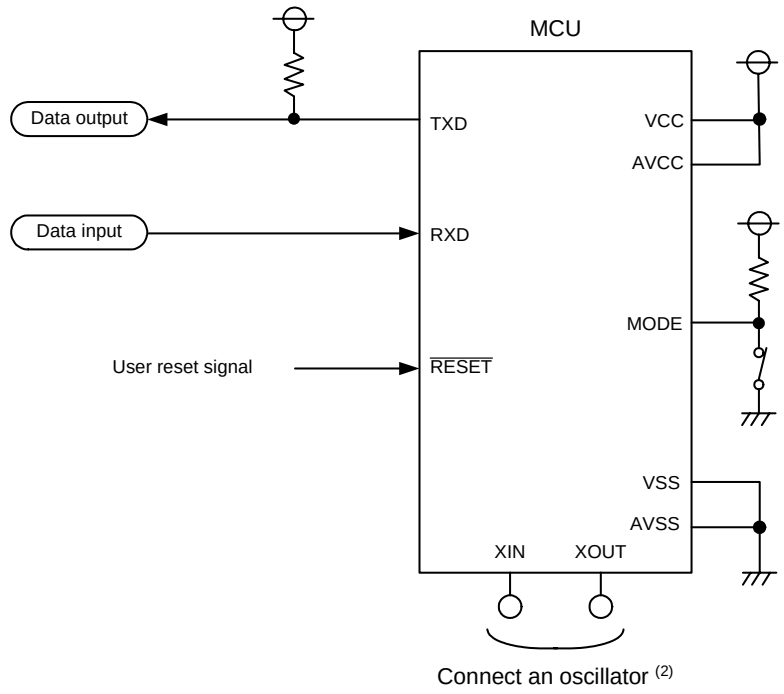
Table 22.7 lists the Pin Functions (Flash Memory Standard Serial I/O Mode 2) and Figure 22.16 shows Pin Handling in Standard Serial I/O Mode 2. Table 22.8 lists the Pin Functions (Flash Memory Standard Serial I/O Mode 3) and Figure 22.17 shows Pin Handling in Standard Serial I/O Mode 3.
After handling the pins shown in Table 22.8 and rewriting the flash memory using the programmer, apply a "H" level signal to the MODE pin and reset the hardware to run a program in the flash memory in single-chip mode.

22.5.1 ID Code Check Function

The ID code check function determines whether the ID codes sent from the serial programmer and those written in the flash memory match.
Refer to **12. ID Code Areas** for details of the ID code check.

Table 22.7 Pin Functions (Flash Memory Standard Serial I/O Mode 2)

Pin	Name	I/O	Description
VCC, VSS	Power supply input		Apply the guaranteed programming and erasure voltage to the VCC pin and 0 V to the VSS pin.
$\overline{\text{RESET}}$	Reset input	I	Reset input pin
P4_6/XIN	P4_6 input/clock input	I	When operating with the on-chip oscillator clock, it is not necessary to connect an oscillation circuit. Operation is not affected even if an external oscillator is connected in the user system.
P4_7/XOUT	P4_7 input/clock output	I/O	
P0_0 to P0_2	Input port P0	I	Input a “H” or “L” level signal or leave open.
P1_0 to P1_3, P1_6, P1_7	Input port P1	I	Input a “H” or “L” level signal or leave open.
P3_0, P3_1, P3_3 to P3_5, P3_7	Input port P3	I	Input a “H” or “L” level signal or leave open.
P4_5	Input port P4	I	Input a “H” or “L” level signal or leave open.
MODE	MODE	I/O	Input a “L” level signal.
P1_4	TXD output	O	Serial data output pin
P1_5	RXD input	I	Serial data input pin

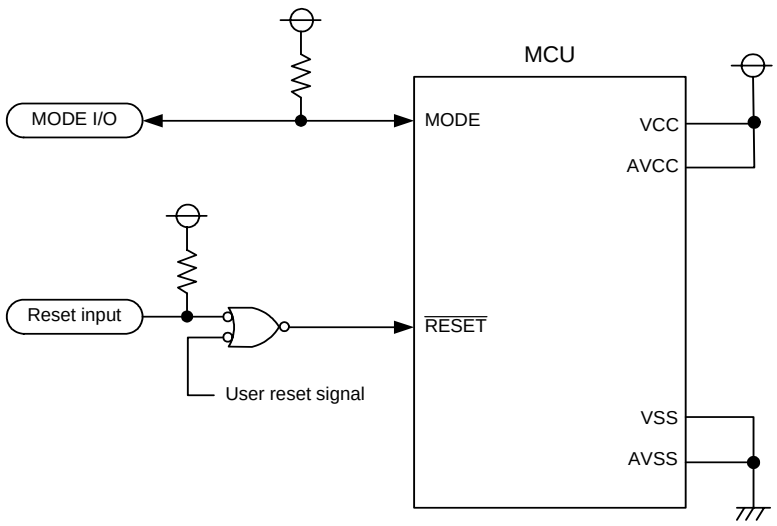


Notes:
1. In this example, modes are switched between single-chip mode and standard serial I/O mode by controlling the MODE input with a switch.
2. When operating with the on-chip oscillator clock, it is not necessary to connect an oscillation circuit. Refer to **Appendix Figure 2.1 Connection Example with MF Ten Nine Cable (M3A-0652CBL)**.

Figure 22.16 Pin Handling in Standard Serial I/O Mode 2

Table 22.8 Pin Functions (Flash Memory Standard Serial I/O Mode 3)

Pin	Name	I/O	Description
VCC, VSS	Power supply input		Apply the guaranteed programming and erasure voltage to the VCC pin and 0 V to the VSS pin.
$\overline{\text{RESET}}$	Reset input	I	Reset input pin
P4_6/XIN	P4_6 input/clock input	I	When operating with the on-chip oscillator clock, it is not necessary to connect an oscillation circuit. Operation is not affected even if an external oscillator is connected in the user system.
P4_7/XOUT	P4_7 input/clock output	I/O	
P0_0 to P0_2	Input port P0	I	Input a “H” or “L” level signal or leave open.
P1_0 to P1_7	Input port P1	I	Input a “H” or “L” level signal or leave open.
P3_0, P3_1, P3_3 to P3_5, P3_7	Input port P3	I	Input a “H” or “L” level signal or leave open.
P4_5	Input port P4	I	Input a “H” or “L” level signal or leave open.
MODE	MODE	I/O	Serial data I/O pin. Connect the pin to a programmer.



Notes:
1. Controlled pins and external circuits vary depending on the programmer. Refer to the programmer manual for details.
2. In this example, modes are switched between single-chip mode and standard serial I/O mode by connecting a programmer.
3. When operating with the on-chip oscillator clock, it is not necessary to connect an oscillation circuit.

Figure 22.17 Pin Handling in Standard Serial I/O Mode 3

22.6 Parallel I/O Mode

Parallel I/O mode is used to input and output software commands, addresses and data necessary to control (read, program, and erase) the on-chip flash memory.
Use a parallel programmer which supports the MCU. Contact the parallel programmer manufacturer for more information. Refer to the user's manual included with your parallel programmer for instructions.
In parallel I/O mode, the user ROM areas shown in Figure 22.1 can be rewritten.

22.6.1 ROM Code Protect Function

The ROM code protect function prevents the flash memory from being read and rewritten. (Refer to **22.3.2 ROM Code Protect Function**.)

22.7 Notes on Flash Memory

22.7.1 CPU Rewrite Mode

22.7.1.1 Prohibited Instructions

The following instructions cannot be used while the program ROM area is being rewritten in EW0 mode because they reference data in the flash memory: UND, INTO, and BRK.

22.7.1.2 Interrupts

Tables 22.9 to 22.10 list CPU Rewrite Mode Interrupts.

Table 22.9 CPU Rewrite Mode Interrupts (1)

Mode	Erase/ Write Target	Status	Maskable Interrupt
EW0	Program ROM	During auto-erasure (suspend enabled)	Usable by allocating a vector in RAM.
		During auto-erasure (suspend disabled)	
		During auto-programming	
EW1	Program ROM	During auto-erasure (suspend enabled)	Auto-erasure suspends after td(SR-SUS) and interrupt handling is executed. Auto-erasure can be restarted by setting the FMR21 bit to 0 after interrupt handling completes. While auto-erasure is being suspended, any block other than the block during auto-erasure execution can be read or written.
		During auto-erasure (suspend disabled or FMR22 = 0)	Auto-erasure and auto-programming have priority and interrupt requests are put on standby. Interrupt handling is executed after auto-erase and auto-program complete.
		During auto-programming	

FMR21, FMR22: Bits in FMR2 register

Table 22.10 CPU Rewrite Mode Interrupts (2)

Mode	Erase/ Write Target	Status	• Watchdog Timer • Oscillation Stop Detection • Voltage Monitor 2 • Voltage Monitor 1 (Note 1)	• Undefined Instruction • INTO Instruction • BRK Instruction • Single Step • Address Match • Address Break (Note 1)
EW0	Program ROM	During auto-erasure (suspend enabled)	When an interrupt request is acknowledged, auto-erasure or auto-programming is forcibly stopped immediately and the flash memory is reset. Interrupt handling starts when the flash memory restarts after the fixed period. Since the block during auto-erasure or the address during auto-programming is forcibly stopped, the normal value may not be read. After the flash memory restarts, execute auto-erasure again and ensure it completes normally. The watchdog timer does not stop during the command operation, so interrupt requests may be generated. Initialize the watchdog timer regularly using the erase-suspend function.	Not usable during auto-erasure or auto-programming.
		During auto-erasure (suspend disabled)		
		During auto-programming		
EW1	Program ROM	During auto-erasure (suspend enabled)	When an interrupt request is acknowledged, auto-erasure or auto-programming is forcibly stopped immediately and the flash memory is reset. Interrupt handling starts when the flash memory restarts after the fixed period. Since the block during auto-erasure or the address during auto-programming is forcibly stopped, the normal value may not be read. After the flash memory restarts, execute auto-erasure again and ensure it completes normally. The watchdog timer does not stop during the command operation, so interrupt requests may be generated. Initialize the watchdog timer regularly using the erase-suspend function.	Not usable during auto-erasure or auto-programming.
		During auto-erasure (suspend disabled or FMR22 = 0)		
		During auto-programming		

FMR21, FMR22: Bits in FMR2 register

Note:

1. Do not use a non-maskable interrupt while block 0 is being auto-erased because the fixed vector is allocated in block 0.

22.7.1.3 How to Access

To set one of the following bits to 1, first write 0 and then 1 immediately. Disable interrupts and DTC activation between writing 0 and writing 1.
- The FMR01 bit or FMR02 bit in the FMR0 register
- The FMR13 bit in the FMR1 register
- The FMR20 bit, FMR22 bit, or FMR 27 bit in the FMR2 register

To set one of the following bits to 0, first write 1 and then 0 immediately. Disable interrupts and DTC activation between writing 1 and writing 0.
- The FMR14 bit, FMR15 bit, FMR16 bit, or FMR17 bit in the FMR1 register

22.7.1.4 Rewriting User ROM Area

In EW0 mode, if the supply voltage drops while rewriting any block in which a rewrite control program is stored, it may not be possible to rewrite the flash memory because the rewrite control program cannot be rewritten correctly. In this case, use standard serial I/O mode.

22.7.1.5 Programming

Do not write additions to the already programmed address.

22.7.1.6 Entering Stop Mode or Wait Mode

Do not enter stop mode or wait mode during erase-suspend.
If the FST7 bit in the FST register is set to 0 (busy (during programming or erasure execution), do not enter to stop mode or wait mode.
Do not enter stop mode or wait mode while the FMR27 bit is 1 (low-current-consumption read mode enabled).

22.7.1.7 Programming and Erasure Voltage for Flash Memory

To perform programming and erasure, use VCC = 2.7 V to 5.5 V as the supply voltage. Do not perform programming and erasure at less than 2.7 V.

22.7.1.8 Block Blank Check

Do not execute the block blank check command during erase-suspend.

22.7.1.9 Low-Current-Consumption Read Mode

In low-speed on-chip oscillator mode, the current consumption when reading the flash memory can be reduced by setting the FMR27 bit in the FMR2 register to 1 (low-current-consumption read mode enabled).
When the CPU clock is set to the low-speed on-chip oscillator clock divided by 4, 8, or 16, low-consumption-current read mode can be used. When divided by 1 (no division) or divided by 2 is set, do not use low-consumption-current read mode. After setting the divide ratio of the CPU clock, set the FMR27 bit to 1.
To reduce the power consumption, refer to **23. Reducing Power Consumption**.
Enter wait mode or stop mode after setting the FMR27 bit to 0 (low-current-consumption read mode disabled).
Do not enter wait mode or stop mode while the FMR27 bit is 1 (low-current-consumption read mode enabled).

23. Reducing Power Consumption

23.1 Overview

This chapter describes key points and processing methods for reducing power consumption.

23.2 Key Points and Processing Methods for Reducing Power Consumption

Key points for reducing power consumption are shown below. They should be referred to when designing a system or creating a program.

23.2.1 Voltage Detection Circuit

If voltage monitor 1 is not used, set the VCA26 bit in the VCA2 register to 0 (voltage detection 1 circuit disabled). If voltage monitor 2 is not used, set the VCA27 bit in the VCA2 register to 0 (voltage detection 2 circuit disabled).
If the power-on reset and voltage monitor 0 reset are not used, set the VCA25 bit in the VCA2 register to 0 (voltage detection 0 circuit disabled).

23.2.2 Ports

Even after the MCU enters wait mode or stop mode, the states of the I/O ports are retained. Current flows into the output ports in the active state, and shoot-through current flows into the input ports in the high-impedance state. Unnecessary ports should be set to input and fixed to a stable electric potential before the MCU enters wait mode or stop mode.

23.2.3 Clocks

Power consumption generally depends on the number of the operating clocks and their frequencies. The fewer the number of operating clocks or the lower their frequencies, the more power consumption decreases. Unnecessary clocks should be stopped accordingly.

Stopping low-speed on-chip oscillator oscillation:	Set the CM14 bit in the CM1 register to 1 (low-speed on-chip oscillator off) and the OCD2 bit in the OCD register to 0 (XIN clock selected).
Stopping high-speed on-chip oscillator oscillation:	Set the FRA00 bit in the FRA0 register to 0.

23.2.4 Wait Mode, Stop Mode

Power consumption can be reduced in wait mode and stop mode. Refer to **9.6 Power Control** for details.

23.2.5 Stopping Peripheral Function Clocks

If the peripheral function f1, f2, f4, f8, and f32 clocks are not necessary in wait mode, set the CM02 bit in the CM0 register to 1 (peripheral function clock stops in wait mode). This will stop the f1, f2, f4, f8, and f32 clocks in wait mode.

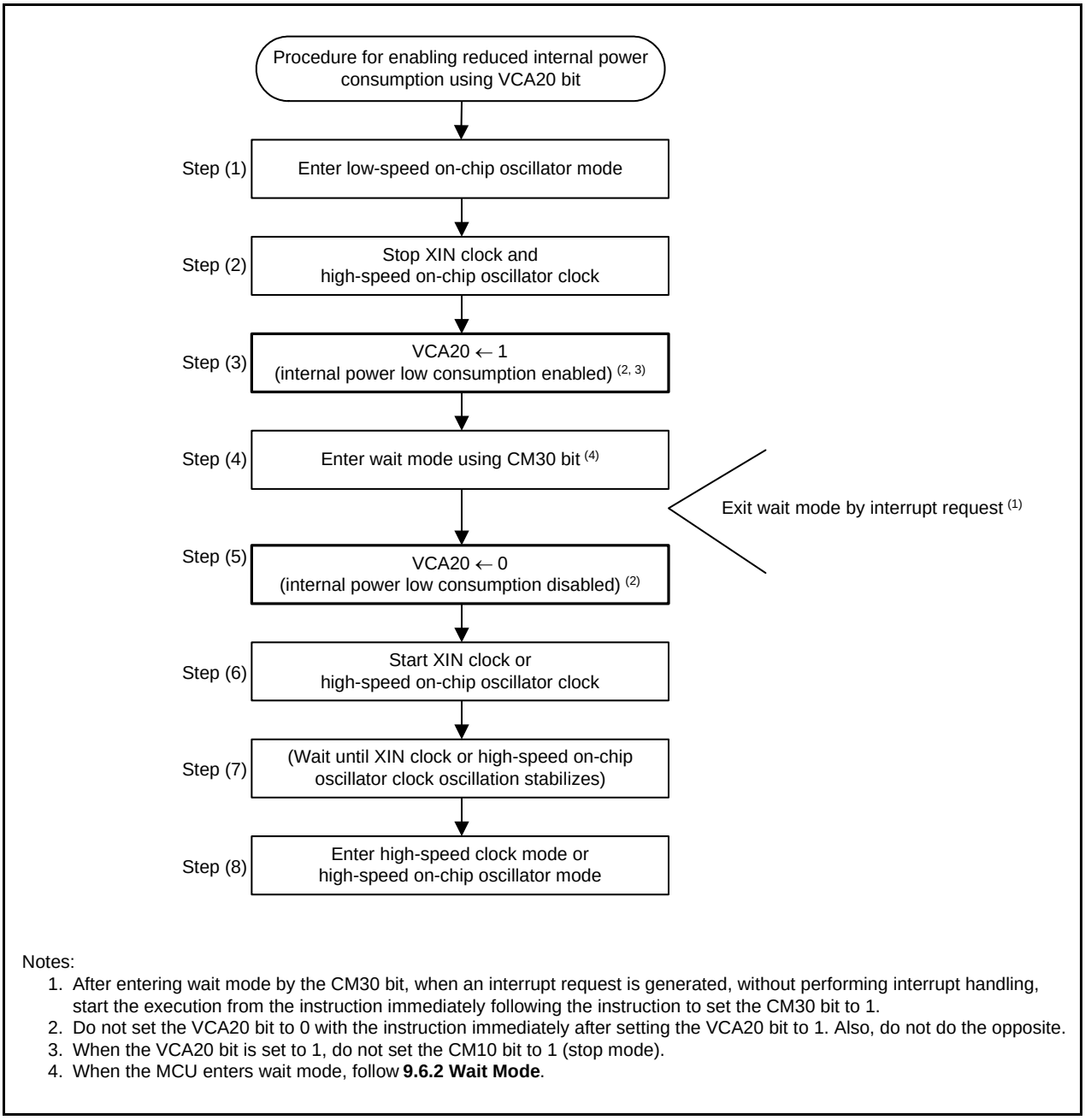
23.2.6 Timers

If timer RA is not used, set the TCKCUT bit in the TRAMR register to 1 (count source cutoff).
If timer RB is not used, set the TCKCUT bit in the TRBMR register to 1 (count source cutoff).
If timer RC is not used, set the MSTTRC bit in the MSTCR register to 1 (standby).

23.2.7 Reducing Internal Power Consumption Using VCA20 Bit

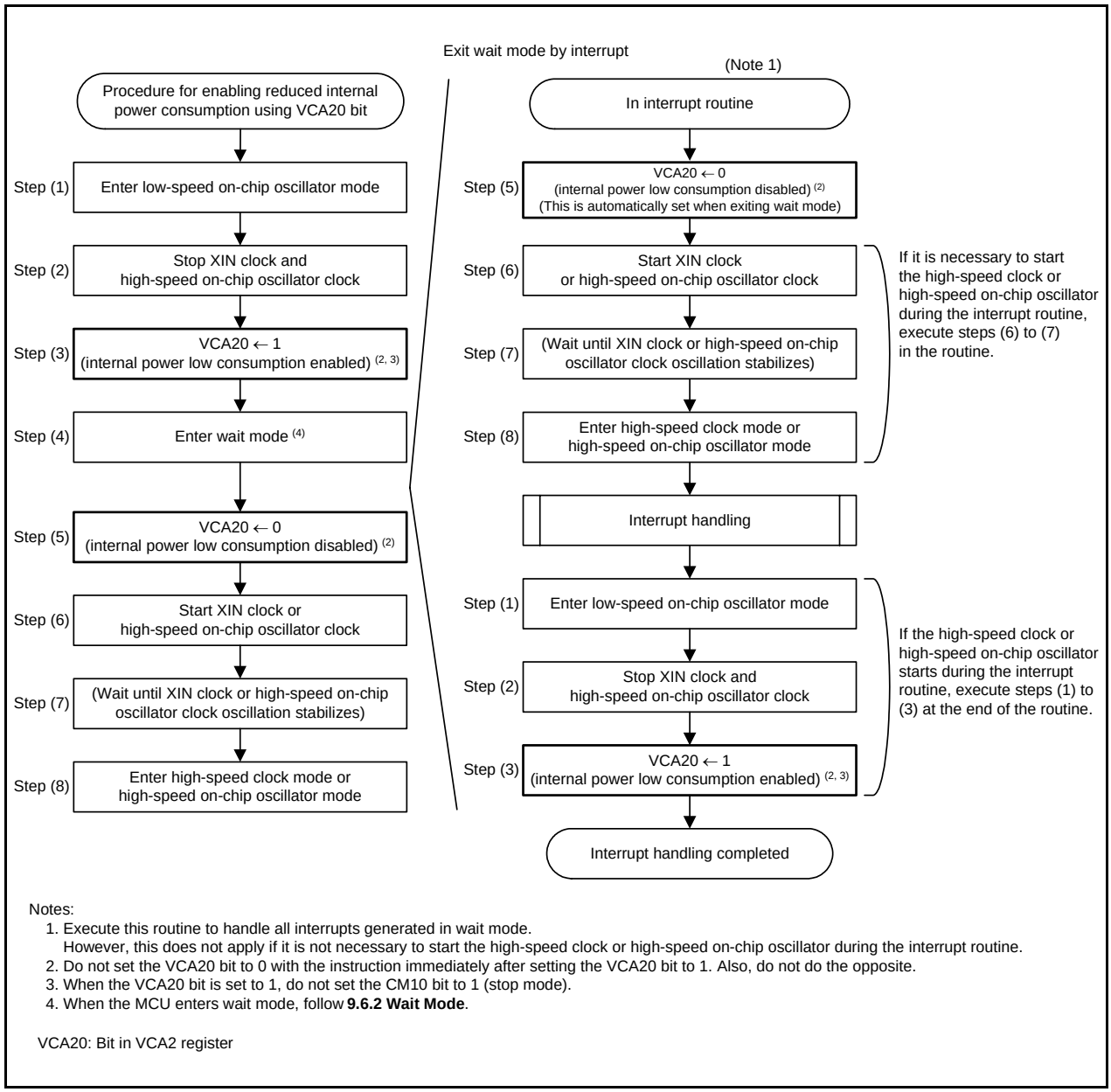
The electric current in wait mode can be further reduced by setting the VCA20 bit in the VCA2 register to 1 (low consumption enabled). Set the VCA20 bit to 1 in low-speed on-chip oscillator mode before entering wait mode.

The setting procedure for reducing internal power consumption using the VCA20 bit differs when the CM30 bit in the CM3 register is set to 1 (MCU enters wait mode) to enter wait mode and when the WAIT instruction is executed to enter wait mode. Figure 23.1 shows the Setting Procedure for Reducing Internal Power Consumption Using VCA20 Bit when CM30 Bit in CM3 Register is Set to 1 (MCU Enters Wait Mode) to Enter Wait Mode. Figure 23.2 shows the Setting Procedure for Reducing Internal Power Consumption Using VCA20 Bit when WAIT Instruction is Executed to Enter Wait Mode.



Notes:
1. After entering wait mode by the CM30 bit, when an interrupt request is generated, without performing interrupt handling, start the execution from the instruction immediately following the instruction to set the CM30 bit to 1.
2. Do not set the VCA20 bit to 0 with the instruction immediately after setting the VCA20 bit to 1. Also, do not do the opposite.
3. When the VCA20 bit is set to 1, do not set the CM10 bit to 1 (stop mode).
4. When the MCU enters wait mode, follow **9.6.2 Wait Mode**.

Figure 23.1 Setting Procedure for Reducing Internal Power Consumption Using VCA20 Bit when CM30 Bit in CM3 Register is Set to 1 (MCU Enters Wait Mode) to Enter Wait Mode



Notes:
1. Execute this routine to handle all interrupts generated in wait mode.
   However, this does not apply if it is not necessary to start the high-speed clock or high-speed on-chip oscillator during the interrupt routine.
2. Do not set the VCA20 bit to 0 with the instruction immediately after setting the VCA20 bit to 1. Also, do not do the opposite.
3. When the VCA20 bit is set to 1, do not set the CM10 bit to 1 (stop mode).
4. When the MCU enters wait mode, follow **9.6.2 Wait Mode**.

VCA20: Bit in VCA2 register

Figure 23.2 Setting Procedure for Reducing Internal Power Consumption Using VCA20 Bit when WAIT Instruction is Executed to Enter Wait Mode

23.2.8 Stopping Flash Memory

In low-speed on-chip oscillator mode, power consumption can be further reduced by stopping the flash memory using the FMSTP bit in the FMR0 register.

Access to the flash memory is disabled by setting the FMSTP bit to 1 (flash memory stops). The FMSTP bit must be written to by a program transferred to RAM.

When the MCU enters stop mode or wait mode while CPU rewrite mode is disabled, the power for the flash memory is automatically turned off. It is turned back on again after the MCU exits stop mode or wait mode. This eliminates the need to set the FMR0 register.

Figure 23.3 shows the Handling Procedure Example for Reducing Power Consumption Using FMSTP Bit.

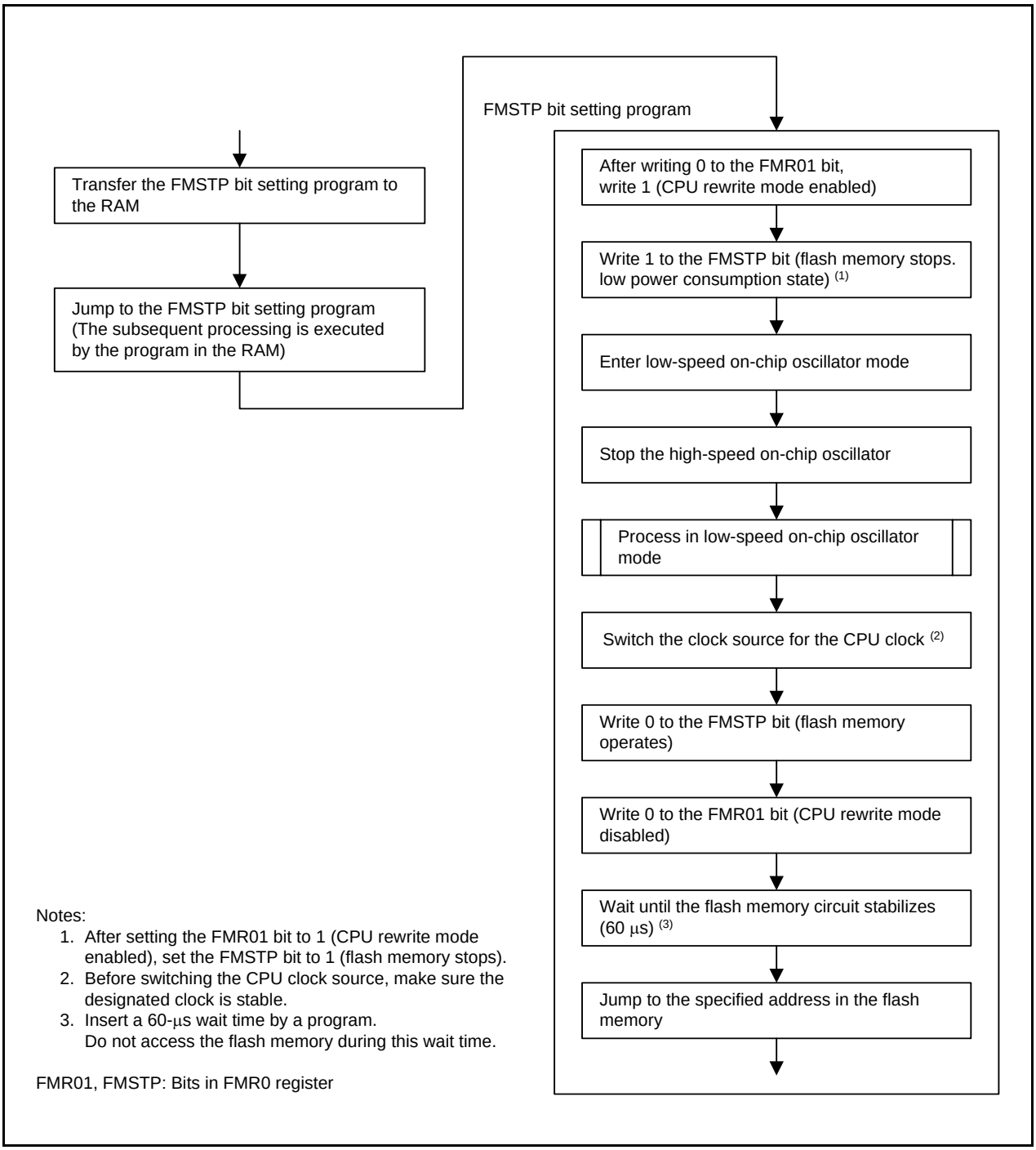
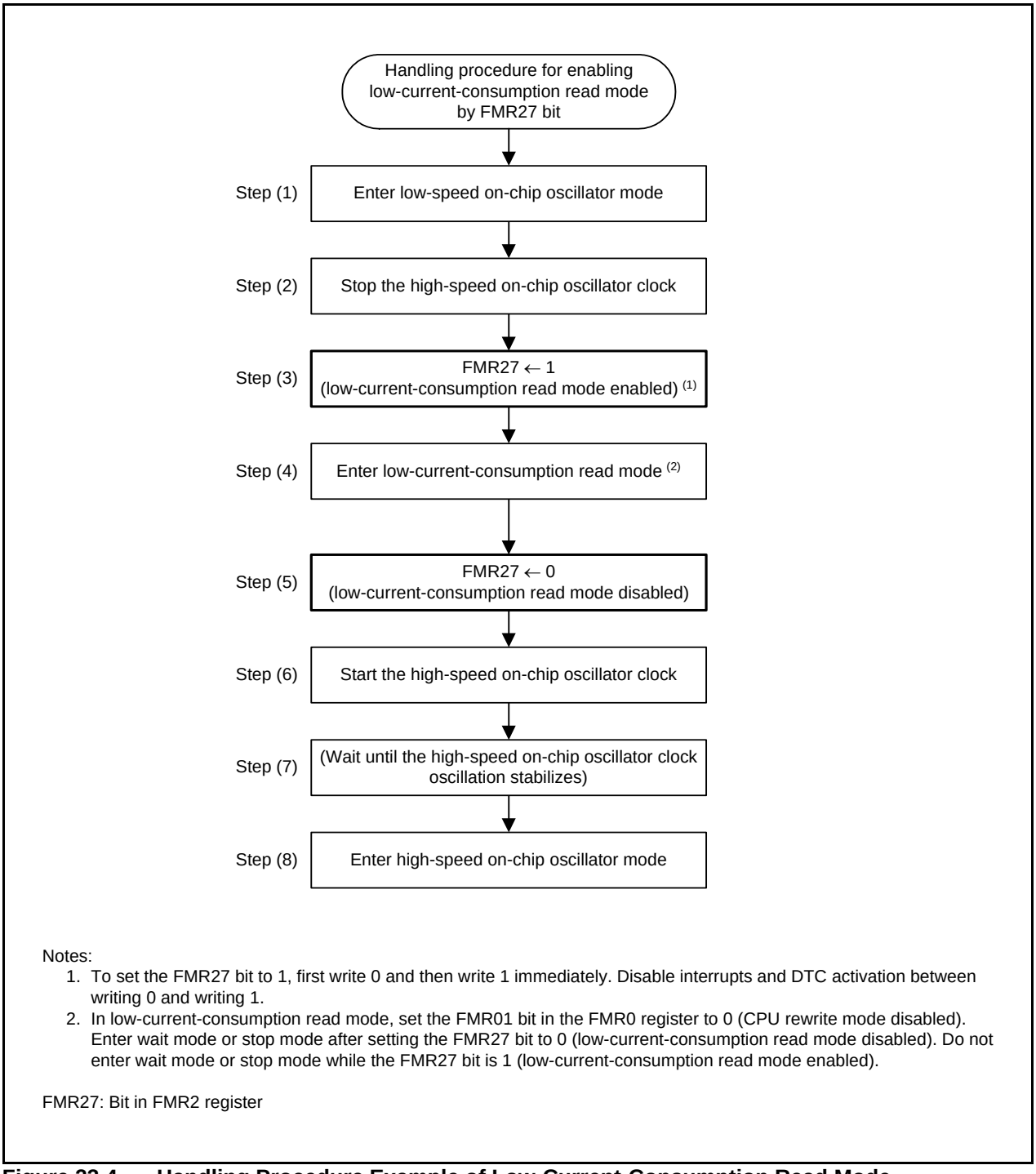


Figure 23.3 Handling Procedure Example for Reducing Power Consumption Using FMSTP Bit

23.2.9 Low-Current-Consumption Read Mode

In low-speed on-chip oscillator mode, the current consumption when reading the flash memory can be reduced by setting the FMR27 bit in the FMR2 register to 1 (low-current-consumption read mode enabled).
When the CPU clock is set to the low-speed on-chip oscillator clock divided by 4, 8, or 16, low-consumption-current read mode can be used. When divided by 1 (no division) or divided by 2 is set, do not use low-consumption-current read mode. After setting the divide ratio of the CPU clock, set the FMR27 bit to 1 (low-current-consumption read mode enabled).
Enter wait mode or stop mode after setting the FMR27 bit to 0 (low-current-consumption read mode disabled). Do not enter wait mode or stop mode while the FMR27 bit is 1 (low-current-consumption read mode enabled).
Figure 23.4 shows the Handling Procedure Example of Low-Current-Consumption Read Mode.



Notes:
1. To set the FMR27 bit to 1, first write 0 and then write 1 immediately. Disable interrupts and DTC activation between writing 0 and writing 1.
2. In low-current-consumption read mode, set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled). Enter wait mode or stop mode after setting the FMR27 bit to 0 (low-current-consumption read mode disabled). Do not enter wait mode or stop mode while the FMR27 bit is 1 (low-current-consumption read mode enabled).

FMR27: Bit in FMR2 register

Figure 23.4 Handling Procedure Example of Low-Current-Consumption Read Mode

24. Electrical Characteristics

Table 24.1 Absolute Maximum Ratings

Symbol	Parameter	Condition	Rated Value	Unit
V_{CC}/AV_{CC}	Supply voltage		−0.3 to 6.5	V
V_I	Input voltage		−0.3 to Vcc + 0.3	V
V_O	Output voltage		−0.3 to Vcc + 0.3	V
P_d	Power dissipation	−20°C ≤ Topr ≤ 85°C	500	mW
T_{opr}	Operating ambient temperature		−20 to 85	°C
T_{stg}	Storage temperature		−65 to 150	°C

Table 24.2 Recommended Operating Conditions

Symbol	Parameter				Conditions	Standard			Unit
						Min.	Typ.	Max.	
V_{CC}/AV_{CC}	Supply voltage					1.8	—	5.5	V
V_{SS}/AV_{SS}	Supply voltage					—	0	—	V
V_{IH}	Input “H” voltage	Other than CMOS input				0.8 Vcc	—	Vcc	V
		CMOS input	Input level switching function (I/O port)	Input level selection : 0.35 Vcc	4.0 V ≤ Vcc ≤ 5.5 V	0.5 Vcc	—	Vcc	V
					2.7 V ≤ Vcc < 4.0 V	0.55 Vcc	—	Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0.65 Vcc	—	Vcc	V
				Input level selection : 0.5 Vcc	4.0 V ≤ Vcc ≤ 5.5 V	0.65 Vcc	—	Vcc	V
					2.7 V ≤ Vcc < 4.0 V	0.7 Vcc	—	Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0.8 Vcc	—	Vcc	V
				Input level selection : 0.7 Vcc	4.0 V ≤ Vcc ≤ 5.5 V	0.85 Vcc	—	Vcc	V
					2.7 V ≤ Vcc < 4.0 V	0.85 Vcc	—	Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0.85 Vcc	—	Vcc	V
		External clock input (XOUT)				1.2	—	Vcc	V
V_{IL}	Input “L” voltage	Other than CMOS input				0	—	0.2 Vcc	V
		CMOS input	Input level switching function (I/O port)	Input level selection : 0.35 Vcc	4.0 V ≤ Vcc ≤ 5.5 V	0	—	0.2 Vcc	V
					2.7 V ≤ Vcc < 4.0 V	0	—	0.2 Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0	—	0.2 Vcc	V
				Input level selection : 0.5 Vcc	4.0 V ≤ Vcc ≤ 5.5 V	0	—	0.4 Vcc	V
					2.7 V ≤ Vcc < 4.0 V	0	—	0.3 Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0	—	0.2 Vcc	V
				Input level selection : 0.7 Vcc	4.0 V ≤ Vcc ≤ 5.5 V	0	—	0.55 Vcc	V
					2.7 V ≤ Vcc < 4.0 V	0	—	0.45 Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0	—	0.35 Vcc	V
		External clock input (XOUT)				0	—	0.4 Vcc	V
$I_{OH(sum)}$	Peak sum output “H” current	Sum of all pins $I_{OH(peak)}$				—	—	−160	mA
$I_{OH(sum)}$	Average sum output “H” current	Sum of all pins $I_{OH(avg)}$				—	—	−80	mA
$I_{OH(peak)}$	Peak output “H” current	Drive capacity Low				—	—	−10	mA
		Drive capacity High				—	—	−40	mA
$I_{OH(avg)}$	Average output “H” current	Drive capacity Low				—	—	−5	mA
		Drive capacity High				—	—	−20	mA
$I_{OL(sum)}$	Peak sum output “L” current	Sum of all pins $I_{OL(peak)}$				—	—	160	mA
$I_{OL(sum)}$	Average sum output “L” current	Sum of all pins $I_{OL(avg)}$				—	—	80	mA
$I_{OL(peak)}$	Peak output “L” current	Drive capacity Low				—	—	10	mA
		Drive capacity High				—	—	40	mA
$I_{OL(avg)}$	Average output “L” current	Drive capacity Low				—	—	5	mA
		Drive capacity High				—	—	20	mA
$f_{(XIN)}$	XIN clock input oscillation frequency				2.7 V ≤ Vcc ≤ 5.5 V	—	—	20	MHz
					1.8 V ≤ Vcc < 2.7 V	—	—	5	MHz
fOCO40M	When used as the count source for timer RC (3)				2.7 V ≤ Vcc ≤ 5.5 V	32	—	40	MHz
fOCO-F	fOCO-F frequency				2.7 V ≤ Vcc ≤ 5.5 V	—	—	20	MHz
					1.8 V ≤ Vcc < 2.7 V	—	—	5	MHz
—	System clock frequency				2.7 V ≤ Vcc ≤ 5.5 V	—	—	20	MHz
					1.8 V ≤ Vcc < 2.7 V	—	—	5	MHz
$f_{(BCLK)}$	CPU clock frequency				2.7 V ≤ Vcc ≤ 5.5 V	—	—	20	MHz
					1.8 V ≤ Vcc < 2.7 V	—	—	5	MHz

Notes:
1. Vcc = 1.8 V to 5.5 V at Topr = −20°C to 85°C, unless otherwise specified.
2. The average output current indicates the average value of current measured during 100 ms.
3. fOCO40M can be used as the count source for timer RC in the range of Vcc = 2.7 V to 5.5 V.

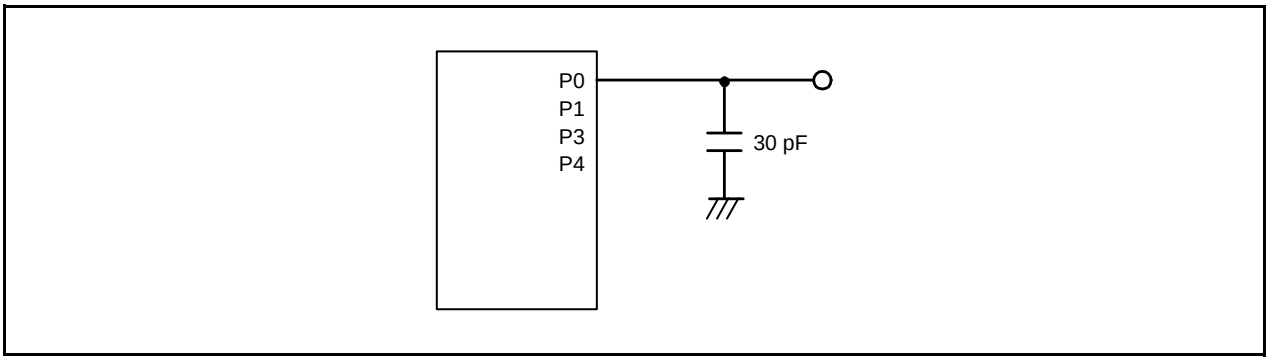


Figure 24.1 Ports P0, P1, P3, P4 Timing Measurement Circuit

Table 24.3 Flash Memory (Program ROM) Electrical Characteristics

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
—	Program/erase endurance (2)		1,000 (3)	—	—	times
—	Byte program time		—	80	500	µs
—	Block erase time		—	0.3	—	s
$t_{d(SR-SUS)}$	Time delay from suspend request until suspend		—	—	5 + CPU clock × 3 cycles	ms
—	Interval from erase start/restart until following suspend request		0	—	—	µs
—	Time from suspend until erase restart		—	—	30 + CPU clock × 1 cycle	µs
$t_{d(CMDRST-READY)}$	Time from when command is forcibly terminated until reading is enabled		—	—	30 + CPU clock × 1 cycle	µs
—	Program, erase voltage		2.7	—	5.5	V
—	Read voltage		1.8	—	5.5	V
—	Program, erase temperature		0	—	60	°C
—	Data hold time (7)	Ambient temperature = 55°C	20	—	—	year

Notes:
1. Vcc = 2.7 V to 5.5 V at Topr = 0°C to 60°C, unless otherwise specified.
2. Definition of programming/erasure endurance
   The programming and erasure endurance is defined on a per-block basis.
   If the programming and erasure endurance is n (n = 1,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.
   However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
4. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
5. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
6. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
7. The data hold time includes time that the power supply is off or the clock is not supplied.

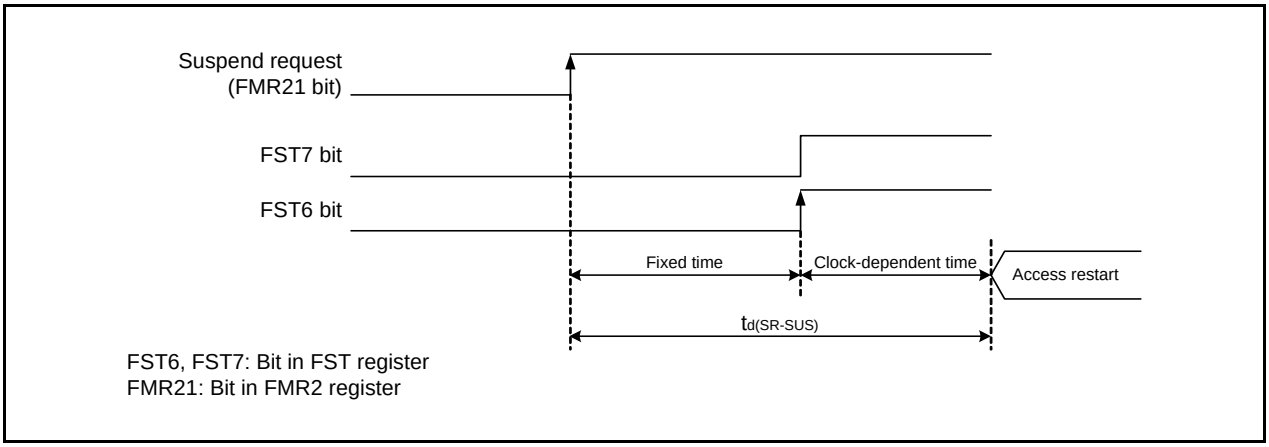


Figure 24.2 Time delay until Suspend

Table 24.4 Voltage Detection 0 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det0}	Voltage detection level Vdet0_0 (2)		1.80	1.90	2.05	V
	Voltage detection level Vdet0_1 (2)		2.15	2.35	2.50	V
	Voltage detection level Vdet0_2 (2)		2.70	2.85	3.05	V
	Voltage detection level Vdet0_3 (2)		3.55	3.80	4.05	V
—	Voltage detection 0 circuit response time (4)	At the falling of Vcc from 5 V to (Vdet0_0 – 0.1) V	—	6	150	µs
—	Voltage detection circuit self power consumption	VCA25 = 1, Vcc = 5.0 V	—	1.5	—	µA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts (3)		—	—	100	µs

Notes:
1. The measurement condition is Vcc = 1.8 V to 5.5 V and Topr = –20°C to 85°C.
2. Select the voltage detection level with bits VDSEL0 and VDSEL1 in the OFS register.
3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA25 bit in the VCA2 register to 0.
4. Time until the voltage monitor 0 reset is generated after the voltage passes V_{det0}.

Table 24.5 Voltage Detection 1 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det1}	Voltage detection level Vdet1_0 (2)	At the falling of Vcc	2.00	2.20	2.40	V
	Voltage detection level Vdet1_1 (2)	At the falling of Vcc	2.15	2.35	2.55	V
	Voltage detection level Vdet1_2 (2)	At the falling of Vcc	2.30	2.50	2.70	V
	Voltage detection level Vdet1_3 (2)	At the falling of Vcc	2.45	2.65	2.85	V
	Voltage detection level Vdet1_4 (2)	At the falling of Vcc	2.60	2.80	3.00	V
	Voltage detection level Vdet1_5 (2)	At the falling of Vcc	2.75	2.95	3.15	V
	Voltage detection level Vdet1_6 (2)	At the falling of Vcc	2.85	3.10	3.40	V
	Voltage detection level Vdet1_7 (2)	At the falling of Vcc	3.00	3.25	3.55	V
	Voltage detection level Vdet1_8 (2)	At the falling of Vcc	3.15	3.40	3.70	V
	Voltage detection level Vdet1_9 (2)	At the falling of Vcc	3.30	3.55	3.85	V
	Voltage detection level Vdet1_A (2)	At the falling of Vcc	3.45	3.70	4.00	V
	Voltage detection level Vdet1_B (2)	At the falling of Vcc	3.60	3.85	4.15	V
	Voltage detection level Vdet1_C (2)	At the falling of Vcc	3.75	4.00	4.30	V
	Voltage detection level Vdet1_D (2)	At the falling of Vcc	3.90	4.15	4.45	V
	Voltage detection level Vdet1_E (2)	At the falling of Vcc	4.05	4.30	4.60	V
	Voltage detection level Vdet1_F (2)	At the falling of Vcc	4.20	4.45	4.75	V
—	Hysteresis width at the rising of Vcc in voltage detection 1 circuit	Vdet1_0 to Vdet1_5 selected	—	0.07	—	V
		Vdet1_6 to Vdet1_F selected	—	0.10	—	V
—	Voltage detection 1 circuit response time (3)	At the falling of Vcc from 5 V to (Vdet1_0 – 0.1) V	—	60	150	µs
—	Voltage detection circuit self power consumption	VCA26 = 1, Vcc = 5.0 V	—	1.7	—	µA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts (4)		—	—	100	µs

Notes:
1. The measurement condition is Vcc = 1.8 V to 5.5 V and Topr = –20°C to 85°C.
2. Select the voltage detection level with bits VD1S0 to VD1S3 in the VD1LS register.
3. Time until the voltage monitor 1 interrupt request is generated after the voltage passes V_{det1}.
4. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.

Table 24.6 Voltage Detection 2 Circuit Electrical Characteristics

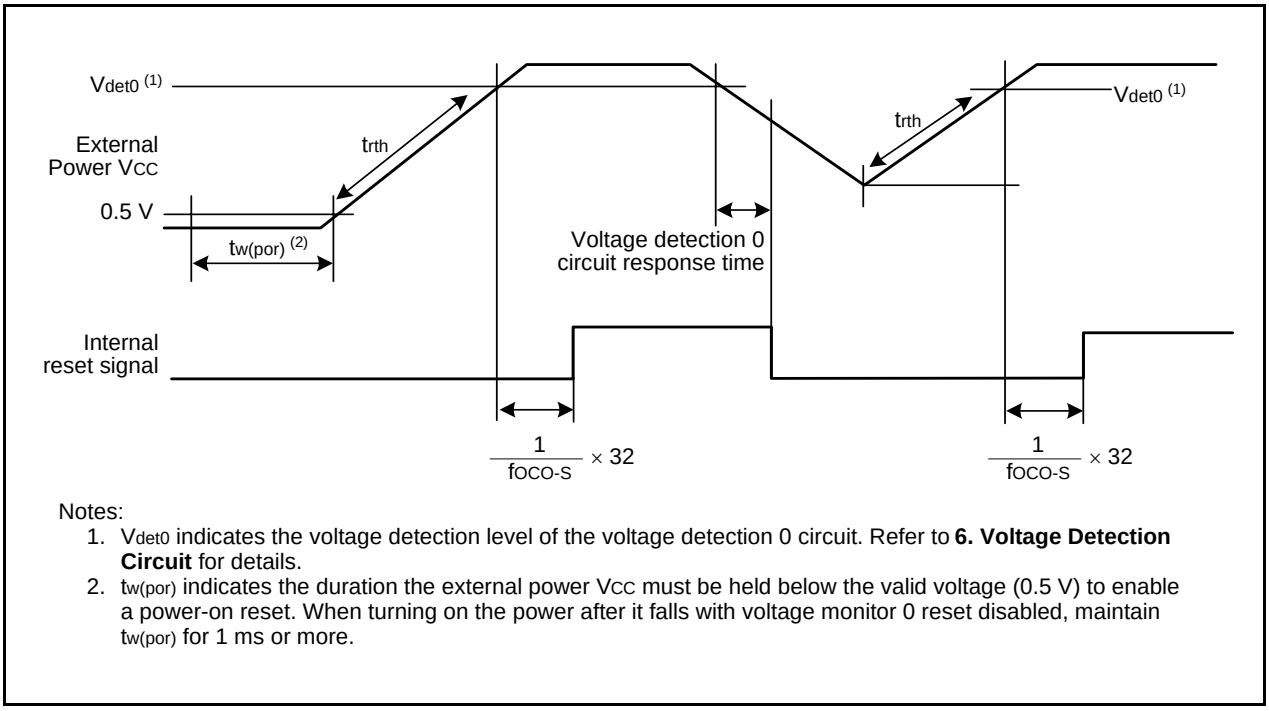
Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det2}	Voltage detection level Vdet2_0	At the falling of Vcc	3.70	4.00	4.30	V
—	Hysteresis width at the rising of Vcc in voltage detection 2 circuit		—	0.10	—	V
—	Voltage detection 2 circuit response time (2)	At the falling of Vcc from 5 V to (Vdet2_0 – 0.1) V	—	20	150	µs
—	Voltage detection circuit self power consumption	VCA27 = 1, Vcc = 5.0 V	—	1.7	—	µA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts (3)		—	—	100	µs

Notes:
1. The measurement condition is Vcc = 1.8 V to 5.5 V and Topr = –20°C to 85°C.
2. Time until the voltage monitor 2 interrupt request is generated after the voltage passes V_{det2}.
3. Necessary time until the voltage detection circuit operates after setting to 1 again after setting the VCA27 bit in the VCA2 register to 0.

Table 24.7 Power-on Reset Circuit (2)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
t_{rth}	External power Vcc rise gradient	(Note 1)	0	—	50000	mV/msec

Notes:
1. The measurement condition is Topr = –20°C to 85°C, unless otherwise specified.
2. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVDAS bit in the OFS register to 0.



Notes:
1. V_{det0} indicates the voltage detection level of the voltage detection 0 circuit. Refer to **6. Voltage Detection Circuit** for details.
2. $t_{w(por)}$ indicates the duration the external power V_{CC} must be held below the valid voltage (0.5 V) to enable a power-on reset. When turning on the power after it falls with voltage monitor 0 reset disabled, maintain $t_{w(por)}$ for 1 ms or more.

Figure 24.3 Power-on Reset Circuit Electrical Characteristics

Table 24.8 High-speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
—	High-speed on-chip oscillator frequency after reset	Vcc = 2.7 V to 5.5 V −20°C ≤ Topr ≤ 85°C	38.4	40	41.6	MHz
	High-speed on-chip oscillator frequency when the FRA4 register correction value is written into the FRA1 register and the FRA5 register correction value into the FRA3 register (2)	Vcc = 2.7 V to 5.5 V −20°C ≤ Topr ≤ 85°C	35.389	36.864	38.338	MHz
	High-speed on-chip oscillator frequency when the FRA6 register correction value is written into the FRA1 register and the FRA7 register correction value into the FRA3 register	Vcc = 2.7 V to 5.5 V −20°C ≤ Topr ≤ 85°C	30.72	32	33.28	MHz
—	Oscillation stability time	Vcc = 5.0 V, Topr = 25°C	—	0.5	3	ms
—	Self power consumption at oscillation	Vcc = 5.0 V, Topr = 25°C	—	400	—	μA

Notes:
1. Vcc = 1.8 V to 5.5 V, Topr = −20°C to 85°C, unless otherwise specified.
2. This enables the setting errors of bit rates such as 9600 bps and 38400 bps to be 0% when the serial interface is used in UART mode.

Table 24.9 Low-speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
fOCO-S	Low-speed on-chip oscillator frequency		60	125	250	kHz
—	Oscillation stability time	Vcc = 5.0 V, Topr = 25°C	—	30	100	μs
—	Self power consumption at oscillation	Vcc = 5.0 V, Topr = 25°C	—	2	—	μA

Note:
1. Vcc = 1.8 V to 5.5 V, Topr = −20°C to 85°C, unless otherwise specified.

Table 24.10 Power Supply Circuit Timing Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
$t_{d(P-R)}$	Time for internal power supply stabilization during power-on (2)		—	—	2000	μs

Notes:
1. The measurement condition is Vcc = 1.8 V to 5.5 V and Topr = 25°C.
2. Waiting time until the internal power supply generation circuit stabilizes during power-on.

Table 24.11 Electrical Characteristics (1) [4.2 V ≤ Vcc ≤ 5.5 V]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	Output “H” voltage	Other than XOUT	Drive capacity High Vcc = 5 V	I_{OH} = –20 mA	Vcc – 2.0	—	Vcc	V
			Drive capacity Low Vcc = 5 V	I_{OH} = –5 mA	Vcc – 2.0	—	Vcc	V
		XOUT	Vcc = 5 V	I_{OH} = –200 μA	1.0	—	Vcc	V
V_{OL}	Output “L” voltage	Other than XOUT	Drive capacity High Vcc = 5 V	I_{OL} = 20 mA	—	—	2.0	V
			Drive capacity Low Vcc = 5 V	I_{OL} = 5 mA	—	—	2.0	V
		XOUT	Vcc = 5 V	I_{OL} = 200 μA	—	—	0.5	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$, $\overline{INT3}$, KI0, KI1, $\overline{KI2}$, $\overline{KI3}$, TRAIO, TRBO, TRCIOA, TRCIOB, TRCIOC, TRCIOD, TRCTRG, TRCCLK, RXD0, CLK0			0.1	1.2	—	V
		$\overline{RESET}$			0.1	1.2	—	V
I_{IH}	Input “H” current		V_I = 5 V, Vcc = 5.0 V		—	—	5.0	μA
I_{IL}	Input “L” current		V_I = 0 V, Vcc = 5.0 V		—	—	–5.0	μA
R_{PULLUP}	Pull-up resistance		V_I = 0 V, Vcc = 5.0 V		25	50	100	kΩ
R_{fXIN}	Feedback resistance	XIN			—	0.3	—	MΩ
V_{RAM}	RAM hold voltage		During stop mode		1.8	—	—	V

Note:
1. 4.2 V ≤ Vcc ≤ 5.5 V at Topr = –20°C to 85°C, f(XIN) = 20 MHz, unless otherwise specified.

Table 24.12 Electrical Characteristics (2) [3.3 V ≤ Vcc ≤ 5.5 V] (Topr = –20°C to 85°C, unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
Icc	Power supply current (Vcc = 3.3 V to 5.5 V) Single-chip mode, output pins are open, other pins are Vss	High-speed clock mode	XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	—	6.5	15	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	—	5.3	12.5	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	—	3.6	—	mA
			XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	—	3	—	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	—	2.2	—	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	—	1.5	—	mA
		High-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator on fOCO-F = 20 MHz Low-speed on-chip oscillator on = 125 kHz No division	—	7	15	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 20 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	—	3	—	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 4 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-16 MSTTRD = MSTTRC = 1	—	1	—	mA
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR27 = 1, VCA20 = 0	—	90	400	µA
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	—	15	100	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	—	4	90	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	—	3.5	—	µA
		Stop mode	XIN clock off, Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	—	2	5.0	µA
			XIN clock off, Topr = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	—	5	—	µA

Timing Requirements
(Unless Otherwise Specified: Vcc = 5 V, Vss = 0 V at Topr = 25°C)

Table 24.13 External Clock Input (XOUT)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XOUT)}$	XOUT input cycle time	50	—	ns
$t_{WH(XOUT)}$	XOUT input “H” width	24	—	ns
$t_{WL(XOUT)}$	XOUT input “L” width	24	—	ns

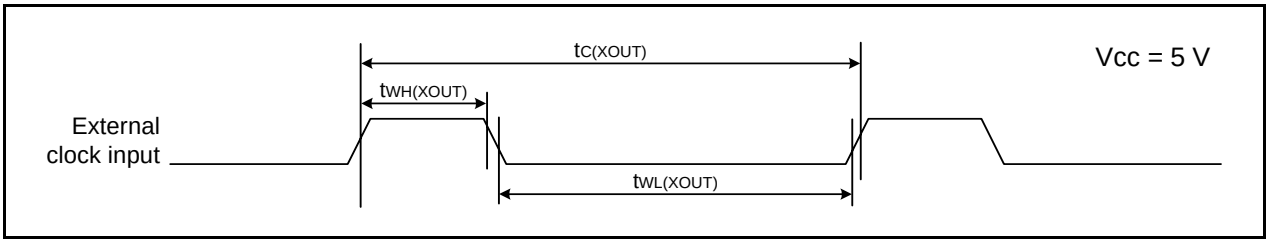


Figure 24.4 External Clock Input Timing Diagram when Vcc = 5 V

Table 24.14 TRAIO Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	100	—	ns
$t_{WH(TRAIO)}$	TRAIO input “H” width	40	—	ns
$t_{WL(TRAIO)}$	TRAIO input “L” width	40	—	ns

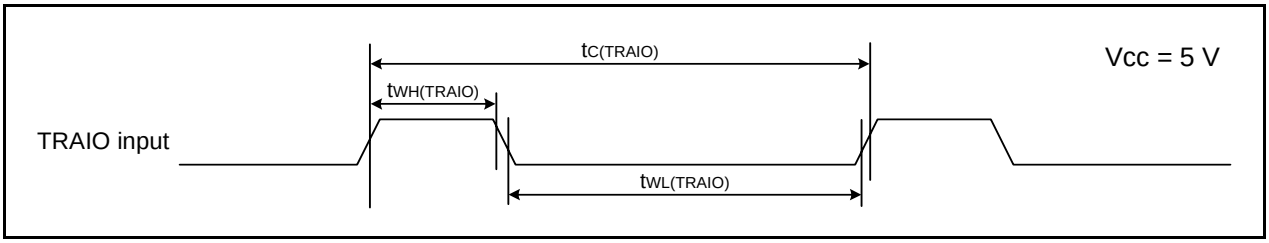


Figure 24.5 TRAIO Input Timing Diagram when Vcc = 5 V

Table 24.15 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLK0 input cycle time	200	—	ns
$t_{W(CKH)}$	CLK0 input “H” width	100	—	ns
$t_{W(CKL)}$	CLK0 input “L” width	100	—	ns
$t_{d(C-Q)}$	TXD0 output delay time	—	50	ns
$t_{h(C-Q)}$	TXD0 hold time	0	—	ns
$t_{su(D-C)}$	RXD0 input setup time	50	—	ns
$t_{h(C-D)}$	RXD0 input hold time	90	—	ns

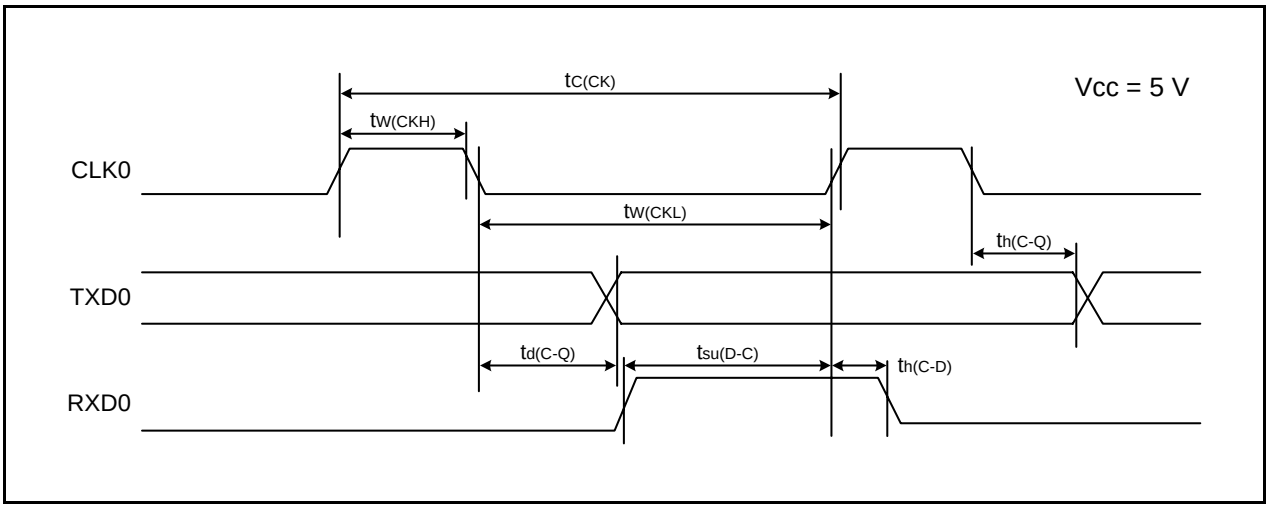


Figure 24.6 Serial Interface Timing Diagram when Vcc = 5 V

Table 24.16 External Interrupt $\overline{INTi}$ (i = 0 to 3) Input, Key Input Interrupt $\overline{KIi}$ (i = 0 to 3)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{INTi}$ input “H” width, $\overline{KIi}$ input “H” width	250 (1)	—	ns
$t_{W(INL)}$	$\overline{INTi}$ input “L” width, $\overline{KIi}$ input “L” width	250 (2)	—	ns

Notes:
1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

Figure 24.7 Input Timing for External Interrupt $\overline{INTi}$ and Key Input Interrupt $\overline{KIi}$ when Vcc = 5 V

Table 24.17 Electrical Characteristics (3) [2.7 V ≤ Vcc < 4.2 V]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	Output “H” voltage	Other than XOUT	Drive capacity High	I_{OH} = –5 mA	Vcc – 0.5	—	Vcc	V
			Drive capacity Low	I_{OH} = –1 mA	Vcc – 0.5	—	Vcc	V
		XOUT		I_{OH} = –200 μA	1.0	—	Vcc	V
V_{OL}	Output “L” voltage	Other than XOUT	Drive capacity High	I_{OL} = 5 mA	—	—	0.5	V
			Drive capacity Low	I_{OL} = 1 mA	—	—	0.5	V
		XOUT		I_{OL} = 200 μA	—	—	0.5	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$, $\overline{INT3}$, KI0, KI1, KI2, KI3, TRAIO, TRBO, TRCIOA, TRCIOB, TRCIOC, TRCIOD, TRCTRG, TRCCLK, RXD0, CLK0			0.1	0.4	—	V
		$\overline{RESET}$			0.1	0.5	—	V
I_{IH}	Input “H” current		V_I = 3 V, Vcc = 3.0 V		—	—	4.0	μA
I_{IL}	Input “L” current		V_I = 0 V, Vcc = 3.0 V		—	—	–4.0	μA
R_{PULLUP}	Pull-up resistance		V_I = 0 V, Vcc = 3.0 V		42	84	168	kΩ
R_{fXIN}	Feedback resistance	XIN			—	0.3	—	MΩ
V_{RAM}	RAM hold voltage		During stop mode		1.8	—	—	V

Note:
1. 2.7 V ≤ Vcc < 4.2 V at Topr = –20°C to 85°C, f(XIN) = 10 MHz, unless otherwise specified.

Table 24.18 Electrical Characteristics (4) [2.7 V ≤ Vcc < 3.3 V] (Topr = –20°C to 85°C, unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
Icc	Power supply current (Vcc = 2.7 V to 3.3 V) Single-chip mode, output pins are open, other pins are Vss	High-speed clock mode	XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	—	3.5	10	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	—	1.5	7.5	mA
		High-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator on fOCO-F = 20 MHz Low-speed on-chip oscillator on = 125 kHz No division	—	7	15	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 20 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	—	3	—	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 10 MHz Low-speed on-chip oscillator on = 125 kHz No division	—	4	—	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 10 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	—	1.5	—	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 4 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-16 MSTTRD = MSTTRC = 1	—	1	—	mA
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR27 = 1, VCA20 = 0	—	90	390	µA
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	—	15	90	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	—	4	80	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	—	3.5	—	µA
		Stop mode	XIN clock off, Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	—	2	5.0	µA
			XIN clock off, Topr = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	—	5	—	µA

Timing requirements
(Unless Otherwise Specified: Vcc = 3 V, Vss = 0 V at Topr = 25°C)

Table 24.19 External Clock Input (XOUT)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XOUT)}$	XOUT input cycle time	50	—	ns
$t_{WH(XOUT)}$	XOUT input “H” width	24	—	ns
$t_{WL(XOUT)}$	XOUT input “L” width	24	—	ns

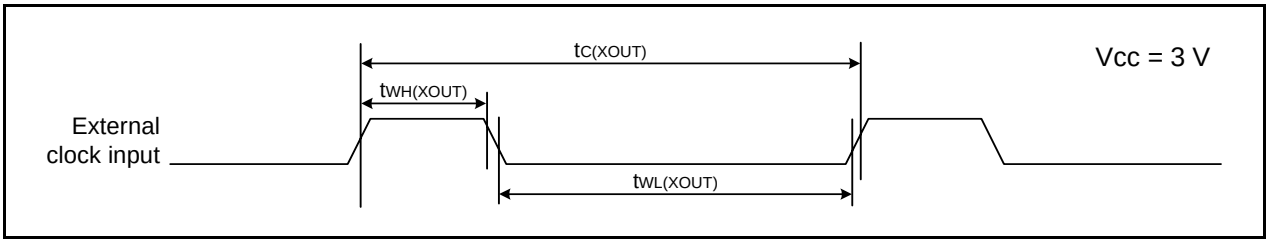


Figure 24.8 External Clock Input Timing Diagram when Vcc = 3 V

Table 24.20 TRAIO Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	300	—	ns
$t_{WH(TRAIO)}$	TRAIO input “H” width	120	—	ns
$t_{WL(TRAIO)}$	TRAIO input “L” width	120	—	ns

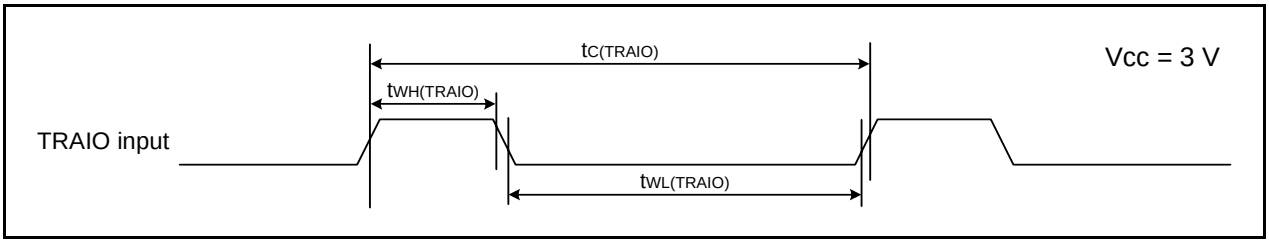


Figure 24.9 TRAIO Input Timing Diagram when Vcc = 3 V

Table 24.21 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLK0 input cycle time	300	—	ns
$t_{W(CKH)}$	CLK0 input “H” width	150	—	ns
$t_{W(CKL)}$	CLK0 Input “L” width	150	—	ns
$t_{d(C-Q)}$	TXD0 output delay time	—	80	ns
$t_{h(C-Q)}$	TXD0 hold time	0	—	ns
$t_{su(D-C)}$	RXD0 input setup time	70	—	ns
$t_{h(C-D)}$	RXD0 input hold time	90	—	ns

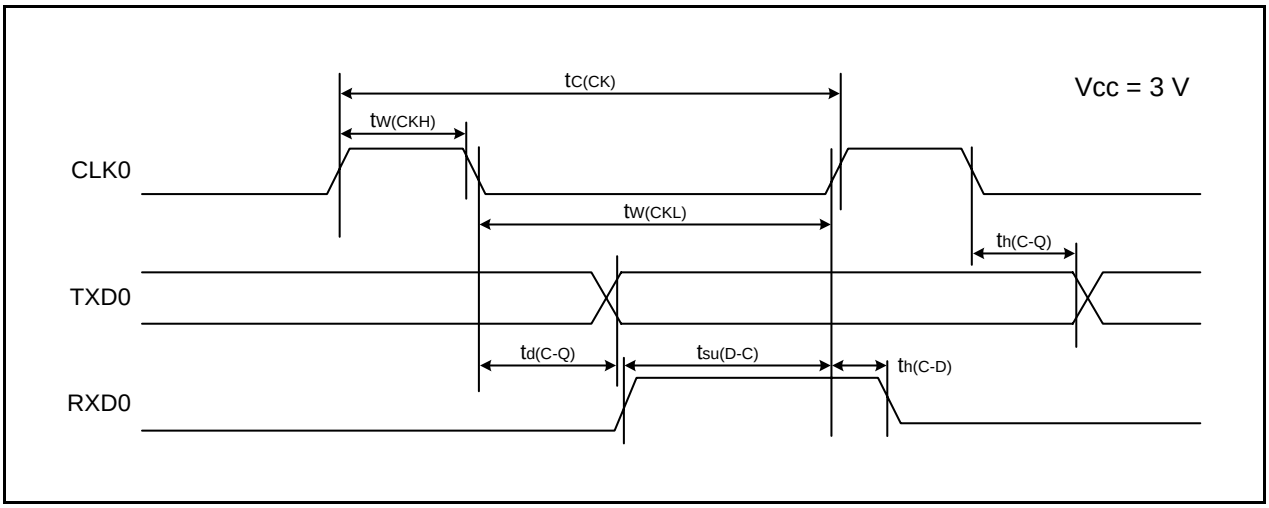


Figure 24.10 Serial Interface Timing Diagram when Vcc = 3 V

Table 24.22 External Interrupt $\overline{INTi}$ (i = 0 to 3) Input, Key Input Interrupt $\overline{KIi}$ (i = 0 to 3)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{INTi}$ input “H” width, $\overline{KIi}$ input “H” width	380 (1)	—	ns
$t_{W(INL)}$	$\overline{INTi}$ input “L” width, $\overline{KIi}$ input “L” width	380 (2)	—	ns

Notes:
1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

Figure 24.11 Input Timing for External Interrupt $\overline{INTi}$ and Key Input Interrupt $\overline{KIi}$ when Vcc = 3 V

Table 24.23 Electrical Characteristics (5) [1.8 V ≤ Vcc < 2.7 V]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	Output “H” voltage	Other than XOUT	Drive capacity High	I_{OH} = –2 mA	Vcc – 0.5	—	Vcc	V
			Drive capacity Low	I_{OH} = –1 mA	Vcc – 0.5	—	Vcc	V
		XOUT		I_{OH} = –200 μA	1.0	—	Vcc	V
V_{OL}	Output “L” voltage	Other than XOUT	Drive capacity High	I_{OL} = 2 mA	—	—	0.5	V
			Drive capacity Low	I_{OL} = 1 mA	—	—	0.5	V
		XOUT		I_{OL} = 200 μA	—	—	0.5	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$, $\overline{INT3}$, KI0, KI1, KI2, KI3, TRAIO, TRBO, TRCIOA, TRCIOB, TRCIOC, TRCIOD, RXD0, CLK0			0.05	0.20	—	V
		$\overline{RESET}$			0.05	0.20	—	V
I_{IH}	Input “H” current		V_I = 2.2 V, Vcc = 2.2 V		—	—	4.0	μA
I_{IL}	Input “L” current		V_I = 0 V, Vcc = 2.2 V		—	—	–4.0	μA
R_{PULLUP}	Pull-up resistance		V_I = 0 V, Vcc = 2.2 V		70	140	300	kΩ
R_{fXIN}	Feedback resistance	XIN			—	0.3	—	MΩ
V_{RAM}	RAM hold voltage		During stop mode		1.8	—	—	V

Note:
1. 1.8 V ≤ Vcc < 2.7 V at Topr = –20°C to 85°C, f(XIN) = 5 MHz, unless otherwise specified.

Table 24.24 Electrical Characteristics (6) [1.8 V ≤ Vcc < 2.7 V] (Topr = –20°C to 85°C, unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
Icc	Power supply current (Vcc = 1.8 V to 2.7 V) Single-chip mode, output pins are open, other pins are Vss	High-speed clock mode	XIN = 5 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	—	2.2	—	mA
			XIN = 5 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	—	0.8	—	mA
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR27 = 1, VCA20 = 0	—	90	300	µA
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	—	15	90	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	—	4	80	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	—	3.5	—	µA
		Stop mode	XIN clock off, Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	—	2	5	µA
			XIN clock off, Topr = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	—	5	—	µA

Timing requirements
(Unless Otherwise Specified: Vcc = 2.2 V, Vss = 0 V at Topr = 25°C)

Table 24.25 External Clock Input (XOUT)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XOUT)}$	XOUT input cycle time	200	—	ns
$t_{WH(XOUT)}$	XOUT input “H” width	90	—	ns
$t_{WL(XOUT)}$	XOUT input “L” width	90	—	ns

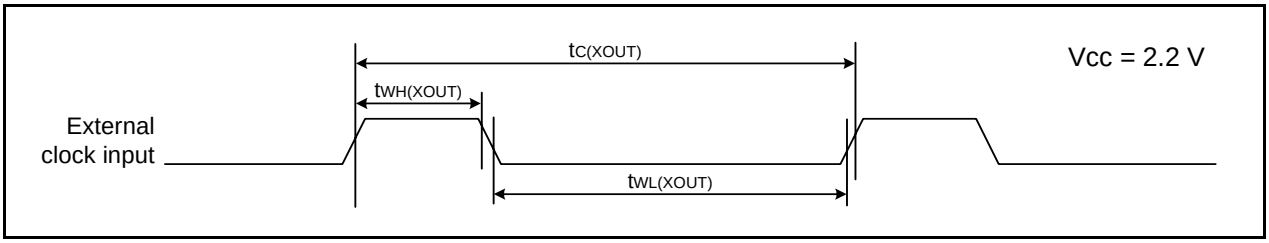


Figure 24.12 External Clock Input Timing Diagram when Vcc = 2.2 V

Table 24.26 TRAIO Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	500	—	ns
$t_{WH(TRAIO)}$	TRAIO input “H” width	200	—	ns
$t_{WL(TRAIO)}$	TRAIO input “L” width	200	—	ns

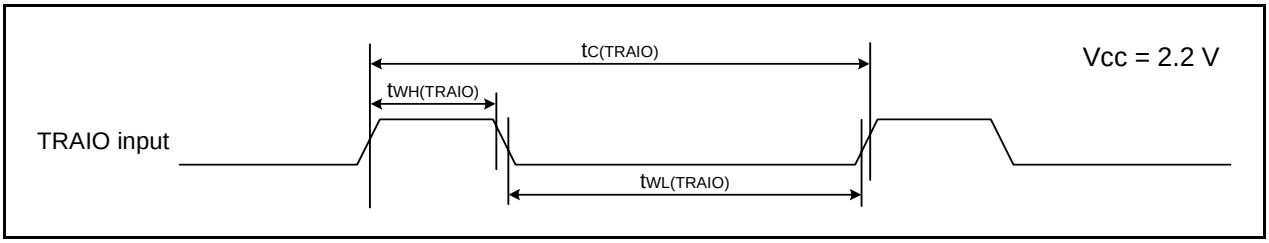


Figure 24.13 TRAIO Input Timing Diagram when Vcc = 2.2 V

Table 24.27 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLK0 input cycle time	800	—	ns
$t_{W(CKH)}$	CLK0 input “H” width	400	—	ns
$t_{W(CKL)}$	CLK0 input “L” width	400	—	ns
$t_{d(C-Q)}$	TXD0 output delay time	—	200	ns
$t_{h(C-Q)}$	TXD0 hold time	0	—	ns
$t_{su(D-C)}$	RXD0 input setup time	150	—	ns
$t_{h(C-D)}$	RXD0 input hold time	90	—	ns

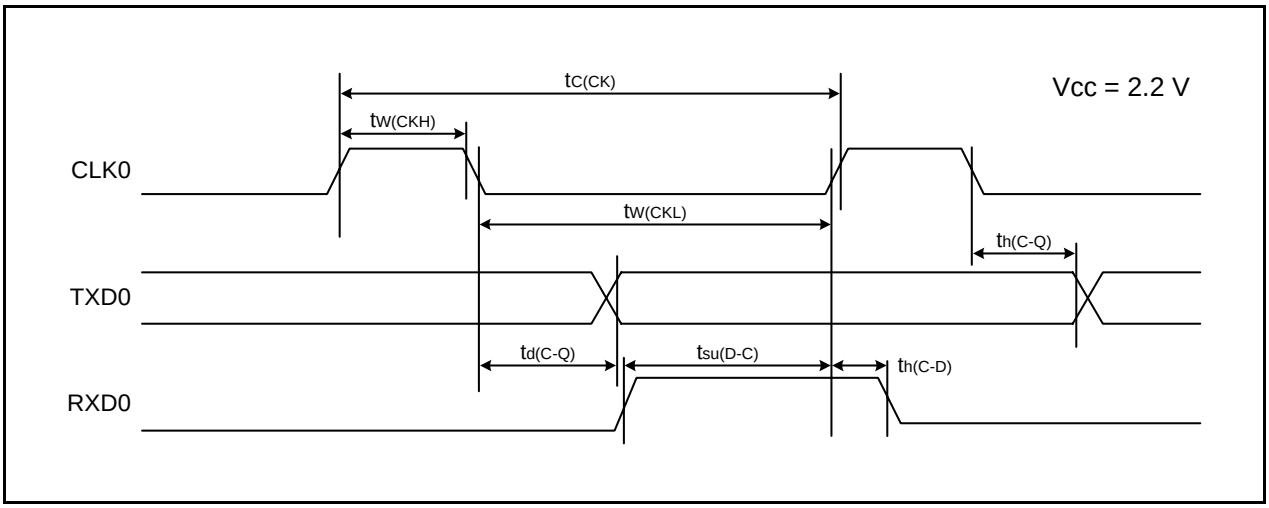


Figure 24.14 Serial Interface Timing Diagram when Vcc = 2.2 V

Table 24.28 External Interrupt $\overline{INTi}$ (i = 0 to 3) Input, Key Input Interrupt $\overline{KIi}$ (i = 0 to 3)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{INTi}$ input “H” width, $\overline{KIi}$ input “H” width	1000 (1)	—	ns
$t_{W(INL)}$	$\overline{INTi}$ input “L” width, $\overline{KIi}$ input “L” width	1000 (2)	—	ns

Notes:
1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

Figure 24.15 Input Timing for External Interrupt $\overline{INTi}$ and Key Input Interrupt $\overline{KIi}$ when Vcc = 2.2 V

25. Usage Notes

25.1 Notes on Clock Generation Circuit

25.1.1 Stop Mode

To enter stop mode, set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled) and then the CM10 bit in the CM1 register to 1 (stop mode). An instruction queue pre-reads 4 bytes from the instruction which sets the CM10 bit to 1 (stop mode) and the program stops.
Insert at least four NOP instructions following the JMP.B instruction after the instruction which sets the CM10 bit to 1.

- Program example to enter stop mode

```
        BCLR    1, FMR0         ; CPU rewrite mode disabled
        BCLR    7, FMR2         ; Low-current-consumption read mode disabled
        BSET    0, PRCR         ; Writing to CM1 register enabled
        FSET    I               ; Enable interrupt
        BSET    0, CM1          ; Stop mode
        JMP.B   LABEL_001
LABEL_001:
        NOP
        NOP
        NOP
        NOP
```

25.1.2 Wait Mode

When entering wait mode, set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled) and the FMR27 bit to 0 (low-current-consumption read mode disabled) before entering the mode. Do not enter wait mode while the FMR01 bit is 1 (CPU rewrite mode enabled) or the FMR27 bit is 1 (low-current-consumption read mode enabled).
To enter wait mode by setting the CM30 bit to 1, set the I flag to 0 (maskable interrupt disabled).
To enter wait mode using the WAIT instruction, set the I flag to 1 (maskable interrupt enabled). An instruction queue pre-reads 4 bytes from the instruction to set the CM30 bit to 1 (MCU enters wait mode) or the WAIT instruction, and then the program stops. Insert at least four NOP instructions after the instruction to set the CM30 bit to 1 (MCU enters wait mode) or the WAIT instruction.

- Program example to execute the WAIT instruction

```
        BCLR    1, FMR0         ; CPU rewrite mode disabled
        BCLR    7, FMR2         ; Low-current-consumption read mode disabled
        FSET    I               ; Enable interrupt
        WAIT                    ; Wait mode
        NOP
        NOP
        NOP
        NOP
```

- Program example to execute the instruction to set the CM30 bit to 1

```
        BCLR    1, FMR0         ; CPU rewrite mode disabled
        BCLR    7, FMR2         ; Low-current-consumption read mode disabled
        BSET    0, PRCR         ; Writing to CM3 register enabled
        FCLR    I               ; Interrupt disabled
        BSET    0, CM3          ; Wait mode
        NOP
        NOP
        NOP
        NOP
        BCLR    0, PRCR         ; Writing to CM3 register disabled
        FSET    I               ; Interrupt enabled
```

25.1.3 Reducing Internal Power Using VCA20 Bit

Set the VCA20 bit to 1 in low-speed clock mode or low-speed on-chip oscillator mode before entering wait mode. To enter wait mode by setting the CM30 bit in the CM3 register to 1 (MCU enters wait mode), follow the procedure shown in Figure 23.1 to set the procedure for reducing internal power consumption using the VCA20 bit.
To enter wait mode by executing WAIT instruction, follow the procedure shown in Figure 23.2 to set the procedure for reducing internal power consumption using the VCA20 bit.

25.1.4 Oscillation Stop Detection Function

Since the oscillation stop detection function cannot be used if the XIN clock frequency is below 2 MHz, set bits OCD1 to OCD0 to 00b. In addition, the OCD3 bit cannot be used to confirm whether the XIN clock oscillation is stable.

25.1.5 Oscillation Circuit Constants

Consult the oscillator manufacturer to determine the optimal oscillation circuit constants for the user system.

25.2 Notes on Interrupts

25.2.1 Reading Address 00000h

Do not read address 00000h by a program. When a maskable interrupt request is acknowledged, the CPU reads interrupt information (interrupt number and interrupt request level) from 00000h in the interrupt sequence. At this time, the IR bit for the acknowledged interrupt is set to 0.
If address 00000h is read by a program, the IR bit for the interrupt which has the highest priority among the enabled interrupts is set to 0. This may cause the interrupt to be canceled, or an unexpected interrupt to be generated.

25.2.2 SP Setting

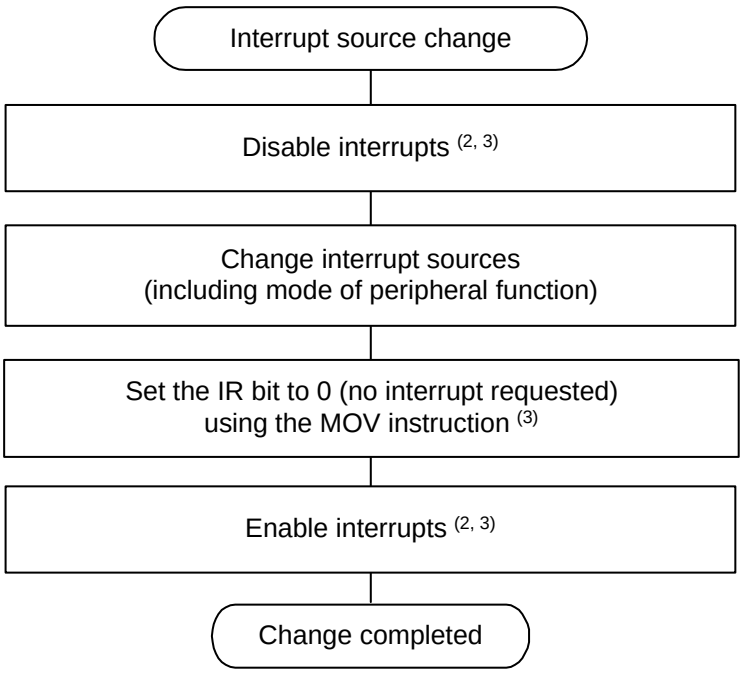
Set a value in the SP before an interrupt is acknowledged. The SP is set to 0000h after a reset. If an interrupt is acknowledged before setting a value in the SP, the program may run out of control.

25.2.3 External Interrupt and Key Input Interrupt

Either the “L” level width or “H” level width shown in the Electrical Characteristics is required for the signal input to pins $\overline{\text{INT0}}$ to $\overline{\text{INT3}}$ and pins $\overline{\text{KI0}}$ to $\overline{\text{KI3}}$, regardless of the CPU clock.
For details, refer to **Table 24.16** (VCC = 5 V), **Table 24.22** (VCC = 3 V), **Table 24.28** (VCC = 2.2 V) **External Interrupt $\overline{\text{INT}}$i (i = 0 to 3) Input, Key Input Interrupt $\overline{\text{KI}}$i (i = 0 to 3)**.

25.2.4 Changing Interrupt Sources

The IR bit in the interrupt control register may be set to 1 (interrupt requested) when the interrupt source changes. To use an interrupt, set the IR bit to 0 (no interrupt requested) after changing interrupt sources.
Changing interrupt sources as referred to here includes all factors that change the source, polarity, or timing of the interrupt assigned to a software interrupt number. Therefore, if a mode change of a peripheral function involves the source, polarity, or timing of an interrupt, set the IR bit to 0 (no interrupt requested) after making these changes. Refer to the descriptions of the individual peripheral functions for related interrupts.
Figure 25.1 shows a Procedure Example for Changing Interrupt Sources.



IR bit: The interrupt control register bit for the interrupt whose source is to be changed

Notes:
1. The above settings must be executed individually. Do not execute two or more settings simultaneously (using one instruction).
2. To prevent interrupt requests from being generated disable the peripheral function before changing the interrupt source. In this case, use the I flag if all maskable interrupts can be disabled.
   If all maskable interrupts cannot be disabled, use bits ILVL0 to ILVL2 for the interrupt whose source is to be changed.
3. To change the interrupt source to the input with the digital filter used, wait for three or more cycles of the sampling clock of the digital filter before setting the IR bit to 0 (no interrupt requested). Refer to **11.9.5 Rewriting Interrupt Control Register** for the instructions to use and related notes.

Figure 25.1 Procedure Example for Changing Interrupt Sources

25.2.5 Rewriting Interrupt Control Register

(a) The contents of the interrupt control register can be rewritten only while no interrupt requests corresponding to that register are generated. If an interrupt request may be generated, disable the interrupt before rewriting the contents of the interrupt control register.

(b) When rewriting the contents of the interrupt control register after disabling the interrupt, be careful to choose appropriate instructions.
Changing any bit other than the IR bit
If an interrupt request corresponding to the register is generated while executing the instruction, the IR bit may not be set to 1 (interrupt requested), and the interrupt may be ignored. If this causes a problem, use one of the following instructions to rewrite the contents of the register: AND, OR, BCLR, and BSET.

Changing the IR bit
Depending on the instruction used, the IR bit may not be set to 0 (no interrupt requested).
Use the MOV instruction to set the IR bit to 0.

(c) When using the I flag to disable an interrupt, set the I flag as shown in the sample programs below. Refer to (b) regarding rewriting the contents of interrupt control registers using the sample programs.

Examples 1 to 3 show how to prevent the I flag from being set to 1 (interrupts enabled) before the contents of the interrupt control register are rewritten for the effects of the internal bus and the instruction queue buffer.

Example 1: Use the NOP instructions to pause program until the interrupt control register is rewritten

```
INT_SWITCH1:
    FCLR    I               ; Disable interrupts
    AND.B   #00H, 0056H     ; Set the TRAIC register to 00h
    NOP
    NOP
    FSET    I               ; Enable interrupts
```

Example 2: Use a dummy read to delay the FSET instruction

```
INT_SWITCH2:
    FCLR    I               ; Disable interrupts
    AND.B   #00H, 0056H     ; Set the TRAIC register to 00h
    MOV.W   MEM,R0          ; Dummy read
    FSET    I               ; Enable interrupts
```

Example 3: Use the POPC instruction to change the I flag

```
INT_SWITCH3:
    PUSHC   FLG
    FCLR    I               ; Disable interrupts
    AND.B   #00H, 0056H     ; Set the TRAIC register to 00h
    POPC    FLG             ; Enable interrupts
```

25.3 Notes on ID Code Areas

25.3.1 Setting Example of ID Code Areas

The ID code areas are allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program. The following shows a setting example.

- To set 55h in all of the ID code areas

```
.org 00FFDCH
.lword dummy | (55000000h)   ; UND
.lword dummy | (55000000h)   ; INTO
.lword dummy; BREAK
.lword dummy | (55000000h)   ; ADDRESS MATCH
.lword dummy | (55000000h)   ; SET SINGLE STEP
.lword dummy | (55000000h)   ; WDT
.lword dummy | (55000000h)   ; ADDRESS BREAK
.lword dummy | (55000000h)   ; RESERVE
```

(Programming formats vary depending on the compiler. Check the compiler manual.)

25.4 Notes on Option Function Select Area

25.4.1 Setting Example of Option Function Select Area

The option function select area is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program. The following shows a setting example.

- To set FFh in the OFS register

```
.org 00FFFCH
.lword reset | (0FF000000h)     ; RESET
```

(Programming formats vary depending on the compiler. Check the compiler manual.)

- To set FFh in the OFS2 register

```
.org 00FFDBH
.byte 0FFh
```

(Programming formats vary depending on the compiler. Check the compiler manual.)

25.5 Notes on DTC

25.5.1 DTC activation source

- Do not generate any DTC activation sources before entering wait mode or during wait mode.
- Do not generate any DTC activation sources before entering stop mode or during stop mode.

25.5.2 DTCENi (i = 0 to 3, 5, 6) Registers

- Modify bits DTCENi0 to DTCENi7 only while an interrupt request corresponding to the bit is not generated.
- When the interrupt source flag in the status register for the peripheral function is 1, do not modify the corresponding activation source bit among bits DTCENi0 to DTCENi7.
- Do not access the DTCENi registers using DTC transfers.

25.5.3 Peripheral Modules

Do not set the status register bit for the peripheral function to 0 using a DTC transfer.

25.5.4 Interrupt Request

No interrupt is generated for the CPU during DTC operation in any of the following cases:
- When the DTC activation source is flash ready status
- When performing the data transfer causing the DTCCTj (j = 0 to 23) register value to change to 0 in normal mode
- When performing the data transfer causing the DTCCRj register value to change to 0 while the RPTINT bit in the DTCCRj register is 1 (interrupt generation enabled) in repeat mode

25.5.5 DTC Chain Transfers

When performing chain transfers using several control data, the number of transfers set to the first control data is enabled and the number of transfers proceeded after the first control data is disabled.
Examples:
- When DTCCT0 = 5 and DTCCT1 = 10, chain transfers are performed as DTCCT0 = DTCCT1 = 5.
- When DTCCT0 = 10 and DTCCT1 = 5, chain transfers are performed as DTCCT0 = DTCCT1 = 10.
- When DTCCT0 = 10, DTCCT1 = 5, and DTCCT2 = 2, chain transfers are performed as DTCCT0 = DTCCT1 = DTCCT2 = 10.

25.6 Notes on Timer RA

- Timer RA stops counting after a reset. Set the values in the timer RA and timer RA prescalers before the count starts.
- Even if the prescaler and timer RA are read out in 16-bit units, these registers are read 1 byte at a time by the MCU. Consequently, the timer value may be updated during the period when these two registers are being read.
- In pulse width measurement mode and pulse period measurement mode, bits TEDGF and TUNDF in the TRACR register can be set to 0 by writing 0 to these bits by a program. However, these bits remain unchanged if 1 is written. When using the READ-MODIFY-WRITE instruction for the TRACR register, the TEDGF or TUNDF bit may be set to 0 although these bits are set to 1 while the instruction is being executed. In this case, write 1 to the TEDGF or TUNDF bit which is not supposed to be set to 0 with the MOV instruction.
- When changing to pulse period measurement mode from another mode, the contents of bits TEDGF and TUNDF are undefined. Write 0 to bits TEDGF and TUNDF before the count starts.
- The TEDGF bit may be set to 1 by the first timer RA prescaler underflow generated after the count starts.
- When using the pulse period measurement mode, leave two or more periods of the timer RA prescaler immediately after the count starts, then set the TEDGF bit to 0.
- The TCSTF bit retains 0 (count stops) for 0 to 1 cycle of the count source after setting the TSTART bit to 1 (count starts) while the count is stopped.

  During this time, do not access registers associated with timer RA (1) other than the TCSTF bit. Timer RA starts counting at the first valid edge of the count source after the TCSTF bit is set to 1 (during count).

  The TCSTF bit remains 1 for 0 to 1 cycle of the count source after setting the TSTART bit to 0 (count stops) while the count is in progress. Timer RA counting is stopped when the TCSTF bit is set to 0.

  During this time, do not access registers associated with timer RA (1) other than the TCSTF bit.

  Note:
  1. Registers associated with timer RA: TRACR, TRAIOC, TRAMR, TRAPRE, and TRA.

- When the TRAPRE register is continuously written during count operation (TCSTF bit is set to 1), allow three or more cycles of the count source clock for each write interval.
- When the TRA register is continuously written during count operation (TCSTF bit is set to 1), allow three or more cycles of the prescaler underflow for each write interval.
- Do not set 00h to the TRA register in pulse width measurement mode and pulse period measurement mode.

25.7 Notes on Timer RB

- Timer RB stops counting after a reset. Set the values in the timer RB and timer RB prescalers before the count starts.
- Even if the prescaler and timer RB is read out in 16-bit units, these registers are read 1 byte at a time by the MCU. Consequently, the timer value may be updated during the period when these two registers are being read.
- In programmable one-shot generation mode and programmable wait one-shot generation mode, when setting the TSTART bit in the TRBCR register to 0 (stops counting) or setting the TOSSP bit in the TRBOCR register to 1 (stops one-shot), the timer reloads the value of reload register and stops. Therefore, in programmable one-shot generation mode and programmable wait one-shot generation mode, read the timer count value before the timer stops.
- The TCSTF bit remains 0 (count stops) for 1 to 2 cycles of the count source after setting the TSTART bit to 1 (count starts) while the count is stopped.
  During this time, do not access registers associated with timer RB (1) other than the TCSTF bit. Timer RB starts counting at the first valid edge of the count source after the TCSTF bit is set to 1 (during count).
  The TCSTF bit remains 1 for 1 to 2 cycles of the count source after setting the TSTART bit to 0 (count stops) while the count is in progress. Timer RB counting is stopped when the TCSTF bit is set to 0.
  During this time, do not access registers associated with timer RB (1) other than the TCSTF bit.

  Note:
  1. Registers associated with timer RB: TRBCR, TRBOCR, TRBIOC, TRBMR, TRBPRE, TRBSC, and TRBPR.

- If the TSTOP bit in the TRBCR register is set to 1 during timer operation, timer RB stops immediately.
- If 1 is written to the TOSST or TOSSP bit in the TRBOCR register, the value of the TOSSTF bit changes after one or two cycles of the count source have elapsed. If the TOSSP bit is written to 1 during the period between when the TOSST bit is written to 1 and when the TOSSTF bit is set to 1, the TOSSTF bit may be set to either 0 or 1 depending on the content state. Likewise, if the TOSST bit is written to 1 during the period between when the TOSSP bit is written to 1 and when the TOSSTF bit is set to 0, the TOSSTF bit may be set to either 0 or 1.
- To use the underflow signal of timer RA as the count source for timer RB, set timer RA in timer mode, pulse output mode, or event count mode.

25.7.1 Timer Mode

To write to registers TRBPRE and TRBPR during count operation (TCSTF bit in the TRBCR register is set to 1), note the following points:

- When the TRBPRE register is written continuously, allow three or more cycles of the count source for each write interval.
- When the TRBPR register is written continuously, allow three or more cycles of the prescaler underflow for each write interval.

25.7.2 Programmable Waveform Generation Mode

To write to registers TRBPRE and TRBPR during count operation (TCSTF bit in the TRBCR register is set to 1), note the following points:

- When the TRBPRE register is written continuously, allow three or more cycles of the count source for each write interval.
- When the TRBPR register is written continuously, allow three or more cycles of the prescaler underflow for each write interval.

25.7.3 Programmable One-shot Generation Mode

To write to registers TRBPRE and TRBPR during count operation (TCSTF bit in the TRBCR register is set to 1), note the following points:

- When the TRBPRE register is written continuously, allow three or more cycles of the count source for each write interval.
- When the TRBPR register is written continuously, allow three or more cycles of the prescaler underflow for each write interval.

25.7.4 Programmable Wait One-shot Generation Mode

To write to registers TRBPRE and TRBPR during count operation (TCSTF bit in the TRBCR register is set to 1), note the following points:

- When the TRBPRE register is written continuously, allow three or more cycles of the count source for each write interval.
- When the TRBPR register is written continuously, allow three or more cycles of the prescaler underflow for each write interval.

25.8 Notes on Timer RC

25.8.1 TRC Register

- The following note applies when the CCLR bit in the TRCCR1 register is set to 1 (clear TRC register at compare match with TRCGRA register).
  When using a program to write a value to the TRC register while the TSTART bit in the TRCMR register is set to 1 (count starts), ensure that the write does not overlap with the timing with which the TRC register is set to 0000h.
  If the timing of the write to the TRC register and the setting of the TRC register to 0000h coincide, the write value will not be written to the TRC register and the TRC register will be set to 0000h.

- Reading from the TRC register immediately after writing to it can result in the value previous to the write being read out. To prevent this, execute the JMP.B instruction between the read and the write instructions.

```
Program Example     MOV.W   #XXXXh, TRC    ; Write
                    JMP.B   L1             ; JMP.B instruction
                L1: MOV.W   TRC, DATA      ; Read
```

25.8.2 TRCSR Register

Reading from the TRCSR register immediately after writing to it can result in the value previous to the write being read out. To prevent this, execute the JMP.B instruction between the read and the write instructions.

```
Program Example     MOV.B   #XXh, TRCSR    ; Write
                    JMP.B   L1             ; JMP.B instruction
                L1: MOV.B   TRCSR, DATA    ; Read
```

25.8.3 TRCCR1 Register

To set bits TCK2 to TCK0 in the TRCCR1 register to 111b (fOCO-F), set fOCO-F to the clock frequency higher than the CPU clock frequency.

25.8.4 Count Source Switching

- Stop the count before switching the count source.

Switching procedure
(1) Set the TSTART bit in the TRCMR register to 0 (count stops).
(2) Change the settings of bits TCK2 to TCK0 in the TRCCR1 register.

- After switching the count source from fOCO40M to another clock, allow a minimum of two cycles of f1 to elapse after changing the clock setting before stopping fOCO40M.

Switching procedure
(1) Set the TSTART bit in the TRCMR register to 0 (count stops).
(2) Change the settings of bits TCK2 to TCK0 in the TRCCR1 register.
(3) Wait for a minimum of two cycles of f1.
(4) Set the FRA00 bit in the FRA0 register to 0 (high-speed on-chip oscillator off).

- After switching the count source from fOCO-F to fOCO40M, allow a minimum of two cycles of fOCO-F to elapse after changing the clock setting before stopping fOCO-F.

Switching procedure
(1) Set the TSTART bit in the TRCMR register to 0 (count stops).
(2) Change the settings of bits TCK2 to TCK0 in the TRCCR1 register.
(3) Wait for a minimum of two cycles of fOCO-F.
(4) Set the FRA00 bit in the FRA0 register to 0 (high-speed on-chip oscillator off).

- After switching the count source from fOCO-F to a clock other than fOCO40M, allow a minimum of one cycle of fOCO-F + fOCO40M to elapse after changing the clock setting before stopping fOCO-F.

Switching procedure
(1) Set the TSTART bit in the TRCMR register to 0 (count stops).
(2) Change the settings of bits TCK2 to TCK0 in the TRCCR1 register.
(3) Wait for a minimum of one cycle of fOCO-F + fOCO40M.
(4) Set the FRA00 bit in the FRA0 register to 0 (high-speed on-chip oscillator off).

25.8.5 Input Capture Function

- Set the pulse width of the input capture signal as follows:
  [When the digital filter is not used]
  Three or more cycles of the timer RC operation clock (refer to **Table 19.1 Timer RC Operation Clock**)
  [When the digital filter is used]
  Five cycles of the digital filter sampling clock + three cycles of the timer RC operating clock, minimum (refer to **Figure 19.5 Digital Filter Block Diagram**)
- The value of the TRC register is transferred to the TRCGRj register one or two cycles of the timer RC operation clock after the input capture signal is input to the TRCIOj (j = A, B, C, or D) pin (when the digital filter function is not used).
- When the input capture function is used, if an edge selected by bits IOj0 and IOj1 (j = A, B, C, or D) in the TRCIOR0 or TRCIOR1 register is input to the TRCIOj pin, the IMFj bit in the TRCSR register is set to 1 even when the TSTART bit in the TRCMR register is 0 (count stops).

25.8.6 TRCMR Register in PWM2 Mode

When the CSEL bit in the TRCCR2 register is set to 1 (count stops at compare match with the TRCGRA register), do not set the TRCMR register at compare match timing of registers TRC and TRCGRA.

25.8.7 Count Source fOCO40M

The count source fOCO40M can be used with supply voltage VCC = 2.7 V to 5.5 V. For supply voltage other than that, do not set bits TCK2 to TCK0 in the TRCCR1 register to 110b (select fOCO40M as the count source).

25.9 Notes on Serial Interface (UART0)

- When reading data from the U0RB register either in clock synchronous serial I/O mode or in clock asynchronous serial I/O mode, always read data in 16-bit units.
  When the high-order byte of the U0RB register is read, bits PER and FER in the U0RB register and the RI bit in the U0C1 register are set to 0.
  To check receive errors, read the U0RB register and then use the read data.

  Program example to read the receive buffer register:
  ```
  MOV.W    00A6H, R0    ; Read the U0RB register
  ```

- When writing data to the U0TB register in clock asynchronous serial I/O mode with 9-bit transfer data length, write data to the high-order byte first and then the low-order byte, in 8-bit units.

  Program example to write to the transmit buffer register:
  ```
  MOV.B    #XXH, 00A3H    ; Write to the high-order byte of the U0TB register
  MOV.B    #XXH, 00A2H    ; Write to the low-order byte of the U0TB register
  ```

25.10 Notes on Sensor Control Unit

25.10.1 Address to Store Detection Data

Set the start address in the SCUDAR register.
Also set the same start address in the DTDARj (j = 0 to 23) register of the DTC.
After measurement of each channel finishes, the values of data 1 and data 2 stored in the SFRs are transferred to RAM using the DTC or SDMA.
Use the DTC so that a total of 32 bits from registers SCUDBR and SCUPRC are transferred as measurement data by a single DTC transfer request in Status 22.
During DTC transfer from the sensor control unit, set the transfer mode to repeat mode (set the MODE bit in the DTCCRj register (j = 0 to 23) to 1) and disable interrupt generation (set the RPTINT bit in the DTCCRj register (j = 0 to 23) to 0).

25.10.2 Measurement Trigger

- If a measurement start trigger is generated during forced stop, all counter values change to 0.
- The measurement start trigger is recognized when bits SCCAP1 to SCCAP0 in the SCUMR register are set from 10b (measurement start trigger from timer RC) to 11b (external trigger ($\overline{\text{SCUTRG}}$) while the $\overline{\text{SCUTRG}}$ pin is held “L” during measurement operation.

25.10.3 Charging Time

To prevent measurement data from being overwritten to the next measurement data, the sensor control unit should be kept charged until DTC transfer or internal SDMA transfer is completed.

25.10.4 SCU Module Standby

The clock supply to the sensor control unit module can be stopped by setting the sensor control unit to module standby mode.
Since the clock supply to the registers in the sensor control unit is also stopped, cancel standby mode and allow at least two cycles to elapse before changing the settings of these registers.
Perform the same processing when stopping all clocks (when setting the CM1_0 bit in the CM register to 1).

25.10.5 SCU Initialization (SCINIT)

To initialize the sensor control unit by setting the SCINIT bit in the SCUCR0 register to 1, perform the following processing:
- Stop measurement (set the SCSTRT bit in the SCUCR0 register to 0)
- Do not output a SCU interrupt request (read the SIF bit in the SCUFR register as 0) or clear the SCU interrupt request (read the SIF bit as 1 and then write 0 to the same bit).

The DTC is not initialized by initialization using the SCINIT bit.
When initializing the touch sensor control unit, also make the required DTC settings.

25.10.6 Restrictions on Clock Settings

Do not change clock settings while measurement is performed using the touch sensor control unit.
Set the CM36 bit to 0 and the CM37 bit to 0 in the CM3 register and do not switch the clock used when exiting wait mode by an interrupt request signal.

25.10.7 Restrictions on Wait Mode

When the touch sensor control unit is used in wait mode, the following restrictions apply.

- Execute a WAIT instruction or set the CM30 bit in the CM3 register to 1 immediately after the SCSTRT bit is set to 1.
- Set the FMR11 bit in the FMR1 register to 1 and the FMSTP bit in the FMR0 register to 0 to not stop the flash memory even during wait mode.
- Do not use the sensor control unit in low-power-consumption wait mode. Set the SVC0 bit in the SVDC register to 0.

25.10.8 Restrictions on Stop Mode

The touch sensor control unit must be stopped (set the SCSTRT bit to 0) and set for initialization (set the SCINIT bit to 1) before setting stop mode (set the CM1_0 bit in the CM1 register to 1) to stop all clocks.

Any setting changes or initialization of the sensor control unit, including the setting change to stop mode, should be performed after measurement completes or before measurement starts, as much as possible.

25.11 Notes on Flash Memory

25.11.1 CPU Rewrite Mode

25.11.1.1 Prohibited Instructions

The following instructions cannot be used while the program ROM area is being rewritten in EW0 mode because they reference data in the flash memory: UND, INTO, and BRK.

25.11.1.2 Interrupts

Tables 25.1 to 25.2 list CPU Rewrite Mode Interrupts.

Table 25.1 CPU Rewrite Mode Interrupts (1)

Mode	Erase/ Write Target	Status	Maskable Interrupt
EW0	Program ROM	During auto-erasure (suspend enabled)	Usable by allocating a vector in RAM.
		During auto-erasure (suspend disabled)	
		During auto-programming	
EW1	Program ROM	During auto-erasure (suspend enabled)	Auto-erasure suspends after td(SR-SUS) and interrupt handling is executed. Auto-erasure can be restarted by setting the FMR21 bit to 0 after interrupt handling completes. While auto-erasure is being suspended, any block other than the block during auto-erasure execution can be read or written.
		During auto-erasure (suspend disabled or FMR22 = 0)	Auto-erasure and auto-programming have priority and interrupt requests are put on standby. Interrupt handling is executed after auto-erase and auto-program complete.
		During auto-programming	

FMR21, FMR22: Bits in FMR2 register

Table 25.2 CPU Rewrite Mode Interrupts (2)

Mode	Erase/ Write Target	Status	• Watchdog Timer • Oscillation Stop Detection • Voltage Monitor 2 • Voltage Monitor 1 (Note 1)	• Undefined Instruction • INTO Instruction • BRK Instruction • Single Step • Address Match • Address Break (Note 1)
EW0	Program ROM	During auto-erasure (suspend enabled)	When an interrupt request is acknowledged, auto-erasure or auto-programming is forcibly stopped immediately and the flash memory is reset. Interrupt handling starts when the flash memory restarts after the fixed period. Since the block during auto-erasure or the address during auto-programming is forcibly stopped, the normal value may not be read. After the flash memory restarts, execute auto-erasure again and ensure it completes normally. The watchdog timer does not stop during the command operation, so interrupt requests may be generated. Initialize the watchdog timer regularly using the erase-suspend function.	Not usable during auto-erasure or auto-programming.
		During auto-erasure (suspend disabled)		
		During auto-programming		
EW1	Program ROM	During auto-erasure (suspend enabled)	When an interrupt request is acknowledged, auto-erasure or auto-programming is forcibly stopped immediately and the flash memory is reset. Interrupt handling starts when the flash memory restarts after the fixed period. Since the block during auto-erasure or the address during auto-programming is forcibly stopped, the normal value may not be read. After the flash memory restarts, execute auto-erasure again and ensure it completes normally. The watchdog timer does not stop during the command operation, so interrupt requests may be generated. Initialize the watchdog timer regularly using the erase-suspend function.	Not usable during auto-erasure or auto-programming.
		During auto-erasure (suspend disabled or FMR22 = 0)		
		During auto-programming		

FMR21, FMR22: Bits in FMR2 register

Note:

1. Do not use a non-maskable interrupt while block 0 is being auto-erased because the fixed vector is allocated in block 0.

25.11.1.3 How to Access

To set one of the following bits to 1, first write 0 and then 1 immediately. Disable interrupts and DTC activation between writing 0 and writing 1.
- The FMR01 bit or FMR02 bit in the FMR0 register
- The FMR13 bit in the FMR1 register
- The FMR20 bit, FMR22 bit, or FMR 27 bit in the FMR2 register

To set one of the following bits to 0, first write 1 and then 0 immediately. Disable interrupts and DTC activation between writing 1 and writing 0.
- The FMR14 bit, FMR15 bit, FMR16 bit, or FMR17 bit in the FMR1 register

25.11.1.4 Rewriting User ROM Area

In EW0 mode, if the supply voltage drops while rewriting any block in which a rewrite control program is stored, it may not be possible to rewrite the flash memory because the rewrite control program cannot be rewritten correctly. In this case, use standard serial I/O mode.

25.11.1.5 Programming

Do not write additions to the already programmed address.

25.11.1.6 Entering Stop Mode or Wait Mode

Do not enter stop mode or wait mode during erase-suspend.
If the FST7 bit in the FST register is set to 0 (busy (during programming or erasure execution), do not enter to stop mode or wait mode.
Do not enter stop mode or wait mode while the FMR27 bit is 1 (low-current-consumption read mode enabled).

25.11.1.7 Programming and Erasure Voltage for Flash Memory

To perform programming and erasure, use VCC = 2.7 V to 5.5 V as the supply voltage. Do not perform programming and erasure at less than 2.7 V.

25.11.1.8 Block Blank Check

Do not execute the block blank check command during erase-suspend.

25.11.1.9 Low-Current-Consumption Read Mode

In low-speed on-chip oscillator mode, the current consumption when reading the flash memory can be reduced by setting the FMR27 bit in the FMR2 register to 1 (low-current-consumption read mode enabled).
When the CPU clock is set to the low-speed on-chip oscillator clock divided by 4, 8, or 16, low-consumption-current read mode can be used. When divided by 1 (no division) or divided by 2 is set, do not use low-consumption-current read mode. After setting the divide ratio of the CPU clock, set the FMR27 bit to 1.
To reduce the power consumption, refer to **23. Reducing Power Consumption**.
Enter wait mode or stop mode after setting the FMR27 bit to 0 (low-current-consumption read mode disabled).
Do not enter wait mode or stop mode while the FMR27 bit is 1 (low-current-consumption read mode enabled).

25.12 Notes on Noise

25.12.1 Inserting a Bypass Capacitor between VCC and VSS Pins as a Countermeasure against Noise and Latch-up

Connect a bypass capacitor (approximately 0.1 μF) using the shortest and thickest wire possible.

25.12.2 Countermeasures against Noise Error of Port Control Registers

During rigorous noise testing or the like, external noise (mainly power supply system noise) can exceed the capacity of the MCU's internal noise control circuitry. In such cases the contents of the port related registers may be changed.

As a firmware countermeasure, it is recommended that the port registers, port direction registers, and pull-up control registers be reset periodically. However, examine the control processing fully before introducing the reset routine as conflicts may be created between the reset routine and interrupt routines.

25.13 Note on Supply Voltage Fluctuation

After reset is deasserted, the supply voltage applied to the VCC pin must meet either or both the allowable ripple voltage Vr (vcc) or ripple voltage falling gradient dVr (vcc)/dt shown in Figure 25.2.

Symbol	Parameter	Standard			Unit
		Min.	Typ.	Max.	
Vr (vcc)	Allowable ripple voltage			0.1 VCC	V
dVr (vcc)/dt	Ripple voltage falling gradient			10	V/ms

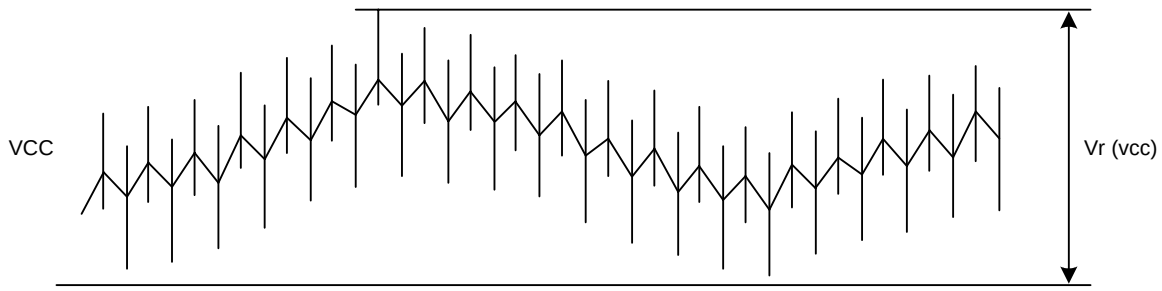


Figure 25.2 Definition of ripple voltage

26. Notes on On-Chip Debugger

When using the on-chip debugger to develop and debug programs for the R5R0C0B Group, take note of the following:

(1) Some of the user flash memory and RAM areas are used by the on-chip debugger. These areas cannot be accessed by the user.
Refer to the on-chip debugger manual for which areas are used.
(2) Do not set the address match interrupt (registers AIER0, AIER1, RMAD0, and RMAD1 and fixed vector tables) in a user system.
(3) Do not use the BRK instruction in a user system.
(4) Debugging is available under the condition of supply voltage VCC = 1.8 V to 5.5 V. Set the supply voltage to 2.7 V or above for rewriting the flash memory.

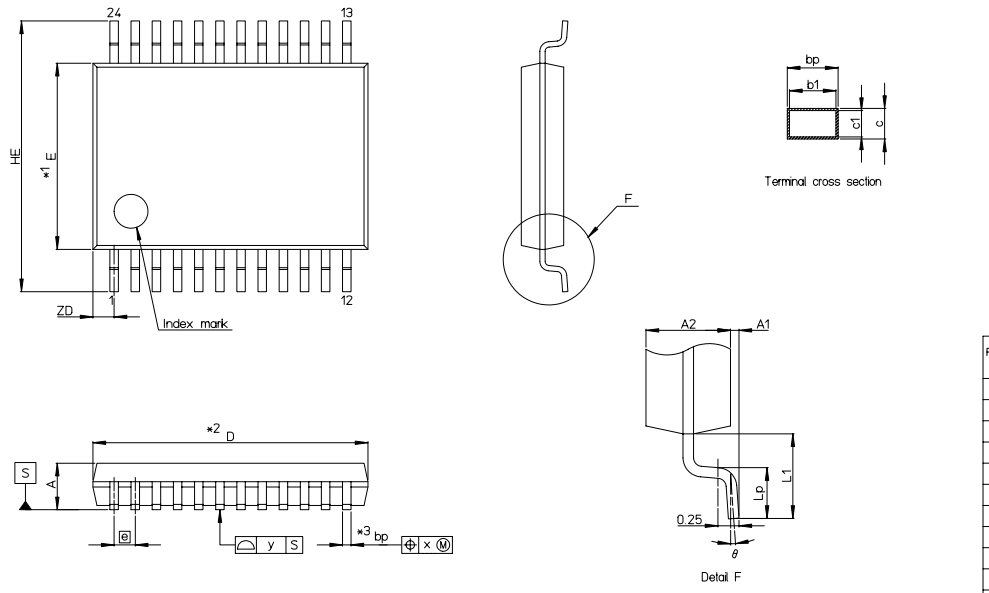
Connecting and using the on-chip debugger has some special restrictions. Refer to the on-chip debugger manual for details.

27. Notes on Emulator Debugger

Connecting and using the emulator debugger has some special restrictions. Refer to the emulator debugger manual for details.

Appendix 1. Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-TSSOP24-4.4x6.5-0.50	PTSP0024KB-A	24P2X-D	0.079g

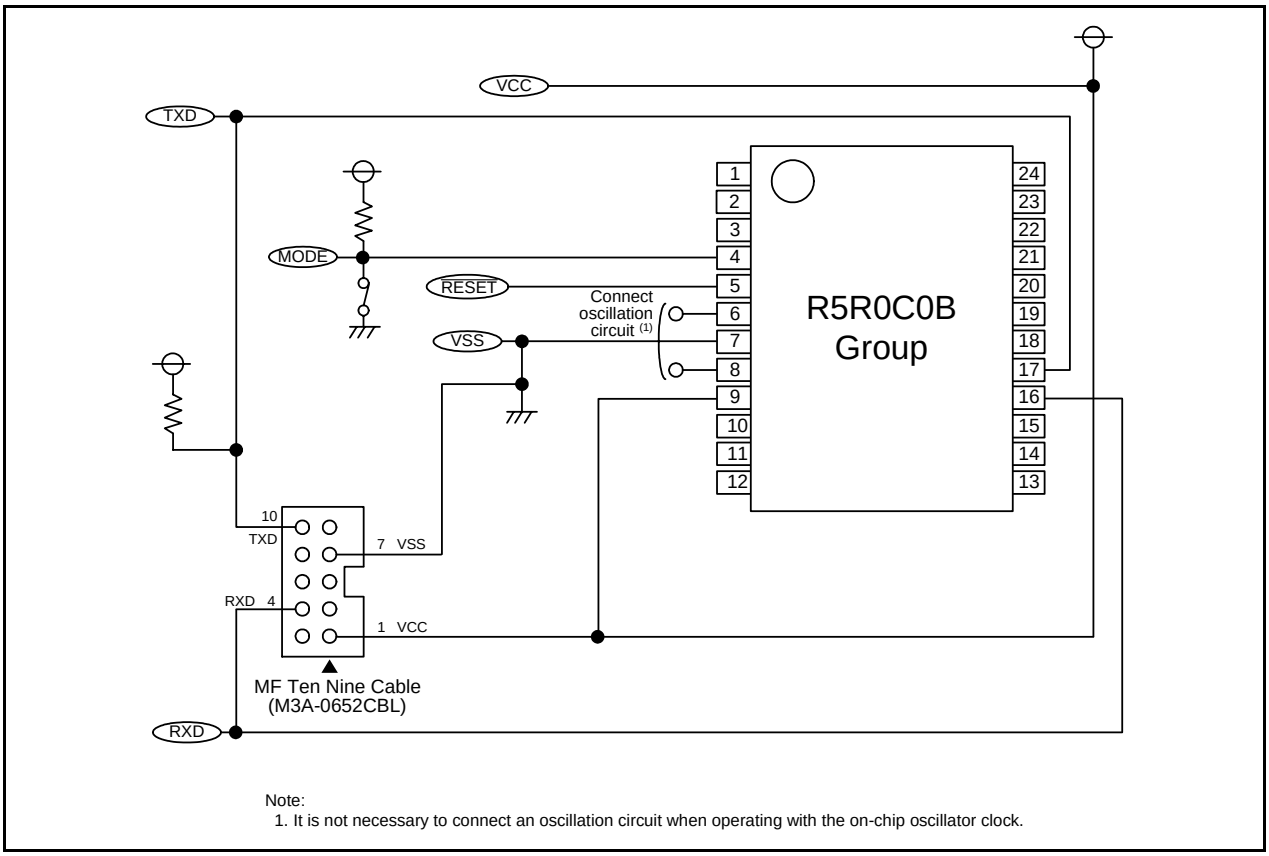


NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

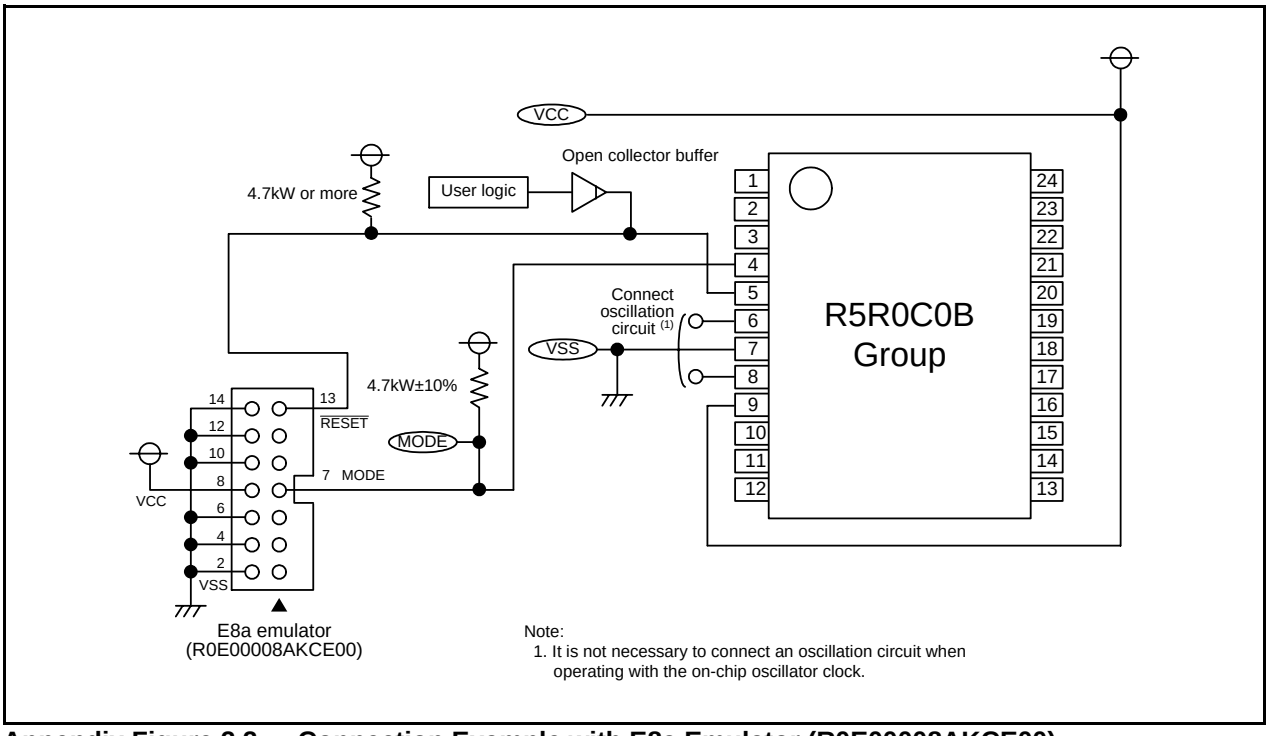
Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	6.4	6.5	6.6
E	4.3	4.4	4.5
A2	0.9	1.0	1.05
A1	0.05	—	0.15
A	—	—	1.2
bp	0.17	—	0.27
b1	0.17	0.20	0.23
c	0.1	—	0.20
c1	0.1	0.125	0.15
θ	0°	—	8°
HE	6.2	6.4	6.6
e	—	0.50	—
x	—	—	0.08
y	—	—	0.1
ZD	—	0.50	—
Lp	0.45	0.6	0.75
L1	—	1.0	—

Appendix 2. Connection Examples between Serial Programmer and On-Chip Debugging Emulator

Appendix Figure 2.1 shows a Connection Example with MF Ten Nine Cable (M3A-0652CBL) and Appendix Figure 2.2 shows a Connection Example with E8a Emulator (R0E00008AKCE00).



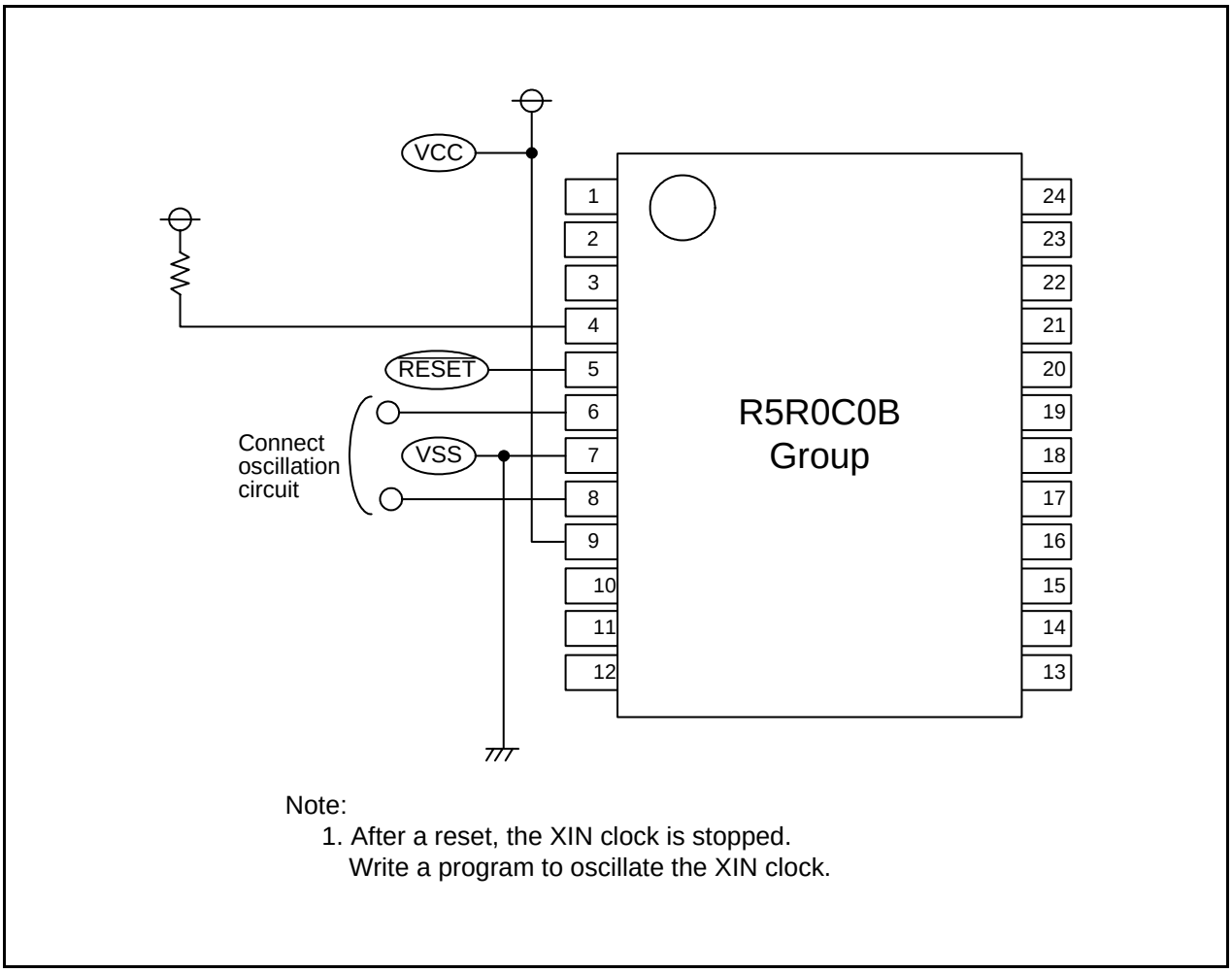
Appendix Figure 2.1 Connection Example with MF Ten Nine Cable (M3A-0652CBL)



Appendix Figure 2.2 Connection Example with E8a Emulator (R0E00008AKCE00)

Appendix 3. Example of Oscillation Evaluation Circuit

Appendix Figure 3.1 shows an Example of Oscillation Evaluation Circuit.



Note:
1. After a reset, the XIN clock is stopped.
Write a program to oscillate the XIN clock.

Appendix Figure 3.1 Example of Oscillation Evaluation Circuit

Index

REVISION HISTORY	R5R0C0B Group User's Manual: Hardware

Rev.	Date	Description	
		Page	Summary
0.10	Dec 07, 2011	—	First Edition issued
1.00	Mar 23, 2012	All pages	"Preliminary", "Under development", "N version" deleted
		3	Table 1.2 "Current Consumption", "Package" revised
		4	Table 1.3 revised
		6	Figure 1.3 "TBD" → "PTS0024KB-A (024P2X-D)"
		43, 101	6.2.4 and 9.2.14 Note1 revised
		98, 103	9.2.6 Note 1 and 9.4.2 "Divide ratio of 8 or more when VCC = 1.8 V ... (divide-by-8 or more)" deleted
		102	"Figure 9.3 Procedure for Reducing ... Using VCA20 bit" deleted
		104	9.5.1 revised
		108	9.6.2.2 revised, 9.6.2.3 added
		110	9.6.2.6 Title added
		111	9.6.2.7 Title added
		119	9.8.2 revised
		120	9.8.3 added
		303	Table 21.2 "000h" → "0000h"
		322	21.2.24 "(i = 0 to 4)" → "(i = 0 to 2)"
		327	Figure 21.5 "SCRVR0 to SCRVR2" → "SCRVR0 to SCRVR7"
		378	23.2.7 revised, Figure 23.1 added
		379	Figure 23.2 Title revised
		388	Table 24.8 revised
		393	Table 24.17 revised
		398	Table 24.24 revised
		422	Appendix 1 revised
1.01	May 22, 2012	4	Table 1.3 "R5R0C0B4FP" → "R5R0C0B4SP", Figure 1.1 revised

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