User's Manual

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RAJ306102 Series

User's Manual: Hardware

General Purpose Motor Control IC

Renesas Electronics
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General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

How to Use This Manual

Readers This manual is intended for user engineers who wish to understand the functions of the RL78/G1F and design and develop application systems and programs for these devices. The target products are as follows.

- 64-pin: RAJ306102

Purpose This manual is intended to give users an understanding of the functions described in the **Organization** below.

Organization The RAJ306102 series manual is separated into three parts: this manual, RL78/G1F hardware Manual and the software edition. This manual explains the function unique to RAJ306102 series. For detailed usage of the RL78/G1F microcomputer, refer to the RL78 / G1F User's Manual Hardware(R01UH0516E) and "Technical Update" on RL78/G1F. (common to the RL78 family).

RAJ306102 Series User's Manual Hardware (This Manual)	**RL78/G1F User's Manual Hardware**	**RL78 Family User's Manual Software**
About RAJ306102 • Pin functions • Internal block functions • Pre-Driver function • How to use RL78/G1F	About RL78/G1F • Pin functions • Internal block functions • Interrupts • Other on-chip peripheral functions • Electrical specifications	• CPU functions • Instruction set • Explanation of each instruction

How to Read This Manual

It is assumed that the readers of this manual have general knowledge of electrical engineering, logic circuits, and microcontrollers.

• To gain a general understanding of functions:

→ Read this manual in the order of the **CONTENTS**. The mark "<R>" shows major revised points. The revised points can be easily searched by copying an "<R>" in the PDF file and specifying it in the "Find what:" field.

• How to interpret the register format:

• To know details of the RL78/G1F Microcontroller instructions:

→ Refer to the separate document **RL78 Family User's Manual Software(R01US0015E).**

Conventions

Data significance: Higher digits on the left and lower digits on the right

Active low representations: $\overline{\times\times\times}$ (overscore over pin and signal name)

Note: Footnote for item marked with Note in the text

Caution: Information requiring particular attention

Remark: Supplementary information

Numerical representations: Binary ·· ×××× or ××××b

Decimal ·· ××××

Hexadecimal.. ××××h or 0x××××

Related Documents

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Documents Related to Devices

Document Name	Document No.
RAJ306102 Series User's Manual Hardware	This manual
RL78/G1F User's Manual Hardware	R01UH0516E
RL78 Family User's Manual Software	R01US0015E
Datasheet RAJ306102 (General-Purpose Motor Control IC)	R18DS0039E

Documents Related to Flash Memory Programming (User's Manual)

Document Name		Document No.
PG-FP5 Flash Memory Programmer		-
	RL78, 78K, V850, RX100, RX200, RX600 (Except RX64x), R8C, SH	R20UT2923E
	Common	R20UT2922E
	Setup Manual	R20UT0930E

Caution: The related documents listed above are subject to change without notice. Be sure to use the latest version of each document when designing. Other Documents

Document Name	Document No.
Renesas Microcontrollers RL78 Family	R01CP0003E
Semiconductor Package Mount Manual	R50ZZ0003E
Semiconductor Reliability Handbook	R51ZZ0001E

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Caution: This product uses SuperFlash® technology licensed from Silicon Storage Technology, Inc.

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Chapter 1 Overview

The RAJ306102 is a general-purpose motor control IC for 3-phase brushless DC (BLDC) motor applications. RAJ306102 combines a smart gate driver and MCU (RL78/G1F) in a single package.

The smart gate driver includes three half-bridge gate drivers, a buck switching regulator and a charge pump for the gate drive voltage, two LDOs for the internal analog and logic circuitry and MCU, three accurate differential amplifiers, a BEMF sense amplifier, three general purpose comparators, and extensive protection functions.

The three half-bridge gate drivers are capable of driving up to three N-channel MOSFET bridges and support bridge voltages from 6V to 65V. Each gate driver supports up to 0.64A source and 1.28A sink peak drive current with adjustable drive strength control. Adaptive and adjustable dead-times are implemented to ensure robustness and flexibility. The active gate holding mechanism prevents miller effect induced cross-conduction and further enhances robustness.

Three accurate differential amplifiers with adjustable gain support ground-side shunt current sensing for each bridge. The device can also support both BLDC sensor/sensorless motor drive by the three general purpose comparators or a BEMF sense amplifier.

The protection functions include supply voltage OV/UV protection, buck regulator OV/UV/OC protection, charge pump UV protection, MOSFET V_{DS} OC protection, current sense OC protection, MOSFET V_{GS} fault, thermal warning, and thermal shutdown.

The smart gate driver can be configured to use SPI interface by the internal connection with MCU. All the parameters can be set through the SPI interface and allows better monitoring. Fault conditions are reported on the nFAULT signal and each status bit in the Fault Status registers.

MCU supports H/W of the safe standard of IEC60730 and IEC61508. The development tools of the RL78 family are available.

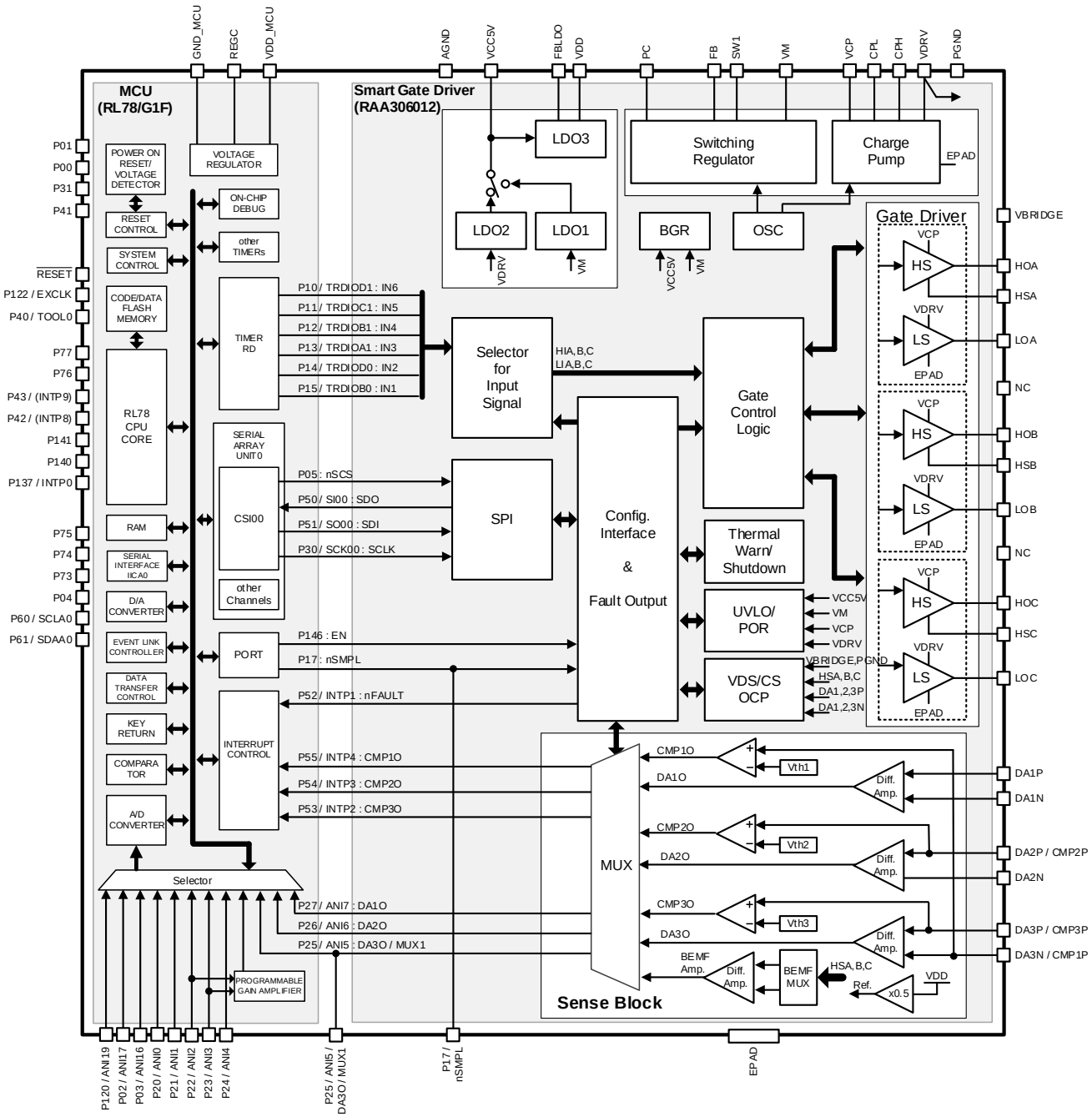


Figure 1-1 RAJ306102 Internal Block Diagram

1.1 Features

Recommended operating power supply voltage conditions

- VBRIDGE: 6 to 65V (Abs. Max 78V)
- VM: 6 to 60V (Abs. Max 65V)

Ambient operating temperature range

- -40 to +105°C

Low power VM supply:

- MCU: 5.2mA (HS Mode: f_{IH} = 32MHz)
- Smart Gate Driver: 2mA (Operating Mode), 28µA (Sleep Mode)

Package

- 8mmx8mm 64 Ld QFN package (0.4mm pitch)

1.1.1 MCU

The MCU used in this device is RL78/G1F (R5F11BLEGFB). The features are shown below. Note that the available peripheral functions are limited due to the presence of internally connected and unconnected pins. For details, please refer to ***1.5*** and ***2.2***.

Ultra-low Power Consumption Technology

- VDD_MCU pin voltage = 3.135 to 5.25V
  This product is limited to the recommended operating voltage condition of the VDD pin.
- Three low power consumption modes (HALT mode, STOP mode, SNOOZE mode)

RL78 CPU Core

- CISC architecture with 3-stage pipeline
- Minimum instruction execution time: Can be changed from high speed (0.03125µs: @ 32MHz operation with high-speed on-chip oscillator) to low speed (1µs: @ 1MHz operation)
- Multiply/divide/multiply & accumulate instructions are supported.
- Address space: 1MB
- General-purpose registers: (8-bit register x 8) x 4 banks
- On-chip RAM: 5.5KB

Code Flash Memory

- Code flash memory: 64KB
- Block size: 1KB
- Prohibition of block erase and rewriting (security function)
- Built-in on-chip debug function
- Self-programming: boot swap function and flash shield window function available

Data Flash Memory

- Data flash memory: 4KB
- Background operation (BGO): Instructions can be executed from the program memory while rewriting the data flash memory.
- Number of rewrites: 1,000,000 times (typ.)
- Voltage of rewrites: VDD_MCU = 3.135 to 5.25V

High-speed On-chip Oscillator

- Select from 64 / 48 / 32 / 24 / 16 / 12 / 8 / 6 / 4 / 3 / 2 / 1MHz
- High accuracy ±1.0% (VDD_MCU = 3.135 to 5.25V, T_A = -20 to +85°C)

Operating Ambient Temperature

- T_A = -40 to +105°C (RAJ306102GNP)

Power Management and Reset Functions

- On-chip power-on-reset (POR) circuit
- On-chip voltage detector (LVD) (configurable interrupt and reset levels)

Data Transfer Controller (DTC)

- Transfer modes: normal transfer mode, repeat transfer mode, block transfer mode
- Activation sources: Activated by interrupt sources.
- Chain transfer function

Event Link Controller (ELC)

- 21 types of event signals can be linked to specific peripheral functions.

Serial Interface

- CSI: 3ch
- UART: 1ch
- I^2C/Simplified I^2C: 2ch

Timer

- 16-bit timer: 9ch
- (Timer Array Unit (TAU): 4ch, Timer RJ: 1ch, Timer RG: 1ch, Timer RX: 1ch
- Timer RD: 2ch (with PWMOPA, Timer RD is for internal connection only.)
- 12-bit interval timer: 1ch
- Real-time clock: 1ch (available only for constant-period interrupt function)
- Watchdog timer: 1ch (Operable with dedicated low-speed on-chip oscillator clock)

A/D Converters

- 8/10-bit resolution A/D converter
- Analog input: 11ch
  - ANI0 - ANI5, ANI16, ANI17, ANI19: 9ch, Input from external connection pins
  - ANI5, ANI6, ANI7: Connected via differential amplifier from DAzP and DAzN pins (z = 1, 2, 3) of smart gate driver

Note: ANI5 can be used both as an external connection pin and via smart gate driver.
An internal pull-down resistor (330kΩ) is connected to ANI5 when used as an external connection pin.

- Internal reference voltage (1.45V) and temperature sensor
- Sample-and-hold (S/H) function: 3ch
  - ANI5 - ANI7: Function of differential amplifiers built into smart gate driver

D/A Converter

- 8-bit resolution D/A converter
- Analog output: 2ch
- Output voltage: 0V to VDD_MCU pin voltage
- Real-time output function

Comparator

- 2ch (Pin selector is provided for 1 channel.)
- Output function of a timer window in combination with the timer array unit
- The external reference voltage or internal reference voltage can be selected as the reference voltage.

Programmable Gain Amplifier (PGA)

- PGA 1ch (built into MCU): PGAI pin input, Selectable gain from x4, x8, x16, x32
- Differential amplifier 3ch (Smart gate driver built-in): Differential input from DAzP, DAzN pins (z = 1, 2, 3), Selectable gain from x5, x10, x20, x40

I/O Ports

- Port: 29pins (I/O: 27 pins, Input: 2 pins)
  N-ch open-drain I/O (6V withstand voltage): 2 pins
  N-ch open-drain I/O (VDD_MCU withstand voltage): 6 pins
- Can be set to N-ch open drain, TTL input buffer, and on-chip pull-up resistor
- On-chip key interrupt function
- On-chip clock output/buzzer output controller

IEC60730 and IEC61508 Compliant Functions

- Flash memory CRC operation function (high-speed CRC, general-purpose CRC)
- RAM parity error detection function
- RAM guard function
- SFR guard function
- Invalid memory access detection function
- Frequency detection function
- A/D test function
- Digital output signal level detection function for I/O pins

Others

- On-chip BCD (binary-coded decimal) correction circuit

Note: For details of each function, refer to ***“RL78/G1F User’s Manual: Hardware (R01UH0516EJ)”.***

1.1.2 Smart Gate Driver

3-phase gate drivers for BLDC Motors

- Peak 0.64A/1.28A source/sink current with 16 adjustable drive strength
- Adaptive and adjustable dead time
- 3-phase HI/LI mode and 3-phase PWM mode
- Input control signal configuration

Fully integrated power supply architecture

- Two 5V LDOs allow for Sleep Mode low I_Q
- 500mA buck switching regulator for the gate drive voltage (5V to 15V adjustable)
- 100mA LDO for peripheral circuit including MCU (voltage adjustable)

3 differential amplifiers with gain setting of x5, x10, x20, and x40 (for current sensing)

BEMF sense amplifier (for sensorless motor drive)

3 general purpose comparators (for Hall sensor motor drive)

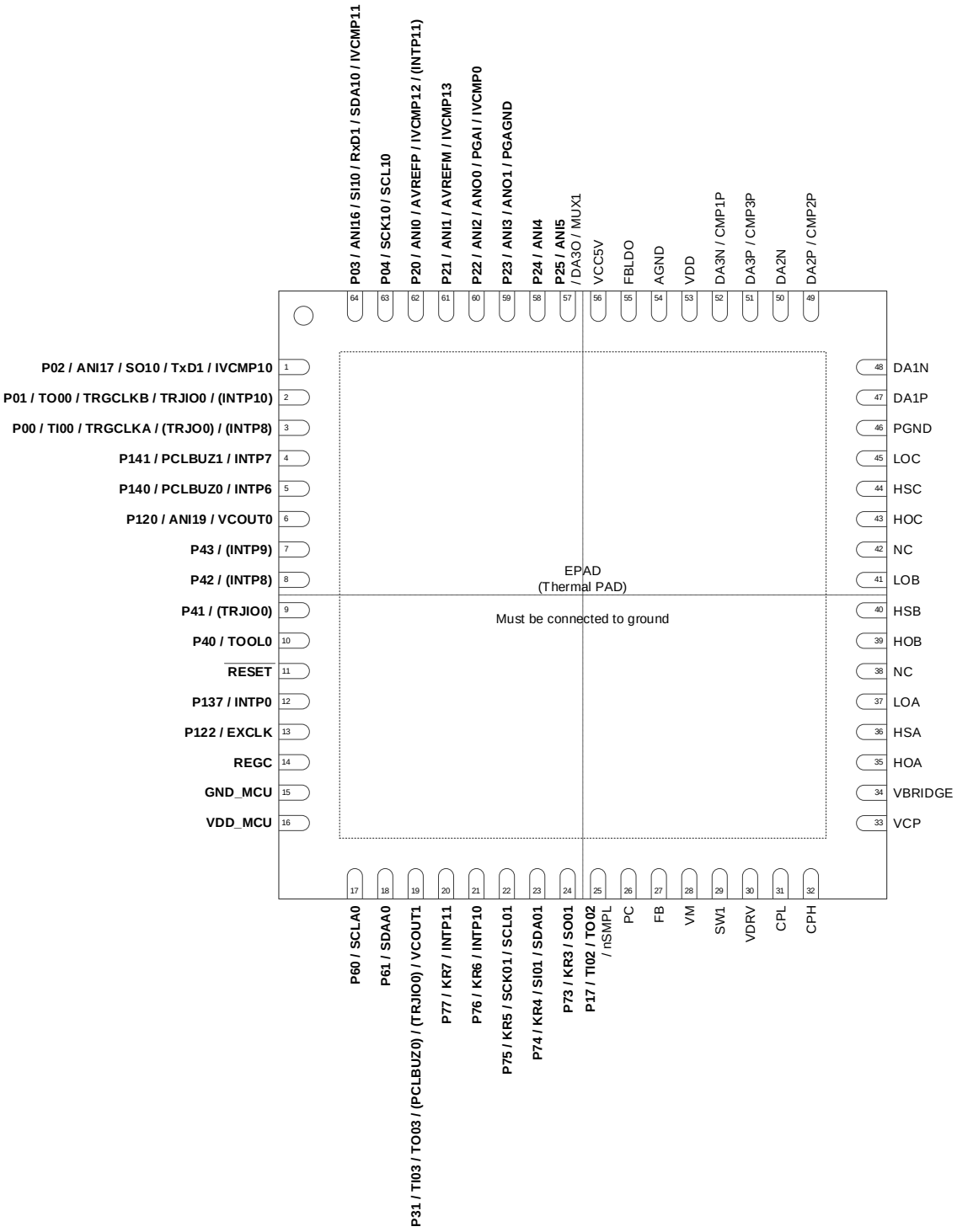
Extensive protection functions (fault detection functions)

- VCC5V undervoltage (VCC_UV)
- VM undervoltage (VM_UV)
- VM overvoltage (VM_OV)
- VCP undervoltage (VCP_UV) for charge pump
- MOSFET V_{DS} overcurrent (VDS_OCP)
- Current sense over current (CS_OCP)
- MOSFET V_{GS} fault (VGS_FAULT)
- Thermal warning (TWARN)
- Thermal shutdown (OTSD)
- Buck regulator overcurrent limiting (SR_OC1)
- Buck regulator overcurrent protection (SR_OCP)
- Buck regulator undervoltage (VDRV_UV)
- Buck regulator overvoltage (VDRV_OV)

1.2 Applications

Power tools, Garden tools, Vacuum Cleaners, Fans, Pumps, Robotics, etc.

1.3 Pin Configurations



bold fonts : RL78/G1F Pins
Normal fonts : Smart Gate Driver Pins

Figure 1-2 Pin Configuration Diagram (Top View)

1.4 Pin Descriptions

Table 1-1 Pin Descriptions (1/3)

PIN		Alternate	I/O				
Number	Name	Function	level	type	Initial	Function	Note
1	**P02**	**ANI17/SO10/ TxD1/IVCMP10**	VDD	IN/OUT	ANALOG	Digital input/output / ADC analog input / Serial data output of CSI10 / Serial data output of UART / Comparator 1 analog voltage input/reference voltage input	1
2	**P01**	**TO00/TRGCLKB/ TRJIO0/(INTP10)**	VDD	IN/OUT	IN	Digital input/output / Timer 00 output / Timer RG external clock input / Timer RJ input/output / (INTP10 interrupt request input)	1
3	**P00**	**TI00/TRGCLKA/ (TRJO0)/(INTP8)**	VDD	IN/OUT	IN	Digital input/output / Timer 00 input / Timer RG external clock input / (Timer RJ output) / (INTP8 interrupt request input)	1
4	**P141**	**PCLBUZ1/ INTP7**	VDD	IN/OUT	IN	Digital input/output / Programmable clock output/Buzzer output / INTP7 interrupt request input	1
5	**P140**	**PCLBUZ0/ INTP6**	VDD	IN/OUT	IN	Digital input/output / Programmable clock output/Buzzer output / INTP6 interrupt request input	1
6	**P120**	**ANI19/VCOUT0**	VDD	IN/OUT	ANALOG	Digital input/output / ADC analog input / Comparator 0 output	1
7	**P43**	**INTP9**	VDD	IN/OUT	IN	Digital input/output / INTP9 interrupt request input	1
8	**P42**	**INTP8**	VDD	IN/OUT	IN	Digital input/output / INTP8 interrupt request input	1
9	**P41**	**(TRJIO0)**	VDD	IN/OUT	IN	Digital input/output / (Timer RJ input/output)	1
10	**P40**	**TOOL0**	VDD	IN/OUT	IN	Digital input/output / Data I/O for flash memory programmer/debugger	1
11	**/RESET**	**-**	VDD	IN	-	The active-low system reset input for RL78/G1F	1
12	**P137**	**INTP0**	VDD	IN	IN	Digital input / INTP0 interrupt request input	1
13	**P122**	**EXCLK**	VDD	IN	IN	Digital input / External clock input for main system clock	1
14	**REGC**	**-**	VDD	-	-	Connect regulator output stabilization capacitor between REGC and GND_MCU for internal operation of RL78/G1F.	1
15	**GND_MCU**	**-**	VDD	GND	-	Ground for RL78/G1F	1
16	**VDD_MCU**	**-**	VDD	POWER	-	Positive power supply input for RL78/G1F Connect to bypass capacitors between VDD_MCU and GND_MCU.	1
17	**P60**	**SCLA0**	VDD	IN/OUT	IN	Digital input/output / Serial clock I/O of serial interface IICA0	1
18	**P61**	**SDAA0**	VDD	IN/OUT	IN	Digital input/output / Serial data I/O of serial interface IICA0	1
19	**P31**	**TI03/TO03/ (PCLBUZ0)/ (TRJIO0)/VCOUT1**	VDD	IN/OUT	IN	Digital input/output / Timer 03 input / Timer 03 output / (Programmable clock output/Buzzer output) / (Timer RJ output) / Comparator 1 output	1
20	**P77**	**KR7/INTP11**	VDD	IN/OUT	IN	Digital input/output / KR7 key interrupt input / INTP11 interrupt request input	1
21	**P76**	**KR6/INTP10**	VDD	IN/OUT	IN	Digital input/output / KR6 key interrupt input / INTP10 interrupt request input	1
22	**P75**	**KR5/SCK01/ SCL01**	VDD	IN/OUT	IN	Digital input/output / KR5 key interrupt input / Serial clock I/O of CSI01 / Serial clock output of IIC01	1
23	**P74**	**KR4/SI01/ SDA01**	VDD	IN/OUT	IN	Digital input/output / KR4 key interrupt input / Serial data input of CSI01 / Serial data I/O of IIC01	1
24	**P73**	**KR3/SO01**	VDD	IN/OUT	IN	Digital input/output / KR3 key interrupt input / Serial data output of CSI01	1
25	**P17**	**TI02/TO02/** nSMPL	VDD	IN/OUT	IN	Digital input/output / Timer 02 input / Timer 02 output / Sample and Hold control input for smart gate driver	1,2

Note1: These are RL78/G1F pins. For details of the pin functions, refer to ***"RL78/G1F User's Manual: Hardware (R01UH0516EJ)"***.

Note2: When using this pin as P17 (Digital input/output), TI02, or TO02 function, the S/H function of the differential amplifier of the smart gate driver is not available. Please set all of the BEMF_SH, DA1_SH, DA2_SH, and DA3_SH bits in SNSCTL2 register of the smart gate driver to "0". Refer to ***3.2.1.15*** for details.

Table 1-2 Pin Descriptions (2/3)

PIN		Alternate	I/O			Function	Note
Number	Name	Function	level	type	Initial		
26	PC	-	VCC5V	OUT	OUT	gm amplifier output for phase compensation of buck switching regulator.	
27	FB	-	VCC5V	IN	IN	Voltage feedback input of buck switching regulator (Ref.=0.8V).	
28	VM	-	VM	POWER	-	Power supply input. Connect bypass capacitors between VM and analog ground.	
29	SW1	-	VM	OUT	OUT	Switch node of buck switching regulator.	
30	VDRV	-	VDRV	POWER	-	Output of buck switching regulator, Low-side gate driver supply. Connect to bypass capacitors between VDRV and analog ground.	
31	CPL	-	VDRV	OUT	OUT	Charge pump low-side switch node. Connect a flying capacitor between CPH and CPL pins.	
32	CPH	-	VCP	OUT	OUT	Charge pump high-side switch node. Connect a flying capacitor between CPH and CPL pins.	
33	VCP	-	VCP	POWER	-	Charge pump output. Connect a bypass capacitor between VCP and VBRIDGE pins.	
34	VBRIDGE	-	VBRIDGE	IN	IN	Charge pump output reference and high-side MOSFET drain sense Input. Connect a bypass capacitor between VBRIDGE pin and power ground.	
35	HOA	-	VCP	OUT	OUT	Phase A high-side gate driver output. Connect to the high-side MOSFET gate.	
36	HSA	-	VBRIDGE	IN	IN	Phase A high-side source sense input. Connect to the high-side MOSFET source.	
37	LOA	-	VDRV	OUT	OUT	Phase A low-side gate driver output. Connect to the low-side MOSFET gate.	
38	NC	-	-	-	-	No connection (Keep open state)	
39	HOB	-	VCP	OUT	OUT	Phase B high-side gate driver output. Connect to the high-side MOSFET gate.	
40	HSB	-	VBRIDGE	IN	IN	Phase B high-side source sense input. Connect to the high-side MOSFET source.	
41	LOB	-	VDRV	OUT	OUT	Phase B low-side gate driver output. Connect to the low-side MOSFET gate.	
42	NC	-	-	-	-	No connection (Keep open state)	
43	HOC	-	VCP	OUT	OUT	Phase C high-side gate driver output. Connect to the high-side MOSFET gate.	
44	HSC	-	VBRIDGE	IN	IN	Phase C high-side source sense input. Connect to the high-side MOSFET source.	
45	LOC	-	VDRV	OUT	OUT	Phase C low-side gate driver output. Connect to the low-side MOSFET gate.	
46	PGND	-	GND	GND	-	Ground sense input of external power stage.	
47	DA1P	-	VDD	IN	IN	Positive input of differential amplifier 1.	
48	DA1N	-	VDD	IN	IN	Negative input of differential amplifier 1.	
49	DA2P	CMP2P	VDD	IN	IN	Positive input of differential amplifier 2 and positive input of comparator 2.	
50	DA2N	-	VDD	IN	IN	Negative input of differential amplifier 2.	
51	DA3P	CMP3P	VDD	IN	IN	Positive input of differential amplifier 3 and positive input of comparator 3.	
52	DA3N	CMP1P	VDD	IN	IN	Negative input of differential amplifier 3 and positive input of comparator 1.	
53	VDD	-	VDD	POWER	-	Internal series regulator output and power supply of output buffers. Connect to a bypass capacitor between VDD and AGND.	
54	AGND	-	GND	GND	-	Device analog ground.	
55	FBLDO	-	VCC5V	IN	IN	Voltage feedback input of internal series regulator (Ref.=1.2V).	
56	VCC5V	-	VCC5V	POWER	-	Internal series regulator output(5V). Connect to a bypass capacitor between VCC5V and AGND.	

Table 1-3 Pin Descriptions (3/3)

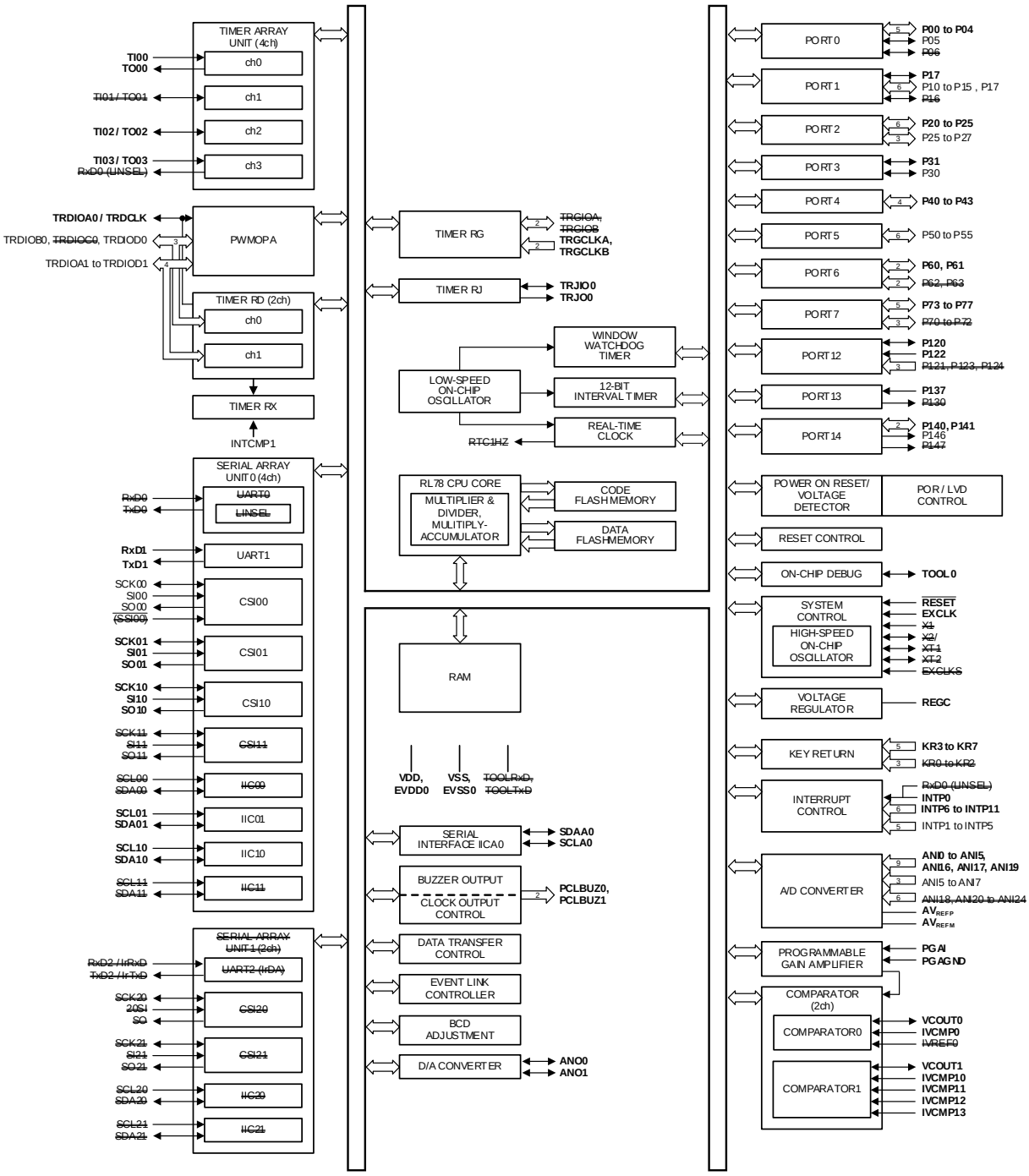
PIN		Alternate	I/O			Function	Note
Number	Name	Function	level	type	Initial		
57	**P25**	**ANI5**/DA3O/MUX1	VDD	IN/OUT	ANALOG	Digital input/output / ADC analog input / Output of differential amplifier 3, BEMF sense amplifier, and multiplexer.	1,3
58	**P24**	**ANI4**	VDD	IN/OUT	ANALOG	Digital input/output / ADC analog input	1
59	**P23**	**ANI3/ANO1/ PGAGND**	VDD	IN/OUT	ANALOG	Digital input/output / ADC analog input / DAC output / PGA reference voltage input	1
60	**P22**	**ANI2/ANO0/ PGAI/IVCMP0**	VDD	IN/OUT	ANALOG	Digital input/output / ADC analog input / DAC output / PGA voltage input / Comparator 0 analog voltage input	1
61	**P21**	**ANI1/AVREFM/ IVCMP13**	VDD	IN/OUT	ANALOG	Digital input/output / ADC analog input / ADC reference(- side) input	1
62	**P20**	**ANI0/AVREFP/ IVCMP12/(INTP11)**	VDD	IN/OUT	ANALOG	Digital input/output / ADC analog input / ADC reference (+ side) input / Comparator 1 analog voltage input/reference voltage input / (External interrupt request input)	1
63	**P04**	**SCK10/SCL10**	VDD	IN/OUT	ANALOG	Digital input/output / Serial clock I/O of CSI10 / Serial clock output of IIC10	1
64	**P03**	**ANI16/SI10/RxD1/ SDA10/IVCMP11**	VDD	IN/OUT	ANALOG	Digital input/output / ADC analog input / Serial data input of CSI10 / Serial data input of UART / Serial data I/O of IIC10 / Comparator 1 analog voltage input/reference voltage input	1
-	EPAD (Thermal PAD)	-	GND	GND	-	Power ground for gate driver and charge pump. Must be connected to power ground.	

Note1: These are RL78/G1F pins. For details of the pin functions, refer to ***"RL78/G1F User's Manual: Hardware (R01UH0516EJ)"***.
Note3: When using this pin as P25 or ANI5 pin, please set MUX bits in SNSCTL5 register of the smart gate driver to "000b". This pin has 330kΩ pulldown resistance. For details, refer to ***3.2.1.18***, and ***6.5.5*** of the ***"RAJ306102 Datasheet (R18DS0039EJ)"***.

1.5 Functions

1.5.1 MCU

1.5.1.1 Block Diagram



Bold fonts **: Output pins**
Normal fonts : Connected to Smart Gate Driver Pins
Double strike-through : Unavailable Pins or functions

Figure 1-3 Block Diagram of MCU

1.5.1.2 Function Overview

Table 1-4, ***Table 1-5*** and ***Table 1-6*** show the function overview comparison between the original RL78/G1F and the incorporated one into this device.

Table 1-4 MCU Section Function Overview Comparison (1/3) Note1

Item		RL78/G1F: R5F11BLExFB (64Pin, x = G: Industrial Applications)	RL78/G1F: R5F11BLEGFB (64Pin) for RAJ306102
Code Flash Memory		64KB	
Data Flash Memory		4KB	
RAM		5.5KB	
Address Space		1MB	
Main System Clock	High-speed System Clock	X1 (Crystal / Ceramic) Oscillation	-
		External main system clock input (EXCLK)	
		HS (High-speed Main) Mode: 1 to 20MHz (VDD = 2.7 to 5.5V) Note2	
		HS (High-speed Main) Mode: 1 to 16MHz (VDD = 2.4 to 5.5V) Note2	
		LS (Low-speed Main) Mode: 1 to 8MHz (VDD = 1.8 to 5.5V) Note2	
		LV (Low Voltage Main) Mode: 1 to 4MHz (VDD = 1.6 to 5.5V) Note2	
	High-speed On-chip Oscillator Clock (f_{IH})	HS (High-speed Main) Mode: 1 to 32MHz (VDD = 2.7 to 5.5V) Note2	
		HS (High-speed Main) Mode: 1 to 16MHz (VDD = 2.4 to 5.5V) Note2	
		LS (Low-speed Main) Mode: 1 to 8MHz (VDD = 1.8 to 5.5V) Note2	
		LV (Low Voltage Main) Mode: 1 to 4MHz (VDD = 1.6 to 5.5V) Note2	
Subsystem Clock		XT1 (crystal) oscillation / External subsystem clock input (EXCLKS) 32.768kHz	-
Low-speed On-chip Oscillator Clock		15kHz (typ.): VDD = 1.6 to 5.5V Note2	
General Purpose Register		8 bits × 32 registers (8 bits × 8 registers× 4 banks)	
Minimum instruction execution time		0.03125µs (High-speed on-chip oscillator clock fIH = 32MHz)	
		0.05µs (High-speed system clock fMX = 20MHz)	
		30.5µs (Subsystem clock fSUB = 32.768kHz)	-
Instruction set		Data transfer (8/16 bits)	
		Addition/ subtraction/logic operations (8/16 bits)	
		Multiplication (8 bits × 8 bits, 16 bits × 16 bits), division (16 bits ÷ 16 bits, 32 bits ÷ 32 bits)	
		Multiplication (16 bits × 16 bits + 32 bits)	
		Rotate, barrel shift, bit manipulation (set, reset, test, and Boolean operation), etc.	
I/O Port	Total	External connection ports: 58	External connection ports: 29, Internal connection ports: 19 Note3
	CMOS I/O	External connection ports: 48 (N-ch O.D. output [VDD withstand voltage]: 12)	External connection ports: 25 (N-ch O.D. output [VDD_MCU withstand voltage]: 5) Internal connection ports: 19 Note3
	CMOS Input	External connection ports: 5	External connection ports: 2 Internal connection ports: 0
	CMOS Output	External connection ports: 1	External connection ports: 0 Internal connection ports: 0
	N-ch O.D. I/O (6V tolerance)	External connection ports: 4	External connection ports: 2 Internal connection ports: 0

Note1: The grade of RL78/G1F incorporated into this device is “G: Industrial applications”. Note that the electrical characteristics of the RL78/G1F are different according to the ambient temperature range used (T_A = -40 to +85°C or T_A = -40 to +105°C).
Note2: The recommended operating voltage range of the RL78/G1F is limited to the recommended operating voltage range of smart gate driver (3.135 to 5.25V).
Note3: P17 and P25 can be used as external connection ports or internal connection ports, so they are counted redundantly for both. Set the suitable port configurations according to the actual application.

Table 1-5 MCU Section Function Overview Comparison (2/3) Note1

Item		RL78/G1F: R5F11BLExFB (64Pin, x = G: Industrial Applications)	RL78/G1F: R5F11BLEGFB (64Pin) for RAJ306102
Timer	16-bit timer	9ch · TAU: 4ch · Timer RJ: 1ch · Timer RD: 2ch (with PWMOPA) · Timer RX: 1ch · Timer RG: 1ch	9ch · TAU: 4ch · Timer RJ: 1ch · Timer RD: 2ch (with PWMOPA) Note4 · Timer RX: 1ch · Timer RG: 1ch
	Watchdog Timer	1ch	
	Real-time Clock (RTC)	1ch	1ch Note5
	12-bit Interval Timer	1ch	1ch Note5
	Timer Output	Timer Output (external): Total 16 · Timer RD: 6 · Timer Array Unit: 4 · Timer RJ: 1 · Timer RG: 2 · Real-time Clock: 1 · Clock output / Buzzer output: 2	Timer Output (internal): Total 6 · Timer RD: 6 Timer output (external): Total 7 · Timer Array Unit: 3 · Timer RJ: 1 · Real-time Clock: 1 · Clock output / Buzzer output: 2
		PWM Output (external): Total 9 · Timer RD: 6 · Timer Array Unit: 3	PWM Output (internal): Total 6 · Timer RD: 6 PWM Output (external): Total 3 · Timer Array Unit: 3
	RTC Output	1 · 1 Hz (subsystem clock: fSUB = 32.768 kHz)	-
Clock output / Buzzer output		2	2 Note4
		2.44kHz, 4.88kHz, 9.76kHz, 1.25MHz, 2.5MHz, 5MHz, 10MHz (Main System Clock: fMAIN = 20MHz operation)	
8/10-bit resolution A/D converter		17ch	11ch (External: 9ch, Internal: 3ch) Note6
8-bit D/A converter		2ch	
Comparator		2ch	2ch + 3ch Note7
Programmable Gain Amplifier (PGA)		1ch	1ch + 3ch Note7
Serial Interface		CSI: 2ch, UART supporting LIN-bus: 1ch, Simplified I^2C: 2ch	CSI00 for internal communication: 1ch, CSI or Simplified I^2C: 2ch
		CSI: 2ch, UART: 1ch, Simplified I^2C: 2ch	CSI00 for internal communication: 1ch, CSI or Simplified I^2C: 1ch, UART: 1ch,
		CSI: 2ch, UART supporting IrDA: 1ch, Simplified I^2C: 2ch	CSI00 for internal communication: 1ch, CSI: 1ch, Simplified I^2C: 1ch
	I^2C Bus (IICA)	1ch	
Data Transfer Controllers (DTC)		33 sources	30 sources
Event Link Controllers (ELC)	Event Input	22 sources	21 sources
	Event Trigger Output	10 sources	
Vector Interrupt Factor	Internal	25 sources	23 sources
	External	13 sources	12 sources
Key Interrupt		8	5

Note1: The grade of RL78/G1F incorporated into this device is “G: Industrial applications”. Note that the electrical characteristics of the RL78/G1F are different according to the ambient temperature range used (T_A = -40 to +85°C or T_A = -40 to +105°C).
Note4: Timer RD is internally connected to the smart gate driver and is dedicated to motor control.
Note5: Functions using the subsystem clock are not supported.
Note6: P25 can be used as an external connection port or internal connection port (Differential amplifier output of smart gate driver). Set the suitable port configurations according to the actual application. Note that the smart gate driver has a pull-down resistor (330kΩ) on the DA3O pin for internal connection, so be careful when using analog functions with external connections.
Note7: This device has not only MCU PGA but also 3 differential amplifiers of the smart gate driver.

Table 1-6 MCU Section Function Overview Comparison (3/3) Note1

Item	RL78/G1F: R5F11BLExFB (64Pin, x = G: Industrial Applications)	RL78/G1F: R5F11BLEGFB (64Pin) for RAJ306102
RESET	Reset by $\overline{\text{RESET}}$ pin	
	Internal reset by watchdog timer	
	Internal reset by power-on-reset	
	Internal reset by voltage detector	
	Internal reset by illegal instruction execution	
	Internal reset by RAM parity error	
	Internal reset by illegal memory access	
Power-on Reset Circuit	Power-on-reset: 1.51±0.04V (T_A = -40 to +85°C), 1.51±0.06V (T_A = -40 to +105°C)	
	Power-down-reset: 1.50±0.04V (T_A = -40 to +85°C), 1.50±0.06V (T_A = -40 to +105°C)	
MCU Detection Circuit	T_A = -40 to +85°C Note8 Rise: 1.67±0.03 to 4.00±0.08V (14 steps), Fall: 1.63±0.03 to 3.98±0.08V (14 steps)	
	T_A = -40 to +105°C Note8 Rise: 2.61±0.1 to 4.06±0.16V (8 steps), Fall: 2.55±0.1 to 3.98±0.15V (8 steps)	
On-chip Debug function	Yes	
MCU Supply Voltage	VDD = 1.6 to 5.5V (T_A = -40 to +85°C)	VDD_MCU = 1.6 to 5.5V Note8
	VDD = 2.4 to 5.5V (T_A = -40 to +105°C)	VDD_MCU = 2.4 to 5.5V (T_A = -40 to +105°C) Note8
Operating Ambient Temperature	T_A = -40 to +105°C (G: Industrial applications)	T_A = -40 to +105°C

Note1: The grade of RL78/G1F incorporated into this device is “G: Industrial applications”. Note that the electrical characteristics of the RL78/G1F are different according to the ambient temperature range used (T_A = -40 to +85°C or T_A = -40 to +105°C).
Note8: The recommended operating voltage range of the VDD pin in this device is 3.135 to 5.25V. Note that the threshold setting range of the MCU voltage detector is different according to the ambient temperature range used (TA = -40 to +85°C or TA = -40 to +105°C).

1.5.2 Smart Gate Driver

1.5.2.1 Block Diagram

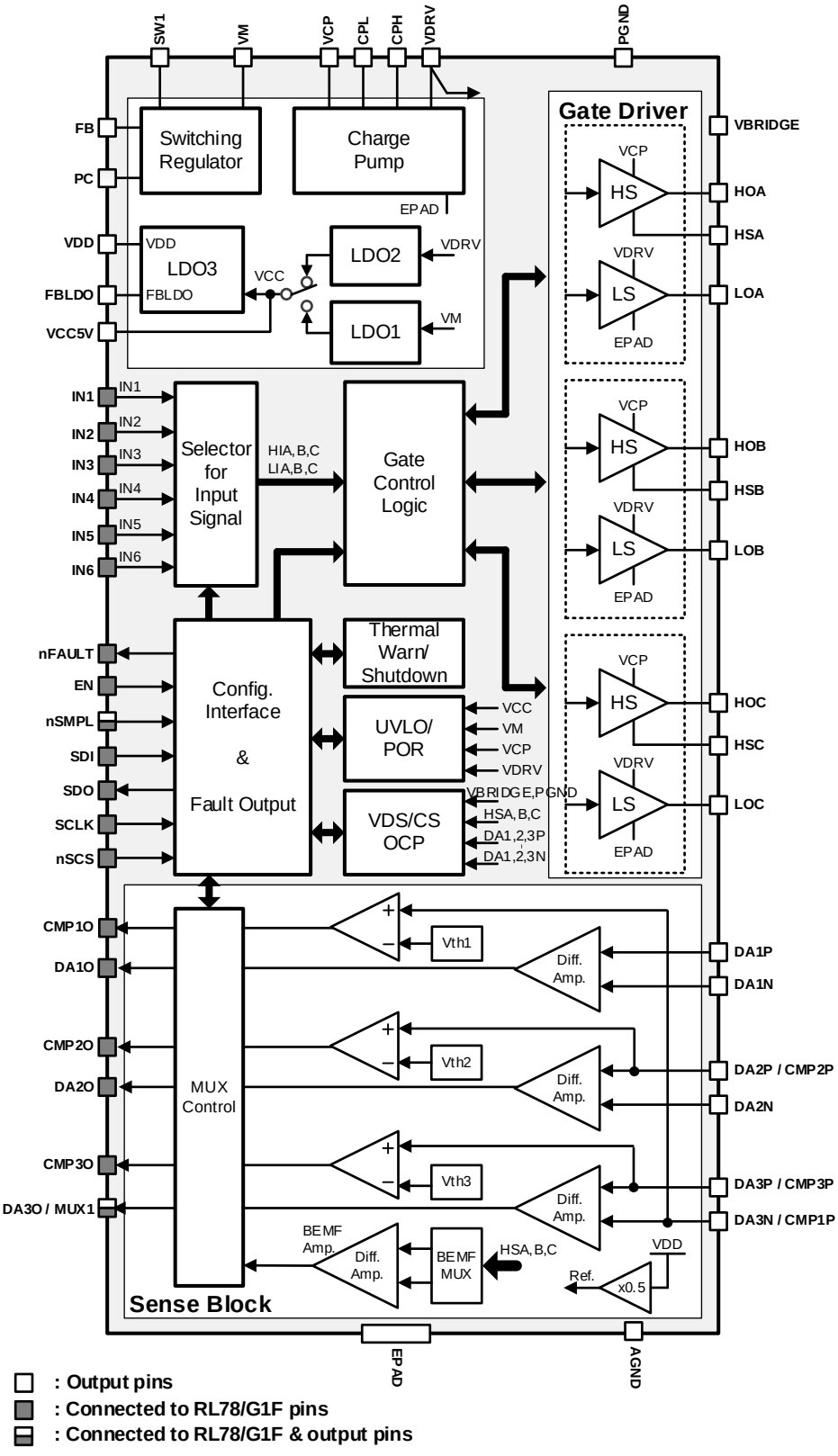


Figure 1-4 Smart Gate Driver Block Diagram Internal Connections between MCU and Smart Gate Driver

1.5.3 Internal Connection Diagram

This device combines MCU (RL78/G1F: R5F11BLEGFB) and smart gate driver (RAA306012) in a single package. ***Figure 1-5*** shows the internal connection diagram between MCU and smart gate driver. The ports marked with "x" are unconnected ports.

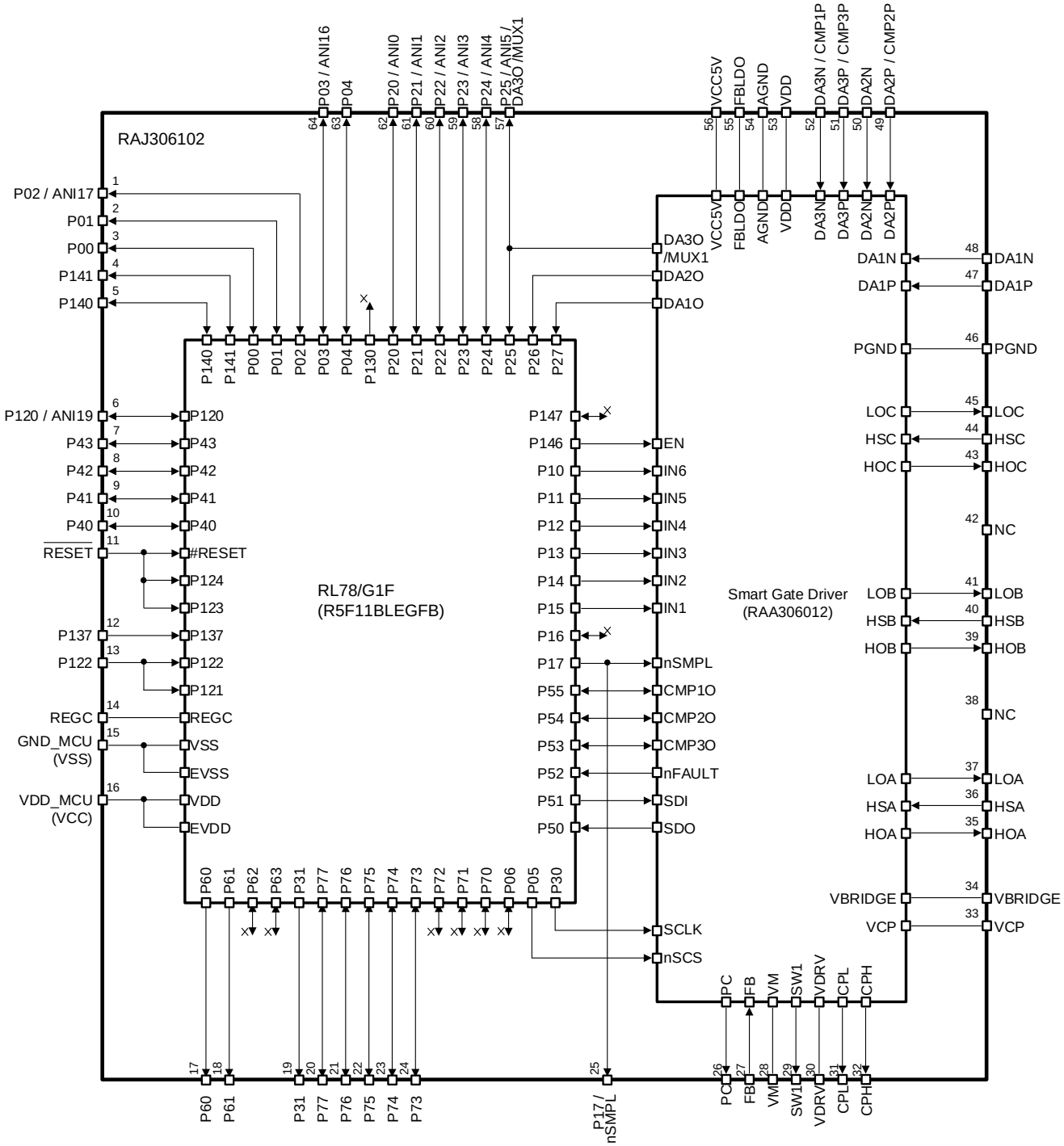


Figure 1-5 Internal Connection Diagram

1.5.4 Internal Connection Table

Table 1-7 shows the internal connections between the RL78/G1F and the smart gate driver.

Table 1-7 Internal Connections between RL78/G1F and Smart Gate Driver

No	I/O for RL78/G1F				Smart Gate Driver		Note
	Port Name	Level	I/O	Initial	Terminal	Function	
1	**P05**	VDD	I/O	Input port	nSCS	SPI chip select input.	
2	**P30 / SCK00**	VDD	I/O	Input port	SCLK	SPI clock input.	1
3	**P50 / SI00**	VDD	I/O	Input port	SDO	SPI data output. (SDO terminal is open-drain output. Set the on-chip pull-up of the MCU.)	1
4	**P51 / SO00**	VDD	I/O	Input port	SDI	SPI data input.	1
5	**P52 / /INTP1**	VDD	I/O	Input port	nFAULT	Fault indicator output. (nFAULT terminal is open-drain output. Set the on-chip pull-up of the MCU.)	1
6	**P53 / INPT2**	VDD	I/O	Input port	CMP3O	Control input for the detect phase selection of BEMF sense amplifier. / Output of comparator 3.	1
7	**P54 / INTP3**	VDD	I/O	Input port	CMP2O	Control input for the detect phase selection of BEMF sense amplifier. / Output of comparator 2.	1
8	**P55 / INTP4**	VDD	I/O	Input port	CMP1O	Control input for the detect phase selection of BEMF sense amplifier. / Output of comparator 1.	1
9	**P17**	VDD	I/O	Input port	nSMPL	Sampling control input of BEMF sense amplifier or differential amplifiers.	2
10	**P15 / TRDIOB0**	VDD	I/O	Input port	IN1	Gate driver control input 1. Control terminal of each phase gate driver is selectable by SPI.	
11	**P14 / TRDIOD0**	VDD	I/O	Analog input	IN2	Gate driver control input 2. Control terminal of each phase gate driver is selectable by SPI.	1
12	**P13 / TRDIOA1**	VDD	I/O	Analog input	IN3	Gate driver control input 3. Control terminal of each phase gate driver is selectable by SPI.	1
13	**P12 / TRDIOB1**	VDD	I/O	Analog input	IN4	Gate driver control input 4. Control terminal of each phase gate driver is selectable by SPI.	1
14	**P11 / TRDIOC1**	VDD	I/O	Analog input	IN5	Gate driver control input 5. Control terminal of each phase gate driver is selectable by SPI.	1
15	**P10 / TRDIOD1**	VDD	I/O	Analog Input	IN6	Gate driver control input 6. Control terminal of each phase gate driver is selectable by SPI.	1
16	**P146**	VDD	I/O	Input port	EN	Enable control terminal for Operating Mode. When this terminal is logic low, the device goes to a low-power sleep mode.	
17	**P27 / ANI7**	VDD	I/O	Analog input	DA1O	Output of differential amplifier 1.	
18	**P26 / ANI6**	VDD	I/O	Analog input	DA2O	Output of differential amplifier 2.	
19	**P25 / ANI5**	VDD	I/O	Analog input	DA3O/ MUX1	Output of differential amplifier 3, BEMF sense amplifier, and multiplexer.	3

Note1: The peripheral I/O redirection registers 0 to 3 (PIOR0 to PIOR3) must be set appropriately to control the gate driver. For details, refer to ***2.2.1.1***.

Note2: When using this port as P17 (Digital input/output), TI02, or TO02 function, the S/H function of the differential amplifier in the smart gate driver is not available. Set all of BEMF_SH, DA1_SH, DA2_SH, and DA3_SH bit in SNSCTL2 register of the smart gate driver to “0”. For details, refer to ***3.2.1.15***.

Note3: When using this port as P25 (Digital input/output) or ANI5 function, Set MUX bits in SNSCTL5 register of the smart gate driver to 000b”. DA3O/MUX1 terminal has 330kΩ pulldown resistance. For details, refer to ***3.2.1.18***, and ***6.5.5*** of the ***“RAJ306102 Datasheet (R18DS0039EJ)”***.

1.6 Typical Application Circuits

1.6.1 Hall Sensor Motor Drive (3 Comparators)

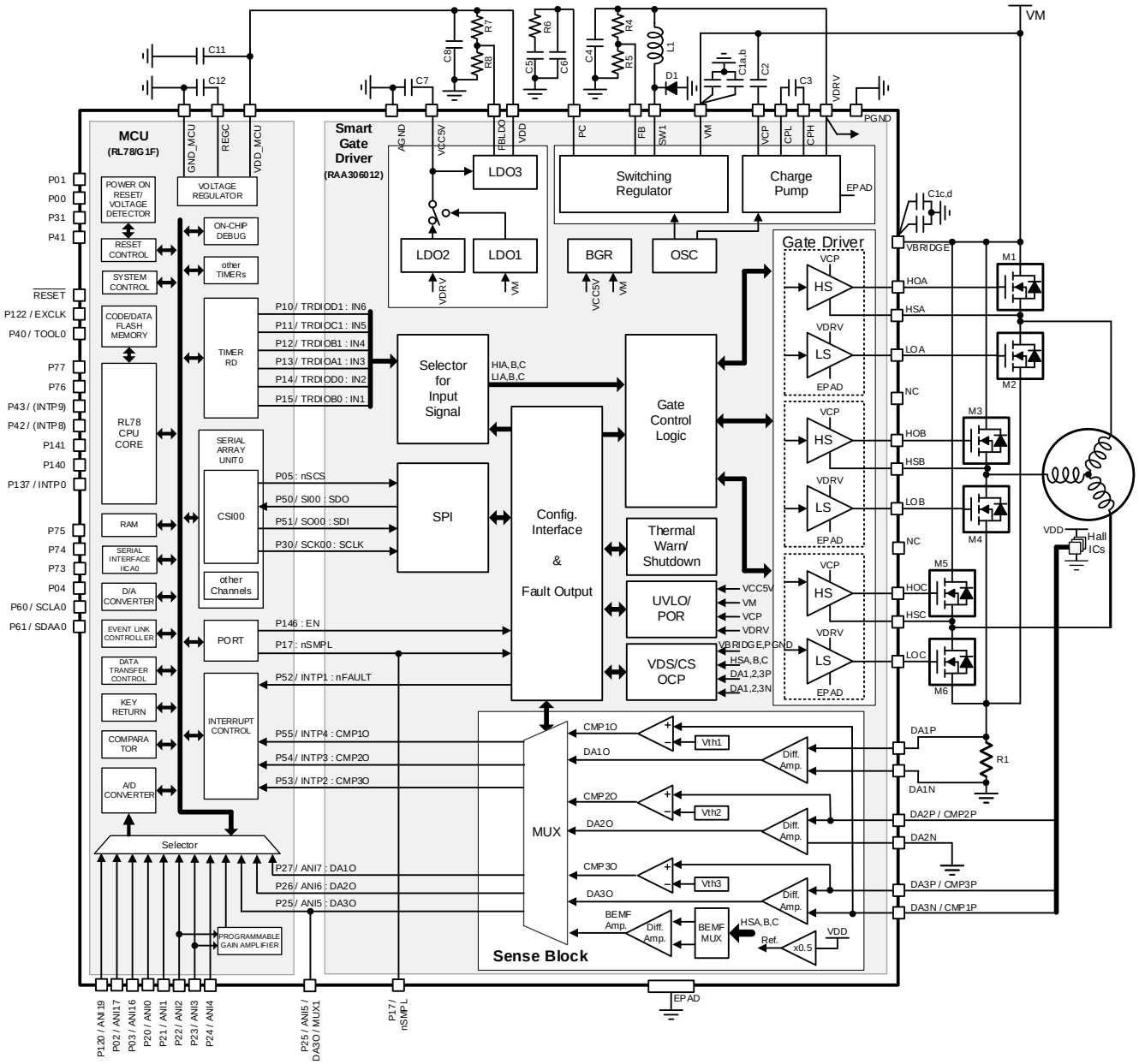


Figure 1-6 Simplified Block Diagram and Application – Hall Sensor Motor Drive by Using 3 Comparators

1.6.2 Sensorless Motor Drive (BEMF Sensing Comparator)

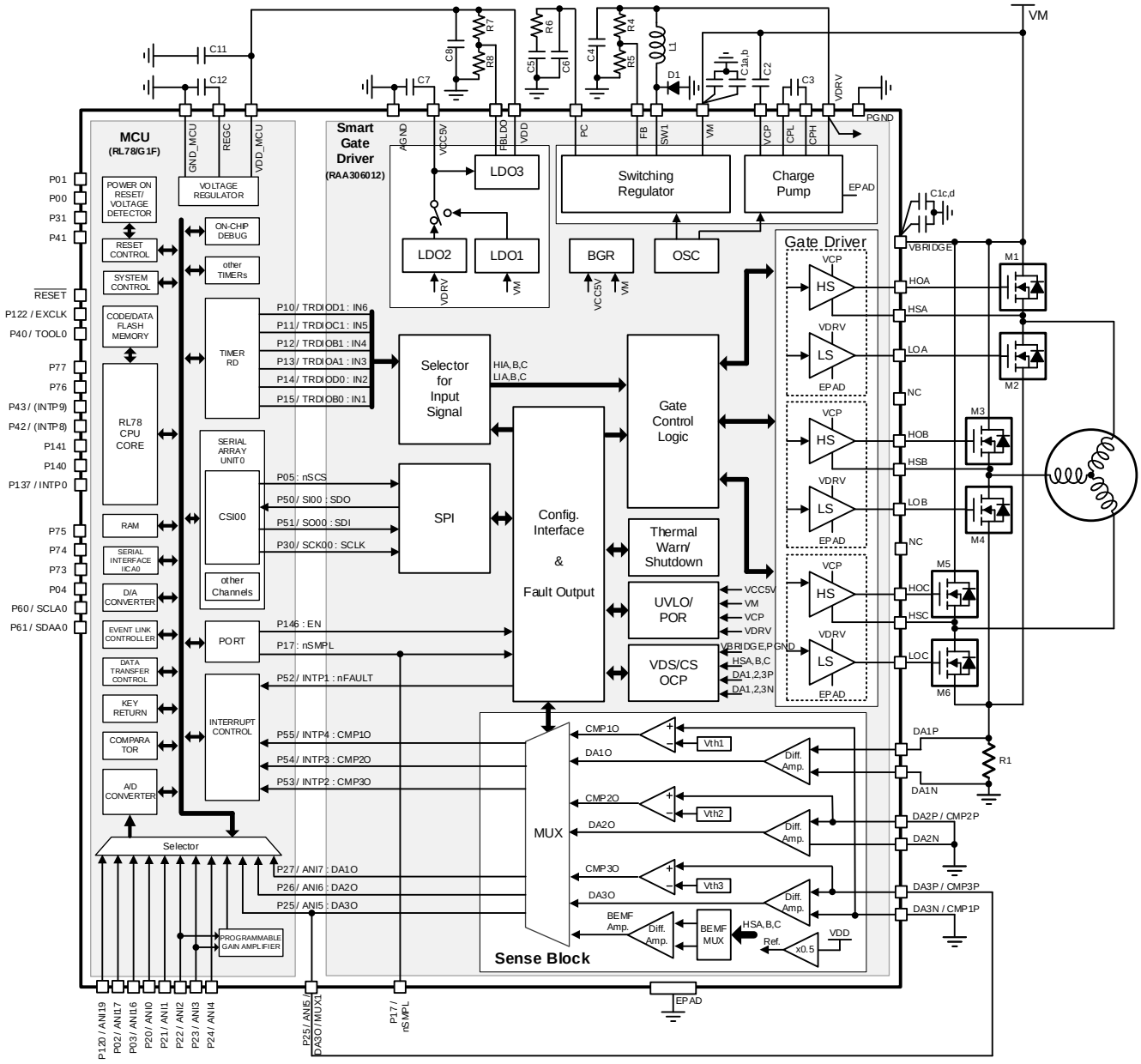


Figure 1-7 Simplified Block Diagram and Application – Sensorless Motor Drive by BEMF Sensing Comparator

1.6.3 Sensorless Motor Drive with MCU 5V Supply (BEMF Sensing Comparator)

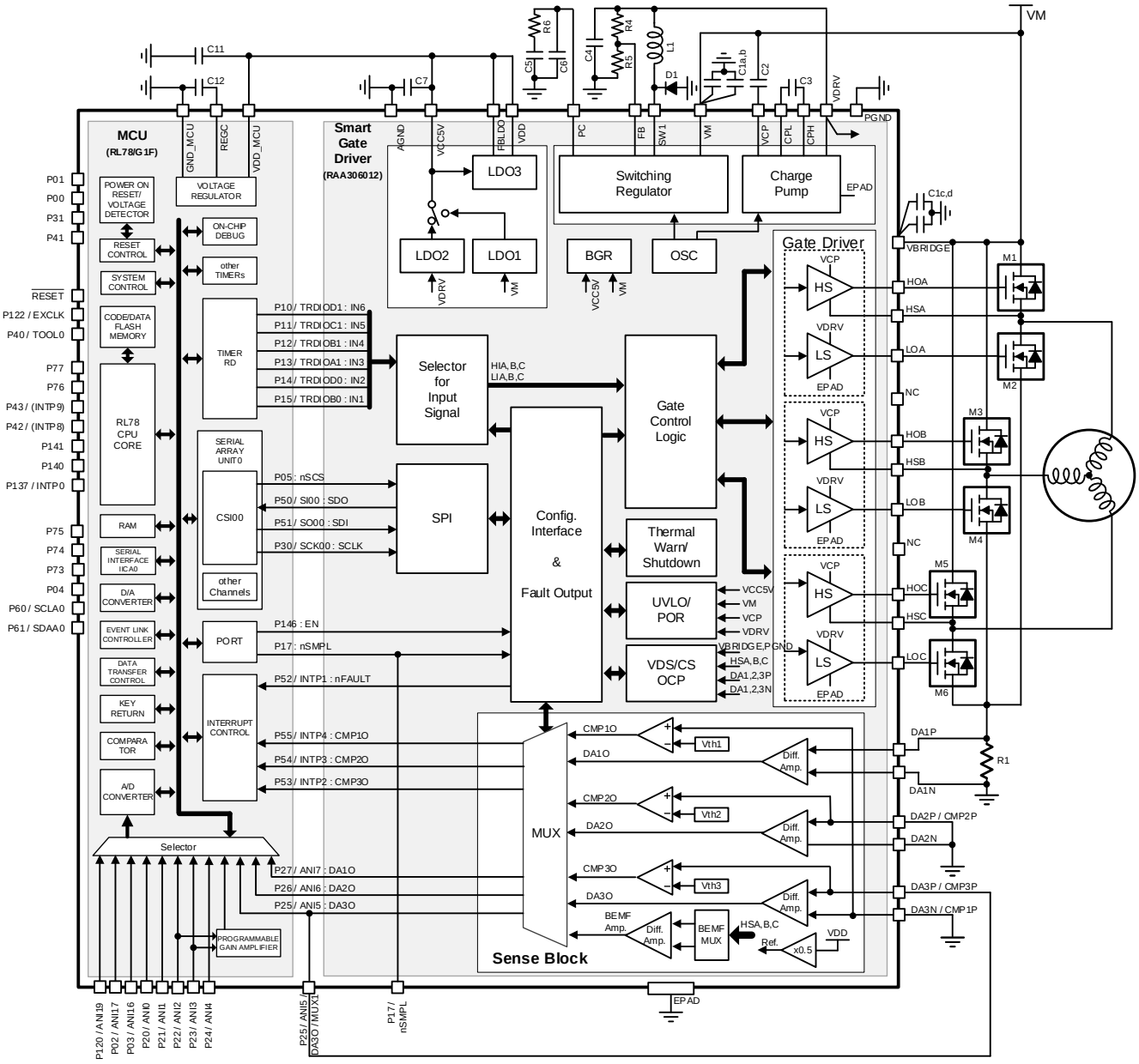


Figure 1-8 Simplified Block Diagram and Application
– Sensorless Motor Drive by BEMF Sensing Comparator with 5V MCU Supply

Chapter 2 MCU: RL78/G1F

The incorporated MCU into this device is a RL78/G1F 64Pin product (R5F11BLEGFB). However, the RL78/G1F in this product has internal connection ports with the smart gate driver and unconnected ports, which limits the usable peripheral functions. This chapter describes the limitations and precautions for the RL78/G1F when using this product. For details on the usage of each function, refer to "***RL78/G1F User's Manual: Hardware (R01UH0516EJ)***" and "***Technical Update***".

2.1 Port Connections, Functions, and Settings

2.1.1 Port Connections to Smart Gate Driver and Pins

Figure 2-1 shows the port connection diagram between the RL78/G1F, smart gate driver, and pins. The ports marked with "x" are unconnected ports.

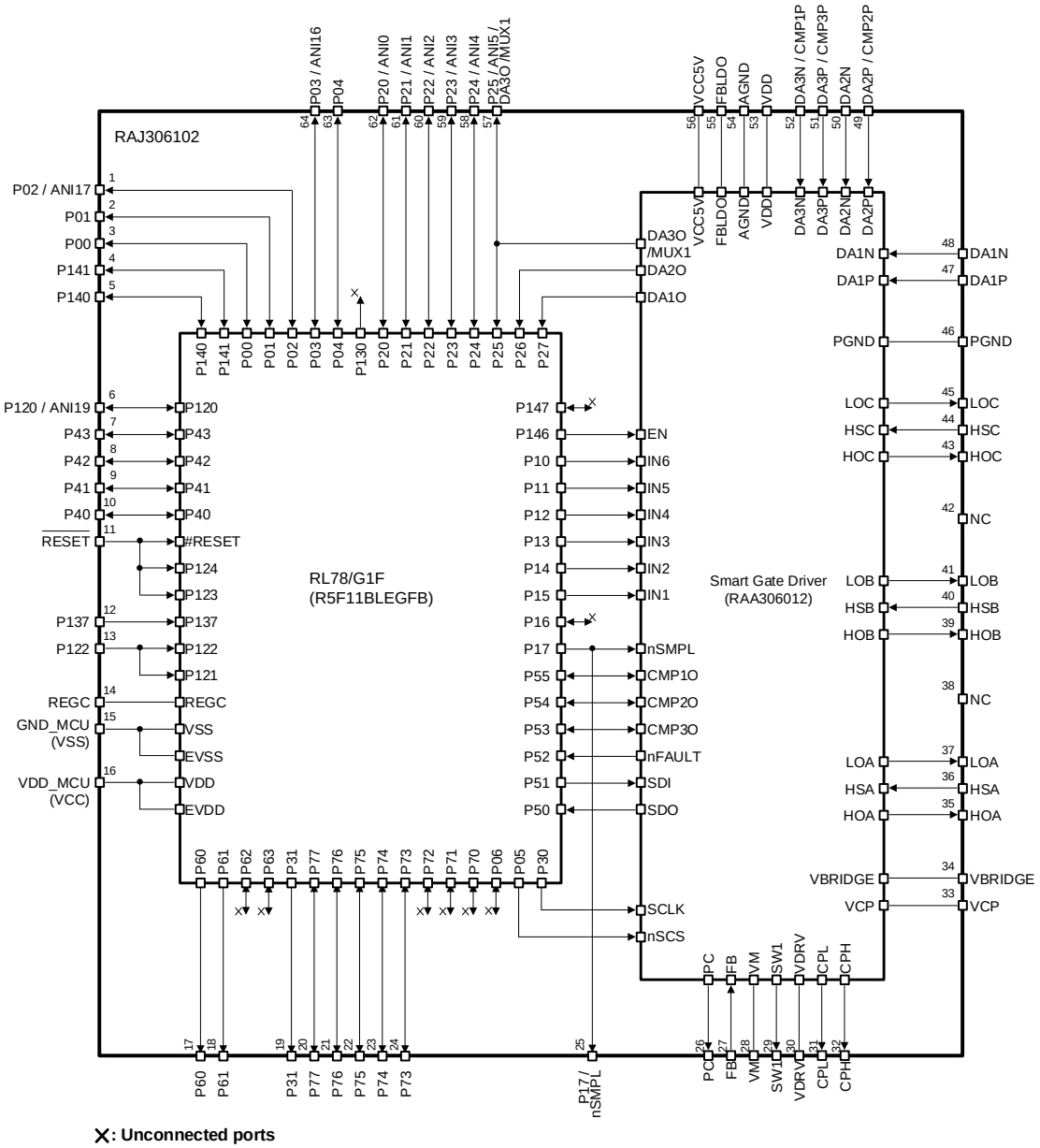


Figure 2-1 Port Connection Diagram between RL78/G1F, Smart Gate Driver, and Pins

2.1.2 Port Functions

Table 2-1 and ***Table 2-2*** show the port functions of the embedded RL78/G1F. The ports marked “Int.” (Internal) in the “Connection” column have functions not available because they are used to control the smart gate driver through internal connections. In addition, the ports marked “No Conn.” (Not connected) and P121, P123, P124 are NOT available, including alternate functions. Assign port functions in consideration of these limitations.

Table 2-1 RL78/G1F Port Functions (1/2) Note1

Port Name	Port Type	I/O	Initial	Connection		Alternate Function		Note
						Available	NOT available	
P00	7-1-4	I/O	Input	Ext.	P00	TI00 / TRGCLK A / (TRJO0) / (INTP8)	–	
P01	8-1-3	I/O	Input	Ext.	P01	TO00 / TRGCLKB / TRJIO0 / (INTP10)	–	
P02	7-9-2	I/O	Analog	Ext.	P02	ANI17 / SO10 / TxD1 / IVCMP10	–	
P03	8-9-2	I/O	Analog	Ext.	P03	ANI16 / SI10 / RxD1 / SDA10 / IVCMP11	–	
P04	8-1-4	I/O	Input	Ext.	P04	SCK10 / SCL10	–	
P05	7-1-3	I/O	Input	Int.	nSCS	-	(INTP10)	
P06	7-1-3	I/O	Input	No Conn.	-	–	P06 / (INTP11) / (TRJIO0)	
P10	8-3-8	I/O	Analog	Int.	IN6	TRDIOD1	ANI20 / SCK11 / SCL11	
P11	7-3-8	I/O	Analog	Int.	IN5	TRDIOC1	ANI21 / SI11 / SDA11	
P12	7-3-7	I/O	Analog	Int.	IN4	TRDIOB1	ANI22 / SO11 / (INTP5)	
P13	7-3-8	I/O	Analog	Int.	IN3	TRDIOA1	ANI23 / TxD2 / SO20 / IrTxD	
P14	8-3-8	I/O	Analog	Int.	IN2	TRDIOD0	ANI24 / RxD2 / SI20 / SDA20 / (SCLA0) / IrRxD	
P15	8-1-8	I/O	Input	Int.	IN1	TRDIOB0	SCK20 / SCL20 / (SDAA0)	
P16	8-1-7	I/O	Input	No Conn.	-	–	P16 / TI01 / TO01 / INTP5 / TRDIOC0 / (SI00) / (RxD0) / (TRDIOA1)	
P17	8-1-8	I/O	Input	Int.	nSMPL	TI02 / TO02	(SO00) / (TxD0) / (TRDIOD0) / TRDIOA0 / TRDCLK	2
				Ext.	P17			
P20	4-9-1	I/O	Analog	Ext.	P20	ANI0 / AVREFP / IVCMP12 / (INTP11)	–	
P21	4-9-1	I/O	Analog	Ext.	P21	ANI1 / AVREFM / IVCMP13	–	
P22	4-16-1	I/O	Analog	Ext.	P22	ANI2 / ANO0 / PGA I / IVCMP0	–	
P23	4-15-1	I/O	Analog	Ext.	P23	ANI3 / ANO1 / PGAGND	–	
P24	4-3-3	I/O	Analog	Ext.	P24	ANI4	–	
P25	4-3-3	I/O	Analog	Int.	DA3O/MUX1	ANI5	–	3
				Ext.	P25			
P26	4-3-3	I/O	Analog	Int.	DA2O	ANI6	–	
P27	4-3-3	I/O	Analog	Int.	DA1O	ANI7	–	
P30	8-1-4	I/O	Input	Int.	SCLK	SCK00	INTP3 / RTC1HZ / SCL00 / TRJO0 / (TRDIOB1)	
P31	7-1-3	I/O	Input	Ext.	P31	TI03 / TO03 / (TRJIO0) / (PCLBUZ0) / VCOUT1	INTP4	
P40	7-1-3	I/O	Input	Ext.	P40	TOOL0	–	
P41	7-1-3	I/O	Input	Ext.	P41	(TRJIO0)	–	
P42	7-1-3	I/O	Input	Ext.	P42	(INTP8)	–	
P43	7-1-3	I/O	Input	Ext.	P43	(INTP9)	–	

Note1: For details on port and alternate functions, refer to “***RL78/G1F User’s Manual: Hardware (R01UH0516EJ)***”. The ports shown in gray hatching are not connected and cannot be assigned, including alternate functions.

Note2: When using this port as P17 (Digital input/output), TI02, or TO02 function, the S/H function of the differential amplifier in the smart gate driver is not available. Please set all of BEMF_SH, DA1_SH, DA2_SH, and DA3_SH bit in SNSCTL2 register of the smart gate driver to “0”. For details, refer to ***3.2.1.15***.

Note3: When using this port as P25 (Digital input/output) or ANI5 function, Set MUX bits in SNSCTL5 register of the smart gate driver to 000b”. DA3O/MUX1 terminal has 330kΩ pulldown resistance. For details, refer to ***3.2.1.18***, and ***6.5.5*** of ***“RAJ306102 Datasheet (R18DS0039EJ)”***.

Table 2-2 RL78/G1F Port Functions (2/2) Note1

Port Name	Port Type	I/O	Initial	Connection		Alternate Function		Note
						Available	NOT available	
P50	8-1-4	I/O	Input	Int.	SDO	SI00	RxD0 / TOOLRxD / SDA00 / TRGIOA / (TRJO0) / (TRDIOC1)	
P51	7-1-4	I/O	Input	Int.	SDI	SO00	INTP2 / TxD0 / TOOLTxD / TRGIOB / (TRDIOD1)	
P52	7-1-3	I/O	Input	Int.	nFAULT	(INTP1)	-	
P53	7-1-3	I/O	Input	Int.	CMP3O	(INTP2)	-	
P54	7-1-3	I/O	Input	Int.	CMP2O	(INTP3)	-	
P55	8-1-4	I/O	Input	Int.	CMP1O	(INTP4)	(PCLBUZ1) / (SCK00)	
P60	12-1-2	I/O	Input	Ext.	P60	SCLA0	-	
P61	12-1-2	I/O	Input	Ext.	P61	SDAA0	-	
P62	12-1-2	I/O	Input	No Conn.	-	-	P62 / $\overline{SSI00}$	
P63	12-1-2	I/O	Input	No Conn.	-	-	P63	
P70	7-1-3	I/O	Input	No Conn.	-	-	P64 / KR0 / SCK21 / SCL21 / (VCOUT1)	
P71	7-1-4	I/O	Input	No Conn.	-	-	P65 / KR1 / SI21 / SDA21 / (VCOUT0)	
P72	7-1-3	I/O	Input	No Conn.	-	-	-	
P73	7-1-3	I/O	Input	Ext.	P73	KR3 / SO01	-	
P74	7-1-4	I/O	Input	Ext.	P74	KR4 / SI01 / SDA01	INTP8	
P75	7-1-3	I/O	Input	Ext.	P75	KR5 / SCK01 / SCL01	INTP9	
P76	7-1-3	I/O	Input	Ext.	P76	KR6 / INTP10	(RxD2)	
P77	7-1-3	I/O	Input	Ext.	P77	KR7 / INTP11	(TxD2)	
P120	7-3-3	I/O	Analog	Ext.	P120	ANI19 / VCOUT0	-	
P121	2-2-1	In	Input	Ext.	P122	-	P121 / X1	
P122	2-2-1	In	Input	Ext.	P122	EXCLK	X2	
P123	2-2-1	In	Input	Ext.	$\overline{RESET}$	-	P123 / XT1	
P124	2-2-1	In	Input	Ext.	$\overline{RESET}$	-	P124 / XT2 / EXCLKS	
P130	1-1-1	Out	Output	No Conn.	-	-	P130	
P137	2-1-2	In	Input	Ext.	P137	INTP0	-	
P140	7-1-3	I/O	Input	Ext.	P140	PCLBUZ0 / INTP6	-	
P141	7-1-3	I/O	Input	Ext.	P141	PCLBUZ1 / INTP7	-	
P146	7-1-3	I/O	Input	Int.	EN	-	-	
P147	7-3-3	I/O	Analog	No Conn.	-	-	P147 / ANI18 / IVREF0	
$\overline{RESET}$	2-1-1	In	-	Ext.	$\overline{RESET}$	-	-	
VDD	-	-	-	Ext.	VDD_MCU	-	-	
EVDD	-	-	-	Ext.	VDD_MCU	-	-	
AGND	-	-	-	Ext.	GND_MCU	-	-	
REGC	-	-	-	Ext.	REGC	-	-	

Note1: For details on port and alternate functions, refer to "***RL78/G1F User's Manual: Hardware (R01UH0516EJ)***". The ports shown in gray hatching are not connected and cannot be assigned, including alternate functions.

2.1.3 Recommended Port Settings

2.1.3.1 Port Assignments

Table 2-3 shows RL78/G1F port assignments and precautions for internally connected and unconnected ports.

Table 2-3 RL78/G1F Port Assignments and Precautions for Internally Connected and Unconnected Ports

Port Symbol	I/O Pins	Pin Count	Internal Connection Ports (Smart Gate Driver Terminals)	Precautions	Note
PORT0	P00 to P04	5	-	-	
	-	-	P05 (nSCS)	This port is used as SPI chip select output of Smart Gate Driver. Set to the digital output port.	
	-	-	P06 (Not connected)	Set to the digital output port.	
PORT1	-	-	P10 - P15 (IN6 - IN1)	This port is used as the output port of PWM signal. Set to Timer RD function.	
	-	-	P16 (Not connected)	Set to the digital output port.	
	P17	1	P17 (nSMPL)	When using the S/H function of the Smart Gate Driver, set to the digital output port. When the S/H function is not used, it can be used as an external connection pin of the MCU.	1
PORT2	P20 – P24	5	-	-	
	P25	1	P25 (DA3O)	When using the input for the differential amplifier output signal (DA3O), set to the analog input port. When the differential amplifier output signal (DA3O) is not used, it can be used as an external connection pin for MCU.	2
	-	-	P26 (DA2O)	Set to the analog input port for the differential amplifier output signal (DA2O).	
	-	-	P27 (DA1O)	Set to the analog input port for the differential amplifier output signal (DA1O).	
PORT3	-	-	P30 (SCLK)	This port is used as SPI clock output of Smart Gate Driver. Set to SCK00 on the Serial Array Unit (CSI00).	
	P31	1	-	-	
PORT4	P40 - P43	4	-	-	
PORT5	-	-	P50 (SDO)	This port is used as SPI data Smart Gate Driver. Set to SI00 on the Serial Array Unit (CSI00).	
	-	-	P51 (SDI)	This port is used as SPI data output to Smart Gate Driver. Set to SO00 on the Serial Array Unit (CSI00).	
	-	-	P52 (nFAULT)	This port is used as the input for Fault indicator output of Smart Gate Driver. Set to the digital input port or the interrupt function. And enable the pull-up resistor option of this port.	
	-	-	P55 - P53 (CMPzO (z = 1, 2, 3))	When using the comparator function of the Smart Gate Driver, set to the digital input port or the interrupt function. When used as the detect phase selection of BEMF sense amplifier, set to the digital output port.	
PORT6	P60, P61	2	-	-	
	-	-	P62, P63 (Not connected)	Set to the digital output port and the output latch to "0b".	
PORT7	-	-	P70 - P72 (Not connected)	Set to the digital output port.	
	P73 - P77	5	-	-	
PORT12	P120, P122	2	-	-	
	-	-	P121 (Not connected)	Connected to P122 internally. Set to the digital input port.	
	-	-	P123, P124 (Not connected)	Connected to RESET Set to the digital input port.	
PORT13	-	-	P130 (Not connected)	No port setting is required by the dedicated output port.	
	P137	1	-	-	
PORT14	P140, P141	2	-	-	
	-	-	P146 (EN)	Set to the digital output port for enable control of Smart Gate Driver.	
	-	-	P147 (Not connected)	Set to the digital input port.	
Total External Connection Pins		29			

Note1: When using this pin as an external connection pin of the MCU, set all of BEMF_SH bit, DA1_SH bit, DA2_SH bit, and DA3_SH bit in the Sense Block Control 2 register (SNSCTL2) of the smart gate driver to “0b”. For details, refer to ***3.2.1.15***.

Note2: When using this pin as an external connection pin of the MCU, set MUX bits in SNSCTL5 register of the smart gate driver to 000b”. DA3O/MUX1 terminal has 330kΩ pulldown resistance. For details, refer to ***3.2.1.18***, and ***6.5.5*** of ***“RAJ306102 Datasheet (R18DS0039EJ)”***.

2.1.3.2 Handling of RL78/G1F Unused and Unconnected Ports

Table 2-4 shows how to handle unused and unconnected ports of RL78/G1F embedded in this product. For unused external connection ports, either handling marked “Input” or "Output" in the “Recommended Handling” is required according to the port mode.

Table 2-4 Handling of RL78/G1F Unused and Unconnected Ports

Port Name	I/O	Connection	Recommended Handling
P00 - P04	I/O	Ext.	Input: Independently connect to VDD_MCU or GND_MCU via a resistor. Output: Leave open.
P06		Not Connected	Set to the digital output port.
P16		Not Connected	
P17		Int. / Ext.	Input: Independently connect to GND_MCU via a resistor. Output: Set the port’s output latch to "0b" and leave the pin open.
P20 - P24		Ext.	Input: Independently connect to VDD_MCU or GND_MCU via a resistor. Output: Leave open.
P25		Int. / Ext.	Set to the analog input port.
P31		Ext.	Input: Independently connect to VDD_MCU or GND_MCU via a resistor. Output: Leave open.
P40 / TOOL0		Ext.	Input: Independently connect to VDD_MCU via a resistor. Output: Leave open.
P41 - P43		Ext.	Input: Independently connect to VDD_MCU or GND_MCU via a resistor. Output: Leave open.
P60, P61		Ext.	Input: Independently connect to VDD_MCU or GND_MCU via a resistor. Output: Set the port’s output latch to “0b” and leave the pin open or set the port’s output latch to “1b” and independently connect to VDD_MCU or GND_MCU via a resistor.
P62, P63		Not Connected	Set to the digital output port and the output latch to "0b".
P70 - P72		Not Connected	Set to the digital output port.
P73 - P77		Ext.	Input: Independently connect to VDD_MCU or GND_MCU via a resistor. Output: Leave open.
P120		Ext.	
P121	In	P122	No port setting is required as it is connected to P122 pin.
P122		Ext.	Independently connect to VDD_MCU or GND_MCU via a resistor.
P123, P124		$\overline{\text{RESET}}$	No port setting is required as it is connected to $\overline{\text{RESET}}$ pin.
P130	Out	Not Connected	No port setting is required by the dedicated output port.
P137	In	Ext.	Independently connect to VDD_MCU or GND_MCU via a resistor.
P140, P141	I/O	Ext.	Input: Independently connect to VDD_MCU or GND_MCU via a resistor. Output: Leave open.
P147		Not Connected	Set to the digital output port.
$\overline{\text{RESET}}$	In	Ext.	Connect to VDD_MCU directly or via a resistor.
REGC	-	Ext.	Connect to GND_MCU via a capacitor (0.47 to 1µF).

2.1.3.3 Internal Connection Port Settings

In this device, some of the RL78/G1F ports are internally connected to the smart gate driver, which changes its operating state according to EN terminal input (P146: EN output port of RL78/G1F). The functions of internal connection terminals INz (z = 1, 2, 3, 4, 5, 6) and CMPzO (z = 1, 2, 3) depend on EN terminal input. Therefore, the suitable port settings according to EN terminal input are necessary for corresponding RL78/G1F ports. ***Table 2-5*** shows the internal connection port settings according to the EN terminal input. The internal connection port settings should be completed before the smart gate driver goes into Operating Mode (before inputting High to the EN terminal). For details on each port setting, refer to ***2.1.4***. In addition, for details on the port setting procedures for INz (z = 1, 2, 3, 4, 5, 6) and CMPzO (z = 1, 2, 3), refer to ***Chapter 4***.

Table 2-5 Port Settings for the Internal Connection Ports

<table>
<tr><th rowspan="2">Port Name</th><th rowspan="2">Initial</th><th rowspan="2">Connection</th><th colspan="2">Port Settings</th><th rowspan="2">Note</th></tr>
<tr><th>EN pin is Low
(Smart Gate Driver is in Sleep Mode)</th><th>EN pin is High
(Smart Gate Driver is in Operating Mode)</th></tr>
<tr><td>P05</td><td rowspan="8">Input port</td><td>nSCS</td><td colspan="2">Set to the digital output port to be used as SPI chip select output of Smart Gate Driver.</td><td>1</td></tr>
<tr><td>P10</td><td>IN6</td><td rowspan="6">Set to the digital output port and set the output latch to "0b".</td><td rowspan="6">Set to the digital output port or Timer RD function to output PWM signal.</td><td rowspan="6">3, 4</td></tr>
<tr><td>P11</td><td>IN5</td></tr>
<tr><td>P12</td><td>IN4</td></tr>
<tr><td>P13</td><td>IN3</td></tr>
<tr><td>P14</td><td>IN2</td></tr>
<tr><td>P15</td><td>IN1</td></tr>
<tr><td rowspan="2">P17</td><td rowspan="2">nSMPL / P17</td><td colspan="2">When using the S/H function (nSMPL): Set to the digital output port.
High output: Hold
Low output: Sample</td><td rowspan="2">2</td></tr>
<tr><td colspan="2">When using port functions (P17): Set the suitable port function (P17).</td></tr>
<tr><td rowspan="2">P25</td><td rowspan="4">Analog input</td><td rowspan="2">DA3O / P25</td><td colspan="2">When using the input for the differential amplifier output signal (DA3O): Set to the analog input port.</td><td rowspan="2"></td></tr>
<tr><td colspan="2">When using port function (P25): Set the suitable port function (P25).
Consider that this pin has 330kohm pulldown resistance.</td></tr>
<tr><td>P26</td><td>DA2O</td><td colspan="2" rowspan="2">Set to the analog input port for the differential amplifier output signal (DA2O/DA1O).</td><td></td></tr>
<tr><td>P27</td><td>DA1O</td><td></td></tr>
<tr><td>P30</td><td rowspan="7">Input port</td><td>SCLK</td><td colspan="2">Set to SCK00 on the Serial Array Unit (CSI00).</td><td>2</td></tr>
<tr><td>P50</td><td>SDO</td><td colspan="2">Set to SI00 on the Serial Array Unit (CSI00) and enable the pull-up resistor option of this port.</td><td></td></tr>
<tr><td>P51</td><td>SDI</td><td colspan="2">Set to SO00 on the Serial Array Unit (CSI00).</td><td>2</td></tr>
<tr><td>P52</td><td>nFAULT</td><td colspan="2">Set to the digital input port or the interrupt function and enable the pull-up resistor option of this port.</td><td></td></tr>
<tr><td>P53</td><td>CMP3O</td><td rowspan="3">Set to the digital input port.</td><td>When using the comparator function of the Smart Gate Driver: Set to the digital input port or the interrupt function.</td><td rowspan="3">5, 6</td></tr>
<tr><td>P54</td><td>CMP2O</td><td rowspan="2">When used as the detect phase selection of BEMF sense amplifier: Set to the digital output port. For the unused port, set to the digital input port. For details, refer to 3.2.1.15.</td></tr>
<tr><td>P55</td><td>CMP1O</td></tr>
<tr><td>P146</td><td>EN</td><td>Set to the digital output port and set the output latch to "0b".</td><td>Set to the digital output port and set the output latch to "1b".</td><td></td></tr>
</table>

Note1: A pull-up resistor (380kΩ) is built into the terminal on the smart gate driver. When the EN terminal is Low, the current required by the pull-up resistor can be reduced by keeping the output to High.
Note2: A pull-down resistor (380kΩ) is built into the terminal on the smart gate driver. When the EN terminal is Low, the current required by the pull-down resistor can be reduced by keeping the output to Low.
Note3: When setting EN pin from Low to High, set the output latch to “0b” first. Also, do not output High by Timer RD or output latch function until the GDSELx (x = A, B, C) registers are set.
Note4: When setting the EN pin from High to Low, set to the digital output port and set the output latch to "0b" first.
Note5: When setting the EN pin from High to Low, set to the digital input port first.
Note6: When used as the detect phase selection of BEMF sense amplifier, set the BEMF_PH bits in SNSCTL2 register of the smart gate driver first and then set the corresponding ports to the digital output port.

2.1.4 Internal Connection Ports for Smart Gate Driver

2.1.4.1 EN Output Port: P146

The EN output port controls the operation mode of the smart gate driver. For details of the Operating Mode, refer to ***6.1*** of the ***"RAJ306102 Datasheet (R18DS0039EJ)"***.

(1) After the MCU reset is released, P146 is a digital input port, but it is driven low by the pull-down resistor (100kΩ) on the EN terminal of the smart gate driver. Therefore, after the MCU reset is released, the operation mode of the smart gate driver is in Sleep Mode.
(2) In the pin setting, it is recommended to set the output latch of the EN output port to "0b" to start from Low output.
(3) When setting "1b" to the output latch of the EN output port, the EN output port goes high, and the smart gate driver enters the Operating Mode. It is important to set the other port settings before setting the EN output port to High because the control by signals other than the EN signal are enabled.
(4) When stopping smart gate driver operation due to any abnormality, set the output latch of the EN output port to "0b" to set the EN output port to Low.

2.1.4.2 SPI Communication Ports (Master Side): P51 (SO00), P52 (SI00), P30 (SCK00), P05

The SPI communication ports are used to set smart gate driver registers and to check the fault status. SPI communication is performed by setting the 3-wire serial I/O (CSI00) of the Serial Array Unit and the Chip Select signal by the P05 digital output port. For SPI timing specifications and communication format of the smart gate driver, refer to ***5.5*** and ***6.6*** of the ***"RAJ306102 Datasheet (R18DS0039EJ)"***, and for details of control registers, refer to ***3.2.1***.

(1) After the MCU reset is released, these ports are digital input ports, but the SDI and SCLK terminals of the smart gate driver are driven Low by a pull-down resistor (380kΩ) each and the nSCS pin is driven High by a pull-up resistor (380kΩ). However, the SDO pin is Hi-Z during non-communication because it is an open-drain output. Therefore, after the MCU reset is released, it is necessary to enable the pull-up resistor option of P50 by the port setting.
(2) In the port settings, set the 3-wire serial I/O (CSI00) of the Serial Array Unit of the MCU and the digital output port of P05. The SDO terminal is an open-drain output, so the pull-up resistor option of P50 must be enabled. For data and clock phase selection in CSI mode, set to type 2 (DAP00 bit = "0b", CKP00 bit = "1b") in serial communication operation setting register 00 (SCR00). Set the communication speed to 2MHz or less.
(3) SPI communication can be performed when the EN output port is high (Operating Mode). When the EN output port is set to Low, SPI communication is disabled. For details of SPI communication sequence for the register setting and fault status check of the smart gate driver, refer to ***Chapter 4***.

2.1.4.3 INz (z = 1, 2, 3, 4, 5, 6) Output Ports: P15, P14, P13, P12, P11, P10

INz (z = 1, 2, 3, 4, 5, 6) output ports control each phase gate driver output of the smart gate driver. These ports are assigned to the gate driver control inputs HIx and LIx (x = A, B, C) according to the register settings of the smart gate driver. The gate driver outputs are controlled based on the truth table (see ***6.4.2*** in the ***"RAJ306102 Datasheet (R18DS0039EJ)"***) according to the polarity of HIx and LIx (x = A, B, C). The port outputs are normally controlled by the digital output or the PWM output by Timer RD.

(1) After the MCU reset is released, these ports are analog or digital input ports, but are driven Low by the pull-down resistors (380kΩ) on each INz (z = 1, 2, 3, 4, 5, 6) terminal of the smart gate driver.

(2) In the port settings, set to the digital output port and set the output latch to "0b" as the setting in Sleep Mode of the smart gate driver. These port settings prevent unexpected gate driver operation when the EN output port is set to High.

(3) After the EN output port is set to High, set the Phase-A Gate Driver Input Selection Register (GDSELA), Phase-B Gate Driver Input Selection Register (GDSELB), and Phase-C Gate Driver Input Selection Register (GDSELC) to the suitable value to assign the gate driver control inputs HIx and LIx (x = A, B, and C) from INz (z = 1, 2, 3, 4, 5, 6) terminals. For this device, please use the following settings. Note that INz (z = 1, 2, 3, 4, 5, 6) output ports should be kept Low during these register settings. These port settings prevent abnormal operation caused by register setting changes. Note that the following settings are for the complementary PWM mode by using Timer RD.

- Phase-A Gate Driver Input Selection Register (GDSELA) = "x001x010b" Note1
- Phase-B Gate Driver Input Selection Register (GDSELB) = "x011x101b" Note1
- Phase-C Gate Driver Input Selection Register (GDSELC) = "x100x110b" Note1

Note1: The "x" position should be set to "0b" or "1b" individually according to the user's control specifications.

(4) The smart gate driver register settings are reset when the EN terminal goes Low. Therefore, when setting the EN output port to Low, set the INz (z = 1, 2, 3, 4, 5, 6) output ports to Low output first and then set the EN output port to Low.

(5) When the nFAULT input port goes Low due to a fault detection and the gate driver is disabled, set the INz (z = 1, 2, 3, 4, 5, 6) output ports to Low. When the smart gate driver is recovered from a fault condition, the gate driver is enabled according to the fault condition. These port settings prevent unexpected gate driver operation. For the fault and recovery action of the smart gate driver, refer to ***6.2*** in the ***"RAJ306102 Datasheet (R18DS0039EJ)"***.

2.1.4.4 nFAULT Input Port: P52

The nFAULT input port is used to input the fault indicator of the smart gate driver. It is pulled low if any of the fault conditions occur. It is pulled high when all the fault conditions are removed, and all chip power rail start-ups are done. The smart gate driver can be configured to enable or disable each fault detection by register settings. For details of the Fault Control Registers, refer to ***3.2.1.5*** and ***3.2.1.6***.

(1) After the MCU reset is released, P52 is a digital input port. Since the nFAULT terminal of the smart gate driver is also an open-drain output, this port is Hi-Z. Therefore, after the MCU reset is released, it is necessary to enable the pull-up resistor option of P52 by the port setting.

(2) In the port settings, set to the digital input port or interrupt function to confirm the fault indicator of the smart gate driver. Also, the pull-up resistor option must be enabled.

(3) At power-on, when the EN output port is Low, the nFAULT input port goes High if the pull-up resistor option of P52 is enabled. The nFAULT input port switches to Low when the EN output port is set to High. The nFAULT input port goes High again if all power rail start-ups of smart gate driver have been done and all fault conditions are removed. For the control sequence considering the nFAULT behavior, refer to ***Chapter 4***.

2.1.4.5 DAzO (z = 1, 2, 3) Input Ports: P27, P26, P25

DAzO (z = 1, 2, 3) input ports are used to input analog output signals from the differential amplifiers, BEMF sense amplifier, or analog multiplexer in the smart gate driver.

(1) After the MCU reset is released, these ports are analog input ports, but are driven Low by the pull-down resistor (330kΩ) on the DAzO (z = 1, 2, 3) terminals of the smart gate driver.
(2) In the port settings, set to the analog input port for A/D conversion of the analog output signal from the smart gate driver.
(3) When the EN output port is high, the output signal of the DA3O terminal can be changed by the analog multiplexer according to register setting of the smart gate driver. For details, refer to Section 6.5.5 of the ***"RAJ306102 Datasheet (R18DS0039EJ)"***.
(4) P25 can also be used as an external connection pin. In this case, set the MUX bit in the Sense Block Control 5 register (SNSCTL5) of the smart gate driver to "000b". A pull-down resistor (330kΩ) is connected to P25. When using this pin as an external connection pin, this impedance must be considered.

2.1.4.6 CMPzO (z = 1, 2, 3) Input/Output Ports: P55, P54, P53

The CMPzO (z = 1, 2, 3) input/output ports are used as digital input ports to input the general purpose comparator output of the smart gate driver or as digital output ports to control the detect phase selection of the BEMF sense amplifier. The terminal functions are switched by the register settings of the smart gate driver. For details of the control register, refer to ***3.2.1.15***, and for details of the detect phase selection of the BEMF sense amplifier, refer to Section ***6.5.3*** of the ***"RAJ306102 Datasheet (R18DS0039EJ)"***.

(1) After the MCU reset is released, these ports are digital input ports, but are driven Low by the pull-down resistor (380kΩ) on the CMPzO (z = 1, 2, 3) terminals of the smart gate driver.
(2) Since the default function of the CMPzO (z = 1, 2, 3) terminals of the smart gate driver is a general purpose comparator output, set to the digital input port or interrupt function for P55, P54, and P53.
(3) To use P55, P54, and P53 for the detect phase selection of the BEMF sense amplifier, the register settings of the smart gate driver must be set to switch the terminal function of the smart gate driver to the detect phase selection input first for avoiding the collision by output signals of the MCU and smart gate driver. And after the register setting, the MCU ports used for the detect phase selection must be set to the digital output port. Note that the detect phase of the BEMF sense amplifier is selected from the two ports P55/P54 or P55/P53. The MCU ports not used as detect phase selection can be used as input port for general purpose comparator output. In this case, set to the digital input port or interrupt function.
(4) The register settings of the smart gate driver are reset when the EN terminal goes Low. To avoid the collision by output signals of the MCU and smart gate driver caused by the reset of register settings, when setting the EN output port to Low, set P55, P54, and P53 to digital input ports first, and then set the EN output port to Low.

2.1.4.7 nSMPL Output Port: P17

The nSMPL output port is used as a digital output port to control the S/H function of the differential amplifier or the BEMF sense amplifier of the smart gate driver. For details of the S/H function, refer to ***6.5.2*** and ***6.5.3*** of the ***"RAJ306102 Datasheet (R18DS0039EJ)"***.

(1) After the MCU reset is released, P17 is a digital input port, but is driven Low by the pull-down resistor (380kΩ) on the nSMPL terminal of the smart gate driver.

(2) In the port setting, when using the S/H function, set to the digital output and set the output latch to "0b". When not using the S/H function, the port can be used as an external connection pin of the MCU.

(3) After the S/H function is enabled by the register setting of the smart gate driver, sampling operation is performed when the nSMPL terminal is Low, and hold operation is performed when the nSMPL terminal is High. Note that the S/H operation of the BEMF sense amplifier has a period of hold operation even when the nSMPL output terminal is low. Refer to Section 6.5.3 in the ***"RAJ306102 Datasheet (R18DS0039EJ)"***.

2.2 Limitations of Peripheral Functions

The RL78/G1F in this product has internally connected and unconnected ports, which limits the peripheral functions that can be used. This section describes the limitations and cautions for each peripheral function. For details on how to use each function, refer to "***RL78/G1F User's Manual: Hardware (R01UH0516EJ)***" and for the latest information, refer to "***Technical Update"***.

Available peripheral functions with no limitations

- Timer RX
- Serial Interface IICA
- D/A Converter
- Programmable Gain Amplifier (PGA)
- Standby Function
- Reset Function
- Safety Function
- Regulator
- On-chip Debug Function
- Binary-coded Decimal (BCD) Correction Circuit Function

Available peripheral functions with limitations

- Port Functions (Peripheral I/O settings)
- Clock Generator
- Timer Array Unit
- Timer RJ
- Timer RD
- Timer RG
- Real-time Clock
- 12-bit Interval Timer
- Clock Output / Buzzer Output Controller
- Watchdog Timer
- A/D Converter
- Comparator (CMP)
- Serial Array Unit
- Data Transfer Controller (DTC)
- Event Link Controller (ELC)
- Interrupt Functions
- Key Interrupt Function
- Power-on-reset Circuit
- Voltage Detector
- Option Bytes
- Flash Memory

Unavailable peripheral function

- IrDA

2.2.1 Port Functions

2.2.1.1 Peripheral I/O Redirection Register

When using this device, set the peripheral I/O redirection registers 0, 1, 2, and 3 (PIOR0, PIOR1, PIOR2, and PIOR3) according to the recommended settings in ***Table 2-6***, ***Table 2-7***, ***Table 2-8***, and ***Table 2-9***. For details on the peripheral I/O redirection registers, refer to Sections ***4.3.7*** to ***4.3.10*** of the "***RL78/G1F User's Manual: Hardware (R01UH0516EJ)***".

Table 2-6 Recommended Settings for Peripheral I/O Redirection Register 0 (PIOR0) Note1

No.	Register Name	Bit Name	Function	Setting Value		Description	Note
				0b	1b		
1	PIOR0	PIOR07	INTP8	P42	P00	In the case of PIOR07 = 0b, INTP8 is assigned to P42 specified by PIOR00 bit (No.31).	3
2			INTP10	P76	P01	In the case of PIOR07 = 0b, INTP10 is assigned to P76 specified by PIOR01 bit (No.11).	
3			INTP11	P77	P20	In the case of PIOR07 = 0b, INTP11 is assigned to P77 specified by PIOR01 bit (No.12).	
4		PIOR06	-	-	-	Cannot be used. Please set to "0b".	2
5		PIOR05	-	-	-	Cannot be used. Please set to "0b".	2
6		PIOR04	PCLBUZ1	P141	P55	Set to "0b". P55 is connected internally as the CMP1O input/output port.	2
7			INTP5	P16	P12	Set to "0b", but this is not available. P16 is an unconnected port. P12 is connected internally as the IN4 output port.	
8		PIOR03	PCLBUZ0	P140	P31	-	
9		PIOR02	SCLA0	P60	P14	Set to "0b". P14 is connected internally as the IN2 output port.	2
10			SDAA0	P61	P15	Set to "0b". P15 is connected internally as the IN1 output port.	
11		PIOR01	INTP10	P76	P05	Set to "0b". INTP10 is specified by PIOR07 bit (No.2).	2
12			INTP11	P77	P06	Set to "0b". INTP11 is specified by PIOR07 bit (No.3).	
13			RxD2	P14	P76	Set to "0b", but this is not available. P14 is connected internally as the IN2 output port.	
14			TxD2	P13	P77	Set to "0b", but this is not available. P13 is connected internally as the IN3 output port.	
15			SCL20	P15	-	Set to "0b", but this is not available. P15 is connected internally as the IN1 output port.	
16			SDA20	P14	-	Set to "0b", but this is not available. P14 is connected internally as the IN2 output port.	
17			SI20	P14	-	Set to "0b", but this is not available. P14 is connected internally as the IN2 output port.	
18			SO20	P13	-	Set to "0b", but this is not available. P13 is connected internally as the IN3 output port.	
19			SCK20	P15	-	Set to "0b", but this is not available. P15 is connected internally as the IN1 output port.	
20			TxD0	P51	P17	Set to "0b", but this is not available. P51 is connected internally as the SPI communication port (SO00).	
21			RxD0	P50	P16	Set to "0b", but this is not available. P50 is connected internally as the SPI communication port (SI00).	
22			SCL00	P30	-	Set to "0b", but this is not available. P30 is connected internally as the SPI communication port (SCK00).	
23			SDA00	P50	-	Set to "0b", but this is not available. P50 is connected internally as the SPI communication port (SI00).	
24			SI00	P50	P16	Set to "0b". SI00 is assigned to P50 for SPI communication with the Smart Gate Driver.	
25			SO00	P51	P17	Set to "0b". SO00 is assigned to P51 for SPI communication with the Smart Gate Driver.	
26			SCK00	P30	P55	Set to "0b". SCK00 is assigned to P30 for SPI communication with the Smart Gate Driver.	
27		PIOR00	INTP1	P50	P52	Set to "1b". INTP1 can be assigned to P52 for nFAULT input port.	3
28			INTP2	P51	P53	Set to "1b". INTP2 can assigned to P53 for CMP3O input port.	
29			INTP3	P30	P54	Set to "1b". INTP3 can be assigned to P54 for CMP2O input port.	
30			INTP4	P31	P55	Set to "1b". INTP4 can be assigned to P55 for CMP1O input port.	
31			INTP8	P74	P42	Set to "1b". INTP8 is assigned according to PIOR07 bit (No.1).	
32			INTP9	P75	P43	Set to "1b". INTP9 is assigned to P43 by the assignment of other port functions.	

Table 2-7 Recommended Settings for Peripheral I/O Redirection Register 1 (PIOR1) Note1

No.	Register Name	Bit Name	Function	Setting Value		Description	Note
				0b	1b		
33	PIOR1	PIOR13/ PIOR12	TRJO0	00b: Assigned to P30 01b: Assigned to P50 10b: Assigned to P00 11b: Invalid		Set PIOR13 and PIOR12 bits to “10b”. Since P30 and P50 are connected internally as the SPI communication ports (SCK00, SI00) respectively, TRJO0 can be assigned to P00 only.	4
34		PIOR11/ PIOR10	TRJIO0	00b: Assigned to P01 01b: Assigned to P31 10b: Assigned to P41 11b: Assigned to P06		Set PIOR11 and PIOR10 bits to a value other than “11b”. This function cannot be assigned to P06 because it is an unconnected port.	4

Table 2-8 Recommended Settings for Peripheral I/O Redirection Register 2 (PIOR2) Note1

No.	Register Name	Bit Name	Function	Setting Value		Description	Note
				0b	1b		
35	PIOR2	PIOR27	-	-	-	Not available. Please set to “0b”.	2
36		PIOR26	TRDIOD0	P14	P17	Set to “0b”. TRDIOD0 is assigned to P14 as the IN2 output port for PWM waveform output.	2
37		PIOR25	TRDIOD1	P10	P51	Set to “0b”. TRDIOD1 is assigned to P10 as the IN6 output port for PWM waveform output.	2
38		PIOR24	TRDIOC1	P11	P50	Set to “0b”. TRDIOC1 is assigned to P11 as the IN5 output port for PWM waveform output.	2
39		PIOR23	TRDIOB1	P12	P30	Set to “0b”. TRDIOB1 is assigned to P12 as the IN4 output port for PWM waveform output.	2
40		PIOR22	TRDIOA1	P13	P16	Set to “0b”. TRDIOA1 is assigned to P13 as the IN3 output port for PWM waveform output.	2
41		PIOR21	VCOUT1	P31	P70	Set to “0b”. P70 is an unconnected port. Output control is set by PIOR32 bit.	4
42		PIOR20	VCOUT0	P120	P71	Set to “0b”. P71 is an unconnected port. Output control is set by PIOR31 bit.	4

Table 2-9 Recommended Settings for Peripheral I/O Redirection Register 3 (PIOR3) Note1

No.	Register Name	Bit Name	Function	Setting Value		Description	Note
				0b	1b		
43	PIOR3	PIOR32	VCOUT1	Output Disable	Output Enable	In the case of PIOR32 = 0b, VCOUT1 output is fixed to Low. Pin output is specified by PIOR21 bit.	4
44		PIOR31	VCOUT0	Output Disable	Output Enable	In the case of PIOR31 = 0b, VCOUT0 output is fixed to Low. Pin output is specified by PIOR20 bit.	4
45		PIOR30	-	-	-	Not available. Please set to “0b”.	2

Note1: Gray areas show unavailable features and settings.
Note2: These settings are required to use this product.
Note3: This setting is recommended when using nFAULT signal and comparator function of the smart gate driver.
Note4: This setting is not necessary if this function is not used.

2.2.2 Clock Generator

The following lists show the available and unavailable clocks. P121, P123, and P124 are unavailable ports, so the clocks from X1 port for the main system clock and XT1, XT2, and EXCLKS ports for the subsystem clocks that are assigned to P121, P123, or P124 are not available.

Available clocks

- f_{HOCO} (High-speed On-chip Oscillator Clock (Maximum 64MHz))
- f_{IH} (High-speed On-chip Oscillator Clock (Maximum 32MHz))
- f_{IL} (Low-speed On-chip Oscillator Clock)
- f_{EX} (External Main System Clock)
- f_{MX} (High-speed System Clock)
- f_{MAIN} (Main System Clock)
- f_{CLK} (CPU/Peripheral Hardware Clock)

Unavailable clocks

- f_X (X1 Clock)
- f_{XT} (XT1 Clock)
- f_{EXS} (External Subsystem Clock)
- f_{SUB} (Subsystem Clock)

2.2.3 Timer Array Unit

Table 2-10 lists the input/output ports of the Timer Array Unit. When timer input and timer output are assigned to the same pin, only either timer input or timer output can be used. Since P16 is an unconnected port, Channel 1 using the timer input/output port TI01/TO01 is not available.

Table 2-10 Input/Output Pins for Timer Array Unit Note1

Timer Array Unit		Port Functions	
Unit	**Channel**	**Available**	**Unavailable**
Unit0	Channel 0	TI00, TO00	-
	Channel 1	-	TI01/TO01
	Channel 2	TI02/TO02	-
	Channel 3	TI03/TO03	-

Note1: Gray areas show unavailable functions.

2.2.4 Timer RJ

Only CPU/peripheral hardware clocks “f_{CLK}, $f_{CLK}/8$, $f_{CLK}/2$”, low-speed on-chip oscillator clock “f_{IL}”, and event inputs from the ELC can be used as the count source. The subsystem clock “f_{SUB} (f_{XT}, f_{EXS})” cannot be used.
Timer RJ output port TRJO can only be assigned to P00. It cannot be assigned to P30 or P50.
Timer RJ input/output port TRJIO can only be assigned to P01, P31, and P41. It cannot be assigned to P06.

2.2.5 Timer RD

The PWM output ports of Timer RD are connected to each INz (z = 1, 2, 3, 4, 5, 6) terminal of the smart gate driver.
The input capture function is not available. For details of port functions and settings, refer to ***2.1.4.3***, ***2.2.1.1***.

2.2.6 Timer RG

Only the phase counting mode using TRGCLKA and TRGCLKB, and timer RG interrupt signal (INTTRG) can be used.
Since P50 and P51 are unconnected ports, the function using TRGIOA and TRGIOB in each mode are not available.

2.2.7 Real-time Clock

Only the constant-period interrupt function using the low-speed on-chip oscillator clock "f_{IL}" as the clock source can be used. The subsystem clock "f_{SUB} (f_{XT}, f_{EXS})" is not available.

2.2.8 12-bit Interval Timer

Only the low-speed on-chip oscillator clock "f_{IL}" can be used as the clock source. The subsystem clock "f_{SUB} (f_{XT}, f_{EXS})" is not available.

2.2.9 Clock Output / Buzzer Output Controller

Use f_{MAIN} as the clock source. The subsystem clock "f_{SUB} (f_{XT}, f_{EXS})" is not available.
P55 is an internal connection port for the smart gate driver, so when using the clock/buzzer output "PCLBUZ1", it should be assigned to P141. Clock/buzzer output "PCLBUZ0" can be assigned to P31 or P140.

2.2.10 Watchdog Timer

The watchdog timer has the restriction on usage due to the technical update of RL78/G1F. In the specific settings and conditions, after clearing the watchdog timer, the watchdog timer interval interrupt (INTWDTI) may be unintentionally generated after one clock of the watchdog timer elapses. In this case, the additional procedure to reset the watchdog timer counter is necessary as the workaround.
For details of this restriction, refer to ***"RL78/G1F Technical Update (TN-RL*-A086A/E)"***.

2.2.11 A/D Converter

Total 9 channels (ANI0 to ANI5, ANI16, ANI17, ANI19) can be used as analog input port for A/D conversion. However, since ANI5 is shared with the differential amplifier output terminal DA3O of the smart gate driver, a pull-down resistor (330kΩ) is connected to ANI5 when used as an external analog input port. This impedance must be considered when using this pin as an external analog input port.
ANI5 to ANI7 can be used for A/D conversion of the differential amplifier outputs DAzO (z = 1, 2, 3) of the smart gate driver.
ANI18 assigned to P147 and ANI20 to ANI24 assigned to P10 to P14 cannot be used due to limitations associated with the internal connected ports and unconnected ports.

2.2.12 Comparator (CMP)

P71 is an unconnected port, comparator output “VCOUT0” can only be assigned to P120.
P70 is an unconnected port, comparator output “VCOUT1” can only be assigned to P31.
P147 is an unconnected port, the comparator 0 reference voltage input “IVREF0” is not available.

2.2.13 Serial Array Unit

Table 2-11 shows the function assignment for each channel of the Serial Array Unit. 3-wire serial I/O (CSI00) is dedicated to internal communication with smart gate driver. 3-wire serial I/O (CSI11, CSI20, CSI21), UART communication (UART0, UART2), and simple I2C communication (IIC00, IIC 11, IIC20, IIC21) are not available due to limitations associated with internal connection ports and unconnected ports.

Table 2-11 Serial Array Unit Function Assignment for Each Channel Note1

Unit	Channel	Used as CSI	Used as UART	Used as simplified I2C
0	0	CSI00 (Not support slave select input function) Note2	UART0 (supporting LIN-bus) (Not available)	IIC00 (Not available)
	1	CSI01		IIC01
	2	CSI10	UART1	IIC10
	3	CSI11 (Not available)		IIC11 (Not available)
1	0	CSI20 (Not available)	UART2 (supporting IrDA) (Not available)	IIC20 (Not available)
	1	CSI21 (Not available)		IIC21 (Not available)

Note1: Gray areas show unavailable functions.
Note2: CSI00 is dedicated to internal communication.

2.2.14 IrDA

The IrDA sends and receives IrDA data communication waveforms in cooperation with UART2. Since UART2 is not available, IrDA also is not available.

2.2.15 Data Transfer Controller (DTC)

Table 2-12 lists the DTC activation sources and vector addresses. Due to limitations on the interrupt functions and the Serial Array Unit, DTC activation sources for unavailable functions are not available.

Table 2-12 DTC Activation Sources and Vector Addresses Note1

DTC Activation Source (Interrupt Request Source)	Source No.	Vector Address	Priority
Reserved	0	Address set in DTCBAR register + 00H	Highest
INTP0	1	Address set in DTCBAR register + 01H	
INTP1	2	Address set in DTCBAR register + 02H	
INTP2	3	Address set in DTCBAR register + 03H	
INTP3	4	Address set in DTCBAR register + 04H	
INTP4	5	Address set in DTCBAR register + 05H	
INTP5	6	Address set in DTCBAR register + 06H	
INTP6	7	Address set in DTCBAR register + 07H	
INTP7	8	Address set in DTCBAR register + 08H	
Key input	9	Address set in DTCBAR register + 09H	
A/D conversion end	10	Address set in DTCBAR register + 0AH	
CSI01 transfer end or buffer empty / IIC01 transfer end	11	Address set in DTCBAR register + 0BH	
UART0 reception transfer end			
CSI00 transfer end or buffer empty	12	Address set in DTCBAR register + 0CH	
UART0 transmission transfer end / IIC00 transfer end			
UART1 reception transfer end	13	Address set in DTCBAR register + 0DH	
CSI11 transfer end or buffer empty / IIC11 transfer end			
UART1 transmission transfer end / CSI10 transfer end or buffer empty / IIC10 transfer end	14	Address set in DTCBAR register + 0EH	
UART2 reception transfer end / CSI21 transfer end or buffer empty / IIC21 transfer end	15	Address set in DTCBAR register + 0FH	
UART2 transmission transfer end / CSI20 transfer end or buffer empty / IIC20 transfer end	16	Address set in DTCBAR register + 10H	
End of channel 0 of Timer Array Unit 0 count or capture	19	Address set in DTCBAR register + 13H	
End of channel 1 of Timer Array Unit 0 count	20	Address set in DTCBAR register + 14H	
End of channel 1 of Timer Array Unit 0 capture			
End of channel 2 of Timer Array Unit 0 count or capture	21	Address set in DTCBAR register + 15H	
End of channel 3 of Timer Array Unit 0 count or capture	22	Address set in DTCBAR register + 16H	
Timer RD compare match A0	27	Address set in DTCBAR register + 1BH	
Timer RD compare match B0	28	Address set in DTCBAR register + 1CH	
Timer RD compare match C0	29	Address set in DTCBAR register + 1DH	
Timer RD compare match D0	30	Address set in DTCBAR register + 1EH	
Timer RD compare match A1	31	Address set in DTCBAR register + 1FH	
Timer RD compare match B1	32	Address set in DTCBAR register + 20H	
Timer RD compare match C1	33	Address set in DTCBAR register + 21H	
Timer RD compare match D1	34	Address set in DTCBAR register + 22H	
Timer RG compare match A	35	Address set in DTCBAR register + 23H	
Timer RG compare match B	36	Address set in DTCBAR register + 24H	
Timer RJ0 underflow	37	Address set in DTCBAR register + 25H	
Comparator detection 0	38	Address set in DTCBAR register + 26H	
Comparator detection 1	39	Address set in DTCBAR register + 27H	Lowest

Note1: Gray areas show unavailable DTC activation sources.

2.2.16 Event Link Controller (ELC)

Table 2-13 shows the correspondence between the event output destination select register (ELSELRn) (n = 00 to 21) and peripheral functions. Due to limitations on the interrupt functions, the Timer RD, and the Timer Array Unit, event signals for unavailable functions are not available.

Table 2-13 Correspondence Between ELSELRn (n = 00 to 21) Register and Peripheral Functions Note1

Register	Event Generator (Output Origin of Event Input n)	Event Description
ELSELR00	External interrupt edge detection 0	INTP0
ELSELR01	External interrupt edge detection 1	INTP1
ELSELR02	External interrupt edge detection 2	INTP2
ELSELR03	External interrupt edge detection 3	INTP3
ELSELR04	External interrupt edge detection 4	INTP4
ELSELR05	External interrupt edge detection 5	INTP5
ELSELR06	Key return signal detection	INTKR
ELSELR07	RTC fixed-cycle signal / Alarm match detection	INTRTC
ELSELR08	Timer RD0 compare match A	INTTRD0
	Timer RD0 input capture A	
ELSELR09	Timer RD0 compare match B	INTTRD0
	Timer RD0 input capture B	
ELSELR10	Timer RD1 compare match A	INTTRD1
	Timer RD1 input capture A	
ELSELR11	Timer RD1 compare match B	INTTRD1
	Timer RD1 input capture B	
ELSELR12	Timer RD1 underflow	TRD1 underflow signal
ELSELR13	Timer RJ0 underflow / End of pulse width measurement period / End of pulse period measurement period	INTTRJ0
ELSELR14	Timer RG input capture A / compare match A	INTTRG
ELSELR15	Timer RG input capture B / compare match B	INTTRG
ELSELR16	TAU channel 00 count end /capture end	INTTM00
ELSELR17	TAU channel 01 count end	INTTM01
	TAU channel 01 capture end	
ELSELR18	TAU channel 02 count end / capture end	INTTM02
ELSELR19	TAU channel 03 count end / capture end	INTTM03
ELSELR20	Comparator detection 0	Comparator detection 0 signal
ELSELR21	Comparator detection 1	Comparator detection 1 signal

Note1: Gray areas show unavailable event signals.

2.2.17 Interrupt Functions

Due to limitations on the port connections, the Serial Array Unit, the Timer Array Unit, and the Timer RD, the interrupt sources for unavailable functions are not available. ***Table 2-14*** and ***Table 2-15*** show the interrupt source list including unavailable sources. ***Table 2-16*** shows the relation between port input interrupt sources and port connections. For available port functions, refer to ***2.2.1.1***.

Table 2-14 Interrupt Source List (1/2) Note1

Interrupt Type	Default Priority Note2	Interrupt Source		Int./ Ext.	Vector Table Address
		Name	Trigger		
Maskable	0	INTWDTI	Watchdog Timer interval (75% of overflow + 1/2 fIL) Note3	Int.	00004H
	1	INTLVI	Voltage detection Note4		00006H
	2	INTP0	Pin input edge detection	Ext.	00008H
	3	INTP1			0000AH
	4	INTP2			0000CH
	5	INTP3			0000EH
	6	INTP4			00010H
	7	INTP5	Pin input edge detection		00012H
	8	INTST2/ INTCSI20/ INTIIC20	UART2 transmission transfer end or buffer empty interrupt / CSI20 transfer end or buffer empty interrupt / IIC20 transfer end	Int.	00014H
	9	INTSR2/ INTCSI21/ INTIIC21	UART2 reception transfer end / CSI21 transfer end or buffer empty interrupt / IIC21 transfer end		00016H
	10	INTSRE2	UART2 reception communication error occurrence		00018H
	11	INTCSI00	CSI00 transfer end or buffer empty interrupt		0001EH
		INTST0/ INTIIC00	UART0 reception transfer end or buffer empty interrupt / IIC00 transfer end		
	12	INTCSI01/ INTIIC01	CSI01 transfer end or buffer empty interrupt / IIC01 transfer end		00020H
		INTSR0	UART0 reception transfer end		
	13	INTTM01H	Timer channel 01 count end / capture end (for upper 8-bit timer operation)		00022H
		INTSRE0	UART0 reception communication error occurrence		
	14	INTST1/ INTCSI10/ INTIIC10	UART1 transmission transfer end or buffer empty interrupt / CSI10 transfer end or buffer empty interrupt / IIC10 transfer end		00024H
	15	INTSR1	UART1 reception transfer end		00026H
		INTCSI11/ INTIIC11	CSI11 transfer end or buffer empty interrupt / IIC11 transfer end		
	16	INTSRE1	UART1 reception communication error occurrence		00028H
		INTTM03H	Timer channel 03 count end or capture end (for upper 8-bit timer operation)		
	17	INTIICA0	IICA0 communication end		0002AH

Note1: Gray areas show unavailable interrupt sources.
Note2: The default priority determines the sequence of interrupts if two or more maskable interrupts occur simultaneously. 0 indicates the highest priority and 37 indicates the lowest priority.
Note3: When bit 7 (WDTINT) of the option byte (000C0H) is set to 1.
Note4: When bit 7 (LVIMD) of the voltage detection level register (LVIS) is cleared to 0.

Table 2-15 Interrupt Source List (2/2) Note1

Interrupt Type	Default Priority Note2	Interrupt Source		Int./ Ext.	Vector Table Address
		Name	Trigger		
	18	INTTM00	Timer channel 00 count end / capture end	Int.	0002CH
	19	INTTM01	Timer channel 01 count end		0002EH
			Timer channel 01 capture end		
	20	INTTM02	Timer channel 02 count end / capture end		00030H
	21	INTTM03	Timer channel 03 count end / capture end		00032H
	22	INTAD	A/D conversion end		00034H
	23	INTRTC	Fixed-cycle signal of real-time clock / alarm match detection		00036H
	24	INTIT	Interval signal detection		00038H
	25	INTKR	Key return signal detection	Ext.	0003AH
	26	INTTRJ0	Timer RJ interrupt	Int.	00040H
	27	INTP6	Pin input edge detection	Ext.	0004AH
	28	INTP7			0004CH
	29	INTP8			0004EH
	30	INTP9			00050H
	31	INTP10	Pin input edge detection	Ext.	00052H
		INTCMP0	Comparator detection 0	Int.	
	32	INTP11	Pin input edge detection	Ext.	00052H
		INTCMP1	Comparator detection 1	Int.	
	33	INTTRD0	Timer RD0 compare match, overflow, underflow interrupt	Int.	00056H
			Timer RD0 input capture		
	34	INTTRD1	Timer RD1 compare match, overflow, underflow interrupt		00058H
			Timer RD1 input capture		
	35	INTTRG	Timer RG input capture, compare match, overflow, underflow interrupt		0005AH
	36	INTTRX	Timer RX overflow detection		0005CH
	37	INTFL	Reserved Note5		00062H
ソフトウェア	—	BRK	Execution of BRK instruction	—	0007EH
リセット	—	RESET	$\overline{\text{RESET}}$ pin input	—	00000H
		POR	Power-on-reset		
		LVD	Voltage detection Note6		
		WDT	Watchdog timer overflow		
		TRAP	Illegal instruction execution Note7		
		IAW	Illegal memory access		
		RPE	RAM parity error		

Note1: Gray areas show unavailable interrupt sources.
Note2: The default priority determines the sequence of interrupts if two or more maskable interrupts occur simultaneously. 0 indicates the highest priority and 37 indicates the lowest priority.
Note5: Used at the flash self-programming library or the data flash library.
Note6: When bit 7 (LVIMD) of the voltage detection level register (LVIS) is set to 1.
Note7: When the instruction code in FFH is executed. Reset by the illegal instruction execution not issued by emulation with the in-circuit emulator or on-chip debug emulator.

Table 2-16 Relation between Port Input Interrupt Sources and Port Connections

Name	External connection ports	Internal connection ports	Unavailable ports for interrupt
INTP0	P137	-	–
INTP1	–	P52	P50
INTP2	–	P53	P51
INTP3	–	P54	P30
INTP4	–	P55	P31
INTP5	–	–	P12, P16
INTP6	P140	–	–
INTP7	P141	–	–
INTP8	P00, P42	–	P74
INTP9	P43	–	P75
INTP10	P01, P76	–	P05
INTP11	P20, P77	–	–
INTKR	P73, P74, P75, P76, P77	-	P70, P71, P72

2.2.18 Key Interrupt Function

Only the key interrupt ports (KR3 to KR7) are available. Key interrupt ports (KR0 to KR2) are not available due to unconnected ports. Be sure to set KRM0 to KRM2 bits on the key return mode register (KRM) to 0.

2.2.19 Power-on-reset Circuit

The operating voltage range of the MCU is limited to the recommended operating voltage range of the VDD pin (VDD = 3.135 to 5.25V). The operation mode and detection voltage (V_{LVDH}, V_{LVDL}, V_{LVD}) for the voltage detector (LVD) should be set appropriately according to the VDD pin voltage and the application.

2.2.20 Voltage Detector

The operating voltage range of the MCU is limited to the recommended operating voltage range of the VDD pin (VDD = 3.135 to 5.25V). The operation mode and detection voltages (V_{LVDH}, V_{LVDL}, V_{LVD}) for the voltage detector (LVD) should be set appropriately according to the VDD pin voltage and the application.

2.2.21 Option Bytes

There are no restrictions on the functions of the option bytes, but the operation modes and detection voltages (V_{LVDH}, V_{LVDL}, V_{LVD}) for the voltage detector (LVD) should be set in consideration of the limitations on the recommended operating voltage range of the VDD pin (VDD = 3.135 to 5.25V).

2.2.22 Flash Memory

The dedicated flash memory programmer can be used to perform write/erase operations by serial communication using the TOOL0 pin via a dedicated single-line UART of the MCU. Serial programming using external device (that incorporates UART) is not available because P50 (TOOLRxD) and P51 (TOOLTxD) for serial communication via dedicated UART of the MCU are internally connected ports.

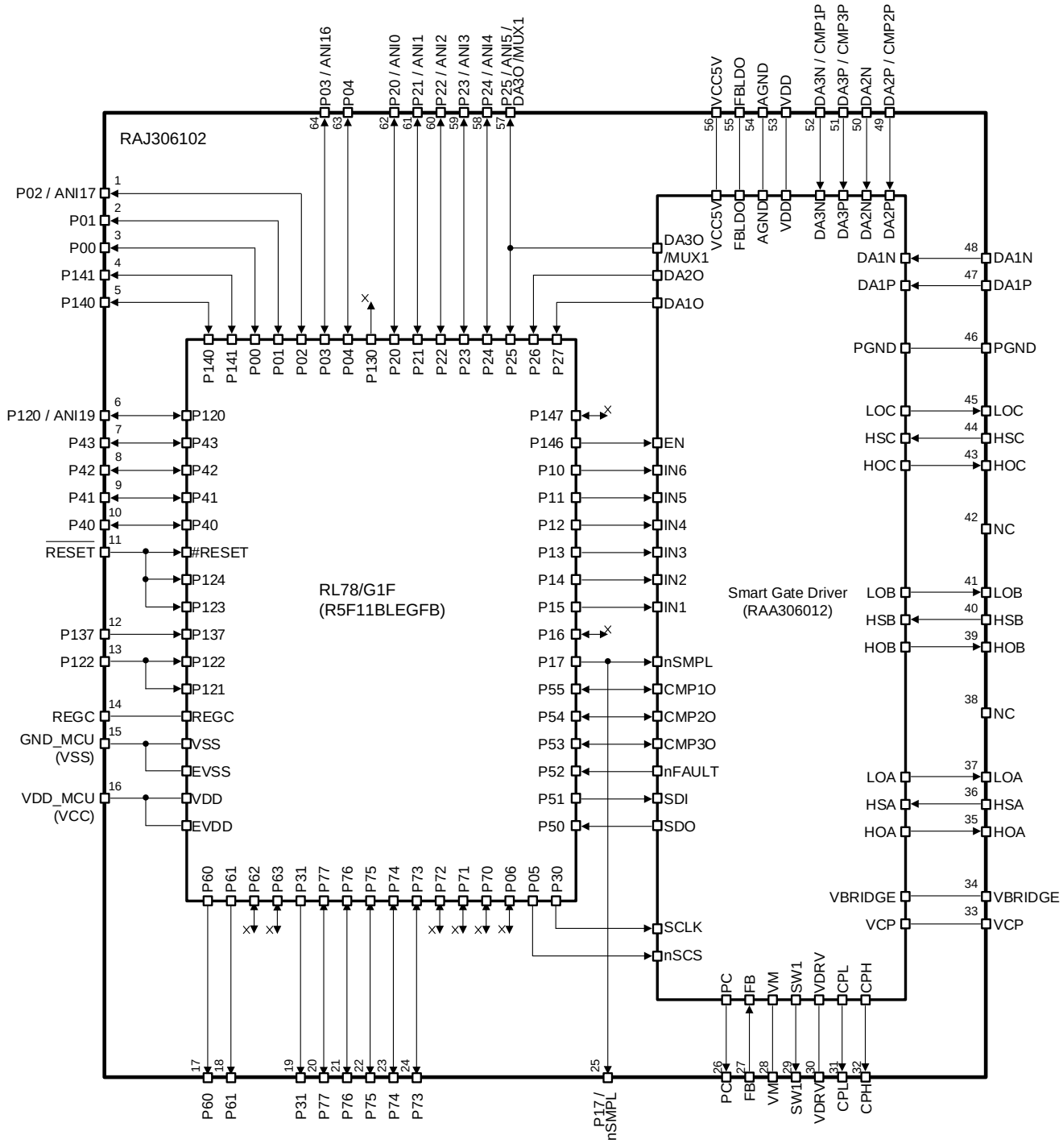
Chapter 3 Smart Gate Driver

This device integrates RAA306012 as a smart gate driver.
The smart gate driver includes three half-bridge gate drivers, a buck switching regulator and a charge pump for the gate drive voltage, two LDOs for the internal analog and logic circuitry and MCU, three accurate differential amplifiers, a BEMF sense amplifier, three general purpose comparators, and extensive protection functions.
The three half-bridge gate drivers are capable of driving up to three N-channel MOSFET bridges and support bridge voltages from 6V to 65V. Each gate driver supports up to 0.64A source and 1.28A sink peak drive current with adjustable drive strength control. Adaptive and adjustable dead-times are implemented to ensure robustness and flexibility. The active gate holding mechanism prevents miller effect induced cross-conduction and further enhances robustness.
Three accurate differential amplifiers with adjustable gain support ground-side shunt current sensing for each bridge. The device can also support both BLDC sensor/sensorless motor drive by the three general purpose comparators or a BEMF sense amplifier.
The protection functions include supply voltage undervoltage/overvoltage (VM_UV/VM_OV), buck regulator undervoltage/undervoltage/overcurrent protection (VDRV_UV/VDRV_OV/SR_OCP), charge pump undervoltage (VCP_UV), MOSFET VDS overcurrent protection (VDS_OCP), shunt current sense overcurrent protection (CS_OCP), MOSFET VGS fault (VGS_FAULT), thermal warning (TWARN), and thermal shutdown (OTSD).
The smart gate driver can be configured to use SPI interface by the internal connection with MCU. All the parameters can be set through the SPI interface and allows better monitoring. Fault conditions are reported on the nFAULT signal and each status bit in the Fault Status registers.
To properly control the smart gate driver, it is important to use not only the control signals from the MCU, but also the external circuit configuration and register settings for each application. This chapter describes the precautions about the register settings, and external circuit configuration for each application.
For details on the smart gate driver, refer to the ***"RAA306012 Datasheet (R18DS0037EJ)"***.

3.1 Terminal Connections and Functions

3.1.1 Terminal Connections with MCU and Pins

Figure 3-1 shows the connection diagram between the smart gate driver terminals, RL78/G1F ports, and pins. “x” is unconnected ports.



X: Unconnected ports

Figure 3-1 Connection Diagram between the Smart Gate Driver Terminals, RL78/G1F Ports, and Pins

3.1.2 Terminal Functions

Table 3-1 and ***Table 3-2*** show the terminal functions of the smart gate driver.
For the internal connection ports with smart gate driver terminals, it is important to set the other port settings before setting the EN output port to High because the control by signals other than the EN signal is enabled. For details on port settings procedures, refer to the notes in this table, ***2.1*** and ***Chapter 4***.

Table 3-1 Terminal Functions of the Smart Gate Driver (1/2)

Ext. Pin Number	Smart Gate Driver Terminal	I/O				RL78/G1F Port	Function	Note
		Level	Type	Initial (EN=Low)	Enable Control			
-	DA1O	VDD	OUT	330kΩ, pulldown	DA1_EN bit	P27/ANI7	Output of differential amplifier 1 Pull-down resistor is disabled when differential amplifier 1 is enabled.	
-	CMP3O	VDD	IN/OUT	OUT/380kΩ, pulldown	BEMF_PH/ CMP3_VTH bits	P53/INPT2	Control input for the detect phase selection of BEMF sense amplifier. Output of comparator 3. The pin function is selected by BEMF_PH bits.	1
-	CMP2O	VDD	IN/OUT	OUT/380kΩ, pulldown	BEMF_PH/ CMP2_VTH bits	P54/INTP3	Control input for the detect phase selection of BEMF sense amplifier. Output of comparator 2. The pin function is selected by BEMF_PH bits.	1
-	CMP1O	VDD	IN/OUT	OUT/380kΩ, pulldown	BEMF_PH/ CMP1_VTH bits	P55/INTP4	Control input for the detect phase selection of BEMF sense amplifier. Output of comparator 1. The pin function is selected by BEMF_PH bits.	1
-	EN	VDD	IN	100kΩ, pulldown	-	P146	Enable control pin for Operation Mode. When this pin is logic low, the device goes to a low-power sleep mode.	1, 2
-	IN6	VDD	IN	380kΩ, pulldown	EN signal	P10/TRDIOD1	Gate driver control input 6. The control input for each phase gate driver is selectable by the register setting.	2
-	IN5	VDD	IN	380kΩ, pulldown	EN signal	P11/TRDIOC1	Gate driver control input 5. The control input for each phase gate driver is selectable by the register setting.	2
-	IN4	VDD	IN	380kΩ, pulldown	EN signal	P12/TRDIOB1	Gate driver control input 4. The control input for each phase gate driver is selectable by the register setting.	2
-	IN3	VDD	IN	380kΩ, pulldown	EN signal	P13/TRDIOA1	Gate driver control input 3. The control input for each phase gate driver is selectable by the register setting.	2
-	IN2	VDD	IN	380kΩ, pulldown	EN signal	P14/TRDIOD0	Gate driver control input 2. The control input for each phase gate driver is selectable by the register setting.	2
-	IN1	VDD	IN	380kΩ, pulldown	EN signal	P15/TRDIOB0	Gate driver control input 1. The control input for each phase gate driver is selectable by the register setting.	2
-	nFAULT	VDD	Open drain OUT	Hi-Z	EN signal	P52//INTP1	Fault indicator output The pull-up resistor option of MCU or external pull-up resistor is required.	3
25	nSMPL	VDD	IN	380kΩ, pulldown	DAz_SH (z = 1, 2, 3) / BEMF_SH bit	P17	Sampling control input of BEMF sense amplifier or differential amplifiers.	4
-	nSCS	VDD	IN	380kΩ, pullup	EN signal	P05	SPI chip select input	5
-	SCLK	VDD	IN	380kΩ, pulldown	EN signal	P30/SCK00	SPI clock input	5
-	SDI	VDD	IN	380kΩ, pulldown	EN signal	P51/SO00	SPI data input	5
-	SDO	VDD	Open drain OUT	Hi-Z	EN signal	P50/SI00	SPI data output The pull-up resistor option of MCU or external pull-up resistor is required.	3, 5
26	PC	VCC	OUT	1kΩ, pulldown	EN signal	-	gm amplifier output for phase compensation of buck switching regulator. When the switching regulator is enabled, the pull-down resistor is disabled.	
27	FB	VCC	IN	-	EN signal	-	Voltage feedback input of buck switching regulator (Ref = 0.8V)	
28	VM	VM	POWER	-	-	-	Power supply input. Connect bypass a capacitors between VM and AGND.	
29	SW1	VM	OUT	Hi-Z	EN signal	-	Switch Node of buck switching regulator	
30	VDRV	VDRV	POWER	-	EN signal	-	Output of buck switching regulator, Low-side gate driver supply Connect to bypass capacitors between VDRV and AGND.	
31	CPL	VDRV	OUT	100kΩ, pulldown	EN signal	-	Charge pump low-side switch node. Connect a flying capacitor between CPH and CPL pins.	
32	CPH	VCP	OUT	Hi-Z	EN signal	-	Charge pump high-side switch node. Connect a flying capacitor between CPH and CPL pins.	

Note1: To avoid the collision by output signals of the MCU and smart gate driver, set the MCU ports to the digital input port before setting the EN output port to Low.
Note2: To avoid unexpected gate drive output, set the INz (z = 1, 2, 3, 4, 5, 6) output ports to Low before setting EN output port to High or recovering from an abnormal condition. For details, refer to the smart gate driver control sequence in ***Chapter 4***.
Note3: After the MCU reset is released, enable the pull-up resistor option by the port setting of the MCU.
Note4: When using P17 (nSMPL) as an external connection pin of the MCU, set all BEMF_SH and DAz_SH (z = 1, 2, 3) bits to “0b”.
Note5: SPI communication is enabled after setting the EN terminal to High.

Table 3-2 Terminal Functions of the Smart Gate Driver (2/2)

Ext. Pin Number	Smart Gate Driver Terminal	I/O				RL78/G1F Port	Function	Note
		Level	Type	Initial (EN=Low)	Enable Control			
33	VCP	VCP	POWER	-	EN signal	-	Charge pump output. Connect a bypass capacitor between VCP and VBRIDGE pins.	
34	VBRIDGE	VBRIDGE	IN	-	EN signal	-	Charge pump output reference and high-side MOSFET drain sense Input. Connect a bypass capacitor between VBRIDGE pin and power ground.	
35	HOA	VCP	OUT	200kΩ, pulldown to HSA	EN signal	-	Phase A high-side gate driver output. Connect to the high-side MOSFET gate.	6
36	HSA	VBRIDGE	IN	300kΩ, pulldown	EN signal	-	Phase A high-side source sense input. Connect to the high-side MOSFET source.	
37	LOA	VDRV	OUT	200kΩ, pulldown to EPAD	EN signal	-	Phase A low-side gate driver output. Connect to the low-side MOSFET gate.	6
38	NC	-	-	-	-	-	Phase B high-side gate driver output. Connect to the high-side MOSFET gate.	
39	HOB	VCP	OUT	200kΩ, pulldown to HSA	EN signal	-	Phase B high-side source sense input. Connect to the high-side MOSFET source.	6
40	HSB	VBRIDGE	IN	300kΩ, pulldown	EN signal	-	Phase B low-side gate driver output. Connect to the low-side MOSFET gate.	
41	LOB	VDRV	OUT	200kΩ, pulldown to EPAD	EN signal	-	Phase C high-side gate driver output. Connect to the high-side MOSFET gate.	6
42	NC	-	-	-	-	-	Phase C high-side source sense input. Connect to the high-side MOSFET source.	
43	HOC	VCP	OUT	200kΩ, pulldown to HSA	EN signal	-	Phase C low-side gate driver output. Connect to the low-side MOSFET gate.	6
44	HSC	VBRIDGE	IN	300kΩ, pulldown	EN signal	-	Ground sense input of external power stage.	
45	LOC	VDRV	OUT	200kΩ, pulldown to EPAD	EN signal	-	Positive input of differential amplifier 1. When the all functions input from this pin are not used, connect to AGND.	6
46	PGND	GND	GND	-	-	-	Negative input of differential amplifier 1. When the all functions input from this pin are not used, connect to AGND.	
47	DA1P	VDD	IN	-	DA1_EN/ DIS_CS1OCP bit	-	Positive input of differential amplifier 2 and positive input of comparator 2. When the all functions input from this pin are not used, connect to AGND.	
48	DA1N	VDD	IN	-	DA1_EN/ DIS_CS1OCP bit	-	Negative input of differential amplifier 2. When the all functions input from this pin are not used, connect to AGND.	
49	DA2P	VDD	IN	-	DA2_EN/ DIS_CS2OCP/ CMP2_VTH bit	-	Positive input of differential amplifier 3 and positive input of comparator 3. When the all functions input from this pin are not used, connect to AGND.	
50	DA2N	VDD	IN	-	DA2_EN/ DIS_CS2OCP bit	-	Negative input of differential amplifier 3 and positive input of comparator 1. When the all functions input from this pin are not used, connect to AGND.	
51	DA3P	VDD	IN	-	DA3_EN/ DIS_CS3OCP/ CMP3_VTH bit	-	Internal series regulator output and power supply of output buffers. Connect to a bypass capacitor between VDD and AGND.	
52	DA3N	VDD	IN	-	DA3_EN/ DIS_CS3OCP/ CMP1_VTH bit	-	Device analog ground.	
53	VDD	VDD	POWER	-	-	-	Voltage feedback input of internal series regulator (Ref.=1.2V).	7
54	AGND	GND	GND	-	-	-	Internal series regulator output(5V). Connect to a bypass capacitor between VCC and AGND.	
55	FBLDO	VCC	IN	-	-	-	Output of differential amplifier 3, BEMF sense amplifier, and multiplexer. When MUX[2:0] is the setting other than 000b, the pull-down resistor is disabled.	
56	VCC5V	VCC	POWER	-	-	-	Output of differential amplifier 2. When the differential amplifier 2 is enabled, the pull-downresistor is disabled.	7
57	DA3O	VDD	OUT	330kΩ, pulldown	MUX bits	P25/ANI5	Power ground for gate driver and charge pump. Must be connected to power ground.	8
-	DA2O	VDD	OUT	330kΩ, pulldown	DA2_EN bit	P26/ANI6	Output of Differential Amplifier 2 When the differential amplifier 2 is enable, the pulldown resistance is cut off.	
-	EPAD (Thermal PAD)	GND	GND	-	-	-	Power Ground for Gate Driver and Charge Pump. Must be connect to Power Ground.	

Note6: Although pull-down resistors are integrated between the HOx - HSx (x = A, B, C) pins and between the LOx (x = A, B, C) - EPAD, external pull-down resistors are required depending on the slew rate of the external MOSFETs power supply.

Note7: The capability of VDD and VCC5V load current depends on the EN terminal and the operation mode. For recommended operating conditions, refer to ***5.3*** in the ***"RAJ306102 Datasheet (R18DS0039EJ)"***.

Note8: When using the external output pin as the MCU ADC input pin, a pull-down resistor (330kΩ) should be considered.

3.2 Control Register

The smart gate driver has built-in Control Registers for checking fault status, enabling/disabling fault detections and function blocks, adjusting gate driver switching characteristics, setting operation mode and gain settings, etc. of sense block. SPI communication and register settings are enabled after setting the EN terminal to High. However, it is recommended that the register settings of the smart gate driver be executed after the smart gate driver mode enters Operating Mode. All registers are reset when the smart gate driver mode enters Sleep Mode or Shutdown Mode, so it is necessary to set each register again after entering Operating Mode.
Figure 3-2 shows SPI communication format. ***Table 3-3*** shows the Control Register map. For the SPI communication port settings of the MCU, refer to ***2.1.4.2***.

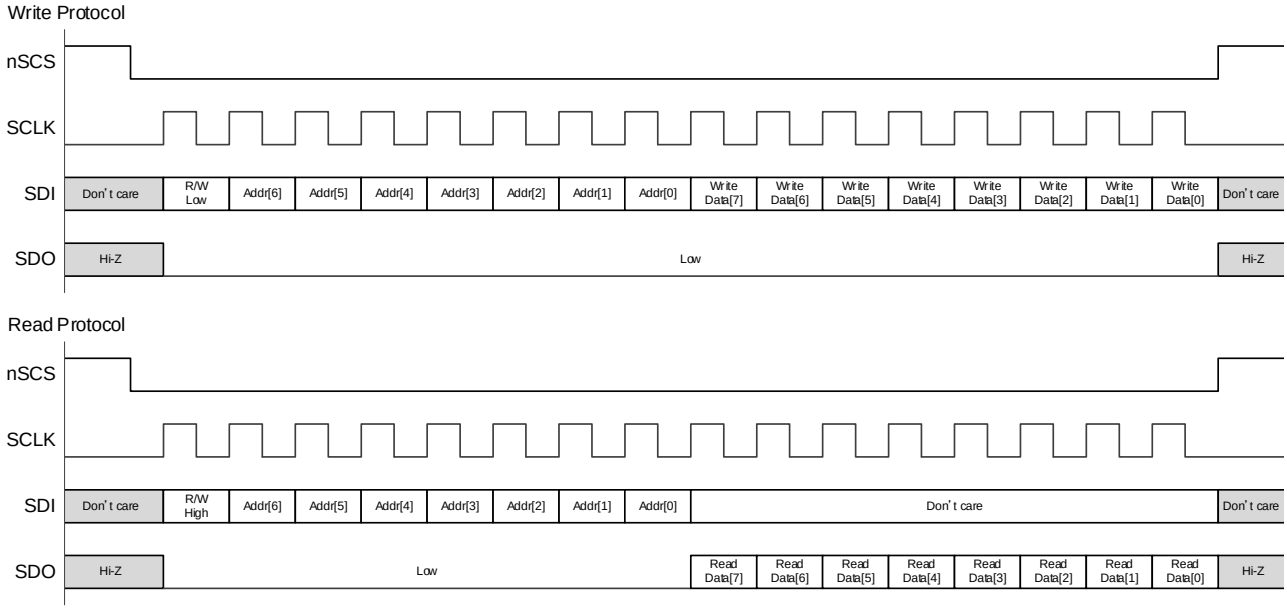


Figure 3-2 SPI Communication Format

Table 3-3 Control Register Map

Address	Register Name	Symbol	Access Type	Initial value	7	6	5	4	3	2	1	0
0x00	Fault Status 0	FLTSTS0	R	00h	FAULT	SR_FAULT	OV_UVLO	VDS_OCP	VGS_FAULT	CS_OCP	OTSD	TWARN
0x01	Fault Status 1	FLTSTS1	R	00h	VDRV_UV	VDRV_OV	SR_OCP	VCP_UV	VM_UV	VM_OV	N/A	N/A
0x02	Fault Status 2	FLTSTS2	R	00h	VDSHA_OCP	VDSLA_OCP	VGSHA_FAULT	VGSLA_FAULT	VDSHB_OCP	VDSLB_OCP	VGSHB_FAULT	VGSLB_FAULT
0x03	Fault Status 3	FLTSTS3	R	00h	VDSHC_OCP	VDSLC_OCP	VGSHC_FAULT	VGSLC_FAULT	N/A	CS1_OCP	CS2_OCP	CS3_OCP
0x04	Fault Control 1	FLTCTL1	R/W	00h	DIS_VDRVUV	DIS_VDRVOV	DIS_SROC	DIS_VCPUV	DIS_VMUV	DIS_VMOV	DIS_OTSD	TWARN_REP
0x05	Fault Control 2	FLTCTL2	R/W	07h	CSOCP_MODE1	CSOCP_MODE0	VDSOCP_MODE1	VDSOCP_MODE0	DIS_VGSFLT	DIS_CS1OCP	DIS_CS2OCP	DIS_CS3OCP
0x06	IC Control 1	ICCTL1	R/W	35h	CLR_FLT	WRITE_LOCK2	WRITE_LOCK1	WRITE_LOCK0	PWMMODE	CSOCP_TH2	CSOCP_TH1	CSOCP_TH0
0x07	IC Control 2	ICCTL2	R/W	50h	DEAD_TIME1	DEAD_TIME0	T_GT1	T_GT0	BEMF_EN	DA1_EN	DA2_EN	DA3_EN
0x08	Gate Driver Control	GDCTL	R/W	FFh	ISRC_HS3	ISRC_HS2	ISRC_HS1	ISRC_HS0	ISRC_LS3	ISRC_LS2	ISRC_LS1	ISRC_LS0
0x09	Over Current Protection Control	OCPCTL	R/W	00h	VDS_TH3	VDS_TH2	VDS_TH1	VDS_TH0	TRETRY_CSOCP	TRETRY_VDSOCP	DEG_TIME1	DEG_TIME0
0x0A	Phase-A Gate Driver Input Selection	GDSELA	R/W	14h	CMP1_HYS	HOA_SEL2	HOA_SEL1	HOA_SEL0	VMUV_TH	LOA_SEL2	LOA_SEL1	LOA_SEL0
0x0B	Phase-B Gate Driver Input Selection	GDSELB	R/W	25h	CMP2_HYS	HOB_SEL2	HOB_SEL1	HOB_SEL0	PDMODE	LOB_SEL2	LOB_SEL1	LOB_SEL0
0x0C	Phase-C Gate Driver Input Selection	GDSELC	R/W	36h	CMP3_HYS	HOC_SEL2	HOC_SEL1	HOC_SEL0	CPUV_TH	LOC_SEL2	LOC_SEL1	LOC_SEL0
0x0D	Sense Block Control 1	SNSCTL1	R/W	AAh	BEMF_GAIN1	BEMF_GAIN0	DA1_GAIN1	DA1_GAIN0	DA2_GAIN1	DA2_GAIN0	DA3_GAIN1	DA3_GAIN0
0x0E	Sense Block Control 2	SNSCTL2	R/W	00h	CAL_BCONN	BEMF_PH2	BEMF_PH1	BEMF_PH0	BEMF_SH	DA1_SH	DA2_SH	DA3_SH
0x0F	Sense Block Control 3	SNSCTL3	R/W	88h	CMP1_VTH3	CMP1_VTH2	CMP1_VTH1	CMP1_VTH0	CMP2_VTH3	CMP2_VTH2	CMP2_VTH1	CMP2_VTH0
0x10	Sense Block Control 4	SNSCTL4	R/W	80h	CMP3_VTH3	CMP3_VTH2	CMP3_VTH1	CMP3_VTH0	CAL_CONN	CAL_DA1	CAL_DA2	CAL_DA3/BEMF
0x11	Sense Block Control 5	SNSCTL5	R/W	00h	DIS_SADT	RESERVED11_6	CTL6_UNLOCK	RESERVED11_4	RESERVED11_3	MUX2	MUX1	MUX0
0x12	Sense Block Control 6	SNSCTL6	R/W	40h	RESERVED12_7	BEMF_OFFSET	RESERVED12_5	RESERVED12_4	RESERVED12_3	RESERVED12_2	RESERVED12_1	GD_AOR

3.2.1 Register Description

3.2.1.1 Fault Status 0 Register: FLTSTS0 (Address = 0x00) [Default = 0x00]

Table 3-4 and ***Table 3-5*** show the details of Fault Status 0 register.

Table 3-4 Fault Status 0 Register FLTSTS0

7	6	5	4	3	2	1	0
FAULT	SR_FAULT	OV_UVLO	VDS_OCP	VGS_FAULT	CS_OCP	OTSD	TWARN
R: 0b	R: 0b	R: 0b	R: 0b	R: 0b	R: 0b	R: 0b	R: 0b

Table 3-5 Fault Status 0 Register FLTSTS0 Description Note1

Bit	Field	Type	Default	Description
7	FAULT	R	0b	Logic OR of all Fault Status bits
6	SR_FAULT	R	0b	Logic OR of the Fault Status bits for buck switching regulator: VDRV_UV, VDRV_OV, SR_OCP
5	OV_UVLO	R	0b	Logic OR of the Fault Status bits for undervoltage and overvoltage: VCP_UV, VM_UV, VM_OV
4	VDS_OCP	R	0b	Logic OR of the Fault Status bits for V_{DS} overcurrent: VDSHx_OCP, VDSLx_OCP
3	VGS_FAULT	R	0b	Logic OR of the Fault Status bits for V_{GS} fault : VGSHx_FAULT, VGSLx_FAULT
2	CS_OCP	R	0b	Logic OR of the Fault Status bits for current sense overcurrent: CS1_OCP, CS2_OCP, CS3_OCP
1	OTSD	R	0b	Indicator of thermal shutdown
0	TWARN	R	0b	Indicator of thermal warning

Note1: Fault Status registers are reset by writing 1b to CLR_FLT of ICCTL1 register, or recovery low pulse (> tsleep: 0.85ms) on EN pin.

3.2.1.2 Fault Status 1 Register: FLTSTS1 (Address = 0x01) [Default = 0x00]

Table 3-6 and ***Table 3-7*** show the details of Fault Status 1 register.

Table 3-6 Fault Status 1 Register FLTSTS1

7	6	5	4	3	2	1	0
VDRV_UV	VDRV_OV	SR_OCP	VCP_UV	VM_UV	VM_OV	N/A	N/A
R: 0b	R: 0b	R: 0b	R: 0b	R: 0b	R: 0b	R: 0b	R: 0b

Table 3-7 Fault Status 1 Register FLTSTS1 Description Note1

Bit	Field	Type	Default	Description
7	VDRV_UV	R	0b	Indicator of VDRV undervoltage (V_{DRVUV})
6	VDRV_OV	R	0b	Indicator of VDRV overvoltage (V_{DRVOV})
5	SR_OCP	R	0b	Indicator of buck switching regulator overcurrent (I_{OC2_SR})
4	VCP_UV	R	0b	Indicator of VCP undervoltage (V_{CPUV})
3	VM_UV	R	0b	Indicator of VM undervoltage (V_{VMUV})
2	VM_OV	R	0b	Indicator of VM overvoltage (V_{VMOV})
1	N/A	R	0b	Not assigned
0	N/A	R	0b	Not assigned

Note1: Fault Status registers are reset by writing 1b to CLR_FLT of ICCTL1 register, or recovery low pulse (> tsleep: 0.85ms) on EN pin.

3.2.1.3 Fault Status 2 Register: FLTSTS2 (Address = 0x02) [Default = 0x00]

Table 3-8 and ***Table 3-9*** show the details of Fault Status 2 register.

Table 3-8 Fault Status 2 Register FLTSTS2

7	6	5	4	3	2	1	0
VDSHA_OCP	VDSLA_OCP	VGSHA_FAULT	VGSLA_FAULT	VDSHB_OCP	VDSLB_OCP	VGSHB_FAULT	VGSLB_FAULT
R: 0b	R: 0b	R: 0b	R: 0b	R: 0b	R: 0b	R: 0b	R: 0b

Table 3-9 Fault Status 2 Register FLTSTS2 Description Note1

Bit	Field	Type	Default	Description
7	VDSHA_OCP	R	0b	Indicator of V_{DS} overcurrent on Phase-A high-side MOSFET
6	VDSLA_OCP	R	0b	Indicator of V_{DS} overcurrent on Phase-A low-side MOSFET
5	VGSHA_FAULT	R	0b	Indicator of V_{GS} fault on Phase-A high-side MOSFET
4	VGSLA_FAULT	R	0b	Indicator of V_{GS} fault on Phase-A low-side MOSFET
3	VDSHB_OCP	R	0b	Indicator of V_{DS} overcurrent on Phase-B high-side MOSFET
2	VDSLB_OCP	R	0b	Indicator of V_{DS} overcurrent on Phase-B low-side MOSFET
1	VGSHB_FAULT	R	0b	Indicator of V_{GS} fault on Phase-B high-side MOSFET
0	VGSLB_FAULT	R	0b	Indicator of V_{GS} fault on Phase-B low-side MOSFET

Note1: Fault Status registers are reset by writing 1b to CLR_FLT of ICCTL1 register, or recovery low pulse (> tsleep: 0.85ms) on EN pin.

3.2.1.4 Fault Status 3 Register: FLTSTS3 (Address = 0x03) [Default = 0x00]

Table 3-10 and ***Table 3-11*** show the details of Fault Status 3 register.

Table 3-10 Fault Status 3 Register FLTSTS3

7	6	5	4	3	2	1	0
VDSHC_OCP	VDSLC_OCP	VGSHC_FAULT	VGSLC_FAULT	N/A	CS1_OCP	CS2_OCP	CS3_OCP
R: 0b	R: 0b	R: 0b	R: 0b	R: 0b	R: 0b	R: 0b	R: 0b

Table 3-11 Fault Status 3 Register FLTSTS3 Description Note1

Bit	Field	Type	Default	Description
7	VDSHC_OCP	R	0b	Indicator of V_{DS} overcurrent on Phase-C high-side MOSFET
6	VDSLC_OCP	R	0b	Indicator of V_{DS} overcurrent on Phase-C low-side MOSFET
5	VGSHC_FAULT	R	0b	Indicator of V_{GS} fault on Phase-C high-side MOSFET
4	VGSLC_FAULT	R	0b	Indicator of V_{GS} fault on Phase-C low-side MOSFET
3	N/A	R	0b	Not assigned
2	CS1_OCP	R	0b	Indicator of current sense overcurrent by DA1P, DA1N inputs
1	CS2_OCP	R	0b	Indicator of current sense overcurrent by DA2P, DA2N inputs
0	CS3_OCP	R	0b	Indicator of current sense overcurrent by DA3P, DA3N inputs

Note1: Fault Status registers are reset by writing 1b to CLR_FLT of ICCTL1 register, or recovery low pulse (> tsleep: 0.85ms) on EN pin.

3.2.1.5 Fault Control 1 Register: FLTCTL1 (Address = 0x04) [Default = 0x00]

Table 3-12 and ***Table 3-13*** show the details of Fault Control 1 register.

Table 3-12 Fault Control 1 Register FLTCTL1

7	6	5	4	3	2	1	0
DIS_VDRVUV	DIS_VDRVOV	DIS_SROC	DIS_VCPUV	DIS_VMUV	DIS_VMOV	DIS_OTSD	TWARN_REP
R/W: 0b	R/W: 0b	R/W: 0b	R/W: 0b	R/W: 0b	R/W: 0b	R/W: 0b	R/W: 0b

Table 3-13 Fault Control 1 Register FLTCTL1 Description

Bit	Field	Type	Default	Description
7	DIS_VDRVUV	R/W	0b	Write 1b to report status only for VDRV undervoltage (V_{DRVUV}) detection
6	DIS_VDRVOV	R/W	0b	Write 1b to report status only for VDRV overvoltage (V_{DRVOV}) detection
5	DIS_SROC	R/W	0b	Write 1b to report status only for buck switching regulator overcurrent (I_{OC2_SR}) protection
4	DIS_VCPUV	R/W	0b	Write 1b to report status only for VCP undervoltage (V_{CPUV}) detection
3	DIS_VMUV	R/W	0b	Write 1b to report status only for VM undervoltage (V_{VMUV}) detection
2	DIS_VMOV	R/W	0b	Write 1b to report status only for VM overvoltage fault (V_{VMOV}) detection
1	DIS_OTSD	R/W	0b	Write 1b to report status only for thermal shutdown
0	TWARN_REP	R/W	0b	0b: Thermal warning is reported on only TWARN bit. 1b: Thermal warning is reported on nFAULT pin, FAULT bit and TWARN bit.

3.2.1.6 Fault Control 2 Register: FLTCTL2 (Address = 0x05) [Default = 0x07]

Table 3-14 and ***Table 3-15*** show the details of Fault Control 2 register.

Table 3-14 Fault Control 2 Register FLTCTL2

7	6	5	4	3	2	1	0
CSOCP_MODE1	CSOCP_MODE0	VDSOCP_MODE1	VDSOCP_MODE0	DIS_VGSFLT	DIS_CS1OCP	DIS_CS2OCP	DIS_CS3OCP
R/W: 0b	R/W: 0b	R/W: 0b	R/W: 0b	R/W: 0b	R/W: 1b	R/W: 1b	R/W: 1b

Table 3-15 Fault Control 2 Register FLTCTL2 Description

Bit	Field	Type	Default	Description
7	CSOCP_MODE1	R/W	0b	Response mode for current sense overcurrent 00b: Latch upon current sense overcurrent [Note2] 01b: Automatic retry upon current sense overcurrent 10b: Report on nFAULT pin, FAULT, CS_OCP and CS1/2/3_OCP bits only. No action takes place. 11b: Disable. No report and no action takes place.
6	CSOCP_MODE0	R/W	0b	
5	VDSOCP_MODE1	R/W	0b	Response mode for V_{DS} overcurrent 00b: Latch upon V_{DS} overcurrent [Note2] 01b: Automatic retry upon V_{DS} overcurrent 10b: Report on nFAULT pin, FAULT, VDS_OCP, VDSHx_OCP and VDSLx_OCP bits only. No action takes place. 11b: Disable, No report and no action takes place
4	VDSOCP_MODE0	R/W	0b	
3	DIS_VGSFLT	R/W	0b	Write 1b to disable V_{GS} fault detection
2	DIS_CS1OCP	R/W	1b	Write 1b to disable current sense overcurrent by DA1P, DA1N inputs
1	DIS_CS2OCP	R/W	1b	Write 1b to disable current sense overcurrent by DA2P, DA2N inputs
0	DIS_CS3OCP	R/W	1b	Write 1b to disable current sense overcurrent by DA3P, DA3N inputs

Note2: Latch is recovered by writing 1b to CLR_FLT of ICCTL1 register, or recovery low pulse (> tsleep: 0.85ms) on EN pin.

3.2.1.7 IC Control 1 Register: ICCTL1 (Address = 0x06) [Default = 0x35]

Table 3-16 and ***Table 3-17*** show the details of IC Control 1 register.

Table 3-16 IC Control 1 Register ICCTL1

7	6	5	4	3	2	1	0
CLR_FLT	WRITE_LOCK2	WRITE_LOCK1	WRITE_LOCK0	PWMMODE	CSOCP_TH2	CSOCP_TH1	CSOCP_TH0
R/W: 0b	R/W: 0b	R/W: 1b	R/W: 1b	R/W: 0b	R/W: 1b	R/W: 0b	R/W: 1b

Table 3-17 IC Control 1 Register ICCTL1 Description

Bit	Field	Type	Default	Description
7	CLR_FLT	R/W	0b	Write 1b to clear the all flagged fault status bits. This bit is reset to 0b automatically.
6	WRITE_LOCK2	R/W	0b	Write 110b to ignore all further register write except WRITE_LOCK[2:0]. Write 011b to unlock to allow register write. Writing other values takes no effect.
5	WRITE_LOCK1	R/W	1b	
4	WRITE_LOCK0	R/W	1b	
3	PWMMODE	R/W	0b	0b: 3-Phase HI/LI mode, 1b: 3-Phase PWM mode
2	CSOCP_TH2	R/W	1b	Threshold voltage setting of current sense overcurrent by DAzP, DAzN (z=1,2,3) inputs 000b: 51mV, 001b: 105mV, 010b: 157mV, 011b: 208mV, 100b: 260mV, 101b: 516mV, 110b: 773mV, 111b: 1029mV
1	CSOCP_TH1	R/W	0b	
0	CSOCP_TH0	R/W	1b	

3.2.1.8 IC Control 2 Register: ICCTL2 (Address = 0x07) [Default = 0x50]

Table 3-18 and ***Table 3-19*** show the details of IC Control 2 register.

Table 3-18 IC Control 2 Register ICCTL2

7	6	5	4	3	2	1	0
DEAD_TIME1	DEAD_TIME0	T_GT1	T_GT0	BEMF_EN	DA1_EN	DA2_EN	DA3_EN
R/W: 0b	R/W: 1b	R/W: 0b	R/W: 1b	R/W: 0b	R/W: 0b	R/W: 0b	R/W: 0b

Table 3-19 IC Control 2 Register Description

Bit	Field	Type	Default	Description
7	DEAD_TIME1	R/W	0b	Dead time from V_{GS} voltage monitor output to start timing of another-side turn on 00b: 50ns, 01b: 100ns, 10b: 200ns, 11b: 400ns
6	DEAD_TIME0	R/W	1b	
5	T_GT1	R/W	0b	Maximum gate transition time 00b: 500ns, 01b: 1000ns, 10b: 2000ns, 11b: 4000ns
4	T_GT0	R/W	1b	
3	BEMF_EN	R/W	0b	Write 1b to enable BEMF sense amplifier.
2	DA1_EN	R/W	0b	Write 1b to enable differential amplifier 1.
1	DA2_EN	R/W	0b	Write 1b to enable differential amplifier 2.
0	DA3_EN	R/W	0b	Write 1b to enable differential amplifier 3.

3.2.1.9 Gate Drive Control Register: GDCTL (Address = 0x08) [Default = 0xFF]

Table 3-20 and ***Table 3-21*** show the details of Gate Drive Control register.

Table 3-20 Gate Control Register GDCTL

7	6	5	4	3	2	1	0
ISRC_HS3	ISRC_HS2	ISRC_HS1	ISRC_HS0	ISRC_LS3	ISRC_LS2	ISRC_LS1	ISRC_LS0
R/W: 1b	R/W: 1b	R/W: 1b	R/W: 1b	R/W: 1b	R/W: 1b	R/W: 1b	R/W: 1b

Table 3-21 Gate Control Register GDCTL Description

Bit	Field	Type	Default	Description
7	ISRC_HS3	R/W	1b	High-side gate driver output source current. Sink current is 2*(source current). 0000b: 50mA, 0001b: 60mA, 0010b: 70mA, 0011b: 80mA, 0100b: 100mA, 0101b: 120mA, 0110b: 140mA, 0111b: 160mA, 1000b: 200mA, 1001b: 240mA, 1010b: 280mA, 1011b: 320mA, 1100b: 400mA, 1101b: 480mA, 1110b: 560mA, 1111b: 640mA
6	ISRC_HS2	R/W	1b	
5	ISRC_HS1	R/W	1b	
4	ISRC_HS0	R/W	1b	
3	ISRC_LS3	R/W	1b	Low-side gate driver output source current. Sink current is 2*(source current). 0000b: 50mA, 0001b: 60mA, 0010b: 70mA, 0011b: 80mA, 0100b: 100mA, 0101b: 120mA, 0110b: 140mA, 0111b: 160mA, 1000b: 200mA, 1001b: 240mA, 1010b: 280mA, 1011b: 320mA, 1100b: 400mA, 1101b: 480mA, 1110b: 560mA, 1111b: 640mA
2	ISRC_LS2	R/W	1b	
1	ISRC_LS1	R/W	1b	
0	ISRC_LS0	R/W	1b	

3.2.1.10 Overcurrent Protection Control Register: OCPCTL (Address = 0x09) [Default = 0x00]

Table 3-22 and ***Table 3-23*** show the details of Overcurrent Protection Control register.

Table 3-22 Overcurrent Protection Control Register OCPCTL

7	6	5	4	3	2	1	0
VDS_TH3	VDS_TH2	VDS_TH1	VDS_TH0	TRETRY_CSOCP	TRETRY_VDSOCP	DEG_TIME1	DEG_TIME0
R/W: 0b	R/W: 0b	R/W: 0b	R/W: 0b	R/W: 0b	R/W: 0b	R/W: 0b	R/W: 0b

Table 3-23 Overcurrent Protection Control Register OCPCTL Description

Bit	Field	Type	Default	Description
7	VDS_TH3	R/W	0b	Threshold voltage setting of V_{DS} overcurrent fault 0000b: 40mV, 0001b: 60mV, 0010b: 80mV, 0011b: 120mV, 0100b: 160mV, 0101b: 200mV, 0110b: 240mV, 0111b: 320mV, 1000b: 400mV, 1001b: 480mV, 1010b: 600mV, 1011b: 720mV, 1100b: 960mV, 1101b: 1200mV, 1110b: 1600mV, 1111b: 2000mV
6	VDS_TH2	R/W	0b	
5	VDS_TH1	R/W	0b	
4	VDS_TH0	R/W	0b	
3	TRETRY_CSOCP	R/W	0b	Retry time for current sense overcurrent fault with CSOCP_MODE=01b, 0b: 4000µs, 1b: 70µs
2	TRETRY_VDSOCP	R/W	0b	Retry time for V_{DS} overcurrent fault with VDSOCP_MODE=01b, 0b: 4000µs, 1b: 70µs
1	DEG_TIME1	R/W	0b	Deglitch time for both current sense and V_{DS} overcurrent fault 00b: 1.57µs, 01b: 2.38µs, 10b: 3.49µs, 11b: 5.73µs
0	DEG_TIME0	R/W	0b	

3.2.1.11 Phase-A Gate Driver Input Selection Register: GDSELA (Address = 0x0A) [Default = 0x14]

Table 3-24 and ***Table 3-25*** show the details of Phase-A Gate Driver Input Selection register.

Table 3-24 Phase-A Gate Driver Input Selection Register GDSELA

7	6	5	4	3	2	1	0
CMP1_HYS	HOA_SEL2	HOA_SEL1	HOA_SEL0	VMUV_TH	LOA_SEL2	LOA_SEL1	LOA_SEL0
R/W: 0b	R/W: 0b	R/W: 0b	R/W: 1b	R/W: 0b	R/W: 1b	R/W: 0b	R/W: 0b

Table 3-25 Phase-A Gate Driver Input Selection Register GDSELA Description

Bit	Field	Type	Default	Description
7	CMP1_HYS	R/W	0b	Comparator 1 hysteresis setting, 0b: +/-44mV, 1b: 0mV
6	HOA_SEL2	R/W	0b	Input selection for Phase-A high-side gate driver Note3 000b: Low fix, 001b: IN1, 010b: IN2, 011b: IN3, 100b: IN4, 101b: IN5, 110b: IN6, 111b: Hi-Z
5	HOA_SEL1	R/W	0b	
4	HOA_SEL0	R/W	1b	
3	VMUV_TH	R/W	0b	VM under voltage threshold setting, 0b: 5.3V, 1b: 7.5V
2	LOA_SEL2	R/W	1b	Input selection for Phase-A low-side gate driver Note3 000b: Low fix, 001b: IN1, 010b: IN2, 011b: IN3, 100b: IN4, 101b: IN5, 110b: IN6, 111b: Hi-Z
1	LOA_SEL1	R/W	0b	
0	LOA_SEL0	R/W	0b	

Note3: When HOx_SEL or LOx_SEL bits set to 111b, the source/sink current of gate driver becomes off (Hi-Z).

3.2.1.12 Phase-B Gate Driver Input Selection Register: GDSELB (Address = 0x0B) [Default = 0x25]

Table 3-26 and ***Table 3-27*** show the details of Phase-B Gate Driver Input Selection register.

Table 3-26 Phase-B Gate Driver Input Selection Register GDSELB

7	6	5	4	3	2	1	0
CMP2_HYS	HOB_SEL2	HOB_SEL1	HOB_SEL0	PDMODE	LOB_SEL2	LOB_SEL1	LOB_SEL0
R/W: 0b	R/W: 0b	R/W: 1b	R/W: 0b	R/W: 0b	R/W: 1b	R/W: 0b	R/W: 1b

Table 3-27 Phase-B Gate Driver Input Selection Register GDSELB Description

Bit	Field	Type	Default	Description
7	CMP2_HYS	R/W	0b	Comparator 2 hysteresis setting, 0b: +/-44mV, 1b: 0mV
6	HOB_SEL2	R/W	0b	Input selection for Phase-B high-side gate driver Note3 000b: Low fix, 001b: IN1, 010b: IN2, 011b: IN3, 100b: IN4, 101b: IN5, 110b: IN6, 111b: Hi-Z
5	HOB_SEL1	R/W	1b	
4	HOB_SEL0	R/W	0b	
3	PDMODE	R/W	0b	Gate driver pulldown mode after VDS_OCP, CS_OCP, 0b: Hi-Z pulldown, 1b: driver output low
2	LOB_SEL2	R/W	1b	Input selection for Phase-B low-side gate driver Note3 000b: Low fix, 001b: IN1, 010b: IN2, 011b: IN3, 100b: IN4, 101b: IN5, 110b: IN6, 111b: Hi-Z
1	LOB_SEL1	R/W	0b	
0	LOB_SEL0	R/W	1b	

Note3: When HOx_SEL or LOx_SEL bits set to 111b, the source/sink current of gate driver becomes off (Hi-Z).

3.2.1.13 Phase-C Gate Driver Input Selection Register: GDSELC (Address = 0x0Ch) [Default = 0x36]

Table 3-28 and ***Table 3-29*** show the details of Phase-C Gate Driver Input Selection register.

Table 3-28 Phase-C Gate Driver Input Selection Register GDSELC

7	6	5	4	3	2	1	0
CMP3_HYS	HOC_SEL2	HOC_SEL1	HOC_SEL0	CPUV_TH	LOC_SEL2	LOC_SEL1	LOC_SEL0
R/W: 0b	R/W: 0b	R/W: 1b	R/W: 1b	R/W: 0b	R/W: 1b	R/W: 1b	R/W: 0b

Table 3-29 Phase-C Gate Driver Input Selection Register GDSELC Description

Bit	Field	Type	Default	Description
7	CMP3_HYS	R/W	0b	Comparator 3 hysteresis setting, 0b: +/-44mV, 1b: 0mV
6	HOC_SEL2	R/W	0b	Input selection for Phase-C high-side gate driver Note3 000b: Low fix, 001b: IN1, 010b: IN2, 011b: IN3, 100b: IN4, 101b: IN5, 110b: IN6, 111b: Hi-Z
5	HOC_SEL1	R/W	1b	
4	HOC_SEL0	R/W	1b	
3	CPUV_TH	R/W	0b	VCP under voltage threshold setting, 0b: 0.58*VDRV, 1b: 0.8*VDRV
2	LOC_SEL2	R/W	1b	Input selection for Phase-C low-side gate driver Note3 000b: Low fix, 001b: IN1, 010b: IN2, 011b: IN3, 100b: IN4, 101b: IN5, 110b: IN6, 111b: Hi-Z
1	LOC_SEL1	R/W	1b	
0	LOC_SEL0	R/W	0b	

Note3: When HOx_SEL or LOx_SEL bits set to 111b, the source/sink current of gate driver becomes off (Hi-Z).

3.2.1.14 Sense Block Control 1 Register: SNSCTL1 (Address = 0x0D) [Default = 0xAA]

Table 3-30 and ***Table 3-31*** show the details of Sense Block Control 1 register.

Table 3-30 Sense Block Control 1 Register SNSCTL1

7	6	5	4	3	2	1	0
BEMF_GAIN1	BEMF_GAIN0	DA1_GAIN1	DA1_GAIN0	DA2_GAIN1	DA2_GAIN0	DA3_GAIN1	DA3_GAIN0
R/W: 1b	R/W: 0b	R/W: 1b	R/W: 0b	R/W: 1b	R/W: 0b	R/W: 1b	R/W: 0b

Table 3-31 Sense Block Control 1 Register SNSCTL1 Description

Bit	Field	Type	Default	Description
7	BEMF_GAIN1	R/W	1b	Gain setting of BEMF sense amplifier with DA3_GAIN=00b 00b: 0.05V/V, 01b: 0.1V/V, 10b: 0.5V/V, 11b: 1.0V/V
6	BEMF_GAIN0	R/W	0b	
5	DA1_GAIN1	R/W	1b	Gain setting of differential amplifier 1 00b: 5V/V, 01b: 10V/V, 10b: 20V/V, 11b: 40V/V
4	DA1_GAIN0	R/W	0b	
3	DA2_GAIN1	R/W	1b	Gain setting of differential amplifier 2 00b: 5V/V, 01b: 10V/V, 10b: 20V/V, 11b: 40V/V
2	DA2_GAIN0	R/W	0b	
1	DA3_GAIN1	R/W	1b	Gain setting of differential amplifier 3 00b: 5V/V, 01b: 10V/V, 10b: 20V/V, 11b: 40V/V
0	DA3_GAIN0	R/W	0b	

3.2.1.15 Sense Block Control 2 Register: SNSCTL2 (Address = 0x0E) [Default = 0x00]

Table 3-32 and ***Table 3-33*** show the details of Sense Block Control 2 register.

Table 3-32 Sense Block Control 2 Register SNSCTL2

7	6	5	4	3	2	1	0
CAL_BCONN	BEMF_PH2	BEMF_PH1	BEMF_PH0	BEMF_SH	DA1_SH	DA2_SH	DA3_SH
R/W: 0b	R/W: 0b	R/W: 0b	R/W: 0b	R/W: 0b	R/W: 0b	R/W: 0b	R/W: 0b

Table 3-33 Sense Block Control 2 Register SNSCTL2 Description

Bit	Field	Type	Default	Description
7	CAL_BCONN	R/W	0b	Input selection of BEMF sense amplifier during BEMF offset calibration 0b: The amplifier inputs are connected to the reference voltage of BEMF sense amplifier (DAREF) 1b: The amplifier inputs are connected to the phase selected by BEMF_PH bits
6	BEMF_PH2	R/W	0b	Detect phase selection of BEMF sense amplifier Note4 00xb: Select automatically from the input signals of the gate driver at every nSMPL falling edge 010b: Select by CMP1O and CMP2O pins (CMP1O, CMP2O)= (0,0): No selection, (0,1): Phase-A, (1,0): Phase-B, (1,1): Phase-C 011b: Select by CMP1O and CMP3O pins (CMP1O, CMP3O)= (0,0): No selection, (0,1): Phase-A, (1,0): Phase-B, (1,1): Phase-C 100b: No selection, 101b: Phase-A, 110b: Phase-B, 111b: Phase-C
5	BEMF_PH1	R/W	0b	
4	BEMF_PH0	R/W	0b	
3	BEMF_SH	R/W	0b	S/H control setting of BEMF sense amplifier Note4 0b: keep sampling, 1b: sampling during nSMPL signal=Low & PWM ON after tGT
2	DA1_SH	R/W	0b	S/H control setting of differential amplifier 1 Note4 0b: keep sampling, 1b: sampling during nSMPL signal=Low
1	DA2_SH	R/W	0b	S/H control setting of differential amplifier 2 Note4 0b: keep sampling, 1b: sampling during nSMPL signal=Low
0	DA3_SH	R/W	0b	S/H control setting of differential amplifier 3 Note4 0b: keep sampling, 1b: sampling during nSMPL signal=Low

Note4: Refer to ***6.5.2***, ***6.5.3*** of ***"RAJ306102 Datasheet (R18DS0039EJ)"***.

3.2.1.16 Sense Block Control 3 Register: SNSCTL3 (Address = 0x0F) [Default = 0x88]

Table 3-35 and ***Table 3-36*** show the details of Sense Block Control 3 register.

Table 3-34 Sense Block Control 3 Register SNSCTL3

7	6	5	4	3	2	1	0
CMP1_VTH3	CMP1_VTH2	CMP1_VTH1	CMP1_VTH0	CMP2_VTH3	CMP2_VTH2	CMP2_VTH1	CMP2_VTH0
R/W: 1b	R/W: 0b	R/W: 0b	R/W: 0b	R/W: 1b	R/W: 0b	R/W: 0b	R/W: 0b

Table 3-35 Sense Block Control 3 Register SNSCTL3 Description

Bit	Field	Type	Default	Description
7	CMP1_VTH3	R/W	1b	Threshold voltage setting of Comparator 1 0000b: Disable, 0001b to 1111b: Threshold voltage= VDD /16 x CMP1_VTH
6	CMP1_VTH2	R/W	0b	
5	CMP1_VTH1	R/W	0b	
4	CMP1_VTH0	R/W	0b	
3	CMP2_VTH3	R/W	1b	Threshold voltage setting of Comparator 2 0000b: Disable, 0001b to 1111b: Threshold voltage= VDD /16 x CMP2_VTH
2	CMP2_VTH2	R/W	0b	
1	CMP2_VTH1	R/W	0b	
0	CMP2_VTH0	R/W	0b	

3.2.1.17 Sense Block Control 4 Register: SNSCTL4 (Address = 0x10) [Default = 0x80]

Table 3-36 and ***Table 3-37*** show the details of Sense Block Control 4 register.

Table 3-36 Sense Block Control 4 Register SNSCTL4

7	6	5	4	3	2	1	0
CMP3_VTH3	CMP3_VTH2	CMP3_VTH1	CMP3_VTH0	CAL_CONN	CAL_DA1	CAL_DA2	CAL_DA3/BEMF
R/W: 1b	R/W: 0b	R/W: 0b	R/W: 0b	R/W: 0b	R/W: 0b	R/W: 0b	R/W: 0b

Table 3-37 Sense Block Control 4 Register SNSCTL4 Description

Bit	Field	Type	Default	Description
7	CMP3_VTH3	R/W	1b	Threshold voltage setting of Comparator 3 0000b: Disable, 0001b to 1111b: Threshold voltage= VDD /16 x CMP3_VTH
6	CMP3_VTH2	R/W	0b	
5	CMP3_VTH1	R/W	0b	
4	CMP3_VTH0	R/W	0b	
3	CAL_CONN	R/W	0b	Input selection of differential amplifier during DC offset calibration 0b: The amplifier inputs are connected to GND. 1b: The amplifier inputs are connected to the external shunt.
2	CAL_DA1	R/W	0b	Write 1b to enable DC offset calibration for differential amplifier 1. This bit is automatically reset to 0 after calibration is done.
1	CAL_DA2	R/W	0b	Write 1b to enable DC offset calibration for differential amplifier 2. This bit is automatically reset to 0 after calibration is done.
0	CAL_DA3/BEMF	R/W	0b	Write 1b to this bit to enable DC offset calibration for differential amplifier 3 if BEMF sensing is disabled (BEMF_EN=0b). Write 1b to this bit to enable DC offset calibration for BEMF sensing amplifiers if BEMF sensing is enabled (BEMF_EN=1b). This bit automatically resets to 0 after calibration is done

3.2.1.18 Sense Block Control 5 Register: SNSCTL5 (Address = 0x11) [Default = 0x00]

Table 3-38 and ***Table 3-39*** show the details of Sense Block Control 5 register.

Table 3-38 Sense Block Control 5 Register SNSCTL5

7	6	5	4	3	2	1	0
DIS_SADT	RESERVED11_6	CTL6_UNLOCK	RESERVED11_4	RESERVED11_3	MUX2	MUX1	MUX0
R/W: 0b	R/W: 0b	R/W: 0b	R/W: 0b	R/W: 0b	R/W: 0b	R/W: 0b	R/W: 0b

Table 3-39 Sense Block Control 5 Register SNSCTL5 Description

Bit	Field	Type	Default	Description
7	DIS_SADT	R/W	0b	Write 1b to disable the adaptive dead time control function
6	RESERVED11_6	R/W	0b	Reserved. The write value should be 0b.
5	CTL6_UNLOCK	R/W	0b	Write 0b to ignore SNSCTL6 register write. Write 1b to unlock to allow SNSCTL6 register write.
4	RESERVED11_4	R/W	0b	Reserved. The write value should be 0b.
3	RESERVED11_3	R/W	0b	Reserved. The write value should be 0b.
2	MUX2	R/W	0b	Output selection of DA3O/MUX1 pin 000b: GND (pulldown: 330kΩ) 001b: VM monitor 010b: TEMP monitor 011b: Differential amplifier reference voltage 101b: Differential amplifier 1 output 110b: Differential amplifier 2 output In case of BEMF_EN=0b, 100b: Differential amplifier 3 output w/ 10kΩ 111b: Differential amplifier 3 output w/o 10kΩ In case of BEMF_EN=1b, 100b: BEMF sense amplifier output w/ 10kΩ 111b: BEMF sense amplifier output w/o 10kΩ
1	MUX1	R/W	0b	
0	MUX0	R/W	0b	

3.2.1.19 Sense Block Control 6 Register: SNSCTL6 (Address = 0x12) [Default = 0x40h]

Table 3-40 and ***Table 3-41*** show the details of Sense Block Control 6 register. CTL6_UNLOCK=1b is necessary to allow SNSCTL6 register write. After writing SNSCTL6 register, CTL6_UNLOCK should be set to 0b.

Table 3-40 Sense Block Control 6 Register SNSCTL6

7	6	5	4	3	2	1	0
RESERVED12_7	BEMF_OFFSET	RESERVED12_5	RESERVED12_4	RESERVED12_3	RESERVED12_2	RESERVED12_1	GD_AOR
R/W: 0b	R/W: 1b	R/W: 0b	R/W: 0b	R/W: 0b	R/W: 0b	R/W: 0b	R/W: 0b

Table 3-41 Sense Block Control 6 Register SNSCTL6 Description

Bit	Field	Type	Default	Description
7	RESERVED12_7	R/W	0b	Reserved. The write value should be 0b.
6	BEMF_OFFSET	R/W	1b	Data selection of BEMF sense amplifier DC offset 0b: calibration data, 1b: trimming data by shipping test This bit automatically sets to 0 after DC offset calibration for BEMF sense amplifier is done.
5	RESERVED12_5	R/W	0b	Reserved. The write value should be 0b.
4	RESERVED12_4	R/W	0b	Reserved. The write value should be 0b.
3	RESERVED12_3	R/W	0b	Reserved. The write value should be 0b.
2	RESERVED12_2	R/W	0b	Reserved. The write value should be 0b.
1	RESERVED12_1	R/W	0b	Reserved. The write value should be 0b.
0	GD_AOR	R/W	0b	Write 1b to enable the active override mode of the gate driver logic.

3.3 Register Settings for Motor Control

RAJ306102 incorporates various sense blocks to control BLDC motors. The optimal motor control for each application can be realized by using these function blocks. This section describes the circuit configuration and register settings for hall sensor motor drive and sensorless motor drive as examples.

3.3.1 Hall Sensor Motor Drive

3.3.1.1 Circuit Diagram

Figure 3-3 shows an example of a simplified application block diagram and application for hall sensor motor drive by using 3 comparators.

In Hall sensor motor drive, the motor is controlled by switching the energized phase according to the position detection signal from the Hall IC. The polarity of the position detection signals can be determined by using general purpose comparators and is input to the CMPzP (z = 1, 2, 3) pins.

When detecting the motor drive current by a shunt resistor or using current sense overcurrent function (CS_OCP), input the differential voltage across the shunt resistor to the DA1P and DA1N pins. The unused pins on the DAzP and DAzN (z = 1, 2, 3) pins should be connected to AGND.

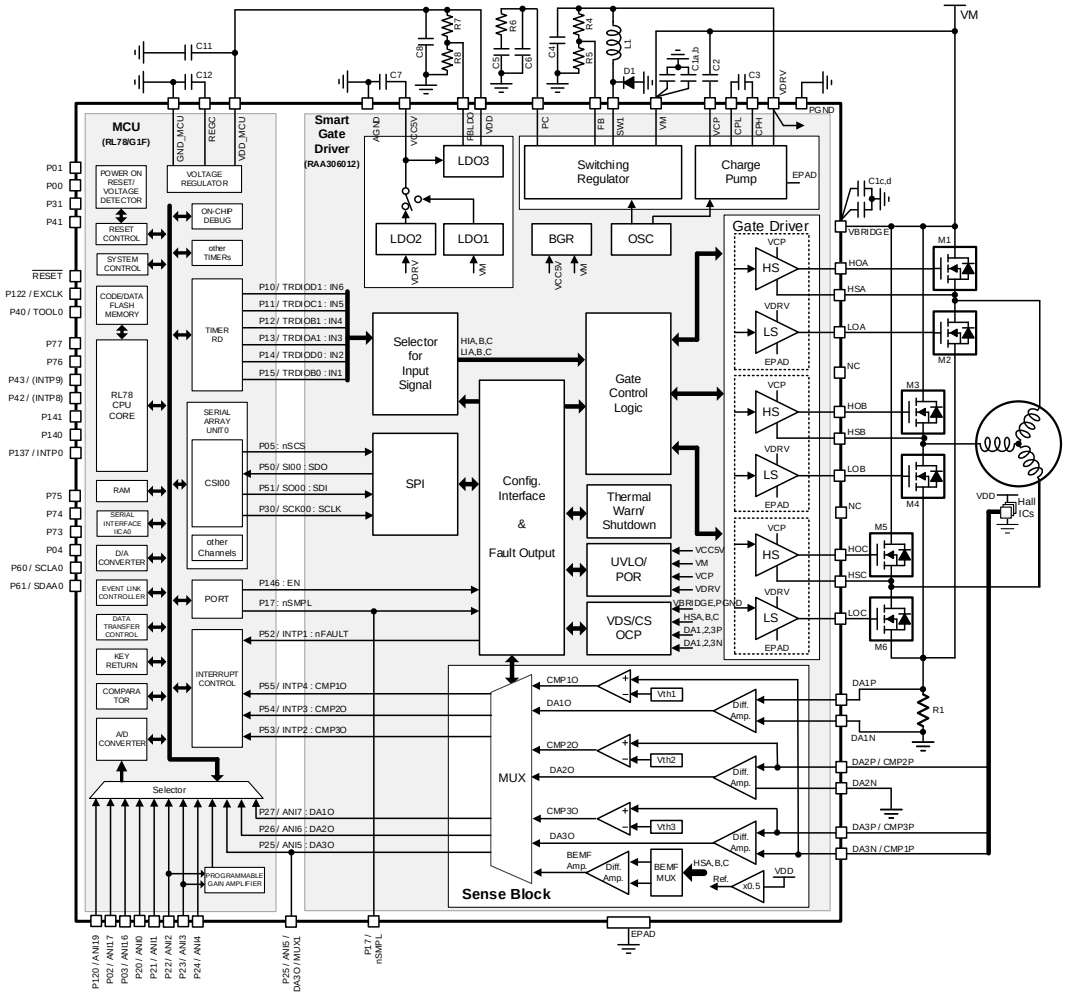


Figure 3-3 **Simplified Application Block Diagram – Hall Sensor Motor Drive by Using 3 Comparators**

3.3.1.2 Register Setting

This device requires register settings for various functions of the smart gate driver before motor control. The following four types of register settings are required for each function.
(a) Fault detection function: enable/disable, response mode, adjustment bits, and Fault Status clear bit
(b) Gate driver: input selection, control mode, and adjustment bits.
(c) Sense block: enable/disable, control bits, and adjustment bits
(d) Sense block calibration: enable bit
In the register settings for hall sensor motor drive by using 3 comparators, the following settings are required for the general purpose comparators and differential amplifier 1 (if used) in the sense block.

- ICCTL2 register: DA1_EN bit
- GDSELA register: CMP1_HYS bit
- GDSELB register: CMP2_HYS bit
- GDSELC register: CMP3_HYS bit
- SNSCTL1 register: DA1_GAIN bit
- SNSCTL2 register: DA1_SH bit
- SNSCTL3 register: CMP1_VTH, CMP2_VTH bits
- SNSCTL4 register: CMP3_VTH, CAL_CONN, CAL_DA1 bits

The start-up sequence of the smart gate driver is configured by dividing the register settings into three steps (Register Setting 1, 2, and 3) for the above register settings (a), (b), (c), and (d).
For the timing of register settings, refer to ***4.1***. The registers to be set in Register Setting 1, 2, and 3 are shown below.

(1) Register Setting 1:

Register Setting 1 mainly includes the registers for the fault detection function. The following register settings are executed in start-up sequence example described in ***4.1***.

- FLTCTL1 register
- FLTCTL2 register
- ICCTL1 register

The response mode and adjustment bits of the fault detection function are also partially assigned to the OCPCTL register and the GDSELx (x = A, B, C) register. If you want to change the threshold value before judging the nFAULT terminal output to confirm the normal start-up, please execute these register settings with Register Setting 1.
When the register settings of the fault detection function are completed, set the CLR_FLT bit to clear the Fault Status.

(2) Register Setting 2:

Register Setting 2 mainly includes the registers for the gate driver and the sense block. The following register settings are executed in start-up sequence example described in ***4.1***.

- ICCTL2 register
- GDCTL register
- OCPCTL register
- GDSELx (x = A, B, C) register
- SNSCTLz (z = 1, 2, 3, 4) register

GDSELx (x = A, B, C) registers are used to select gate driver input signals. For MCU (RL78/G1F), the following settings are recommended.

- HOA_SEL bits = “001b” (IN1 input)
- LOA_SEL bits = “010b” (IN2 input)
- HOB_SEL bits = “011b” (IN3 input)
- LOB_SEL bits = “101b” (IN5 input)
- HOC_SEL bits = “100b” (IN4 input)
- LOC_SEL bits = “110b” (IN6 input)

Until these bit settings are completed, all INz (z = 1, 2, 3, 4, 5, 6) signals must be Low to avoid unexpected gate driver outputs. Also, all INz (z = 1, 2, 3, 4, 5, 6) signals must be Low before the EN terminal is set to Low because all registers are reset when the EN terminal is set to Low. For details, refer to the control sequence examples in ***4.1*** and ***4.2***.

The differential amplifiers also have register settings (CAL_DAz (z = 1, 2, 3) bits) to enable DC offset calibration. DC offset calibration can be performed separately for each differential amplifier, so be sure to perform the DC offset calibration corresponding to the differential amplifier used. To achieve highly accurate calibration, CAL_CONN = “1b” is recommended. With this setting, the inputs of the differential amplifier during the calibration period are the DAzP and DAzN (z = 1, 2, 3) pins, and normal calibration cannot be performed with current flowing through the shunt resistor.

(3) Register Setting 3

Register Setting 3 includes other settings of the gate driver and the sense block. The following register settings are executed in start-up sequence example described in ***4.1***.

- SNSCLT2 register
- SNSCTL5 register
- SNSCTL6 register

Although the SNSCTL2 register setting is not required for Hall sensor control, the setting is provided in consideration of the versatility of the start-up sequence.

The SNSCTL6 register has a write-protection function. Since setting the CTL6_UNLOCK bit of the SNSCTL5 register is required to allow SNSCTL6 register write, set the registers according to the following procedures.

(1) Set CTL6_UNLOCK bit of SNSCTL5 register to “1b” (Release the write lock to the SNSCTL6 register)
(2) Set SNSCTL6 register to “0x41”
(3) Set CTL6_UNLOCK bit of SNSCTL5 register to “0b” (Set the write lock to SNSCTL6 register)

The BEMF_OFFSET bit and the GD_AOR bit in the SNSCTL6 register must be set to “1b”. The RESERVED bits in the SNSCTL5 and SNSCTL6 registers must be set to “0b”.

3.3.1.3 Control Method and Operating Waveforms

In Hall sensor motor drive, the motor is controlled by switching the energized phase according to the position detection signal from the Hall IC. The polarity of the position detection signals can be detected by using general purpose comparators in the smart gate driver and interrupt functions of MCU.

Figure 3-4 shows an operating waveform diagram for Hall sensor motor drive by using 3 comparators. The polarity change of the Hall IC outputs (CMPzP (z = 1, 2, 3) inputs) depend on the mounting position of the Hall sensor, so the pattern of the energized phase must be changed according to the relation between the rotor position and the polarity of the Hall IC output.

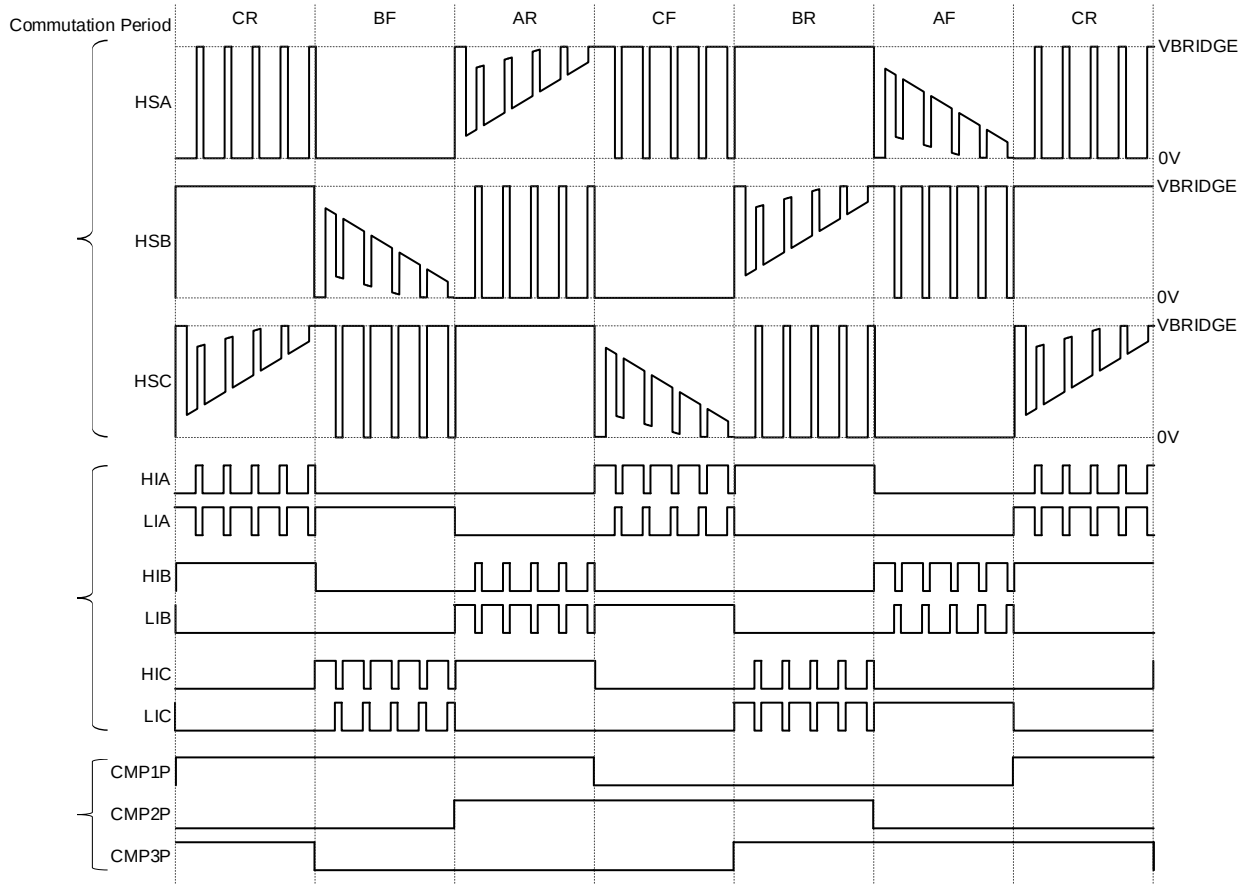


Figure 3-4 Operating Waveform Diagram – Hall Sensor Motor Drive by Using 3 Comparators

3.3.2 Sensorless Motor Drive by BEMF Sensing Comparator

3.3.2.1 Circuit Diagram

Figure 3-5 shows an example of a simplified application block diagram and application for sensorless motor drive by BEMF sensing comparator.

In sensorless motor drive by BEMF sensing comparator, the motor is controlled by switching the energized phase according to the induced voltage (BEMF) generated by the motor rotation. Motor position detection is performed by detecting the BEMF zero crossing using a general-purpose comparator or an A/D converter in the MCU in addition to the BEMF sense amplifier built into the smart gate driver. When using the general-purpose comparator built into the smart gate driver as a method to detect the BEMF zero crossing, connect the DA3O/MUX1 pin to the CMP2P pin or the CMP3P pin. ***Figure 3-5*** shows an example of input to the CMP3P pin. When using the A/D converter in the MCU as a method to detect the BEMF zero crossing, it is not necessary to connect to the A/D converter input pin because the DA3O/MUX1 pin is connected to the ANI5 analog input port of the MCU internally. When using a comparator in the MCU, connect the DA3O/MUX1 pin to the comparator input pin to be used.

When detecting the motor drive current by a shunt resistor or using current sense overcurrent function (CS_OCP), input the differential voltage across the shunt resistor to the DA1P and DA1N pins. The unused pins on the DAzP and DAzN (z = 1, 2, 3) pins should be connected to AGND.

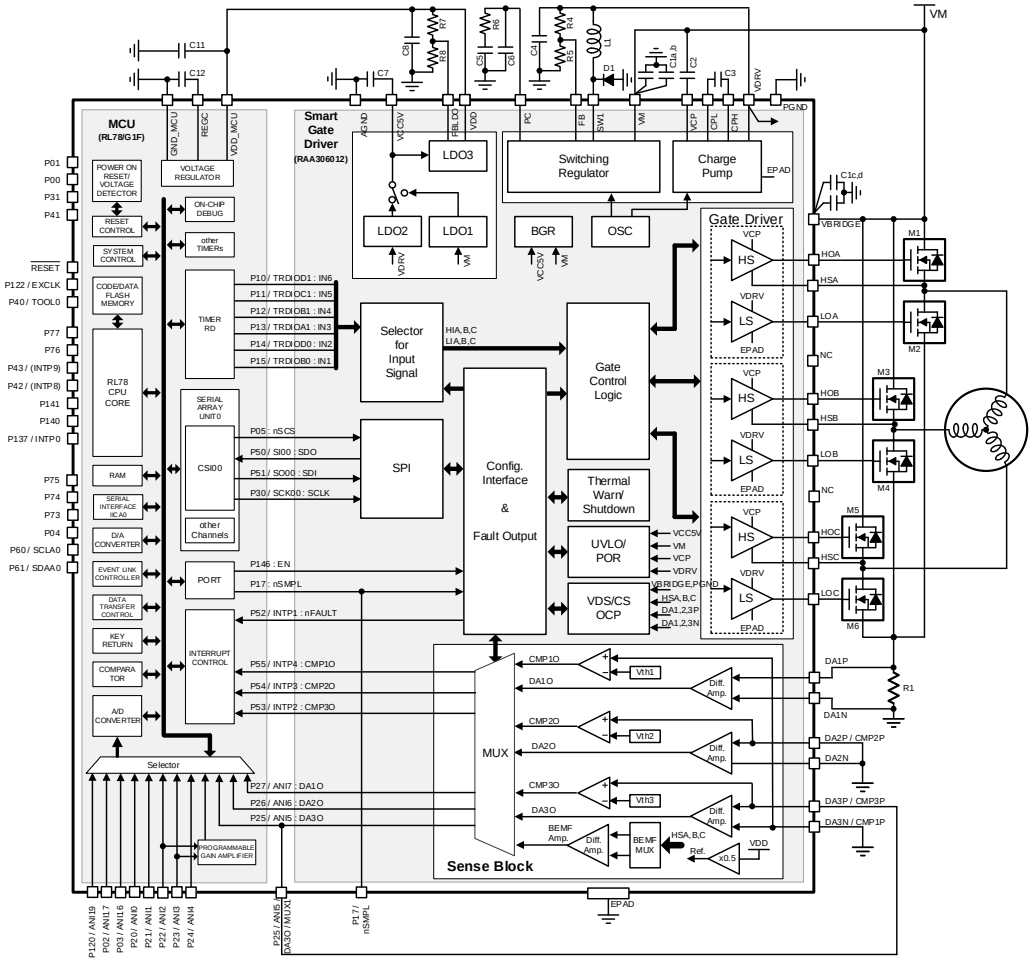


Figure 3-5 Simplified Application Block Diagram – Sensorless Motor Drive by BEMF Sensing Comparator

3.3.2.2 Register Settings

In the register settings for sensorless motor drive by BEMF sensing comparator, the following settings are required for the BEMF sense amplifier, general-purpose comparator, and differential amplifier 1 (if used) in the sense block.

- ICCTL2 register: BEMF_EN, DA1_EN bits
- GDSELC register: CMP3_HYS bit
- SNSCTL1 register: BEMF_GAIN, DA1_GAIN bits
- SNSCTL2 register: BEMF_PH, BEMF_SH, DA1_SH bits
- SNSCTL3 register: CMP1_VTH, CMP2_VTH bits
- SNSCTL4 register: CMP3_VTH, CAL_CONN, CAL_DA1 bits
- SNSCTL5 register: MUX bits
- SNSCTL6 register: BEMF_OFFSET bit

The start-up sequence of the smart gate driver is configured by dividing the register settings into three steps (Register Setting 1, 2, and 3) similar to the Hall sensor motor drive by using 3 comparators. The similar settings and procedures are used except for the above register settings of the sense block. For details on each register, refer to ***3.3.1.2***.

For details on the BEMF sense amplifier, refer to ***6.5.3*** in the ***"RAJ306102 Datasheet (R18DS0039EJ)"***. Also, for output control of the DA3O/MUX1 pin, refer to ***6.5.5*** in the ***"RAJ306102 Datasheet (R18DS0039EJ)"***. The unused general-purpose comparator can be disabled by setting CMPz_VTH (z = 1, 2, 3) bits to "0000b". It is recommended to set these bits together with the DAz_EN (z = 1, 2, 3) bits to disable unused differential amplifiers to reduce power consumption.

3.3.2.3 Control Method and Operating Waveforms

In sensorless motor drive by BEMF sensing comparator, the motor is controlled by switching the energized phase according to the BEMF zero crossing signal using a general-purpose comparator or an A/D converter in the MCU in addition to the BEMF sense amplifier built into the smart gate driver. The switching timing of the energized phase is controlled by using a timer so that the BEMF zero crossing comes in the center of the switching timing interval.

Figure 3-6 shows an operating waveform diagram for sensorless motor drive by BEMF sensing comparator. Since BEMF can be observed in the de-energized phase, the BEMF detection phase must be selected suitably each time the energized phase is switched. The selection method of the BEMF detection phase can be selected by the BEMF_PH bits. For details, refer to ***6.5.3*** in the ***"RAJ306102 Datasheet (R18DS0039EJ)"***. In addition, a detection mask time must be provided to prevent zero-crossing false detection due to kickback that occurs when switching the energized phase. Set an appropriate detection mask time considering the motor speed, drive current, etc.

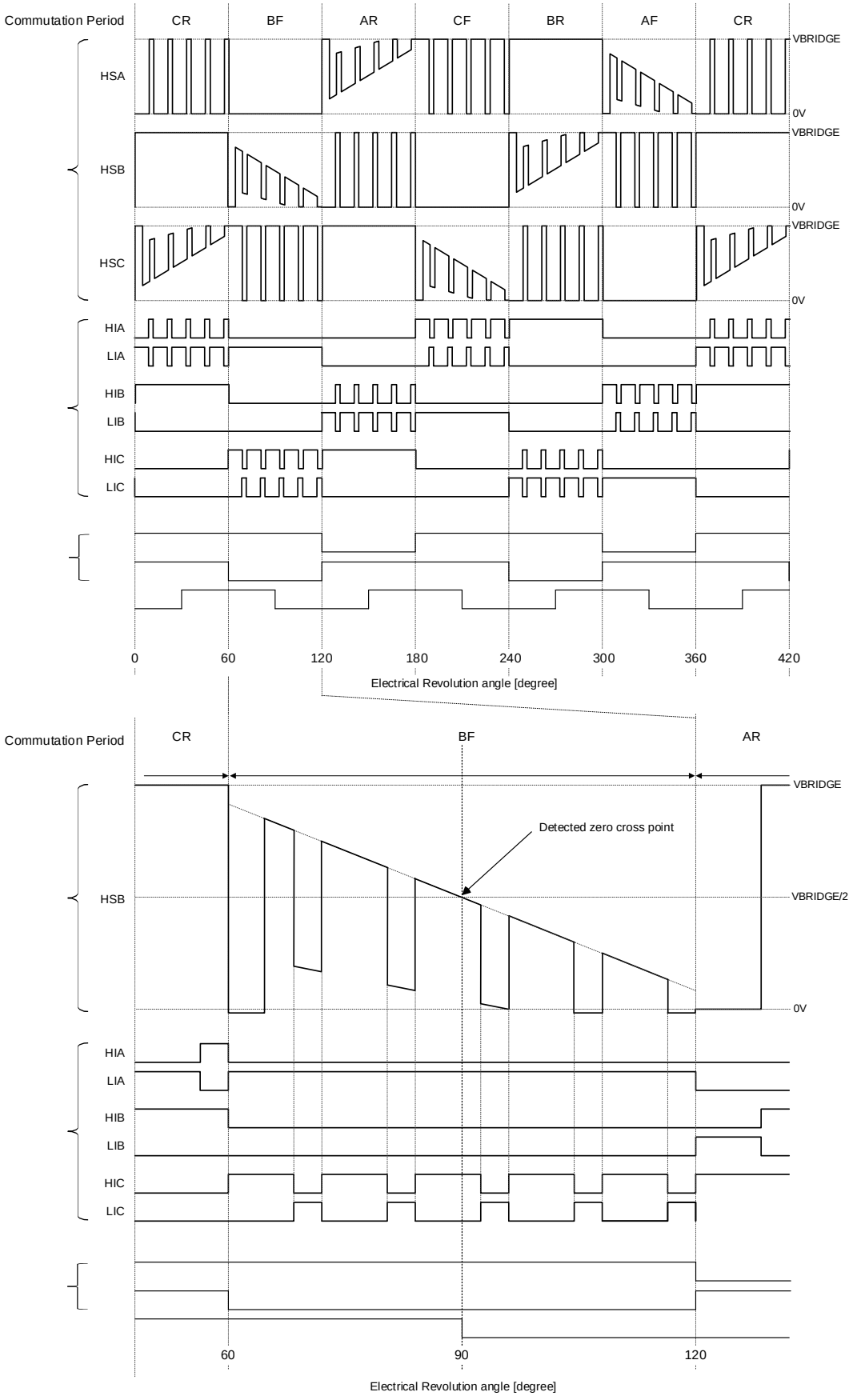


Figure 3-6 Operating Waveform Diagram – Sensorless Motor Drive by BEMF Sensing Comparator

Chapter 4 Control Sequence

This device incorporates the MCU (RL78/G1F) and smart gate driver (RAA306012) in a single package. To use this product to control a motor, the smart gate driver must be set to Operating Mode after the MCU reset is released, and the appropriate PWM signal must be input to INz (z = 1, 2, 3, 4, 5, 6). The smart gate driver operation mode depends on the EN output port setting of the MCU and the fault status of the smart gate driver. This chapter shows the flowchart and notes on each step for the following two control sequence examples to control the smart gate driver operation mode.

1. Start-up sequence
2. Error recovery sequence

For details on the smart gate driver power-on sequence, operation modes and Fault Management, refer to ***6.1*** and ***6.2*** in the ***"RAJ306102 Datasheet (R18DS0039EJ)"*** respectively. For details on register settings corresponding to motor control, refer to ***3.2***, ***3.3*** and ***"Source Files for Each Sample Program of RAJ306102"***.

4.1 Start-up Sequence Example

Figure 4-1 shows a flowchart of a start-up sequence example for the smart gate driver. In addition, the following are points to be noted at each step.

(1) Confirm power-on completion

This step is to judge the operation start of the start-up sequence. VCC5V pin voltage must be 4.0V (VCCUVR) or higher and the VM pin voltage must be 5.5V (VMUVR) or higher for the smart gate driver to start up. In this sequence example, after the measured VBRIDGE (= VM) pin voltage is at least 80% of the normal operating voltage, the sequence transitions to the next step. Consider an appropriate power supply confirmation method depending on the actual application, such as when using separate power supplies for the VM and VBRIDGE pins. In applications where the power-on completion is guaranteed by setting a wait time, it is acceptable to use a method that does not measure the power supply voltage.

(2) Wait for Smart Gate Driver start-up completion

This step is to wait until the power rail start-ups of the smart gate driver are done after the activation of the smart gate driver. First, the INz (z = 1, 2, 3, 4, 5, 6) output ports of the MCU are set to Low and the CMPzO (z = 1, 2, 3) input/output ports are set to digital input ports. The outputs of general-purpose comparators in the smart gate driver are set to output by default. These port settings of the MCU in advance can avoid unexpected gate driver outputs or output signal collisions with I/O ports of the MCU.

The smart gate driver is activated when the EN output port of the MCU is set to High. The nFAULT input port goes Low when the smart gate driver's band-gap voltage rises. The successful activation of the smart gate driver can be confirmed by checking the nFAULT input port.

After confirming the successful activation of the smart gate driver, a 15ms wait time is set. This is the wait time for the ready time of the internal oscillator, the DC offset calibration time of the differential amplifiers, the start-up time of the buck switching regulator and the charge pump. The wake-up time delay (twake) from the EN output port sets to High to the nFAULT input port goes High is 6.5ms (typ.), but since it varies depending on the clock frequency of the internal oscillator and the start-up time of the charge pump including external capacitors, check the actual start-up completion time and set to an appropriate wait time.

(3) Enable/disable fault detection functions and clear the Fault Status z (z = 0, 1, 2, 3) registers

This step is to select enable/disable for each fault detection function and clear the Fault Status z (z = 0, 1, 2, 3) registers (FLTSTSz (z = 0, 1, 2, 3)), which contain the indicators corresponding to each fault detection, before driving the motor.
The Fault Control 1 register (FLTCTL1) and the Fault Control 2 register (FLTCTL2) are used to select enable/disable for each fault detection function. Only current sense overcurrent protection by shunt resistor (CS_OCP), where the input signals to DAzP and DAzN (z = 1, 2, 3) are different depending on the application, is disabled by default. Enable the suitable fault detection functions according to the actual application and specifications. The Fault Status z (z = 0, 1, 2, 3) register can be cleared by setting the CLR_FLT bit in the IC Control 1 register (ICCTL1) to “1b”. The CLR_FLT bit automatically returns to “0b”. It is recommended that the other settings in the IC Control 1 register (ICCTL1) be set together when setting the CLR_FLT bit.
A 1ms wait time is provided as the status clear execution time after completing Register Setting 1 (refer to ***3.3.1.2 (1))*** as the status clear execution time, even 300µs including variation is sufficient.

(4) Confirm normal start-up completion and set registers according to application

This step is to confirm the normal start-up completion of the smart gate driver, set the various registers of the gate driver and sense block, and complete the start-up sequence.
nFAULT input port is checked, and if it is High, the start-up is judged to have been completed normally. This indicates that the smart gate driver has entered to the Operating Mode. However, if the nFAULT input port is low, it means that a fault detection has been triggered and the Initial Error is judged. If an error occurs at start-up after power-on, it is assumed that some power rails are abnormal, so set the EN output port to Low to stop the smart gate driver operation.
After confirming the nFAULT input port is High, set register settings for the gate driver and sense block as Register Setting 2 (refer to ***3.3.1.2 (2))***. In this example sequence, it is configured that the DC offset calibration of the differential amplifiers to be used is executed in Register Setting 2. The DC offset calibration of the corresponding amplifiers is initiated by setting the CAL_DA1 bit, CAL_DA2 bit, and CAL_DA3/BEMF bit in the Sense Block Control 4 register (SNSCTL4) to “1b”. By using the CAL_CONN bit, it is possible to perform offset calibration with high accuracy using the same inputs as the actual differential amplifier. It is recommended that the CAL_CONN bit be set to “1b”. However, note that when a motor is being driven or motor current is flowing through the shunt resistor, it is impossible to perform a normal offset calibration.
A 1ms wait time is provided after the initiation of the DC offset calibration in Register Setting 2. Since the DC offset calibration requires a wait time of 400µs per amplifier, set the wait time according to the number of amplifier to be calibrated, or use the automatic clear function of the CAL_DA1 bit, CAL_DA2 bit, and CAL_DA3/BEMF bit to confirm completion of the DC offset calibration.
In Register Setting 3 (refer to ***3.3.1.2 (3))***, set the detect phase selection method of the BEMF sense amplifier and change the Sense Block Control 6 register (SNSCTL6) setting to the recommended value.
When using the BEMF sense amplifier, the BEMF_PH bit in the Sense Block Control 2 register (SNSCTL2) must be set to the appropriate selection method. For details, refer to ***6.5.3*** in the ***“RAJ306102 Datasheet (R18DS0039EJ)”***.
Sense Block Control 6 register (SNSCTL6) has a write-protection function and is initially in a write-locked state, so set the registers according to the following procedure.
(1) Set CTL6_UNLOCK bit of SNSCTL5 register to “1b” (Release the write lock to the SNSCTL6 register)
(2) Set SNSCTL6 register to “0x41”
(3) Set CTL6_UNLOCK bit of SNSCTL5 register to “0b” (Set the write lock to SNSCTL6 register)
After completing Register Setting 3, the MCU can change the CMPzO (z = 1, 2, 3) input/output port settings according to application. This completes the start-up sequence.

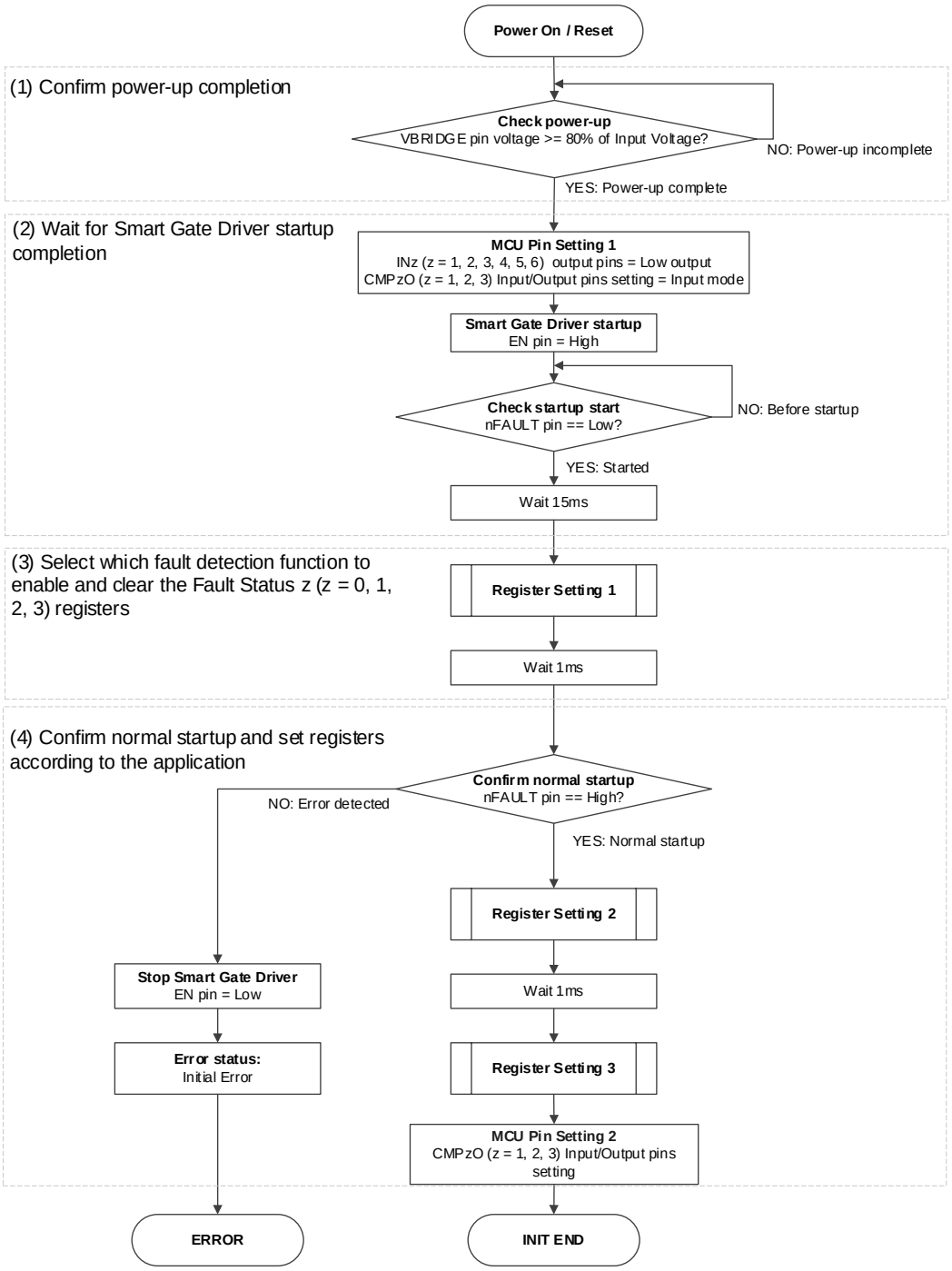


Figure 4-1 Smart Gate Driver Start-up Sequence Example

4.2 Error Recovery Sequence Example

Figure 4-2 shows a flowchart of an error recovery sequence example for the smart gate driver. The fault and recovery actions for the fault detection functions of the smart gate driver depend on the contents of the fault detection. Although these actions also depend on the register settings for the fault detection function, they are classified as followings in the sequence example shown in ***Figure 4-2.***
(a) Fault detection with automatic recovery (OTSD, TWARN, VM_UV, VM_OV, VDRV_OV)
(b) Fault detection with automatic recovery and the power rails restart (VCP_UV, SR_OCP, VDRV_UV)
(c) Fault detection without automatic recovery (latched mode fault) (VDS_OCP, VGS_FAULT, CS_OCP)
In the error recovery sequence, it is important to check the contents of the fault detection, classify them according to the contents of the fault detection and the recovery action as described above, and then design a recovery flow corresponding to each fault detection. The followings are points to be noted at each step of the error recovery sequence. This sequence example is used in the sample program of this device. All errors including the abnormality of the motor drive are configured to pass through this sequence. Refer to ***"Source Files for Each Sample Program of RAJ306102"*** and modify the sequence configuration according to the specification of error handling on application.

(1) Check operation status

In the first step of the error recovery sequence, the status of the EN output port is checked to judge whether the detected error is recoverable or not. When the EN output port is Low, the error corresponds to an Initial Error in the start-up sequence, a Regulator Error that the power rails could not be restarted as described below, or an Overcurrent Error that is not automatically recoverable. In these cases, the EN output port is configured to remain Low as a non-recoverable error detection.

(2) Check error contents and port settings

This step is to confirm whether the error has been detected in the smart gate driver and to change the port settings in advance for recovery. If the smart gate driver does not report any error (FAULT bit in Fault Status 0 register (FLTSTS0) is "0b"), the error is judged as being caused by other than the smart gate driver, such as a motor rotation error. In this case, the smart gate driver does not need to recover, and the error recovery sequence is terminated.
However, if the FAULT bit is "1b", the smart gate driver is judged to have occurred the fault. The INz (z = 1, 2, 3, 4, 5, 6) output ports must be set to Low and the CMPzO (z = 1, 2, 3) input/output ports must be set to Input mode. These port settings avoid unexpected gate driver outputs or output signal collisions with the I/O ports of the MCU by the recovery action from the fault condition.

(3) Classify error

This step is to classify the detected error into (a), (b), and (c) using the read result of the Fault Status z (z = 0, 1, 2, 3) registers (FLTSTSz (z = 0, 1, 2, 3)). If multiple errors are detected, it is recommended that they be classified according to the priority of (c), (b), and (a). Consider the appropriate classification for each error detection according to the application and specifications.

(4) Confirm recovery

This step is to confirm the automatic recovery completion of the smart gate driver by checking the nFAULT input port. When the nFAULT input port is Low, the operation mode of the smart gate driver has not returned to the Operating Mode, so the error recovery sequence is terminated and restarted again. When the nFAULT input port is High, the Operating Mode is recovered, the smart gate driver can operate normally, and the sequence step transitions to (7) Handling to complete recovery.

(5) Confirm power rails restart and Handling to stop

This step judges whether the power rails have recovered by restart for the error classified as (b) in the step of (3) Classify error. If it cannot be recovered, the handling to stop the smart gate driver is executed.
If SR_OCP or VDRV_UV error is detected, the buck switching regulator enters Hiccup mode, where the PWM is disabled for a dummy cycle (63ms) and the true soft-start cycle is attempted again after the dummy cycle. Considering the variation of the dummy cycle and the soft-start period, a wait time of 100ms or more (150ms in the sequence example) is provided before checking the nFAULT input port to judge whether the power rails have recovered.
In this sequence example, this nFAULT check is repeated up to 5 times, and if the nFAULT input port goes High and the power rails recover, the sequence step transitions to (7) Handling to complete recovery. If not, the EN output port is set to Low to stop the smart gate driver, the Regulator Error is judged, the error recovery sequence is terminated, and the smart gate driver remains stopped.
This sequence example shows the same sequence of checking the nFAULT input port every 150ms when a VCP_UV fault is detected. Since the charge pump does not enter Hiccup mode like the buck switching regulator, the timing for checking the nFAULT input port can be changed to the different check timing from the buck switching regulator. Please consider the appropriate check timing and handling according to the actual application and specifications.

(6) Handling to stop for latched mode fault

This step is to stop the smart gate driver when a fault is detected that keeps the smart gate driver in Fault Management Mode. Since this fault detection is caused by the half bridge error, the EN output port is set to Low to stop the smart gate driver, the Overcurrent Error is judged, the error recovery sequence is terminated, and the smart gate driver remains stopped.

(7) Handling to complete recovery

This step is to clear the Fault Status z (z = 0, 1, 2, 3) registers and to reconfigure the I/O ports of the MCU for the motor restart when the automatic recovery of the smart gate driver is confirmed in the (4) Confirm recovery and (5) Confirm power rails restart and Handling to stop. The CLR_FLT bit in the IC Control 1 register (ICCTL1) clears the Fault Status z (z = 0, 1, 2, 3) registers and the CMPzO (z = 1, 2, 3) input/output ports are changed to application-specific settings to complete the error recovery sequence. The error recovery sequence is terminated.

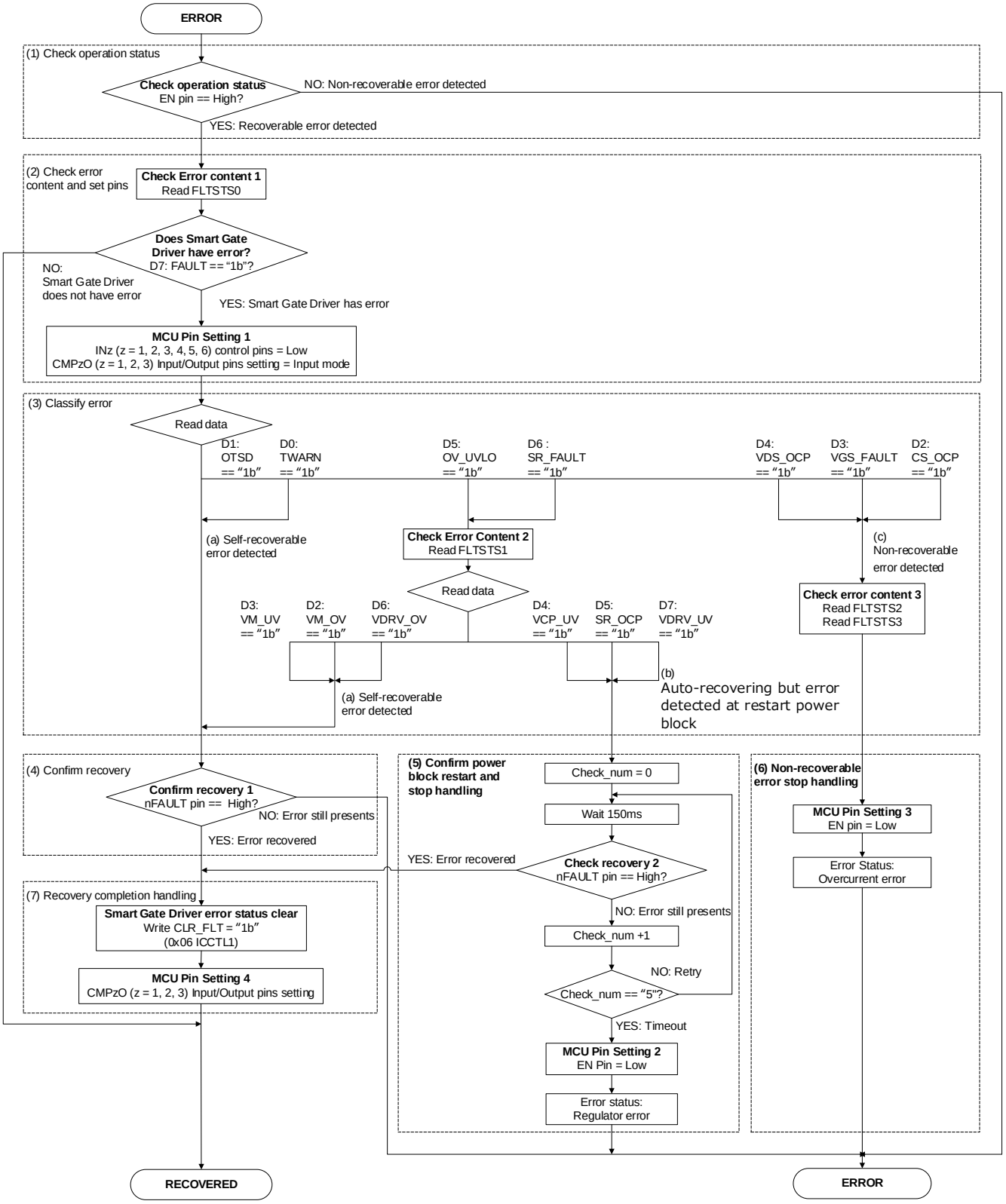


Figure 4-2 Smart Gate Driver Error Recovery Sequence Example

Chapter 5 Circuit Design, Component Selection, and Board Layout Recommendations

The RAJ306102 incorporates the MCU (RL78/G1F) and smart gate driver (RAA306012) in a single package, it is important to use this device with the appropriate hardware configuration. This chapter describes the circuit design, component selection and precautions, and board layout recommendations. The appropriate hardware configuration for each application should be determined by careful checks and verifications based on the operating environment, conditions, and specifications.

5.1 Circuit Design, Component Selection, and Precautions

Figure 5-1 and ***Table 5-1*** show an example of the external circuit for sensorless motor drive by BEMF sensing comparator motor drive and the external component list. The effective capacitance value of the capacitor decreases from the nominal value according to the applied voltage due to the DC bias characteristics. Please select the capacitors in consideration of the DC bias characteristics of the product. The capacitance values shown in the following descriptions are nominal values.
The example parts list shows the effective capacitance value of the capacitor used on our evaluation board (RTK0EML2J0D01021BJ) as a reference.

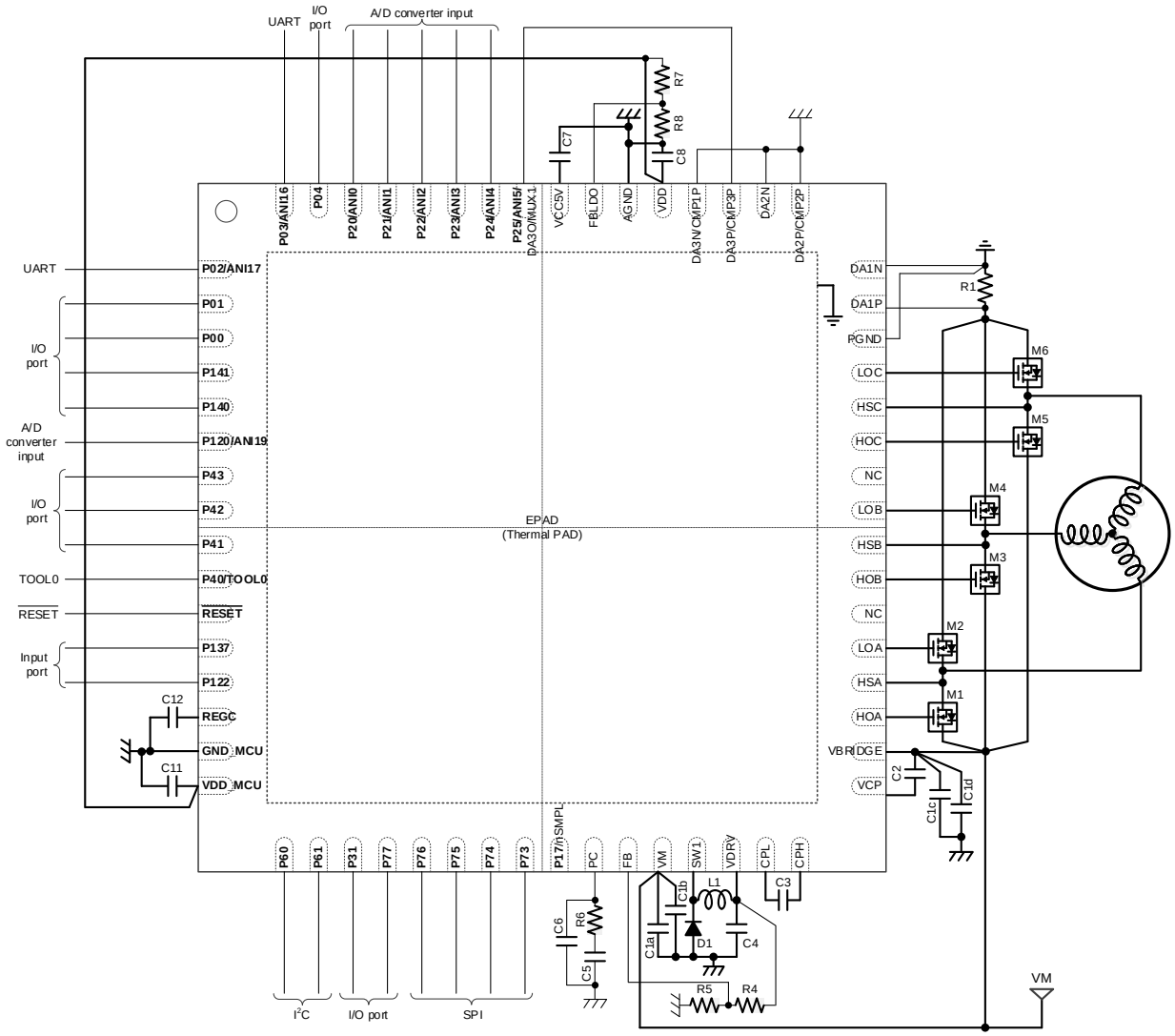


Figure 5-1 External Circuit Example of Sensorless Motor Drive by BEMF Sensing Comparator

Table 5-1 External Component List Example for Sensorless Motor Drive by BEMF Sensing Comparator

Part No.	Recommended Value	Effective Value	Ratings	Purpose	Notes
R1	Depend on application	-	Depend on application	Shunt resistance for current sense	
R4	48.7kΩ	-	-	Bleeder resistance for VDRV output voltage setting	1
R5	3.48kΩ	-	-	Bleeder resistance for VDRV output voltage setting	1
R6	60.4kΩ	-	-	Phase compensation resistance for the switching regulator	4
R7	160kΩ	-	-	Bleeder resistance for VDD output voltage setting	2
R8	91kΩ	-	-	Bleeder resistance for VDD output voltage setting	2
C1a	3x 4.7µF	2 x 5.45µF	100V	Bypass capacitance for VM terminal	5
C1b	0.1µF	0.038µF	100V	Bypass capacitance for VM terminal	5
C1c	4.7µF	5.45µF	100V	Bypass capacitance for VBRIDGE terminal	5
C1d	0.1µF	0.038µF	100V	Bypass capacitance for VBRIDGE terminal	5
C2	2.2µF	1.04µF	25V	Bypass capacitance for VCP terminal	3
C3	0.22µF	0.18µF	100V	Pumping capacitance for the charge pump	3
C4	10µF	5.5µF	25V	Output capacitance for the switching regulator, VDRV terminal	4
C5	2200pF	2190pF	10V	Phase compensation capacitance for the switching regulator	4
C6	DNP	DNP	10V	Phase compensation capacitance for the switching regulator	
C7	22µF	10.3µF	10V	Output capacitance for the linear regulator, VCC5V terminal	
C8	22µF	10.3µF	10V	Output capacitance for the linear regulator, VDD terminal	
C11	0.1µF	0.072µF	10V	Bypass capacitance for VDD_MCU terminal	
C12	0.47µF	0.85µF	10V	Regulator output stabilization capacitance	
M1 to M6	Depend on application	-	Depend on application	Power MOSFET for the motor drive	
L1	22µH or 33µH	-	>2A	Coil for the switching regulator	
D1	0.6V	-	100V, >2A	Schottky rectifier diode for the switching regulator	

Note1: VDRV output voltage is 12V with these resistors.
Note2: VDD output voltage is 3.310V with these resistors.
Note3: Please consider the effective capacitance. The smaller C3 causes the larger voltage to drop of VCP.
The smaller C2 causes the larger voltage ripple of VCP.
Note4: Please select the suitable value of R6 and C5 depending on C4 effective capacitance.
Note5: The suitable capacitance depends on the constraints of the application and characteristic.

5.1.1 VM, VBRIDGE Pin Capacitors (C1a, C1b, C1c, C1d)

This device operates by supplying DC power (6 to 65V) to the VM and VBRIDGE pins. The capacitors are required in the power supply line to stabilize the power supply and to handle high frequency currents. These capacitors can prevent abrupt voltage changes during system power-on. Increasing capacitance helps reduce power supply ripple but increases size and cost. The appropriate capacitor should be selected considering the motor system operating voltage, switching frequency, required current capability, allowable power supply ripple, motor type, and start-up/stop sequence constraints.
The power supply line for high frequency components causes an increase in impedance due to parasitic inductance of the battery and cables; a local capacitor placed near to the power supply pins of this device has the effect of reducing the impedance for high frequencies and thus contributes as a preferable path for the high frequency components. The appropriate local capacitor should be selected based on ripple current, resonant frequency, package, cost constraints, etc. In a typical application, electrolytic capacitors are placed near to the DC power input, and several ceramic capacitors are placed near to the VM and VBRIDGE pins of this device as well.

5.1.2 Linear Regulator Components (C7, C8, R7, R8)

In this device, the VCC5V pin or the VDD pin can be used as a power supply for peripheral circuits including the MCU. LDO3 that supplies voltage to the VDD pin are supplied from LDO1 and LDO2 that supply 5V to the VCC5V pin. Therefore, the allowable external load current capability is defined as the total of VCC5V pin and the VDD pin load current including MCU.
The total current supplied from the VCC5V and VDD pins to the MCU and peripheral circuits should not exceed the allowable external load current as shown below. When the EN output port is low, LDO1 is ON and LDO2 is OFF. For details on the ON/OFF states of LDO1 and LDO2 according to the Power-On sequence, the smart gate driver mode, and fault and recovery action of fault detection functions, refer to ***6.1***, ***6.3.1*** and ***6.2*** in the ***"RAJ306102 Datasheet (R18DS0039EJ)"***.

Table 5-2 External Load Current Capability for VCC5V and VDD Pins

Condition			External Load Current Capability
EN output port	5V LDO1	5V LDO2	
Low	ON	OFF	50mA
High	ON	OFF	70mA
High	OFF	ON	90mA

5.1.2.1 VCC5V Pin Capacitor (C7)

This device contains two LDOs: LDO1 and LDO2, which supply 5V to the VCC5V pin. These LDOs can supply 5V to the analog and logic circuits in the smart gate driver as well as 5V to the peripheral circuits including the MCU.
The voltage on the VCC5V pin is generated by LDO1, which is powered by the VM pin, while the smart gate driver is disabled (EN output pin = Low), before the smart gate driver is enabled (EN output pin = High) and the buck switching regulator completes start-up. After the start-up of buck switching regulator is completed, the voltage on the VCC5V pin is generated by LDO2, which is powered by the VDRV pin. A ceramic capacitor of 22µF (with an effective capacitance value of about 10µF) is recommended as the decoupling capacitor (C7) on the VCC5V pin. This capacitor should be placed as close as possible to the VCC5V and AGND pins.

5.1.2.2 VDD Pin Capacitor (C8), VDD Output Voltage Setting Resistors (R7, R8)

The smart gate driver uses VDD pin as the interface power supply.
There are three methods to supply voltage to the VDD pin: (1) by using LDO3, (2) by supplying 5V from the VCC5V pin, or (3) by using an external power supply. The following are precautions for each method.

(1) Supply using LDO3

The external connection and components are shown in ***Figure 5-2 (1).*** The LDO3 output voltage VDD is determined by the bleeder resistors (R7, R8) that are fed back to the FBLDO pin, allowing fine adjustment of the output voltage within the recommended operating conditions. The bleeder resistors should be selected based on ***EQ 5-1.*** Increasing the total value of the bleeder resistor can reduce the current consumption in Sleep Mode. However, note that the stability is reduced by the pole determined by the parasitic capacitance of FBLDO pin and the bleeder resistors.

EQ 5-1

$$V_{DD} = V_{REF\_DD}\left(1 + \frac{R_7}{R_8}\right)$$

where: V_{REF_DD}: FBLDO pin reference voltage = 1.2V, R_7: resistance between VDD and FBLDO pins, R_8: resistance between FBLDO and AGND pins

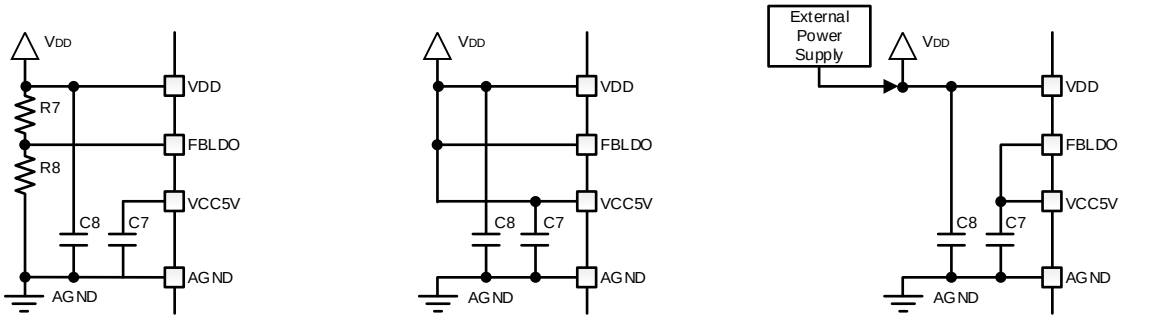
If R_7 = 160kΩ and R_8 = 91kΩ, the output voltage of LDO3 becomes 3.310V. A 22µF (effective capacitance value of about 10µF) ceramic capacitor is recommended as the decoupling capacitor (C8) on the VDD pin. This capacitor should be placed as close as possible to the VDD and AGND pins.

(2) Supply 5V from the VCC5V pin

The external connection and components are shown in ***Figure 5-2 (2)***. A 0.1µF ceramic capacitor is recommended as a decoupling capacitor (C8) for the VDD pin. This capacitor should be placed as close as possible to the VDD and AGND pins.

(3) Supply using an external power supply

The external connection and components are shown in ***Figure 5-2 (3)***. Connect an external power supply to the VDD pin. Also, connect the FBLDO pin to the VCC5V pin. Note that the recommended operating voltage range VDDope for the VDD pin voltage is limited from 3.135 to 5.25V. A 0.1µF ceramic capacitor is recommended as the decoupling capacitor (C8) on the VDD pin. This capacitor should be placed as close as possible to the VDD and AGND pins.



(1) V_{DD} = LDO3 (2) V_{DD} = VCC5V (3) V_{DD} = External power supply

Figure 5-2 VDD Pin Voltage Supply Methods

5.1.3 Components for Buck Switching Regulator (R4, R5, L1, C4, C5, R6)

5.1.3.1 Resistors for VDRV Output Voltage Setting (R4, R5)

The VDRV pin is the output pin of the buck switching regulator. It is used as the power supply for the low-side gate driver and the power supply for LDO2, which supplies 5V to the VCC5V pin. The output voltage depends on the bleeder ratio (R4/R5) of the external feedback resistor configured with the VDRV and FB pins shown in ***Figure 5-3.***

The output voltage V_{DRV} is adjustable from 5 to 15V and can be calculated using **EQ 5-2**.

EQ 5-2

$$V_{DRV} = V_{REF\_SR}\left(1 + \frac{R_4}{R_5}\right)$$

where: V_{REF_SR}: FB pin reference voltage = 0.8V, R_4: resistance between VDRV and FB pin, R5: resistance between FB and AGND pin.

For example, if R_4 = 48.7kΩ and R_5 = 3.48kΩ, then V_{DRV} = 12V; if R_4 = 47kΩ and R_5 = 3.3kΩ, then V_{DRV} = 12.19V.

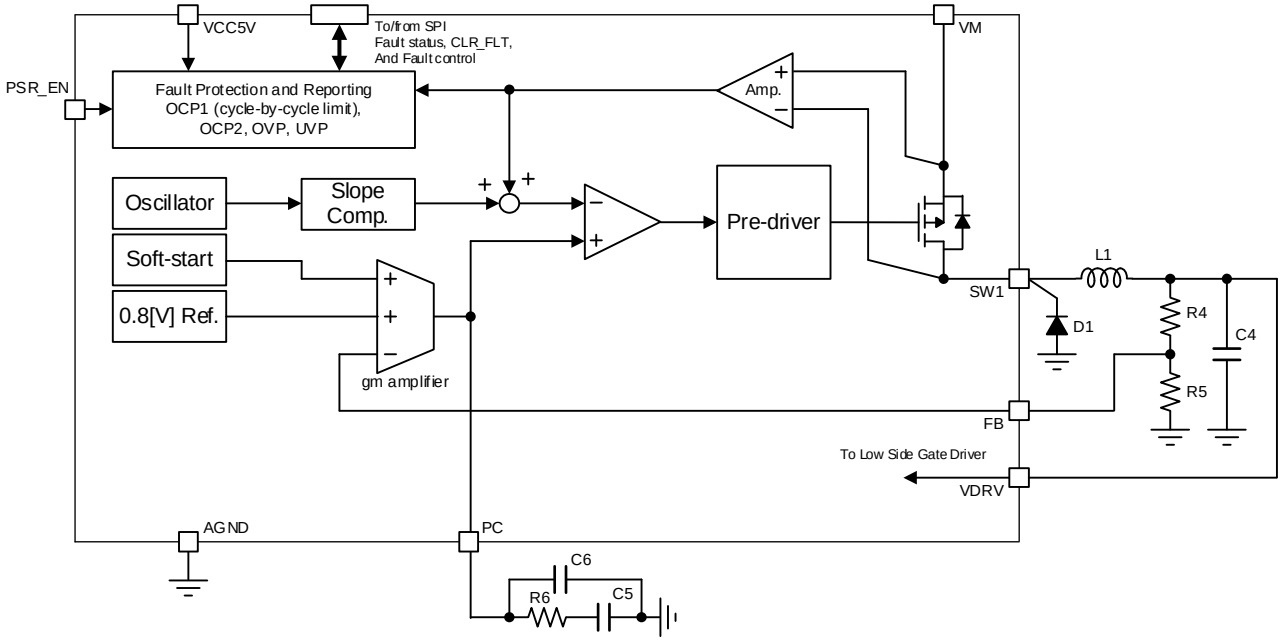


Figure 5-3 Buck Switching Regulator Block Diagram

5.1.3.2 Inductor (L1)

The buck switching regulator generates the VDRV pin voltage at a switching frequency of 500kHz. The buck switching regulator requires a 33µH or 22µH inductor (L1). The inductance of the inductor (L1) determines the ripple current (ΔI). Generally, the ripple current is assumed to be about 30 to 40% of the maximum output load current. Select a inductor (L1) with its peak current including ripple current not exceeding 1A considering the size of the component and load conditions. The values of ripple current (ΔI) and peak current (I_{peak}) of the inductor (L1) can be estimated by ***EQ 5-3*** and ***EQ 5-4***. A 33µH inductor has a ripple current (ΔI) larger than the expected value, as shown in the example below, but this is the recommended value considering the output ripple voltage (ΔV_{DRV}).

EQ 5-3

$$\Delta I = \frac{V_M - V_{DRV}}{f_{sw} \times L_1} \times \frac{V_{DRV}}{V_M}$$

where V_M: input voltage, V_{DRV}: output voltage, f_{sw} : switching frequency = 500kHz, L_1: inductance.

EQ 5-4

$$I_{peak} = I_o + \frac{\Delta I}{2}$$

where I_o: maximum output load current.

For example, if V_M = 48V, V_{DRV} = 12V, L_1 = 33µH, I_o = 0.5A, then ΔI = 0.545A and I_{peak} = 0.773A. If the ripple current (ΔI) of the inductor (L1) becomes large and the peak current (I_{peak}) becomes larger, the current limit (IOC1_SR) (1.2A typ.) per PWM cycle may be triggered when the load current of the VDRV pin is large. Since this limits the load current capability, the inductance should be selected considering the required load current. However, increasing the inductance can reduce the ripple current and ripple voltage. However, the larger inductance worsens the load transient response, so the actual output voltage (V_{DRV}) waveform should be checked for the suitable component selection. Also, for the inductor specification of the maximum DC current, select a component whose inductance does not decrease significantly even under the current limit (I_{OC1_SR}) conditions.

5.1.3.3 Input Capacitors (C1a, C1b), Output Capacitor (C4)

An output capacitor (C4) is required to smooth the inductor current. The output ripple voltage (ΔV_{DRV}) and load transient response are two important factors when selecting the output capacitor (C4). These characteristics should be considered in terms of the effective capacitance value considering the DC bias characteristic. For the characteristics of capacitors used in the actual application, refer to the "***Datasheets of Relevant Components"***. Under the assumption that low ESR ceramic capacitors are used, the capacitance required to satisfy the output ripple voltage (ΔV_{DRV}) in a buck switching regulator can be estimated by ***EQ 5-5***.

EQ 5-5

$$\Delta V_{DRV} = \frac{\Delta I}{8 \times f_{sw} \times C_4}$$

where ΔI: ripple current of the inductor, f_{sw}: switching frequency = 500kHz, C_4: effective capacitance of the output capacitor.

For example, if ΔI = 0.545A and C_4 = 5.5µF (effective capacitance value), then ΔV_{DRV} = 24.8mV.
In general, to supply a stable input voltage, the main power supply source requires electrolytic capacitors with capacitance corresponding to the input power supply conditions of the system. For better EMC performance, it is important to absorb the switching frequency pulse current by the buck switching regulator, and the input capacitors on the VM pin (C1a, C1b) should be able to handle the RMS current from the switching power supply circuit. Therefore, ceramic capacitors must be used for the input capacitors on the VM pin. The multiple capacitors including 1µF or more and 0.1µF are recommended according to EMC performance. These capacitors should be placed as close as possible to this device. (For the placement of each capacitor, refer to ***5.2***.)

5.1.3.4 Phase Compensation Capacitor (C5) and Resistor (R6)

The phase compensation is required for the stable operation of the buck switching regulator. The following describes how to select the phase compensation capacitor (C5) and resistor (R6).
First, determine the open-loop gain. The buck switching regulator consists of the following three gains, A1, A2, and A3, which can be obtained by ***EQ 5-6***, ***EQ 5-7*** and ***EQ 5-8*** respectively.

- A1: Gain from VDRV to FB pin by resistor voltage divider
- A2: Gain from FB pin to gm amplifier output (PC pin)
- A3: Gain from PC pin to VDRV pin

The open-loop transfer function A_{OPN} is the product of these gains and can be obtained by ***EQ 5-9***. If V_{DRV} = 12V, I_o = 0.5A, then A_{OPN} = 9766V/V = 79.79dB.

EQ 5-6

$$A_1 = \frac{V_{REF\_SR}}{V_{DRV}}$$

where V_{REF_SR}: FB pin reference voltage = 0.8V, V_{DRV}: VDRV pin voltage (V).

EQ 5-7

$$A_2 = g_{m\_SR} \times R_{oSR}$$

where g_{m_SR}: g_m amplifier transconductance = 200µA/V, R_{oSR}: g_m amplifier output resistance = 14MΩ.

EQ 5-8

$$A_3 = g_{m\_PW} \times R_{OUT} = g_{m\_PW} \times \frac{V_{DRV}}{I_o}$$

where g_{m_PW}: g_m amplifier current gain = 2.18A/V, R_{OUT}: VDRV pin output resistance, I_o: output load current (A).

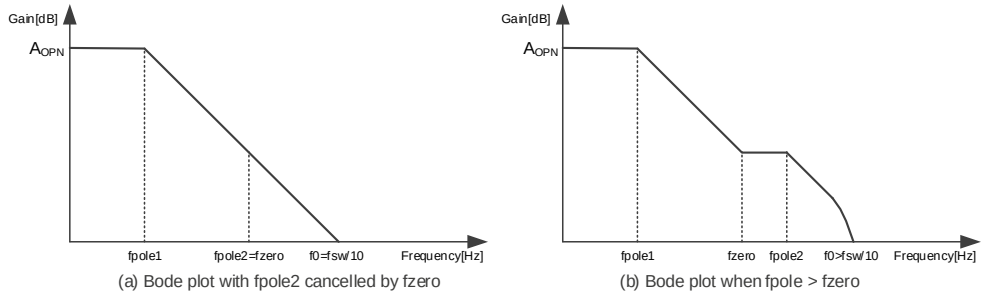
EQ 5-9

$$A_{OPN} = A_1 \times A_2 \times A_3$$

Next, determine the target bandwidth (f_0). In the buck switching regulator, the frequency response is mainly determined by the poles (1) and (2), and zero (3). (4) is a double pole due to switching operation, and the target bandwidth is set to a frequency lower than this double pole.

(1) f_{pole1}: 1st pole determined by g_m amplifier output resistance R_{oSR} and phase compensation capacitance (C_5)
(2) f_{pole2}: 2nd pole determined by VDRV pin output resistance R_{OUT} and output capacitance (C_4)
(3) f_{zero}: Zero determined by phase compensation resistance (R_6) and phase compensation capacitance (C_5)
(4) Double pole at half switching frequency (f_{sw}/2)

The target bandwidth (f_0) is set to 1/10 or less of the switching frequency (f_{sw}) to avoid stability degradation due to the phase delay of (4). The stability is ensured by setting (1) to match the target bandwidth (f_0) and canceling the pole (2) with the zero (3) (***Figure 5-4 (a)***).



(a) Bode plot with fpole2 cancelled by fzero (b) Bode plot when fpole > fzero

Figure 5-4 Image Diagram of Bandwidth and Phase Compensation for the Buck Switching Regulator

The 1st pole (f_{pole1}) is obtained by ***EQ 5-10***.

EQ 5-10

$$f_{pole1} = \frac{1}{2\pi \times R_{oSR} \times C_5}$$

where R_{oSR}: g_m amplifier output resistance = 14MΩ, C_5: phase compensation capacitance.

However, when the target bandwidth (f0) is set to 1/N of the switching frequency (fsw), the 1st pole (fpole1) can also be obtained using the open loop gain (AOPN) as in ***EQ 5-11***.

EQ 5-11

$$f_{pole1} = \frac{f_{sw}/\ N}{A_{OPN}}$$

Therefore, the phase compensation capacitance (C5) can be calculated by ***EQ 5-12*** using ***EQ 5-10***, ***EQ 5-11***.

EQ 5-12

$$C_5 = \frac{A_{OPN} \times N}{2\pi \times R_{oSR} \times f_{sw}0}$$

If the target bandwidth (f_0) is 50kHz (N = 10), which is 1/10 of the switching frequency f_{sw} = 500kHz, A_{OPN} = 9766V/V, R_{oSR} = 14MΩ, then C_5 = 2221pF ≈ 2200pF.
The 2nd pole can be obtained by ***EQ 5-13***.

EQ 5-13

$$f_{pole2} = \frac{1}{2\pi \times R_{OUT} \times C_4} = \frac{I_o}{2\pi \times V_{DRV} \times C_4}$$

where R_{OUT}: VDRV pin output resistance (Ω), C_4: VDRV pin output effective capacitance, I_O: output load current (A).

One the other hand, zero (f_{zero}) is obtained by ***EQ 5-14***.

EQ 5-14

$$f_{zero} = \frac{1}{2\pi \times R_6 \times C_5}$$

where R_6: phase compensation resistance, C_5: phase compensation capacitance.

Since the first-order characteristic determined by the 1st pole (f_{pole1}) and the open-loop gain (A_{OPN}) can be obtained by canceling the 2nd pole (f_{pole2}) with zero (f_{zero}), the phase compensation resistance (R_6) can be calculated by using ***EQ 5-15***.

EQ 5-15

$$R_6 = \frac{V_{DRV} \times C_4}{I_o \times C_5}$$

If V_{DRV} = 12V, I_o = 0.5A, C_5 = 2200pF, C_4 = 5.5µF (effective capacitance value), then R_6 = 60kΩ ≈ 60.4kΩ. The output capacitor (C4) on the VDRV pin should be calculated with the effective capacitance value considering DC bias characteristics. The 2nd pole (f_{pole2}) depends on the output capacitance (C4). If the effective capacitance value is smaller than the value used in the calculation example, the 2nd pole (f_{pole2}) becomes a higher frequency than expected, and the actual bandwidth increases from the target bandwidth (f_0) as shown in ***Figure 5-4 (b)***. It causes the double pole (f_{pole1n}, f_{pole2n}) at a frequency of 1/2 of the switching frequency (f_{sw}) to be more susceptible and may affect stability.

5.1.4 Charge Pump Output Capacitor (C2), Pumping Capacitor (C3)

The charge pump output VCP pin is the power supply for the high-side gate driver. For charge pump operation, a pumping (flying) capacitor (C3) is required between the CPH and CPL pins. A ceramic capacitor with an effective capacitance value of 0.22µF allows a maximum load current of 28mA. The capacitor (C3) with the smaller effective capacitance value causes the greater the drop in VCP pin voltage at the same load. Select a capacitor (C3) that is appropriate for your external MOSFET, PWM frequency, and VCP pin voltage. The load current (I_{VCP}) to drive the external MOSFET can be estimated by ***EQ 5-16.*** Note that the load current (I_{VCP}) increases if there are multiple phases operating PWM simultaneously in a 3-phase or 2-phase PWM drive.

EQ 5-16

$$I_{VCP} > N \times Q_g \times f_{PWM}$$

where N: number of simultaneous PWM phases, Q_g: external MOSFET gate input total charge, f_{PWM}: PWM frequency.

A ceramic capacitor with an effective capacitance value of at least 1µF is required between the VCP pin and the VBRIDGE pin as the output capacitor (C2). The output capacitor (C2) should be 5 times larger than the pumping capacitor (C3) considering the output ripple voltage due to charge pump operation.

5.1.5 External MOSFETs (M1 to M6) and Register Settings

5.1.5.1 ISRC_HS and ISRC_LS Bits Setting

The gate drive source (charge) currents (I_{SRCH}, I_{SRCL}) are adjusted by the ISRC_HS and ISRC_LS bits respectively based on the gate-to-drain charge (Q_{gd}) of the external MOSFETs, and the target rise and fall times (t_{RISE}, t_{FALL}) of the half-bridge gate driver output. If the gate drive source currents (I_{SRCH}, I_{SRCL}) set for the external MOSFETs are small, the gate-to-source voltage (V_{GS}) of the external MOSFET may not be fully charged within the maximum gate transition time (t_{GT}) set by the T_GT bit, causing a V_{GS} fault (VGS_FAULT) to be detected or an on-resistance power loss. In addition, slow rise and fall times increase the switching power loss. Set the ISRC_HS and ISRC_LS bits appropriately according to the actual application including the external MOSFET and the motor. Using the gate-to-drain charge (Q_{gd}) of the external MOSFET and the target rise time (t_{RISE}) of the half-bridge gate driver output, the gate drive source current (I_{SRCH}) is calculated using ***EQ 5-17***.

EQ 5-17

$$I_{SRCH} > \frac{Q_{gd}}{t_{RISE}}$$

where Q_{gd}: external MOSFET gate-to-drain charge, t_{RISE}: target rise time.

The gate-drive sink (discharge) currents (I_{SNKH}, I_{SNKL}) are set to twice the gate-drive source currents (I_{SRCH}, I_{SRCL}). The target rise and fall time (t_{RISE}, t_{FALL}) should be set appropriately considering these characteristics.

5.1.5.2 DEAD_TIME Bit Setting

The adaptive dead-time function monitors the gate voltage of an external MOSFET during the turn-off transition, detects that the gate-to-source voltage (V_{GS}) falls below a threshold voltage (1V typ.), and then turns on the complementary MOSFET after an extra dead-time (t_{DT}) has elapsed. This function prevents the simultaneous turn-on of high-side and low-side external MOSFETs resulting shoot through and optimizes the diode power loss due to the dead time. The extra dead time (t_{DT}) can be adjusted by the DEAD_TIME bit. The value of the DEAD_TIME bit should be adjusted to ensure that the gate-source voltage (V_{GS}) after the extra dead time (t_{DT}) is less than the gate threshold voltage (V_{TH}), considering the gate-source charge (Q_{gs}) (at V_{GS} = 1V) and gate threshold voltage (V_{TH}) of the external MOSFET.
It is a recommended procedure to optimize the margin between the timing at which the gate-source voltage (V_{GS}) of the one-side external MOSFET falls a threshold voltage (1V typ.) and the turn-on timing of the complementary MOSFET. To prevent external MOSFET breakdown, set the DEAD_TIME bit from “11b” to smaller value gradually with monitoring the gate-source voltage (V_{GS}) of external MOSFETs.

5.1.5.3 T_GT Bit Setting

For half-bridge output switching characteristics optimized by adjusting the ISRC_HS and ISRC_LS bits, set the T_GT bit so that the maximum gate transition time (t_{GT}) is longer than the time required to complete charging the gate-to-source voltage (V_{GS}) of the external MOSFET. A sufficiently long maximum gate transition time (t_{GT}) has no effect on the switching characteristics of the half-bridge outputs, but an optimal maximum gate transition time (t_{GT}) provides low power consumption of gate driver in PWM operation.
It is a recommended procedure to optimize the margin between the timing to complete charging the gate-source voltage (V_{GS}) of the external MOSFET and the timing to complete the maximum gate transition time (t_{GT}). To prevent unintended detection of a V_{GS} fault (VGS_FAULT), set the T_GT bit from “11b” to smaller value gradually with monitoring the gate-source voltage (V_{GS}) of external MOSFETs.

5.1.6 Current Sensing Shunt Resistors (R1, R2, R3) and Differential Amplifier Gain

In this device, the motor drive current can be detected by measuring the differential voltage across the shunt resistor for current sensing (now referred to as “shunt resistor”) with the A/D converter of the MCU via a differential amplifier. The shunt resistor (Rz (z = 1, 2, 3)) is selected based on ***Figure 5-5***, ***EQ 5-18*** and ***EQ 5-20*** using the target current sensing range (I_{SNS}), supply voltage (V_{DD}), differential amplifier output range (V_{O_CSA}), input offset voltage (V_{IO_CSA}), and gain (G_{CSA}).

EQ 5-18

$$V_{O\_DM} = (V_{DD} - V_{O\_CSA}) - (0.5 \times V_{DD} + G_{CSA} \times V_{IO\_CSA})$$

For diffrential amplifier gain G_{CSA} = 20V/V, it becomes ***EQ 5-19***.

EQ 5-19

$$V_{O\_DM} = (3.3V - 0.4V) - (1.65V + 20 \times 5mV) = 1.15V$$

The shunt resistor Rz (z = 1, 2, 3) that can operate within the output dynamic range (V_{O_DM}) is calculated using ***EQ 5-20***.

EQ 5-20

$$R_z < \frac{V_{O\_DM}}{G_{CSA} \times I_{SNS}}$$

For a target current sensing range (I_{SNS}) = 50A, it becomes ***EQ 5-21***.

EQ 5-21

$$R_z < \frac{1.15V}{20 \times 50A} = 1.15m\Omega$$

If Rz = 1mΩ is selected, the power dissipation (P_{SNS}) of the shunt resistor Rz (z = 1, 2, 3) becomes ***EQ 5-22***, using the effective value of the target current sensing range (I_{SNS_RMS}).

EQ 5-22

$$P_{SNS} = I_{SNS\_RMS}^2 \times R_z = 35.4A^2 \times 1m\Omega = 1.25W$$

Please also select the shunt resistor Rz (z = 1, 2, 3) with consideration of the power rating of the component.

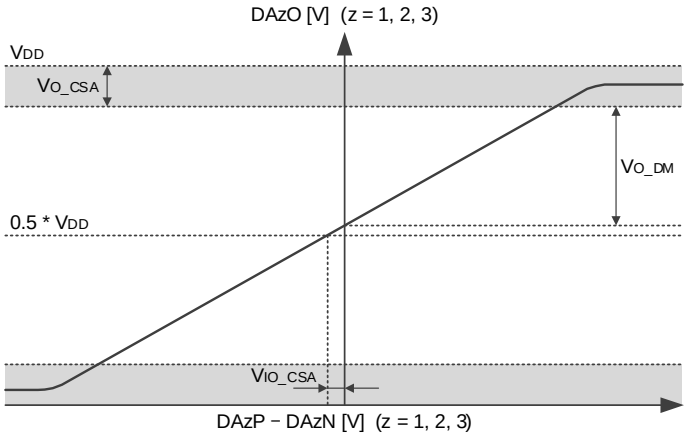


Figure 5-5 **Output Dynamic Range of Current Sensing**

5.1.7 External Protection Circuit Example

5.1.7.1 Phase Voltage Clamp Circuit with Resistor and Diode

Dead time is necessary to prevent shoot-through current generated by the simultaneous turning on of the high-side and low-side external MOSFETs during motor drive. When sourcing current to the motor, the motor drive current flows through the body diode of the low-side external MOSFET until the low-side external MOSFET is turned on after the high-side external MOSFET is turned off by the complementary PWM operation, but a negative voltage spike may occur at the timing of the falling edge on the bridge output.
In this device, the allowable negative voltage level is specified as the absolute maximum ratings of the HSx (x = A, B, C) pins. These ratings are $VHSx_{abs}$ (x = A, B, C) = -5V for continuous time and $VHSx_{tran}$ (x = A, B, C) = -7V. for transient within 200ns. Negative voltage spikes exceeding the absolute maximum ratings may cause product failure and must be protected by an external circuit.
The magnitude of negative voltage spikes depends on various factors such as operating supply voltage, dead time, transition time of the half-bridge output, external MOSFETs, shunt resistors, and motors, as well as board layout. To avoid negative voltage spikes exceeding the absolute maximum rating during the switching period of the half-bridge output, an external clamping circuit with resistors and diodes may be required.
Figure 5-6 shows an example circuit. The resistors (R_{Sx} (x = A, B, C)) are inserted in the gate drive sink (discharge) current path of the high-side external MOSFET, thus affecting the fall time of the half-bridge output and the gate voltage monitoring of the adaptive dead-time function.
Resistors (R_{Sx} (x = A, B, C)) should be selected to be 10Ω or less, and their effects as well as side effects should be checked with actual waveforms. Resistors (R_{Sx} (x = A, B, C)) and diodes (D_{SxN} (x = A, B, C)) should be placed as close as possible to this device in the board layout design.
A positive voltage spike exceeding the absolute maximum ratings may also occur at the timing of the rising edge on the bridge output when sinking current from the motor. Consider adding diodes (D_{SxP} (x = A, B, C)) for protection of positive voltage spikes if necessary.

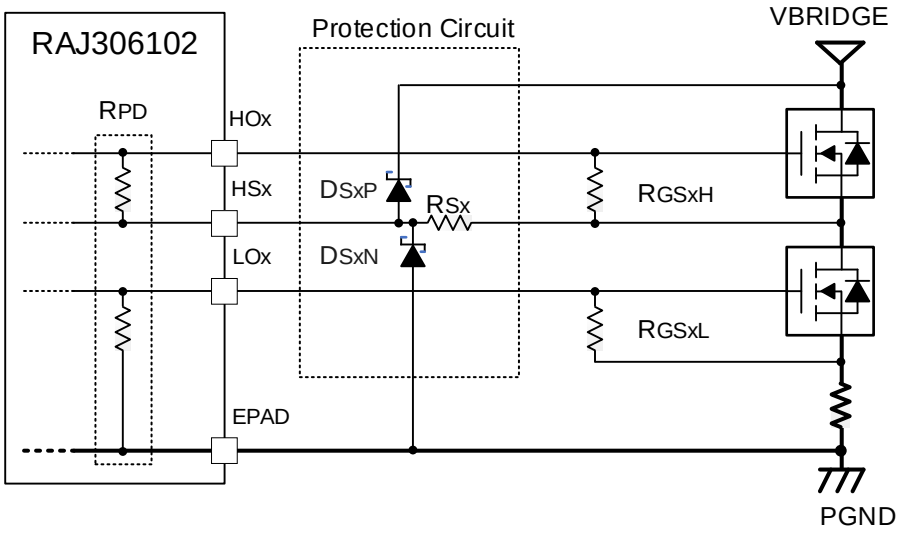


Figure 5-6 Example of Phase Voltage Clamp Circuit with 6 Resistors and Diodes (RSx, DSxP, DSxN (x = A, B, C))

5.1.7.2 Gate-Source Pull-down Resistors for External MOSFETs

This device has built-in pull-down resistors (R_{PD} = 200kΩ typ.) between the HOx and HSx (x = A, B, C) pins and between the LOx (x = A, B, C) and EPAD. After the EN output port is set to Low or a fault is detected, HOx and LOx (x = A, B, C) pins of the gate driver output become Hi-Z. These pull-down resistors (R_{PD}) discharge the gate-to-source voltage (V_{GS}) of external MOSFETs. For some fault detections related to external MOSFETs, the PDMODE bit can be used to select an operation that sets the gate driver to Low output. When an external MOSFET with a large input gate capacitance is used, the discharge time of gate-to-source voltage (V_{GS}) becomes longer. Then external pull-down resistors (R_{GSxH}, R_{GSxL} (x = A, B, C)) should be added as shown in ***Figure 5-7***.

Depending on the slew rate of the external MOSFETs power supply (VBRIDGE) at power-on, the gate voltage may rise due to the charging current of the gate-to-drain capacitance (C_{gd}) of the external MOSFET, causing a shoot-through current. However, while the external MOSFET is on, the HOx and LOx (x = A, B, C) pins at the output of the gate driver are High, which causes current to flow through the pull-down resistor and increases current consumption. Consider adding external pull-down resistors (R_{GSxH}, R_{GSxL} (x = A, B, C)) if necessary. The appropriate resistance value should be considered the discharge time, gate voltage rise, and current consumption corresponding to the operating conditions.

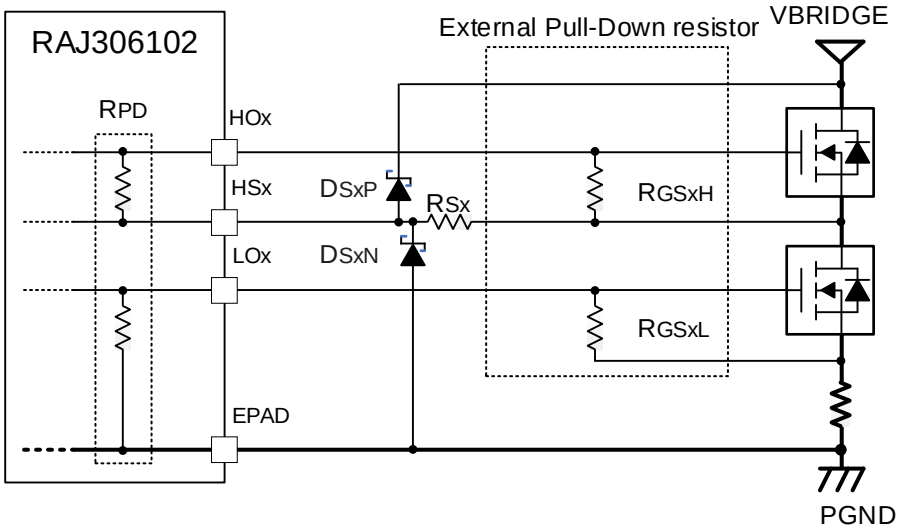


Figure 5-7 Gate-Source Pull-Down Resistors for External MOSFETs (RGSxH, RGSxL (x = A, B, C))

5.2 Board Layout Recommendations

In motor drive applications, a well-considered board layout is important for highly accurate analog signal detection, such as shunt current sensing signals and A/D converter input signals. Since motor drive applications including this device have a buck switching regulator that switches at high voltage and a gate driver that drives an external MOSFETs, pay attention to the classification of GND wiring, placement of external components, and wiring routing. The followings are guidelines of each item for board layout. For the countermeasure against noise of RL78/G1F, refer to "***Application Note: Notes and Countermeasures Against Noise for the RL78 Family (R01AN0839)***".

5.2.1 GND Nets

This device uses four GND pins: EPAD, PGND, AGND, and GND_MCU. ***Table 5-3*** shows the blocks using each GND pin.

Table 5-3 Relationship Between 3 GND Nets and Related Blocks

GND	Block
EPAD	Gate driver, Charge pump
PGND	Gate driver
AGND	Differential amplifier, BEMF sense amplifier, General-purpose comparator, LDO, Buck switching regulator control block, Control logic block
GND_MCU	RL78/G1F

Considering the above the GND separation in this device, it is recommended that the GND wiring be divided into 3 GND nets, which consist of PGND net (EPAD, PGND), AGND (AGND, GND_MCU), and REG_GND net. The REG_GND net is defined as the GND of the external components through which the switching current of the buck switching regulator flows. In addition, to avoid noise interference between GNDs, the common impedance with the GND planes of other GND nets should be as small as possible. The followings are precautions for each GND net wiring.

PGND Net

The PGND net is a GND plane that carries the gate discharge current of the external MOSFET associated with the switching of the half bridge. It is recommended that the PGND net be wired in a single layer without vias. The PGND pin and EPAD should be connected near this device without vias. If the wiring of PGND net in a single layer is difficult, connect the layers of the board with many vias to minimize parasitic inductance. Also, separate the wiring from the vicinity of the GND connector on the board (GND of the system) so that there is no common impedance with the GND on the half-bridge side. Since the peak gate discharge current exceeds 1A depending on the external MOSFET used and its switching characteristics (depending on the ISRC_LS bit), ensure that the wiring width is sufficient for the actual application. It is recommended that external components and circuits referenced to the PGND net be adequately covered by the GND plane of the PGND net to avoid noise effects on other blocks.

Since the EPAD is also used for heat dissipation of this device, it is recommended that EPAD be connected by a sufficient number of vias to allow heat dissipation to the rear of the board.

AGND Net

The AGND net is the reference GND plane for the built-in analog circuitry and the MCU (RL78/G1F). Therefore, it is important that the layout of the AGND net is designed to minimize the noise interference. The minimal overlap with the GND plane of other GND nets and with noisy power supply planes such as VM, VBRIDGE, and half-bridge power supplies is recommended. It is also recommended that external components and circuits referenced to the AGND net be adequately covered by the GND plane of the AGND net. The AGND net is used as a shield against wiring of high-precision analog signals such as shunt current sensing signals and A/D converter input signals.

REG_GND Net

The REG_GND net is the GND for external components through which the switching current of the buck switching regulator flows. To design a board layout that considers the noise countermeasure associated with the switching current of the buck switching regulator is one of the most important design items in applications that include switching power supplies. Since the switching current path changes depending on whether the switching element is on or off, it is recommended that a dedicated GND net (REG_GND) be provided for the GND of external capacitors (C1a, C1b), Schottky diode (D1), and output capacitor (C4) on the VDRV pin. It is important to place the GNDs of these components as close as possible to minimize noise due to parasitic inductance. Even if it is not possible to shorten the distance between the GNDs of external components, this wiring should be directly connected in a single layer.

The wiring from external components GND to the GND connector on the board (GND of the system) should be connected through vias to separate the REG_GND net from other GND nets. It is recommended that these vias be placed near the output capacitor (C4), where there is little current variation due to switching. It is also recommended that the external components and circuits of the buck switching regulator be sufficiently covered by a plane of the REG_GND net on a separate layer to suppress noise interference. Note that this plane must also be connected to the GND connector on the board (GND of the system) through a via to separate it from other GND nets.

5.2.2 Capacitors and Wirings for Power Supply Pins

This device has the following eight power supply pins, including the built-in regulator output pin. ***Table 5-4*** lists the bypass capacitors or output capacitors connected to each power supply pin, and the blocks using each pin. It is recommended that these capacitors be placed as close to this device as possible and be connected to this device in a single layer with low impedance without vias. The VM and VBRIDGE pins should be wired from near the power supply connector on the board (power supply of the system) where the voltage is relatively stable on the board, with consideration of the voltage drop. The followings are precautions to be considered when wiring power supplies, including half-bridge power supplies.

Table 5-4 Power Supply Pin Capacitors and Power Supply Destination Block

Power Supply Pins	Part No.	Power Supply Destination Blocks
VM – REG_GND	C1a, C1b	Buck switching regulator, LDO1
VBRIDGE – PGND	C1c, C1d	Gate driver
VCP – VBRIDGE	C2	Gate driver
VDRV – REG_GND	C4	Gate driver, LDO2, LDO3
VCC5V – AGND	C7	Differential amplifier, BEMF sense amplifier, General-purpose comparator, Buck switching regulator control block, Control logic block
VDD – AGND	C8	Differential amplifier, BEMF sense amplifier, General-purpose comparator
VDD_MCU, REGC – AGND	C11, C12	RL78/G1F

VM Pin Wiring

Like the wiring of REG_GND net, wiring to the power supply connector on the board (power supply of the system) is recommended to be connected on a separate layer with vias near the VM pin bypass capacitors (C1a, C1b). The purpose is to have the bypass capacitors (C1a, C1b) absorb the abrupt current changes that occur in the buck switching regulator as much as possible. The VM pin wiring should be independently connected to the power supply connector on the board even if it is used at the same potential as the VBRIDGE pin.

Half-bridge Power Supply, VBRIDGE Pin Wiring

To bypass the high current path of the external MOSFETs, electrolytic capacitors are usually added. These electrolytic capacitors are placed so that the length of the high current path through the external MOSFETs is minimized, considering the placement of the external MOSFETs and shunt resistors. Wiring should be designed to minimize parasitic inductance, with sufficient wiring width and enough vias connecting between layers of the board according to the actual application. Wiring to the bypass capacitors (C1c, C1d) at the VBRIDGE pin should be independent from the electrolytic capacitor terminals to minimize the common impedance with the high current path.

5.2.3 Buck Switching Regulator

The most important aspect of the board layout for the buck switching regulator is the minimization of noise generated by the switching regulator. As shown in ***Figure 5-8***, the buck switching regulator changes the switching current flow path according to the (1) the switching element (MP1) on, (2) MP1 off, and (3) MP1 transition process from off to on, and the steep current change at the switch timing of MP1 generates noise. To minimize this noise, it is required to minimize the area of the current loop in (3) shown in ***Figure 5-8***. The followings are some points to be considered for minimizing the area of the current loop in (3). It is very important to connect the wiring between the external components of the buck switching regulator in a single layer without vias to minimize noise.

- Place VM pin capacitors (C1a, C1b) and Schottky diode (D1) as close as possible to this device and keep wiring between the elements and this device pins as short as possible.
- Make the REG_GND wiring between VM pin capacitors (C1a, C1b) and Schottky diode (D1) as short as possible.
- Also, consider the following precautions when implementing the board layout.
- Design the board layout so that the area of the current loop in (1) composed of the inductor (L1), output capacitor (C4), and Schottky diode (D1) is small.
- The wiring between the SW1 pin and the inductor (L1), and the REG_GND wiring between the Schottky diode (D1) and the output capacitor (C4) should be as short as possible, giving priority to the board layout for (3), because current flows continuously in the conditions (1) and (2).
- The wiring area (length and width) between the SW1 pin and the inductor (L1) should be small to the extent that it does not interfere with the current capacity and the heat generated by the inductor (L1).
- The wiring to VDRV pin should be wired from the land of the output capacitor (C4), not between the inductor (L1) and the output capacitor (C4).

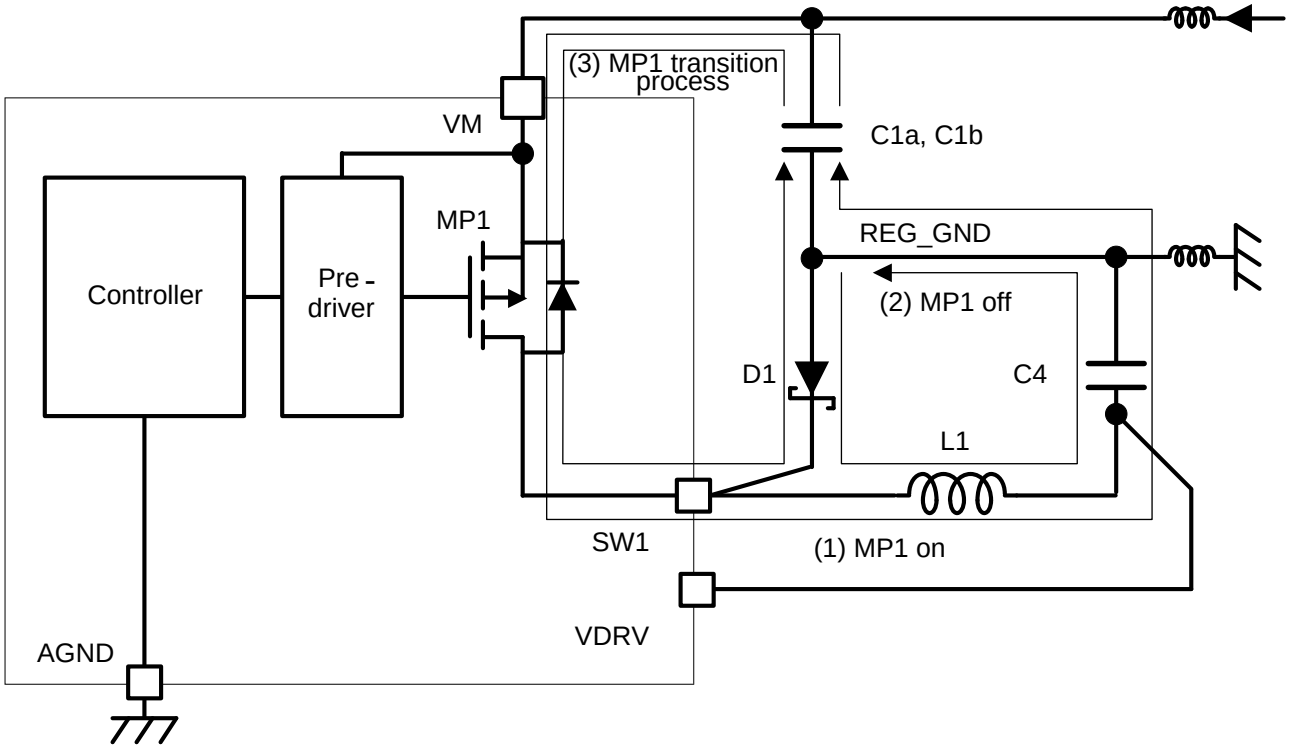


Figure 5-8 Current Path of the Buck Switching Regulator

5.2.4 N-ch MOSFET Bridge

The placing and wiring of the external MOSFETs should be considered to minimize the gate current loop that controls the on/off of the external MOSFETs. For high-side MOSFETs, it is recommended that the wiring from the MOSFETs gate to HOx (x = A, B, C) and from HSx (x = A, B, C) to the external MOSFETs source be shortened and parallel wiring. For low-side external MOSFETs, it is recommended that the wiring from the gate of the MOSFET to LOx (x = A, B, C) and from EPAD to the GND side of the shunt resistors be shortened and parallel wiring.
Note that the gate-drive sink (discharge) currents (I_{SNKH}, I_{SNKL}) exceed 1A depending on the external MOSFET used and the switching characteristics (ISRC_HS, ISRC_LS bit dependent). Ensure sufficient wiring width considering the peak current for the actual application. In addition, to avoid mismatch with respect to the propagation delay of the half-bridge output, the placing and wiring of external components in each phase should be as symmetrical as possible.

5.2.5 Charge Pump

Place the pumping capacitor (C3) and the output capacitor (C2) of the charge pump as close to this device as possible, and make the loop caused by the wirings of CPH and CPL to the C3 as small as possible. The loop caused by the wirings of VCP and VBRIDGE to C2 should be as small as possible. Since these wirings are subject to large current variations during charging and pumping operations, it is recommended that they be connected in a single layer without vias. Note that the wiring loop to C3 and the wiring loop to C2 should be sufficiently covered by a GND plane in the PGND net.

5.2.6 Shunt Current Sensing

For current sensing by the shunt resistors (R1, R2, R3), it is recommended that the wirings be used Kelvin connections and connected to the differential amplifier input DAzP and DAzN (z = 1, 2, 3) pins with parallel and equal length to accurately detect the differential voltages across the shunt resistors. To avoid noise interference to the differential wirings, it is also recommended to provide shields on both sides, upper, and lower layers of the AGND net. It is recommended that wirings be done as far away from noise sources such as the wirings of power supply and Hall IC output as possible. An R-C filter can be inserted just before the differential input DAzP and DAzN (z = 1, 2, 3) pins for the purpose of noise reduction, but these pins have an input impedance of 10kΩ, so use a resistor of 20Ω or less to prevent gain errors. Also, when inserting R-C filters, select an appropriate cut-off frequency by fully considering the timing of the signals to be detected and the delay time due to the R-C filter.

Chapter 6 Precautions for Use

6.1 High Temperature Operation

The following operating temperature profile is assumed for the usage of this device. Please take the use within this profile into consideration.

High ambient temperature environment 1: 85°C < Ta ≤ 125°C, 1.0 hr/day
High ambient temperature environment 2: 55°C < Ta ≤ 85°C, 4.0 hrs/day
Not high ambient temperature environment: -40°C ≤ Ta ≤ 55°C, 19.0 hrs/day

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